CHAPTER 9

OPERATING PRINCIPLES OF A REPRESENTATIVE SSB TRANSCEIVER, AN/URC-32 (PART II)

INTRODUCTION

This chapter describes the operation of the frequency generator, frequency comparator, and power amplifier of the Radio Set AN/URC-32 single-sideband transceiver. The discussion of the dynamic handset, handset adapter, audio and control unit, sideband generator, and c-w and fsk unit is given in chapter 8 of this training course.

In the discussion in chapter 8, the methods of producing the various input signals (voice, c-w, and fsk) for the transmit operation are considered, along with the methods used to produce the upper and lower single sideband carrier signals. The processes of i-f amplification, detection, and audio amplification of the received signals are also considered.

In this chapter, we will consider the process by which the i-f signal from the balanced modulators of the sideband generator is converted to an r-f signal during transmission, and how the r-f incoming signal is converted to an i-f signal during receive operation. The 100-kc reference oscillator and 100-kc frequency correction circuits also are considered.

FREQUENCY GENERATOR

The frequency generator is shown in figure 9-1. It is an important part of the transceiver (fig. 9-2, A). The band change and frequency change controls on the front panel of the frequency generator determine the frequency to which the unit is tuned.

The frequency generator (fig. 9-2, B) consists of a main chassis and five plug-in units. These units include the:

1. R-f tuner
2. Stabilized master oscillator
3. Sidestep oscillator (optional)
4. Frequency divider
5. Reference oscillator or isolation amplifier

R-F TUNER BLOCK DIAGRAM

The r-f tuner of the frequency generator (fig. 9-2, C) is an i-f to r-f translator during transmit condition, and an r-f to i-f translator during receive condition. During the transmit condition, the r-f tuner accepts the 300-kc single-sideband signal from the balanced modulators of the sideband generator (ch. 8, fig. 8-13) and translates it to any desired frequency (in 1-kc steps) ranging from 2.0 to 30.0 mc.

During receive condition, the r-f tuner (fig. 9-2) accepts the selected received signal (as indicated on the band dial of fig. 9-1) and translates it to a 300-kc i-f signal. This signal is fed to the i-f/a-f amplifier of the sideband generator (or a-m/i-f amplifier depending on the type of reception) for demodulation and amplification as discussed in chapter 8.

The r-f tuner is tunable through its normal operating range (2.0 to 30.0 mc) in four bands. These bands are:

Band 1—1.7 to 3.7 mc
Band 2—3.7 to 7.7 mc
Band 3—7.7 to 15.7 mc
Band 4—15.7 to 31.7 mc

The r-f tuner can be tuned in 1-kc steps over the entire tuning range.

During transmit and receive conditions on band 1, the r-f tuner performs a single frequency conversion. The heterodyning process takes place in V1A (fig. 9-2, C) for transmit and in V1B for receive. On bands 2, 3, and 4, the r-f tuner performs a double frequency conversion in either V3A or V3B.

On receive operation, the r-f input signal from the transmit-receive relay (at the antenna input) is fed through the keying relay, K2, to receiver r-f amplifier, V8. (K2 permits passage of the received signal during receive condition and applies an additional bias to cut off the stages of the receiver during transmit.) On

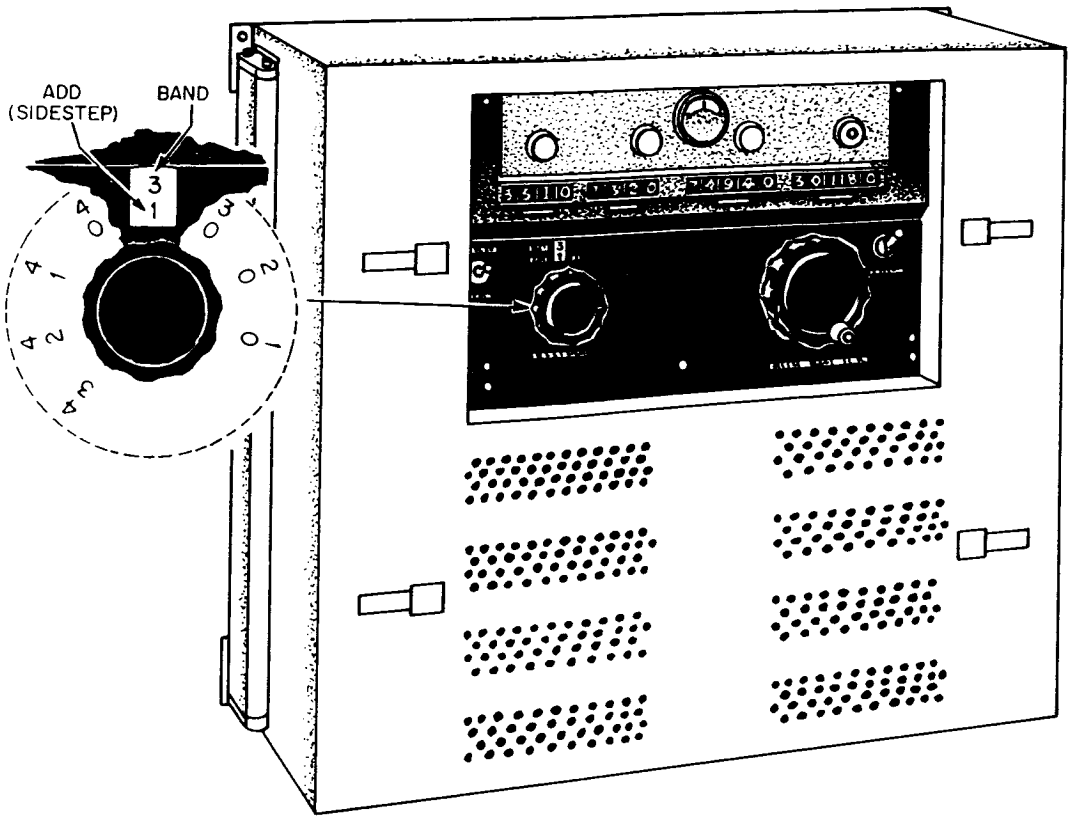

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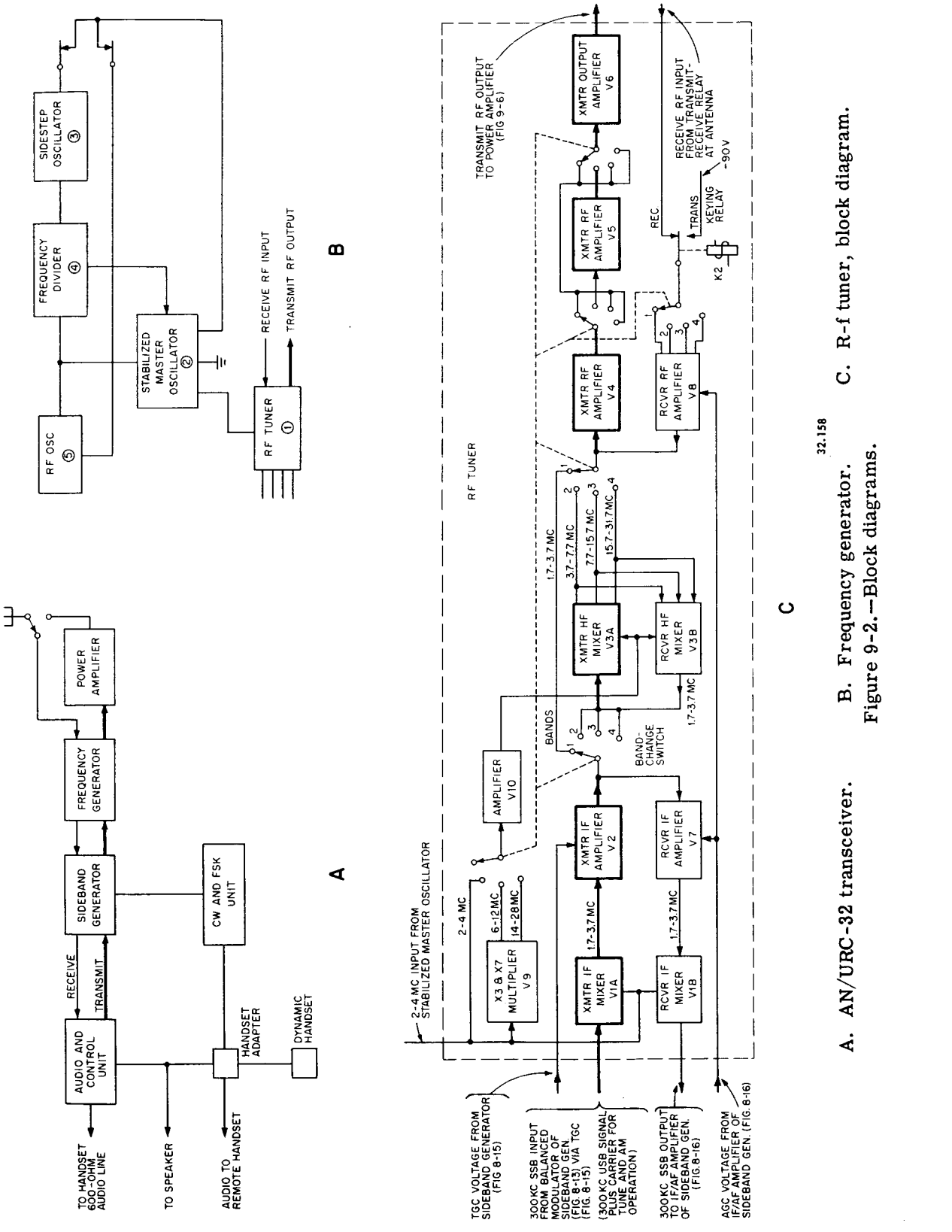
Figure 9-1.—Frequency generator.

bands 2, 3, and 4, the output of V8 is fed to receive h-f mixer, V3B, where it is converted to a 1.7 to 3.7 mc variable i-f signal.

On band 1, the output of V8 is in the 1.7 to 3.7 mc range, and is fed directly to receive i-f amplifier, V7. The 1.7 to 3.7 mc variable i-f signal (during receive operation) is amplified by receive i-f amplifier V7 and fed to receiver i-f mixer, V1B, where it is converted to a 300-kc fixed i-f signal. The V1B output is fed to the i-f/a-f amplifier of the sideband generator (ch. 8, fig. 8-16). An automatic gain control (agc) voltage from the sideband generator controls the gain of the receiver amplifiers, V7 and V8 (fig. 9-2, C).

On transmit operation, the 300-kc fixed i-f signal from the balanced modulators of the sideband generator is converted to a 1.7 to 3.7 mc variable i-f signal in transmit i-f mixer, V1A by mixing with a 2-4 mc signal from the stabilized master oscillator. The variable i-f signal is amplified by transmit i-f amplifier, V2. The gain of V2 is controlled by a tgc (transmit gain control) voltage from the tgc unit of the sideband generator (fig. 8-15). On band 1, the output of V2 (fig. 9-2, C) is fed through the band-change switch to the transmit r-f amplifier, V4.

During transmission on bands 2, 3, and 4, the output of V2 is fed through the band-change switch to the transmit h-f mixer, V3A, where it is converted to an r-f signal in the range of 3.7 to 31.7 mc, depending on the band selected. The transmit h-f mixer, V3A, is followed by three stages of r-f amplification on band 2, and by two stages of amplification on bands 1, 3, and 4. The necessity for greater amplification on band 2 is caused by losses in special tuned circuits used during transmission on this band. The output from V6, is fed to the power amplifier, V1 (fig. 9-6).



A. AN/URC-32 transceiver. B. Frequency generator. C. R-f tuner, block diagram.

Figure 9-2.—Block diagrams.

R-F TUNER, RECEIVE FUNCTION

The stages of the r-f tuner (fig. 9-3) are normally keyed to the receive condition by keying relay, K2. Another keying relay in the sideband generator (not shown) transfers the +130 volt power supply from either receive tubes to transmit tubes or vice versa, so that both do not function simultaneously. The received signal from the antenna is fed through contacts 7 and 2 of K2, through S1G, through one of the tuned circuits, Z14-Z17, through S1F, and through C48, to the control grid of receive r-f amplifier, V8. The amplified output at the V8 plate on band 1 is between 1.7 and 3.7 mc, and requires no further heterodyning to be accepted by subsequent stages of the receiver. Thus, on band 1, the V8 plate output is fed through S1E and S1B, developed across Z4, Z5, and Z6, and applied through C13 to the control grid of variable i-f amplifier, V7.

Bands 2, 3, and 4 receiver input frequencies (from 3.7 to 31.7 mc inclusive) require frequency conversion down to the 1.7 to 3.7 mc receiver variable i-f range. Thus, the V8 plate output on these bands is applied through S1E, the selected tuned circuits (Z7-Z13), through S1C, R57, and C109, to the grid of receive h-f mixer, V3B. On band 2, injection frequencies from amplifier, V10, via the T8 secondary and S1Q are applied to the V3B cathode. On band 3, multiplier, V9, is added. On band 4, the V10 output is applied via T9 to the V3B cathode. The injection frequencies are 2-4 mc for band 2, 6-12 mc for band 3, and 14-28 mc for band 4. A detailed explanation concerning the generation of the injection frequencies will be treated later in this chapter in the discussion of the stabilized master oscillator and the transmit function of the AN/URC-32.

By providing different injection frequencies to V3B for bands 2, 3, and 4, the V3B difference frequency plate output on all bands is always in the range from 1.7 to 3.7 mc. This signal is fed from the V3B plate through S1B (in the bands 2, 3, and 4 positions), developed across Z4, Z5, and Z6, and through C13, to the receive variable i-f amplifier, V7.

The 1.7 to 3.7 mc plate output is developed across Z1, Z2, and Z3 and coupled through C1 to the receiver i-f mixer, V1B. A 2- to 4-mc injection signal is applied to the cathode of V1B from the stabilized master oscillator (SMO, not shown) via T7 in Z25, and C94. The injection frequency changes in accordance with the input frequency to which the receiver is tuned so that the difference frequency at the plate of V1B is always 300 kc. This 300-kc signal contains the audio intelligence and is coupled via T2 to the i-f/a-f amplifier (ch. 8, fig. 8-16) during single sideband operation, or to the a-m i-f/a-f amplifier (fig. 8-19) during a-m reception.

The gain of the receiver variable i-f amplifier, V7 (fig. 9-3) and the receiver r-f amplifier, V8, is controlled by an agc voltage from the i-f/a-f amplifier (ch. 8, fig. 8-16). The gain of these stages and the i-f stages in the sideband generator is also controlled by a manually adjusted receiver r-f gain control (not shown). This control sets the threshold (cutoff) bias on the agc bus.

R-F TUNER, TRANSMIT FUNCTION

During transmit operation, the 300-kc modulated single-sideband i-f signal from either the upper or lower sideband balanced modulator (fig. 8-12) is fed through the tgc unit to input transformer, T1 (upper left, fig. 9-3) of the r-f tuner. T1 acts as an autotransformer to provide a voltage stepup in the signal path on bands 2, 3, and 4.

The 300-kc input signal at T1 is applied through S1A and R62 to the grid of V1A. An injection signal between 2 and 4 mc (depending on the operating frequency) is applied to the V1A cathode from the stabilized master oscillator (fig. 9-2, B), through the primary tuned circuit of Z25. Stage V1A operates as a subtractive mixer (difference frequency output) so that the 300-kc i-f input mixes with the 2 to 4 mc injection signal to produce a variable i-f output signal from V1A in the frequency range from 1.7 to 3.7 mc. The subtractive mixing in V1A inverts the sideband signals from the balanced modulators. This output is called a variable i-f signal, as the i-f output changes for each change in the injection frequency over the frequency band.

The V1A plate output is fed across three parallel tuned circuits, Z1, Z2, and Z3. The function of the triple-tuned circuits is to provide additional selectivity over that normally obtained from a single tuned circuit.

The 1.7 to 3.7 mc variable i-f signal from Z3 is coupled through C11 to the control grid of V2. The gain of V2 is controlled by the tgc voltage which is fed to the V2 variable mu control grid (via R3 and R21) from the tgc unit of the sideband generator (fig. 8-15). The tgc voltage is negative-going and proportional to the signal amplitude at the output stage of the transmitter. The action is similar to that of automatic gain control (agc) voltage used in

receivers, and prevents subsequent overdriving of the transmitter power amplifier on peak modulating signals.

During transmit operation on band 1, a frequency between 1.7 and 3.7 mc is to be transmitted. The V2 output frequency is always in this range so that no further heterodyning is necessary to produce any of the band 1 operating frequencies. Thus, on band 1, S1B and S1E bypass transmitter h-f mixer, V3A.

On bands 2, 3, and 4 (whose combined frequency ranges cover from 3.7 to 31.7 mc), S1B and S1E connect mixer, V3A in the signal path. The mixing action in V3A produces the desired carrier frequency.

On band 2 the heterodyne frequency for V3A is obtained by coupling the 2- to 4-mc signal from the T7 secondary through S1M (in the band 2 position), amplifying this signal in V10, and feeding the output from the T8 secondary through S1Q and C174 to the V3A cathode. Sections S1P and S1S connect all of the Z28 primary tuned circuit capacitors in parallel on band 2 to make the circuit capable of being tuned over the 2- to 4-mc range by the band change control.

Additive mixer, V3A, utilizes the sum frequency and operates only during transmit condition. The injection of the variable i-f signal of 1.7 to 3.7 mc at the V3A grid along with the 2 to 4 mc amplified SMO signal at the cathode results in an output of 3.7 to 7.7 mc at the plate for operation on band 2.

On band 3, the heterodyne frequency at the V3A cathode is obtained by multiplying the 2- to 4-mc input from the SMO three times (6-12 mc) in the V9 plate circuit. Inductor, L27, tunes the circuit over the 6.0- to 12.0-mc range. The V9 output is amplified in V10 and applied from the T8 secondary through S1Q (in the band 3 position) and through C174 to the V3A cathode. Capacitors, C137, C138, and the T8 primary tune the plate circuit for V10 on band 3. The V3A output is from 1.7+6 or 7.7 to 3.7+12 or 15.7 mc.

On band 4, the 2- to 4-mc input is multiplied 7 times in V9. The plate of V9 on band 4 is tuned by C129, C130, and L27. The Z26 tank is coupled to the plate tank by a capacitance of less than 1 mmf. The output signal between 14.0 and 28.0 mc is fed through S1M (in the band 4 position), and amplified in V10. The V10 plate circuit is tuned by Z29 and Z30. The output of Z30 (at the T9 secondary) is fed through S1Q and C174 to the V3A cathode. The mixing action in V3A on band 4 produces a 15.7 to 31.7 mc output at the V3A plate.

The output of V3A is amplified in V4 and developed across the selected plate tuned circuit (Z14, Z15, Z16, or Z17). The V4 output for bands 1, 3, and 4, is taken from Z14, Z16, or Z17, respectively, and applied through band switches S1H and S1I, and through current limiting resistor, R13, to the transmitter output amplifier, V6. On band 2, the output of V4 is amplified in transmitter r-f amplifier, V5. The V5 plate load includes three cascade connected parallel L-C tuned circuits (Z18, Z19, and Z20). The Z20 output is coupled through S1I and R13 to the V6 grid. The three tuned circuits provide additional selectivity in order to reject the second harmonic frequencies of the variable i-f and SMO signals which are within the band 2 frequencies (3.7 to 7.7 mc).

The output of V6 during single-sideband operation is a nominal 0.15 watt PEP (peak envelope power) signal which is fed through S1J, the selected plate tuned circuit (any one unit of Z21 through Z24), and S1K, to the power amplifier chassis (fig. 9-6).

POWER AMPLIFIER

The power amplifier is a two stage r-f power amplifier which amplifies the 0.15 watt PEP signal from the frequency generator to a nominal output power of 500 watts PEP. It contains a driver stage (V1-V2), a power amplifier stage (V3-V4), a tgc rectifier, a bias and filament supply, and the necessary control and interlock circuits.

The driver and power amplifier plate circuits are manually tuned through the frequency range of 1.7 to 31.7 mc in 4 bands. The power amplifier plate circuit uses a tuned pi network to obtain an unbalanced 50-ohm output impedance over the complete range of frequencies.

DRIVER STAGE

The output r-f signal from V6 (fig. 9-3) is fed through coaxial cable to r-f input jack, J1 (fig. 9-6). Resistor, R1 terminates the line in its characteristic impedance.

Driver tubes V1 and V2 are connected in parallel to increase the current carrying capabilities of the stage and to ensure conservative operation of the tubes. Parasitic suppressors, Z1 and Z2, reduce the generation of undesired frequencies.

The shunt-fed plate output tuned circuit of V1 and V2 comprises variable inductor, L4, and one of the capacitors C16, C17, or C18, in shunt with the input capacitance between the grid and

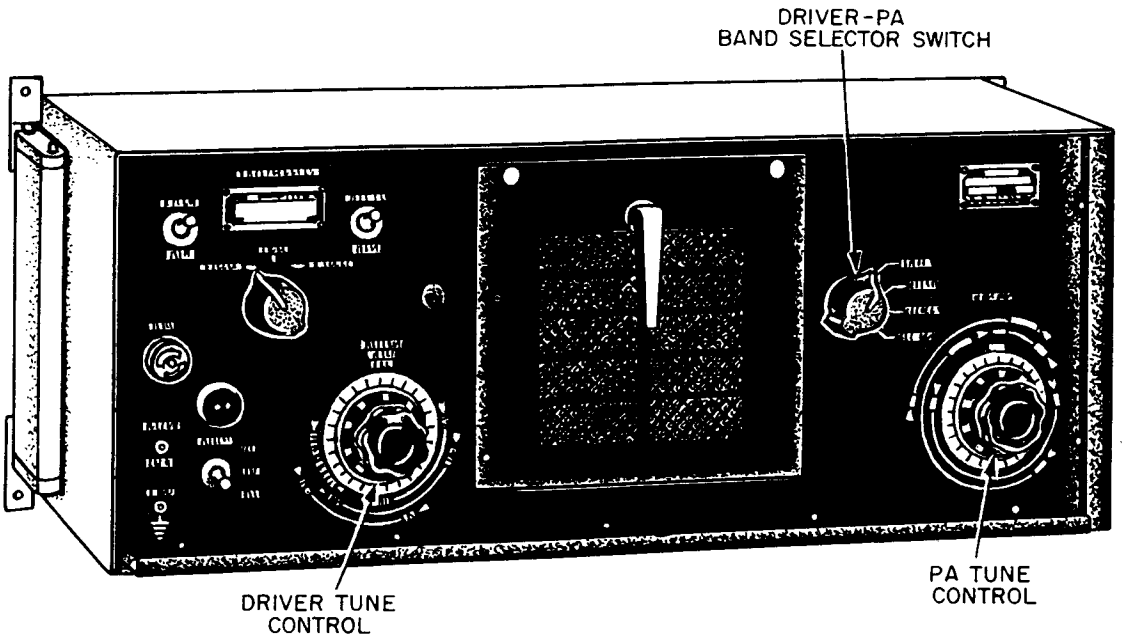


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Figure 9-4.—Power amplifier.

ground of the power amplifier stage. The driver plate tank is tuned to the desired operating frequency by the driver tune control on the PA front panel (fig. 9-4) which varies the inductance of L4 (fig. 9-6).

Driver-PA band selector switch, S4 (section S4A) selects the V1 and V2 driver plate tuning capacitance for operation on any of the four bands. The switch is shown in the band 1 position. On bands 2, 3, and 4, S4A connects one of the resistors, R28, R27, or R26, in parallel with the tuned circuit. This action reduces the Q of the circuit from that obtained on band 1 so that the V3 and V4 power amplifier grid driving voltage remains approximately equal on each of the four bands.

POWER AMPLIFIER STAGE

The power amplifier stage, V3 and V4, is parallel connected and uses two 4X250B tetrodes. Parasitic suppressors, R38 (in the grid input path) and Z3 and Z4 (in the plate circuits) suppress undesired oscillations.

The driver, V1 and V2, output from the C9-L4 junction is amplified in V3 and V4. On bands 1 and 2, L8 and L9 in series constitute the PA plate load inductance. For operation on bands 3 and 4, S4D closes (opposite to the position shown) to short L9.

Capacitor, C20 couples the 500-watt PEP output signal from the power amplifier to a pi network (low pass filter) consisting of C33, PA tune control, L10, C29, and any of the capacitors C21 through C28 as determined by the position of S4B. The C33 and C29 capacitances are used in the network on all bands. On band 1, driver-PA band selector switch, S4B, connects C21 to C28 inclusive in parallel with C33. On band 2, S4B removes C21 and C25 to C28 inclusive from the circuit. On band 3, S4B removes C23 and C24 in addition to those previously removed. On band 4, only C33 and C29 remain in the pi network. PA tune control, L10, tunes the pi network to the desired operating frequency within the selected band. With proper adjustment, the pi network presents a 50-ohm output impedance over all four bands.

Loading the transmitter is accomplished for each of the four bands by switching taps on L11, and by the selection of one of the capacitors C30, C31, or C32. Both the L and C selections are made by S4C. The loading network permits the transmitter output to be tuned over the entire 1.7 to 31.7 mc range with nearly constant output. Output power is delivered via r-f output jack, J2, to an antenna network (if used) or to the antenna.

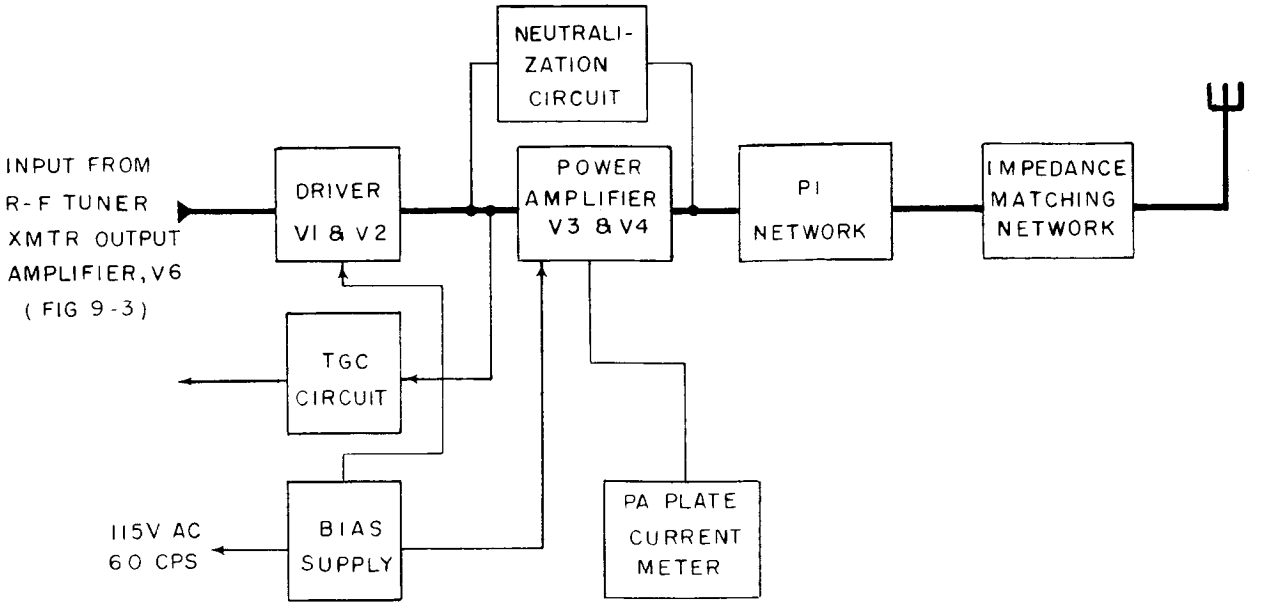


Figure 9-5.—Power amplifier, block diagram.

Neutralization

A bridge neutralization circuit is included in the power amplifier stage, V3 and V4, to balance out the feedback from plate to grid due to interelectrode capacitance of the tubes. Simplified diagrams of the neutralizing circuit are shown in figure 9-7.

The neutralizing feedback voltage is applied from the plates of V3 and V4 (fig. 9-7, A) to the grids of these tubes through C10, C8, and C12. These capacitors are lumped together as Cn in figure 9-7, B. The grid-plate interelectrode capacitance is represented as Cgp and Cgf represents the sum of the input capacitances to V3 and V4 which consists of the grid-cathode interelectrode capacitance and all stray capacitance. The combined capacitance, along with the driver tank inductance, L4, form the bridge circuit in figure 9-7, B.

The grid-plate capacitance, Cn, can be adjusted within limits for different amounts of feedback voltage. The Cn capacity is properly adjusted when Ecn = Ecgp. Since L4 is connected between diagonally opposite corners of the bridge, it follows that the bridge is balanced when Ecn/Ec15 = Ecgp/Ecgf. When this occurs, the r-f feedback potential to ground from both ends of L4 is equal and in-phase so that no feedback r-f voltage via Cn or Cgp is developed across L4. Only the output voltage across the L4 driver tank is applied to the V3-V4 grids.

Transmit Gain Control Circuit

The transmit gain control circuit (fig. 9-8) automatically adjusts the gain of the transmitter i-f amplifier, V2, in the r-f tuner (fig. 9-3) and of the tgc amplifier in the sideband generator (ch. 8, fig. 8-15). The tgc output (fig. 9-8) is a negative voltage which is applied to the grids of these stages. This action ensures that the driving signal to the power amplifier, V3 and V4 (fig. 9-6) will operate the power amplifier tubes at maximum capability but that it will not overdrive the tubes.

The tgc output voltage is obtained by rectifying a small portion of the driver (V1-V2) output signal which exists from the bottom of the driver plate tank to ground (across C15).

The amplitude of the driver plate tank input controls the amplitude of the tgc output. With no audio input, the driver plate tank signal is zero and the tgc bias across C51 comes from the PA bias supply.

With an audio input the amplitude of the driver plate tank voltage increases and C51 charges to a higher voltage. The C51 output is negative to ground and comprises the tgc signal.

POWER SUPPLY

Plate voltage for the power amplifier tubes, V3 and V4, is obtained from the +2000-volt high voltage supply (fig. 9-9, A) which utilizes eight

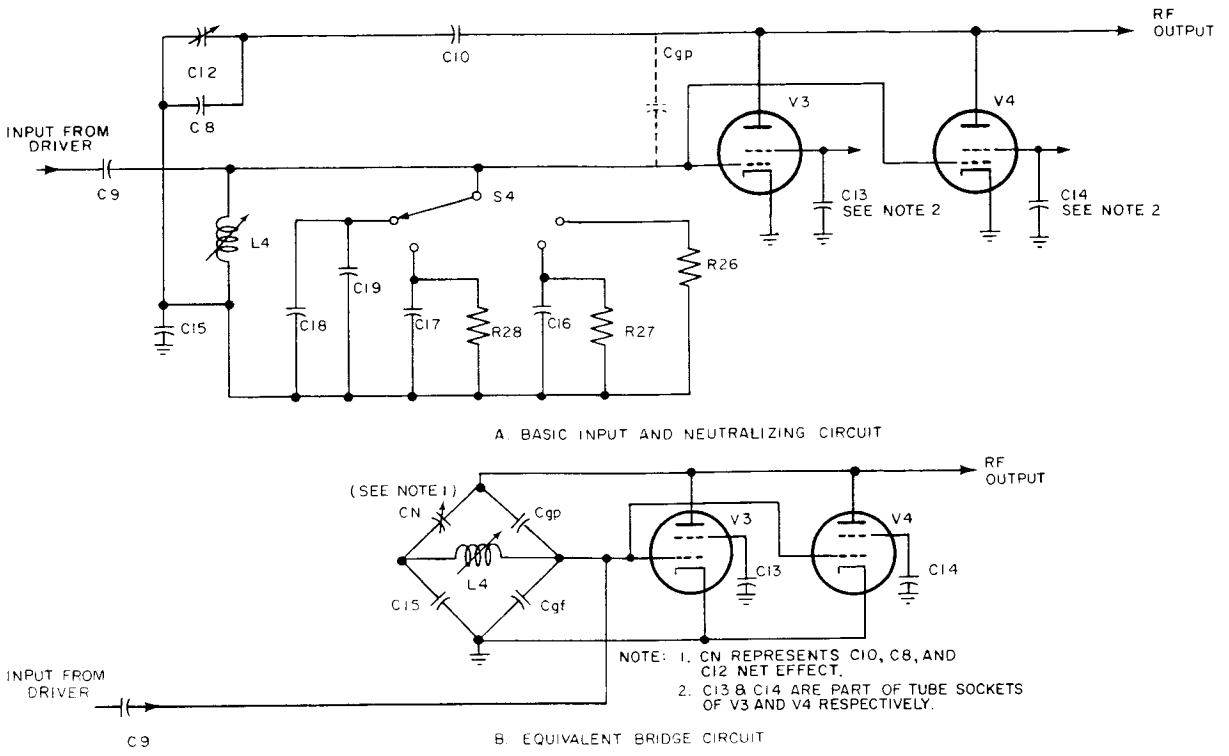


Figure 9-7.—Power amplifier neutralizing circuit, schematic diagram.

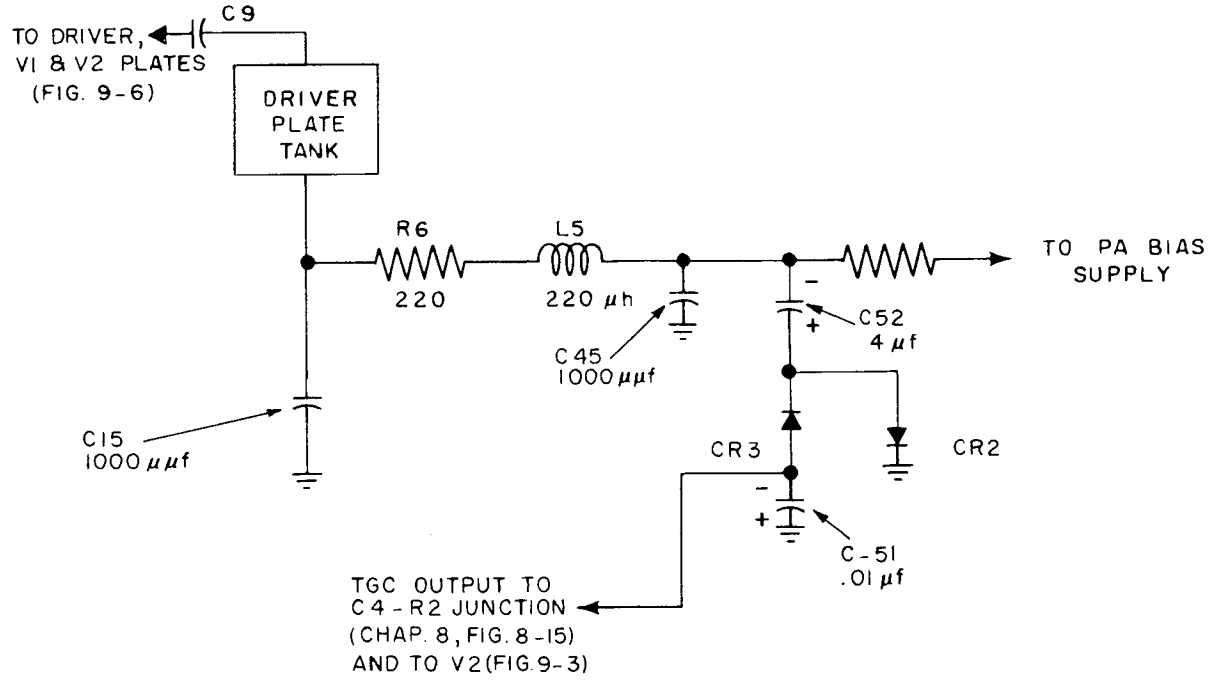
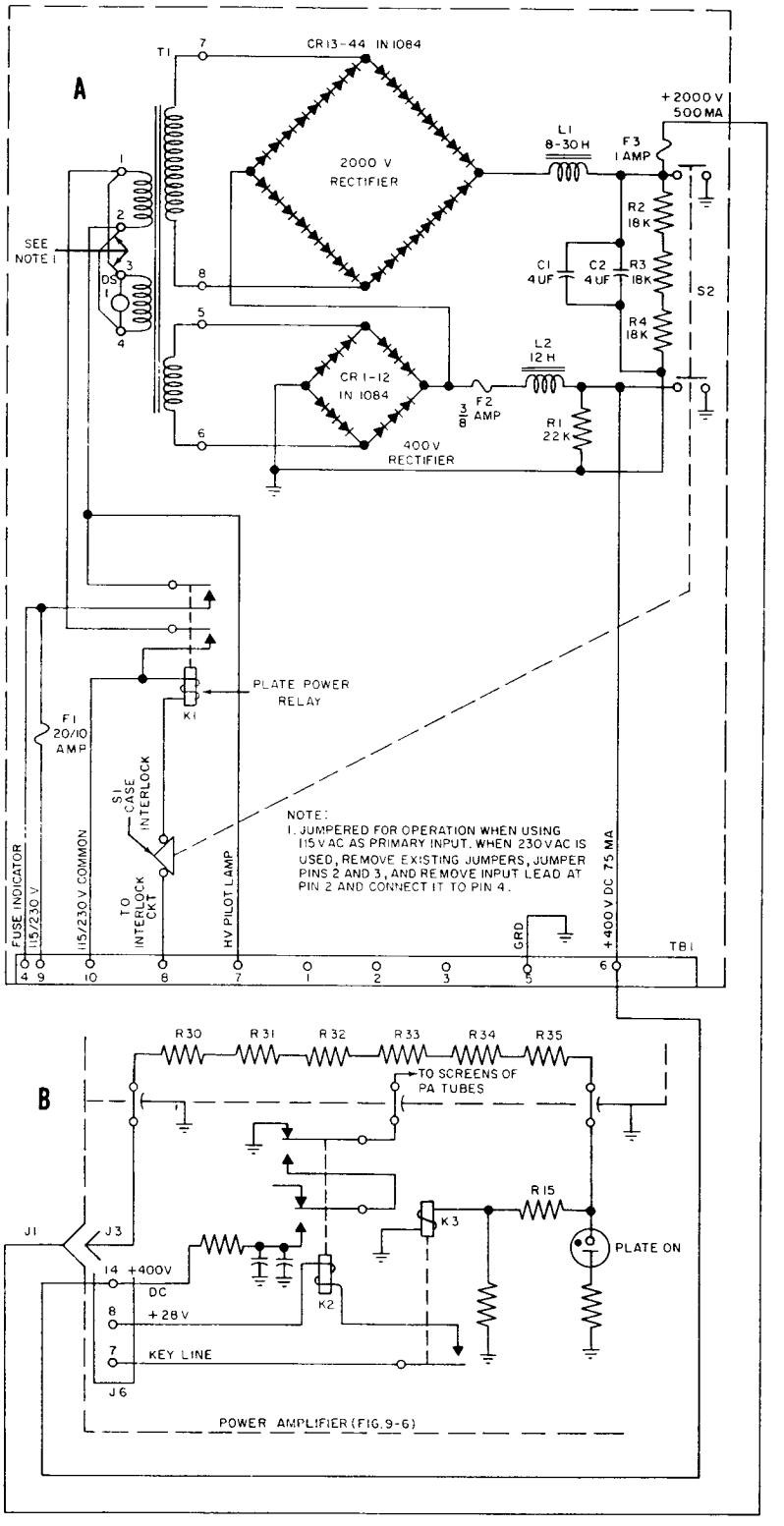


Figure 9-8.—Transmit gain control, schematic diagram.



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A. High voltage power supply. B. Control circuit.

Figure 9-9.—High voltage power supply and control circuit.

series connected silicon rectifiers in each leg of a bridge circuit. Silicon rectifiers operate efficiently at much higher temperatures than will selenium or germanium rectifiers. In addition, silicon rectifiers have less reverse (leakage) current which results in less power loss and less heat radiation in the power supply unit.

The high voltage power supply is connected as a conventional full-wave bridge rectifier circuit. Switch, S1, is a case interlock which operates S2 to the open position (as shown) when the high voltage power supply cabinet is closed. With S2 open, ground is removed from the output circuits and a rectified +400 volts is developed from the L2-R1 junction to ground. This potential is applied via terminal 6 of TB1, terminal 14 of J6 (fig. 9-6) through R16 (during TUNE operation only), and through the contacts of the keying relay, K2, to the plates and screens of the driver stage, V1 and V2, and to the screen grids of the power amplifier, V3 and V4. When energized, the K2 solenoid is connected between a +28 volts d-c and the key line. The relay operates only if the +400 volt relay, K3, is energized and the key line is completed to ground.

Relay, K3, is series connected in the +2000 volt bleeder circuit through R15, R35, through R30, J3, and J1 (fig. 9-9), so that K3 (fig. 9-6) energizes as soon as the +2000 volt output is available. If the transmitter key line is closed, K2 will also become energized. This action prevents possible damage to the transmitter power amplifier tubes (V3 and V4) by delaying the application of the screen voltage to these tubes until plate voltage is applied.

Section S1B (fig. 9-6) of fil-off-tune-operate switch, S1, is open in the TUNE position (as shown), and R16 is connected in series with the +400 volt input line. The voltage drop across R16 lowers the screen potentials of V1 through V4, and the plate potential of V1 and V2. This permits the operator to tune the transmitter at potentials which will not seriously damage the stages if the driving signals are weak.

When S1 is placed in the OPERATE position, R16 is shorted out through S1B and a tune-operate interlock (not shown) to the +400 volt supply. This action raises the driver screen and plate potentials and the power amplifier screen potential to the normal operating level.

A conventional type low voltage power supply (fig. 9-9, B) using semiconductor diode rectifiers from a common power transformer, supplies +250 volt d-c filtered at 37 ma, +130 volt d-c filtered at 315 ma, +28 volt d-c unfiltered at 1.5 ampere, +28 volt d-c partly filtered at 580 ma, +28 volt d-c regulated at 180 ma, -90 volt d-c filtered at 6 ma, and 12.6 volt-a-c at 5.2 amperes.

STABILIZED MASTER OSCILLATOR

In conventional a-m transmitters, the final output is obtained by multiplying the basic oscillator frequency in one or more stages. Special care must be taken to ensure that the multiplier stages operate at an exact harmonic frequency during tuning, and that the stages remain on frequency throughout the transmission.

In single-sideband transmitters, the final output is generally obtained by heterodyning in mixer stages. The sum frequency can be many times the original frequency and contain the same modulation components. To yield the desired output frequency, the injection frequency must be exact, and may be controlled automatically. This process is used in the transmitter section of the AN/URC-32.

The reference oscillator (fig. 9-10, A) is crystal-controlled and provides the basic reference frequency for all of the units of the transceiver. The frequency divider reduces the 100 kc reference oscillator output to a 1 kc signal which is rich in harmonic content, and contains a spectrum of frequencies separated by 1 kc. These frequencies are fed to the sidestep oscillator and used to produce the output injection frequencies to the SMO.

The injection frequency to the r-f tuner (fig. 9-3) is generated in master oscillator, V2 (fig. 9-10, B) in the SMO. The output frequency to the r-f tuner (at the output of the buffer amplifier, V1) is always in the 2- to 4-mc range. This signal is fed directly to the transmit and receive i-f mixers, V1A and V1B, in the r-f tuner on all bands.

The stabilized master oscillator consists of a master oscillator, V2, and a stabilizing loop which utilizes all of the remaining stages of the SMO block. The stabilizing loop operates in conjunction with the master oscillator to produce the injection frequencies for the r-f tuner on bands 3 and 4, and provides error correction for the master oscillator.

The master oscillator is a capacitance inductance-tuned oscillator that can be mechanically adjusted in 0.5-kc increments through the frequency range of 2 to 4 mc. It can be tuned to any one of 2000 1-kc r-f tuner channels in band 1 and any one of 4000 1-kc r-f tuner channels in band 2.

Bands 3 and 4 of the r-f tuner, containing 8,000 and 16,000 1-kc channels, respectively,

require the master oscillator to produce a greater number of injection frequencies than are possible with the mechanical positioning device. Generation of the additional increments is accomplished by mechanically positioning the master oscillator to the nearest lower 0.5-kc increment and then operating the stabilizing loop automatically to electronically position the master oscillator to the additional required increments.

Electronic tuning of the master oscillator is accomplished by varying the d-c component of current in a saturable reactor located in the tuning circuit of the oscillator. This process is described later. The master oscillator output frequency can be determined by the following formula:

$$F_{MO} = \frac{DIAL + ADD + 300}{BAND \quad MULT}$$

Where F_{MO} = the master oscillator frequency in kilocycles

DIAL = the frequency generator dial frequency

ADD = the ADD KC indication on the band change switch (fig. 9-1)

300 = the 300-kc fixed i-f subtracted in the r-f tuner i-f mixer

BAND MULT = multiplication of the master oscillator frequency in the r-f tuner

BAND 1 = 1
BAND 2 = 2
BAND 3 = 4
BAND 4 = 8

The master oscillator stabilizing loop electronically tunes the master oscillator to the desired frequency and phase locks it to the reference oscillator, thereby maintaining a master oscillator frequency accuracy and stability equal to that of the reference oscillator. This action is accomplished by comparing the master oscillator signal with the reference oscillator signal in a phase and frequency discriminator.

The stabilizing loop operates as follows: The 2- to 4-mc output of the master oscillator, V2, is multiplied by 8 (in CR1 thru CR4 and V3) and applied to a subtractive mixer, V4. This signal is heterodyned with a frequency in the range of 19.5 to 35.5 mc (selected in 100-kc increments) from the spectrum generator, V9. The multiplication of the oscillator output (F_1) in CR1 through CR4 and V3, and subsequent heterodyning of this signal with the spectrum generator 100-kc increment (F_{SG}) yields a frequency (F_2), equal to $F_{SG}-F_1$, and in the range of 3.4 to 3.5 mc over the entire range of the oscillator operating frequency.

The triggering signal for the 100-kc spectrum generator is obtained from the reference oscillator. The output of mixer, V4, is filtered in FL1 and applied to mixer, V5. This input is beat with a signal from the sidestep oscillator or the reference oscillator.

The oscillator injection in V5 is used to obtain the signal frequencies which control the phase and frequency discriminator. The difference frequency output of V5, between 1000 and 1104 kc, is filtered and applied to mixer, V6, where it is beat with a signal from the interpolation oscillator, V7. The interpolation oscillator, V7, which is tuned by the mechanically operated tuning shaft, supplies an injection signal which will produce a mixer (V6) difference frequency, F_4. This frequency is 455 kc plus the master oscillator error and the interpolation oscillator error.

The mixer, V6, output frequency (F_4) is filtered, amplified, and applied to the phase and frequency discriminator. Here F_4 is compared with a reference frequency (F_{REF}).

The reference frequency (F_{REF}) is generated by converting a 4-kc signal from the frequency divider to a 4-kc spectrum in the 1000- to 1100-kc frequency range and mixing it in V8 with the interpolation oscillator, V7, output. The reference frequency (F_{REF}) is equal to 455 kc plus the interpolation oscillator error. The interpolation error, which is present in both F_{REF} and F_4 is balanced out in the phase and frequency discriminator.

When F_4 (which contains the oscillator error) is exactly 455 kc, phase discrimination of F_{REF} and F_4 results in a tuning current output from the discriminator (f-m detector) which phase locks the master oscillator on frequency. In the phase locked condition, the master oscillator output frequency assumes the correct phase (Φ_{COR}) and in comparison with the reference phase (Φ_{REF}) produces an output which maintains equilibrium in the stabilizing loop and holds the master oscillator on frequency. Thus, in the phase locked condition, the master oscillator frequency (F_{MO}) tracks the reference frequency (F_{REF}) resulting in a master oscillator stability equal to the reference frequency stability.

During setup, the master oscillator frequency is incorrect, resulting in F_4 being above or below the reference frequency (F_{REF}) which is 455 kc. The resulting output of the frequency discriminator tunes the master oscillator to the proper frequency.

MASTER OSCILLATOR

The master oscillator, V2, of the SMO (fig. 9-11, A) is a modified Hartley oscillator which is followed by a buffer amplifier stage, V1 (not shown). The master oscillator and associated control circuits (referred to as the stabilized master oscillator) furnish the injection frequencies for the frequency conversion circuits of the r-f tuner.

Presently, there are two models of the stabilized master oscillator. The original design (model A) is now being replaced by a later version (model B) which provides increased tuning accuracy. At the time of the development of the original circuit, the most practical type of electronic frequency control was the saturable reactor. This method of control is used in the model A stabilized master oscillator. A saturable reactor is driven from a current source and therefore requires considerable power for its operation. The model B stabilized master oscillator contains a new type of component called a silicon capacitor. This component is a relatively high-impedance voltage-driven diode which exhibits a change in capacity as the voltage across it changes and requires little driving power. The model B stabilized master oscillator only is explained in this chapter.

MODIFIED FREQUENCY DISCRIMINATOR

When a master oscillator, V2, frequency is being selected, or if the oscillator frequency is incorrect, the frequency discriminator, in the phase and frequency discriminator (fig. 9-10, B) will produce an error voltage. This voltage is impressed across a silicon capacitor, C11 (fig. 9-11, A), in the oscillator grid tank.

The capacity of C11 varies as the voltage across it varies. An increase in voltage decreases the capacitance, and a decrease in voltage increases capacitance.

The input 455-kc i-f signal, plus or minus any oscillator error, is applied to the frequency discriminator circuit from Q3 of the SMO (fig. 9-10, B). The Q3 output (fig. 9-11, A) is applied via C32 to the L3-C4 discriminator tank, and by C33 to the L4-C5 tank. These tank circuits perform dual function by providing impedance matching between the Q3 output tank and the frequency discriminator circuit, and by providing the discriminator action for master oscillator frequency correction.

L3-C4 is tuned to resonate above the 455-kc no-error i-f signal, and L4-C5 is tuned to resonate below 455 kc. Thus, at 455 kc, L3-C4 is inductive (because it is operating below parallel resonance) and L4-C5 is capacitive (operating above parallel resonance) for zero-error input.

A +16-volt d-c potential is maintained at the R9-CR7 junction by the Zener breakdown action of CR7. This potential is applied via R25 to R30 inclusive and R8 to silicon capacitor, C11. The capacitance of C11 varies inversely with the d-c voltage across it.

C11 and C10 in series are connected in parallel with C9 to form the total capacitance in the V2 oscillator tank. If the d-c voltage component across C11 remains constant the total capacitance in the V2 oscillator tank will remain constant and the V2 oscillator output will be at a fixed frequency.

Consider the discriminator action when zero error (455-kc ± Ocps) is introduced to the discriminator via C32 and C33. Because each of the discriminator tank circuits (L3-C4 and L4-C5) are tuned an equal number of cycles above and below the 455-kc input, it follows that each of the tuned circuits will produce equal magnitudes of voltage for the 455 kc ± 0 input. During each negative alternation of the voltage across L3-C4, a current flows through CR1 and R25 to develop a polarity across R25, as shown. L4-C5 causes a conduction through CR2 and R26 on negative alternations to develop a voltage across R26. This voltage is equal and opposite to the voltage across R25, and the net change in voltage across R25 and R26 is zero. Thus, the voltage along the divider (and across C11) to ground remains constant and there is no change in the oscillator output frequency.

If an input error frequency below 455 kc is applied from Q3 to the discriminator tuned circuits, L4-C5 (tuned below 455 kc) will develop a larger voltage than will L3-C4 which is tuned above 455 kc. The rectified voltage across R26 will be larger than the voltage across R25, and a net voltage is developed which decreases the voltage across C11. The decreased C11 voltage increases the C11 capacitance in the V2 oscillator tank and the oscillator frequency decreases. This action decreases the discriminator input error.

An input error frequency above 455 kc will cause the reverse action to occur and a larger voltage will be developed across R25 than across

R26. The larger R25 voltage increases the voltage along all points of the divider (with respect to ground) and consequently increases the voltage across C11. As the C11 voltage increases, its capacitance decreases. The resulting decrease in tank capacitance raises the frequency of the oscillator and the discriminator input error decreases.

Note that when the signal is fed through a subtractive mixer (or any odd number of subtractive mixers) as in figure 9-11, A, frequency inversion occurs. For example, if the output i-f signal decreases from 455 kc to 450 kc the oscillator input frequency will increase from 1000 kc to 1005 kc. The corrective signal fed back to the oscillator from the phase discriminator must therefore decrease the oscillator frequency from 1005 kc to 1000 kc in order to increase the output i-f signal from 450 kc to 455 kc.

Conversely, when the output i-f signal increases from 455 kc to 460 kc the oscillator frequency will decrease from 1000 kc to 995 kc. The corrective signal in this case must increase the oscillator frequency from 995 kc to 1000 kc in order to decrease the i-f output from 460 kc to 455 kc.

Thus to increase the output i-f signal frequency the oscillator frequency must be decreased; conversely, to decrease the output i-f signal frequency, the oscillator frequency must be increased.

When the master oscillator error is greater than 2.2 kc the frequency discriminator output controls the master oscillator feedback correction.

MODIFIED PHASE DISCRIMINATOR

When the V2 master oscillator frequency error signal is less than 2.2 kc, the phase discriminator (fig. 9-11, A) assumes control of the master oscillator correction. The 455-kc i-f signal (E_{SIG}) plus or minus the oscillator error signal is applied to the T4 secondary center tap. A reference signal voltage (E_{REF}) is coupled to the phase discriminator tank from the T4 primary. This signal originates in a temperature controlled reference oscillator, and is applied to the phase discriminator from the reference i-f amplifier, Q7 to Q9, inclusive (fig. 9-10, B).

It will be helpful at this time to analyze the voltage across R25 and R26 (fig. 9-11, A) as a result of frequency discrimination. You will recall that the frequency discriminator output consists of rectified half wave r-f pulses at a frequency of 455 kc ± the oscillator error frequency. The voltage across R28 and R29 at the phase discriminator varies at the same rate. Thus, CR5 and CR6 are controlled by two voltages; 455 kc plus or minus the oscillator error (E_{SIG}) applied from the R28-R29 junction to ground and by the reference voltage (E_{REF}) induced from the T4 primary.

When the signal at the T4 secondary center tap is exactly 455 kc (no V2 oscillator error frequency), voltages E_{ab} and E_{bc} (fig. 9-11, B) are equal, and CR5 and CR6 conduct equally through R28 and R29, respectively. The pulsating direct currents through these resistors are equal and 180 degrees out-of-phase, and the resulting voltage change across C29 and C30 to ground is zero. Thus, no voltage change occurs across voltage variable capacitor, C11, and the V2 oscillator frequency is not changed.

If the V2 oscillator frequency is too high, the signal voltage will lead the reference voltage (fig. 9-11, C). This action produces a larger voltage across R28 and a smaller voltage across R29. The R28 voltage polarity increases the voltage across C29, C30, and C11. The capacitance of C11 decreases and the V2 oscillator frequency increases to null the oscillator error.

The reverse action occurs when the V2 oscillator frequency is too low (fig. 9-11, D). In this condition the voltage across R28 is smaller than the voltage across R29 and the voltage across C29, C30, and C11 decreases. This action increases the capacitance of C11. The frequency of V2 decreases to null the oscillator error.

SIDESTEP OSCILLATOR BLOCK DIAGRAM

The sidestep oscillator (fig. 9-10, B) provides the injection frequency for the subtractive mixer, V5, of the SMO. The term "sidestep" refers to a change from a given frequency by a definite number of kilocycles. The injection frequency is sidestepped by 1, 2, or 3 kc, as required, to obtain the electronic tuning necessary to supplement the mechanical tuning of the master oscillator in the SMO. The sidesteps, 1, 2, and 3, are referred to as ADD 1, ADD 2, and ADD 3, respectively (fig. 9-1) and indicate the number of kilocycles the sidestep oscillator output is displaced from 2400 kc.

The output of the pulse generator (Q1, Q2), the 2.4 mc injection signal, and the crystal oscillator, V2, output are mixed in the subtractive mixer, V1, to provide a 455 kc output (table 9-1). This signal is mixed with the crystal oscillator output in additive mixer, V4, to produce the sidestep oscillator output. The output can be

Table 9-1.—Method of Sidestep Oscillator Frequency Correction.

REFERENCE OSCILLATOR INJECTION TO V1	CRYSTAL OSCILLATOR (V2) INJECTION TO V1	PULSE GENERATOR (Q1, Q2) INJECTION TO V1	FILTER (FL1) OUTPUT	CRYSTAL OSCILLATOR (V2) INJECTION TO V4	ADDITIVE MIXER (V4) OUTPUT
2400 kc	1945 kc	0 kc	455 kc	1945 kc	2400 kc
2400 kc	1944 kc	1 kc	455 kc	1944 kc	2399 kc
2400 kc	1943 kc	2 kc	455 kc	1943 kc	2398 kc
2400 kc	1942 kc	3 kc	455 kc	1942 kc	2397 kc

changed in steps of 1 kc by selection of the V2 crystal oscillator frequency, while maintaining a stability on all output frequencies equal to that of the reference oscillator input.

The sidestep oscillator (fig. 9-10, B) is not used on band 1, band 2, band 3 add 0, and band 4 add 0. On these bands, a 2400 kc signal from the reference oscillator is fed directly to the second mixer, V5, of the SMO by relay, K1 (in the position shown).

When the band switch is in the ADD 1, ADD 2, or ADD 3 position, K1 (at the output of the SMO) is energized and its lower contacts are open while the upper contacts are closed. The output of the crystal oscillator, V2, in the sidestep oscillator is heterodyned with a 455-kc signal in an additive mixer, V4, to produce a sum frequency which serves as the injection frequency for the SMO. This signal is fed through the upper contacts of K1 to the second mixer, V5, of the SMO.

On band 4 ADD 1, K3 and K1 are energized, the crystal oscillator, V2, operates at 1944 kc (K2 deenergizes as shown). After heterodyning in the additive mixer, V4, the sidestep oscillator output frequency will be 2399 kc. This signal is fed through K1 to subtractive mixer, V5, in the SMO.

On band 4 ADD 2 and band 3 ADD 1, K2 in the sidestep oscillator is energized (and K3 is not) and crystal oscillator, V2, operates at 1943 kc. The sidestep oscillator output frequency to V5 of the SMO will be 2398 kc.

On band 4 ADD 3, both K3 and K2 in the sidestep oscillator are energized. Oscillator, V2, operates at 1942 kc and the output frequency from the sidestep oscillator to the second mixer, V5 of the SMO is 2397 kc.

The pulse generator, Q1 and Q2, subtractive mixer, V1, filter, FL1, and tuned amplifier, V3, operate in a correction loop to eliminate the possibility of frequency error in the sidestep oscillator output which originates in the crystal oscillator, V2. The pulse generator, Q1 and Q2, is driven by a 1-kc signal from the frequency divider circuit, and produces a 1-kc keying pulse that is used to key subtractive mixer, V1, into conduction at a 1-kc rate. Mixer, V1, also receives a 2400-kc signal from the reference oscillator. The keying of the mixer at a 1-kc rate produces a spectrum of frequencies above and below 2400 kc which are separated by 1 kc.

A third signal component in the mixer, V1, is fed from the crystal-controlled oscillator, V2, and may be either 1945, 1944, 1943, or 1942 kilocycles, depending on the control of crystal selection relays, K3 and K2. The crystal oscillator signal is beat with the 1-kc spectrum frequency of the 2400-kc signal which will produce a 455-kc difference frequency (± the oscillator error). For example, if the selected V2 frequency is 1943 kc the V1 output is (2400-1) - (1943 + 1) = 455 kc.

A bandpass mechanical filter, FL1, which immediately follows the subtractive mixer, V1, has adequate rejection to adjacent 1-kc spectrum frequencies but a sufficient bandpass width to accommodate the crystal oscillator error. The 455-kc signal, plus or minus any oscillator error, is amplified in V3, and applied to the additive mixer, V4. The crystal oscillator signal is injected directly into the additive mixer and combines with the 455-kc signal (± the oscillator error) to produce a sidestep output signal on any one of four frequencies: 2400, 2399, 2398, or 2397 kc. The use of the subtractive mixer, V1, and then the additive mixer, V4, cancels the crystal oscillator error, resulting in a sidestep oscillator stability equal to that of the reference oscillator.

For example, when operating on band 4 ADD 1, K3 is energized to select the 1944-kc crystal. Assume an oscillator error in V2 of 100 cps. The action of the 1-kc triggering signal from

the pulse generator produces the 1-kc spectrum frequencies above and below 2400 kc. The 455-kc difference frequency will be obtained by heterodyning the 2399-kc spectrum frequency with the crystal oscillator output. However, because of the oscillator error, the heterodyning process in V1 produces:

$$\begin{array}{r} 2399.000 \text{ kc} \\ -\ 1944.100 \text{ kc} \\ \hline 454.900 \text{ kc} \end{array}$$

This signal is passed through FL1, amplified in V3, and applied to the additive mixer, V4, where it is beat with the original crystal oscillator output. The resulting frequency is:

$$\begin{array}{r} 1944.100 \text{ kc} \\ +\ 454.900 \text{ kc} \\ \hline 2399.000 \text{ kc} \end{array}$$

Thus, the V2 oscillator error is cancelled, and the sidestep oscillator output to the second mixer, V5, in the SMO is exactly 2399 kc.

FREQUENCY DIVIDER

The frequency divider (fig. 9-10, B) supplies a 4-kc signal to the SMO and a 1-kc signal to the sidestep oscillator.

FUNCTIONAL DESCRIPTION

The frequency divider consists of a square wave generator-amplifier, Q1, and three multivibrator-type frequency dividers. The 100-kc signal from the reference oscillator is amplified in Q1, and divided to 20 kc by one multivibrator (Q2 and Q3). The 20-kc signal is divided to 4 kc by another multivibrator (Q4 and Q5), and the 4-kc signal is divided to one kc by a third multivibrator (Q6 and Q7). Because the 4-kc and 1-kc input signals are derived from the 100-kc input signal, their stability is equal to that of the reference oscillator.

TWENTY-KILOCYCLE DIVIDER CIRCUIT

Each of the divider stages of the frequency divider assembly (fig. 9-10, B) function as a synchronized multivibrator. The synchronizing signal is obtained from the reference oscillator via square wave generator-amplifier, Q1. The divider circuit of Q2 and Q3 is described below with the aid of the circuit diagram of figure 9-12, A, and the curves of figures 9-12, B and C.

Both of the transistors (Q2 and Q3) are forward biased in the base-emitter circuit. As with all free-running multivibrators, the unbalance in the two multivibrator sections serves as the initial trigger pulse to begin the oscillations.

Assume that Q2 (and its associated multivibrator section) conducts the heavier current when the equipment is initially energized. The collector voltage of Q2 decreases, and C3 discharges through R5. The voltage increases across R5, causing point A to become less positive to ground. This action decreases the current through CR4 and decreases the forward base-emitter bias of Q3. As the Q3 collector current decreases, the Q3 collector voltage increases, and C2 assumes a charge via CR3 and the base-emitter of Q2. This action results in a further increase in the forward base-emitter bias of Q2, and collector current increases. The Q2 collector voltage decreases and C3 continues to discharge through R5. Diode CR4 conducts less and the base-emitter current of Q3 decreases further. The action is cumulative until Q2 is conducting at saturation and Q3 is at cut off.

The saturation of Q2 causes the Q2 collector voltage to ground to become steady (fixed), and the discharge current of C3 through R5 drops to zero. This action raises the forward bias on the base-emitter circuit of Q3 and permits CR4 to again conduct. The rise in forward base-emitter current of Q3 causes an increase in the Q3 collector current, and the Q3 collector voltage to ground decreases.

As the collector voltage of Q3 decreases, C2 discharges through R4, the +27.5 volt supply, the emitter-collector of Q3, and the 5-6 winding of T1. The increase in voltage across R4 decreases the forward bias current through CR3 and the base-emitter of Q2, until Q2 is cut off and Q3 is conducting at saturation. Thus, oscillations occur in Q2 and Q3.

Synchronizing pulses are applied to the multivibrator via T1. The two secondary windings of T1 are connected so that the synchronizing pulse introduced from the T1 primary increases the base-emitter current of Q2 and Q3. The synchronizing voltage in the 4-3 winding of T1 causes the Q3 base-emitter current to increase while the 5-6 voltage causes a similar action in the base-emitter circuit of Q2. The initial trigger pulse will cause one of the transistors to conduct more current than the other due to inherent differences in the characteristics of the two transistors.

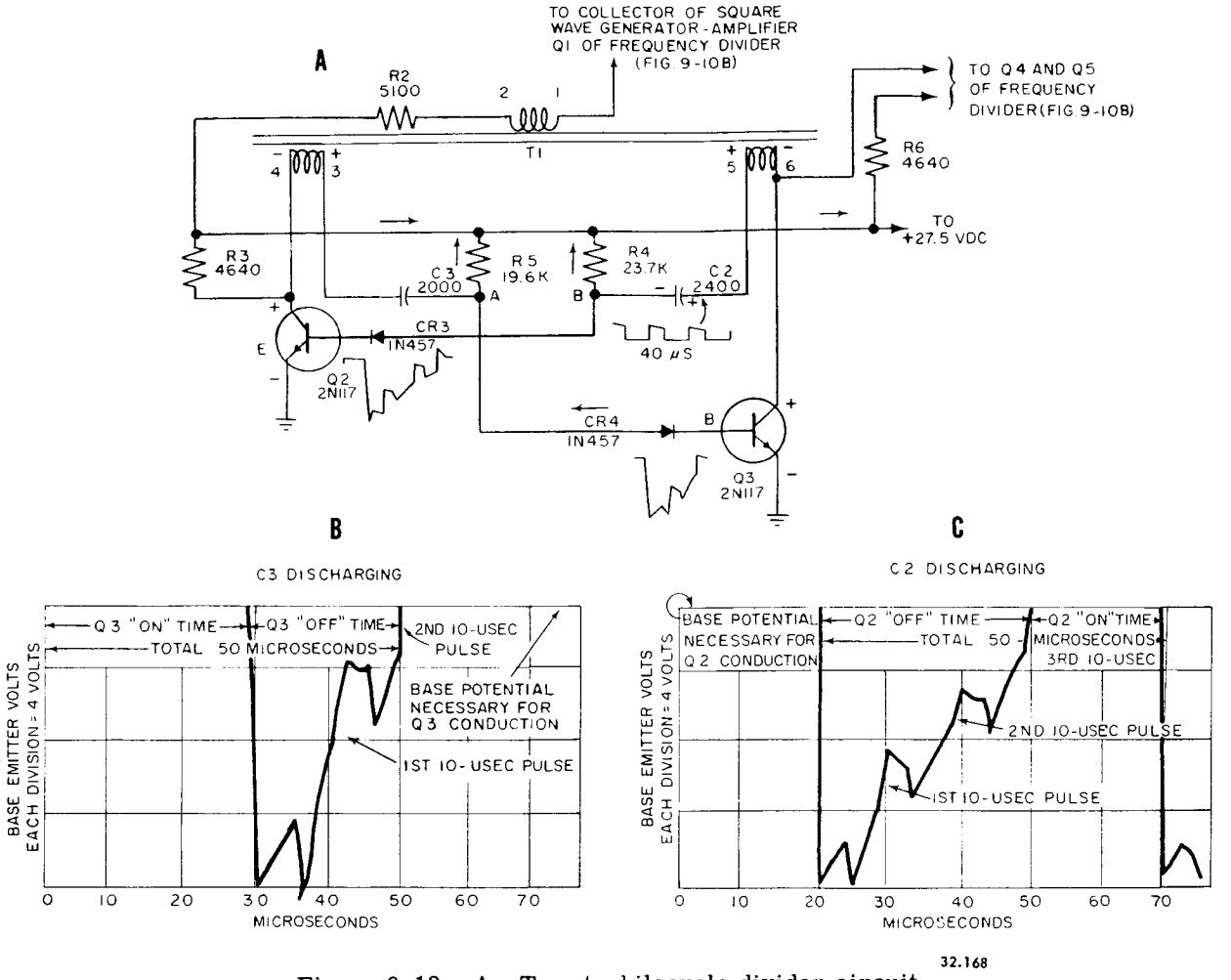


Figure 9-12.—A. Twenty-kilocycle divider circuit.
B. Q3 base-emitter volts.
C. Q2 base-emitter volts.

The synchronizing pulses occur at a 100-kc rate (10-μs intervals) from the reference oscillator (fig. 9-10, B) and are superimposed upon the discharge voltage of C2 and C3 during the time that each of these capacitors is discharging. This produces a discharge curve, as shown in figure 9-12, B, when C3 is discharging, and at C when C2 is discharging. The synchronizing pulses are represented as positive-going pulses on each of the curves.

The presence of the synchronizing pulses (at 10-μs intervals) on the discharge curve causes each of the transistors to begin conducting collector current before the 35 (or 25) μs period has actually expired. To understand this action, assume that Q2 conducts the heavier current when the synchronizing pulse is applied. The drop in the Q2 collector voltage causes C3 to discharge through R5, and drives Q3 into cutoff (fig. 9-12, B). Normally, the total time required for the C3-R5 discharge to a point which will allow Q3 to conduct is 25 μs. However, the presence of the synchronizing pulse on the discharge curve after each 10-μs interval causes the base-emitter voltage of Q3 to be sufficiently increased to allow Q3 to conduct after 20 μs.

When Q3 conducts, the collector voltage decrease at Q3 causes C2 to conduct a heavy discharge current through R4 and cuts off Q2. The normal cutoff time of Q2 is 35 μs. The discharge curve of C2 is shown in figure 9-12, C. It will be noted that the third synchronizing pulse reduces the Q2 base-emitter bias voltage sufficiently to permit Q2 to again conduct after 30 μs.

By controlling the multivibrator in this manner, the total duration of one multivibrator cycle is 50 μs, and the pulse recurrence rate is 20 kc. As previously stated, the multivibrator output pulses are divided by 5 in a second multivibrator to produce a 4-kc output and the 4-kc output is divided by 4 in a third multivibrator to produce a 1-kc output. Frequency division in these multivibrators is similar to that described for the 20-kc multivibrators.

REFERENCE OSCILLATOR

The reference oscillator (fig. 9-13) provides the basic reference frequencies of 100 kc and 2400 kc for the entire equipment. The reference oscillator signal is generated by a 3-mc crystal-controlled transistor oscillator, Q5.

Because the frequency accuracy of the equipment depends on the stability of the 3-mc crystal oscillator, the oscillator crystal, Y1, is enclosed in a temperature-controlled oven (fig. 9-14). The oven temperature is maintained at +80° C.

The heater, R9 through R12, is supplied by a 5-kc oscillator-amplifier, Q3, whose output amplitude varies according to the oven temperature. This arrangement maintains the oven temperature closer to +80° C than can be accomplished by the more conventional thermal contact-type relay.

A feedback voltage proportional to the degrees error in the oven is applied from a resistive bridge circuit (comprising R9 thru R12) to the stages in a regenerative loop (Q1, Q3, Q2, and Q4). The resistors in the bridge are the temperature sensing elements in the oven. Two of the bridge arms (diagonally opposite) are composed of nickel wire, and the other two of a low temperature coefficient alloy.

When the bridge circuit is unbalanced, a potential difference exists between the R9-R11 and R10-R12 junctions. This potential difference is applied between the emitter and base of Q3. The Q3 input voltage is amplified and applied via T2 to the driver amplifier, Q1. The Q1 output is push-pull amplified in Q2 and Q4 and applied via T3 to the oven heater bridge. For a large temperature error, the feedback voltage from the bridge is large, and the bridge temperature rises rapidly. As the temperature error decreases, the feedback voltage decreases, and the rate of temperature rise in the oven decreases. When the +80° C temperature is reached, the attenuation (heat loss) in the bridge is approximately equal to the gain of the regenerative loop, and the feedback voltage is practically zero.

The 3-mc output of the oscillator is fed through a buffer amplifier, Q6, to a regenerative divider loop circuit (fig. 9-13). This circuit consists of subtractive mixer, Q7, and a times 4 multiplier stage, Q10. The action in the regenerative divider loop causes it to provide its own heterodyning frequency. The initial heterodyning signals which start the regenerative action are derived from noise frequencies in the tuned circuits of the loop.

The 2.4-mc output of the Q10 multiplier stage is fed through output amplifier, Q12, to the sidestep oscillator (fig. 9-10, B).

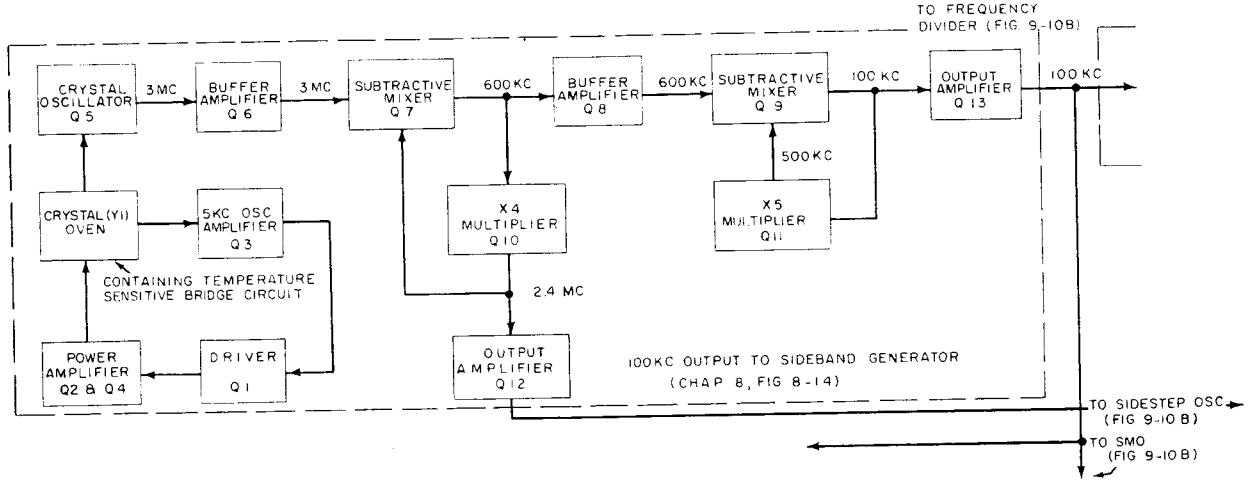


Figure 9-13.—Reference oscillator, block diagram. 32.169

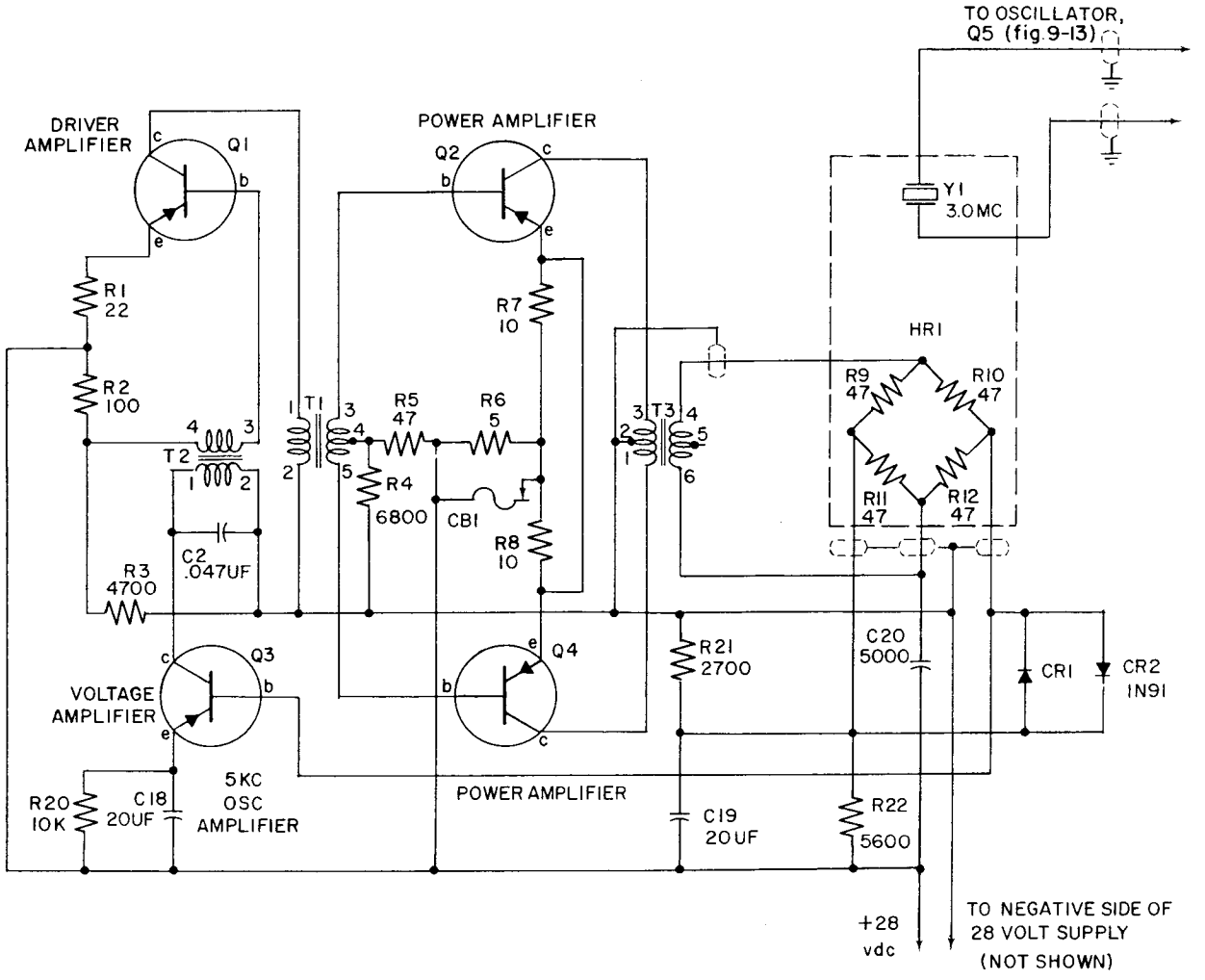


Figure 9-14.—3-mc crystal oven and regenerative loop.[32.170]

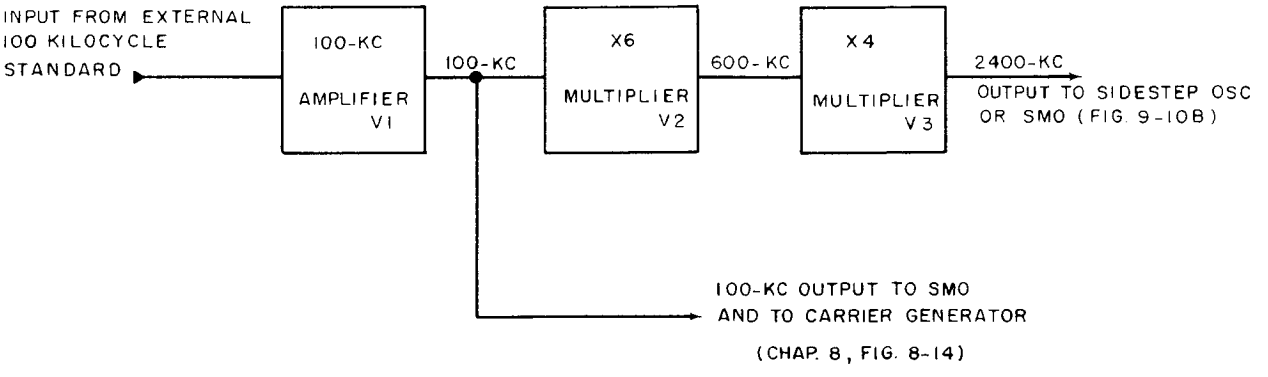


Figure 9-15.—Isolation amplifier, block diagram.[32.171]

The 600-kc output of the regenerative loop is fed through buffer amplifier, Q8, to another regenerative divider loop which consists of subtractive mixer, Q9, and times 5 multiplier stage, Q11. Buffer, Q8, isolates the two regenerative loop circuits. The 100-kc output of the loop is amplified in Q13, and fed to the frequency divider, the SMO, and to the sideband generator. The 100-kc output of the reference oscillator represents the frequency standard for the equipment, and has a long-term stability of one part per million.

ISOLATION AMPLIFIER

The isolation amplifier (fig. 9-15) replaces the reference oscillator when an external 100-kc standard is used. This unit receives and amplifies the 100-kc signal from the external standard, and provides the 2.4-mc signal for operation of the sidestep oscillator and stabilized master oscillator.

The isolation amplifier consists of a 100-kc amplifier, V1, a times 6 multiplier stage, V2, and a times 4 multiplier stage, V3. The 100-kc amplifier, V1, supplies the 100-kc input to the SMO and to the carrier generator (fig. 8-14). This signal is also applied to the times 6 multiplier, V2 (fig. 9-15).

The 600-kc output of V2 is multiplied by 4 in V3. The resulting 2.4-mc output of V3 is fed to the sidestep oscillator (fig. 9-10, B).

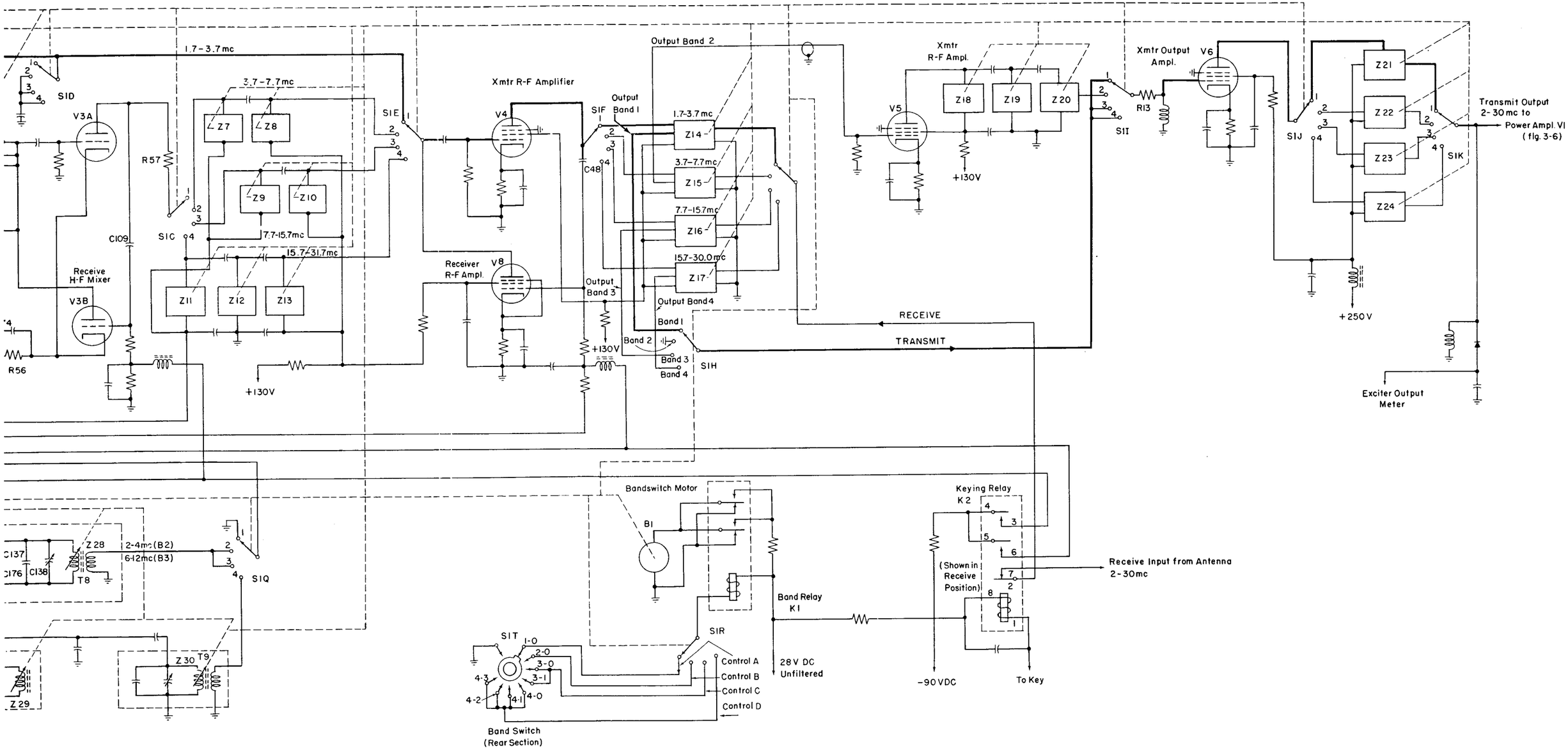
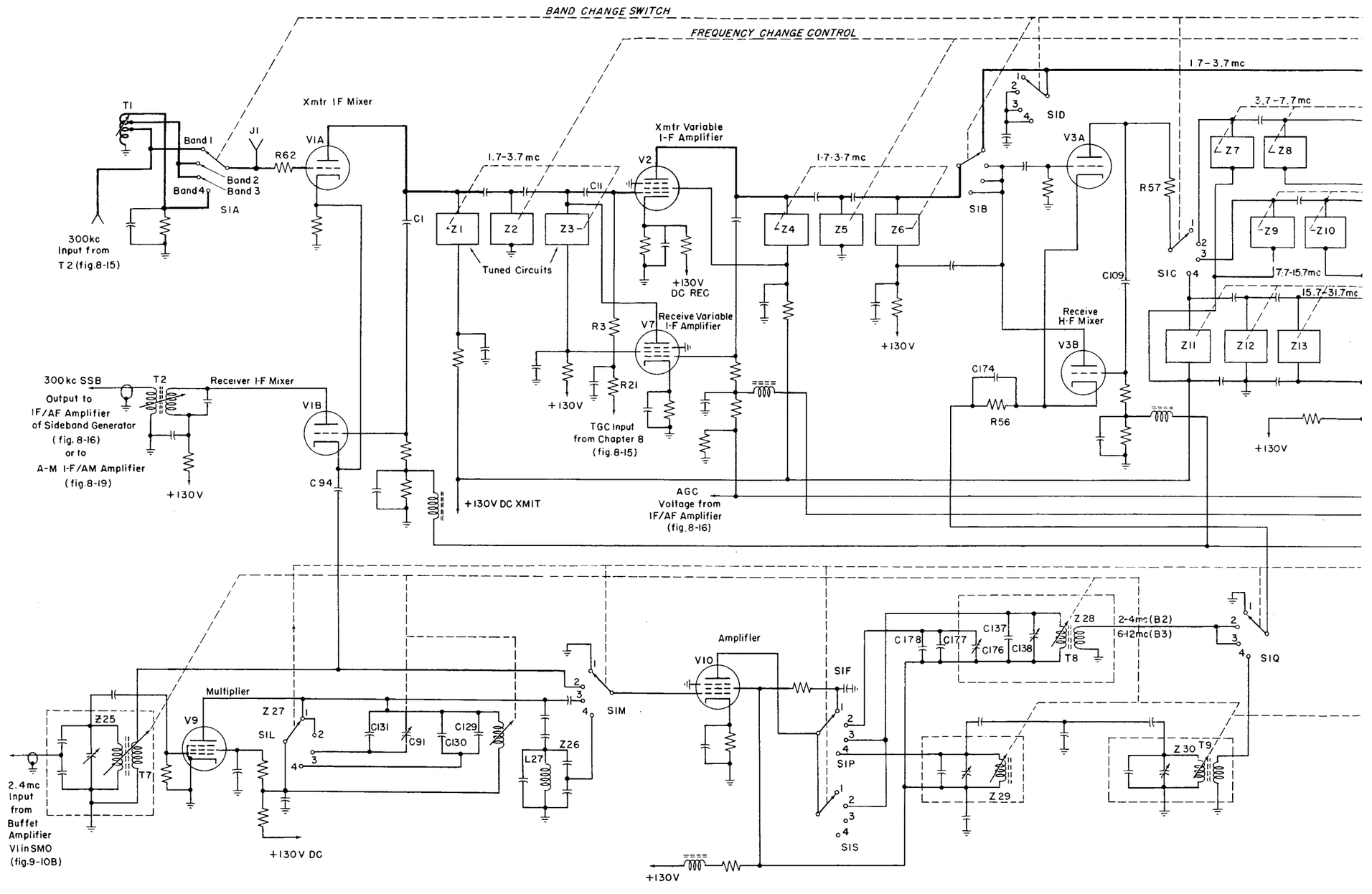
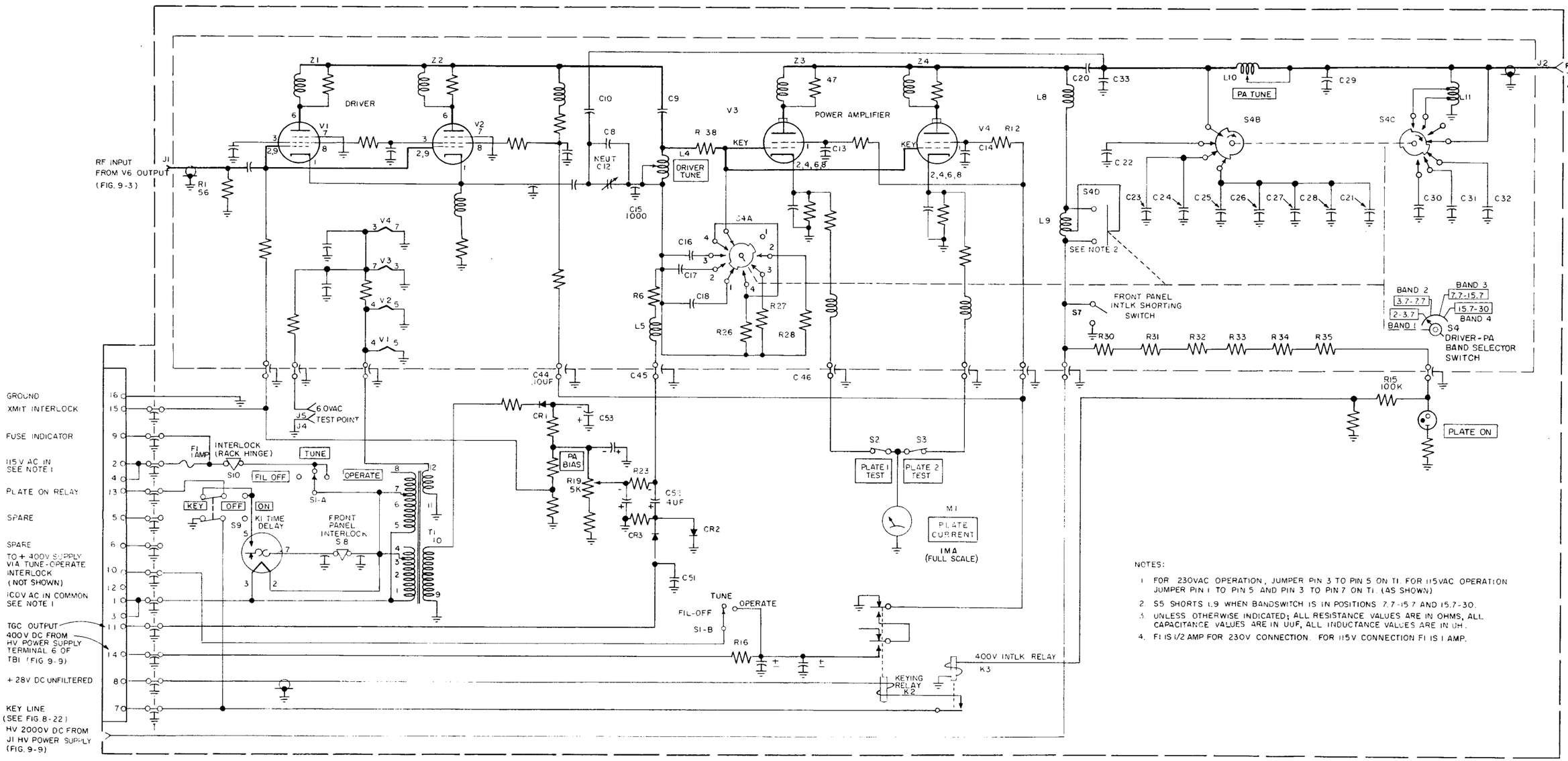


Figure 9-3.—R-f tuner, schematic diagram.[32.159]


BAND CHANGE SWITCH
FREQUENCY CHANGE CONTROL
T1
Band 1
Band 2
Band 3
Band 4
S1A
J1
300kc
Input from
T2 (fig.8-15)
Xmtr I-F Mixer
V1A
R62
C1
1.7-3.7 mc
Z1
Z2
Z3
Tuned Circuits
C11
Xmtr Variable
I-F Amplifier
V2
+130V
DC REC
Z4
Z5
Z6
+130V
S1B
S1D
V3A
1.7-3.7 mc
3.7-7.7 mc
Z7
Z8
R57
Z9
Z10
S1C
C109
7.7-15.7mc
15.7-31.7mc
Receive
H-F Mixer
V3B
Z11
Z12
Z13
C174
R56
+130V
R3
V7
Receive Variable
I-F Amplifier
R21
+130V
TGC Input
from Chapter 8
(fig.8-15)
300kc SSB
Output to
I-F/A-F Amplifier
of Sideband Generator
(fig.8-16)
or to
A-M I-F/AM Amplifier
(fig.8-19)
T2
Receiver I-F Mixer
V1B
+130V
C94
+130V DC XMIT
AGC
Voltage from
I-F/A-F Amplifier
(fig.8-16)
Multiplier
V9
Z25
T7
Z27
S1L
C131
C91
C129
C130
Z26
L27
S1M
2.4mc
Input
from
Buffet
Amplifier
V1 in SMO
(fig.9-10B)
+130V DC
Amplifier
V10
S1F
C178
C177
C137
C176
C138
Z28
T8
2-4mc (B2)
6-12mc (B3)
S1Q
S1P
Z29
Z30
T9
S1S
+130V



NOTES:

1. FOR 230VAC OPERATION, JUMPER PIN 3 TO PIN 5 ON T1. FOR 115VAC OPERATION JUMPER PIN 1 TO PIN 5 AND PIN 3 TO PIN 7 ON T1. (AS SHOWN)
2. S5 SHORTS L9 WHEN BANDSWITCH IS IN POSITIONS 7.7-15.7 AND 15.7-30.
3. UNLESS OTHERWISE INDICATED; ALL RESISTANCE VALUES ARE IN OHMS, ALL CAPACITANCE VALUES ARE IN UUF, ALL INDUCTANCE VALUES ARE IN UH.
4. F1 IS 1/2 AMP FOR 230V CONNECTION. FOR 115V CONNECTION F1 IS 1 AMP.

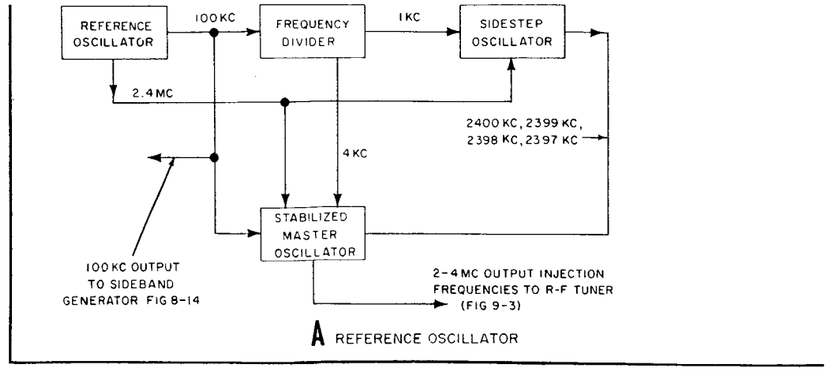
32.162

Figure 9-6.—Power amplifier, schematic diagram.

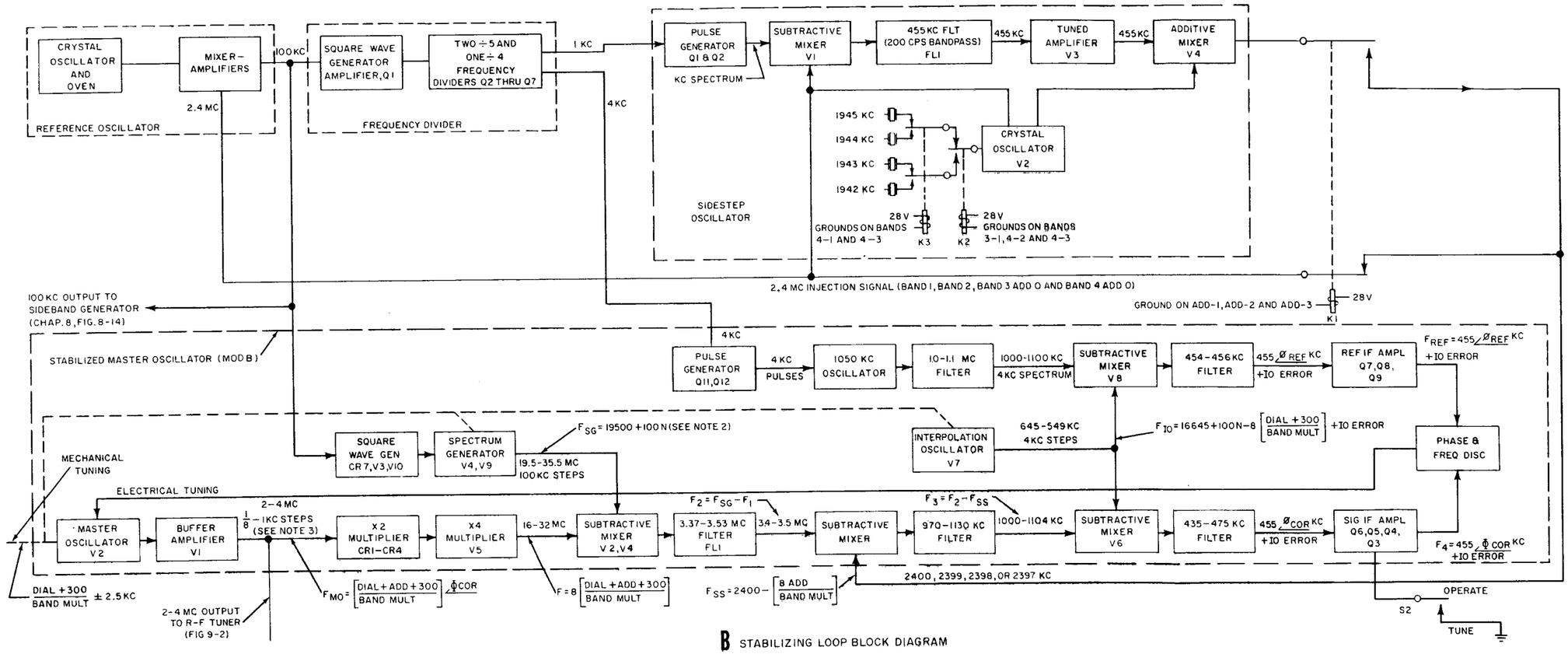
1. | BAND | 1 | 2 | 3 | 4 | |
   |---|---|---|---|---|---|
   | BAND MULT | 1 | 2 | 4 | 8 | |

2. $N = \frac{\text{DIAL} + 300}{12.5 \times \text{BAND MULT}} - 160$ WITH ALL DIGITS BEHIND THE UNITS DIGITS DROPPED. N IS A WHOLE NUMBER BETWEEN 0 AND 160 WHICH REPRESENTS THE NUMBER OF COURSE POSITIONS TRAVELED BY THE FREQ. CHANGE MECHANICAL LINKAGE.

3. BAND 1 MO OUTPUT IN 1KC STEPS.
   BAND 2 MO OUTPUT IN .5KC STEPS.
   BAND 3 MO OUTPUT IN .25KC STEPS.
   BAND 4 MO OUTPUT IN .125KC STEPS.



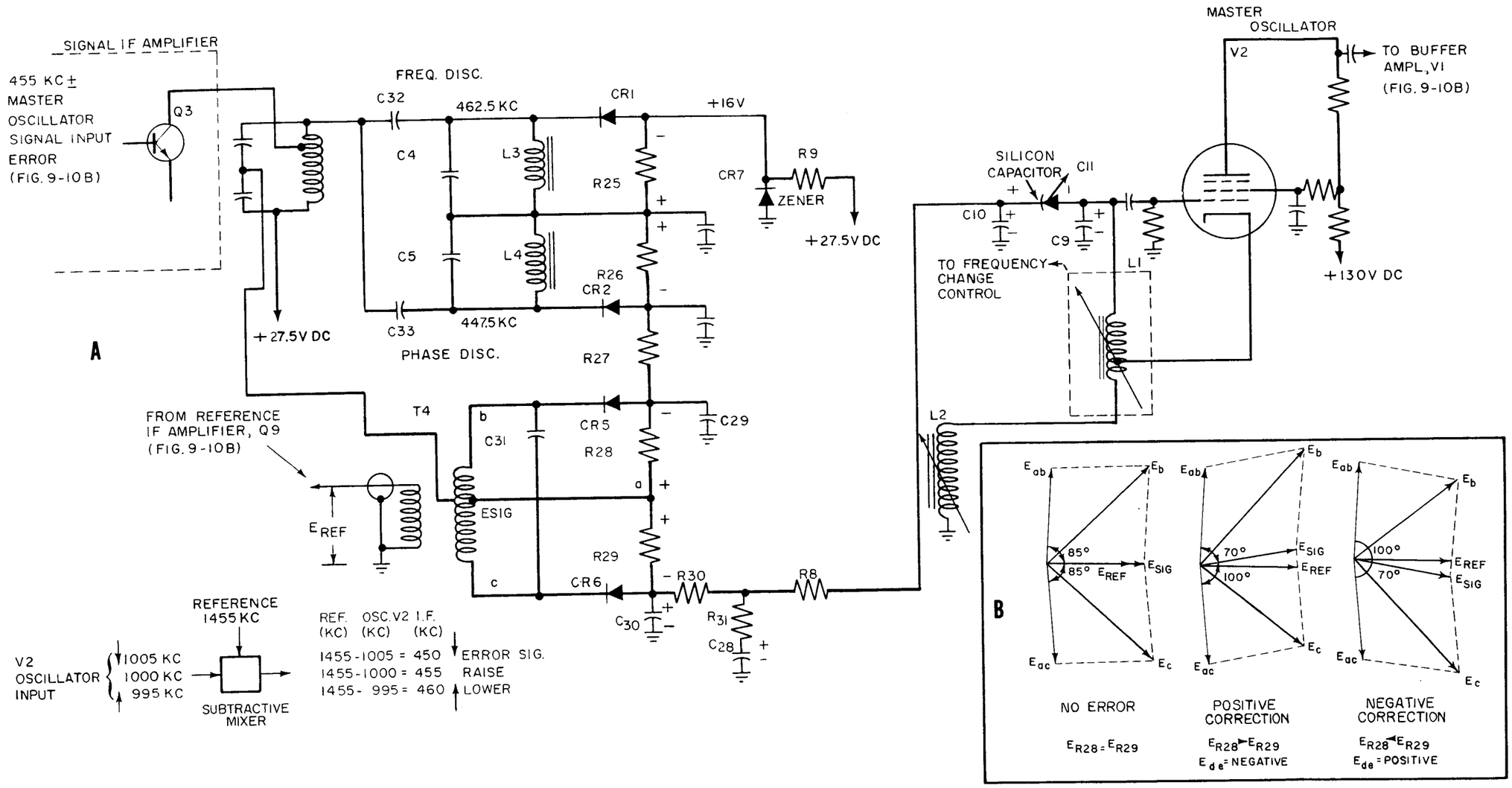
A REFERENCE OSCILLATOR



B STABILIZING LOOP BLOCK DIAGRAM

32.166

Figure 9-10.—Stabilizing loop.



32.167

Figure 9-11.—Modified master oscillator, phase and frequency discriminator.