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Handbook
PREFERRED CIRCUITS
Navy Aeronautical Electronic Equipment

VOLUME II

SEMICONDUCTOR DEVICE CIRCUITS

PREPARED BY
NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
FOR
BUREAU OF NAVAL WEAPONS
DEPARTMENT OF THE NAVY

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FOREWORD

The purpose of the Preferred Circuits Handbook is to document proven electronic circuits and to encourage their use in the design of Naval airborne electronic equipment.

Present day technological advances have made it possible to produce versatile, reliable, miniaturized electronic equipment to a degree not thought possible a few years ago. Use of Preferred Circuits Handbook is a contribution to this end. Furthermore, savings can be realized in more efficient use of engineering manpower, more rapid analysis of circuit failures, fewer educational programs, shorter research and development time and lower inventories without any sacrifice of good design practices.

The ultimate success of the preferred circuits program depends upon the active participation of the design engineer and equipment manufacturer in utilizing the circuits, in criticising the material presently in the Handbook, and in submitting improved or additional circuits for inclusion in the Handbook. Such material should be addressed to the Chief, Bureau of Naval Weapons, RAAV–41, Department of Navy, Washington 25, D.C.

PREFACE

The Revised Handbook Preferred Circuits is published in two parts: Volume I, Electron Tube Circuits, and Volume II, Semiconductor Device Circuits. Volume II contains Preferred Semiconductor Circuits PSC 1 through PSC 22. The first five of these are new circuits; the remaining 17 were previously published in the Supplements to the original Handbook Preferred Circuits.*

This Handbook of Preferred Semiconductor Device Circuits has been prepared within the Engineering Electronics Section, Instrumentation Division of the National Bureau of Standards for the Avionics Branch, Aircraft Division, Bureau of Naval Weapons, Department of the Navy. The Preferred Semiconductor Device Circuits have been developed by a group of engineers consisting of P. M. Fulcomer, O. B. Laug, J. H. Muncy, S. Rubin, and A. M. Torain, with laboratory assistance by M. R. Doggett. Most of the editing was done by K. M. Schwarz. The drafting and illustrations are the work of E. W. Bair, E. W. Duck, and J. W. Sutton. The suggestions and encouragement of G. Shapiro, Chief of the Engineering Electronics Section, and many others, both within and without the National Bureau of Standards, are gratefully acknowledged.

GEORGE J. ROGERS,
National Bureau of Standards.

*Navy copies were reprinted, incorporating three of the supplements with the basic, Vol. I. Therefore Vol. II will contain reprints of some circuits contained in the basic publication and Supplement No. 4.

INTRODUCTION

In 1952 the Industrial Planning Division of the Bureau of Aeronautics (now integrated into the Bureau of Naval Weapons), Department of the Navy, requested the National Bureau of Standards to undertake a preliminary program leading toward electronic circuit standardization. This interest in circuit standardization was prompted by the increasing use of mechanized production and the prospect of automatic production of electronic equipment, and by the belief that the reliability of electronic equipment could be improved by the use of circuit designs which had been proven in field use. Other advantages of circuit standardization are the more efficient utilization of engineering manpower in the design, development, production, and maintenance of electronic equipment; economies in the production and procurement of equipment and spare parts; and improvements in spare parts distribution.

Preliminary studies indicated that a large percentage of the circuit functions could be standardized without adverse effect on equipment performance. The program of vacuum-tube circuit selection and testing which followed resulted in the publication of the original Handbook Preferred Circuits in September, 1955. The Circuits in this Handbook were derived on the basis of experimental measurements on a large number of examples taken from both commercial and military equipment, and represented designs that were well established. In almost all cases, similar circuits had been in use for at least 10 years, with only minor improvements. After publication of the Handbook, other vacuum-tube circuits which met these same qualifications were added in published supplements.

The success and acceptance of the vacuum-tube program led to the initiation of a similar program for transistor circuits. Preferred transistor circuits cannot be based on a large sampling of existing systems, because only a few transistorized equipments have seen extensive field service. Furthermore, since transistor circuits are undergoing constant improvement, preferred transistor circuits can be expected to become outdated and require replacement more frequently than vacuum-tube circuits. Nevertheless, many of the advantages outlined for the preferred vacuum-tube circuits apply as well to preferred transistor circuits.

At first the transistor work was supplementary to the vacuum-tube program, and the transistor circuits were published with the vacuum-tube circuits, but separated from them by beginning the numbering of the transistor circuits with PC 201. In 1959 the transistor program was expanded and assumed a status independent of the vacuum-tube program. At the same time administrative control of the program was transferred to the Avionics Branch, Aircraft Division, of the Bureau of Naval Weapons, and technical supervision was delegated to the Naval Air Development Center, Johnsville, Pennsylvania. Although for a time the transistor circuits continued to be published with the vacuum-tube circuits, a separate Handbook for transistor circuits was planned. As a result, the Revised Handbook Preferred Circuits is published in two parts, Volume I, Electron Tube Circuits, and Volume II, Semiconductor Device Circuits.

Since the semiconductor circuits now appear in a separate handbook, it is no longer necessary to begin numbering them at 201. The numbering has also been changed to a sequential system, rather than the block system used

in the original Handbook. Numbers PSC 1 through PSC 22 appear in this Handbook; Supplement No. 1 will begin with PSC 23, and future additions will be numbered consecutively. To distinguish these circuits from the electron tube circuits bearing the same number, and in recognition of the fact that semiconductor circuits other than transistor circuits will in the future appear in this manual, the name of these circuits has been changed to Preferred Semiconductor Circuits, abbreviated PSC in the titles.

Volume II is designed for loose-leaf binding to facilitate the addition of new circuits and the revision of existing circuits as they are updated. The pages in each preferred circuit are numbered independently for the same reason.

In the selection of the preferred circuits, first preference has been given to circuits of mature design which are applicable in many different types of electronic equipment. The following general rules were adopted for the selection and design of the circuits:

1. The circuit must be a functional unit without regard to the number of transistors or other semiconductor devices included.

2. The circuit should represent the highest performance consistent with conservative and stable design.

3. Components must be chosen from types which are covered by military specifications. Wherever possible preferred components and values should be used. In particular, transistors and diodes must be chosen from those which appear on the Preferred and Guidance List of Transistors (MIL–STD–701) in effect at the time of publication of the circuit.

4. The circuit must be designed to operate as specified with any component which is acceptable under the military specifications for its type. Sufficient derating and compensation must be included to obtain the specified performance when the critical components have reached their end-of-life limits.

5. When regulated supply voltages are required, those specified in MIL–STD–706A, Power Supply Voltages for Electronic Equipment, must be used.

6. Interaction between circuits must be minimized by providing sufficient decoupling between circuits, or by providing sufficient information about transients introduced by the preferred circuit and transients which it can tolerate to permit effective decoupling circuits to be designed.

These circuits serve as a guide to current design practice, and as a base against which improvement can be measured. They represent, so to speak, a least common denominator in that a large percentage of applications can be satisfactorily fulfilled by their employment. They are not offered as definitive solutions, nor as being considerably superior to available alternates or to other circuits that might be devised to replace them. It is hoped that engineers will use the Preferred Circuits as a convenient summary of the state of the art, and as a means of avoiding unnecessary diversification and design effort.

ORGANIZATION OF THE HANDBOOK AND DIRECTIONS FOR ITS USE

Volume II of the Handbook Preferred Circuits is intended as a design tool for engineers who are familiar with semiconductor circuits, but who may not have a detailed knowledge of the circuit type under consideration. It is assumed that the user of this manual is looking for a functional circuit for a particular application. It is the purpose of this Handbook to suggest such a circuit, specify its performance in such terms that the prospective user can determine whether it meets his need or not, and furnish him with design information for the building of it.

Each Preferred Circuit consists of the circuit schematic and its specifications, and text sections giving application, design, and performance information about the circuit.

The Preferred Circuit SCHEMATIC and accompanying SPECIFICATIONS will give sufficient information in most cases to determine whether or not the Preferred Circuit has the characteristics required in a given application. Component values are usually given on the schematic diagram. When the values must be chosen to meet the conditions of operation, instructions for the selection of the component values, generally in the form of equations, are given in the specifications. The specifications also give additional component information, the operating characteristics of the circuit, and its power requirements.

The power dissipated in resistors, the voltage stress to which capacitors are subjected (unless this is obvious from the circuit configuration), and the limiting resistor and capacitor values are given in the specifications to assist in the selection of COMPONENTS. As used in the Preferred Circuits the term "limits" includes the initial tolerance of the component and the drifts caused by environmental changes, aging, or any other cause. The specified performance of the circuit assumes that the component values remain within these limits during the time that the circuit is in operation. The resistor dissipation and capacitor voltage values allow for changes in the components and supply voltages within the limits specified.

The OPERATING CHARACTERISTICS are specified as completely as possible, the form varying with the type of circuit. This information is supplemented by the text section on performance.

POWER REQUIREMENTS include the supply voltages, the degree to which each must be regulated, and the current required at each voltage.

The text section headed APPLICATION lists typical applications of the Preferred Circuit, and may include additional information, such as a comparison of this circuit and other similar Preferred Circuits, detrimental properties of the circuit, or limitations in its use. By reference to the Preferred Circuit schematic, the specifications, and the section on application, a prospective user should be able to determine whether or not the circuit meets his needs.

The section on DESIGN CONSIDERATIONS is intended to explain the design choices made in the circuit where the choice is not obvious, and to give pertinent information about the design. This section includes criteria for the choice of values, and any precautions that need to be taken in the selec-

tion of parts. Mechanical construction details are not usually given, but particular precautions are included where necessary. Theory is not covered except where required for the discussion of other design considerations.

In the third major text section, PERFORMANCE is discussed in more detail than is possible in the specifications. The performance specified for the circuit is based on "worst case" design, but the effect of changes in critical components and in supply voltages is discussed in sufficient detail so that the designer who uses the statistical approach will have a basis for determining the relative effects of supply voltage and component characteristic changes. Since electronic circuits are not ideal building blocks, but are affected by the circuits which precede and follow them, the effects of load and source impedance and of power supply transients are discussed.

All of the Preferred Semiconductor Circuits contain the major divisions listed above. Other divisions may be added as needed, as for example Section 4 in PSC 9, entitled EXAMPLES OF USE.

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CONTENTS

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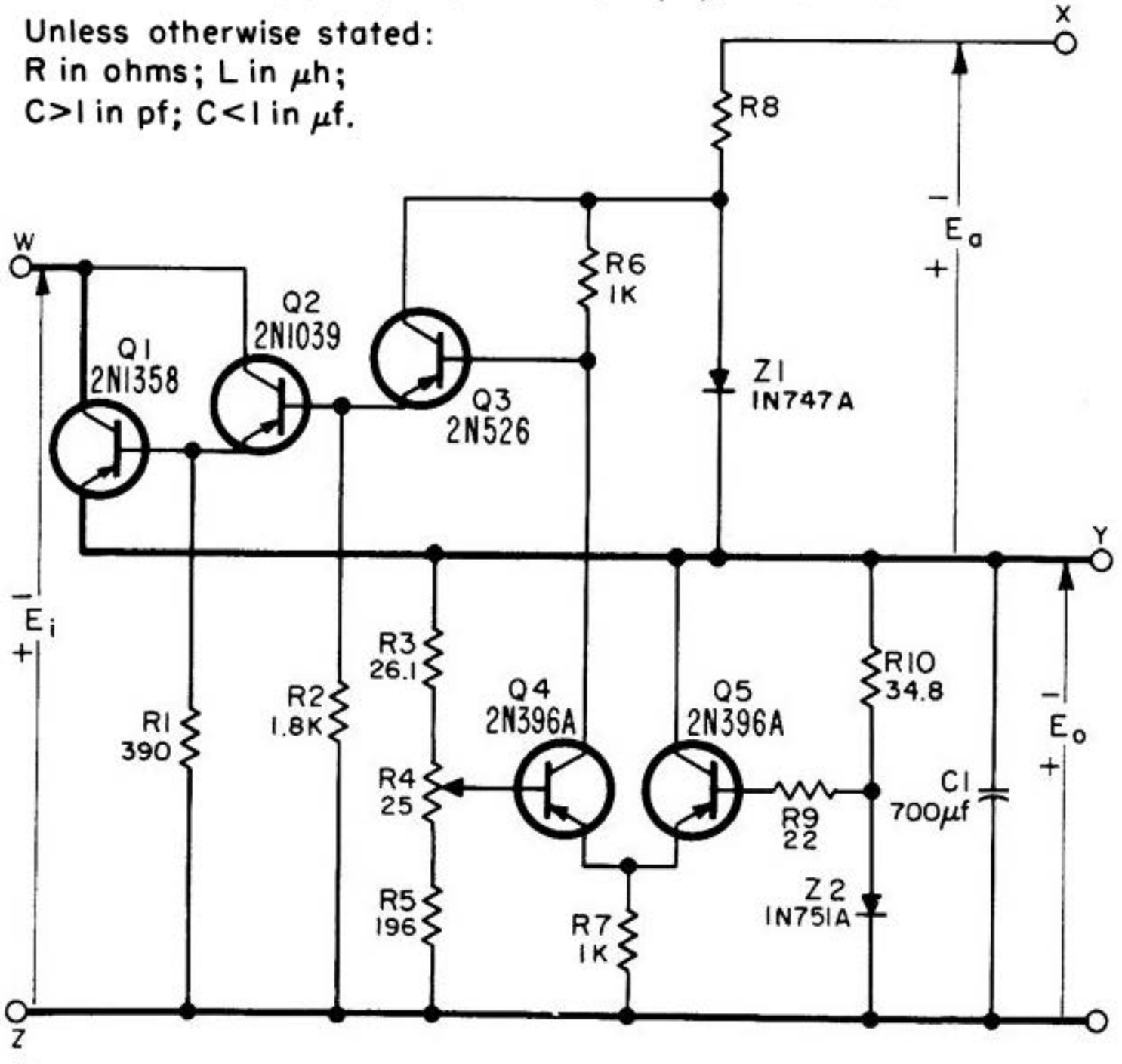
PREFERRED CIRCUIT NO. PSC 1

DC REGULATOR ±6 VOLTS: 1% REGULATION

PREFERRED CIRCUIT NO. PSC 1
DC REGULATOR FOR ± 6 VOLTS, 1% REGULATION



NOTES:

A. Either output terminal may be grounded, but the negative input terminal, W, must not be grounded.

B. The auxiliary supply, E_a, may be returned to the positive output terminal, Z, instead of to the negative terminal, Y, as shown. A floating auxiliary supply is necessary if return is made to the ungrounded output terminal. See Section 2.4.

C. Transistors Q1 and Q2 must be mounted on a heat sink. A clip-on heat sink should be used with Q3 for increased reliability. See Section 2.5.

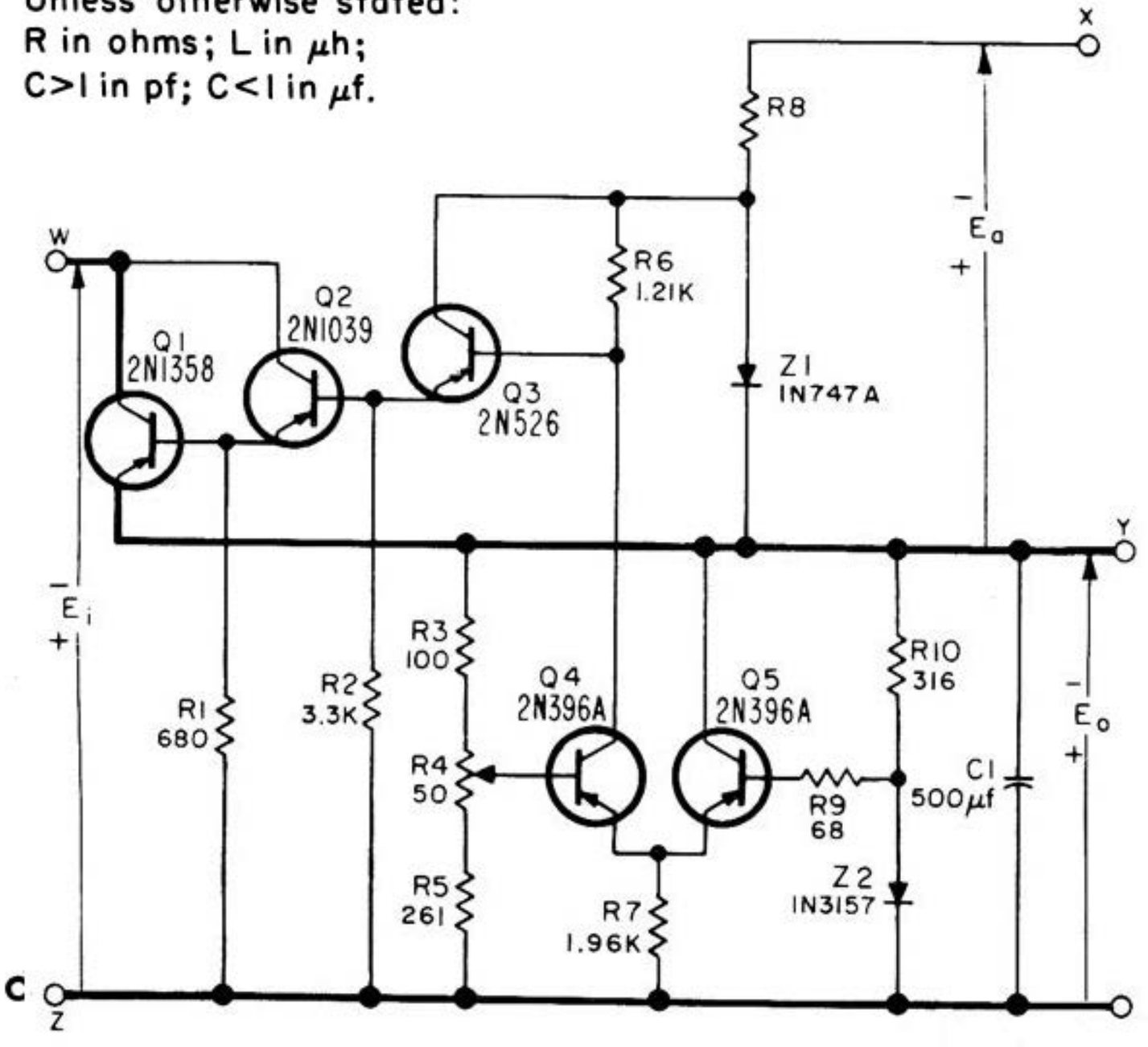
D. Contact and lead resistance should be kept to a minimum along the positive and negative output busses. See Section 2.9.

PREFERRED CIRCUIT NO. PSC 2

DC REGULATOR ±12 VOLTS: 1% REGULATION

PREFERRED CIRCUIT NO. PSC 2
DC REGULATOR FOR ±12 VOLTS, 1% REGULATION

Unless otherwise stated:
R in ohms; L in μh;
C>1 in pf; C<1 in μf.



NOTES:

A. Either output terminal may be grounded, but the negative input terminal, W, must not be grounded.

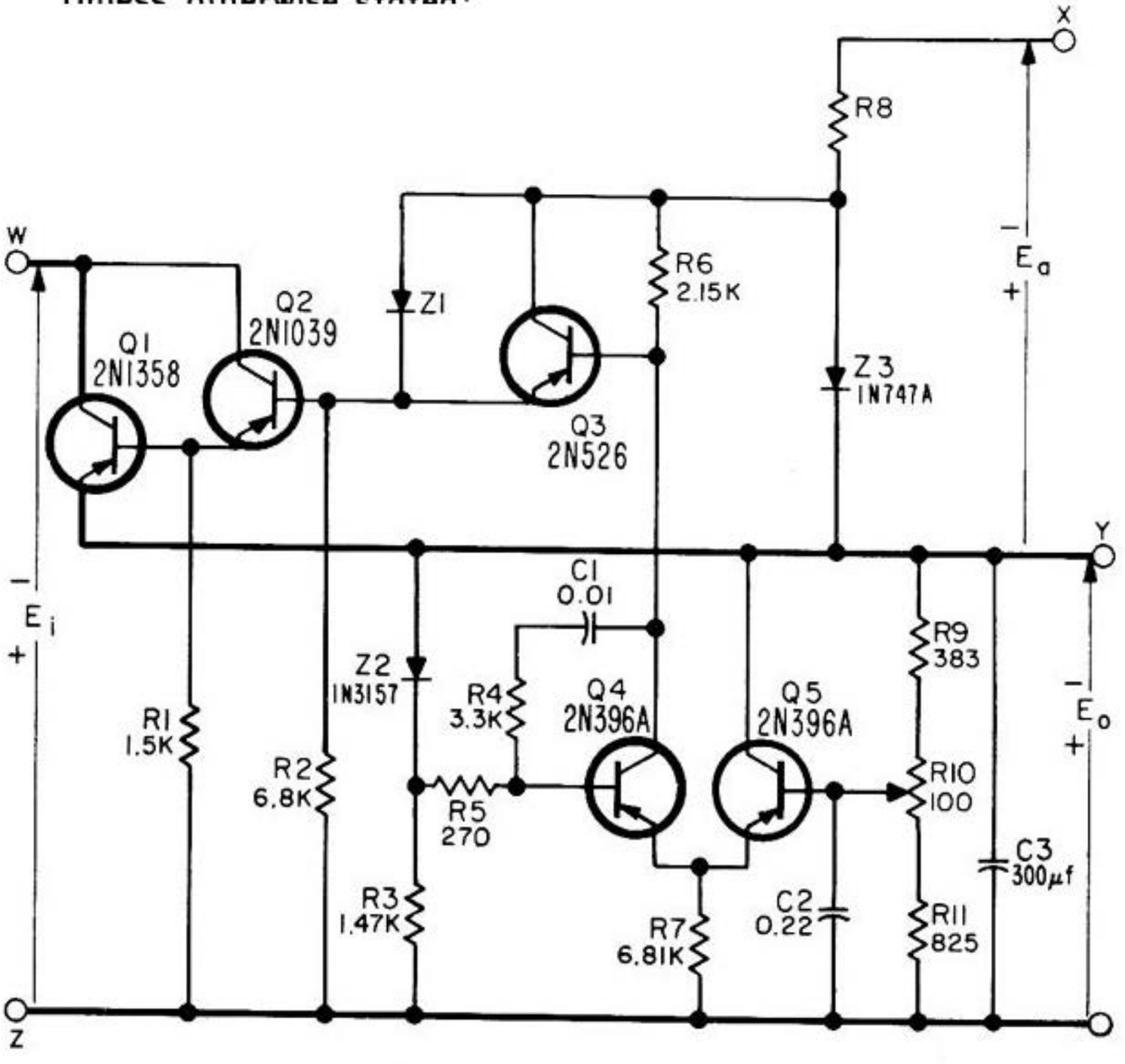
B. The auxiliary supply, E_a, may be returned to the positive output terminal, Z, instead of to the negative terminal, Y, as shown. A floating auxiliary supply is necessary if return is made to the ungrounded output terminal. See Section 2.4.

C. Transistors Q1 and Q2 must be mounted on a heat sink. A clip-on heat sink should be used with Q3 for increased reliability. See Section 2.5.

D. Contact and lead resistance should be kept to a minimum along the positive and negative output busses. See Section 2.9.

PREFERRED CIRCUIT NO. PSC 2
DC REGULATOR FOR ±12 VOLTS, 1% REGULATION

Unless otherwise stated:

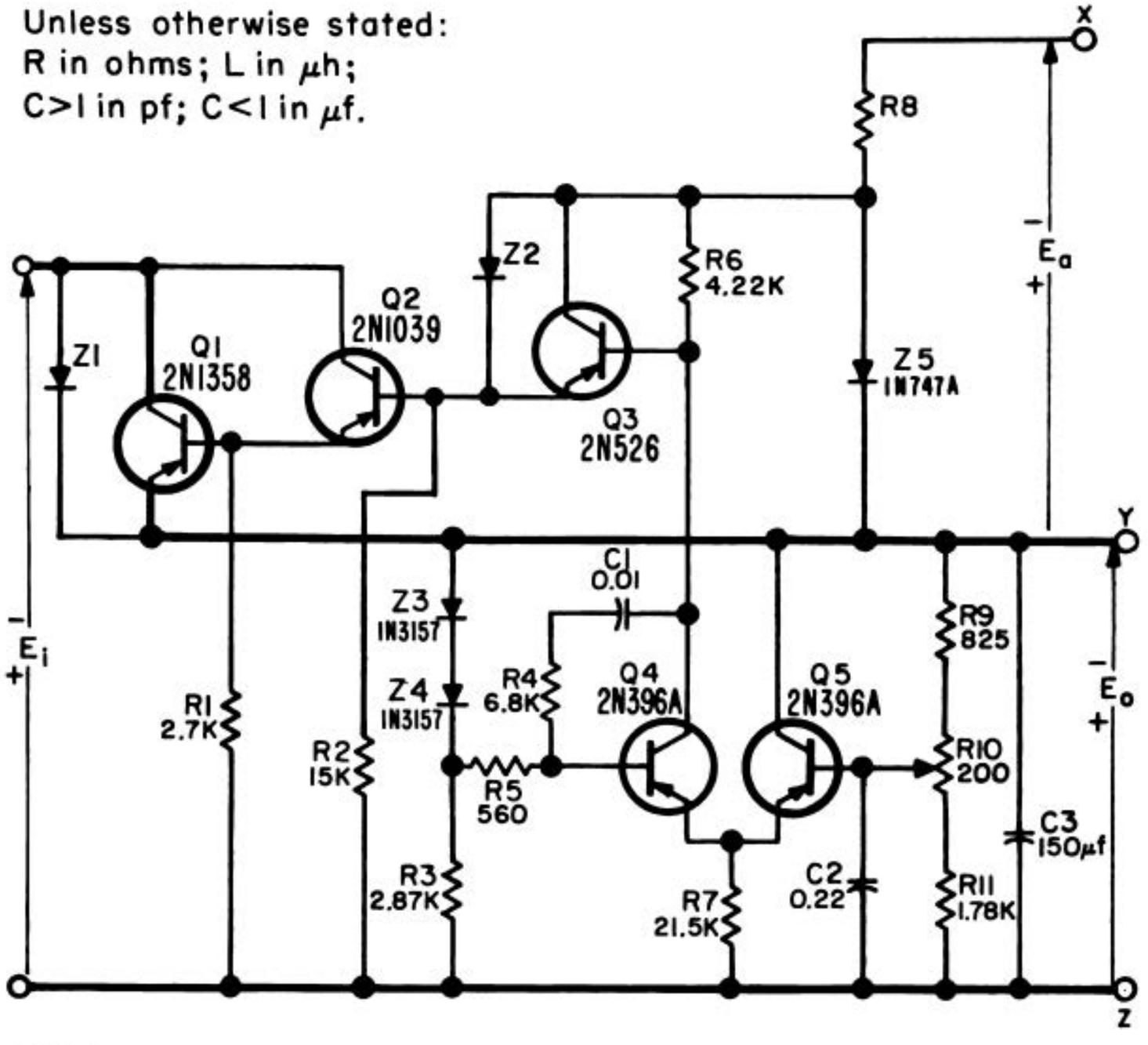


B. The auxiliary supply, E_a, may be returned to the positive output terminal, Z, instead of to the negative terminal, Y, as shown. A floating auxiliary supply is necessary if return is made to the ungrounded output terminal. See Section 2.4.

C. Transistors Q1 and Q2 must be mounted on a heat sink. A clip-on heat sink should be used with Q3 for increased reliability. See Section 2.5.

D. Contact and lead resistance should be kept to a minimum along the positive and negative output busses. See Section 2.9.

PREFERRED CIRCUIT NO. PSC 4
DC REGULATOR FOR ±50 VOLTS, 1% REGULATION



NOTES:

A. Either output terminal may be grounded, but the negative input terminal, W, must not be grounded.

B. The auxiliary supply, E_a, may be returned to the positive output terminal, Z, instead of to the negative terminal, Y, as shown. A floating auxiliary supply is necessary if return is made to the ungrounded output terminal. See Section 2.4.

C. Transistors Q1 and Q2 must be mounted on a heat sink. A clip-on heat sink should be used with Q3 for increased reliability. See Section 2.5.

D. Contact and lead resistance should be kept to a minimum along the positive and negative output busses. See Section 2.9.

Components:

Z1: Breakdown voltage not greater than 50 volts nor less than the voltage drop across the series control element (input voltage minus 50 volts). Power rating not less than 3 watts at 65°C. Suggested types: 1N2970B through 1N2995B or 1N2804B through 1N2829B.

Z2: Breakdown voltage between 5 and 20 volts. Power rating not less than 250 mw at 65°C. Suggested types: 1N752A through 1N758A or 1N962B through 1N967B.

R8: Resistance and power dissipation are determined by the auxiliary supply voltage and the limits on auxiliary current. See Section 2.4.

R9, R11: Percentage change in the ratio of R9 to R11 due to environmental changes must be less than $\pm 1\%$ to obtain the output regulation specified. Initial tolerance of each may be $\pm 1\%$. Power dissipation rating must be conservative and chosen so that watts per ohm are approximately equal for the two resistors.

R10: Percentage change in resistance due to environmental changes must be less than $\pm 5\%$ to obtain the output regulation specified. Initial tolerance may be $\pm 10\%$.

C3: This capacitance may be obtained by paralleling several smaller units. A tantalum capacitor is required for reliable operation at low temperature. At 25°C the capacitance should not be less than 130 μf. At -55°C the decrease in apparent capacitance should be less than 25%, and the increase in series resistance should be less than 10 times.

Maximum power dissipation (Note 1): R1: 1.2 watt; R2: 0.2 watt; R3: 0.5 watt; R4, R5, R6: $\leq$0.01 watt; R7, R10: 0.07 watt; R8: see above; R9: 0.3 watt; R11: 0.6 watt.

Limits (these are not tolerances; see Note 2): R1, R2, R4, R5: $\pm 20\%$; R3: $\pm 2\%$; R6, R7: $\pm 5\%$; R8, R9, R10, R11: see above; C1: $\pm 30\%$; C2: $+100\%$, -30%; C3: see above.

Power requirements:

Input from unregulated source:

Voltage, E_i: Minimum, 50.8 volts. Maximum is dependent upon the thermal resistance of the heat sink, the maximum load current, and the maximum operating temperature for the particular application (see Section 2.5 and Figure 4-2). Absolute maximum, 100 volts.

Current, I_i: 850 ma maximum.

Auxiliary supply:

Voltage, E_a: Minimum 5 volts (Note 3). Maximum, not limited. The voltage may be unregulated.

Current, I_a: Minimum, 25 ma. Maximum, 75 ma. (Limits determined by Z5 and controlled by proper selection of R8. See Section 2.4.)

Operating characteristics:

Temperature range: -55°C to $+65$°C (see Section 2.5 and Figure 4-2).

Output voltage: 50 volts, positive or negative.

Output current: 0 to 750 ma (see Section 2.5 and Figure 4-2).

Total steady-state regulation plus stability (see Section 3.1): $\pm 1\%$.

Regulation for input voltage variation between 50.8 and 78.8 volts: $\pm 0.03\%$.

Regulation for load current variation between 0 and 750 ma: $\pm 0.2\%$.

Regulation for auxiliary supply current variation between 25 and 75 ma: $\pm 0.1\%$

Temperature stability: $\pm 0.01\%$ per °C.

Time stability (8 hour period): $\pm 0.05\%$.

Transient Regulation (see Section 3.2):

Regulation for input voltage changes: $\pm 0.3\%$ at 25°C, $\pm 1\%$ at -55°C. (Input voltage change between 50.8 and 78.8 volts in 0.02 μsec.)

Regulation for load current changes: $\pm 0.3\%$ at 25°C, $\pm 1\%$ at -55°C. (Load current change between 0 and 750 ma in 1.0 μsec.)

(Specifications continued on next page)

PSC 4 DC REGULATOR ±50 VOLTS: 1% REGULATION

1. APPLICATION

PSC 4 is intended for use with an unregulated dc power source to provide a supply voltage stabilized against changes of source voltage, load current, and environmental conditions (notably temperature). Ripple reduction and low output impedance are furnished as a by-product of the above criteria. PSC 4 will supply up to 750 ma at 50 volts and is designed for applications requiring less than 1% supply voltage variation together with low power loss across the regulating element.

The 1% regulation specified includes output voltage stability with time (for periods up to 8 hours) and with changes of environment; it does not include extremely short duration output voltage transients resulting from large step changes of input voltage or load current. Transient regulation is 1% for a ±20% step change of input voltage, or for a zero to maximum step change in load. The duration of the transient will not exceed 50 μsec for step changes of input voltage and 100 μsec for step changes in load current.

Overload and short circuit protection is not included in PSC 4 for reasons of simplicity and efficiency. Should this characteristic be required, it may be added to the circuit [1] or supplied externally by relay control.

2. DESIGN CONSIDERATIONS

2.1 *Basic Regulator Circuit:* PSC 4 is a series regulator (control element in series with load) employing negative feedback for control of the output voltage. Transistor Q1 is the series control element; Q2 and Q3 are emitter followers which match the output impedance of the voltage amplifier to the input impedance of the series control element; Q4 combined with Q5 is a differential amplifier which forms the comparison circuit and develops the voltage amplification of the feedback loop; R9, R10, and R11 comprise the sampling circuit; and voltage reference diodes Z3 and Z4 comprise the reference element.

The circuit configuration is the same as that of PSC 3 except that the reference element consists of two 8.4-volt reference diodes in series, and that regulator diode Z1 is added to prevent voltage breakdown of Q1 and Q2. Both of these changes are required because of the higher input and output voltages of PSC 4. Details of this circuit type and its operation are found in Sections 2.1 and 2.2 of PSC 3. Basic opera-

[1] C. A. Franklin, P. M. Thompson, and W. M. Caton, "Precision High-Voltage Transistor-Operated Power Regulators with Overload Protection", *The Proceedings of the Institution of Electrical Engineers*, Volume 106, Part B, Supplement No. 16, May, 1959, pp. 714–725.

Operating characteristics—*Continued*

Transient recovery time (see Section 3.2):
After input voltage changes: 50 μsec.
After load current changes: 100 μsec.
Input ripple reduction (Note 4): >1,000.
Output impedance at 25°C: <0.1 ohm, dc to 10kc; <0.2 ohm, 10kc to 300kc.

NOTES:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than a specified amount. For the components listed here, only the total deviation is important. Thus the specified maximum deviation, termed "limits", includes initial tolerance plus drifts caused by environmental changes or aging.

3. The minimum is 55 volts if the auxiliary supply is returned to the positive terminal, Z.

4. Input ripple reduction is the ratio of ac ripple present in the input voltage to the resulting ac ripple present in the output voltage for any ripple frequency between 0 and 800 cps.

tion of the series regulator is described in Section 2.1 of PSC 1.

2.2 *Selection of Transistor and Diode Types:* Germanium transistors are used throughout because of their present price advantage over similar silicon units and their lower base-emitter voltage drop. The maximum operating temperature, although lower than that which may be obtained with silicon units, is satisfactory for many applications. PNP types are specified, although similar NPN types, if and when available, could be used equally well by reversing the polarity at all input and output terminals. Three of the four transistor types have been on the Military Preferred and Guidence List of Transistors and Diodes (MIL-STD-701) since September, 1959, with every indication that they will remain. The fourth type, the 2N1358, is an electrical equivalent which replaces the 2N174 on MIL-STD-701B. The reasons for the selection of these transistor types are given in PSC 1, Section 2.3.

Regulator diode types for Z1 and Z2 are not specified because a number of different types will meet the given requirements. Of the types appearing on MIL-STD-701B, the series 1N2970B through 1N2995B or 1N2804B through 1N2829B will satisfy the requirements for Z1, and the series 1N752A through 1N758A or 1N962B through 1N967B will satisfy the requirements for Z2. The reference element, Z3,Z4, must be an extremely stable, temperature-compensated unit. The 1N3157 is specified, but the 1N3156, a similar unit with slightly less temperature stability which does not appear on MIL-STD-701, is perfectly satisfactory for use in PSC 4.

2.3 *Regulator Efficiency:* The voltage drop across the series control element is minimized by use of an auxiliary power supply, E_a. This reduces the power loss in the series element and maximizes regulator efficiency. These improvements are discussed in PSC 1, Section 2.4. The voltage drop across the series element may be as small as 0.8 volts without causing Q1 to lose control of the output voltage.

A single series transistor is used rather than two or more in parallel. Although larger load currents may be handled by a parallel combination, a loss of efficiency results due to the power dissipated in current balancing resistors, which must be added in series with each emitter. Additional emitter followers are also necessary to handle the increased control current.

2.4 *Requirements for Auxiliary Voltage Supply, E_a:* The auxiliary voltage supply may be either regulated or unregulated. Choice of nominal voltage and degree of regulation is left to the user, so long as the auxiliary current can be maintained within the stated 25- to 75-ma limits by selection of R8. The minimum auxiliary current is that necessary to keep regulator diode, Z5, operating in a range of relatively low dynamic impedance; the maximum auxiliary current is determined by the maximum permissible power dissipation in Z5 at high temperature.

The characteristics of resistor R8 should be such that initial tolerance and environmental effects will not cause its resistance to exceed the limits indicated below,

$$\frac{E_{a_{min}}-3.6}{.025} \geqq R8 \geqq \frac{E_{a_{max}}-3.6}{0.75},$$

where R8 is in ohms and E_a is the voltage of the auxiliary supply selected by the user. The inequality allows for variation of E_a from its nominal value. In the term to the left, the numerator is the minimum voltage which will appear across R8, and the denominator is the minimum current, in amperes, which must be furnished by the auxiliary supply. In the term to the right, the numerator is the maximum voltage which will appear across R8, and the denominator is the maximum current which the auxiliary supply may furnish.

Auxiliary supply ripple reduction (the ratio of the ac ripple, e_a, present in the auxiliary supply voltage to the resulting ac ripple, e_{oa}, appearing in the output voltage) is proportional to $R8/r_{Z5}$, where r_{Z5} is the dynamic impedance of Z5. Since r_{Z5} is a function of the current through the regulator diode, and since diode current is a function of the auxiliary supply current, I_a, ripple reduction is a function of both R8 and I_a as shown in Figure 4-1. This relationship should be kept in mind when choosing the auxiliary supply and the consequent value of R8.

The auxiliary supply is shown returned to the negative output terminal, Y, but may also

be returned to the positive terminal, Z. If it is returned to the positive terminal, however, the auxiliary supply voltage must be 50 volts larger for a given auxiliary current, and a 50-ma minimum load is required to assure a return patch for the auxiliary current.

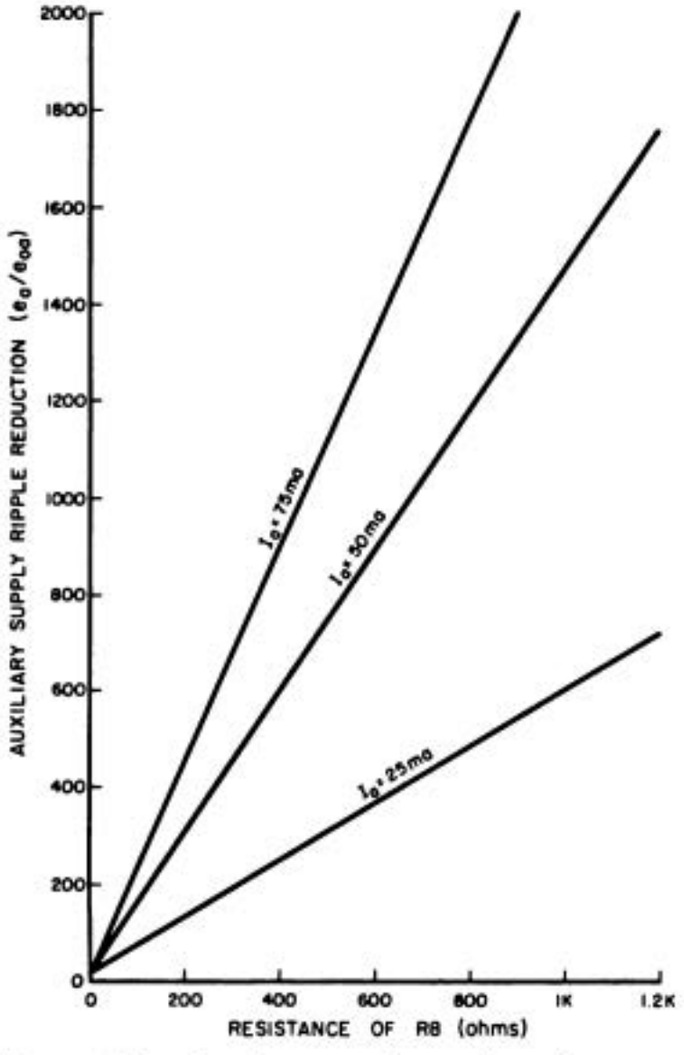


Figure 4–1.—Auxiliary supply ripple reduction as a function of R8 and auxiliary supply current, I_a.

2.5 *Determining Regulator Operating Range Limitations:* Circuit operation at the absolute maximum ratings specified for ambient temperature (65°C) and load current (750 ma) may not be possible in every application. Since the series transistor, Q1, may dissipate only a limited amount of power, the upper ratings for input voltage, load current, and ambient temperature are actually dependent variables, one of which may have to be sacrificed for the others, depending upon the particular application. Their order of magnitude depends upon the thermal resistance from Q1 case to ambient air.[2] A low thermal resistance allows each rating to be proportionately higher (up to the absolute maximum), while a high thermal resistance requires that each rating be proportionately lower.

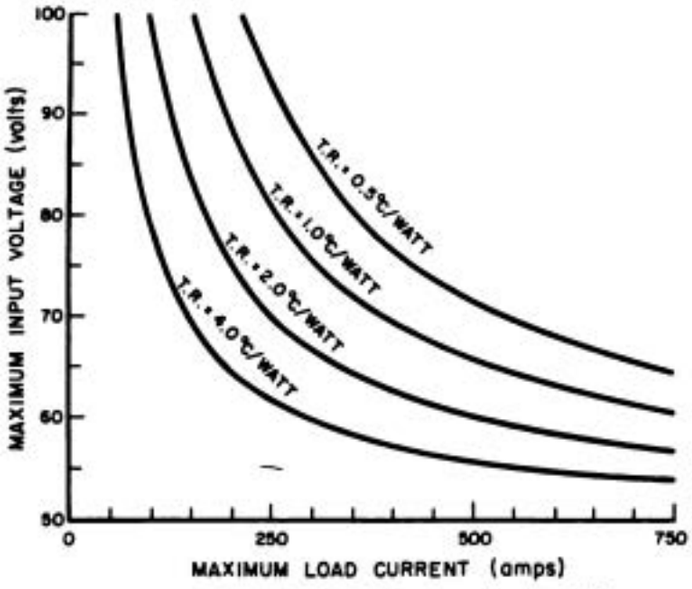
To achieve a relatively low thermal resistance, Q1 must be mounted on a heat sink. The thermal resistance form transistor case to ambient air is then the sum of the thermal resistance from transistor case to heat sink and from heat sink to ambient air. With suitable heat-conducting compounds and adequate mounting pressure, the former can be made quite small. The major consideration then becomes the thermal resistance from heat sink to ambient air.[3]

The four variables, maximum input voltage, maximum load current, maximum ambient temperature, and thermal resistance from Q1 case to ambient air, are interrelated for the user in figure 4–2. Voltage and current limits are shown as a function of thermal resistance at ambient temperatures of 65°C, 55°C, and 45°C. As an example, Figure 4–2(a) shows that if the maximum input voltage is 64.4 volts, the thermal resistance from Q1 case to ambient air must be 0.5°C/watt to permit circuit operation at the absolute maximum 750-ma load current and 65°C ambient temperature ratings.

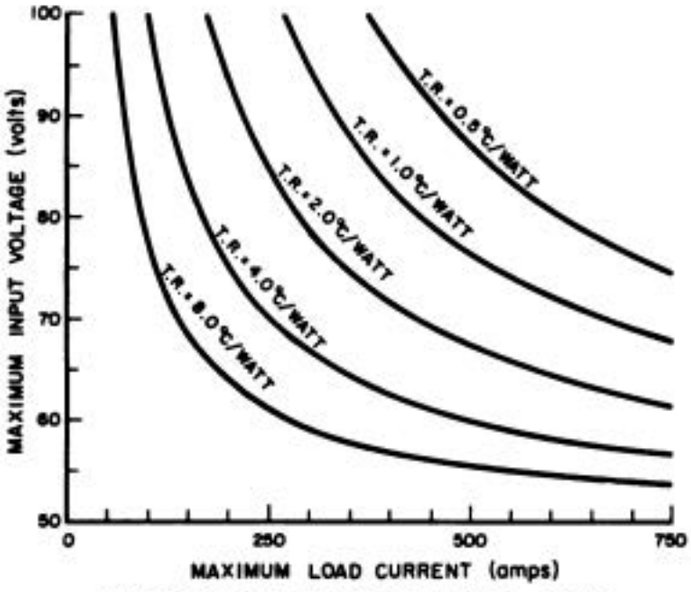
Emitter follower, Q2, must also be mounted on a heat sink, although the power dissipated

[2] Thermal resistance is defined as the resistance offered by a material to the flow of heat from a point of higher thermal potential (transistor case) to a point of lower thermal potential (ambient air) and is expressed as the ratio of the thermal potential difference (degrees centigrade) to the thermal energy flow (watts). For a discussion of thermal resistance, refer to C. Webber, "Thermal Resistance Determines Power Safely Dissipated at a Collector Junction", *Electronic Design*, Volume 8, Number 21, October 12, 1960, pp. 52, 53.

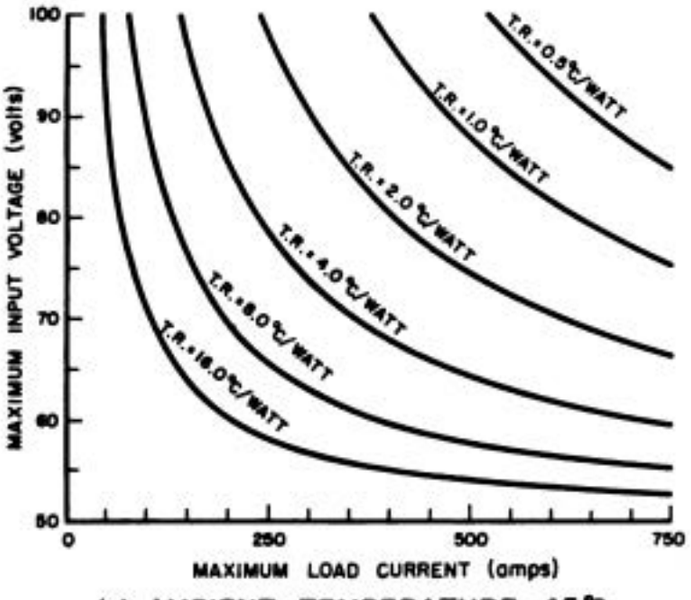
[3] This quantity depends upon a number of factors which include the size, shape, material, and orientation of the heat sink, and the amount of air flow past it. The first three factors are predetermined for a commercial heat sink so that a specification of thermal resistance as a function of air flow and/or orientation generally accompanies the commercial unit. Thermal resistance is not always specified directly and may need to be determined from a graph which shows the temperature rise across the heat sink for a given power dissipation by the heat sink. The user who wishes either to develop his own heat sink or to determine the thermal resistance of an unknown heat sink may refer to W. Luft, "Taking the Heat Off Semiconductor Devices", *Electronics*, Volume 32, Number 24, June 12, 1959, pp. 53–56.



(a) AMBIENT TEMPERATURE = 65°C



(b) AMBIENT TEMPERATURE = 55°C



(c) AMBIENT TEMPERATURE = 45°C

in it is considerably less than that in the series transistor, Q1. However, if the thermal resistance from the case of Q2 to ambient air is more than 5 times that from the case of Q1 to ambient air, the dissipation limit of Q2 becomes the controlling factor and Figure 4-2 no longer applies.

Absolute maximum load current is limited by the amount which the sampling divider can be loaded without affecting the voltage comparison; absolute maximum ambient temperature is determined by reverse current considerations in the differential amplifier. These effects are discussed in PSC 1, Section 2.6. Absolute maximum input voltage is limited by voltage breakdown in Q1 and Q2. This is discussed in the following section.

2.6 *Prevention of Voltage Breakdown in Q1 and Q2:* The collector-emitter voltage of Q1 and Q2 must not exceed 50 volts, since a larger voltage, even instantaneously, may result in voltage breakdown of either or both transistors. Regulator diode Z1 is placed across the series control element to prevent voltage breakdown upon: (1) application of input power, (2) removal of the auxiliary voltage before removal of the input voltage, or (3) short circuit of the output terminals. It furnishes protection under transient conditions only; other means must be provided for the subsequent removal of input voltage under conditions (2) or (3). The breakdown voltage of Z1 must not be greater than 50 volts, and, to prevent shorting the series control element under steady-state conditions, must not be less than the maximum steady state drop across the series element (the difference between maximum input voltage and 50 volts).

2.7 *Additional Steady-State Design Considerations:* The following paragraphs contain additional regulator design information based on steady-state conditions of input voltage and load current. Among the items discussed are I_{co} compensation, output-voltage adjustment range, reference voltage choice, and stability against environmental change.

Figure 4-2.—Maximum input voltage vs. maximum load current as a function of thermal resistance (T.R.) from series transistor case to ambient air.

(a) Emitter followers: Q2 and Q3 serve as current amplifiers and do not contribute to the voltage amplification of the feedback circuit. Their function is to amplify the relatively low current output of the high output impedance differential amplifier, Q4,Q5, to provide sufficient current drive for the low impedance base input of the series control element, Q1.

Resistors R1 and R2 furnish a path for I_{co} flow in Q1 and Q2, respectively. This assures output regulation down to zero load current, even at elevated temperatures. Without a path for I_{co} flow, regulation would cease when load current became less than either $\beta_1 I_{co1}$ or $\beta_1\beta_2 I_{co2}$ where β_1, β_2, I_{co1}, and I_{co2} are the current amplification and collector-base reverse current, respectively, for Q1 and Q2. At room temperature or lower, when I_{co} is negligible, current flow through R1 and R2 is added to the collector current of Q2 and Q3, respectively.

The maximum I_{co} flow in Q3 must be small to reduce the effect which a change of I_{co3} with temperature has on the differential amplifier, Q4,Q5. Small I_{co3} is achieved by arranging the circuit to use a low-power transistor with relatively low I_{co} for Q3. The collector current for Q3 is furnished from the auxiliary supply rather than from the unregulated input so that the voltage drop across Q3 and hence the power Q3 must dissipate may be limited by Z5. This configuration also prevents saturation of Q3, thereby allowing a lower minimum voltage drop across the series control element.

Regulator diode Z2 is included to prevent failure of Q3 should removal of the unregulated input voltage precede removal of the auxiliary supply voltage. Protection is required for the transient conditions only, hence a low-power regulator diode may be used.

(b) Comparison circuit: A differential amplifier comparison circuit, Q4,Q5, is used to reduce the disadvantages inherent in a single transistor configuration. Base-emitter voltage variations with temperature in one transistor of the differential amplifier tend to cancel similar variations in the other. Both the reference element, Z3,Z4, and the sampling divider, R9,R10,R11, are subject to very small current changes, since each may be located in a base circuit as opposed to the single transistor configuration, where one must be located in the emitter circuit. Resistor R5 is added to the base circuit of Q4 to minimize output voltage change with variation in transistor collector-base reverse current, I_{co}, caused by temperature changes. A change in the I_{co} of Q5 causes the voltage division of the sampling divider to change. This would give a false indication of output voltage if the similar change in the I_{co} of Q4 flowing through R5 did not produce a change in Q4 base voltage which tends to offset the change in sampling divider output. The comparison circuit is discussed more completely in PSC 1, Section 2.7(b).

(c) Reference element: The stability of the reference element, Z3,Z4, and of the sampling divider resistors, R9, R10, and R11, primarily determines regulator stability with time and with changes of environment. Two voltage reference diodes in series, each having a low temperature coefficient and a low dynamic impedance, are used for the reference element. Since the current drawn by these diodes is many times larger than the maximum base current of Q4, base current variations do not affect the reference voltage. Resistor R3 should be temperature stable to assure constant reference current; its initial tolerance is not so important as its subsequent stability against environmental changes.

The choice of reference voltage is determined primarily by the reference diodes available. Ideally, the magnitude of the reference voltage should be as near as possible to the magnitude of the regulated output voltage.[4] Regulator diodes with a breakdown voltage in the 40- to 50-volt range are available, but due to the nature of this device, their temperature coefficient and dynamic impedance are both larger than those of the lower voltage, temperature-compensated reference diodes. The benefit derived from a large reference voltage is thus lost due to the reduced stability of this voltage. PSC 4 uses a temperature-compensated 8.4-volt reference diode, the IN3157,

[4] Before application to the comparison circuit, any change in regulated output voltage is reduced by a factor approximately equal to $V_Z E_s$ where V_Z is the reference voltage. This reduction may also be expressed as a function of the sampling divider, R9,R10, R11, but the result is unnecessarily complicated by potentiometer R10.

whose low dynamic impedance and low temperature coefficient make it ideally suited for use as the reference element. Two of these diodes are connected in series to give a somewhat larger reference voltage while maintaining good stability.

(d) Sampling divider: The regulated output voltage is sensitive to any change in the sampling divider resistors, R9, R10, and R11. The initial tolerance of these resistors is not so important as their subsequent stability against environmental changes. Resistors whose wattage ratings are very conservative should be used, and to insure that the ratio of the resistances remains relatively constant, the wattage ratings of R9 and R11 should be in the same ratio as the actual power dissipation.

The range of adjustment required in potentiometer R10 is determined primarily by the permissible operating voltage tolerance of the reference element, although some additional range is required to cover the initial tolerance of R9 and R11. By using 1% tolerance resistors for R9 and R11, the required adjustment range is minimized, assuring easy adjustment of the output voltage to 50 volts, and the prevention of gross misadjustment.

2.8 *Dynamic Design Considerations:* In an ideal voltage regulator, output voltage regulation for changes of input voltage or load current would be independent of the frequency of change. In a practical regulator, of course, this is not the case. Due to the frequency limitations of the transistors used in PSC 4, the negative feedback loop begins to lose control of the output voltage at frequencies above 5 kc. Reduction of output voltage variations at frequencies above 60 kc depends essentially upon output capacitor C3, while output voltage control at frequencies between 5 kc and 60 kc is a combined function of the negative feedback loop and the output capacitor.

Phase shift present in the high-gain negative feedback loop at frequencies above 5 kc might be sufficient to cause oscillation if it were not for R4 and C1, which reduce the amplification of the feedback loop over this range of frequencies, thus preventing oscillation. By themselves, however, R4 and C1 would also cause some loss of low frequency amplification and hence less ripple reduction. Capacitor C2 counteracts this loss by improving the sampling ratio of the comparison circuit [5] for ac variations. The combination of R4, C1, and C2 thus provides protection against the possibility of oscillation without sacrificing regulator performance.

These components would not be necessary if doubling the value of output capacitor C3 were feasible, since C3 could then decrease the signal fed to the differential amplifier at frequencies above 5 kc sufficiently to prevent oscillation. To achieve the large capacitance at the required voltage rating, however, would require the paralleling of at least six smaller capacitance units. Economics and space factors negate this solution. The use of higher frequency transistors would permit the use of a smaller value for C3, but germanium transistors of this type do not have the necessary power ratings.

Output capacitor C3 must be a tantalum type for operation at low temperatures. The decrease of apparent capacitance caused by the increase of series resistance at low temperature is prohibitively large for any other electrolytic type.

2.9 *Mechanical Construction:* Certain precautions should be taken in the construction of PSC 4 to assure maximum performance. Mechanical construction will affect steady-state regulation for load variations, and could be a factor in determining transient regulation characteristics.

Due to the high maximum load current, care should be taken to keep contact and lead resistance to a minimum along the positive and negative output busses. Maximum steady-state regulation for load variations is achieved when physical contact between the sampling divider, R9,R10,R11, and the output busses is made at the regulator output terminals. To achieve approximately the same regulation at the load, the lead resistance between output terminals and the load must be kept to a minimum. When small lead resistance between regulator and load is physically impossible, steady-state regulation for load current changes can be maximized at the load by use of remote sensing, as described in PSC 1, Section 2.9.

Best transient regulation is achieved when output capacitor C3 is physically connected,

[5] *Ibid.*

along with the sampling divider, to the regulator output terminals, and when the capacitor leads are kept as short as possible. This reduces lead inductance, which raises regulator output impedance at high frequency and causes a large voltage spike to accompany a step change in either input voltage or load current. To achieve best transient regulation at the load, lead inductance between regulator output terminals and the load must be kept to a minimum. Since this may be physically impossible, a second output capacitor placed directly across the load can be used to compensate for the lead inductance between regulator and load.

For minimum load transient recovery time, the lead resistance between load and output capacitor C3 should be a minimum. This reduces the charging and discharging time for C3.

3. PERFORMANCE

PSC 4 is designed to furnish a supply voltage with percentage variation not exceeding 1% at output currents from zero to 750 ma and ambient temperatures from −55 to +65°C. Whether circuit operation is possible at these absolute maximum ratings for load current and ambient temperature depends upon the heat dissipating quality of the heat sink and the maximum input voltage for the particular application. The minimum input voltage is 50.8 volts, and the maximum input voltage must not exceed either 100 volts or the sum of Z1 breakdown voltage plus 50 volts. Ripple or transients which reduce the input voltage to a value lower than the specified minimum of 50.8 volts will reverse-bias the series control element causing spikes to appear in the output voltage. Ripple or transients which increase the input voltage to a value larger than the sum of Z1 breakdown voltage plus 50 volts will cause Z1 to conduct, shunting the series control element. Refer to Sections 2.5 and 2.6 for a more detailed discussion of voltage, current, and temperature limits.

3.1 *Stability and Steady-State Regulation:* Steady-state regulation (as contrasted to dynamic or transient regulation) is defined as the maximum variation of output voltage after all transients have subsided, when either the input voltage, load current, or auxiliary supply current is varied between specified maximum and minimum values. The regulation is expressed as a precentage of the nominal output voltage. Stability is defined as the constancy of output voltage with environmental change and time. The *total* steady-state regulation plus stability of PSC 4 is ±1%, i.e., the sum of the individual percentage variations in output voltage due to changes of input voltage, load current, auxiliary supply current, and ambient temperature will not exceed ±1% of the nominal output voltage over an 8-hour period.

Figure 4–3 shows typical variation in output voltage as a function of input voltage, load current, ambient temperature, and auxiliary supply current. Stability of the output voltage with time could not be included in the figure, but variations in the output voltage were determined to be less than ±0.05% for an 8-hour period. The data in the figure are independent of the heat sink used, provided it can adequately dissipate the power involved. The measurements at high voltage and current were made instantaneously to avoid excessive collector dissipation and the consequent dependence of output voltage variation on the thermal resistance from transistor case to ambient air.

Total steady-state regulation plus stability for a particular regulator may differ from the value (approximately ±0.3%) shown in Figure 4–3 but the direction and general magnitude of output voltage variation with input voltage, load current, and auxiliary supply current will be similar to that shown. Output voltage variation with ambient temperature for a particular regulator is not as predictable, but it will not exceed the specified ±0.01% per degree centigrade. Figure 4–3 shows the temperature coefficient to be approximately equal to +0.007% per degree centigrade between 25°C and 65°C, and approximately equal to +0.003% per degree centigrade between 25°C and −55°C.

Since regulation for input voltage changes, i.e., the slope of the lines representing constant load current in Figure 4–3, is poorest at large load current, the ±0.03% regulation specified on page 4–3 is for maximum load current. Regulation for load current changes, i.e., the vertical distance between curves representing constant load current, is poorest for low input voltages, and the ±0.2% specified is for mini-

mum input voltage. Regulation for auxiliary supply current variation (determined from Figure 4-3 by comparing the position of dotted and solid curves) is relatively independent of input voltage and load current. Current rather than voltage is used as the auxiliary supply variable, since both maximum and minimum limits are placed on the current drawn from the auxiliary supply, while the voltage may be any value larger than the minimum necessary to operate Z5.

The steady-state condition is achieved much more quickly after a change in either input voltage, load current, or auxiliary supply current than after a change in ambient temperature. Since each component part may have a different thermal time constant, the initial variation of output voltage with temperature may be larger than, or in a direction opposite to, the final steady-state value. The time required to reach temperature equilibrium depends primarily upon the rate of heat transfer for the particular application. At no time, however, will the output voltage variation with temperature exceed the $\pm 0.01\%$ per degree centigrade specified.

3.2 *Transient Regulation:* Transient regulation is defined as the difference between the maximum instantaneous variation of the output voltage in response to a positive or negative step change of input voltage or load current, and the steady-state voltage excursion which remains after all transients have subsided, expressed as a percentage of the nominal output voltage. This regulator characteristic, often unspecified, is of considerable importance if the regulator furnishes power to semiconductor circuits. Voltage transients exceeding the normal "regulation" can be fatal to semiconductors operated near their maximum voltage limit.

Transient regulation is specified as a function of ambient temperature, since the user may obtain better performance by limiting the minimum ambient temperature. Transient regulation is a function of output capacitor C3, which becomes less effective as the temperature decreases. As in the case of the corresponding steady-state regulation, transient regulation for input voltage changes is poorest at maximum load, and transient regulation for load current

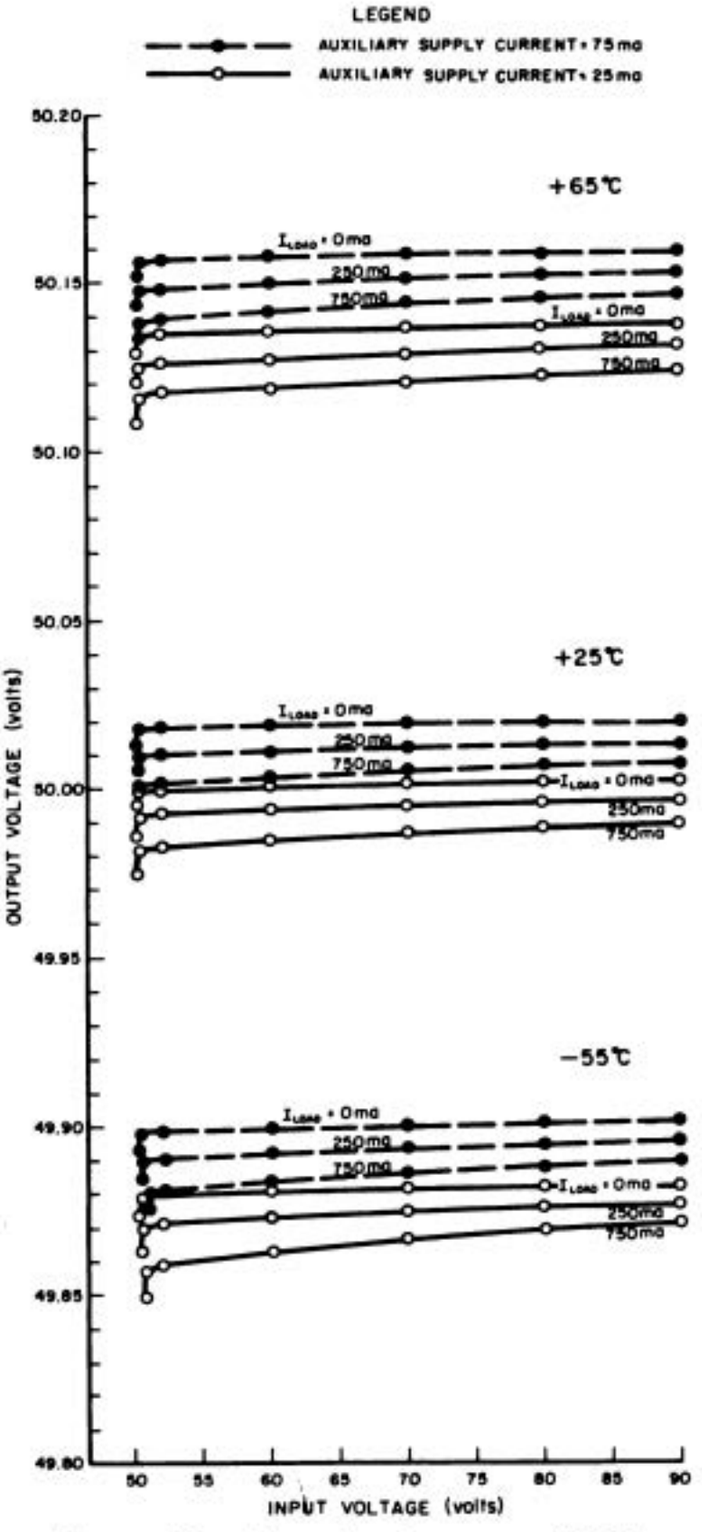


Figure 4-3.—Typical performance of PSC 4.

changes is poorest at minimum input. The values specified on page 4-3 are for these "worst" conditions. Optimum mechanical construction as specified in Section 2.9 is assumed, however.

Transient recovery time is defined as the interval from the application of a specified step change in either input voltage or load current to the time when the output voltage reaches and remains within the specified steady-state

tolerance. The transient recovery time is less than 50 μsec after step changes of input voltage and less than 100 μsec after step changes of load current.

3.3 *Ripple Reduction:* The output ripple voltage must be specified in terms of the ripple voltage applied to PSC 4 both from the unregulated power source and from the auxiliary voltage supply. The ripple reduction figure specified for each indicates the amount by which the applied ripple voltage is reduced. Each depends somewhat upon the ripple frequency because of R4, C1, and C2, but the figures quoted are the minimum values for any frequency from 0 to 800 cps. Larger values of both types of ripple reduction may be achieved by increasing the value of C2.

Input ripple reduction is defined as the ratio of the ac ripple present in the input voltage to the resulting ac ripple present in the output voltage at a specified ripple frequency. It is a function of the amplification in the negative feedback loop and of the small-signal forward voltage transfer ratio[6] of Q1, and is poorest at maximum load current and minimum input voltage. Maximum load current is accompanied by maximum control current to the base of Q3, which loads the differential amplifier and reduces the loop amplification. Minimum input voltage results in minimum voltage between the collector and emitter of Q1 and an accompanying low small-signal forward voltage transfer ratio. Input ripple reduction is 1000 at a load of 750 ma and an input of 51 volts. This increases to 2000 if either the load is decreased to 100 ma or the input voltage is increased to 53 volts.

Auxiliary supply ripple reduction is defined as the ratio of the ac ripple present in the auxiliary supply voltage to the resulting ac ripple appearing in the output voltage at a specified ripple frequency. It is a function of resistor R8, the current drawn from the auxiliary supply, and the voltage amplification provided by the differential amplifier. Since the first two are determined by the user, the auxiliary supply ripple reduction may be selected to fit the application (see Section 2.4 and Figure 4–1).

[6] Small-signal forward voltage transfer ratio is defined as the ratio of ac collector-emitter voltage to ac base-emitter voltage at constant collector current.

3.4 *Output Impedance:* Output impedance may be defined as the internal impedance, expressed in ohms, appearing at the output terminals of a power supply at any given frequency. A low value for this impedance is desirable in order to minimuze feedback between circuits through the supply voltage source. Low output impedance also permits good output voltage regulation for changes in load current.

Figure 4–4 is an impedance vs. frequency curve for an ambient temperature of 25°C. Output impedance is shown for load currents of 100, 250, and 750 ma. Below a frequency of approximately 5 kc, impedance is a function of amplification in the negative feedback loop and the small-signal forward transconductance[7] of Q1. Within this range, output impedance increases as current decreases, because the forward transconductance deteriorates considerably at low currents. At frequencies above 5 kc, the feedback loop begins to lose control and output capacitor C3 begins to take over. Above approximately 60 kc, the output impedance is essentially a function of the output capacitance and associated lead inductance. The hump in the impedance curve lies between the frequencies where the feedback loop begins to lose effectiveness and where output capacitor C3 takes over completely. The size of the hump, which indicates the tendency of the circuit to oscillate, has been reduced by the addition of resistor R4 and capacitor C1. The hump is more pronounced for large load currents because of increased phase shift in the feedback loop.

Curve A represents the output impedance when C3 is located a short distance away from the regulator output terminals. The rise in impedance is due to a lead inductance of approximately 0.2 μh. Curve B represents the impedance when C3 is located directly across the output terminals.

At high temperature the curves are much the same as those shown in Figure 4–4. Impedance at frequencies below 20 kc may increase slightly due to decreased loop effectiveness, but high frequency impedance should remain unaffected. At low temperatures, however, the high frequency impedance may rise consid-

[7] Small-signal forward transconductance is defined as the ratio of ac collector current to ac base-emitter voltage at constant collector-emitter voltage.

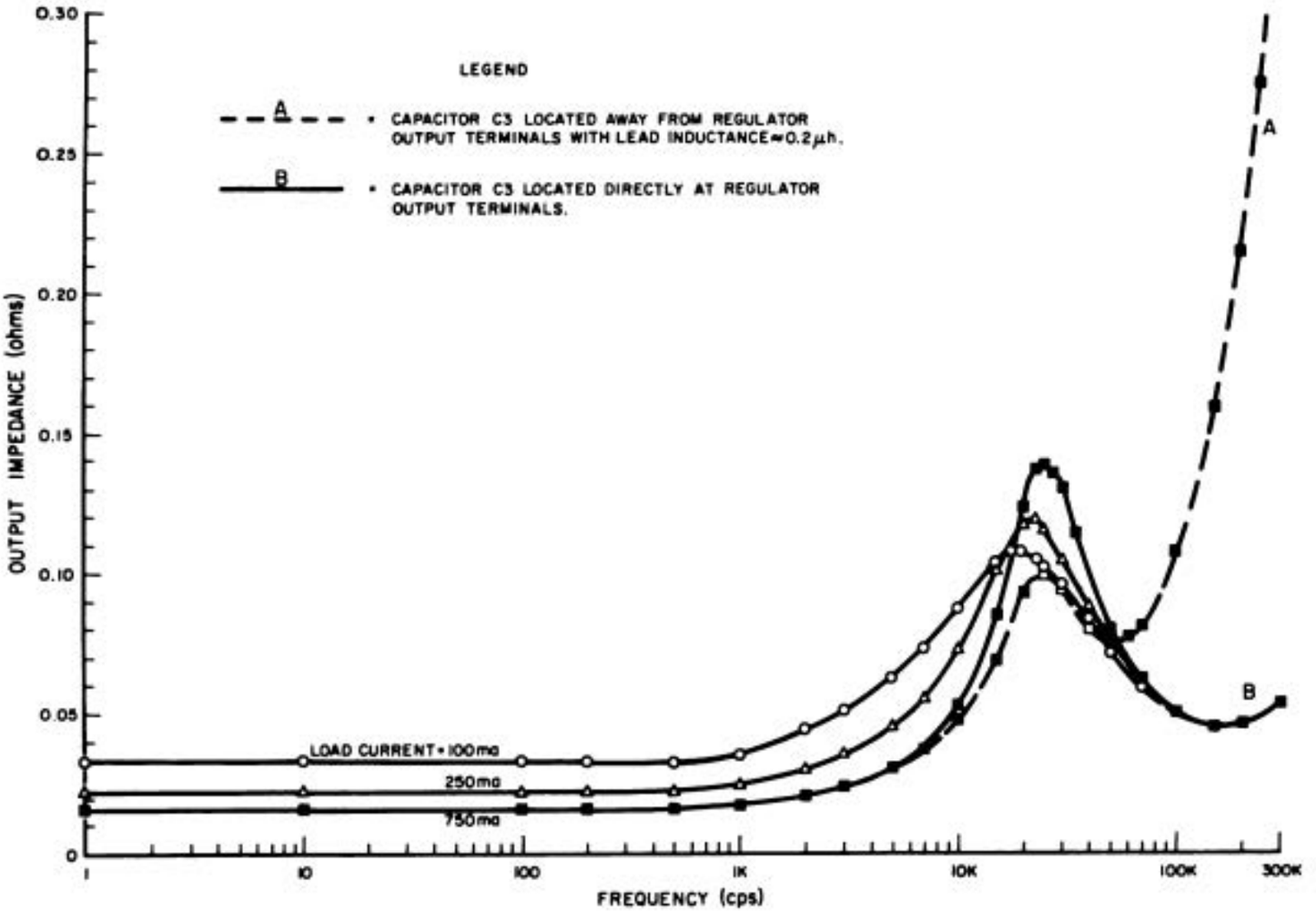


Figure 4-4.—Output impedance as a function of frequency and dc load.

erably due to the reduced effectiveness of output capacitor C3.

3.5 *Warm-Up Time:* Warm-up time is the interval between the application of input power and the instant at which the output voltage reaches and stays within its $\pm 1\%$ steady-state tolerance. It is primarily a function of the relative wattage ratings on voltage divider resistors R9 and R11, and is less than 2 msec if the wattages are correctly chosen. A maximum of 5 minutes may be required for the output voltage to remain within its $\pm 0.05\%$ stability vs. time rating, however. No output voltage transient accompanies the application of input power.

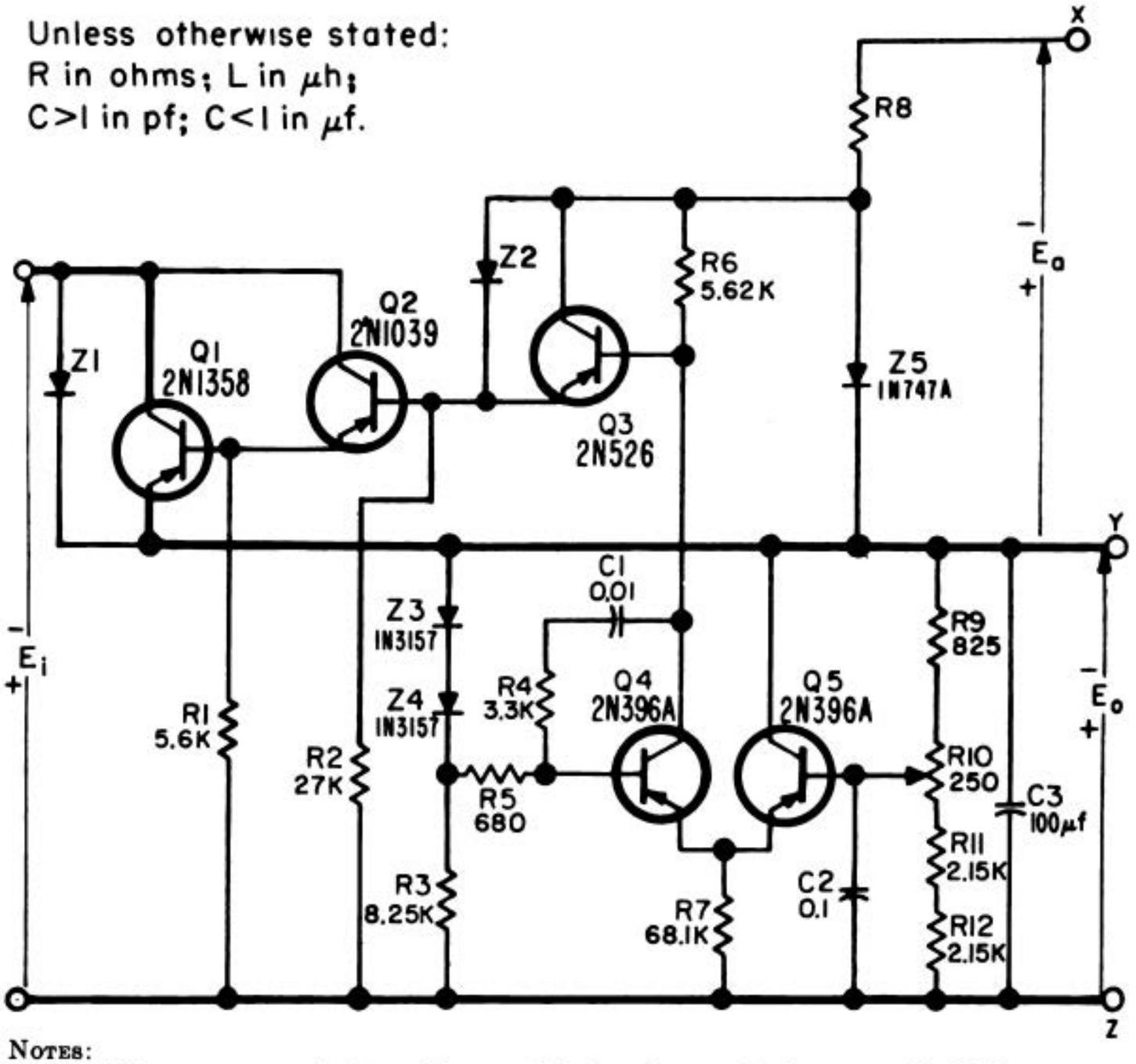
Notes

PREFERRED CIRCUIT NO. PSC 5

DC REGULATOR ±100 VOLTS: 1% REGULATION

PREFERRED CIRCUIT NO. PSC 5

DC REGULATOR FOR ±100 VOLTS: 1% REGULATION



NOTES:

A. Either output terminal may be grounded, but the negative input terminal, W, must not be grounded.

B. The auxiliary supply, E_a, may be returned to the positive output terminal, Z, instead of to the negative terminal, Y, as shown. A floating auxiliary supply is necessary if return is made to the ungrounded output terminal. See Section 2.4.

C. Transistors Q1 and Q2 must be mounted on a heat sink. A clip-on heat sink should be used with Q3 for increased reliability. See Section 2.5.

D. Contact and lead resistance should be kept to a minimum along the positive and negative output busses. See Section 2.9.

Components:

Z1: Breakdown voltage not greater than 50 volts nor less than the voltage drop across the series control element (input voltage minus 50 volts). Power rating not less than 3 watts at 65°C. Suggested types: 1N2970B through 1N2995B or 1N2804B through 1N2829B.

Z2: Breakdown voltage between 5 and 20 volts. Power rating not less than 250 mw at 65°C. Suggested types: 1N752A through 1N758A or 1N962B through 1N967B.

Components—*Continued*

R8: Resistance and power dissipation are determined by the auxiliary supply voltage and the limits on auxiliary current. See Section 2.4.

R9, R11, R12: Percentage change in the ratio of R9 to R11 + R12 due to environmental changes must be less than ±1% to obtain the output regulation specified. Initial tolerance of each may be ±1%. Power dissipation rating must be conservative and chosen so that watts per ohm are approximately equal for the three resistors.

R10: Percentage change in resistance due to environmental changes must be less than ±5% to obtain the output regulation specified. Initial tolerance may be ±10%.

C3: This capacitance may be obtained by paralleling several smaller units. A tantalum capacitor is required for reliable operation at low temperature. At 25°C the capacitance should not be less than 80 μf. At −55°C the decrease in apparent capacitance should be less than 20%, and the increase in series resistance should be less than 10 times.

Maximum power dissipation (Note 1): R1: 2.2 watts; R2: 0.5 watt; R3: 1.0 watt; R4, R5, R6: <0.01 watt; R7, R10: 0.12 watt; R8: see above; R9: 0.3 watt; R11, R12: 0.8 watt.

Limits (these are not tolerances; see Note 2): R1, R2, R4, R5: ±20%; R3: ±2%; R6, R7: ±5%; R8, R9, R10, R11, R12: see above; C1: ±30%; C2: +100%, −30%; C3: see above.

Power requirements:

Input from unregulated source:

Voltage, E_i: Minimum, 100.7 volts. Maximum is dependent upon the thermal resistance of the heat sink, the maximum load current, and the maximum operating temperature for the particular application (see Section 2.5 and Figure 5-2). Absolute maximum, 150 volts.

Current, I_i: 450 ma maximum.

Auxiliary supply:

Voltage, E_a: Minimum 5 volts (Note 3). Maximum, not limited. The voltage may be unregulated.

Current, I_a: Minimum, 25 ma. Maximum, 75 ma. (Limits determined by Z5 and controlled by proper selection of R8. See Section 2.3.)

Operating characteristics:

Temperature range: −55°C to +65°C (see Section 2.5 and Figure 5-2).

Output voltage: 100 volts, positive or negative.

Output current: 0 to 400 ma (see Section 2.5 and Figure 5-2).

Total steady-state regulation plus stability (see Section 3.1): ±1%.

Regulation for input voltage variation between 101 and 150 volts: ±0.02%.

Regulation for load current variation between 0 and 400 ma: ±0.1%.

Regulation for auxiliary supply current variation between 25 and 75 ma: ±0.1%.

Temperature stability: ±0.01% per °C.

Time stability (8 hour period): ±0.05%.

Transient regulation (see Section 3.2):

Regulation for input voltage changes: ±0.3% at 25°C, ±1% at −55°C.
(Input voltage change between 101 and 150 volts in 0.02 μsec.)

Regulation for load current changes: ±0.3% at 25°C, ±1% at −55°C.
(Load current change between 0 and 400 ma in 1.0 μsec.)

Transient recovery time (see Section 3.2):

After input voltage changes: 50 μsec.

After load current changes: 100 μsec.

Input ripple reduction (Note 4): >1000.

Output impedance at 25°C: <0.1 ohm, dc to 1 kc; <0.2 ohm, 1 kc to 5 kc; <0.5 ohm, 5 kc to 300 kc.

(For Notes, see bottom of next page)

PSC 5 DC REGULATOR ±100 VOLTS: 1% REGULATION

1. APPLICATION

PSC 5 is intended for use with an unregulated dc power source to provide a supply voltage stabilized against changes of source voltage, load current, and environmental conditions (notably temperature). Ripple reduction and low output impedance are furnished as a by-product of the above criteria. PSC 5 will supply up to 400 ma at 100 volts and is designed for applications requiring less than 1% supply voltage variation together with low power loss across the regulating element.

The 1% regulation specified includes output voltage stability with time (for periods up to 8 hours) and with changes of environment; it does not include extremely short duration output voltage transients resulting from large step changes of input voltage or load current. Transient regulation is 1% for a ±20% step change of input voltage, or for a zero to maximum step change in load. The duration of the transient will not exceed 50 μsec for step changes of input voltage and 100 μsec for step changes in load current.

Overload and short circuit protection is not included in PSC 5 for reasons of simplicity and efficiency. Should this characteristic be required, it may be added to the circuit[1] or supplied externally by relay control.

2. DESIGN CONSIDERATIONS

2.1 *Basic Regulator Circuit:* PSC 5 is a series regulator (control element in series with load) employing negative feedback for control of the output voltage. Transistor Q1 is the series control element; Q2 and Q3 are emitter followers which match the output impedance of the voltage amplifier to the input impedance of the series control element; Q4 combined with Q5 is a differential amplifier which forms the comparison circuit and develops the voltage amplification of the feedback loop; R9, R10, R11, and R12 comprise the sampling circuit; and voltage reference diodes Z3 and Z4 comprise the reference element. Refer to PSC 1, Section 2.1, for a discussion concerning the choice of this regulator type and an explanation of its basic operation. Detailed operation of the circuit is described in Section 2.2 of PSC 3.

The circuit configuration is identical to that of PSC 4 except that two resistors, R11 and R12, are used in the lower arm of the sampling divider. This is necessary because of the larger power dissipated in the sampling divider of PSC 5.

2.2 *Selection of Transistor and Diode Types:* Germanium transistors are used throughout because of their present price advantage over similar silicon units and their lower base-emitter voltage drop. The maximum operating temperature, although lower than that which may be obtained with silicon units, is satisfactory for many applications. PNP types are specified, although similar NPN types, if and when available, could be used equally well by reversing the polarity at all input and output terminals. Three of the four transistor types have been on the Military Preferred and

[1] C. A. Franklin, P. M. Thompson, and W. M. Caton, "Precision High-Voltage Transistor-Operated Power Regulators with Overload Protection", *The Proceedings of the Institution of Electrical Engineers*, Volume 106, Part B, Supplement No. 16, May, 1959, pp. 714–725.

NOTES:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than a specified amount. For the components listed here, only the total deviation is important. Thus the specified maximum deviation, termed "limits", includes initial tolerance plus drifts caused by environmental changes or aging.

3. The minimum is 105 volts if the auxiliary supply is returned to the positive terminal, Z.

4. Input ripple reduction is the ratio of ac ripple present in the input voltage to the resulting ac ripple present in the output voltage for any ripple frequency between 0 and 800 cps.

Guidance List of Transistors and Diodes (MIL-STD-701) since September, 1959, with every indication that they will remain. The fourth type, the 2N1358, is an electrical equivalent which replaces the 2N174 on MIL-STD-701B. The reasons for the selection of these transistor types are given in PSC 1, Section 2.3.

Regulator diode types for Z1 and Z2 are not specified because a number of different types will meet the given requirements. Of the types appearing on MIL-STD-701B, the series 1N2970B through 1N2995B or 1N2804B through 1N2829B will satisfy the requirements for Z1, and the series 1N752A through 1N758A or 1N962B through 1N967B will satisfy the requirements for Z2. The reference element, Z3,Z4, must be an extremely stable, temperature compensated unit. The 1N3157 is specified, but the 1N3156, a similar unit with slightly less temperature stability which does not appear on MIL-STD-701, is perfectly satisfactory for use in PSC 5.

2.3 *Regulator Efficiency:* The voltage drop across the series control element is minimized by use of an auxiliary power supply, E_a. This reduces the power loss in the series element and maximizes regulator efficiency. These improvements are discussed in PSC 1, Section 2.4. The voltage drop across the series element may be as small as 0.7 volts without causing Q1 to lose control of the output voltage.

A single series transistor is used rather than two or more in parallel. Although larger load currents may be handled by a parallel combination, a loss of efficiency results due to the power dissipated in current balancing resistors, which must be added in series with each emitter. Additional emitter followers are also necessary to handle the increased control current.

2.4 *Requirements for Auxiliary Voltage Supply, E_a:* The auxiliary voltage supply may be either regulated or unregulated. Choice of nominal voltage and degree of regulation is left to the user so long as the auxiliary current can be maintained within the stated 25- to 75-ma by selection of R8. The minimum auxiliary current is that necessary to keep regulator diode, Z5, operating in a range of relatively low dynamic impedance; the maximum auxiliary current is determined by the maximum permissible power dissipation in Z5 at high temperature.

The characteristics of resistor R8 should be such that initial tolerance and environmental effects will not cause its resistance to exceed the limits indicated below,

$$\frac{E_{a_{min}}-3.6}{.025} \geqq R8 \geqq \frac{E_{a_{max}}-3.6}{.075}$$

where R8 is in ohms and E_a is the voltage of the auxiliary supply selected by the user. The inequality allows for variation of E_a from its nominal value. In the term to the left, the numerator is the minimum voltage which will appear across R8, and the denominator is the minimum current, in amperes, which must be furnished by the auxiliary supply. In the term to the right, the numerator is the maximum voltage which will appear across R8, and the denominator is the maximum current which the auxiliary supply may furnish.

Auxiliary supply ripple reduction (the ratio of the ac ripple, e_a, present in the auxiliary supply voltage to the resulting ac ripple, e_{oa}, appearing in the output voltage) is proportional to RS/r_{zs}, where r_{zs} is the dynamic impedance of Z5. Since r_{zs} is a function of the current through the regulator diode, and since diode current is a function of the auxiliary supply current, I_a, ripple reduction is a function of both R8 and I_a as shown in Figure 5-1. This relationship should be kept in mind when choosing the auxiliary supply and the consequent value of R8.

The auxiliary supply is shown returned to the negative output terminal, Y, but may also be returned to the positive terminal, Z. If it is returned to the positive terminal, however, the auxiliary supply voltage must be 100 volts larger for a given auxiliary current, and a 50 ma minimum load is required to assure a return path for the auxiliary current.

2.5 *Determining Regulator Operating Range Limitations:* Circuit operation at the absolute maximum ratings specified for ambient temperature (65° C) and load current (400 ma) may not be possible in every application. Since the series transistor, Q1, may dissipate only a limited amount of power, the upper ratings for input voltage, load current, and

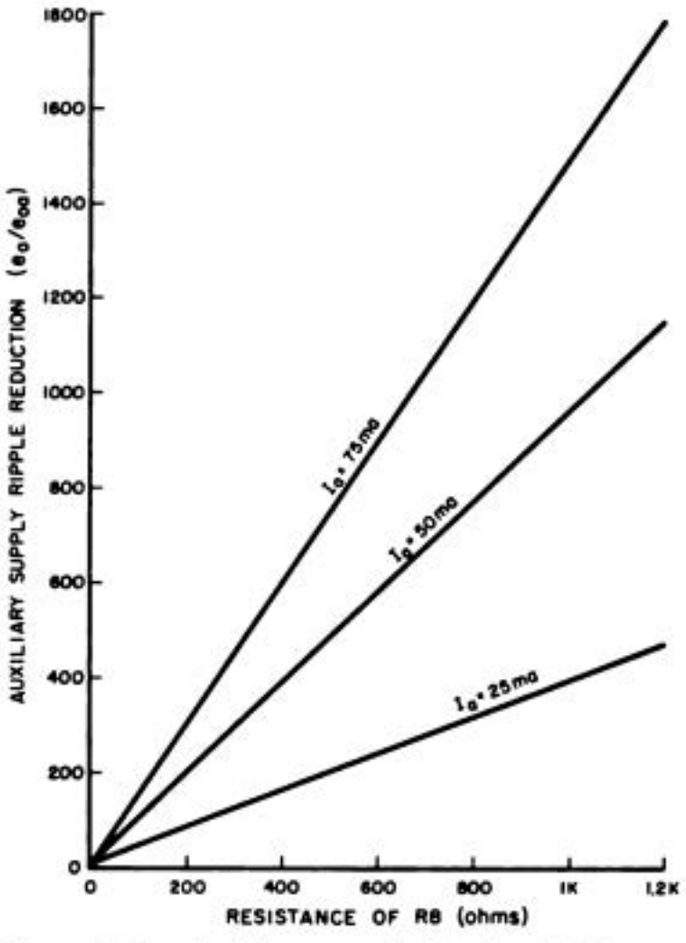


Figure 5–1.—Auxiliary supply ripple reduction as a function of R8 and auxiliary supply current, I_a.

ambient temperature are actually dependent variables, one of which may have to be sacrificed for the others, depending upon the particular application. Their order of magnitude depends upon the thermal resistance from Q1 case to ambient air.[2] A low thermal resistance allows each rating to be proportionately higher (up to the absolute maximum), while a high thermal resistance requires that each rating be proportionately lower.

To achieve a relatively low thermal resistance, Q1 must be mounted on a heat sink. The thermal resistance from transistor case to ambient air is then the sum of the thermal resistance from transistor case to heat sink and from heat sink to ambient air. With suitable heat-conducting compounds and adequate mounting pressure, the former can be made quite small. The major consideration then becomes the thermal resistance from heat sink to ambient air.[3]

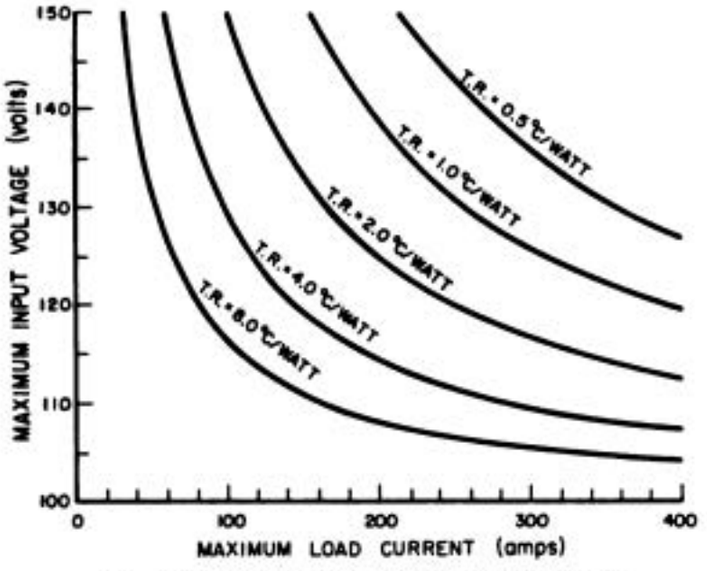
The four variables, maximum input voltage, maximum load current, maximum ambient temperature, and thermal resistance from Q1 case to ambient air, are interrelated for the user in Figure 5–2. Voltage and current limits are shown as a function of thermal resistance at ambient temperatures of 65°C, 55°C, and 45°C. As an example, Figure 5–2(a) shows that if the maximum input voltage is 127 volts, the thermal resistance from Q1 case to ambient air must be 0.5°C/watt to permit circuit operation at the absolute maximum 400-ma load current and 65°C ambient temperature ratings.

Emitter follower, Q2, must also be mounted on a heat sink, although the power dissipated in it is considerably less than that in the series transistor, Q1, However, if the thermal resistance from the case of Q2 to ambient air is more than 5 times that from the case of Q1 to ambient air, the dissipation limit of Q2 becomes the controlling factor and Figure 5–2 no longer applies.

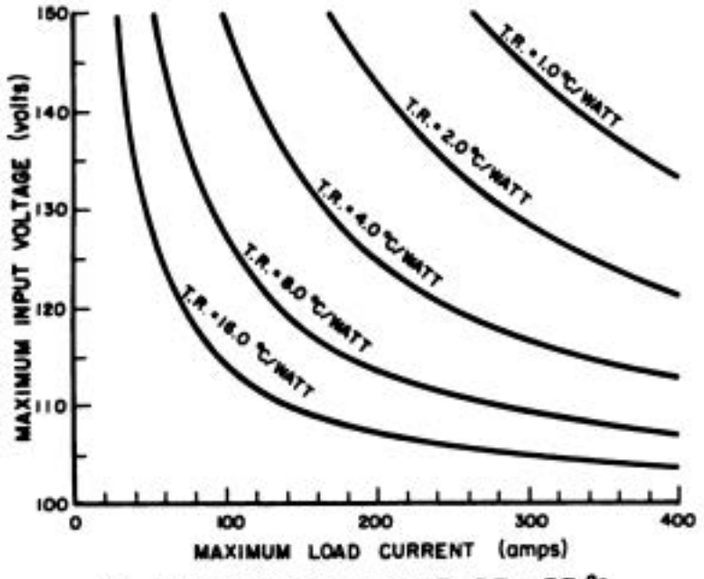
Absolute maximum load current is limited by the amount which the sampling divider can be loaded without affecting the voltage comparison; absolute maximum ambient temperature is determined by reverse current considerations in the differential amplifier. These effects are discussed in PSC 1, Section 2.6. Absolute maximum input voltage is limited by voltage

[2] Thermal resistance is defined as the resistance offered by a material to the flow of heat from a point of higher thermal potential (transistor case) to a point of lower thermal potential (ambient air) and is expressed as the ratio of the thermal potential difference (degrees centigrade) to the thermal energy flow (watts). For a discussion of thermal resistance, refer to C. Webber, "Thermal Resistance Determines Power Safely Dissipated at a Collector Junction", *Electronic Design*, Volume 8, Number 21, October 12, 1960, pp. 52, 53.

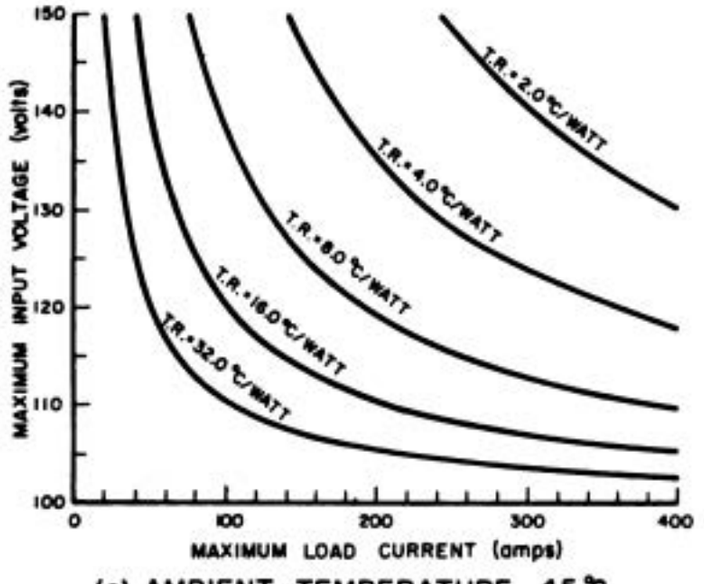
[3] This quantity depends upon a number of factors which include the size, shape, material, and orientation of the heat sink, and the amount of air flow past it. The first three factors are predetermined for a commercial heat sink so that a specification of thermal resistance as a function of air flow and/or orientation generally accompanies the commercial unit. Thermal resistance is not always specified directly and may need to be determined from a graph which shows the temperature rise across the heat sink for a given power dissipation by the heat sink. The user who wishes either to develop his own heat sink or to determine the thermal resistance of an unknown heat sink may refer to W. Luft, "Taking the Heat Off Semiconductor Devices", *Electronics*, Volume 32, Number 24, June 12, 1959, pp. 53–56.



(a) AMBIENT TEMPERATURE = 65 °C



(b) AMBIENT TEMPERATURE = 55 °C



(c) AMBIENT TEMPERATURE = 45 °C

Figure 5-2.—Maximum input voltage vs. maximum load current as a function of thermal resistance (T.R.) from series transistor case to ambient air.

breakdown in Q1 and Q2. This is discussed in the following section.

2.6 *Prevention of Voltage Breakdown in Q1 and Q2:* The collector-emitter voltage of Q1 and Q2 must not exceed 50 volts, since a larger voltage, even instantaneously, may result in voltage breakdown of either or both transistors. Regulator diode Z1 is placed across the series control element to prevent voltage breakdown upon: (1) application of input power, (2) removal of the auxiliary voltage before removal of the input voltage, or (3) short circuit of the output terminals. It furnishes protection under transient conditions only; other means must be provided for the subsequent removal of input voltage under conditions (2) or (3). The breakdown voltage of Z1 must not be greater than 50 volts, and, to prevent shorting the series control element under steady-state conditions, must not be less than the maximum steady state drop across the series element (the difference between maximum input voltage and 100 volts).

2.7 *Additional Steady-State Design Considerations:* The following paragraphs contain additional regulator design information based on steady-state conditions of input voltage and load current. Among the items discussed are I_{co} compensation, output-voltage adjustment range, reference voltage choice, and stability against environmental change.

(a) Emitter followers: Q2 and Q3 serve as current amplifiers and do not contribute to the voltage amplification of the feedback circuit. Their function is to amplify the relatively low current output of the high output impedance differential amplifier, Q4,Q5, to provide sufficient current drive for the low impedance base input of the series control element, Q1.

Resistors R1 and R2 furnish a path for I_{co} flow in Q1 and Q2, respectively. This assures output regulation down to zero load current, even at elevated temperatures. Without a path for I_{co} flow, regulation would cease when load current became less than either $\beta_1 I_{co1}$ or $\beta_1\beta_2 I_{co2}$ where β_1, β_2, I_{co1}, and I_{co2} are the current amplification and collector-base reverse current, respectively, for Q1 and Q2. At room temperature or lower, when I_{co} is negligible, current

flow through R1 and R2 is added to the collector current of Q2 and Q3, respectively.

The maximum I_{co} flow in Q3 must be small to reduce the effect which a change of I_{co3} with temperature has on the differential amplifier, Q4,Q5. Small I_{co3} is achieved by arranging the circuit to use a low-power transistor with relatively low I_{co} for Q3. The collector current for Q3 is furnished from the auxiliary supply rather than from the unregulated input so that the voltage drop across Q3 and hence the power Q3 must dissipate may be limited by Z5. This configuration also prevents saturation of Q3, thereby allowing a lower minimum voltage drop across the series control element.

Regulator diode Z2 is included to prevent failure of Q3 should removal of the unregulated input voltage precede removal of the auxiliary supply voltage. Protection is required for the transient conditions only, hence a low-power regulator diode may be used.

(b) Comparison circuit: A differential amplifier comparison circuit, Q4,Q5, is used to reduce the disadvantages inherent in a single transistor configuration. Base-emitter voltage variations with temperature in one transistor of the differential amplifier tend to cancel similar variations in the other. Both the reference element, Z3,Z4, and the sampling divider, R9,R10,R11,R12, are subject to very small current changes, since each may be located in a base circuit as opposed to the single transistor configuration, where one must be located in the emitter circuit. Resistor R5 is added to the base circuit of Q4 to minimize output voltage change with variation in transistor collector-base reverse current, I_{co}, caused by temperature changes. A change in the I_{co} of Q5 causes the voltage division of the sampling divider to change. This would give a false indication of output voltage if the similar change in the I_{co} of Q4 flowing through R5 did not produce a change in Q4 base voltage which tends to offset the change in sampling divider output. The comparison circuit is discussed more completely in PSC 1, Section 2.7(b).

(c) Reference element: The stability of the reference element, Z3,Z4, and of the sampling divider resistors, R9, R10, R11, and R12, primarily determines regulator stability with time and with changes of environment. Two voltage reference diodes in series, each having a low temperature coefficient and a low dynamic impedance, are used for the reference element. Since the current drawn by these diodes is many times larger than the maximum base current of Q4, base current variations do not affect the reference voltage. Resistor R3 should be temperature stable to assure constant reference current; its initial tolerance is not so important as its subsequent stability against environmental changes.

The choice of reference voltage is determined primarily by the reference diodes available. Ideally, the magnitude of the reference voltage should be as near as possible to the magnitude of the regulated output voltage.[4] Regulator diodes with a breakdown voltage in the 80- to 100-volt range are available, but due to the nature of this device, their temperature coefficient and dynamic impedance are both larger than those of the lower-voltage, temperature-compensated reference diodes. The benefit derived from a large reference voltage is thus lost due to the reduced stability of this voltage. PSC 5 uses a temperature-compensated 8.4-volt reference diode, the 1N3157, whose low dynamic impedance and low temperature coefficient make it ideally suited for use as the reference element. Two of these diodes are connected in series to give a somewhat larger reference voltage while maintaining good stability. More than two in series, however, will cause the voltage rating of Q4 and Q5 to be exceeded.

(d) Sampling divider: The regulated output voltage is sensitive to any change in the sampling divider resistors, R9, R10, R11, and R12. The initial tolerance of these resistors is not so important as their subsequent stability against environmental changes. Resistors whose wattage ratings are very conservative should be used, and to insure that the ratio of the resistances remains relatively constant, the wattage ratings of R9, R11, and R12 should be in the same ratio as the actual power dissipation.

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[4] Before application to the comparison circuit, any change in regulated output voltage is reduced by a factor approximately equal to V_Z/E_O, where V_Z is the reference voltage. This reduction may also be expressed as a function of the sampling divider R9,R10, R11,R12, but the result is unnecessarily complicated by potentiometer R10.

The range of adjustment required in potentiometer R10 is determined primarily by the permissible operating voltage tolerance of the reference element, although some additional range is required to cover the initial tolerance of R9, R11, and R12. By using 1% tolerance resistors for the sampling divider resistors, the required adjustment range is minimized, assuring easy adjustment of the output voltage to 100 volts, and the prevention of gross misadjustment.

2.8 *Dynamic Design Considerations:* In an ideal voltage regulator, output voltage regulation for changes of input voltage or load current would be independent of the frequency of change. In a practical regulator, of course, this is not the case. Due to the frequency limitations of the transistors used in PSC 5, the negative feedback loop begins to lose control of the output voltage at frequencies above 5 kc. Reduction of output voltage variations at frequencies above 60 kc depends essentially upon output capacitor C3, while output voltage control at frequencies between 5 kc and 60 kc is a combined function of the negative feedback loop and the output capacitor.

Phase shift present in the high-gain negative feedback loop at frequencies above 5 kc might be sufficient to cause oscillation if it were not for R4 and C1, which reduce the amplification of the feedback loop over this range of frequencies, thus preventing oscillation. By themselves, however, R4 and C1 would also cause some loss of low frequency amplification and hence less ripple reduction. Capacitor C2 counteracts this loss by improving the sampling ratio of the comparison circuit [5] for ac variations. The combination of R4, C1 and C2 thus provides protection against the possibility of oscillation without sacrificing regulator performance.

These components would not be necessary if doubling the value of output capacitor C3 were feasible, since C3 could then decrease the signal fed to the differential amplifier at frequencies above 5 kc sufficiently to prevent oscillation. To achieve the large capacitance at the required voltage rating, however, would require the paralleling of at least eight smaller capacitance units. Economics and space factors negate this solution. The use of higher frequency transistors would permit the use of a smaller value for C3, but germanium transistors of this type do not have the necessary power ratings.

Output capacitor C3 must be a tantalum type for operation at low temperatures. The decrease of apparent capacitance caused by the increase of series resistance at low temperature is prohibitively large for any other electrolytic type.

2.9 *Mechanical Construction:* Certain precautions should be taken in the construction of PSC 5 to assure maximum performance. Mechanical construction will affect steady-state regulation for load variations, and could be a factor in determining transient regulation characteristics.

Care should be taken to keep contact and lead resistance to a minimum along the positive and negative output busses. Maximum steady-state regulation for load variations is achieved when physical contact between the sampling divider, R9,R10,R11,R12, and the output busses is made at the regulator output terminals. To achieve approximately the same regulation at the load, the lead resistance between output terminals and the load must be kept to a minimum.

Best transient regulation is achieved when output capacitor C3 is physically connected, along with the sampling divider, to the regulator output terminals and when the capacitor leads are kept as short as possible. This reduces lead inductance, which raises regulator output impedance at high frequency and causes a large voltage spike to accompany a step change in either input voltage or load current. To achieve best transient regulation at the load, lead inductance between regulator output terminals and the load must be kept to a minimum. Since this may be physically impossible, a second output capacitor placed directly across the load can be used to compensate for the lead inductance between regulator and load.

For minimum load transient recovery time, the lead resistance between load and output capacitor C3 should be a minimum. This reduces the charging and discharging time for C3.

[5] *Ibid.*

3. PERFORMANCE

PSC 5 is designed to furnish a supply voltage with percentage variation not exceeding 1% at output currents from zero to 400 ma and ambient temperatures from −55 to +65°C. Whether circuit operation is possible at these absolute maximum ratings for load current and ambient temperature depends upon the heat dissipating quality of the heat sink and the maximum input voltage for the particular application. The minimum input voltage is 100.7 volts, and the maximum input voltage must not exceed either 150 volts or the sum of Z1 breakdown voltage plus 100 volts. Ripple or transients which reduce the input voltage to a value lower than the specified minimum of 100.7 volts will reverse-bias the series control element causing spikes to appear in the output voltage. Ripple or transients which increase the input voltage to a value larger than the sum of Z1 breakdown voltage plus 100 volts will cause Z1 to conduct, shunting the series control element. Refer to Sections 2.5 and 2.6 for a more detailed discussion of voltage, current, and temperature limits.

3.1 *Stability and Steady-State Regulation:* Steady-state regulation (as contrasted to dynamic or transient regulation) is defined as the maximum variation of output voltage after all transients have subsided, when either the input voltage, load current, or auxiliary supply current is varied between specified maximum and minimum values. The regulation is expressed as a percentage of the nominal output voltage. Stability is defined as the constancy of output voltage with environmental change and time. The *total* steady-state regulation plus stability of PSC 5 is ±1%, i.e., the sum of the individual percentage variations in output voltage due to changes of input voltage, load current, auxiliary supply current, and ambient temperature will not exceed ±1% of the nominal output voltage over an 8-hour period.

Figure 5–3 shows typical variation in output voltage as a function of input voltage, load current, ambient temperature, and auxiliary supply current. Stability of the output voltage with time could not be included in the figure, but variations in the output voltage were were determined to be less than ±0.05% for an 8-hour period. The data in the figure are independent of the heat sink used, provided it can adequately dissipate the power involved. The measurements at high voltage and current were made instantaneously to avoid excessive collector dissipation and the consequent dependence of output voltage variation on the thermal resistance from transistor case to ambient air.

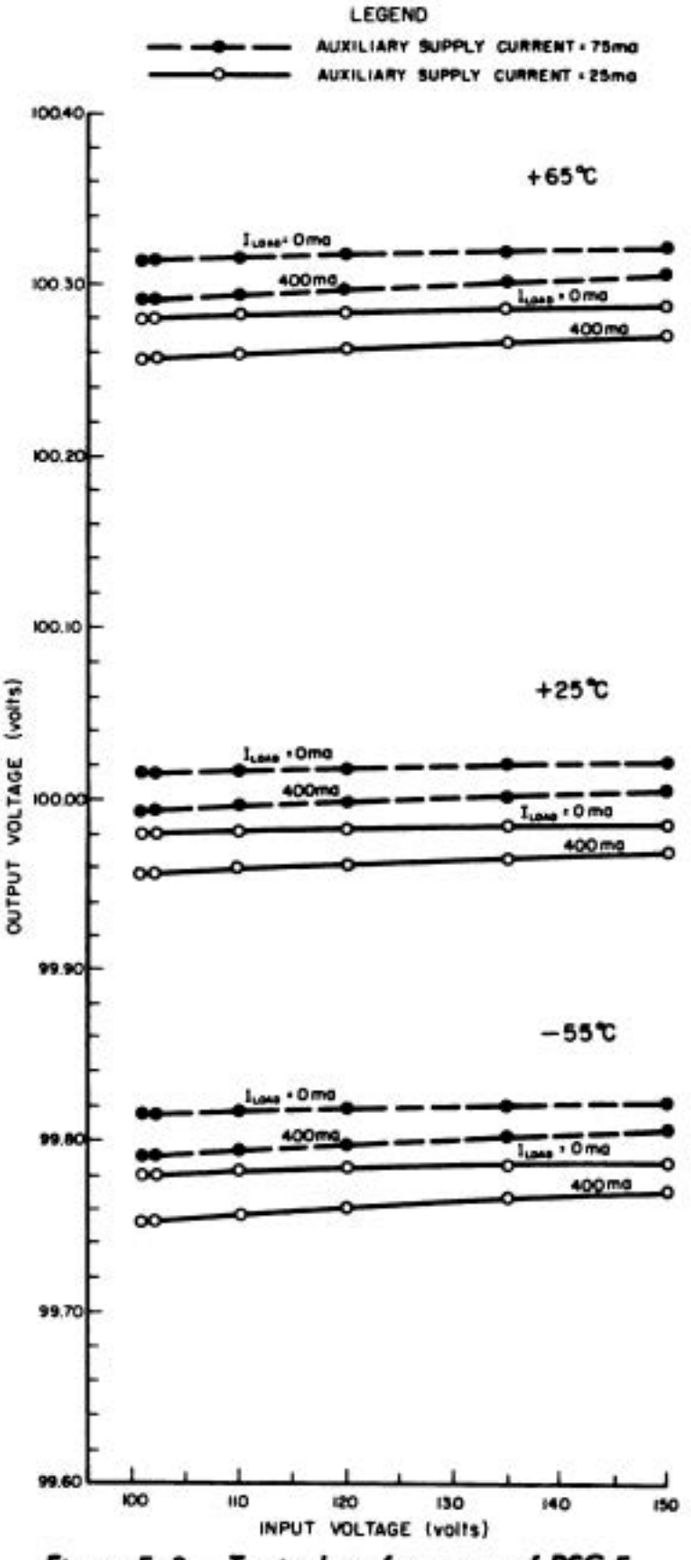


Figure 5–3.—Typical performance of PSC 5.

Total steady-state regulation plus stability for a particular regulator may differ from the value (approximately ±0.3%) shown in Figure

5-3 but the direction and general magnitude of output voltage variation with input voltage, load current, and auxiliary supply current will be similar to that shown. Output voltage variation with ambient temperature for a particular regulator is not as predictable, but it will not exceed the specified $\pm 0.01\%$ per degree centigrade. Figure 5-3 shows the temperature coefficient to be approximately equal to $+0.0075\%$ per degree centigrade between 25°C and 65°C, and approximately equal to $+0.0025\%$ per degree centigrade between 25°C and −55°C.

Since regulation for input voltage changes, i.e., the slope of the lines representing constant load current in Figure 5-3, is poorest at large load current, the $\pm 0.02\%$ regulation specified on page 5-3 is for maximum load current. Regulation for load current changes, i.e., the vertical distance between curves representing constant load current, is poorest for low input voltages, and the $\pm 0.1\%$ specified is for minimum input voltage. Regulation for axuiliary supply current variation (determined from Figure 5-3 by comparing the position of dotted and solid curves) is relatively independent of input voltage and load current. Current rather than voltage is used as the auxiliary supply variable, since both maximum and minimum limits are placed on the current drawn from the auxiliary supply, while the voltage may be any value larger than the minimum necessary to operate Z5.

The steady-state condition is achieved much more quickly after a change in either input voltage, load current, or auxiliary supply current than after a change in ambient temperature. Since each component part may have a different thermal time constant, the initial variation of output voltage with temperature may be larger than, or in a direction opposite to, the final steady, state value. The time required to reach temperature equilibrium depends primarily upon the rate of heat transfer for the particular application. At no time, however, will the output voltage variation with temperature exceed the $\pm 0.01\%$ per degree centigrade specified.

3.2 *Transient Regulation:* Transient regulation is defined as the difference between the maximum instantaneous variation of the output voltage in response to a positive or negative step change of input voltage or load current, and the steady-state voltage excursion which remains after all transients have subsided, expressed as a percentage of the nominal output voltage. This regulator characteristic, often unspecified, is of considerable importance if the regulator furnishes power to semiconductor circuits. Voltage transients exceeding the normal "regulation" can be fatal to semiconductors operated near their maximum voltage limit.

Transient regulation is specified as a function of ambient temperature, since the user may obtain better performance by limiting the minimum ambient temperature. Transient regulation is a function of output capacitor C3, which becomes less effective as the temperature decreases. As in the case of the corresponding steady-state regulation, transient regulation for input voltage changes is poorest at maximum load, and transient regulation for load current changes is poorest at minimum input. The values specified on page 5-3 are for these "worst" conditions. Optimum mechanical construction as specified in Section 2.9 is assumed, however.

Transient recovery time is defined as the interval from the application of a specified step change in either input voltage or load current to the time when the output voltage reaches and remains within the specified steady-state tolerance. The transient recovery time is less than 50 μsec after step changes of input voltage and less than 100 μsec after step changes of load current.

3.3 *Ripple Reduction:* The output ripple voltage must be specified in terms of the ripple voltage applied to PSC 5 both from the unregulated power source and from the auxiliary voltage supply. The ripple reduction figure specified for each indicates the amount by which the applied ripple voltage is reduced. Each depends somewhat upon the ripple frequency because of R4, C1, and C2, but the figures quoted are the minimum values for any frequency from 0 to 800 cps. Larger values of both types of ripple reduction may be achieved by increasing the value of C2.

Input ripple reduction is defined as the ratio of the ac ripple present in the input voltage to the resulting ac ripple present in the output

voltage at a specified ripple frequency. It is a function of the amplification in the negative feedback loop and of the small-signal forward voltage transfer ratio[6] of Q1, and is poorest at maximum load current and minimum input voltage. Maximum load current is accompanied by maximum control current to the base of Q3, which loads the differential amplifier and reduces the loop amplification. Minimum input voltage results in minimum voltage between the collector and emitter of Q1 and an accompanying low small-signal forward voltage transfer ratio. Input ripple reduction is 1,000 at a load of 400 ma and an input of 101 volts. This increases to 1,500 at 105 volts input and to 2,500 at 110 volts input.

Auxiliary supply ripple reduction is defined as the ratio of the ac ripple present in the auxiliary supply voltage to the resulting ac ripple appearing in the output voltage at a specified ripple frequency. It is a function of resistor R8, the current drawn from the auxiliary supply, and the voltage amplification provided by the differential amplifier. Since the first two are determined by the user, the auxiliary supply ripple reduction may be selected to fit the application (see Section 2.4 and Figure 5–1).

3.4 *Output Impedance:* Output impedance may be defined as the internal impedance, expressed in ohms, appearing at the output terminals of a power supply at any given frequency. A low value for this impedance is desirable in order to minimize feedback between circuits through the supply voltage source. Low output impedance also permits good output voltage regulation for changes in load current.

Figure 5–4 is an impedance vs. frequency curve for an ambient temperature of 25°C. Output impedance is shown for load currents of 50, 200, and 400 ma. Below a frequency of approximately 5 kc, impedance is a function of amplification in the negative feedback loop and the small-signal forward transconductance[7] of Q1. Within this range, output impedance increases as current decreases, because the forward conductance deteriorates considerably at low currents. At frequencies above 5 kc, the feedback loop begins to lose control and output capacitor C3 begins to take over. Above approximately 60 kc, the output impedance is essentially a function of the output capacitance and associated lead inductance. The hump in the impedance curve lies between the frequencies where the feedback loop begins to lose effectiveness and where output capacitor C3 takes over completely. The size of the hump, which indicates the tendency of the circuit to oscillate, has been reduced by the addition of resistor R4 and capacitor C1. The hump is more pronounced for large load currents because of increased phase shift in the feedback loop.

Curve A represents the output impedance when C3 is located a short distance away from regulator output terminals. The rise in impedance is due to a lead inductance of approximately 0.2 μh. Curve B represents the impedance when C3 is located directly across the output terminals.

At high temperature the curves are much the same as those shown in Figure 5–4. Impedance at frequencies below 20 kc may increase slightly due to decreased loop effectiveness, but high frequency impedance should remain unaffected. At low temperatures, however, the high frequency impedance may rise considerably due to the reduced effectiveness of output capacitor C3.

3.5 *Warm-Up Time:* Warm-up time is the interval between the application of input power and the instant at which the output voltage reaches and stays within its ±1% steady-state tolerance. It is primarily a function of the relative wattage ratings on voltage divider resistors R9, R11, and R12, and is less than 2 μsec if the wattages are correctly chosen. A maximum of 10 minutes may be required for the output voltage to remain within its ±0.05% stability vs. time rating, however. No output voltage transient accompanies the application of input power.

[6] Small-signal forward voltage transfer ratio is defined as the ratio of ac collector-emitter voltage to ac base-emitter voltage at constant collector current.

[7] Small-signal forward transconductance is defined as the ratio of ac collector current to ac base-emitter voltage at constant collector-emitter voltage.

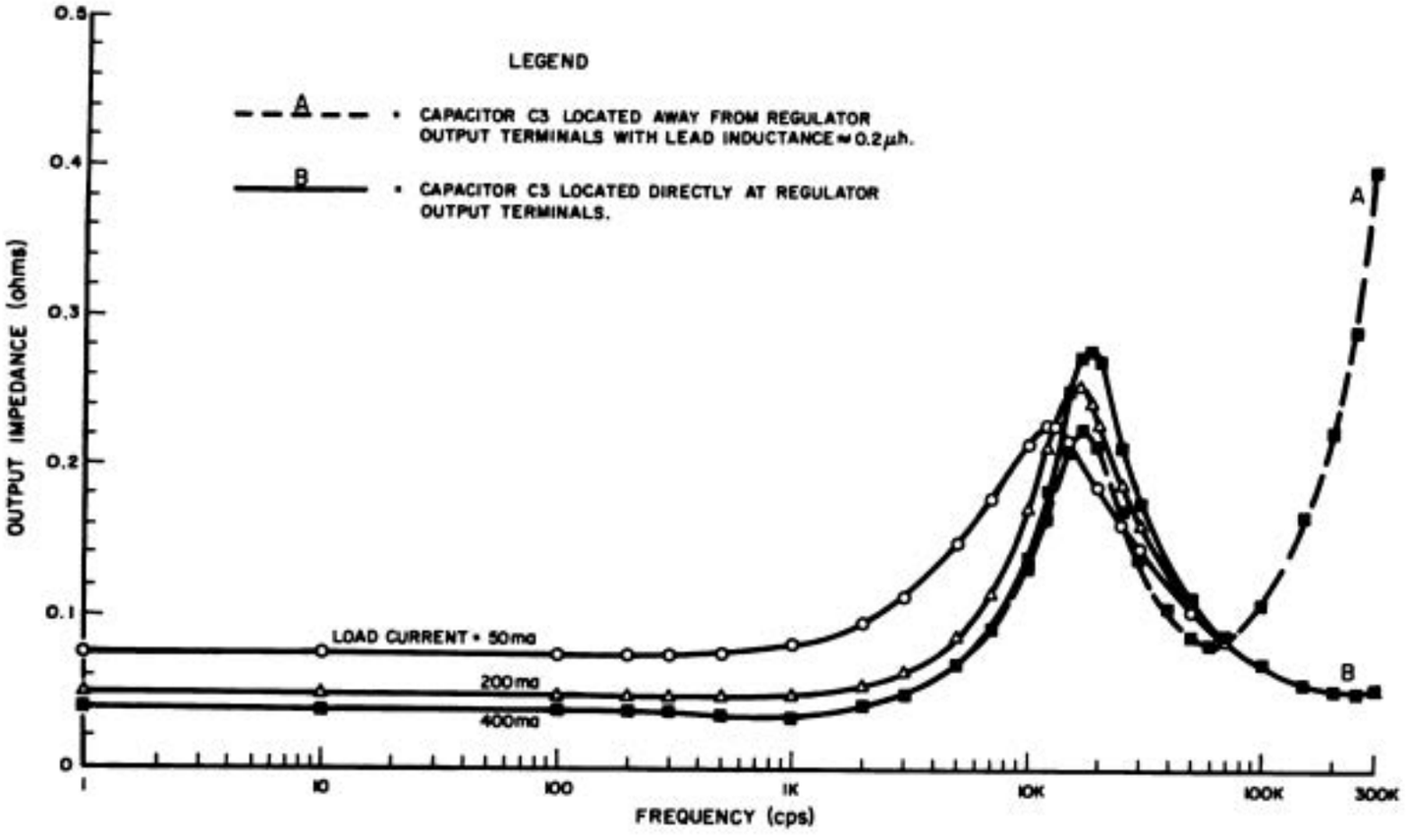


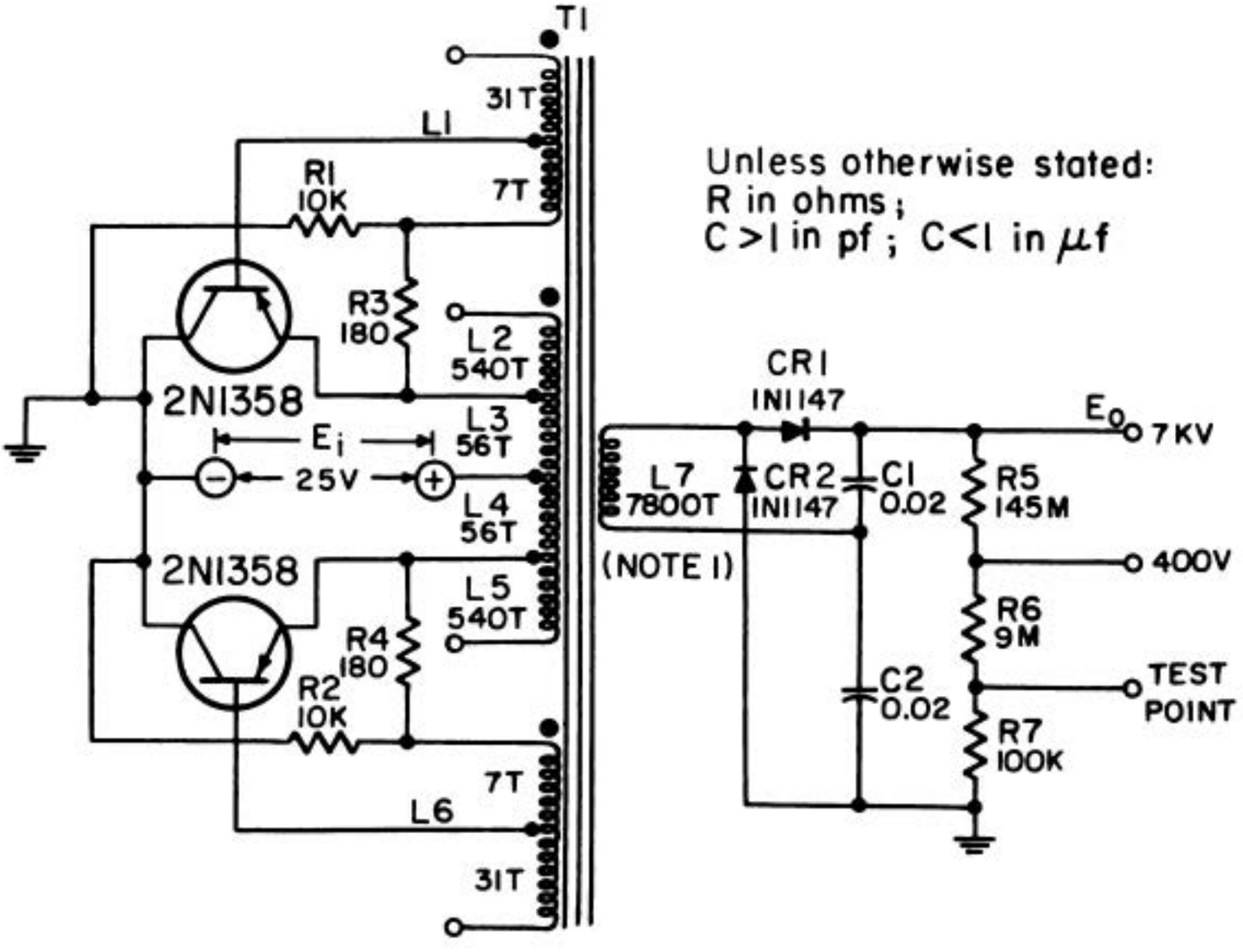
Figure 5-4.—Output impedance as a function of frequency and dc load.

Notes

PREFERRED CIRCUIT NO. PSC 6
7 KV CRT POWER SUPPLY

(Originally published as PC 202)

PREFERRED CIRCUIT NO. PSC 6
7 KV CRT POWER SUPPLY



Components:

T1: See Figure 6–1.

Maximum power dissipation (Note 2): R1, R2: 70 mw; R3, R4: 500 mw; R5: 350 mw; R6: 25 mw; R7; <1 mw.

Limits (these are not tolerances; see Note 2): All R: ±10%. All C: ±20%.

Operating characteristics:

Operating temperature: −55°C to +71°C.

Input voltage, E_i: 25 volts dc ±1%.

Output voltage, E_o: 7 kv dc.

Ripple (peak to peak): 16 volts at 100 μa (see Figure 6–4).
17 volts at 200 μa.

Operating frequency: ≈450 cps.

Power requirements:

Maximum input power: 220 ma at 25 volts for E_o=7 kv, I_o=200 μa.

NOTES:

1. Lead from inner end of secondary should be connected to the junction of C1 and C2 to limit the maximum voltage stress between the feedback and secondary windings to $E_o/2$.

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified above. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

PSC 6 7 KV CRT POWER SUPPLY

1. APPLICATION

PSC 6 has been designed to provide the high voltage source for the screen grid and final anode of 5- to 12-inch magnetic deflection cathode-ray tubes in equipment where full or partial transistorization exists. It will operate in the ambient temperature range of —55 to 71°C.

2. DESIGN CONSIDERATIONS

2.1 *Circuit Choice:* A full-wave dc-to-dc converter with the transistor load connected between voltage source and emitter was chosen because the collectors can be physically attached to a grounded or chassis-connected heat sink. Further, this circuit can be used with the same transformer-rectifier-filter package used in the equivalent electron tube circuits.

2.2 *Transistor Choice:* Type 2N1358 transistors are used because they are the units in MIL-STD-701 which most nearly meet the voltage, power, and saturation resistance requirements of the circuit.

2.3 *High-voltage transformer:* The transformer (Fig. 6-1) is so designed that it may be operated from a 300-volt supply when vacuum tube operation is desired (see Volume I, PC 6), or from a 25-volt supply when used with the transistor circuit. The input voltage for transistor operation was chosen as 25 volts to provide sufficient safety margin for the collector-emitter voltage of the transistor. The next higher standard regulated voltage is 50 volts,[1] which is too high to provide any safety margin even for transistors with a 100-volt peak inverse rating.

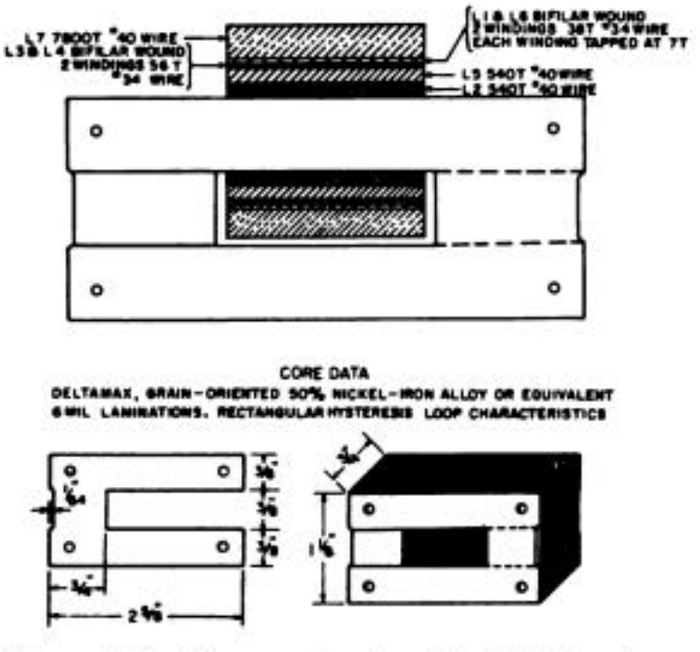


Figure 6-1.—Construction details of high voltage transformer.

No attempt has been made to optimize the size and weight of the transformer. The choice of number of turns and physical core size was a compromise between ease of construction, size, and weight on one hand, and power efficiency on the other. If advanced construction techniques make possible a better transformer design, the improved transformer may be substituted without requiring any circuit changes in PSC 6.

The core of the transformer is made of nickel-iron U laminations. This material has a square-loop hysteresis curve and a high permeability, which permits a minimum of primary turns for a given input voltage and flux density. The U lamination was chosen over the wound toroidal construction because of the ease with which the windings can be formed and insulation applied. The latter is especially important because of the insulation requirements of the high-voltage winding.

The two 540-turn primary windings, L2 and L5, are layer wound next to the transformer core. Next is the portion of the primary designed for use with transistors. Since the primary current is higher in the transistor circuit than it is in the vacuum tube circuit, larger wire is used in this section of the primary. The two halves of winding L3,L4 are bifilar wound. The two feedback windings, L1 and L6, are placed on the transformer next and are also bifilar wound. Since the bifilar windings are all relatively low voltage windings, the difference of potential between end turns does not create a serious insulation problem. The secondary, L7, constitutes the outside winding.

The bifilar windings are used to reduce the overshoot caused by leakage inductance. Because of the bifilar winding, the two primary

[1] MIL-STD-706A, Regulated DC Power Supply Voltages within Electronic Equipment.

sections used with transistors and the feedback windings are more closely coupled to each other than they would be if layer winding were used. When either transistor turns off, the energy stored in the leakage inductance is tightly coupled to the other transistor, which is conducting and rapidly dissipates the energy. In the absence of the close coupling, the energy stored in the leakage inductance would tend to dissipate in the off transistor, causing a much larger overshoot.

2.4 *Test point:* To allow measurement of the output voltage without special equipment, such as high-voltage probes, a tap is provided on the high-voltage bleeder for connecting a microammeter between the test point and ground. The resistance of the microammeter will be very small with respect to the 100,000-ohm portion of the bleeder resistor; therefore, such connection is physically equivalent to inserting the microammeter in series with the 154 megohm bleeder. Since the 154 megohm bleeder will not be made up of precision resistors, the case containing transformer, rectifier, filter, and bleeder must have the current in microamperes corresponding to 7 kv printed on it. This calibration would take place in final test, and therefor the inscription on the case does not unduly complicate unit production.

2.5 *Screen Grid Voltage:* A second tap on the high-voltage bleeder provides 400 volts for the screen grid of the cathode-ray tube.

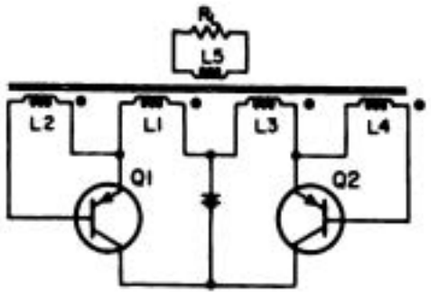


Figure 6–2.—Simplified circuit diagram of PSC 6.

2.6 *Theory of Operation:* If a perfect voltage source were connected in series with a perfect inductor and a switch, then with the switch closed the voltage across the inductor would remain constant with time and would be equal to the potential of the voltage source. The current through the inductor would rise linearly with time at such a rate that the change of flux linkages as a function of time would be equal to the source voltage.

In a physical circuit, the voltage source has resistance; the switch can be approximated by a transistor which is biased on, and which has a nonlinear resistance. Further, the inductor, if air core, has resistance; if iron core, it has resistance plus nonlinear inductance. Under these conditions, the voltage across the inductor will no longer be constant, and the rate of change of current with time will be nonlinear. This nonlinearity can be accentuated by using a square-loop core which saturates sharply, and by inductively coupling the main source of transistor forward bias from this inductor. The inductor has now become a transformer. The addition of a second transistor and a duplicate pair of windings makes a full-wave device. By adding a fifth winding, means are provided for isolating a load from the input in addition to effecting an impedance transformation.

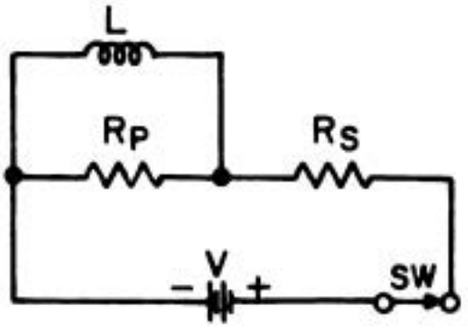


Figure 6–3.—Circuit equivalent to PSC 6 when one transistor is on and the other off.

In a circuit such as the one described (see Fig. 6–2), when the voltage source is initially switched on, one of the two transistors will conduct more heavily than the other. This unbalanced current flow is caused by dissimilarities in the two halves of the circuit. The base windings L2 and L4 are so connected that the unbalance once having started, will regeneratively increase until one transistor is biased on and the other biased off. Under these conditions, the approximate equivalent circuit of Figure 6–3 may be used, since L3, L4, and Q2 are effectively out of the circuit. Here a parallel resistor, R_p, is connected across a perfect inductor, L. In series with this combination are a voltage source, V, and a resistor, R_s. R_p represents the sum of the transformer losses and load power, while R_s represents the

sum of the source and switch (transistor) losses. If an imperfect inductor, an imperfect voltage source, and an imperfect switch are used, closing the switch will cause an initial rise in current. This will be followed by an approximately linear current rise, varying at a rate that keeps $L(di/dt)$ equal to V minus IR_s. Since IR_s increases with I, the magnitude of di/dt will decrease with time if L remains constant. When the integral of the instantaneous induced emf, e, times the differential time, dt,[2] reaches the saturation flux density of the core, the inductance of the coil drops sharply. This allows a rapid current rise in the coil. The coefficient of coupling of L1 and L2 (see Fig. 6–2) is drastically reduced by the saturation of the transformer core, with the result that the base-emitter drive of the transistor is reduced. The circuit will no longer be capable of maintaining an increasing di/dt, because the transistor will be called on to pass a rapidly increasing current when its base drive has decreased sharply; therefore di/dt will begin to decrease. The resultant emf will be in such a direction as to back bias the base of the transistor which was on, and forward bias the base of the transistor which was off. The reversal of direction of $d\phi/dt$ due to the decreasing di/dt will proceed regeneratively and switch the transistor which was initially biased on, to a biased off state. It will simultaneously switch the transistor which was biased off to a biased on state. The process will now repeat itself.

2.7 *Operation With One Transistor Inoperative:* A short circuit between transistor junctions will overload PSC 6 and stop oscillation. If one transistor fails because of an open circuit in one of the junctions, however, PSC 6 will continue to operate but at a reduced output voltage. This type of failure in one transistor during a mission will cause increased indicator tube deflection, but the change will be small and may not be noticed by the operator. Further, because the transistors are not designed for quick interchange, replacement during a mission is unlikely. However, because the transistors operate far below maximum dissipation ratings, operation with a single transistor should suffice until the next maintenance check.

2.8 *Regulation:* In general, the regulation of the supply (Fig. 6–4) will be sufficeint for most uses with no additional circuitry required. For reduction of output ripple and output impedance, additional capacitance may be added across the cathode-ray tube input. The output voltage stability can be improved by the use of a regulator in the collector circuit of the transistors, but such a regulator becomes rather complex if stability better than that provided by PSC 6 is desired.

3. MEASURED PERFORMANCE

High-voltage power supplies of the dc-to-dc converter type have a bleeder resistor connected across the output as an integral part of the circuit. This resistor is usually encapsulated, along with the output filter capacitors and associated parts. With this in mind all load current measurements below are exclusive of the bleeder current.

3.1 *Output Characteristics as a Function of Load Current:* Magnetic deflection cathode-ray tube final-anode currents, in general, average less than 100 μa. The curves (Figs. 6–4, 6–5) are plotted considerably beyond this point to demonstrate operating characteristics at extended current ranges.

The relationship between output voltage and current is shown in Figure 6–4. The change in output voltage for a change in load current of 100 μa is less than 2%.

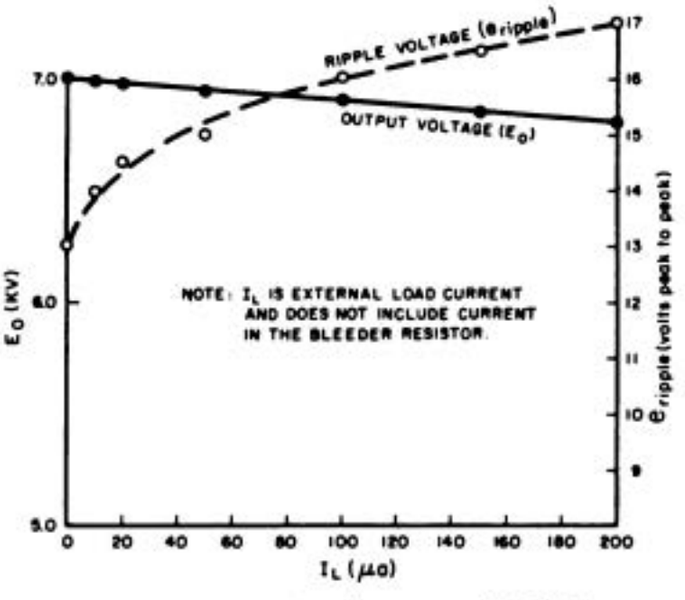


Figure 6–4.—Normal output of PSC 6.

[2] $\int edt$ is the best measure of the total flux linkages in the core at any instant, since the nonlinearity of the core does not enter the equation as it does when ampere turns are used.

When one transistor is disconnected, the frequency of the oscillation increases by a factor of approximately three, and the variation of output voltage as a function of load current is increased. Under these conditions, the average variation is approximately 9% for a variation of load current of 100 μa. The output voltage plotted in Figure 6-5 was measured by setting the output voltage with both transistors operating to 7 kv for no-load conditions and then disconnecting one transistor. Under the no-load condition, there was a change in output of less than 50 volts in 7 kv.

3.2 *Effect of Variations of Transistor Parameters:* The parameters of most interest are the on-resistance of the transistor and the input impedance, h_{IE}, in the grounded emitter configuration. The 2N1358 has an input impedance which is small compared to the 180-ohm resistor in series with the base; therefore, variations in value of two to one in h_{IE} have negligible effect on the operation of the transistor. The voltage across the collector-emitter terminals, with an input voltage of 3 volts to the transistor, varies from 60 to 90 mv for a collector current of 200 ma. This is the typical operating condition of the transistor when in the on condition, and this voltage drop is small (less than 0.1 volt) compared to the drops in the other portions of the collector-emitter loop. Under these conditions, variations of two to one in this drop will effect the output voltage by less than 50 volts in 7 kv.

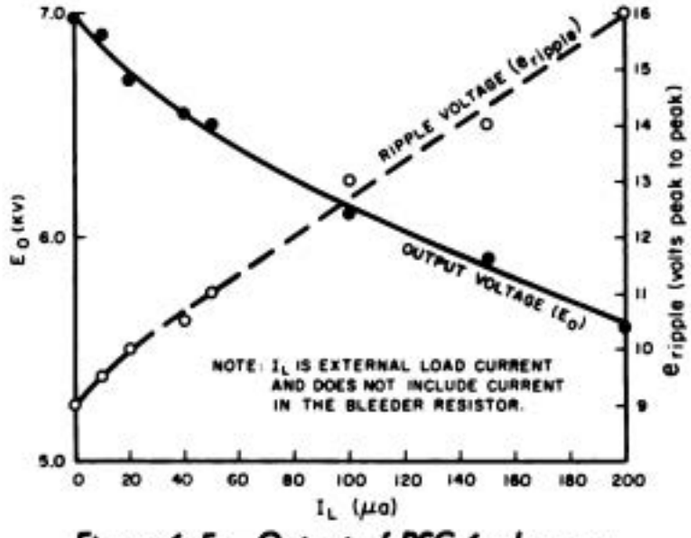
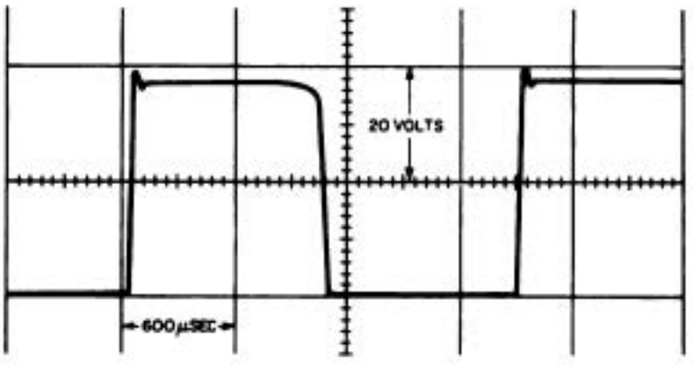
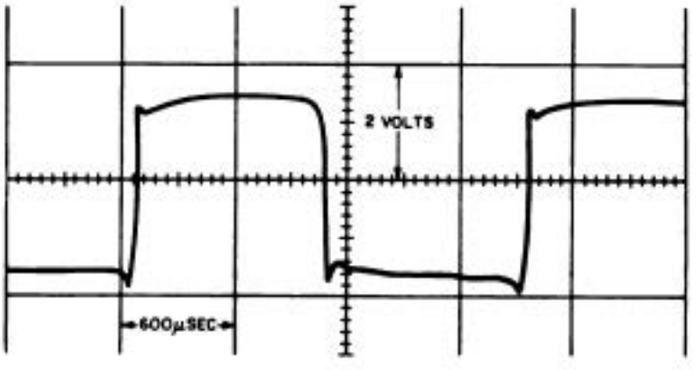


Figure 6-5.—Output of PSC 6 when one transistor is open.



(a) EMITTER-COLLECTOR VOLTAGE

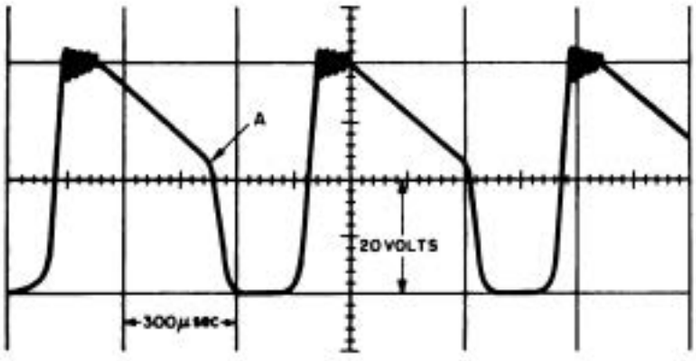


(b) BASE-EMITTER VOLTAGE

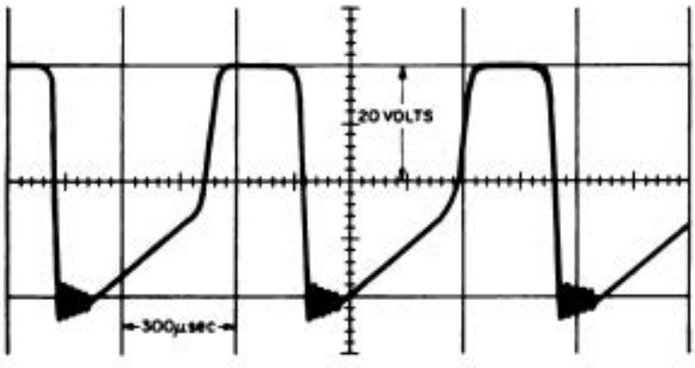
Figure 6-6.—Waveforms for load current of 35μa, normal operation.

3.3 *Pertinent waveforms:* Oscillographic displays of typical waveforms are shown in Figure 6-6. Figure 6-6(a) shows the normal emitter-collector waveform. It can be seen that the overshoot is less than 2 volts in magnitude. This small overshoot, which is achieved by the bifilar winding of both primary and feedback coils, provides an adequate safety factor, since the transistor used has a peak rating of 80 volts with the base biased off. The base-emitter waveform is shown in (b).

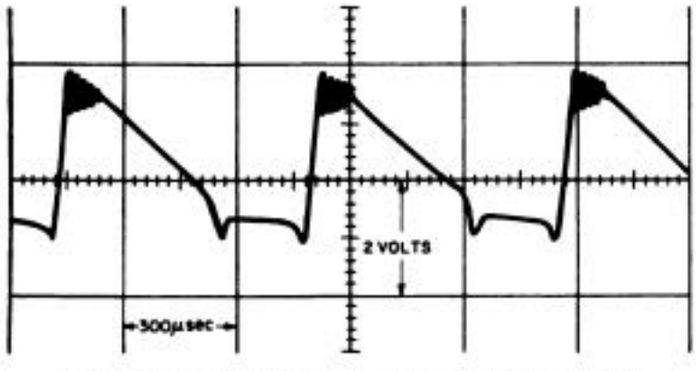
The waveforms shown in Figure 6-7 were observed after removal of one transistor and show operating conditions with one transistor disabled. The circuit under these conditions is shown in Figure 6-8. The emitter, base, and collector of the operating transistor are labeled E, B, and C, respectively, while the



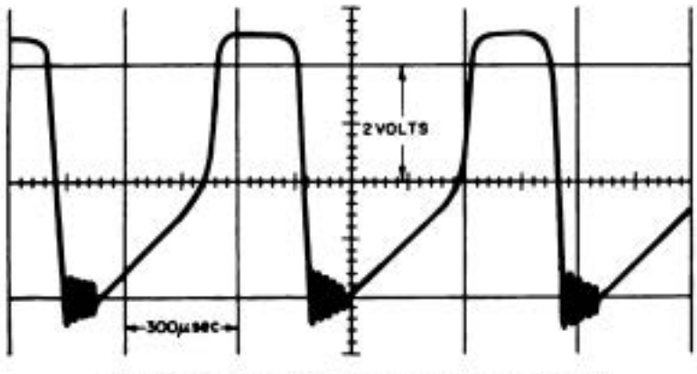
(a) EMITTER-COLLECTOR VOLTAGE (points E and C, Fig. 6-8)



(b) VOLTAGE BETWEEN POINTS E' and C', Fig. 6-8



(c) BASE-EMITTER VOLTAGE (points E and B, Fig. 6-8)



(d) VOLTAGE BETWEEN POINTS E' and B', Fig. 6-8

Figure 6-7.—Waveforms when one transistor is removed from the circuit.

terminals to which the removed transistor had been connected are labeled with primes. The top waveform, (a), which shows the variation of voltage across the emitter-collector of the transistor remaining in the circuit, can best be understood by starting at point A on the curve. At this point, the voltage from emitter to collector is approximately equal to the supply voltage. Because the base is forward-biased by the voltage divider, R1,R3, current begins to flow in the collector-emitter circuit and the transistor turns rapidly on, as it did when there were two transistors in the circuit. However, with only one transistor operating, the core is not starting from negative saturation, but from a point near zero flux density, and the flat portion of the curve is much shorter than for normal operation with two transistors. When the core saturates and the rate of change of flux reverses, the base-emitter voltage reverses and biases the single operating transistor from "on" to "off". The energy stored in the transformer now dissipates via the coupled secondary load and allows the back emf across the transistor to drop toward the supply potential, as shown by the diagonal portion of the waveform. At this point there is insufficient reverse bias to overcome the forward bias supplied by the voltage divider, R1,R3, and the cycle repeats. In Figure 6-7 (c), the base-voltage clipping due to the flow of base current is obvious when compared to the open circuit measurements of (d).

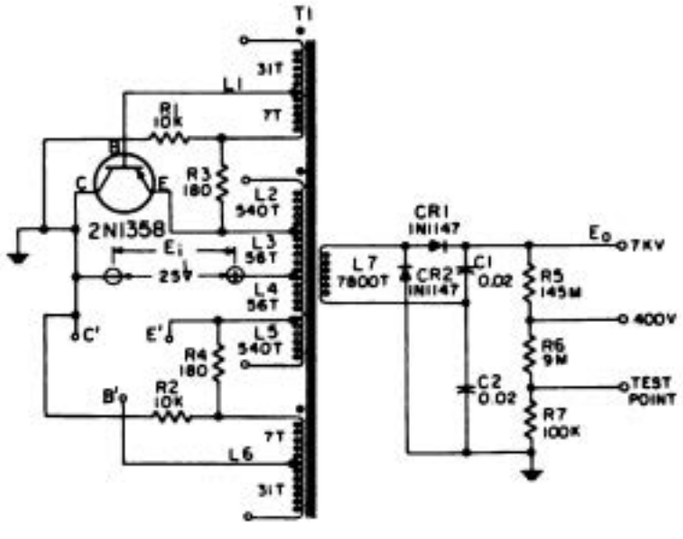


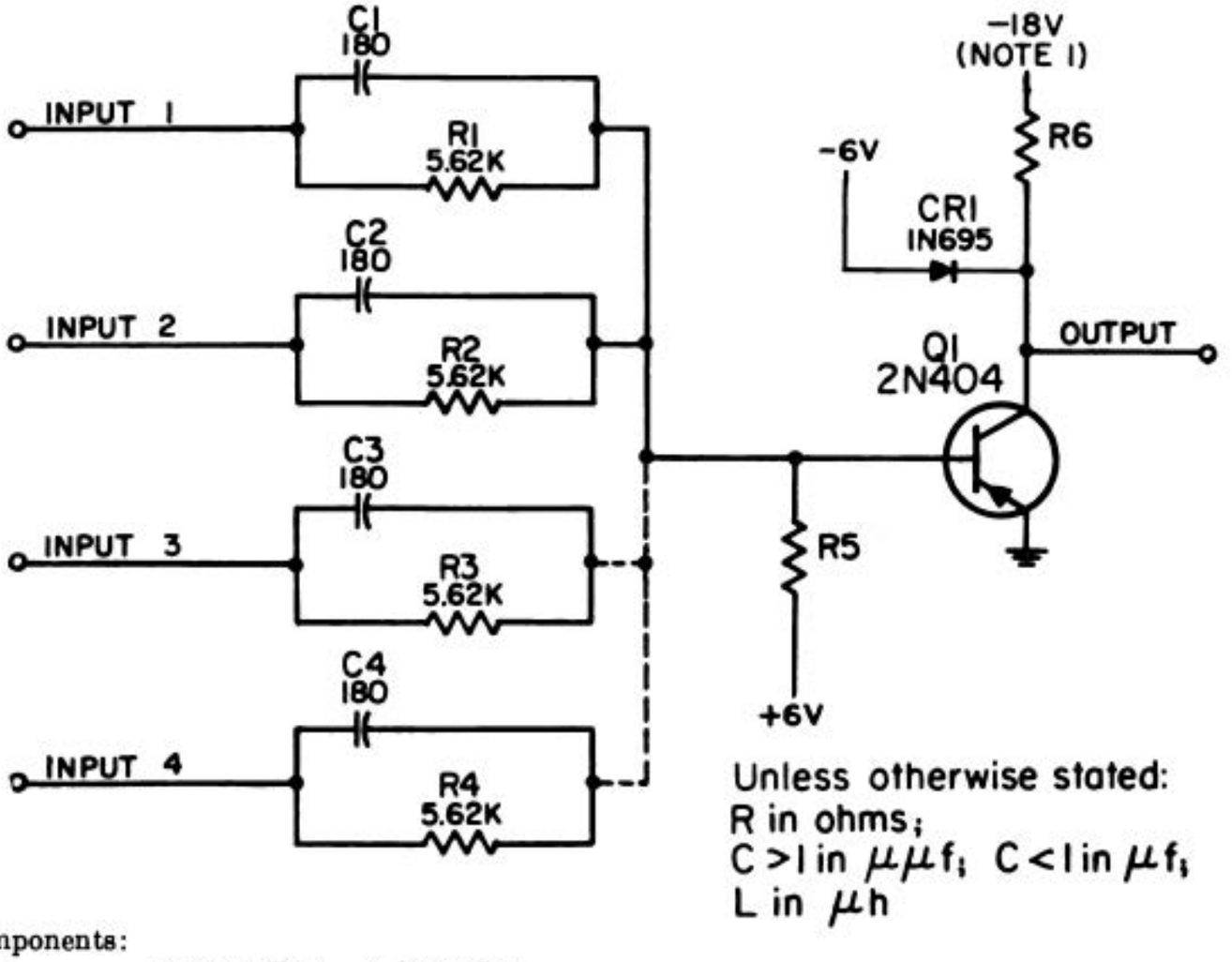
Figure 6-8.—PSC 6 with one transistor removed.

Notes

PREFERRED CIRCUIT NO. PSC 7
2 AND 4 INPUT GENERAL PURPOSE NOR GATE

(Originally published as PC 210)

PREFERRED CIRCUIT NO. PSC 7
2 AND 4 INPUT GENERAL PURPOSE NOR GATE



Components:

	2 Input Gate	*4 Input Gate*
R5:	26.1KΩ	21.5KΩ
R6:	2.15KΩ	2.61KΩ

Maximum power dissipation (Note 2): R1, R2, R3, R4, R5: 8 mw; R6: 200 mw.
Limits (these are not tolerances; see Note 3): All R: ±5%. All C: ±10%.

Operating characteristics:

Temperature range: −30°C to +60°C.
Input impedance: One "G" load (see Section 2.3).
Input signal characteristics:
Level (Note 4):
Logical "1": −6.2 volts ±10% at 1.2 ma maximum.
Logical "0": −0.15 volts.
Pulse (Note 5):
Polarity: Positive or negative.
Amplitude: 6 volts ±10%.
Width at 50% amplitude: 0.8 μsec minimum; 5 μsec maximum.
Rise time (Note 5): ≤0.2 μsec.

(Specifications continued on next page)

Operating characteristics—*Continued*

Switching characteristics (Note 7):

Input signal	Output signal
Level change from 0 v to −6 v with rise time of 1.4 μsec.	Level change from −6 to 0 v. Turn-on time (Note 8): 1.6 μsec max. Delay time: 0.9 μsec max. Rise time: 0.7 μsec max.
Level change from −6 v to 0 v with rise time of 0.5 μsec.	Level change from 0 v to −6 v. Turn-off time (Note 9): 1.3 μsec max. Storage time: 0.4 μsec max. Rise time: 0.9 μsec max.
Negative-going pulse with rise time of 0.2 μsec.	Positive-going pulse. Turn-on time: 0.35 μsec max. Delay time: 0.15 μsec max. Rise time: 0.2 μsec max.
Positive-going pulse with rise time of 0.2 μsec.	Negative-going pulse. Turn-off time: 0.35 μsec max. Storage time: 0.15 μsec max. Rise time: 0.2 μsec max.

Maximum load: (see Section 2.3).

Circuit	Type of output			
	Direct current	Level	Positive pulse	Negative pulse
2 input gate	4 ma at −6.2 v ±10%.	Maximum of 4 loads, no more than 2 of which are F loads.	4 loads F or G	One G load only.
4 input gate	3.5 ma at −6.2 v ±10%.	Maximum of 3 loads, no more than 2 of which are F loads.	3 loads F or G	One G load only.

Power requirements:

Voltages	Current	
	2 Input gate	4 Input gate
−18 v ±10%	9.5 ma	8 ma
−6 v ±10%	9.5 ma	8 ma
+6 v ±10%	0.27 ma	0.33 ma

(For notes, see bottom of next page)

PSC 7 2 AND 4 INPUT GENERAL PURPOSE NOR GATE

1. APPLICATION

PSC 7 performs the general purpose AND, OR, and inversion functions in a compatible set of digital logic circuits [1] for use in computer, control, and communication equipment operating within the temperature limits of −30 and +60°C. It can be used as (1) an AND gate for positive levels, or positive-going pulses; (2) an OR gate for negative levels, or negative-going pulses; and (3) an inverter for positive- or negative-going pulses or levels. It cannot be used as an AND gate for pulses when a spurious output pulse can cause errors; under these conditions, PSC 8, the pulse gate, must be used (see Sec. 2.2).

2. DESIGN CONSIDERATIONS

From the logistic and maintenance standpoints, it is impractical to design a different NOR gate [2] for every possible number of inputs. The usual solution is to select a multiple input gate as the standard building block. If more inputs are required, they can be formed by combination of the standard building blocks. If fewer inputs are required, the unused terminals are grounded. PSC 7 is designed for two- and four-input circuits, since this system offers maximum flexibility for gate operation. When PSC 7 is used as an inverter, the two-input circuit is used with one input grounded. Thus one circuit is capable of performing three of the five basic computer functions.

[1] See also Preferred Semiconductor Circuits PSC 8 through PSC 13.

[2] An AND gate is a circuit having an output and a multiplicity of inputs so designed that the output is energized when and only when every input is in a prescribed state. An OR gate is one whose output is energized when any one or more of the inputs is in its prescribed state. See IRE Standards on Electronic Computers, Proc. IRE, Vol. 44, No. 9, September, 1956, pp. 1166–1173. A NOR gate is a circuit which is capable of operating either as an AND gate or as an OR gate.

NOTES:

1. The −18-volt supply is obtained by connecting a −12-volt source in series with the −6-volt supply (Section 2.4).

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus the drifts caused by environmental changes or aging.

4. The minimum duration of a level is 5 μsec.

5. Positive pulses are referenced to −6.2 volts ±10%. Negative pulses are referenced to ground (actually about −0.15 volt).

6. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude.

7. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature. The load in each case was maximum for that type of operation.

8. The turn-on time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change, and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

9. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

2.1 *Circuit Configuration:* A single-transistor common-emitter amplifier operating as a NOR gate was chosen for the general purpose gate function. When the circuit is used as an AND gate, the transistor is normally on and cannot be turned off unless all the inputs are simultaneously at their most positive voltage (zero volts). When the circuit is operating as an OR gate, the transistor is normally off and can be turned on by any of the inputs which change from zero to a −6-volt level. If more than one of the inputs is driven negative, the transistor is driven deeper into saturation, but the output signal is unaffected. PSC 7 can be used as an inverter by using the 2-input gate and grounding the unused input.

The output is clamped to −6 volts in the OFF state by diode CR1 and to ground in the ON state by the saturated transistor. The positive 6-volt bias supply, together with the resistor R5, provides a current bias which prevents I_{CBO} flow in the base region during cut-off condition, and therefore prevents I_{CBO} multiplication. The clamped operation using CR1 standardizes the magnitude of the output pulses and levels.

Clamped operation also increases the speed of the ON to OFF transition in two ways. First, limiting the maximum magnitude of the input signal by clamped driving-circuits limits the number of the minority carriers stored in the base of the driven circuit. This in turn allows the minority carriers to be cleared out of the base more rapidly in the ON to OFF transition, and therefore decreases storage time.[3] Second, the rise time of the output voltage is decreased because the voltage change is limited by the clamp to the initial portion of an exponential waveform.

The change from a 2-input to a 4-input gate is accomplished by changing the resistance of R5 and R6 and adding two RC input circuits. When PSC 7 is used as an inverter for positive-going signals, the AND gate output-loading restrictions apply. When it is used as an inverter for negative-going signals, the OR gate output-loading restrictions apply.

2.2 *AND Circuit Operation:* During AND gate operation a spurious pulse can appear at the output.[4] Assume all inputs to the gate are initially at −6 volts and then one input is driven positive. A positive transient will feed through the input capacitor and drive minority carriers out of the base region. In transistors with low minority-carrier storage characteristics, this depletion of minority carriers will cause the transistor to turn off temporarily, and a spurious output pulse will result. The magnitude and duration of this unwanted output pulse could be reduced if the input capacitor were reduced in magnitude to limit minority carrier removal during the transient. Use of a smaller capacitor, however, would prevent a pulse from turning the transistor on under worst operating conditions when the circuit was being used as an OR gate or as an inverter for negative-going pulses.

The spurious output pulses cause no difficulty when the output of the AND gate is eventually directed to the resistive input of a bistable multivibrator, such as PSC 9. The resistive inputs are integrating networks with a time constant sufficient to prevent the maximum amplitude and duration of the spurious pulses from causing an unwanted signal. If the AND function must be performed on a mixture of levels and pulses and the gate output must drive a load other than the resistor inputs *a*, *c*, *e*, or *g* of PSC 9, the pulse gate, PSC 8, must be used.

2.3 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PSC 7 through PSC 13, are abitrarily given in terms of "F" and "G" loads. The "G" (gate) load is equivalent to the input impedance of PSC 7; the "F" (flip-flop) load is derived from the input impedance of the bistable miltivibrator, PSC 9.

The equivalent circuit of each of these loads is shown in Figure 7–1. The actual load impedance may vary somewhat from the equivalent circuit describing it; however, allowances were made for this in formulating the loading

[3] For a definition of storage time, see Note 9, p. 7–4.

[4] A. I. Pressman, *Design of Transistorized Circuits for Digital Computers*, John F. Rider, Inc., N.Y., 1959, pp. 210–212.

rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

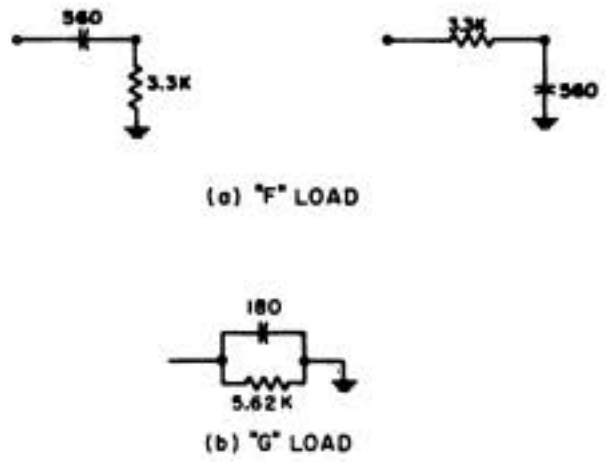


Figure 7–1.—Equivalent circuits of loads and input impedances.

2.4 *Power Supplies:* The −18-volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6-volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6-volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18-volt supply flowing in the reverse direction through the −6-volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6-volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PSC 9. When PSC 7 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels.

Insertion of a 50 μf capacitor between the −6-volt supply and ground at the power distribution point for each group of circuits will serve to keep the transient level within reasonable limits. In addition, 0.4 μf extended-foil polystyrene capacitors should be spotted along the power distribution lines to filter out high frequency transients. The filtering requirements should be determined by checking the distribution points of the power supply leads with an oscilloscope capable of responding to signals in the 10 mc range.

In computer and data processing equipment, hundreds of transistors may be installed in a single equipment bay. The current can exceed 20 amperes in the steady state, and variational currents of several amperes can flow at a given time. This large variational current gives rise to a difference of potential along the ground bus which may be of sufficient amplitude to cause an equipment error. General precautions to observe in laying out grounds are:

1. Use flat strip conductors to decrease lead inductance.
2. Use a fanning out of ground distribution; i.e., where possible, run each circuit or circuit group common ground directly to the ground bus.
3. Run these intermediate ground busses to a main ground bus with an increased size comparable to the number of intermediate busses joining it.
4. To check the adequacy of the ground system, use a high frequency oscilloscope with its ground connected to the central ground point or to a point on the main ground bus, and run the oscilloscope probe along the main and intermediate ground busses. The magnitude of the voltage transients along the bus caused by variational currents flowing in the bus will serve as an indication of the effectiveness of the ground system.

3. PERFORMANCE

Input and output waveforms for typical operation of the general purpose NOR gate, PSC 7, are shown in Figures 7–2 and 7–3. All traces were obtained at a sweep speed of 0.2 μsec per division. Only the two-input gate operation is illustrated, since the waveforms for the four-input version do not differ significantly from those shown.

Figure 7–2 shows the output when the input is a positive pulse. Since the input waveform is not significantly affected by output loading, only one input trace is illustrated. Maximum output loading is determined by the deterioration permissible in the rise time of the output waveform. The rise time, in turn, is

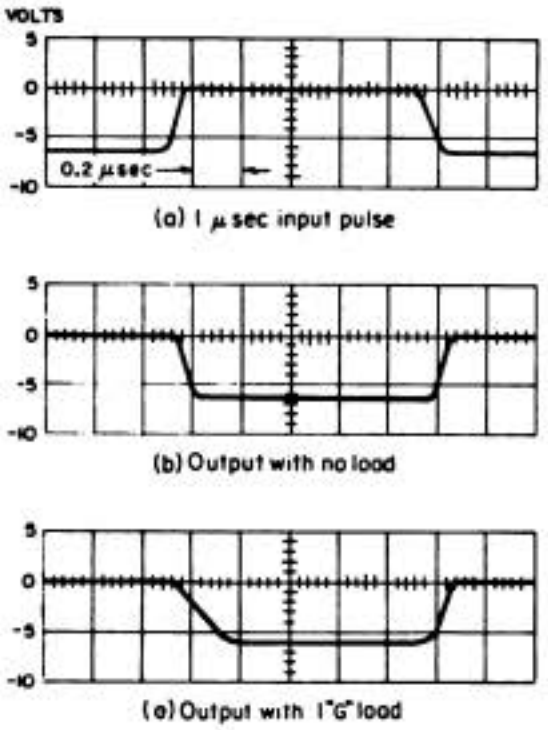


Figure 7-2.—Typical waveforms for 2 input gate with positive input signal.

determined by the time constant of the circuit consisting of the load in parallel with the transistor collector resistor, since the transistor is off during this transition. Comparison of waveforms (b) and (c) shows that the output waveform rise time deteriorates rapidly, although with 1 "G" load, it is within the specified 0.2 μsec maximum.

For a negative input pulse (Figure 7-3), the leading edge of the output waveform is generated by the discharge of the load capacitor through the transistor. The rise times are faster than they are with positive inputs, since the resistance in parallel with the load now includes the saturation resistance of the transistor, but they are more dependent on transistor characteristics, such as the saturation resistance, beta, and delay time. As indicated in (d), the rise time with 4 "G" loads is still within the 0.2 μsec maximum. The trailing edge of the output waveforms illustrates the increase in turn-off time as the load on the circuit is increased.

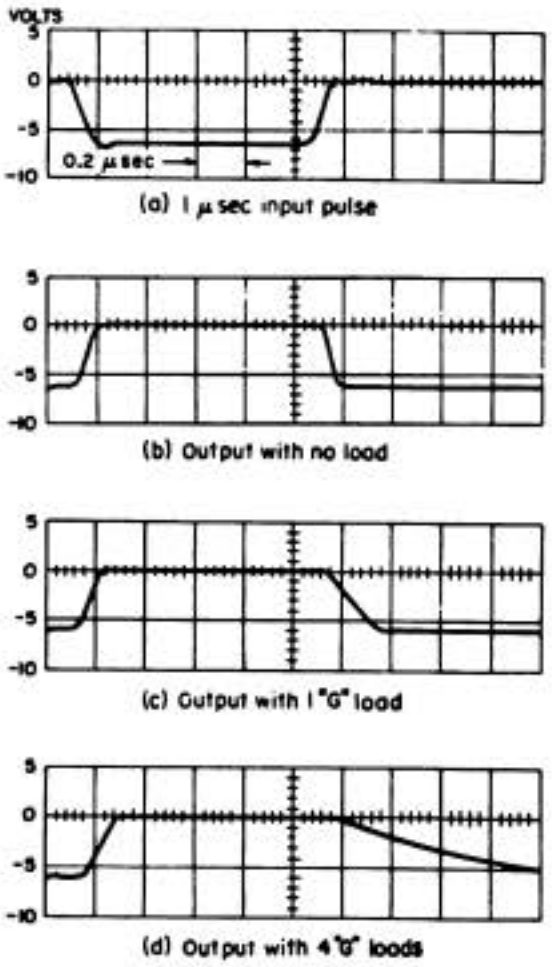


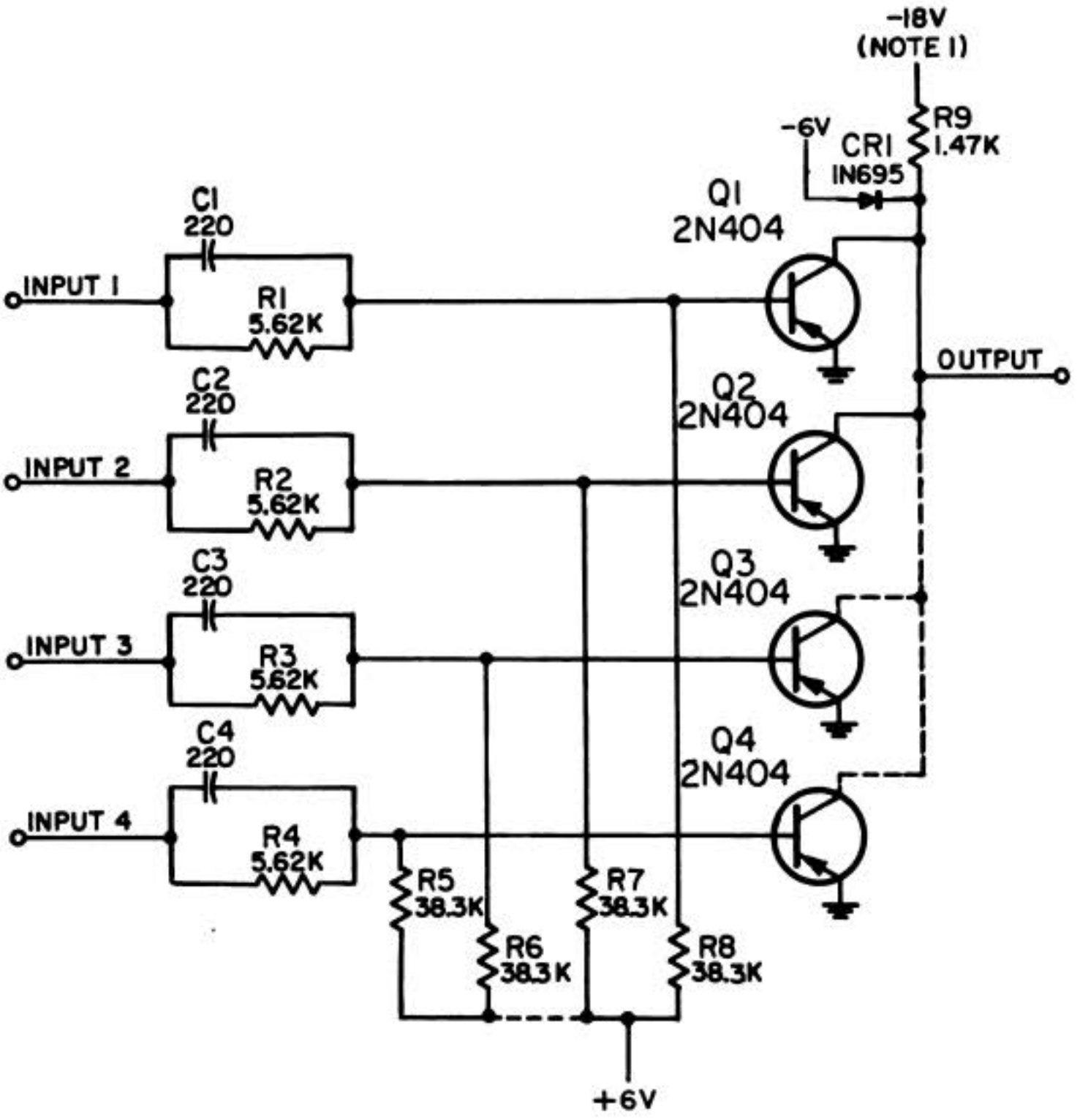
Figure 7-3.—Typical waveforms for 2 input gate with negative input signal.

Notes

PREFERRED CIRCUIT NO. PSC 8
2 AND 4 INPUT PULSE NOR GATE

(Originally published as PC 211)

PREFERRED CIRCUIT NO. PSC 8
2 AND 4 INPUT PULSE NOR GATE



Unless otherwise stated, R in ohms; C>1 in $\mu\mu$f; C<1 in μf; L in μh

Components:

Maximum power dissipation (Note 2): R1, R2, R3, R4: 8 mw; R5, R6, R7, R8: 2 mw; R9: 300 mw.

Limits (these are not tolerances; see Note 3): All R: $\pm 5\%$. All C: $\pm 10\%$.

(Specifications continued on next page)

Operating characteristics:

Temperature range: −30°C to +60°C.

Input impedance: One "G" load (see Section 2.1).

Input signal characteristics:

Level (Note 4):

Logical "1": −6.2 volts ±10% at 1.2 ma maximum.

Logical "0": −0.15 volts.

Pulse (Note 5).

Polarity: Positive or negative.

Amplitude: 6 volts ±10%.

Width at 50% amplitude: 0.8 μsec minimum; 5 μsec maximum.

Rise time (Note 6): ≤0.2 μsec.

Switching characteristics (Note 7):

Input signal	Output signal
Level change from 0 v to −6 v with rise time of 1.4 μsec.	Level change from −6 v to 0 v. Turn-on time (Note 8): 1.6 μsec max. Delay time: 0.9 μsec max. Rise time: 0.7 μsec max.
Level change from −6 v to 0 v with rise time of 0.5 μsec.	Level change from 0 v to −6 v. Turn-off time (Note 9): 1.2 μsec max. Storage time: 0.4 μsec max. Rise time: 0.8 μsec max.
Negative-going pulse with rise time of 0.2 μsec.	Positive-going pulse. Turn-on time: 0.35 μsec max. Delay time: 0.15 μsec max. Rise time: 0.2 μsec max.
Positive-going pulse with rise time of 0.2 μsec.	Negative-going pulse. Turn-off time: 0.33 μsec max. Storage time: 0.15 μsec max. Rise time: 0.18 μsec max.

Maximum load (see Section 2.1):

Circuit	Type of output			
	Direct current	Level	Positive pulse	Negative pulse
2 and 4 input gates.	6 ma at −6.2 v ±10%.	Maximum of 4 loads, no more than 2 of which are F loads.	Maximum of 4 loads, no more than 2 of which are F loads.	One G load only.

(Specifications continued on next page)

PSC 8 2 AND 4 INPUT PULSE NOR GATE

1. APPLICATION

PSC 8 is a special purpose NOR gate designed for use in computer, control, and communication equipment operating within the temperature limits of −30 and +60°C. It is used only for the AND operation when the general purpose NOR gate, PSC 7, would prove unsatisfactory due to the possible occurrence of spurious pulses in the output. PSC 8 should not be used as an OR gate or for inversion because in these applications it offers no advantage over PSC 7 and is wasteful of transistors and power.

2. DESIGN CONSIDERATIONS

PSC 8 is similar to PSC 7 except that it employs one transistor per input. It is similar to all the circuits of the digital logic set [1] in that current bias is used to prevent I_{CBO} flow in the base region, and clamped operation is used

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Power requirements:

Voltages	Current	
	2 Input gate	4 Input gate
−18 v ±10%	14 ma	14 ma
−6 v ±10%	14 ma	14 ma
+6 v ±10%	0.35 ma	0.7 ma

NOTES:

1. The −18-volt supply is obtained by connecting a −12-volt source in series with the −6-volt supply (see Section 2.2).

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus the drifts caused by environmental changes or aging.

4. The minimum duration of a level is 5μ sec.

5. Positive pulses are referenced to −6.2 volts ±10%. Negative pulses are referenced to ground (actually about −0.15 volt).

6. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude.

7. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature. The load in each case was maximum for that type of operation.

8. The turn-on time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change, and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

9. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

to obtain the benefits of standardization of the output voltage amplitude and speed up of the ON to OFF transition.

The value of the speed-up capacitors in the input circuits of the transistors has been increased to 220 pf from the 180 pf used in PSC 7. This increases the turn-off speed and compensates for the effect of the output capacitance of the additional transistors. It also increases the load presented to the driving circuit, but this is offset by the decrease in the number of input RC circuits to one per transistor. Hence, the input impedance of PSC 8 is the same as that of PSC 7.

When PSC 8 is used as an AND gate, spurious output pulses are prevented because the output terminal is clamped to ground if any of the transistors are conducting. If all inputs are at the −6-volt level and one input changes to the zero-volt level, the transistor associated with that input will be cut off, but all the other transistors will remain on in saturation and the output voltage will not change.

2.1 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PSC 7 through PSC 13, are arbitrarily given in terms of "F" and "G" loads. The "F" (flip-flop) load is derived from the input impedance of the bistable multivibrator, PSC 9. The "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PSC 7.

The equivalent circuit of each of these loads is shown in Figure 8–1. The actual load impedance may vary somewhat from the equivalent circuit describing it. Allowances were made for this, however, in formulating the output loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F"

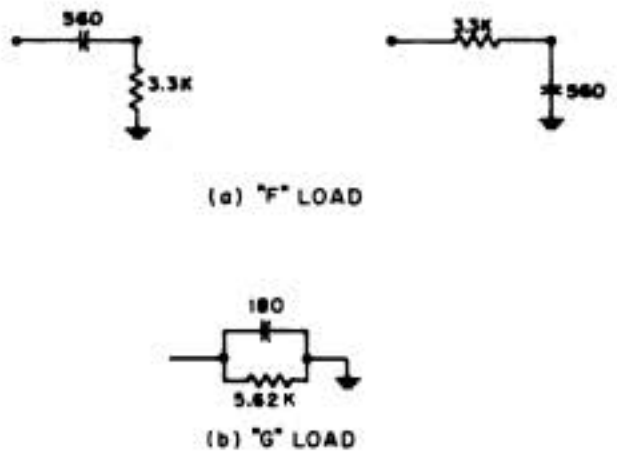


Figure 8–1.—Equivalent circuits of loads and input impedances.

load is a less accurate approximation than the "G" load.

2.2 *Power Supplies:* The −18-volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6-volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6-volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18-volt supply flowing in the reverse direction through the −6-volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6 volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PSC 9.

When PSC 8 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Section 2.4 of PSC 7.

3. PERFORMANCE

The performance of PSC 8 as an AND gate is illustrated by Figure 8–2. Only waveforms for the two-input gate are shown, since the performance of the four-input version is not significantly different. No curves of the OR operation are included, because PSC 8 is not

[1] See also Preferred Semiconductor Circuits PSC 7 through PSC 13.

intended for such use. All traces were obtained at a sweep speed of 0.2 μsec per division.

Only one input signal is shown in trace (a), since the input signal is not significantly affected by output loading. The traces of the output signals for no load and 1 "G" load (traces (b) and (c) respectively) do not differ significantly from those of PSC 7 when used as an AND gate.

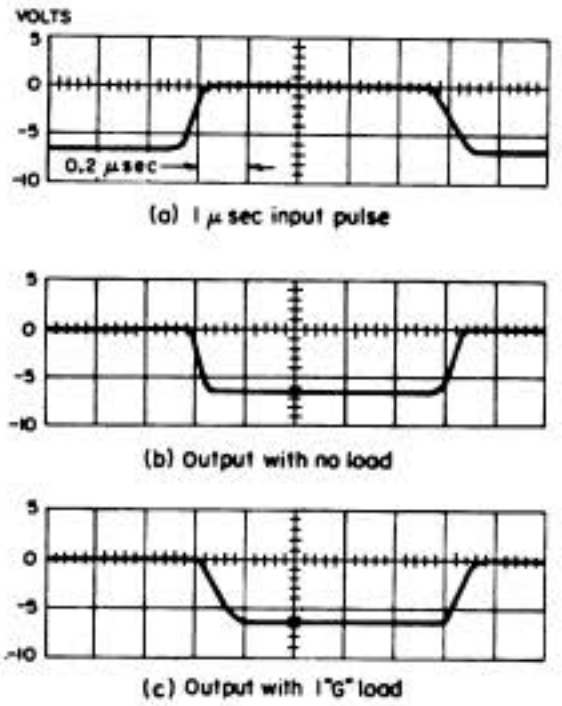


Figure 8-2.—Typical wavetorms for 2-input AND gate.

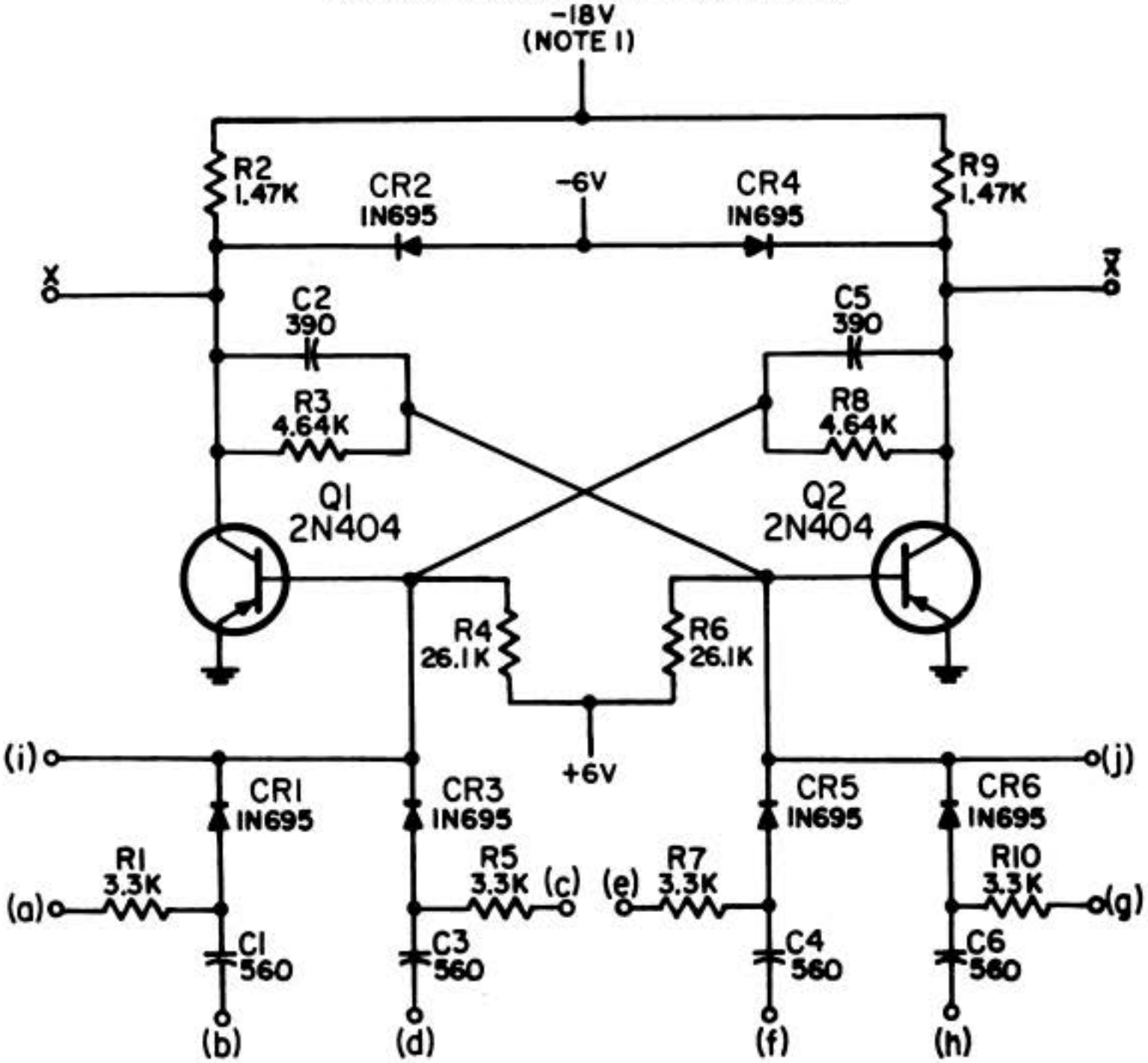
Notes

PREFERRED CIRCUIT NO. PSC 9
150 KC BISTABLE MULTIVIBRATOR

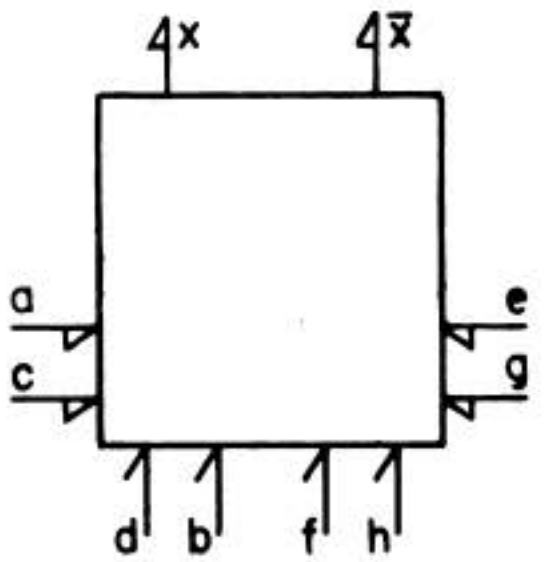
(Originally published as PC 212)

PREFERRED CIRCUIT NO. PSC 9

150 KC BISTABLE MULTIVIBRATOR



Unless otherwise stated: R in ohms; C>1 in $\mu\mu$f; C<1 in μf; L in μh



Symbol for PSC 9

(For specifications, see next page)

Components:

Maximum power dissipation (Note 2): R1, R4, R5, R6, R7, R10: <5 mw; R3, R8: 10 mw; R2, R9: 0.25 watt.

Limits (these are not tolerances; see Note 3): R1, R5, R7, R10: ±20%; all other R: ±5%. All C: ±10%.

Operating characteristics:

Temperature range: −30°C to +60°C.

Maximum operating rate: 150 kc (see Section 2.2).

Input impedance: One "F" load (see Section 2.4).

Input signal characteristics (terminals *b*, *d*, *f*, and *h*):

Polarity: Positive.

Amplitude: 6 volts reference to −6.2 volts ±10%.

Rise time: ≤0.4 μsec.

Width at 50% amplitude: 0.8 μsec minimum.

Switching and output characteristics under worst operating conditions:

Output	Level change	Maximum switching time (Note 4)	Maximum load
Collector of transistor switching from off to on.	−6 v to 0 v	Turn on time (Note 5): 0.9 μsec. Delay time: 0.5 μsec. Rise time: 0.4 μsec.	4 RC loads, type "F" or "G" (see Section 2.4).
Collector of transistor switching from on to off.	0 v to −6 v	Turn off time (Note 6): 1.6 μsec. Storage time: 0.2 μsec. Rise time: 1.4 μsec.	4 RC loads, type "F" or "G" (see Section 2.4). DC load: 5 ma ±10%.

Power requirements:

−18 volts ±10% at 24 ma.

−6 volts ±10% at 24 ma.

+6 volts ±10% at 0.5 ma.

NOTES:

1. The −18-volt supply is obtained by connecting a −12-volt source in series with the −6-volt supply (see Section 2.5).

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature, and with 4 loads connected to each output. See Figures 9–6 and 9–7 for the effects of the load.

5. The turn-on time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change, and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

6. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

PSC 9 150 KC BISTABLE MULTIVIBRATOR

1. APPLICATION

PSC 9 is a bistable multivibrator designed as the storage element in a compatible set of digital logic circuits [1] for use in computer, control, and communications equipment operating within the temperature limits of −30 and +60°C. It operates in conjunction with input diode gates which are an integral part of the circuit. For maximum versatility, direct connection is also provided to the base of each transistor. PSC 9 can be used as a counter and as a serial or parallel shift register at operating rates up to 150 kc under maximum load.

2. DESIGN CONSIDERATIONS

PSC 9 consists of two grounded-emitter amplifiers, similar to the circuit of PSC 7, with the output of each tied to the input of the other. The transistors are stabilized against I_{CBO} multiplication by resistors returned to a positive 6-volt potential. One output is clamped to −6 volts by diodes CR2 or CR4 and the other to ground (maximum −0.15 volts) by the saturated ON transistor. The diode gates, CR1, R1, C1; CR3, R5, C3; CR5, R7, C4; and CR6, R10, C6, are an integral part of the circuit.

2.1 *Circuit Operation:* Operation of the circuit is best described if it is assumed that the circuit is in a quiescent state, with Q1 off and Q2 on. The voltage at the collector of Q1 is then −6.2 volts (6 volts clamping plus the drop of −0.2 volts across diode CR2). This voltage causes sufficient current to flow through R3 from the base of Q2 to keep Q2 in saturation. Since Q2 is saturated, its collector is approximately at ground potential, and Q1 is held in the OFF condition by the positive bias (approximately 1 volt) applied to its base by the divider R4,R8.

To change the state of the multivibrator, a positive-going pulse is applied to the base of the ON transistor, Q2. After a delay caused by the base storage of minority carriers, Q2 begins to turn off, and the voltage at its collector begins to fall at a rate determined primarily by the RC network (which includes all loads) tied to its collector. This negative voltage change at the collector of Q2 is coupled back to the base of Q1 through the feedback network, C5,R8, and initiates the turn-on process in Q1. After a delay which depends on the characteristics of the transistor, the voltage at the collector of Q1 starts to rise, and the change is coupled to the base of Q2. The transition then proceeds regeneratively until Q1 is on and Q2 is off. Since the switching is not completely regenerative, the input pulse generator must provide a sink for the minority carriers stored in the base of Q2 and must maintain the base of Q2 at ground potential until Q2 has begun to turn off.

2.2 *Diode Gates:* The diodes connected to the transistor bases offer low resistance paths to positive-going input signals and discriminate against negative-going waveforms. The diodes may be primed, i.e., biased to allow easy flow of forward current, by bringing the associated resistive input connection (*a*, *c*, *e*, or *g*) to ground potential. They can be inhibited, i.e., biased to prevent the flow of forward current, by lowering the voltage at the resistive input to −6 volts. (The actual voltage is −6.2 volts ±10%, and the ground potential may be as large as −0.15 volts. For brevity, however, these values are referred to as −6 volts and ground potential.) The 1.85 μsec time constant of the diode gates determines the maximum operating rate of the multivibrator. More than three time constants are allowed for the gates to settle at the fastest operating rate (150 kc).

2.3 *Binary cells:* The binary cell is the elementary storage unit of a digital computer. The common binary cell connections discussed in this section are illustrated by means of block diagrams which are labeled to correspond with PSC 9. The nomenclature used is taken from *Logical Design of Digital Computers.*[2]

The response of a binary cell to a positive pulse depends on the condition of both the diode gate and the multivibrator at the time that the pulse is applied. A positive trigger applied

[1] See also Preferred Semiconductor Circuits PSC 7 through PSC 13.

[2] M. Phister, *Logical Design of Digital Computers*, John Wiley and Sons, Inc., New York, 1958.

to one of the pulse inputs (*b*, *d*, *f*, or *h*) will cause the multivibrator to change states only if the diode gate is primed, and if the associated transistor is in the ON state. The ON transistor may be identified in Figures 9-1 through 9-4 as the one with the "0" output.

(*a*) T connection: When the T connection, Figure 9-1, is used, the multivibrator changes state once for each positive pulse applied to the T input. One of the diode gates, *ab* or *ef*, is always primed because of the connection of the resistive inputs *a* and *e* to the outputs X and $\overline{X}$, respectively. If the cell is originally in the "1" state,[3] as shown in the figure, a positive pulse put into T will flow through *f*, because the associated diode is primed by connection to the "0" output at $\overline{X}$, and the diode gate *ab* is inhibited by connection to the "1" output at X. This pulse will cause the multivibrator to change state and in so doing will prime the diode gate *ab* so that the binary is ready for the next pulse. Diode gates *cd* and *gh* are not needed in the T connection and are inhibited by connection to the −6-volt source to prevent spurious signals or pickup at *d* and *h* from interfering with the operation of the cell.

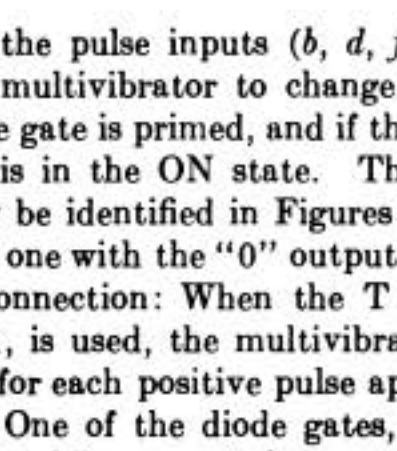


Figure 9-1.—T connection.

(*b*) RS connection: In the RS connection, shown in Figure 9-2, both the *cd* and *gh* gates are always primed, and positive input pulses must be directed to the proper gate to cause the cell to change state. If the counter is in the "1" state as shown, a positive pulse directed to the *h* input will cause the cell to change to the zero state, but a positive signal directed to the *d* terminal will have no effect. Once the counter changes to the "0" state a positive pulse must be directed to the *d* input to put the binary in the "1" state again. The R input, terminal *h*, is the reset input, since it is used to place the binary cell in the "0" state. The S input, terminal *d*, is the set input since it is used to place the binary in the "1" state. If positive pulses arrive simultaneously at the R and S inputs, the action of the multivibrator is not predictable.

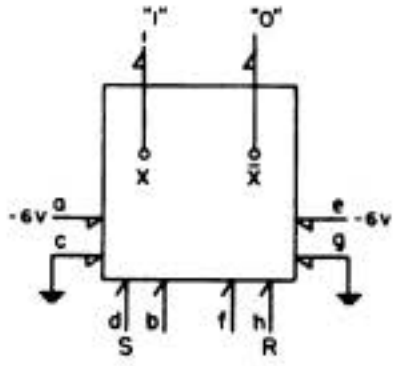


Figure 9-2.—RS connection.

(*c*) JK connection: If positive pulses can arrive simultaneously at both sides of the multivibrator, the JK connection, Figure 9-3, is used. This is merely a T connection with separate trigger inputs. As in the RS connection, positive input pulses must be directed to the proper input to cause the binary cell to change its state, but only the input which is connected to the base of the ON transistor is primed. Therefore, if positive pulses come into both the J and K inputs simultaneously, only the ON transistor will receive the pulse, and the binary will change states. The JK connection is used in preference to the RS connection only when simultaneous pulses at the set and reset inputs must be dealt with.

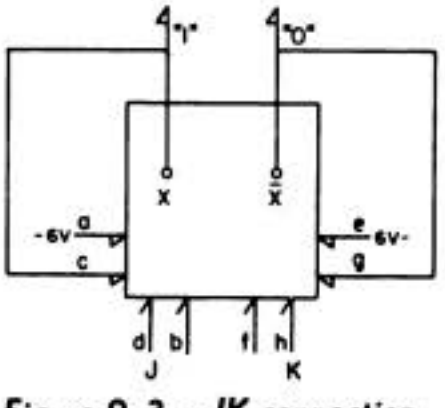


Figure 9-3.—JK connection.

(*d*) RST connection: The RST connection (Figure 9-4) is the usual binary cell connection for a digital counter bit and is discussed in detail in Section 4.1. It may be triggered by positive pulses directed to the T terminal, or

[3] The output of a binary cell is said to be "1" when the indicating output (X output of PSC 9) is "1" (−6 volts) and "0" when the indicating output is "0".

by set and reset pulses directed in the proper order to the S and R terminals. The JKT connection can be formed by connecting the *c* and *g* terminals to the X and $\overline{X}$ outputs, respectively, instead of to ground as shown in Figure 9–4. Since this constitutes double loading on the outputs, this connection is not ordinarily used.

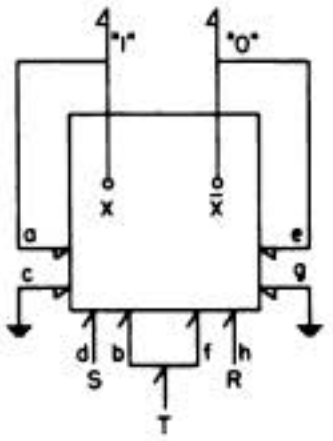


Figure 9–4.—RST connection.

2.4 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PSC 7 through PSC 13, are arbitrarily given in terms of "F" and "G" loads. The "F" (flip-flop) load is derived from the input impedance of the bistable multivibrator, PSC 9. The "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PSC 7.

The equivalent circuit of each of these loads is shown in Figure 9–5. The actual load impedance may vary somewhat from the equivalent circuit describing it. Allowances were made for this, however, in formulating the output loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

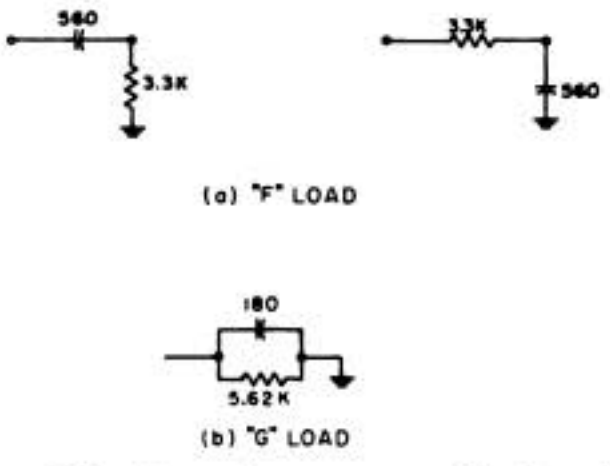


Figure 9–5.—Equivalent circuits of loads and input impedances.

2.5 *Power Supplies:* The −18-volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6-volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6-volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18-volt supply flowing in the reverse direction through the −6-volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6-volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads, such as other bistable multivibrators.

When PSC 9 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Section 2.4 of PSC 7.

3. PERFORMANCE

Figures 9–6 through 9–9 illustrate the effect of load on the performance of PSC 9. All waveforms were taken at a sweep speed of 0.2 μsec per division with a vertical scale of 5 volts per division.

Figure 9–6 shows the waveforms at the indicating output, X, for several load combinations when the binary is being switched from 0 to 1. Under these conditions transistor Q1 is turned off by the input signal, and the voltage at its collector, which is the X output, changes from ground to −6 volts. The capacitive load on the collector must charge through a resistance roughly equivalent to the parallel combination of R2, R3, and the load resistance. The rise time of the output wave-

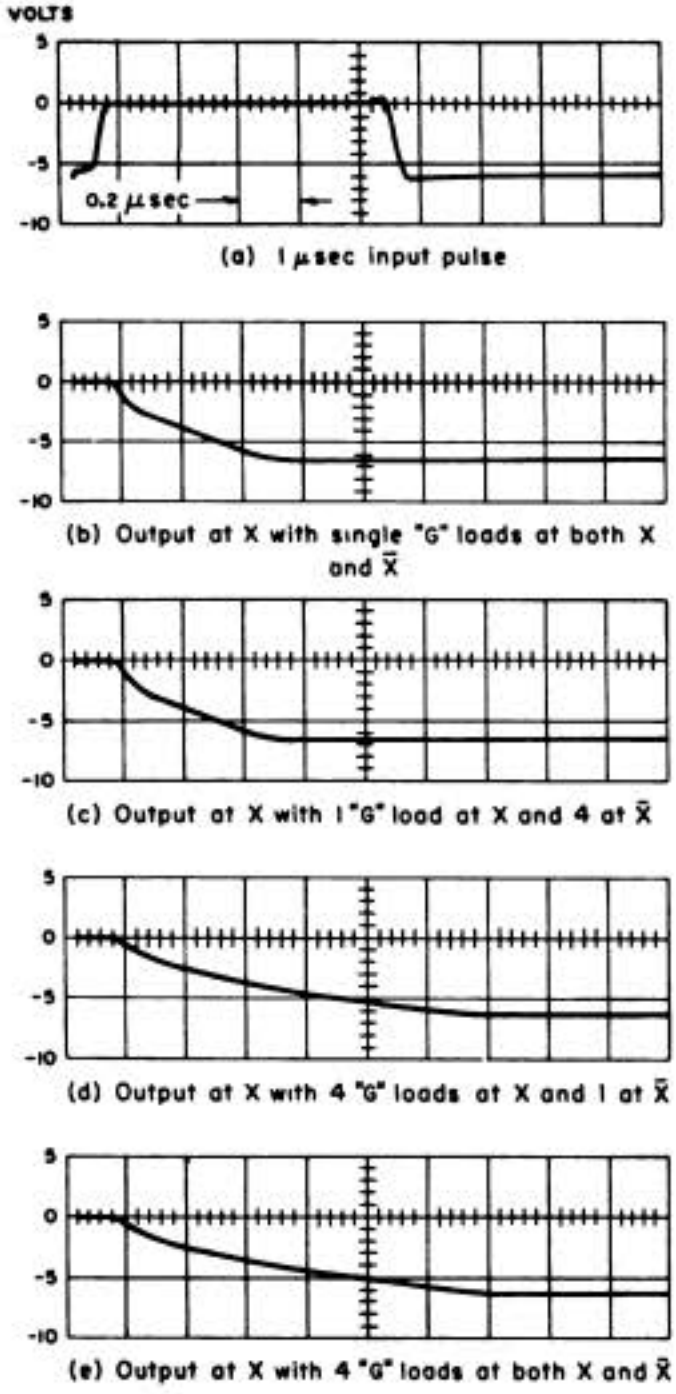


Figure 9-6.—Effects of the loads on the 0 to 1 transition at the X output.

form is principally determined by the time required to charge this capacitance, and as can be seen by comparing traces b with c and d with e, the rise time of the X output for the 0 to 1 transition is a function of the load on X and is relatively unaffected by the load on $\overline{X}$.

Figure 9-7 shows the waveforms at the indicating output when the binary is being switched from 1 to 0, for the same load combinations as in Figure 9-6. In this case Q1 is turned on by Q2, and the load on the collector of Q2, the $\overline{X}$ output, has a significant effect on the output at X, as can be seen by comparing traces b with c and d with e.

The switching sequence for the 1 to 0 transition at the X output is shown in Figures 9-8 and 9-9. The input pulse is applied to transistor Q2 which turns off. Q2 collector ($\overline{X}$ output) voltage falls to −6 volts relatively slowly because the capacitance connected to the collector must charge through the equivalent resistance mentioned above. By contrast, the rise of Q1 collector voltage is more rapid because the saturation resistance of the transistor furnishes an additional discharge path for the load capitance, but there is considerable delay in the turn-on of Q1 because the base drive comes from the slowly changing collector voltage of Q2. When four "G" loads are connected to the $\overline{X}$ output (Fig. 9-9), the rise time of the waveform at $\overline{X}$ is further increased, causing further delay in the turn-on of Q1.

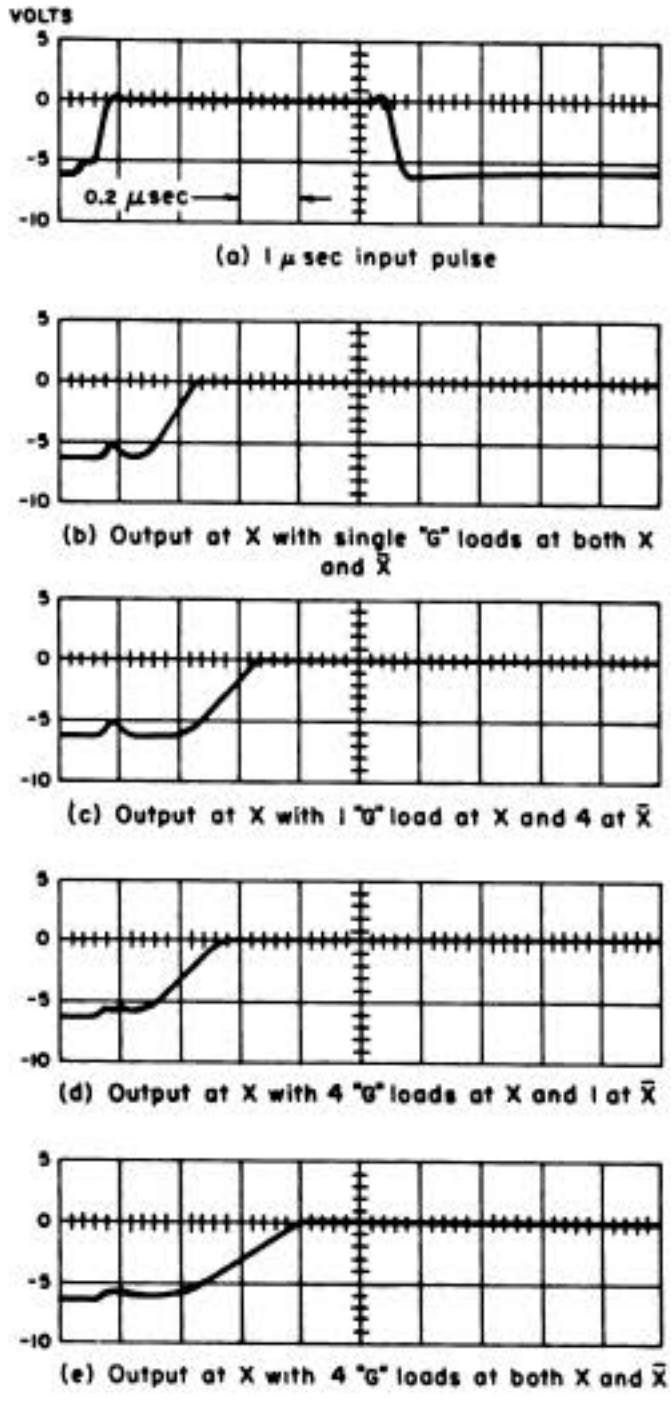


Figure 9-7.—Effects of the loads on the 1 to 0 transition at the X output.

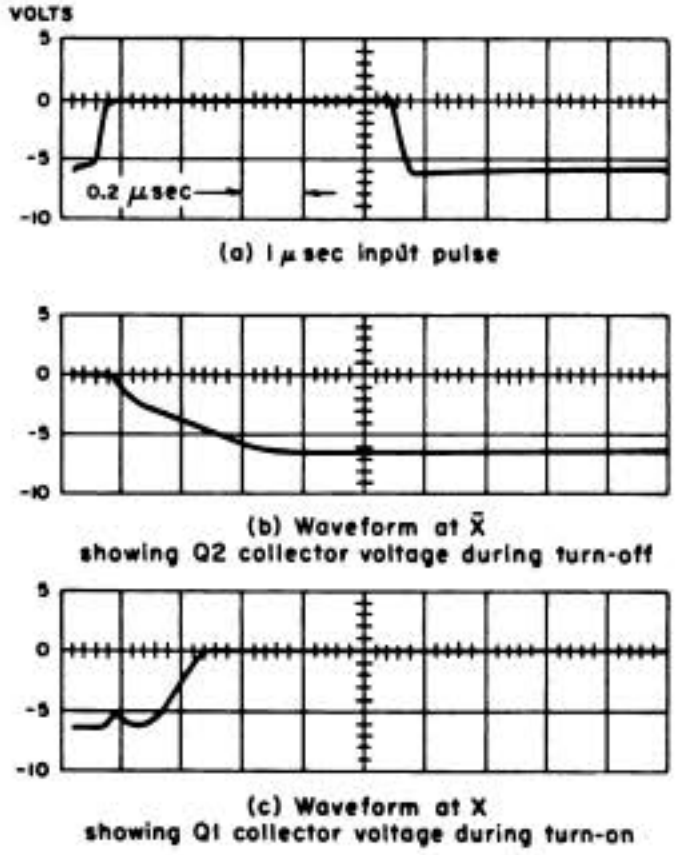


Figure 9–8.—Switching sequence showing the resetting of PSC 9 with single "G" loads at both X and X̄.

Since the load on the X output has not changed, the increase in the turn-on time of Q1 is mostly caused by the increase in delay time.

Although these waveforms (Figures 9–6—9–9) illustrate the effect of load on the waveform at the indicating output, similar results would be obtained at the X̄ output. In general, the delay and rise times of the output waveform at a given output are proportional to the load on that output during the 0 to 1 transition, but are primarily controlled by the load on the other output during the 1 to 0 transition.

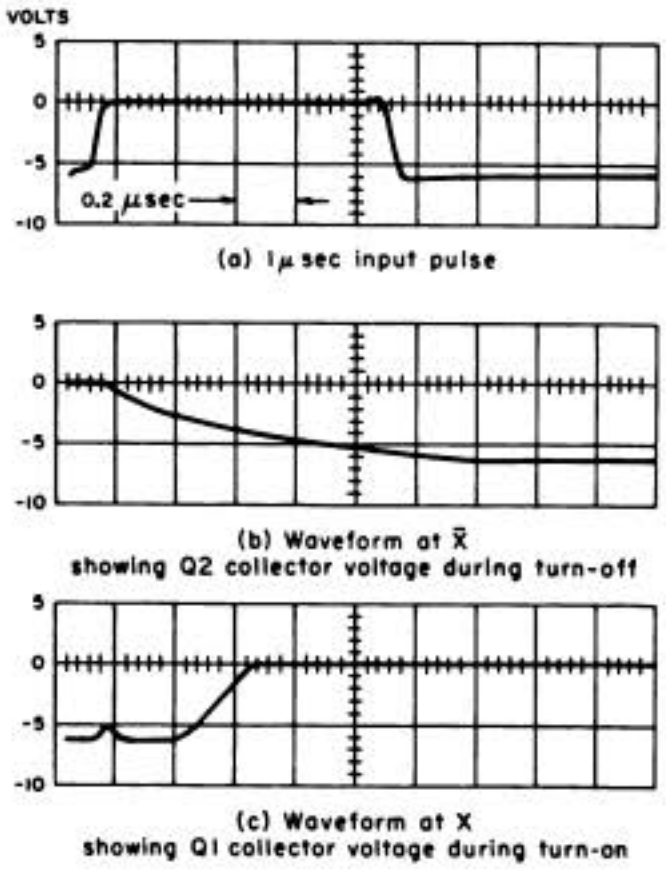


Figure 9–9.—Switching sequence showing the resetting with 4 "G" loads at X̄ and 1 at X.

4. EXAMPLES OF USE

PSC 9, when connected as a binary cell, can indicate a "1" or a "0" and can store 1 "bit" of information; "n" such circuits can be connected in tandem to form an n-bit register to store n bits of information or an n-bit counter to count from 0 to (2^n-1).

4.1 *Counters:* Four binary cells of the RST type connected as a 4-bit counter are shown in Figure 9–10. The pulses to be counted are fed into the counter through the trigger (T) input of the first counter, and the indicating output of each counter except the last is fed to the trigger input of the succeeding binary. The output of the last binary may be used, for instance, to initiate the eighth or sixteenth step in a given process; or the counter may be used to count items, in which case a visual indication of the count can be had by connecting an indicator, such as PSC 13, to the X terminal of each binary. Depending on the system logic, the set level and reset level connections may be primed by connecting them to ground, or they may be connected to external logic which will inhibit them until a set or reset pulse is due to arrive.

To illustrate the operation, assume that the set and reset levels have been grounded and that a reset pulse has been put into the counter so that all the indicating outputs read "0". The first positive pulse to enter the trigger input will cause the X output of binary C1 to change from "0" to "1". This change will be coupled to the trigger input of C2, but since it is negative-going, it will have no effect on C2. When the second positive trigger pulse enters the trigger input, however, the indicating output of C1 will change from "1" to "0", and this positive-going change will cause C2 to change from "0" to "1". This change in C2 output will be coupled to the input of C3 but will not affect C3 since it is negative-going. This sequence of events will be repeated for every

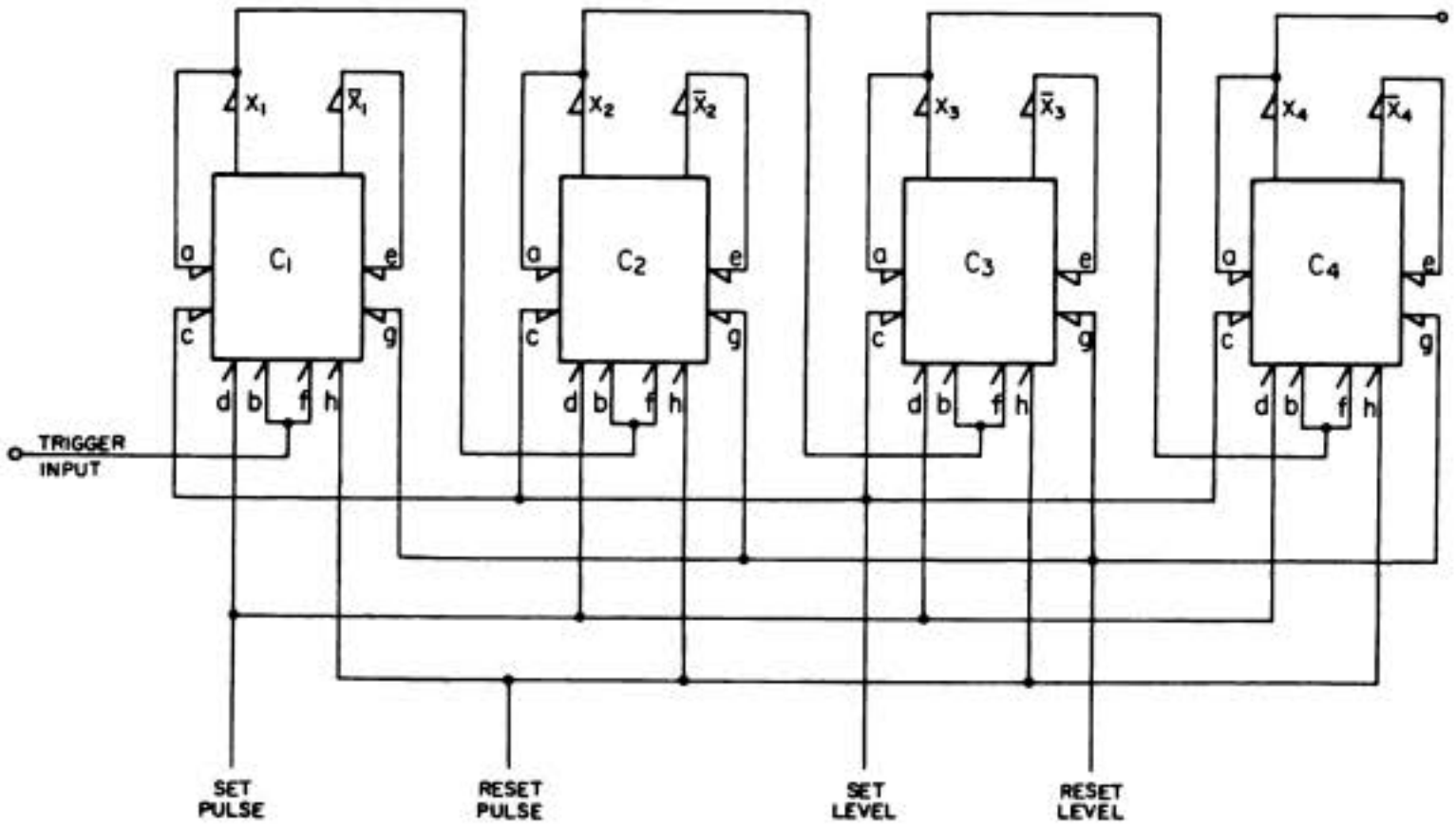


Figure 9–10.—Connections for a 4-bit binary counter.

positive pulse or positive change of voltage at the trigger input, with each succeeding binary changing state once for every two changes of state of the preceding one. Fifteen positive input pulses or level changes would be required to cause all the binaries in Figure 9–10 to read "1".

4.2 *Shift Registers:* A group of binary cells may be connected in tandem to form a shift register, which is a device capable of retaining information in the form of an ordered set of characters and of displacing that information one or more places to the left or right. Information can be inserted in such a register in parallel, i.e., in all cells simultaneously, or it can be inserted serially, in which case one bit is inserted in the first cell, then shifted to the second cell when a second bit is inserted in the first, and the process continued until an ordered set of data has been inserted in the register. Data contained in a shift register, whether initially inserted in parallel or in serial form, can be shifted out serially when so required.

When PSC 9 is used to form a shift register, a modified T connection is used, as shown in Figure 9–11. The capacitive inputs of one set and one reset gate are connected together to form a common trigger terminal as in the T connection, but the resistive inputs associated with each of these gates are primed or inhibited in accordance with the data to be inserted in the cell. The input data is applied to the level gates, *a* and *e*, and is registered in the cell by the shift pulse which is applied to the common trigger input. For proper operation, the inputs at *a* and *e* must be different, that is, if the level at *a* is "1", the level at *e* must be "0", and vice versa.

Since the function of the shift register binary is to store information, it must duplicate at its output the signal applied to the input terminals. When triggered, it must change state if the input and output are different, but must remain in the same state if the input and output are the same, and the proper action must be determined by the level inputs. If the output of the cell is "1", as indi-

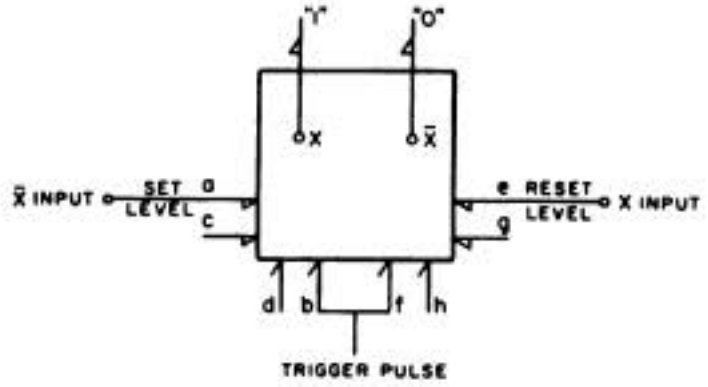


Figure 9–11.—Modified T connection used for shift register.

cated in Figure 9–11, and a "0" is to be shifted in, the reset side of the binary must be primed so that the trigger pulse will cause the binary to change from "1" to "0". This can be accomplished by directing the "0" to be shifted in to the reset level input, terminal *e*. If a "1" is to be shifted in, it must be directed to the reset side of the binary to inhibit the reset gate and prevent a change in state. If at the same time a "0" is directed to the set level input, terminal *a*, the set gate will be primed but no change in the state of the binary will occur because this directs the trigger pulse to the OFF transistor.

If the output of the register binary is originally "0", on the other hand, and a "1" is to be shifted in, a "0" level must be directed to the set input so that the shift pulse will cause the binary to change from "0" to "1". If, at the same time, the "1" to be shifted in is directed to the reset input, it will not prevent the required change in state of the binary. If a "0" is to be shifted in, it must be directed to the reset input so that the shift pulse will be directed to the OFF transistor, preventing a change in state of the binary. Correct operation of the register binary will be obtained, therefore, if the indicating output of the driving circuit is connected to the reset side, and the opposite signal connected to the set side of the register binary.

To connect several binary cells to form a shift register, the set level of each cell is connected to the $\overline{X}$ output of the previous cell, and the reset level is connected to the X output. If the data are to be registered serially, the input to the first cell is connected to logic external to the register (a NOR gate, a second register, etc.), care being taken to continue the cross connection of set and reset level inputs as was done between cells. In the case of parallel input, however, the resistive inputs to the gates of *each* cell of the register are connected to the inserting logic. For example, if the inserted information comes from a binary counter, the reset input to each cell of the shift register is connected to the indicating output of the same ordered cell of the counter, and each set input of the register is connected to the non-indicating output of the counter. Although information may be shifted into the

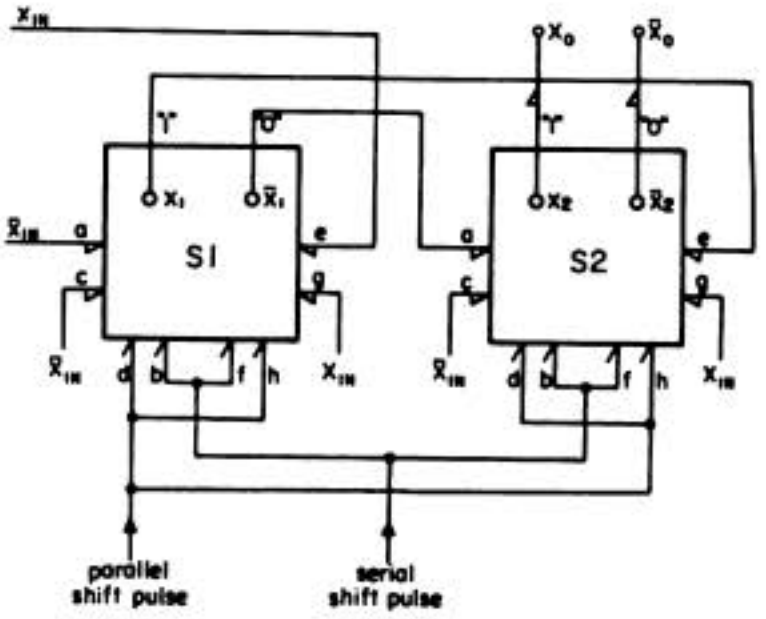


Figure 9–12.—Two-stage shift register.

register either serially or in parallel, it is usually shifted out serially.

Figure 9–12 shows a two-stage shift register connected for both serial and parallel operation. The modified T connection using gates *ab* and *ef* is used for the serial shift. The trigger terminals formed by connecting terminals *b* and *f* of each of the cells are all connected together to form the serial shift pulse terminal, since the shift pulse is applied to all cells simultaneously. Now, however, use is made of the two extra gates of each cell *cd* and *gh* to form an additional modified T connection. The resistive inputs of each of these gates may be connected to individual cells of the data source so that data can be shifted into S1 and S2 simultaneously when a parallel shift pulse is applied.

In a shift register, the shift pulse is applied to all cells of the register simultaneously. When the register is operating serially, each cell must register the output of the preceding cell as it was prior to the shift pulse, even though this output may also be changing as the driving cell responds to the shift pulse. This is made possible by the time delay associated with the level inputs to the cell gates, which delay prevents the prime or inhibit signals on the gate diodes from changing materially during the transition period following the application of the shift pulse. The shift pulse, which is capacitively coupled to the gate diodes, has a maximum rise time of 0.4 μsec. The integrating network as-

sociated with the level input of each diode gate has a time constant of 1.85 csec, which is sufficient to prevent a significant change in level magnitude during the transition time.

4.3 *Circuit Modifications:* The basic circuit of PSC 9 can be modified to allow manual setting of individual cells in a logical array, or of entire registers or groups of registers. A normally closed switch inserted in the emitter of Q2 permits resetting of the binary by opening the switch. Since several emitters can be returned to ground through the same switch, this method permits resetting of several binaries simultaneously. The binaries can be set by placing the switch in the emitter of Q1.

Individual binaries can be set or reset by using a manually-operated, normally-open switch to ground temporarily the collector of Q2 or Q1. This is feasible because PSC 9 can operate without damage to the circuit when either collector is temporarily grounded.

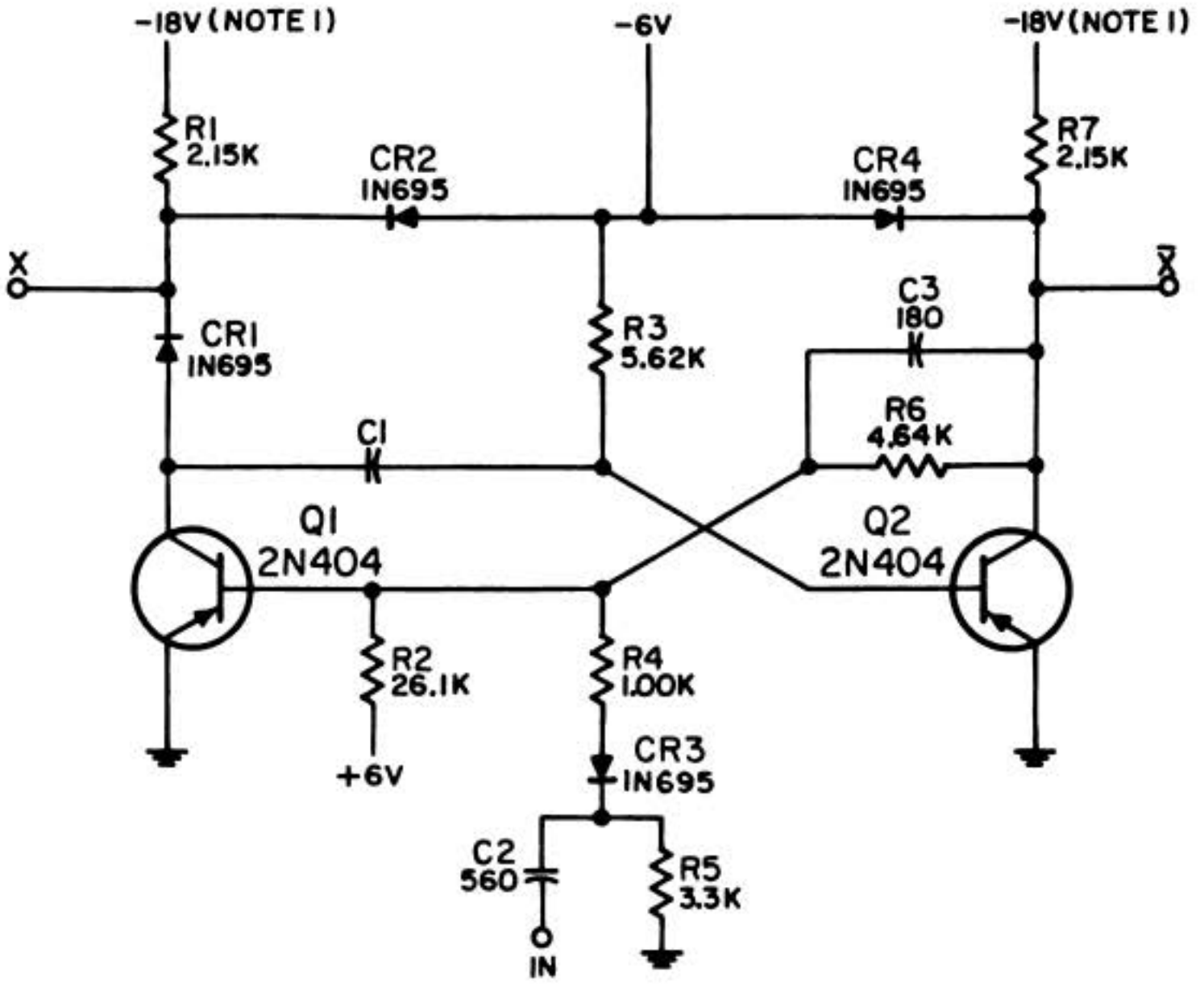
Notes

PREFERRED CIRCUIT NO. PSC 10

MONOSTABLE MULTIVIBRATOR

(Originally published as PC 213)

PREFERRED CIRCUIT NO. PSC 10
MONOSTABLE MULTIVIBRATOR



Unless otherwise stated; R in ohms; C > 1 in $\mu\mu$f; C < 1 in μf; L in μh

Components:

$$C1 \quad (\text{pf}) = \frac{\text{Total time delay } (\mu\text{sec})}{3.9 \times 10^{-3}}$$

Maximum power dissipation (Note 2): R1, R7: 180 mw; R2, R4, R5, R6: <10 mw; R3: 12 mw.
Limits (these are not tolerances; see Note 3): R5: ±20%; all other R: ±5%. C1: ±5%; all other C: ±10%.

Operating characteristics:

Temperature range: −30°C to +60°C.
Total time delay (Note 4): 2 μsec to 0.1 second.
Recovery time: Approximately 25% of total time delay.
Input impedance: One "F" load (see Section 2.3).
Input pulse characteristics:
Polarity: Negative.
Amplitude: 6 volts ±10% referenced to ground.
Rise time (Note 5): ≤0.4 μsec.
Width at 50% amplitude: 0.5 μsec minimum.

(Specifications continued on next page)

Operating characteristics—*Continued*

Switching characteristics with maximum load attached:

Output	Maximum switching time (Note 6)
X	Turn-on time (Note 7): 0.7 μsec. Delay time: 0.3 μsec. Rise time: 0.4 μsec. Turn-off time (Note 8): $8.9 \times 10^3 \times C1$ μsec + 0.1 μsec. Storage time: 0.1 μsec. Fall time: $8.9 \times 10^3 \times C1$ μsec.
$\overline{X}$	Turn-off time: See Section 3.3. Storage time: 0.2 μsec. Rise time: See Section 3.3. Turn-on time: 1.0 μsec (Note 9). Delay time: 0.5 μsec. Fall time: 0.5 μsec.

Maximum output load:

Output	Direct current	RC load
X	4 ma at −6.2 volts ±10%	Not used.
$\overline{X}$	3 ma at −6.2 volts ±10%	2 "F" or "G".

Power requirements:
−18 volts ±10% at 10 ma.
− 6 volts ±10% at 10 ma.
+ 6 volts ±10% at 0.25 ma.

NOTES:

1. The −18-volt supply is obtained by connecting a −12-volt source in series with the −6-volt supply (see Section 2.4).

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. The total time delay is a function of R3,C1 and is the time interval between the points where the leading edge of the input signal and the trailing edge of the output signal have completed 10% of their total amplitude change (see Section 3.1).

5. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude; fall time is the time required for the trailing edge of the waveform to decrease from 90% to 10% of its maximum amplitude.

6. The maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature. Two RC loads were connected to the $\overline{X}$ output during these measurements.

(Notes continued on bottom of next page)

PSC 10 MONOSTABLE MULTIVIBRATOR

1. APPLICATION

PSC 10 is a monostable multivibrator designed to perform the delay function in a compatible set of digital logic circuits[1] for use in computer, control, and communications equipment operating within the temperature limits of −30 and +60°C. Delays between 2 microseconds and 100 milliseconds can be obtained by selection of feedback capacitor C1. The timing resistor, R3, may be replaced by a variable resistor to provide adjustment of the time delay.

2. DESIGN CONSIDERATIONS

2.1 *Circuit Configuration:* PSC 10 consists of two cross-coupled common-emitter circuits. It differs from the bistable multivibrator, PSC 9, mainly in the cross-coupling network configuration. PSC 10 is stable in only one state, because the coupling from the collector of Q1 to the base of Q2 is achieved by means of a capacitor rather than a parallel RC network. Connection of the base of Q2 to the −6-volt supply through R3 causes Q2 to remain on in saturation in the absence of external signals. As in other circuits of this group, the collector of the OFF transistor is clamped to −6 volts by diode CR2 or CR4.

Diode CR1 clips any positive-going noise peaks on the −6-volt supply and prevents them from feeding through CR2 and coupling through C1 into the base of Q2. Since Q2 is normally on, a positive pulse at the base might turn if off. Hence, CR1 is connected with a polarity which discriminates against positive pulses, but at the same time does not interfere with transistor current flow through the collector of Q1.

Diode CR3, capacitor C2, and resistor R5 comprise a diode gate similar to the gates used in the bistable multivibrator, PSC 9. The chief difference is the polarity of the diode connection in PSC 10, which allows a negative-going waveform to go through the gate but discriminates against positive signals. Resistor R4 reduces the loading on the driving circuit when transistor Q1 is turned on by the input signal, and also increases the ability of the circuit to discriminate against noise.

2.2 *Circuit Operation:* In the stable state Q1 is off, Q2 is in saturation, and C1 is charged via CR1 and the emitter-base diode of Q2 to a potential of 6 volts. Application of a negative-going input voltage drives the base of Q1 negative with respect to ground and thus causes a current to flow in the base-emitter circuit of Q1 which will charge the base.[2,3] The time taken to charge the base is quite small. At the end of this period, collector current begins to flow, and the potential at Q1 collector rises toward ground.

As the potential at the collector of Q1 rises, it is impressed on the base of Q2 via C1.

[1] See also Preferred Semiconductor Circuits PSC 7 through PSC 13.

[2] R. Beaufoy and J. J. Sparkes, "The Junction Transistor as a Charge-Controlled Device," *ATE Journal*, Vol. 13, No. 4, Oct., 1957, pp 310–327. (Automatic Telephone and Electric Co., Strowger Works, Liverpool 7, England.)

[3] R. S. Ledley, *Digital Computer and Control Engineering*, McGraw-Hill, New York, 1960, pp. 658–667.

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7. The turn-on time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change, and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

8. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (the time required for the first 10% change in collector voltage) and the fall time (the time required for the voltage change from 10% to 90%).

9. In this case the signal which turns the transistor on is the negative portion of the base waveform (Fig. 10–4(e)). The fall time is measured, therefore, from the point where the negative portion of Q2 base voltage first reaches 10% of its final amplitude.

When Q1 saturates, it clamps one side of C1 to ground. Since C1 has had no time to discharge, the other side impresses a positive voltage with respect to ground on the base of Q2. This voltage acts to drive the minority carriers out of the base of Q2 and to turn it off. Although the +6 volts impressed on the base causes Q2 to come out of saturation rapidly, the voltage at the collector of Q2 falls at a rate primarily determined by the effective capacitance of the collector load. The negative voltage at the collector of Q2 is applied to the base of Q1 and keeps Q1 on until Q2 is turned back on by the discharge of C1.

Q2 is kept off by the potential applied to its base, but this potential falls from +6 volts toward −6 volts as C1 discharges through R3. When the voltage at the base of Q2 goes slightly negative with respect to ground, the base-emitter circuit of Q2 begins to conduct and collector current starts to flow. The voltage at the collector of Q2 rises toward ground and is applied to the base of Q1, turning it off.

With Q1 off and Q2 on, one side of C1 is connected to ground via the base-emitter diode of Q2, and the other side is connected to the −18-volt supply through CR1 and R1. CR2 is back biased until the negative potential at the collector of Q1 reaches −6 volts. The recovery time of the circuit is a function of the time required to charge C1 through R1. Since C1 also controls the time delay, the recovery time is related to the delay time and is about 25% of the total delay time if R3 is a fixed resistor of the value shown. The recovery time must be added to the total delay time to determine the maximum operating rate of the circuit. At the conclusion of the recovery time, Q1 is off, Q2 is on, and the circuit has returned to its initial stable state.

The sequence of these events is shown by the waveforms in Figure 10–1. The time delay generated by PSC 10 begins when the leading edge of the input pulse reaches 10% of its peak amplitude, and ends when the trailing edge of the output waveform has completed 10% of its change. The waveform at the base of Q2 is the basic timing waveform determined by the values of R3 and C1. The beginning of this waveform, as well as the leading edge of the output voltage waveform,

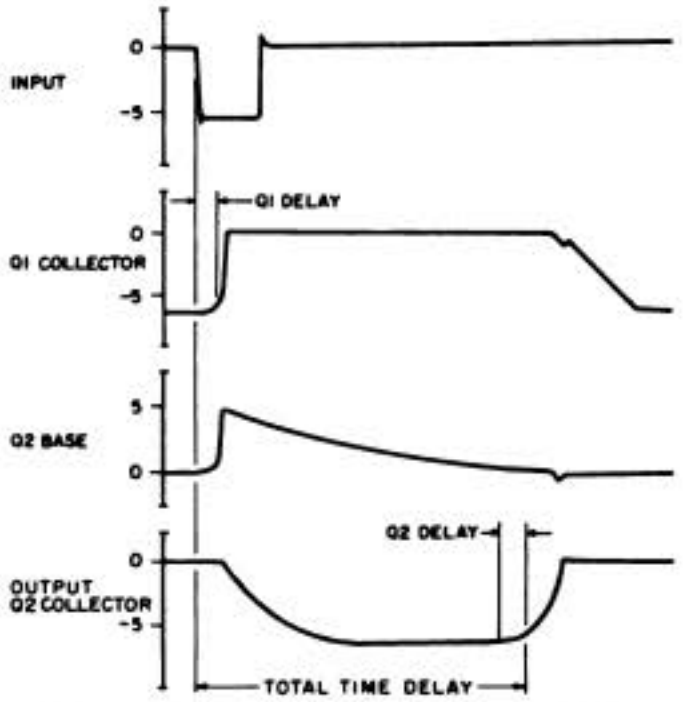


Figure 10–1.—Operation of time delay multivibrator.

is delayed from the leading edge of the input pulse by the delay time[4] of Q1. The delay time of Q2,[5] which ends after the trailing edge of the output waveform has completed 10% of its change, also contributes to the total time delay. The time required to complete both the trailing edge of the output waveform (Q2 collector) and the trailing edge of Q1 collector waveform is a function of the loads attached to each of these collectors. Although Q1 has turned off before the completion of the output waveform, its collector voltage falls at a rate determined by the time required to recharge C1 through R1 and the emitter-base diode of Q2. This determines the recovery time of the circuit but does not affect the time delay.

2.3 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PSC 7 through 13, are arbitrarily given in terms of "F" and "G" loads. The "F" (flip-flop) load is derived from the input impedance of the bistable multivibrator, PSC 9; the "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PSC 7.

[4] For a definition of delay time, see Note 7, p. 10–4.
[5] See Note 9, p. 10–4.

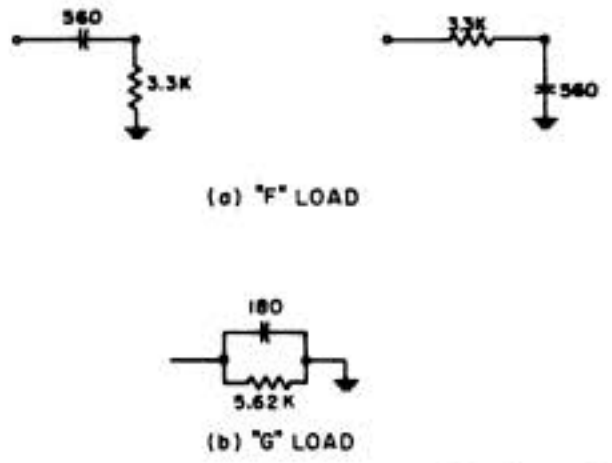


Figure 10–2.—Equivalent circuits of loads and input impedances.

The equivalent circuit of each of these loads is shown in Figure 10–2. The actual load impedance may vary somewhat from the equivalent circuit describing it. Allowances were made for this, however, in formulating the output loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

2.4 *Power Supplies:* The −18-volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6-volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6-volt supply. If the −18-volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18-volt supply flowing in the reverse direction through the −6-volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6-volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PSC 9.

When PSC 10 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Section 2.4 of PSC 7

3. PERFORMANCE

3.1 *Factors Affecting Time Delay Accuracy:* Three principal sources of error in the total delay time are as follows:

(1) The delay times of the two transistors Q1 and Q2. The effect of delay time is discussed in Section 2.2 where it is shown that the time interval between the beginning of the input pulse and the end of the output waveform includes the delay time of the transistors as well as the basic time interval determined by R3,C1.

(2) Variation in the input characteristics of Q2. The principal characteristics of Q2 which affect the delay are the storage time and I_{CBO} characteristic. During the storage time of Q2, which begins at the same time that C1 begins to discharge, a portion of the charge from C1 flows into the base of Q2 to neutralize the minority carriers stored there during saturation. This charge subtracts from the initial charge of C1 and shortens the total delay. The back resistance of the emitter-base diode of Q2 is in parallel with R3 so that I_{CBO} current flow further shortens the time delay. These are the principal cources of error for time delays less than 10 μsec. They cause a variation in the total time delay of from ±10% at 2 μsec to ±6% at 10 μsec. In the range from 10 to 100 μsec (where the effect of delay time is negligible) the variation is less than 6%.

(3) Variations in the values of R3 and C1. The actual time delay varies directly with variations in R3 and C1. The variations due to the initial tolerance of the components plus the changes caused by temperature and time add an additional ±10% variation to the total time delay, under the worst conditions. If R3 is made adjustable, and C1 is selected to have a temperature coefficient opposite that of R3, this additional deviation can be held to ±2%, or less.

3.2 *Input Signal Requirements:* As indicated by the waveforms in Figure 10–1, the initiation of the timing cycle is non-regenerative. The input signal, therefore, must supply sufficient charge to turn Q1 on. The combinations of input-signal width and amplitude required for reliable triggering when all components affecting triggering sensitivity are at their worst-case limits are shown in Figure

10-3. The 0.5 μsec minimum pulse width specified on page 10-2.is based on a minimum amplitude of 5.4 volts (6 volts—10%) and on the consideration that the effective amplitude may be reduced by noise on the —6-volt supply.

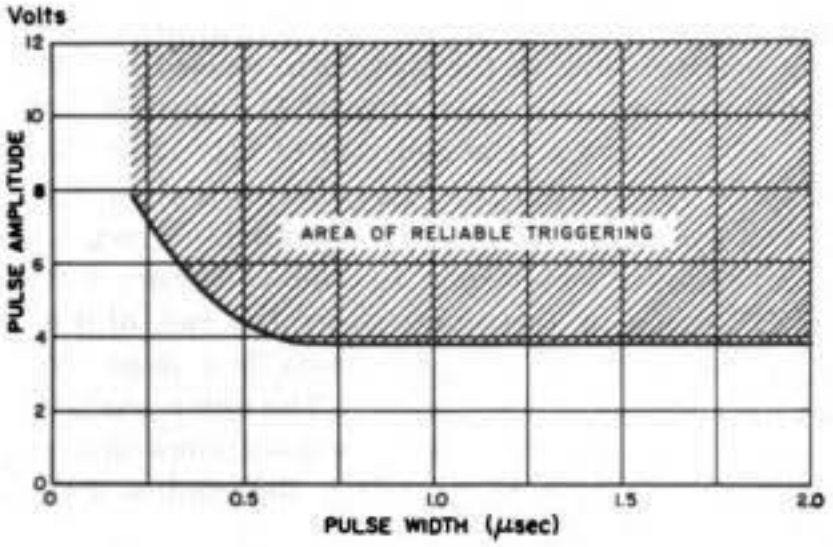


Figure 10-3.—Trigger requirements.

3.3 *Typical Waveforms:* Typical waveforms are shown in Figure 10-4 (a) through (f) and are discussed in the corresponding paragraph below. All of the waveforms were made at a sweep speed of 1 μsec per division.

(a) Input pulse. A negative 1 μsec pulse of approximately 6 volts amplitude is applied as a trigger. The pulse width must be greater than the turn-on time of Q1 to assure proper triggering.

(b) Voltage at anode of gate diode, CR3.

(c) Voltage at the base of Q1. Prior to the application of the trigger, the base of Q1 is maintained slightly positive by the bias supply. The base is driven negative by the trigger, causing Q1 to turn on. When Q1 turns on, it causes Q2 to turn off, and the potential from the collector of Q2, applied via the voltage divider R6,R2 keeps Q1 on. At the completion of the cycle, the charge stored in C3 provides a current source necessary for fast replacement of the minority carriers stored in the base of Q1. When Q1 turns off, the discharge of C3 causes the base to be momentarily driven positive.

(d) Voltage at the collector of Q1. Initially, Q1 is biased off, and the collector is clamped at —6 volts by diode CR2. When a negative pulse is applied to the base of Q1, its collector voltage rises with a time constant which is a function of the individual transistor.

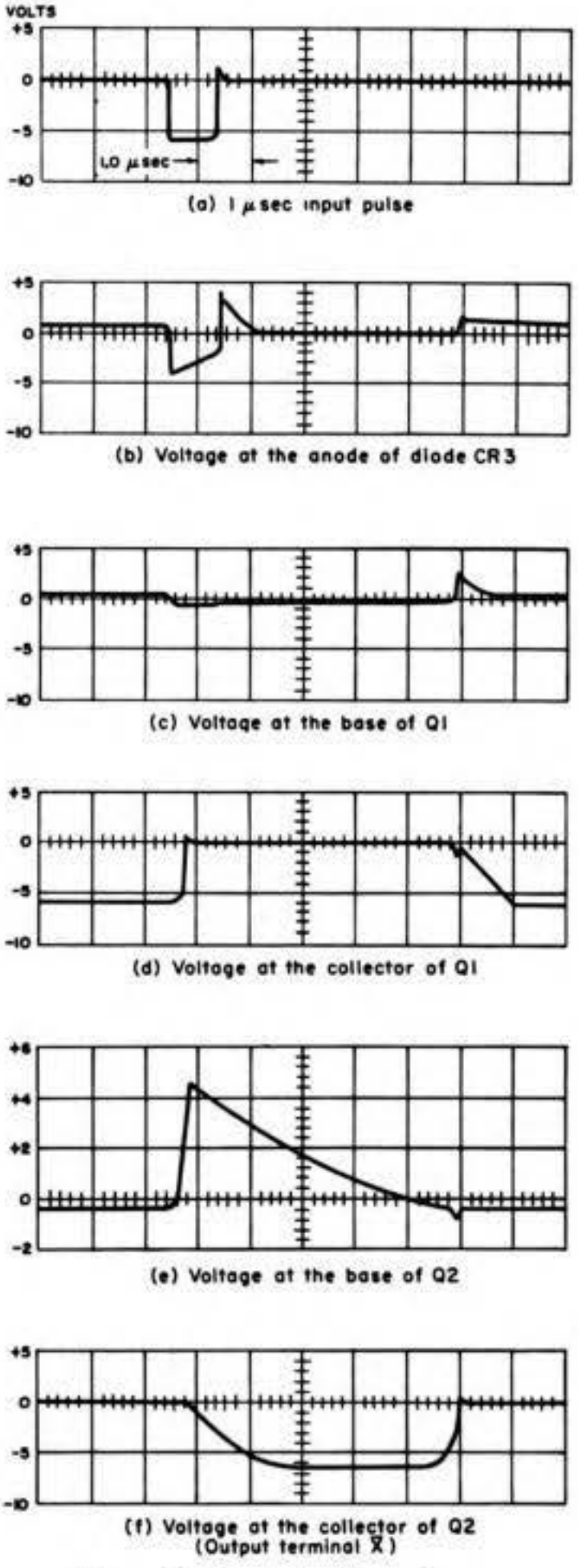


Figure 10-4.—Typical waveforms.

The delay between the initiation of the input pulse and the rise of Q1 collector voltage adds to the total time delay. At the end of the cycle, when the voltage at the base of Q1

becomes positive, Q1 begins to turn off. The turn-off time is a function of the storage characteristics of Q1, but does not affect the total time delay. The voltage at the output terminal X is the same as that at the collector of Q1 except for less than 0.1 volt difference in amplitude caused by the voltage drop in diode CR1.

(e) Voltage at the base of Q2. Initially Q2 is on, and the base voltage is clamped at approximately −0.4 volt by its base-emitter diode. When Q1 collector voltage rises, the voltage at the base of Q2 follows because of the capacitor C1 connecting the two points. The charge drawn by the base of Q2 during turn-off partly accounts for the attenuation of the peak magnitude of the waveform at the base of Q2 with respect to the change in Q1 collector voltage. Following the completion of Q1 turn-on, the voltage at the base of Q2 is derived from the charged capacitor C1 which now has its negative plate clamped to ground by the saturated transistor Q1. The base potential of Q2 decreases as C1 discharges from approximately +6 volts toward −6 volts through R3. When the potential reaches zero volts, Q2 enters the conductive region. From this point on there is a definite bend in the waveform caused by the decreasing input impedance of the base of Q2.

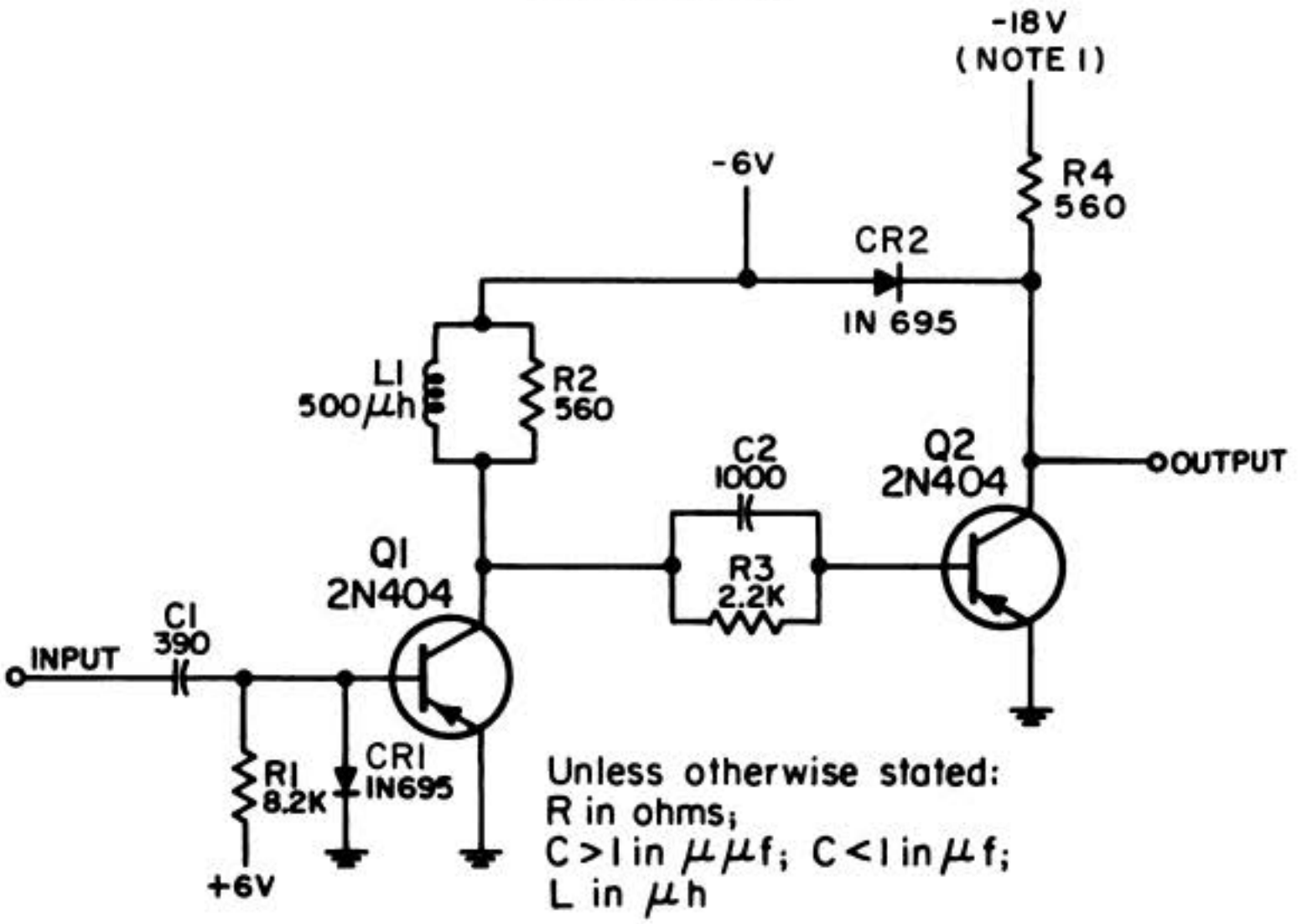
(f) Voltage at the collector of Q2. Initially Q2 is in saturation, and its collector is about 0.1 volt negative with respect to ground. The load capacitance connected to the collector (two "G" loads in this case) slows the rise of the leading edge of the waveform but does not affect the total time delay. The delay characteristics of Q2 do affect the total time delay, since it is this delay which determines how quickly Q2 will enter the conductive region once its base goes negative.

Notes

PREFERRED CIRCUIT NO. PSC 11
PULSE SHAPER

(Originally published as PC 214)

PREFERRED CIRCUIT NO. PSC 11
PULSE SHAPER



Components:

Maximum power dissipation (Note 2): R1: <10 mw; R2: 80 mw; R3: 45 mw; R4: 700 mw.
Limits (these are not tolerances; see Note 3): R1, R4: ±5%; R2, R3: ±20%. All C: ±10%
L1: ±10%.

Operating characteristics:

Temperature range: −30°C to +60°C.
Input impedance: Two "G" loads (see Section 2.3).
Input pulse characteristics:
Polarity: Negative.
Minimum amplitude: 6 volts ±10% referenced to ground.
Width at 50% amplitude: 0.8 μsec minimum.
Rise time (Note 4): ≤1.0 μsec.
Output pulse width: 0.8 to 1.4 μsec; nominal 1.0 μsec.
Switching characteristics:

Signal	Maximum no. of loads	Maximum switching time (Note 5)
Pulse	4 "F" or "G"	Turn-off time (Note 6): 0.7 μsec. Storage time: 0.5 μsec. Rise time: 0.2 μsec.
Level	8 "F" or "G"	Turn-off time: 0.9 μsec. Storage time: 0.5 μsec. Rise time: 0.4 μsec.

Maximum dc load: 15 ma at −6.2 volts ±10%.

(Specifications continued on next page)

PSC 11 PULSE SHAPER

1. APPLICATION

PSC 11 is a pulse forming and shaping circuit designed for use in computer, control, and communication equipment operating within the temperature range of −30 to +60°C.[1] It is generally used in conjunction with the monostable multivibrator, PSC 10, to form a 1-μsec pulse at the conclusion of the delay period. It is also used to reshape a pulse which has suffered deterioration by passage through a long chain of gates, or it may be used to produce a 1-μsec pulse whose leading edge coincides with the trailing edge of a positive pulse, thus delaying the output by the width of the input pulse.

2. DESIGN CONSIDERATIONS

PSC 11 consists of two grounded emitter amplifiers. The first stage, which employs an RL collector load, performs the primary shaping function and controls the pulse width. The output stage, an overdriven amplifier, serves as a buffer-power amplifier, and in addition squares off the trailing edge of the output. The output pulse width is primarily determined by the values of L1 and C1 but is also affected by the transistor characteristics, as well as the characteristics of diode CR1, the resistance of R1, and bias voltage changes. Within the temperature and component limits for which the circuit is designed, the pulse width may vary from a minimum of 0.8 μsec to a maximum of 1.4 μsec.

2.1 *Circuit Operation:* In the quiescent state, transistor Q1 is biased off by the positive voltage at the junction of the voltage divider, R1,CR1. The voltage at the collector of Q1 is approximately that of the −6-volt supply, since the drop through L1 caused by the I_{CBO} of Q1 and the base current of Q2 is negligible. Transistor Q2 is biased on by the potential applied from the −6-volt supply via the 2.2KΩ resistor, R3. C2 is charged to a potential of 6 volts.

When a negative signal is applied to the input terminal, it biases CR1 off, turns Q1 on, and causes charging current to flow into capacitor C1 via the emitter-base diode of Q1. A small current will also flow into C1 from the positive 6-volt supply through R1. The base of Q1 is heavily overdriven by the component of C1 charging current that flows through its

[1] See also Preferred Semiconductor Circuits PSC 7 through PSC 13.

Power requirements:

−18 volts ±10% at 45 ma.
−6 volts ±10% at 48 ma.
+6 volts ±10% at 1 ma.

NOTES:

1. The −18-volt supply is obtained by connecting a −12 volt source in series with the −6 volt supply (see Section 2.4).

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus the drifts caused by environmental changes or aging.

4. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude.

5. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature.

6. The turn-off time is the time required for the collector voltage to complete the first 90% of its total amplitude change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change, and includes the storage time (time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).

emitter-base diode, and the transistor is forced deeply into saturation.

The voltage at the collector of Q1 rises sharply to ground potential as the transistor is driven into saturation. Since the collector of the saturated transistor is maintained near ground potential, the −6-volt supply potential is impressed across the load which consists of L1 and R2 in parallel. If a constant voltage is to be maintained across an inductor, however, the source must be capable of supplying a constantly increasing current, since the voltage across the inductor is proportional to the rate of change of current through it. To maintain an essentially constant voltage across L1, therefore, the collector current of the transistor must increase at a constant rate. This is possible in spite of the decreasing base current, because although the base current is decreasing. it is more than sufficient to keep the transistor in saturation. Under these conditions the collector current is limited by the impedence of the load, and not by the transistor itself.

After approximately one microsecond the collector current has increased so much that the base drive is no longer sufficient to keep the transistor in saturation. If the collector current were to remain constant from this point on, the voltage across the load would drop to zero at a rate determined by the time constant L1/R2. Actually, the collector current decreases somewhat during this time, so that the trailing edge of the pulse at Q1 collector falls more rapidly than would be predicted from the time constant of the load circuit alone. When, as a result of the decreasing voltage across the load, the voltage at Q1 collector reaches approximately −6 volts, Q2 turns on. The voltage at the collector of Q1 continues to change, however, because of the discharge of the energy stored in L1.

The waveform at the collector of Q1 is not satisfactory as an output, primarily because of the negative overshoot at the trailing edge. The addition of the second stage, using Q2 as an overdriven amplifier, eliminates the overshoot, provides a low impedance output, and isolates the timing elements from the load. The base of Q2 is connected to the collector of Q1 by resistor R3 and capacitor C2, which is initially charged to a potential of 6 volts with its positive side grounded through the emitter-base diode of Q2. When Q1 is turned on by the leading edge of the input signal, the base of Q2 is driven positive causing Q2 to turn off rapidly. The time constant of the interstage network, R3, C2, is long enough to maintain the bias on the base and keep Q2 off until Q1 collector voltage again drops to approximately −6 volts. At this time the base of Q2 is driven negative, turning Q2 on and providing an additional discharge path for the remaining energy stored in L1. The overdrive caused by the discharge of L1 through the emitter-base diode of Q2 decreases Q2 delay time and improves the trailing edge of the output pulse.

2.2 *Output Pulse Width:* The output pulse width of PSC 11 may be reduced if the input signal does not meet the minimum requirements. In addition, the output pulse width may vary from 0.8 to 1.4 μsec with changes in some of the circuit parameters. In general, a decrease in Q1 collector current flow, or a decrease in the charging rate of the capacitor C1, will widen the pulse, and an increase will have the opposite effect. Several of the factors which affect the pulse width and their effect are listed in Table 11–1.

2.3 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. The input impedance and maximum load for each circuit of the set of digital logic circuits, PSC 7 through PSC 13, are arbitrarily given in terms of "F" and "G" loads to simplify the loading rules. The "F" (flip-flop) load is derived from the input impedance of the multivibrator, PSC 9; the "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PSC 7.

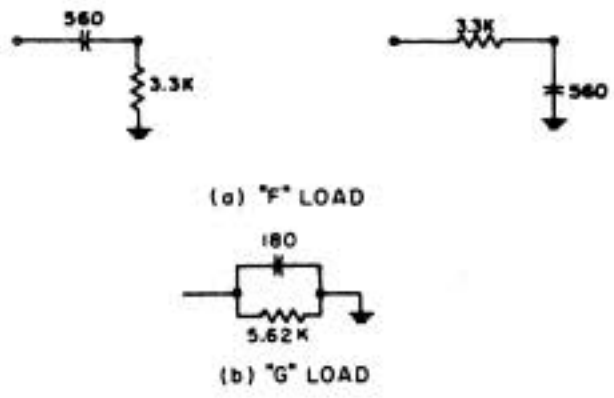


Figure 11–1.—Equivalent circuits of loads and input impedances.

TABLE 11-1.—*Factors Affecting Pulse Width*

Physical change	Effect	Reason
Increase C1	Widen pulse	Takes longer to charge C1.
Increase R1	Widen pulse	Reduces portion of C1 charging current which comes from +6-volt supply.
Decrease +6 volt potential.	Widen pulse	Reduces portion of C1 charging current which comes from bias supply.
Increase Q1 Beta	Widen pulse	Reduces base current needed to sustain given collector current flow.
Increase L1	Widen pulse	Decreases rate of increase of collector current during ON time.
Increase the storage characteristics of Q1.	Widen pulse	Widens the output pulse because it has little effect on the leading edge, but delays the trailing edge. Q1 is initially biased off. Its turn on is rapid and not significantly affected by the transistor storage characteristics. Its turn off, which initiates the trailing edge of the output pulse, is slower, however, and depends on the storage time of the transistor.
Increase the storage characteristics of Q2.	Narrow pulse	Narrows the output pulse because it delays the leading edge but has little effect on the trailing edge. The turn off of Q2, which forms the leading edge of the output pulse, is a function of the storage characteristics of the transistor. The effect of the storage characteristics on the turn on of Q2 is minimized by the large signal applied to the base to turn the transistor on.

The equivalent circuit of each of these loads is shown in Figure 11–1. The actual load impedance may vary somewhat from the equivalent circuit describing it; however, allowances were made for this in formulating the output loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

2.4 *Power Supplies.* The −18-volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6-volt supply. In this way the clamping diode current can be maintained when the transistor is biased off without causing reverse current flow in the −6-volt supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping diode current will be maintained by a current from the −18-volt supply flowing in the reverse direction through the −6-volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6-volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PSC 9.

When PSC 11 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in Section 2.4 of PSC 7.

3. PERFORMANCE

Voltage waveforms at points of interest throughout PSC 11 are illustrated in Figure 11–2, a through e, and discussed in the corresponding paragraph below. All of the traces were recorded at a sweep speed of 0.5 μsec per division. The input signal was furnished by a general purpose NOR gate, PSC 7, used as an inverter; 4 "G" loads formed the load on the output of PSC 11.

(a) Input signal: A 4 μsec pulse is used for the input signal to allow the display of the complete pulse forming and shaping cycle of PSC 11. The break in the leading edge of the waveform occurs when the emitter-base diode of Q1 starts to conduct, lowering the input impedance of PSC 11, and loading the signal source.

(b) Base voltage of Q1: Prior to the application of the input signal, the base is clamped at a slight positive voltage by the biasing cir-

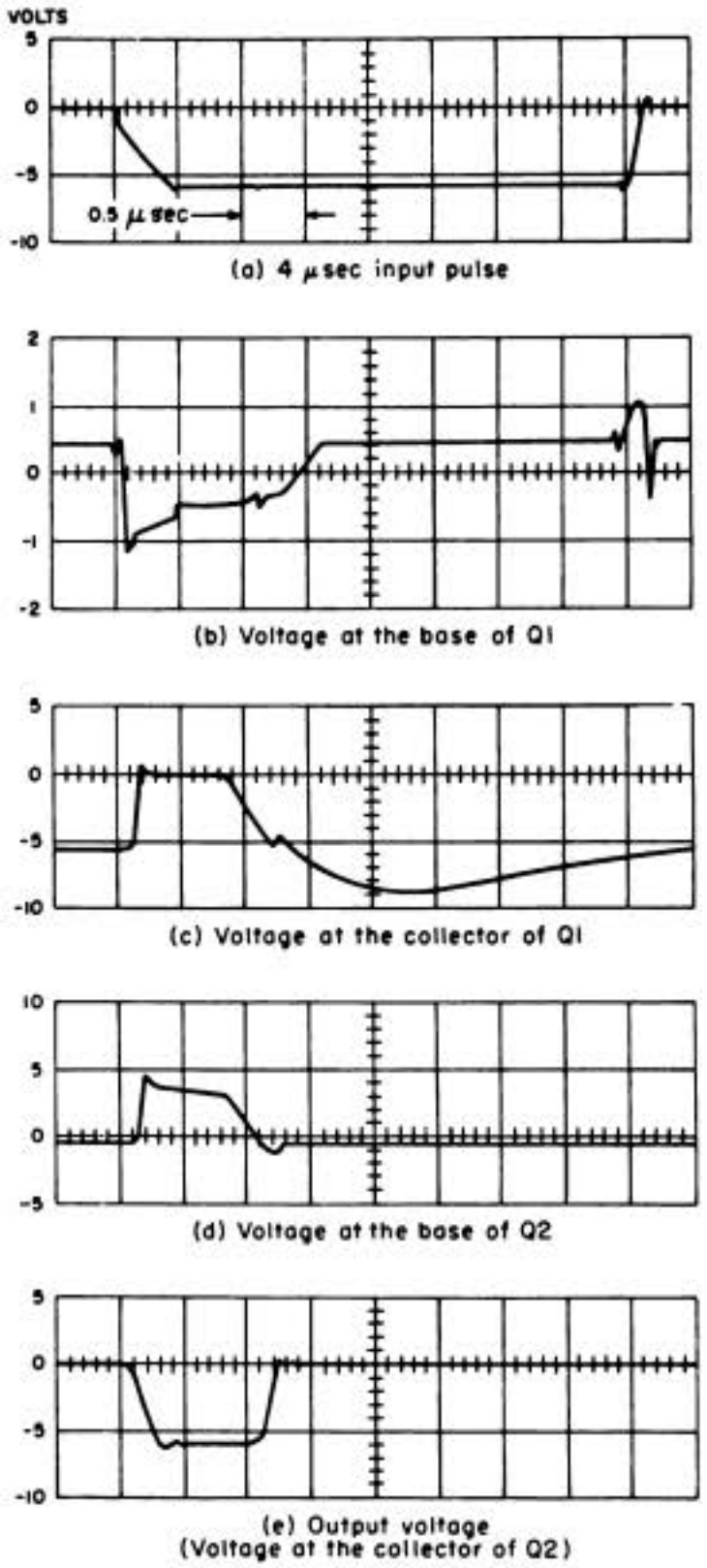


Figure 11–2.—Typical waveforms.

cuit. With the application of the trigger pulse, the base voltage falls rapidly at about the same rate as the input signal until the base-emitter diode starts to conduct. From this point on the charging of capacitor C1 gradually reduces the base voltage. When the base current is no longer sufficient to maintain the collector current, Q1 turns off, and the biasing circuit restores the base voltage to its original condition.

(c) Voltage at the collector of Q1: The heavy drive at the base of Q1 rapidly forces Q1 into saturation and produces a fast rising leading edge on the collector voltage waveform. As long as Q1 remains in saturation and the base drive is sufficient to maintain an increasing current through inductor L1, the collector voltage remains at approximately ground potential. When the transistor comes out of saturation, the collector voltage falls at a rate determined by the decreasing collector current and by the load, L1,R2. When the voltage at Q1 collector reaches about −6 volts, Q2 turns on and its base-emitter diode in series with the parallel combination of C2 and R3 furnishes an additional discharge path for the energy stored in the inductor. The discharge of this energy causes the negative voltage swing after Q1 turns off.

(d) Voltage at the base of Q2: Initially Q2 is on and its base is approximately at ground potential. Q2 base voltage tends to follow the rise in Q1 collector voltage when Q1 turns on, because the base of Q2 is connected to the collector of Q1 by resistor R3 and capacitor C2, which discharges little during the 1 μsec pulse. The extent of the discharge of C2 can be judged by the reduction in Q2 base voltage during the time that Q1 collector is grounded. During the trailing edge of the pulse at Q1 collector, the base voltage of Q2 drops to a slight negative value and the overshoot on the Q1 collector waveform is clipped by the base-emitter diode of Q2.

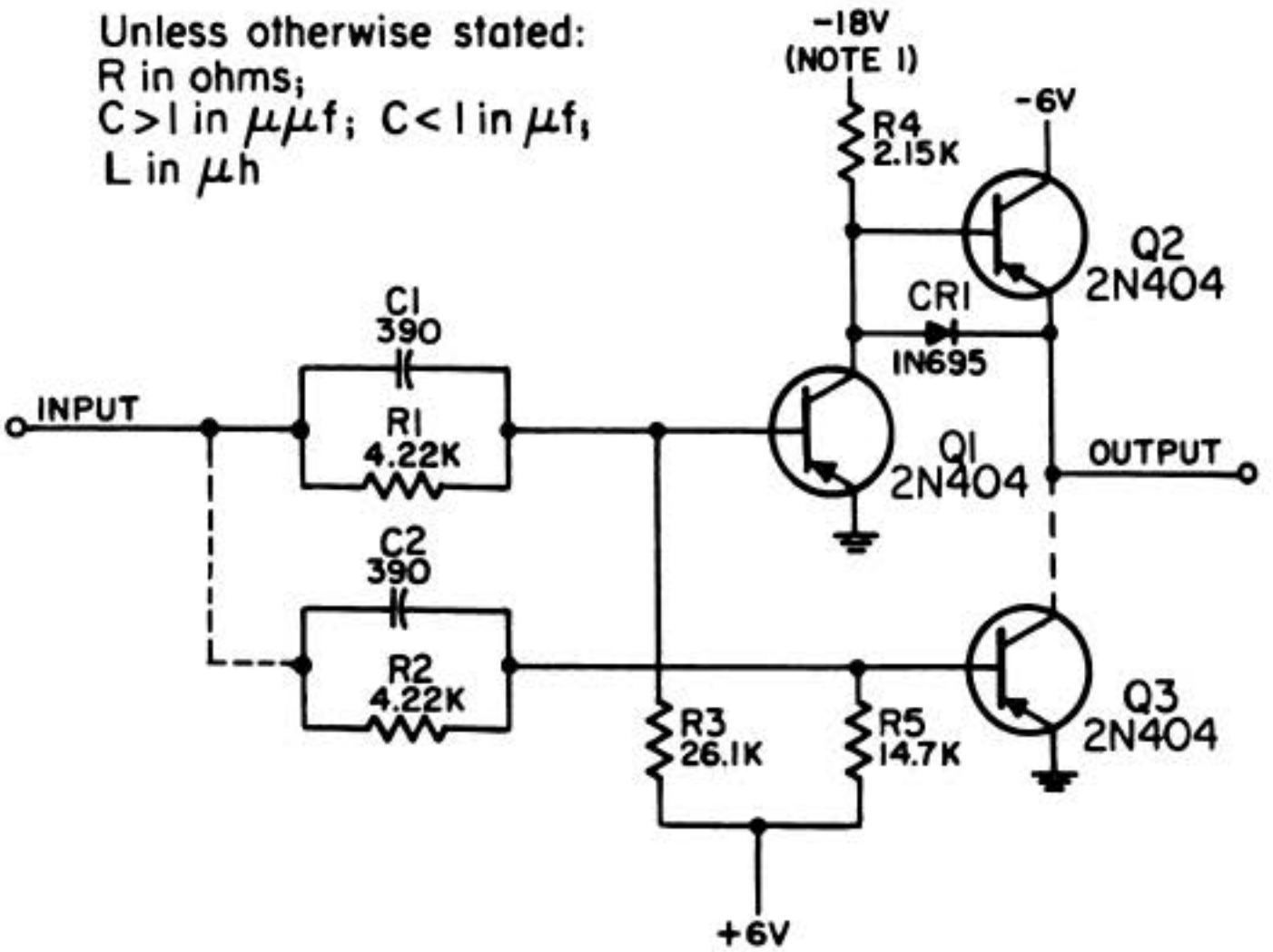
(e) Output voltage (voltage at the collector of Q2): The overshoot which appeared at the collector of Q1 is eliminated, and the speed of the trailing edge of the output waveform is improved by the action of Q2. The output pulse width is 1 μsec.

Notes

PREFERRED CIRCUIT NO. PSC 12
PULSE POWER AMPLIFIER

(Originally published as PC 215)

PREFERRED CIRCUIT NO. PSC 12
PULSE POWER AMPLIFIER



Components:

Maximum power dissipation (Note 2): R1,R2,R3,R5: <10 mw; R4: 180 mw.
Limits (these are not tolerances; see Note 3): All R: ±5%. All C: ±10%.

Operating characteristics:

Temperature range: −30°C to +60°C.
Input impedance (see Section 2.3):
For 2 transistor amplifier: 2 "G" loads.
For 3 transistor amplifier: 4 "G" loads.
Input signal characteristics:
Level (Note 4):
Logical "1": −6.2 volts ±10% at 3.1 ma.
Logical "0": −0.15 volts.
Pulse (Note 5):
Polarity: Positive or negative.
Amplitude: 6 volts ±10%.
Width at 50% amplitude: 0.8 μsec minimum; 5 μsec maximum.
Rise time (Note 6): ≤0.2 μsec.

(Specifications continued on next page)

Operating characteristics—*Continued*

Switching characteristics for two- or three-transistor circuit (Note 7):

Input signal	Output signal
Level change from 0 v to −6 v with rise time of 0.4 μsec.	Level change from −6 v to 0 v. Turn-on time (Note 8): 0.4 μsec max. Delay time: 0.2 μsec max. Rise time: 0.2 μsec max.
Level change from −6 v to 0 v with rise time of 0.4 μsec.	Level change from 0 v to −6 v. Turn-off time (Note 9): 0.7 μsec max. Storage time: 0.2 μsec max. Rise time: 0.5 μsec max.
Negative-going pulse with rise time of 0.2 μsec.	Positive-going pulse Turn-on time: 0.35 μsec max. Delay time: 0.15 μsec max. Rise time: 0.2 μsec max.
Positive-going pulse with rise time of 0.2 μsec.	Negative-going pulse Turn-off time: 0.35 μsec max. Storage time: 0.15 μsec max. Rise time: 0.2 μsec max.

Maximum load (see Section 2.3).

Circuit	Type of output			
	Direct current	Level	Positive pulse	Negative pulse
2-transistor amplifier	44 ma at −6.2 v ±10% 1 ma at −0.15 v	12 loads "F" or "G"	12 loads "F" or "G"	12 loads "F" or "G"
3-transistor amplifier	44 ma at −6.2 v ±10% 1 ma at −0.15 v	40 loads "F" or "G"	40 loads "F" or "G"	12 loads "F" or "G"

Power requirements:

Voltage	Maximum current	
	2-transistor circuit	3-transistor circuit
−18 volts ±10%	10 ma	10 ma
−6 volts ±10% (note 10)	50 ma	50 ma
+6 volts ±10%	0.9 ma	0.9 ma

(For notes, see bottom of next page)

PSC 12 PULSE POWER AMPLIFIER

1. APPLICATION

PSC 12 is a pulse power amplifier designed for use as an auxiliary driving element when the load to be driven by PSC 7, 8, 9, 10, or 11 exceeds the specified maximum for that circuit. PSC 12 has an input impedance equal to 2 "G" loads, but is capable of driving 12 "F" or "G" loads. The addition of two resistors, R2 and R3, a capacitor, C2, and a transistor, Q3, increases the input impedance of PSC 12 to 4 "G" loads, but allows the circuit to drive 40 "F" or "G" loads with a positive-going output signal.

2. DESIGN CONSIDERATIONS

The maximum number of loads that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. The rise time of the output signal is in turn determined by the rapidity with which the load capacitance can be charged or discharged, depending on the polarity of the desired output signal. PSC 12 is basically a two-transistor circuit consisting of a grounded-emitter amplifier driving an emitter follower. A second grounded-emitter amplifier stage can be added in parallel with the first to improve the performance of the circuit for positive-going output signals.

2.1 *Circuit Configuration:* The grounded-emitter amplifier, Q1, serves as a low-impedance discharge path for the capacitive portion of the load when the output signal is positive going, and emitter follower, Q2, is a low-impedance discharge path for this same capacitance when the output signal is negative going. Resistor R3, together with the positive 6-volt supply, provides the base of Q1 with a positive bias current which prevents I_{CBO} multiplication when

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NOTES:

1. The —18-volt supply is obtained by connecting a —12-volt source in series with the —6-volt supply. (See section 2.4.)
2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.
3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.
4. The minimum duration of a level is 5 μsec.
5. Positive pulses are referenced to —6.2 volts ±10%; negative pulses are referenced to ground (actually about —0.15 volt).
6. Rise time is used in the usual pulse sense to mean the time required for the leading edge of the waveform to change from 10% to 90% of its maximum amplitude.
7. Maximum switching times were obtained by operating the circuit with the worst combination of limit transistors, components, supply voltages, and temperature. The load in each case was maximum for that type of operation.
8. The turn-on time is the time required for the collector voltage to complete the first 90% of its total change when the transistor is turned on. It is measured from the instant that the signal applied to the transistor to turn it on completes 10% of its amplitude change and includes the delay time (the time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).
9. The turn-off time is the time required for the collector voltage to complete the first 90% of its total change when the transistor is turned off. It is measured from the instant that the signal applied to the transistor to turn it off completes 10% of its amplitude change and includes the storage time (time required for the first 10% change in collector voltage) and the rise time (the time required for the voltage change from 10% to 90%).
10. The current specified is maximum for the circuit; actual current requirements vary with the load. The —6-volt supply must furnish any external dc load plus 1.2 ma for each RC load used.

Q1 is off. When Q1 is on, the low impedance path it provides between the base of Q2 and ground keeps the multiplied Q2 collector current in the vicinity of I_{CES} in magnitude.

When Q1 is off, the rise in its collector voltage is limited to approximately −6 volts by the clamping action of the internal base-collector diode of Q2. Q2 thus replaces the diodes used for clamping in the other circuits of the digital set, standardizing output amplitude and allowing faster rise time for negative-going signals than could be achieved without such clamping.

In the 3-transistor circuit, Q3 furnishes an additional discharge path for the load capacitance when the signal is positive-going. It carries more of the discharge current than does Q1 because Q1 has the added impedance of diode CR1 in series with it, while Q3 does not; Q3 therefore tends to become hotter than Q1 and requires more positive bias current to prevent I_{CBO} multiplication.

2.2 *Circuit Operation:* PSC 12 operates as an inverting power amplifier for either pulses or levels. When a negative 6-volt potential is applied to the input, Q1 is turned on in saturation, and the positive-going potential at its collector turns Q2 off. During the first few tenths of a volt change in Q1 collector voltage, diode CR1 remains back biased, keeping the collector of Q1 disconnected from the load and allowing fast turn-off of Q2. For the remainder of the discharge of the load capacitance the diode is in series with Q1, and the voltage across the load drops to ground potential at a rate determined by the impedance of Q1 and CR1 in series and the capacitive component of the load.

When the input terminal is brought to ground potential, Q1 is turned off, and the output voltage falls toward −6 volts at a rate determined by the impedance of the saturated transistor Q2 and the capacitive component of the load. Diode CR1 disconnects the collector of Q1 from the load, thus allowing the collector of Q1 to rise rapidly and cause a fast turn-on of Q2.

The third transistor stage, Q3 and its associated components, when added to PSC 12 operates in parallel with Q1. Since Q3 does not have a diode in series with it, it reduces the impedance of the discharge path by more than half and therefore increases the circuit capabilities by a greater percentage than it decreases the input impedance. For negative-going outputs the performance is unaffected; when the output is positive-going, however, the rise time is decreased because of the decrease in output impedance under these conditions.

2.3 *Input Impedances and Loads:* The maximum load that can be driven by any of the digital circuits is determined by the effect of the load on the rise time of the output signal. To simplify the loading rules, the input impedance and maximum load for each circuit of the set of digital logic circuits, PSC 7 through PSC 13, are arbitrarily given in terms of "F" and "G" loads. The "F" (flip-flop) load is derived from the input impedance of the bistable multivibrator, PSC 9. The "G" (gate) load is equivalent to the input impedance of the general purpose NOR gate, PSC 7.

The equivalent circuit of each of these loads is shown in Figure 12–1. The actual load

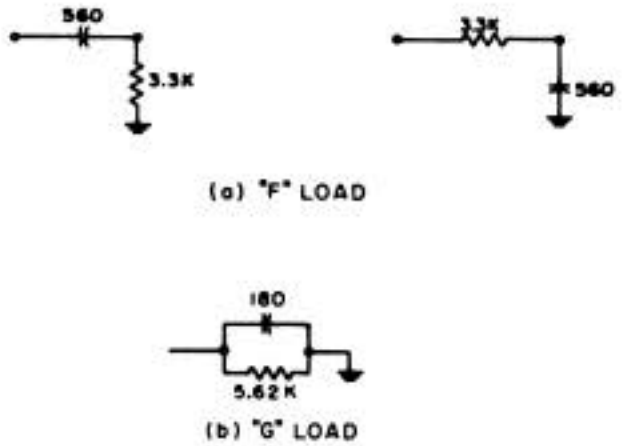


Figure 12–1.—Equivalent circuits of loads and input impedances.

impedance may vary somewhat from the equivalent circuit describing it. Allowances were made for this, however, in formulating the output loading rules. The two forms of the "F" load represent the two methods of coupling into the flip-flop. Because the transistor loads the junction of the resistor and capacitor in the actual input circuit of the flip-flop, the "F" load is a less accurate approximation than the "G" load.

2.4 *Power Supplies:* The −18-volt supply should be obtained by connecting the positive side of a 12-volt floating source to the −6-volt supply. In this way Q1 collector voltage can be clamped when the transistor is biased off without causing reverse current flow in the −6-volt

supply. If the −18 volts is supplied from a separate source and the transistor is off, the clamping current will be maintained by a current from the −18-volt supply flowing in the reverse direction through the −6-volt supply, because the two supplies will be connected in series opposition.

Supply voltages should not deviate more than 10% from the nominal values of 6 volts, −6 volts, and −18 volts. The noise level on the −6 volt supply must not exceed 1.7 volts in peak magnitude to prevent spurious triggering of loads such as bistable multivibrator PSC 9.

When PSC 12 is used in a system, additional filtering of power leads is required to keep external and system induced noise to tolerable levels. This problem is discussed at length in section 2.4 of PSC 7.

3. PERFORMANCE

Typical operating characteristics of PSC 12 when used as a three-transistor circuit are shown in Figures 12–2 and 12–3. The effect of changing from a three- to a two-transistor circuit is illustrated in Figures 12–4 and 12–5. This change was accomplished by disconnecting R2 and C2 from the input terminal, thereby effectively removing Q3 from the circuit. In all of the figures the waveforms were obtained at a sweep speed of 0.2 μsec per division.

Figure 12–2 illustrates the effect of loading on the output of PSC 12 operating with a negative input. Trace (a) shows the input signal, which remains relatively unaffected by the changes in output loading. The change in slope of the leading edge (trace (a)) occurs when transistors Q1 and Q3 go into saturation and sharply increase the load on the input source. Trace (b) shows the output voltage under light-loading conditions. As shown in trace (c), an increase to medium-loading conditions results in a reduced slope of both leading and trailing edges of the output signal. Trace (d) shows that under maximum loading conditions the leading edge rise time remains within the 0.2 μsec specification.

Figure 12–3 illustrates the effect of loading on the output of PSC 12 when the input signal is a positive pulse. Here, the input signal was furnished by PSC 7 used as an inverter. The effect of the 4 "G" input impedance of PSC 12

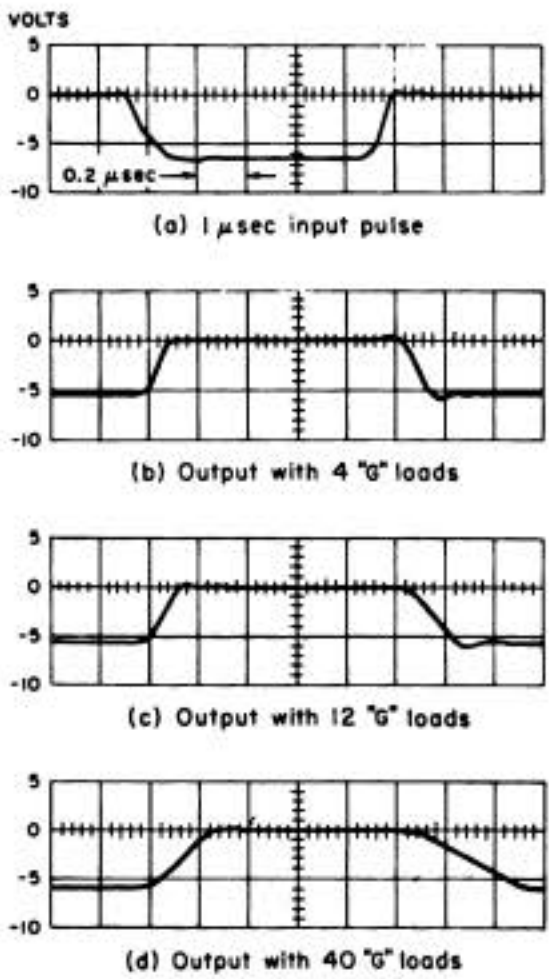


Figure 12–2.—Typical waveforms for three-transistor circuit with negative input.

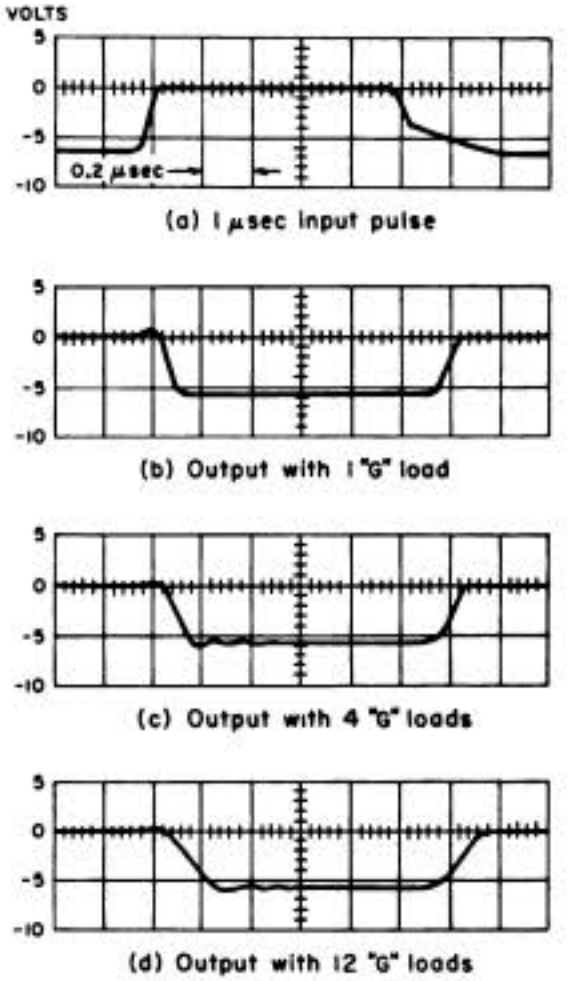
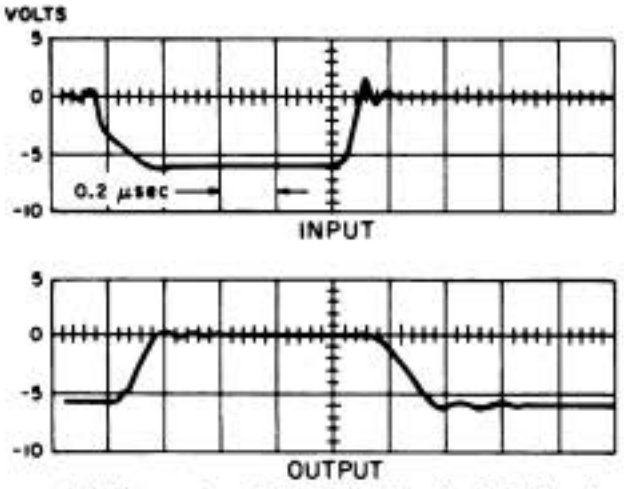
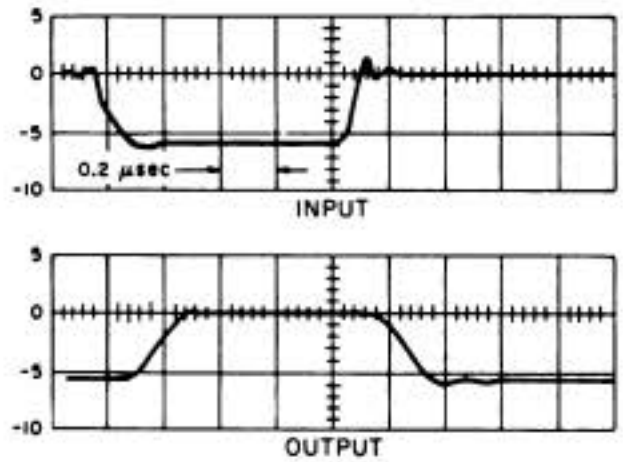


Figure 12–3.—Typical waveforms for three-transistor circuit with positive input.

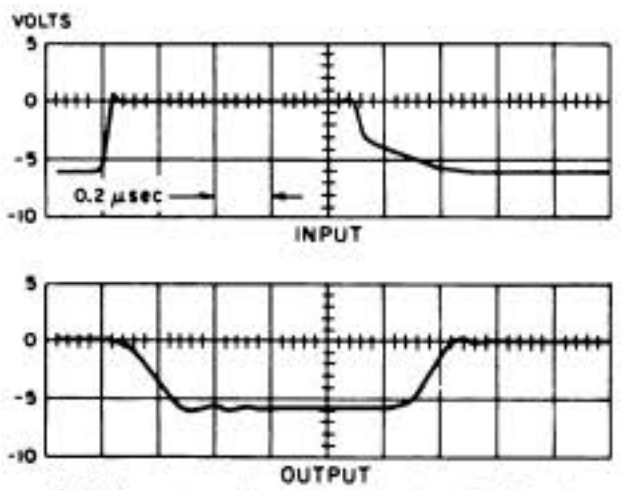


(a) Three-transistor circuit with 12 "G" loads

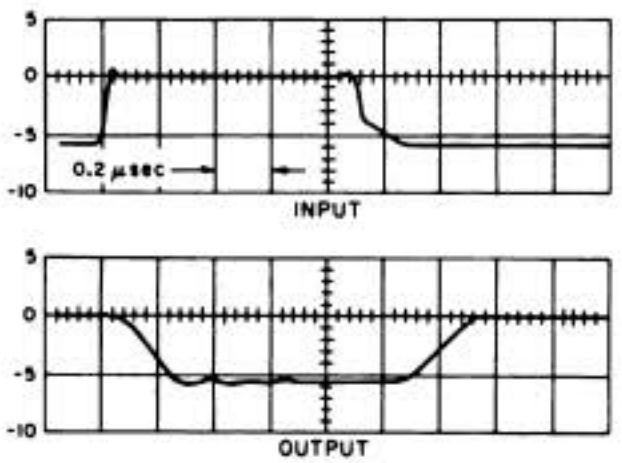


(a) Two-transistor circuit with 12 "G" loads

Figure 12–4.—Comparison of the performance of the two- and three-transistor circuits for negative input signals.



(a) Three-transistor circuit with 12 "G" loads



(b) Two-transistor circuit with 12 "G" loads

Figure 12–5.—Comparison of the performance of the two- and three-transistor circuits for positive input signals.

on the gate is evident from the sharp break in the trailing edge slope in trace (a). Traces (b), (c), and (d) once again show the output waveform for light, medium, and maximum loading. Trace (d) shows that 12 "G" loads can be driven without the leading edge rise time of the output waveform exceeding the 0.2 μsec limit.

In Figure 12–4 are shown the input and output waveforms for both the two- and three-transistor versions of PSC 12. The 12 "G" load is the maximum that can be driven by the two-transistor version. The advantage of the two-transistor version is seen in the faster input rise time permitted by the decreased loading on the driving source. However, the slope of the leading edge of the output waveform is significantly reduced when the third transistor is rendered inactive, because the leading edge of the output waveform is formed by the discharge of the load capacitance through transistors Q1 and Q3 which have been turned on by the negative input pulse. Transistor Q3 is the more effective discharge path because it is not in series with a diode as is Q1, and Q3 is the transistor that has been removed in the two-transistor version.

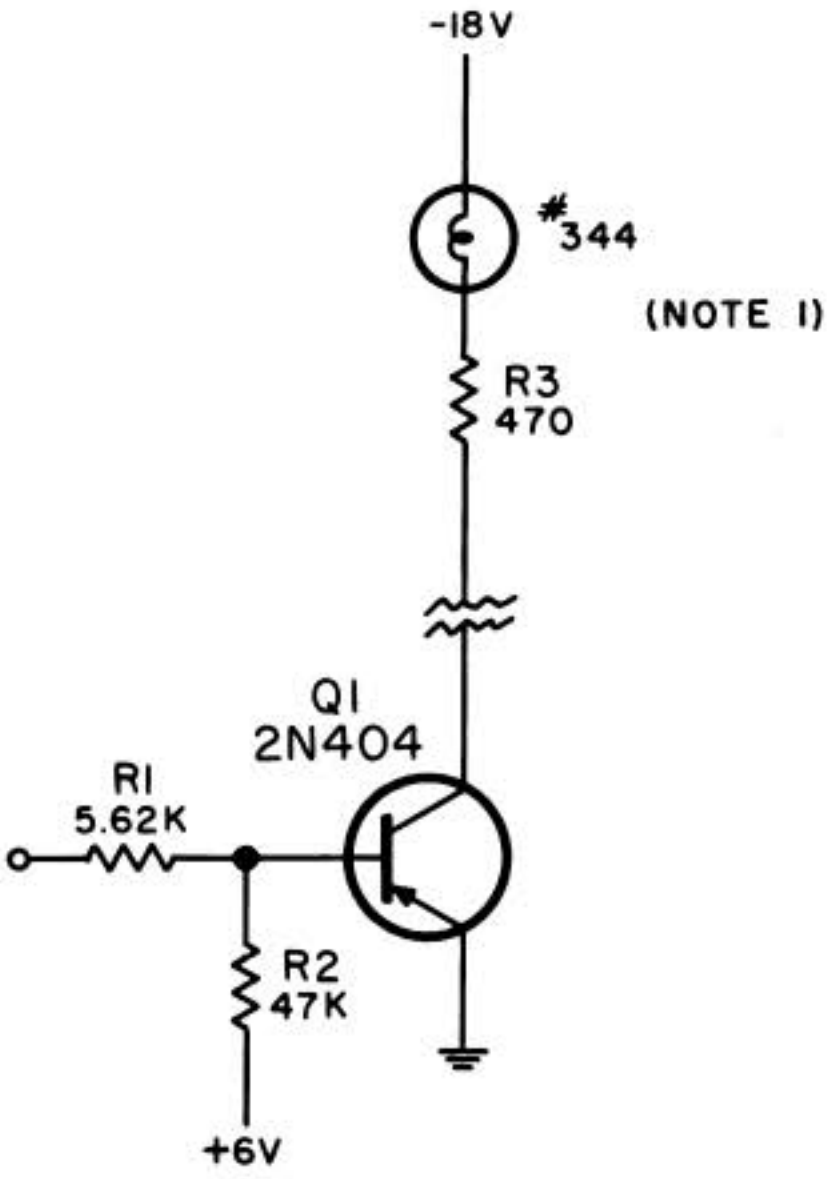
Figure 12–5 is a repetition of the measurements illustrated in Figure 12–4, but the input pulse is now positive rather than negative. Note that the slope of the leading edge of the output signal is unaffected by the presence or absence of Q3 in the circuit. This is to be expected, since during the leading edge of a negative-going output signal, the load capacity is being charged by Q2, while Q1 and Q3 are both cut off. Since Q2 is not affected by the removal of Q3, the leading edge rise time of negative-going output signals is not affected by the presence or absence of Q3.

Notes

PREFERRED CIRCUIT NO. PSC 13
INDICATOR

(Originally published as PC 216)

PREFERRED CIRCUIT NO. PSC 13
INDICATOR



Unless otherwise stated: R in ohms

Components:

Maximum power dissipation (Note 2): R1: 8 mw; R2: 5 mw; R3: 180 mw.

Limits (these are not tolerances; see Note 3): R1, R2: ±5%; R3: ±20%.

Operating characteristics:

Temperature range: —54°C to +71°C.

Input impedance: ½ "F" load (Note 4).

Input signal:

	Indicator action
Logical "0" (ground potential)	No light
Logical "1" (−6.2 volts ±10% at 1.2 ma)	Lamp lights

Power requirements:

−18 volts ±10% at 15 ma.

+6 volts ±10% at 0.16 ma.

(For Notes, see bottom of next page)

PSC 13 INDICATOR

1. APPLICATION

PSC 13 is used as an indicator in the compatible set of digital logic circuits.[1] The circuit is designed for a nominal drive of 15 ma at 10 volts to insure conservative operation of the type 344 bulb under limit conditions. It can be used to drive electromechanical devices which operate within the same power limits, or to drive devices with 6-volt ratings, in which case a −6-volt source is used for the collector supply.

[1] See also Preferred Semiconductor Circuits PSC 7 through PSC 12.

2. DESIGN CONSIDERATIONS

PSC 13 is a common-emitter amplifier designed to drive a type 344 light bulb which has a rating of 18 ma at 12 volts. A positive current bias derived from the +6 volt supply via resistor R2 prevents I_{CBO} current amplification at temperatures up to 71° C. Resistor R1 is chosen to insure saturation with low beta transistors at temperatures of 0° C and above. At lower temperatures Q1 may not saturate, but the added dissipation in Q1 is no problem at low temperatures. Further heating in this instance will increase beta and therefore lead to saturation and decreased dissipation.

Notes:

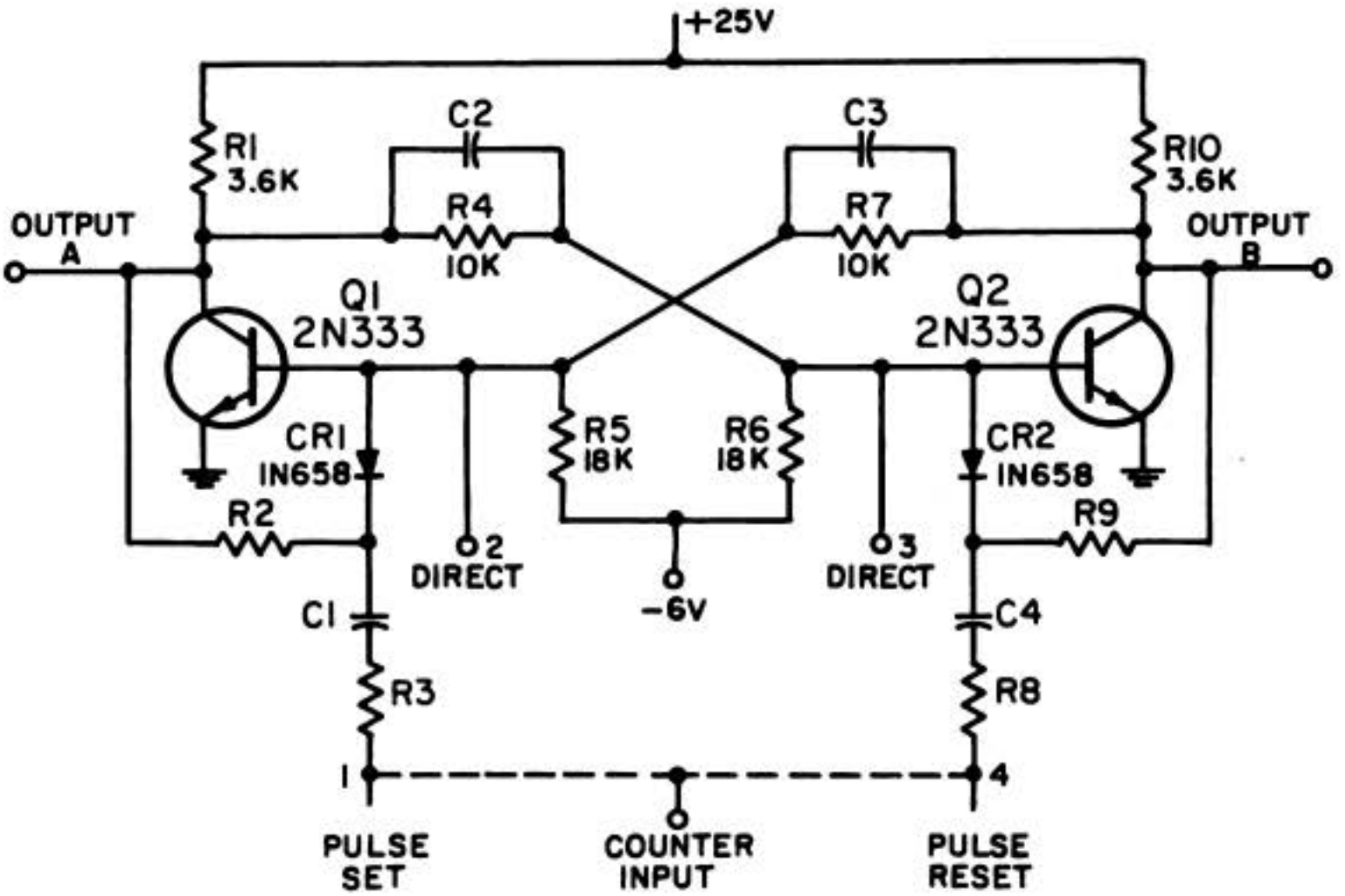
1. The indicator and the amplifier may be in different locations.
2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.
3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.
4. The "F" load is the input impedance of the flip-flop circuit, PSC 9.

Notes

PREFERRED CIRCUIT NO. PSC 14
SATURATING BISTABLE MULTIVIBRATOR

(Originally published as PC 250)

PREFERRED CIRCUIT NO. PSC 14
SATURATING BISTABLE MULTIVIBRATOR



Unless otherwise stated: R in ohms; C in pf

Components:

Q1, Q2: See Note 1. For component values not specified on the schematic diagram, see Table 14–1, page 14–4.

Maximum power dissipation (Note 2): R1, R10: 250 mw; R2, R3, R4, R5, R6, R7, R8, R9. <50 mw.

Limits (these are not tolerances; see Note 3): R1, R4, R5, R6, R7, R10: ±5%; R2, R3, R8, R9: ±10%. All C: ±10%.

Operating characteristics:

Temperature range: −65°C to +125°C with temperature stable resistors and capacitors.

Input levels and minimum durations:

Counter or pulse: 7 volts negative; 3-μsec duration at —7-volt level.

Direct: +1 ma for 10 μsec, or —4 ma for 5 μsec.

Maximum pulse repetition frqeuency: 40 kc.

Delay time: 2 to 5 μsec.

Output levels, both A and B: 18±3 volts for 10% supply voltage variation.

Output impedance:

Positive-going waveform: 2.5KΩ

Negative-going waveform: Less than 500 Ω.

Power requirements: +25 volts, ±10% at 10 ma; —6 volts ±10% at 0.7 ma.

(For Notes, see bottom of next page)

PSC 14 SATURATING BISTABLE MULTIVIBRATOR

1. APPLICATION

PSC 14 is a slow-speed, stable, saturating multivibrator for use as a counter, shift register, gate, or switch. It provides transitional stages between electromechanical readout and higher speed nonsaturating bistable counters. The design was optimized to accept wide tolerance transistors and should be employed when selection is to be avoided.

2. DESIGN CONSIDERATIONS

The circuit is triggered by turning off the on transistor and allowing the resulting transient to regenerate, holding the circuit in the new state. In the rest condition the dc voltages applied to the diode terminals are such that the diode associated with the off transistor is biased off by approximately 20 volts. The diode associated with the on transistor is biased off by less than the collector saturation voltage of the on transistor, approximately one-half volt. A negative pulse with the specified amplitude will, when applied to the counter input, be steered to the base of the on transistor and cause a change of state. A positive pulse will not be passed by the steering diodes.

The input circuit must furnish to the base circuit of the on transistor a negative pulse of sufficient voltage and time duration to drive the transistor out of saturation. The required voltage and width of the applied pulse are related. Experimental measurements show that at a given impedance level the product of the two is very nearly constant for the minimum trigger level.

Three sets of part values for input connections 1 and 4 are listed in Table 14–1. When PSC 14 is driven from a low-impedance pulse source, the component values and performance specifications of Adaption 1 apply. When PSC 14 is driven from a higher impedance source, such as a non-saturating bistable multivibrator or a time delay multivibrator, the component values and performance specifications of Adaption 2 apply. When successive stages of PSC 14 are cascaded, the first stage is either Adaption 1 or Adaption 2, and the successive stages should have the component values specified for Adaption 3. Instead of buffer amplifiers being used to prevent reaction on prior stages, various values are used for the resistors and capacitors listed without sacrifice of ultraconservative performance.

2.1 *Circuit Operation:* The bias circuit permits one transistor to conduct in saturation while the other transistor is held in the off condition. The dc circuit elements have been chosen so that transistors with low limit values of dc current gain, h_{FE}, will saturate. Higher gain transistors will consequently be driven further into saturation.

In the design of this circuit care was taken to use the extreme lower limit value of h_{FE}. This value has been found to be approximately 7 for the 2N333.

The output voltage swing is expressed as

$$\Delta V_2 \approx V_{CC}\frac{\mathrm{R7}}{\mathrm{R7}+\mathrm{R10}} - V_{CE(sat)2},$$

NOTES:

1. The 2N333 has been dropped from the Preferred and Guidance List of Transistors (MIL–STD–701) since this circuit was first published in 1959. The 2N335, which appears on the current Preferred List, is similar to the 2N333 in all important respects except beta. If the 2N335 is used in PSC 14, the 70% higher beta will result in the "on" transistor being driven further into saturation with a resulting increase in transition time. This can be offset by increasing the trigger amplitude.

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

where V_{CC}=collector supply voltage and $V_{CE(sat)2}$=collector to emitter saturation voltage. From this relationship it is readily determined that the output amplitude depends on the transistor saturation resistance. This is one of the most important advantages of saturating type switching circuits.

2.2 *Impedance:* Some changes in the circuit impedance can be made. Only the relative values of the circuit resistances are of importance, except that for a fixed supply voltage the value of R5 and R6 is limited by the I_{CBO} and the $V_{CE(sat)}$ characteristics of the transistor, rather than by the other circuit elements. It is recommended that R5 and R6 not exceed 20,000 ohms; larger values of the other resistances may be chosen.

The resistor values should not be scaled down beyond that point where either the collector current ratings or the power dissipation of the transistors is exceeded. The resistors in PSC 14 may be reduced to approximately one-half of the values given without exceeding the ratings of the 2N333 up to a case temperature of 125°C. However, input circuit Adaption 2 is not recommended for use with resistance values lower than those given. Note that the saturation resistance of the transistor is not affected by this scaling down, so that the output impedance for a negative-going signal does not change.

2.3 *Transistor Type*: The transistor characteristics of greatest importance to the circuit operation are: (1) collector voltage, power, and current ratings; (2) dc and high-frequency current gain; (3) base-to-emitter voltage required to sustain saturated conduction; (4) collector-to-emitter voltage during saturated conduction; and (5) maximum I_{CBO} to be encountered.

The transistor power dissipation is dependent on the saturation collector voltage, as well as on the saturation collector current. The power loss in the transistor is particularly low if transistors having a low value of saturation resistance are used.

3. PERFORMANCE

3.1 *Pulse Input:* The input circuit may be used for either set-reset or counter operation.

The characteristics required of the input signal are dependent on the values of R2, R9, R3, R8, C1, and C4. Values of these components have been chosen to provide operation from three general types of input, as outlined below and in Table 14–1.

(a) Adaption 1 will operate from pulse inputs occurring at frequencies up to 40 kc. The highest frequency response is obtained

TABLE 14–1.—*Component values and performance*

Adaption No.	Signal source	Max. source imped.	R2 R9	R3 R8	C2 C3	C1 C4	Input imped.	Input		Output		Number of set-reset loads	Minimum circuit recovery time
								Max. rep. rate	Trigger voltage range	Rise time (tr)	Fall time (tf)		
		ohms	ohms	ohms	μμf	μμf	ohms	kc	volts	μsec	μsec		μsec
1	Operation from low impedance pulse source	[1] 500	2.2K	[1] 500	1200	1500	1K	[2] 40	3–5	15	2.5	0	[2] 20
								[2] 40	3–5	25	3.0	2	[2] 25
								25	7–25	40	5.0	5	40
								12.5	7–25	80	7.5	10	80
2	Operation from non-saturating multivibrator or from either output of time delay multivibrator	[2] 1K	5.6K	[2] 1K	680	1000	1.5K	20	7–25	15	1.5	0	50
								20		25	2.0	2	50
								20		40	3.0	5	50
								12.5		80	5.0	10	80
3	Cascaded operation of identical stages or from either of above adaptions	500	5.6K	2.2K	680	560	3K	40	14–25	15	1.0	0	25
								40		25	1.5	2	25
								25		40	3.0	5	40
								12.5		80	7.0	10	80

[1] Total of source and isolating resistance is 500 ohms, ±10%.
[2] Total of source and isolating resistance is 1000 ohms, ±10%.
[3] With input pulse width of 3–5 μsec duration.

when the pulse width of the negative-going input signal is 3 to 5 μsec. Pulse widths less than 3 μsec do not provide reliable operation, while pulses wider than 5 μsec do not allow the input circuit sufficient recovery time at 40 kc.

Generally, the duration of the more positive portion of the input signal should be a minimum of 16 μsec. For this circuit, the specified value of R3, as well as that of R8, is the sum of the source resistance and the physical isolating resistance.

(b) Signal sources for driving Adaption 2 can be a non-saturating flip-flop or either output of a time delay multivibrator. In this operation, only two set-reset (or one counter connection) inputs per source are recommended. A typical recovery time of the input circuit is approximately 50 μsec.

(c) Adaption 3 is intended for cascaded operation. Signal sources for driving Adaption 3 can be either Adaption 1, 2, or 3. The recovery time of the input circuit is approximately 20 μsec.

The minimum input required for reliable triggering of the three adaptions is plotted in Figure 14–1 as a voltage of a given amplitude and rise time. The curves for the three adaptions show that for rise times below a certain value, dependent on the circuit, each circuit requires a minimum amplitude for triggering. The minimum duration of the applied trigger pulse, or the rest time after a negative-going ramp is applied, should not be less than 3 μsec, although shorter pulses of greater amplitude will cause triggering.

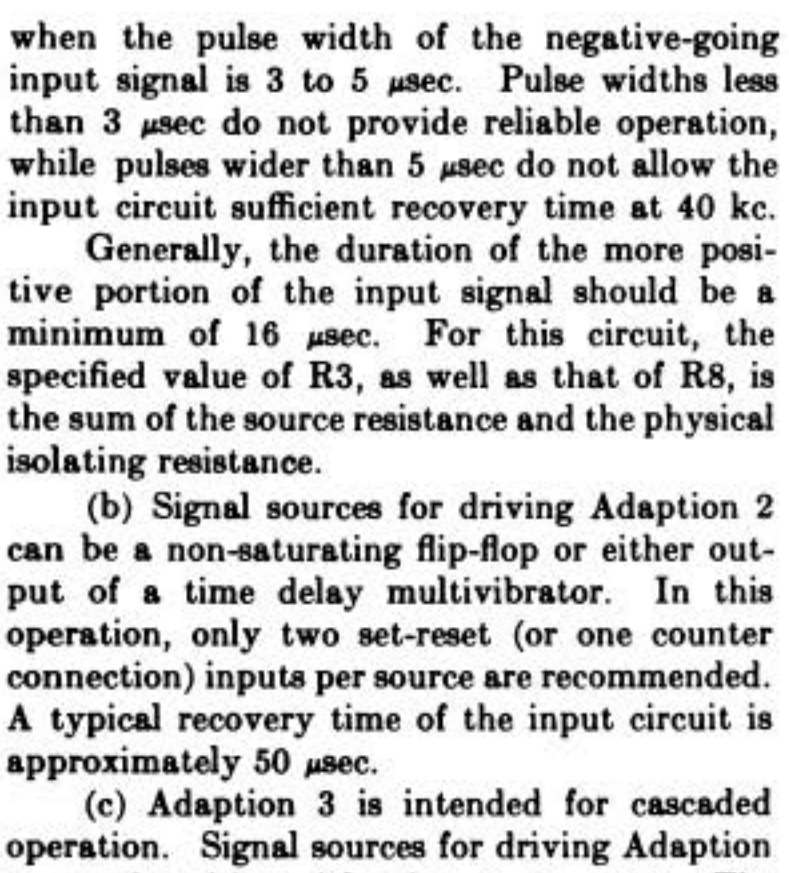


Figure 14–1.—Amplitude required for triggering vs. rise time.

3.2 *Direct Input:* The direct input can be used for reset of the transistor by applying to the base a negative voltage source that will cause a current of 4 ma to ground for 5 μsec. Alternatively, a positive pulse from a source that will cause a current of 1 ma for 10 μsec may be used. The positive voltage resets the opposite transitor to the "off" condition.

The direct connection can also be used for the insertion of blocking pulses from a subsequent counter stage to provide other than

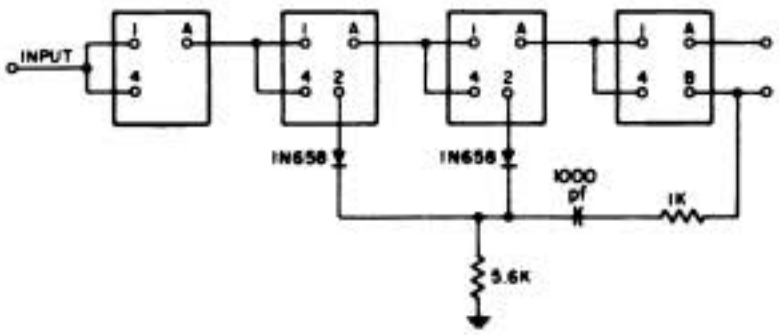


Figure 14–2.—Four stages of PSC 14 connected for operation as a decade counter.

binary counting operation, as illustrated in Figure 14–2.

3.3 *Output:* The two outputs are complementary voltages of either 1 or 19 volts. The maximum circuit switching time is 2 to 5 μsec.

Figure 14–3 shows the output waveform. The irregularity on the more positive portion of the waveform is caused by the recovery of the input circuit from a positive-going input. Usually the spike is absorbed in the rise time of Adaption 1. In Adaptions 2 and 3 the height of the spike does not exceed 2 volts.

The rise and fall times of the outputs, which are dependent on the loading, are tabulated in Table 14–1 for various combinations.

3.4 *Cascaded Operation:* Stages may be directly cascaded by connecting the inputs to the output of a previous stage. The number of inputs that can be connected depends on the

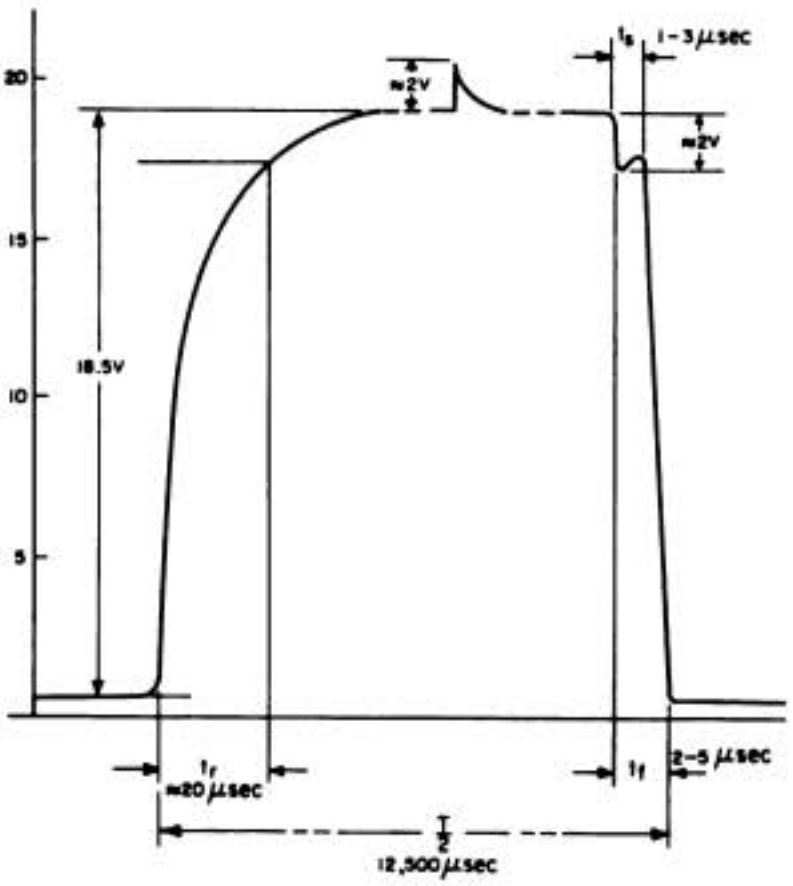


Figure 14–3.—Output waveform.

input circuit used and the repetition rate desired.

The fundamental limit on the degree of loading permissible is the deterioration of the output fall time under load to the point that triggering voltages consistent with Figure 14–1 are not obtained. The limit imposed by this consideration is 10 set-reset loads, or 5 counter stages, per either or both outputs. The speed-up capacitor C2 or C3 connected to the collector of the loaded side of the flip-flop should be increased by about 200 pf for each set-reset input connected to the output.

Another consideration when the stages are cascaded is the deterioration of the output rise time under load. First, a deteriorated output rise time may not drive the opposite transistor into saturation under some conditions; second, the time required for the output voltage to increase to its full "off" value exceeds the input pulse duration.

The increase in rise time restricts the upper limit on the circuit frequency response, as shown in Table 14–1. The loads are always assumed to be Adaption 3.

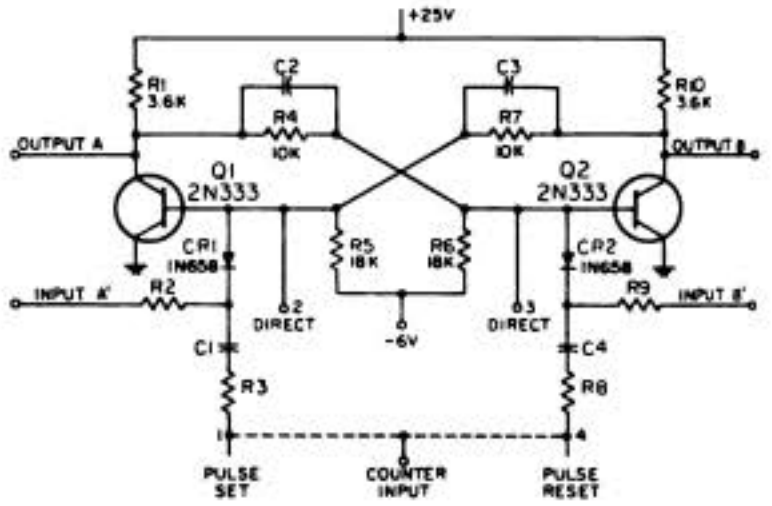


Figure 14–4.—Modification of PSC 14 for use in shift registers.

A method of connecting four flip-flop stages for decade counter operation is shown in Figure 14–2. This circuit has an asymmetrical output at terminal A of the fourth stage, a positive pulse of 20% duty cycle. The outputs have the same general characteristics as the binary circuit.

The saturating bistable multivibrator may be modified as shown in Figure 14–4 to allow its use in a shift register. One method of interconnection is shown in figure 14–5.

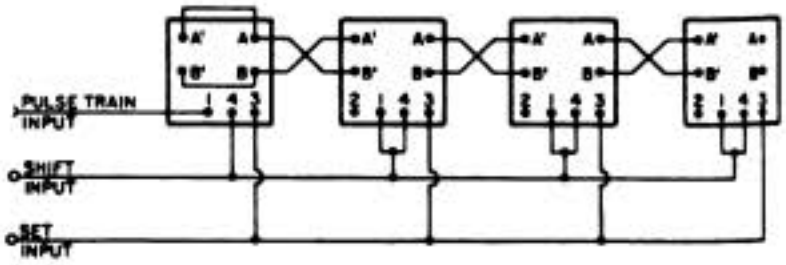


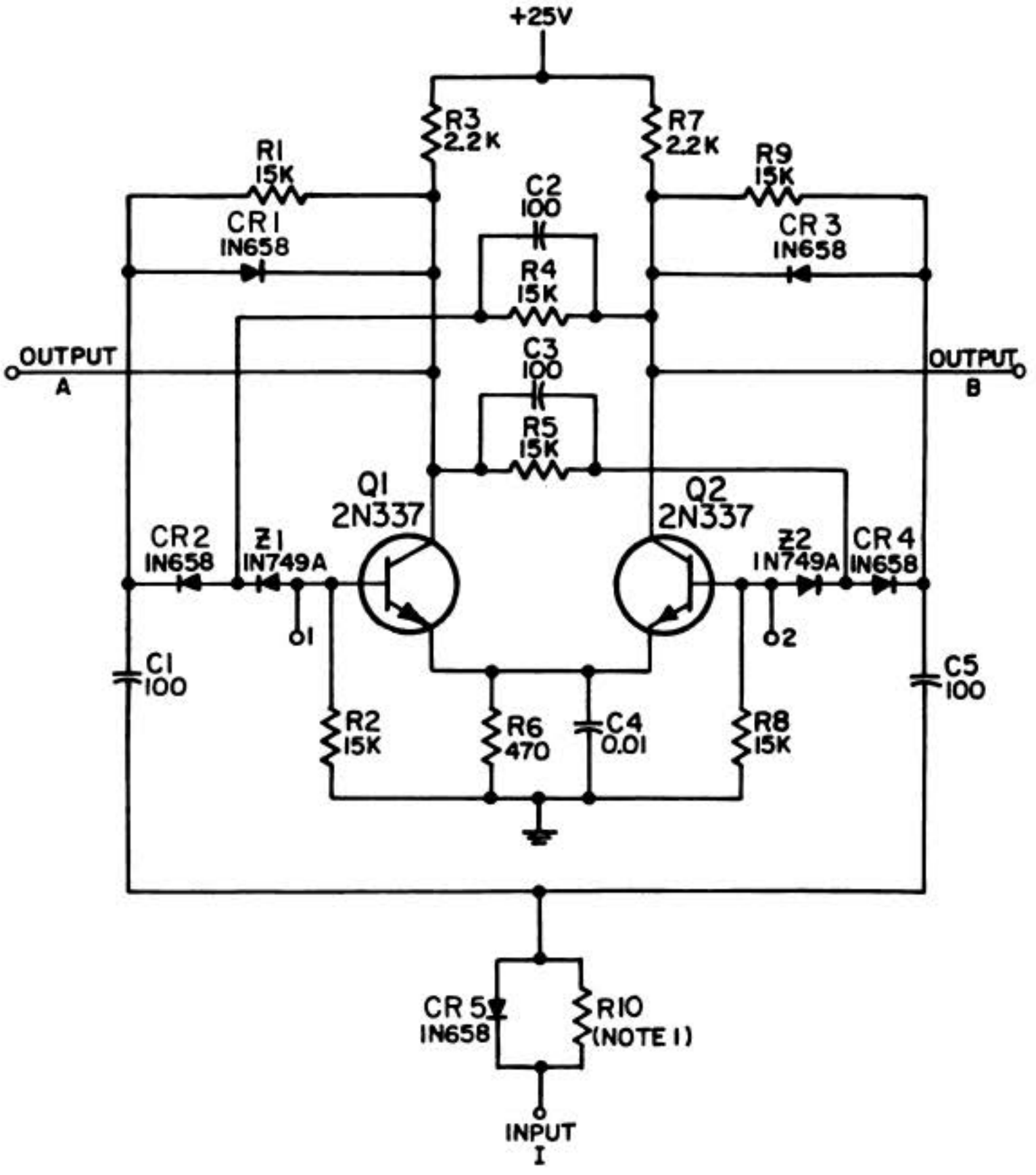
Figure 14–5.—Interconnection of modified PSC 14 for shift registers.

Notes

PREFERRED CIRCUIT NO. PSC 15
NON-SATURATING BISTABLE MULTIVIBRATOR

(Originally published as PC 253)

PREFERRED CIRCUIT NO. PSC 15
NON-SATURATING BISTABLE MULTIVIBRATOR



Unless otherwise stated: R in ohms; C>1 in pf; C<1 in μf; L in μh

(For specifications, see next page)

PSC 15 BISTABLE NON-SATURATING MULTIVIBRATOR

1. APPLICATION

PSC 15 is a bistable counting multivibrator which is used for frequency division of pulse trains when high stability is required. Cascade connection with appropriate feedback can provide any desired ratio. Among other uses of PSC 15 are coding, gating, and synchronizing.

2. DESIGN CONSIDERATIONS

Achievement of high counting rates with grown junction silicon transistors requires that the collector current saturation region be avoided, since when saturation occurs, the charge stored in the base region increases the trigger voltage requirement and prevents the

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Components:

ZI, Z2: 4.3 volts ±10% at 5 ma.

Maximum power dissipation (Note 2): R1, R2, R8, R9, R10: <0.01 watt; R4, R5: 0.02 watt; R3, R7: 0.17 watt; R6: 0.05 watt.

Limits (these are not tolerances; see Note 3): R3, R4, R5, R6, R7: ±10%; R1, R2, R8, R9, R10: ±20%. C1, C2, C3, C5: ±10%; C4: ±20%.

Operating characteristics:

Temperature range: −55°C to +125°C.

Maximum operating rate: 1 mc.

Input signal:

Polarity: Negative.

Amplitude: 12–20 volts.

Maximum rise time: 0.4 μsec for 1 mc operation (Note 4).

Maximum fall time: 0.04 to 0.4 μsec for 1 mc operation (Note 4).

Input impedance: 110 pf.

Output amplitude: 16 volts (Note 5).

Maximum delay: 0.2 μsec. (Start of trigger to start of output.)

Maximum loading:

Input: 1000 pf.

Output: 220 pf total both outputs, 1 mc operation.
440 pf total both outputs, 500 kc operation.

Power requirements: 25 volts ±5% at 10 ma.

NOTES:

1. If the input signal has a fall time shorter than 0.3 μsec, the input diode CR5 and resistor R10 must be included to prevent false triggering by the trailing edge of the trigger. For fall times between 0.15 and 0.3 μsec, a 470Ω resistor is satisfactory. If the fall time is less than 0.15 μsec, a 1KΩ resistor should be used. The input diode and resistor need not be added between cascaded stages.

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. For 500 kc operation, the maximum rise time is 0.6 μsec. Maximum fall time is limited only by the repetition rate.

5. The maximum variation in output amplitude is ±1% plus the percentage change in supply voltage. The output amplitude may vary ±1% over the temperature range; variation in the supply voltage will cause an equal percentage variation in output amplitude.

transistor from turning off quickly. Saturation is avoided by using breakdown diodes to prevent the collector junction from becoming forward biased. This is believed to be one of the best of the several methods available in that it does not require several low impedance supply voltages or selection of transistors. In addition, the output voltage is highly stabilized against changes as the temperature varies.

Saturation does occur if the breakdown diodes Z1 and Z2 are removed, even though, under these conditions, a back voltage of 0.9 volts is measured between collector and base of the ON transistor. This voltage, measured at the transistor terminals, does not indicate the actual condition at the collector junction. In the 2N337 it was found that the voltage drop across the bulk resistance of the collector material is sufficient to cause a back voltage to be measured at the transistor *terminals* even when the collector *junction* is forward biased. If saturation is to be prevented, therefore, the collector-to-base voltage must be clamped high enough to allow for this added voltage drop in the collector circuit.

2.1 *Switching and Steering:* The operation of PSC 15 is conventional except for the breakdown diodes, Z1 and Z2, which prevent the collector-to-base voltage of the conducting transistor from entering the saturation region. The circuit is triggered by a negative-going wave front at the base of the ON transistor. Positive-going wave fronts are rejected and the negative-going wave fronts directed to the correct stage by steering diodes CR2 and CR4. When the circuit is in the quiescent condition, the dc voltages applied to these diodes through R1 and R9 are such that the diode associated with the OFF transistor (CR2, Figure 15–1) is biased off by approximately 18 volts, while the diode associated with the transistor to be switched (CR4, Figure 15–1) is biased in the forward direction. Clamping diodes CR1 and CR3 provide low resistance paths for the discharge of capacitors C1 and C5 after a positive-going wavefront or after the trailing edge of a negative trigger. Input resistor R10 is added to slow the rise of positive-going wave fronts, since these are coupled, through the clamping diode associated with the ON transistor, to be base of the OFF transistor and may cause false triggering. Diode CR5 bypasses R10 for negative-going wave fronts so that the rise time of the desired trigger is unaffected. The diode and resistor need not be included if the rise of positive-going wave fronts is longer than 0.3 μsec.

2.2 *Static Conditions:* The dc voltages (Figure 15–1) are such that all three diodes associated with the ON transistor are conducting. Diodes CR3 and CR4 conduct in the forward direction, and breakdown diode Z2 conducts in the reverse direction. Collector-to-base voltage, V_{CB}, of the ON transistor may thus be represented as

$$V_{CB} = -V_{CR3} - V_{CR4} - V_{Z2},$$

where all voltage drops are in the conventional current forward direction. Typically $V_{CB} = -0.5 - 0.5 + 3.2 = 2.2$ volts. Variation in this value with temperature is small due to the canceling effect of the voltage drops, i.e., all three diodes have negative temperature coefficients, but the breakdown diode contributes a positive voltage drop while the other two diodes contribute negative voltage drops.

Typical potentials associated with the ON transistor over the temperature range are given in Table 15–1. Collector-to-emitter voltage,

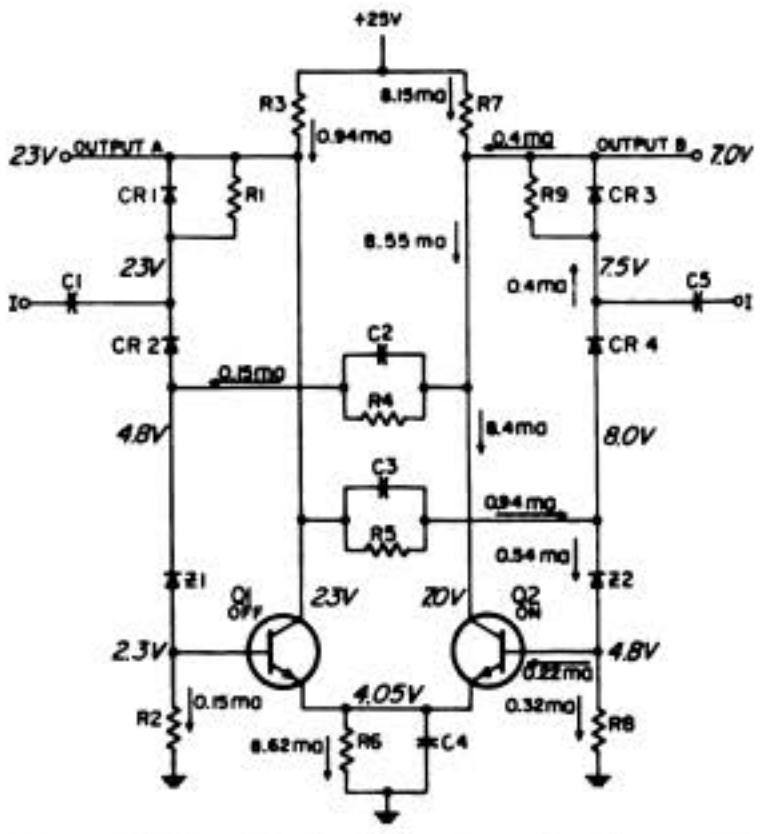


Figure 15–1.—Typical currents and voltages with Q2 conducting.

TABLE 15-1.—*Potentials associated with the conducting transistor*

	−55° C	+25° C	+125° C
V_{Z2}	3.4 v	3.2 v	2.85 v
V_{CR3}	0.7	0.5	0.3
V_{CR4}	0.7	0.5	0.3
V_{CB}	2.0	2.2	2.25
V_{BE}	0.9	0.75	0.65
V_{CE}	2.9	2.95	2.9

V_{CE}, equal to the sum of V_{CB} and V_{BE}, is seen to be practically constant, thus stabilizing the collector current against changes in temperature. The OFF collector voltage is not dependent on the transistors and hence is relatively independent of temperature, while the ON collector voltage is determined by the collector current, I_C, which is stabilized. As a result the output voltage, equal to the difference between transistor ON and OFF collector voltages (see Figure 15-1) is also stabilized against temperature changes.

3. PERFORMANCE

The operating characteristics shown on page 15-3 are conservative. Input resistor R10 is not needed if the rise of positive-going wave fronts is slow or if operation is confined to room temperatures. In the latter case, if the rise time of the negative input signal is less than 0.1 μsec, PSC 15 can be triggered by a signal of 4 to 8 volts, and the counting rate and output loading may both be increased. When the transistor beta increases with temperature, higher input voltages are required, necessitating the addition of the input resistor to prevent false triggering. The input signal voltage level will be less critical if the transistors are selected to obtain betas near the center of the range. Typical output voltage waveforms are shown in Figure 15-2.

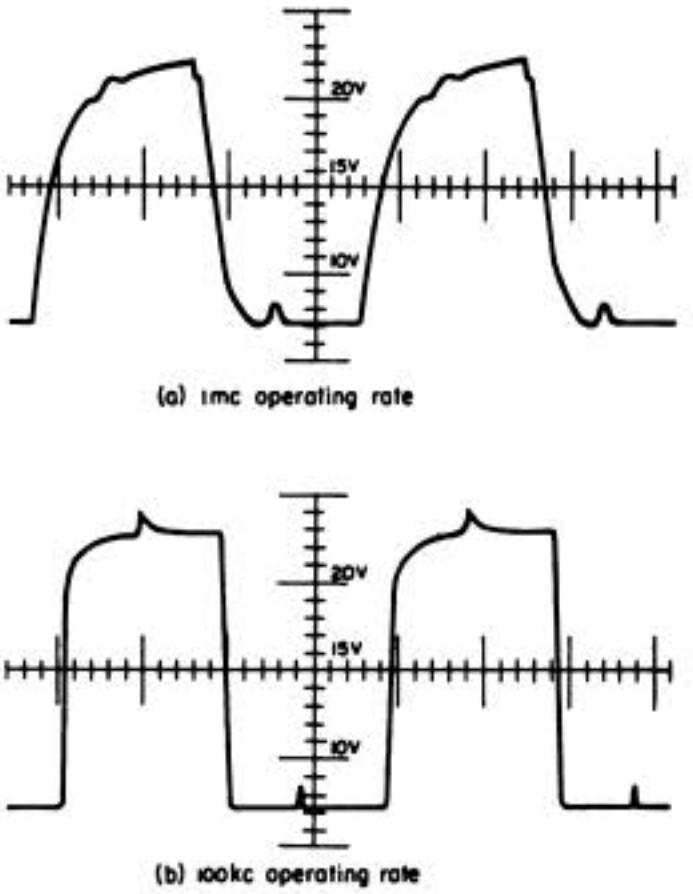


Figure 15-2.—Typical output voltage waveforms.

4. EXAMPLE OF USE

A typical method of connecting four stages of PSC 15 to obtain a decade counter is shown in Figure 15-3. Capacitor C1, resistor R2, and diodes CR2, CR3, and CR4 introduce feedback of the correct polarity to convert binary operation to decade operation.[1] If the input to the decade has a fall time shorter than 0.3 μsec, input diode CR1 and resistor R1 must be included to prevent false triggering (see Note 1, page 15-3, and Section 2.1).

[1] J. Millman and H. Taub, *Pulse and Digital Circuits*, McGraw-Hill, New York, 1956, p. 327.

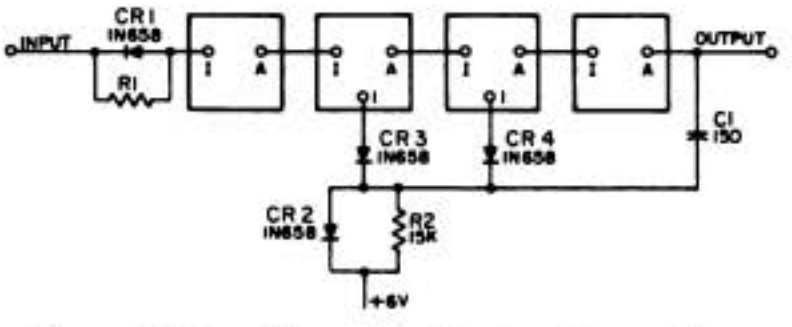


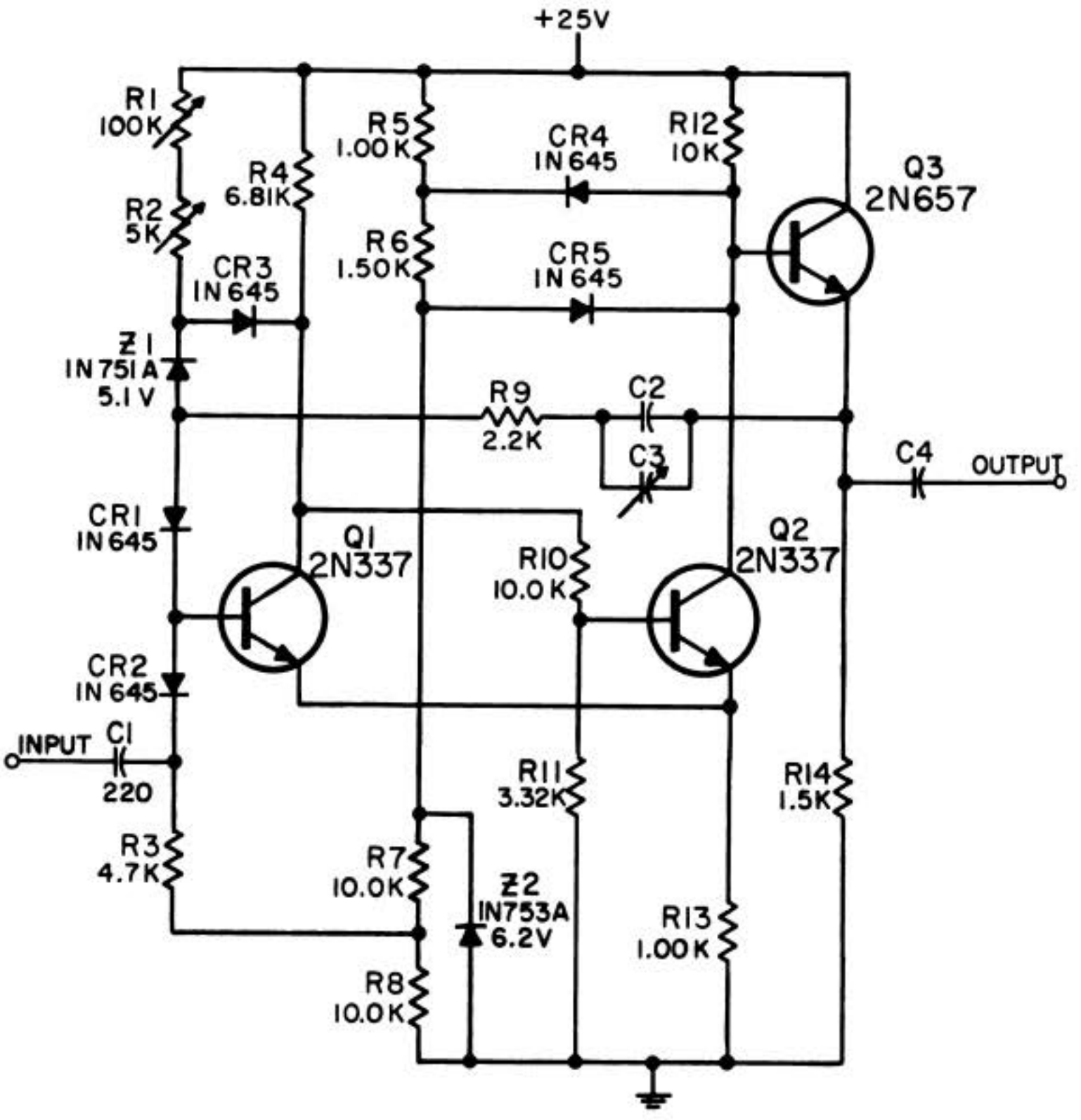
Figure 15-3.—Connection for decade counting.

Notes

PREFERRED CIRCUIT NO. PSC 16
MULTIVIBRATOR VARIABLE GATE GENERATOR

(Originally published as PC 252)

PREFERRED CIRCUIT NO. PSC 16
MULTIVIBRATOR VARIABLE GATE GENERATOR



Unless otherwise stated: R in ohms; C>1 in pf; C<1 in μf; L in μh

(For specifications, see next page)

Components:

Z1: 5.1 volts ±5% at 5 ma; temperature coefficient ≈−0.015%/°C; dissipation=5 mw at 125°C.

Z2: 6.2 volts ±5% at 5 ma; temperature coefficient ≈+0.02%/°C; dissipation=50 mw at 125°C.

R1: Variable from 10KΩ to 100KΩ for continuously variable gate; 30KΩ to 100KΩ for fine control on step-switched gate. Linearity <0.2%.

C2: Select for desired gate width (see Table 16-1) and for temperature compensation (see Figure 16-3). (Note 1.)

C3: See Section 2.2 of text.

C4: Select for maximum allowable percentage droop of output gate.

$C4 > \frac{100 T_{max}}{R_L P}$, where T_{max}=maximum gate width, R_L=load resistance, and P=maximum percentage droop desired.

Maximum power dissipation (Note 2): R2, R3, R7, R8, R9, R11: <0.01 watt; R13: 0.01watt; R1, R10: 0.02 watt; R4, R12: 0.05 watt; R5: 0.06 watt; R6: 0.1 watt; R14: 0.2 watt.

Limits (these are not tolerances; see Note 3 below): R1, R2, R5, R6, R7, R8, R10, R11, R13: ±1%; R4: ±2%; R12: ±5%; R3, R9, R14: ±10%. C2: See Section 2.4 of text; C3: ±5%; C1, C4: ±20%.

Operating characteristics:

Temperature range: −55°C to +125°C.

Input signal:

Polarity: Negative.

Amplitude: 10–20 volts.

Repetition rate: Limited by circuit recovery time. (See below.)

Wave front slope: >10 volts/μsec.

Pulse duration: 1 μsec to $0.5 T_{min}$, where T_{min}=minimum gate width to be generated.

Output gate:

Polarity: Negative.

Amplitude (Note 4): 12.5 volts.

Width: 10–10,000 μsec continuously variable by R1 in 10 to 1 segments selected by C2.

Accuracy and linearity: Accurate to ±2% over the temperature range; linear to ±1%; over-all accuracy and linearity=±3%.

Rise time (Note 5): 1.0 μsec (longest).

Fall time (Note 5): 2.0 μsec (longest).

Maximum jitter: 0.1% of gate width.

Loading: 8KΩ (min.). 220 pf (max.).

Recovery time: $<0.85\ T_{max}$ where T_{max}=gate width generated when R1=100KΩ.

Delay: 0.1 to 0.3 μsec. (Start of trigger to start of output.)

Power requirements: 25 volts ±1% at 24 ma.

NOTES:

1. Gate widths may be step-switched by C2 with R1 acting as a fine control.

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. In this circuit the initial tolerance of all resistors need only be ±10%; however, drifts due to environmental changes or aging must be held to the percentage specified.

4. The maximum variation in output amplitude is ±3% plus the percentage change in supply voltage. The output amplitude may vary ±3% over the temperature range; variations in the supply voltage will cause an equal percentage variation in output amplitude.

5. Rise and fall times may be reduced 50% by using a 2N697 in place of the 2N657.

PSC 16 MULTIVIBRATOR VARIABLE GATE GENERATOR

1. APPLICATION

PSC 16 generates a rectangular waveform, commonly referred to as a "gate", whose duration is relatively independent of temperature effects and directly proportional to the setting of a linear potentiometer. Such a circuit is frequently used in radar equipment to produce movable markers for display. If desired, the gate may be step-switched by capacitor C2, with the potentiometer acting as a fine control.

2. DESIGN CONSIDERATIONS

A variable rectangular waveform may be generated by either of two basic circuits, the phantastron or the monostable multivibrator. PSC 16 is similar to the cathode-coupled version of the latter circuit. Because transistors are sensitive to temperature and operating point changes, certain complexities must be added to the basic circuit in order to obtain a gate continuously variable over a 10 to 1 range and stabilized against temperature changes. These additions are as follows: a breakdown diode, Z1, in combination with a rectifier diode, CR3, to prevent saturation of the normally ON transistor, Q1; a breakdown diode, Z2, in combination with two clamping diodes, CR4 and CR5, to stabilize both the output voltage and the voltage applied across the timing capacitor, C2, against temperature changes; a rectifier diode, CR1, to prevent excess reverse bias from being applied to the base-emitter junction of Q1; and an emitter-follower output to reduce loading effects on the gate width.

2.1 *Circuit Operation*: In the rest state, Q1 is held on by base current flow through R1, R2, Z1, and CR1, while Q2 is biased off by an emitter voltage which is larger than its base voltage. Diode CR4 is conducting, holding the Q2 collector to approximately 18 volts, a level determined by the divider consisting of R5, R6, and Z2.

The circuit is triggered by a negative-going wave front at the base of the ON transistor Q1, turning it off. The resulting regeneration through Q2 cuts off the base current of Q1 and completes the switching action. Diode CR1 prevents the negative voltage that occurs at the junction Z1,R9 immediately after switching (Fig. 16–1) from being applied to the base of Q1 and exceeding the emitter-to-base reverse breakdown voltage of that transistor. Positive-going input wave fronts are rejected by steering diode CR2. During switching, resistor R9 prevents the emitter follower, Q3, from loading the trigger source through CR1 and C2.

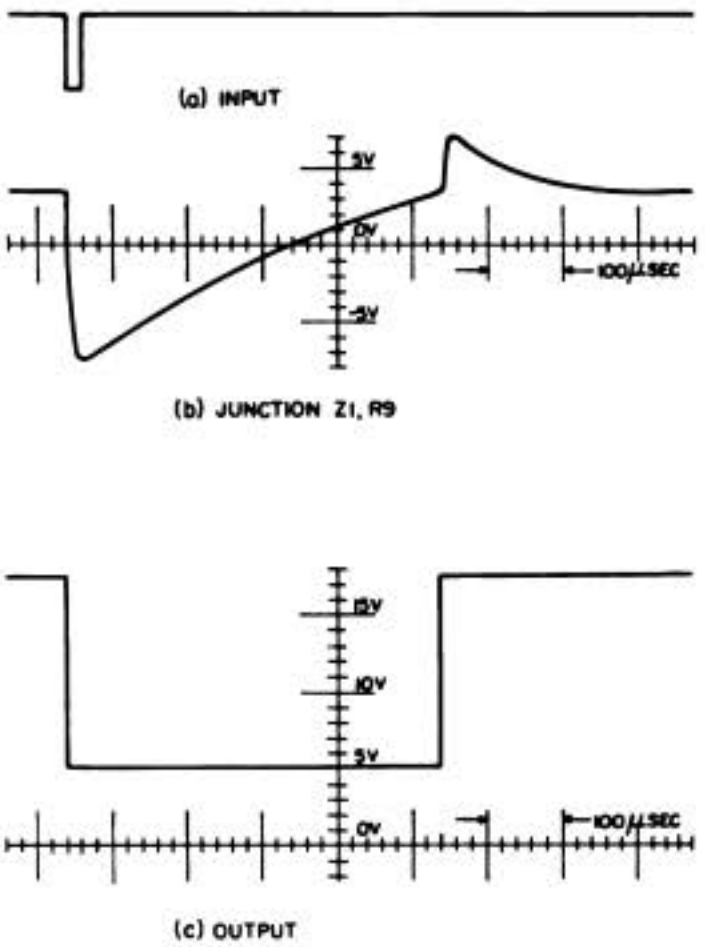


Figure 16–1.—Typical waveforms.

After switching, the circuit is in a quasi-stable state with Q1 off, Q2 on, and diode CR5 conducting, holding Q2 collector voltage to approximately the breakdown voltage of Z2. During this time, capacitor C2 discharges through R1, R2, Z1, R9, and R14, causing the voltage at the junction of Z1 and R9 to rise in an exponential curve (Fig. 16–1) until CR1 begins to conduct, supplying base current to Q1, and ending the quasi-stable state. The discharge of C2, adjustable by R1, produces the timing waveform which controls the gate width. For adjustment to be linear over a 10 to 1 range, resistors R2, R9, and R14 must be small relative to the minimum value of R1.

Due to emitter-follower action, the dc output voltage follows the Q2 collector at all times. The output voltage is well stabilized against

changes in temperature, since the upper and lower limits of its swing are clamped by diodes CR4 and CR5 respectively. Even more important, the change in voltage applied across C2, which affects the timing waveform and gate width, is also clamped and is therefore temperature stable.

Emitter follower Q3 improves circuit operation by decreasing the effect of output loading on gate width, and by allowing a quick recharge of C2 after the end of the gate, thus decreasing the recovery time of the circuit. For low output impedance and linear adjustment of gate width by R1, emitter resistor R14 must be small, thereby increasing the power dissipation requirements of Q3. The 2N657 or the 2N697 must be used if the circuit is required to operate over the entire high-temperature range. The 2N337 may be used if the operating temperature is limited to a range of 5°C to 40°C.

2.2 *Gate Width Range and Adjustment:* The value of capacitor C2 is chosen for the range of gate widths desired. Table 16-1 gives the approximate values required to obtain gate widths of 10–100 μsec, 100 μsec–1 msec, or 1–10 msec. Capacitor C3 should equal approximately 10% of C2 to allow precise calibration of R1 (see Section 2.3) for any set of circuit component values within the specified limits. However, for a particular set of components, an approximate value for C3 may be determined experimentally and a fixed capacitor inserted. A variable capacitor only 1% the value of C2 may then be used for calibration of R1.

A potentiometer control of C2 discharge time provides the continuous adjustment of gate width. For a linear adjustment over a wide range, the timing potentiometer, R1, must be placed in the base circuit of Q1, since attempting to isolate it from the dc circuit of the transistor base would introduce shunting resistance, reducing the range of adjustment of the potentiometer and destroying its linearity. The necessary location of the timing adjustment in the dc base circuit, however, results in a wide range of base currents to the normally ON transistor. If it were not for breakdown diode Z1, the lower values of timing resistance would result in large base currents and saturation of the transistor. Under these conditions, the charge stored in the base region would prevent the transistor from turning off quickly and would require trigger voltages much too large for correct triggering under non-saturated conditions, i. e., when higher values of timing resistance are used. The discrepancy would be magnified by changes in transistor beta with temperature.

Although saturation occurs when the collector-base *junction* is biased in the *forward* direction, the voltage drop in the bulk resistance of the 2N337 collector under these conditions is large enough to result in a *reverse* bias being measured between the collector and base *terminals*. Breakdown diode Z1 in combination with diode CR3 prevents saturation by holding the collector-to-base voltage, V_{CB}, to a value greater than the aforesaid voltage drop, in this case approximately 1 volt under worst conditions. For Q1, V_{CB} may be represented as

$$V_{CB} = -V_{CR3} - V_{z1} + V_{CR1},$$

where the voltage drops are in the conventional current forward direction. Typically $V_{CB} = -0.5 + 4.0 + 0.5 = 4.0$ volts.

2.3 *Calibration of Gate Width Adjustment:* In most applications, potentiometer R1 will be calibrated so that gate width may be read directly from the potentiometer dial in terms of units appropriate to a particular application. The calibration is accomplished for any set of circuit component values within the specified limits by adjustment of R2 and C3.

The percentage change in gate width with variation of C3 is constant over the entire range of R1, while the percentage change with variation of R2 is largest at low values of R1. C3 is set so that the dial tracks near the high end of

TABLE 16-1.—*Approximate value of C2 for desired gate width*

Gate width* μsec	R1 Ω	C2 μf
10–100	10K–100K	0.0016
100–1000	10K–100K	0.016
1000–10,000	10K–100K	0.16

*Gate width ≈ 0.6 R1C2 when R1 > 30KΩ.

the range of R1; R2 is set to compensate for the reduction in the voltage change applied to the junction of Z1,R9 (see Fig. 16-1) as the resistance of R1 is reduced. C3 and R2 should be adjusted to obtain the best independent linearity [1] for the particular transistors and breakdown diodes in the circuit.

The procedure is first to set R2 at the center of its range and R1 at a large value, adjusting C3 for the desired dial reading. Then set R1 near its minimum value of 10KΩ, and adjust R2 for the desired dial reading. Repeat the above procedure until interaction between the two adjustments is eliminated, remembering to adjust for minimum error over the entire range. This may necessitate checking a few intermediate settings of R1. If replacement of a transistor or breakdown diode is necessary, the calibration should be rechecked. Figure 16-2 is a typical curve showing the independent linearity of the gate width adjustment.

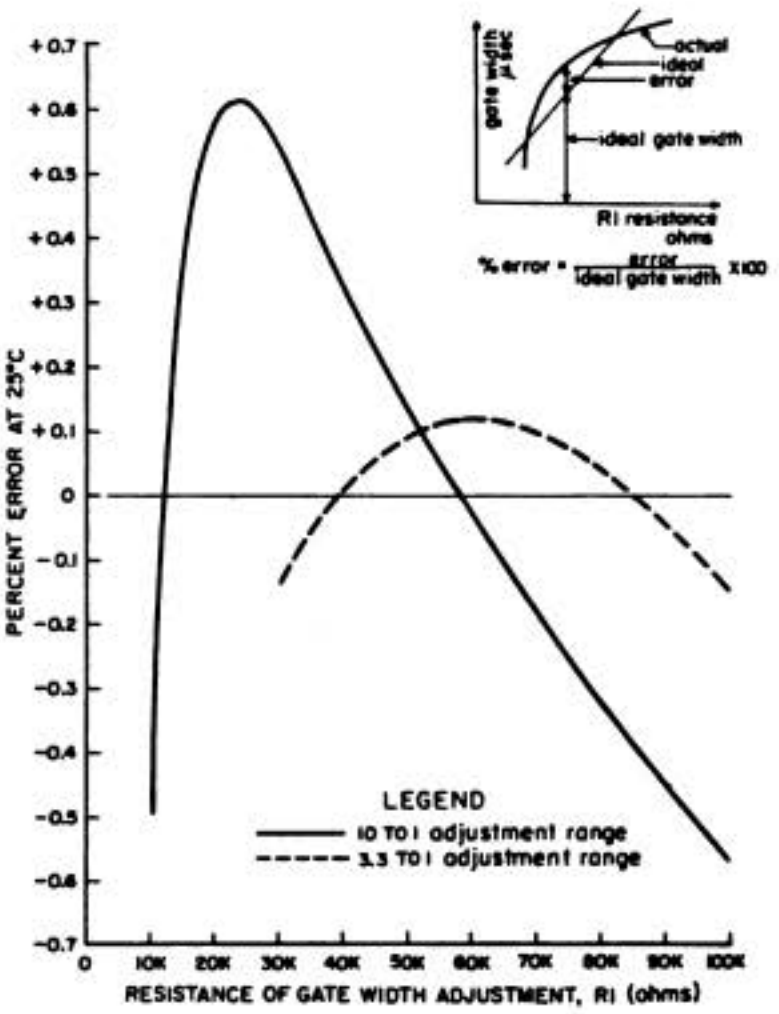


Figure 16-2.—Independent linearity of gate width adjustment.

2.4 *Temperature Compensation and Selection of C2:* An important consideration when choosing C2 is its percent change with temperature over the complete temperature range of −55°C to +125°C. PSC 16 is designed so that normal changes in C2 capacitance with temperature will compensate for temperature changes in the remainder of the circuit. In a typical circuit, for exact temperature compensation of gate width, C2 should have a temperature characteristic similar to that shown in Figure 16-3. Stated another way, a typical circuit with C2 unaffected by temperature would have a percentage change in gate width vs. temperature curve exactly like the curve of Figure 16-3, except that the ordinate scale would be inverted. Adding to this the percent changes of C2 with temperature would give an over-all circuit in which the gate width does not vary at all with temperature.

It should be noted that the solid curve of Figure 16-3 is typical. The curve for exact compensation may vary ±2% from that shown (dashed curves). Exact temperature compensation could be obtained by matching C2 to the remainder of the circuit, but this is seldom possible.

PERFORMANCE

3.1 *Output Gate:* PSC 16 generates a rectangular waveform (gate), 12.5 volts in amplitude, which may be varied linearly by a potentiometer over a 10 to 1 range. Longest rise and fall times of the gate are 1.0 μsec and 2.0 μsec, respectively. Independent linearity [2] over the temperature range is ±3% or better.

Independent linearity of the gate width adjustment at 25°C is better than ±1% over a 10 to 1 continuous adjustment range (Fig. 16-2) and better than 0.3% over a 3.3 to 1 adjustment range, i.e., R1 variation from 30KΩ to 100KΩ. Over the −55°C to 125°C temperature range, the output gate width, whether step-switched or continuously variable, is accurate within ±2% of its value at 25°C. Reduc-

[1] Independent linearity is the deviation when the slope and position of the straight line representing desired output versus shaft rotation may be chosen to make the deviation a minimum. This is the deviation from the "best fit" straight line as opposed for instance to using the straight line determined by the zero and 100% points. See J. F. Blackburn, Components Handbook, *Rad. Lab. Series*, Vol. 17, McGraw-Hill, N.Y., 1949, pp. 266, 267.

[2] *Ibid.*

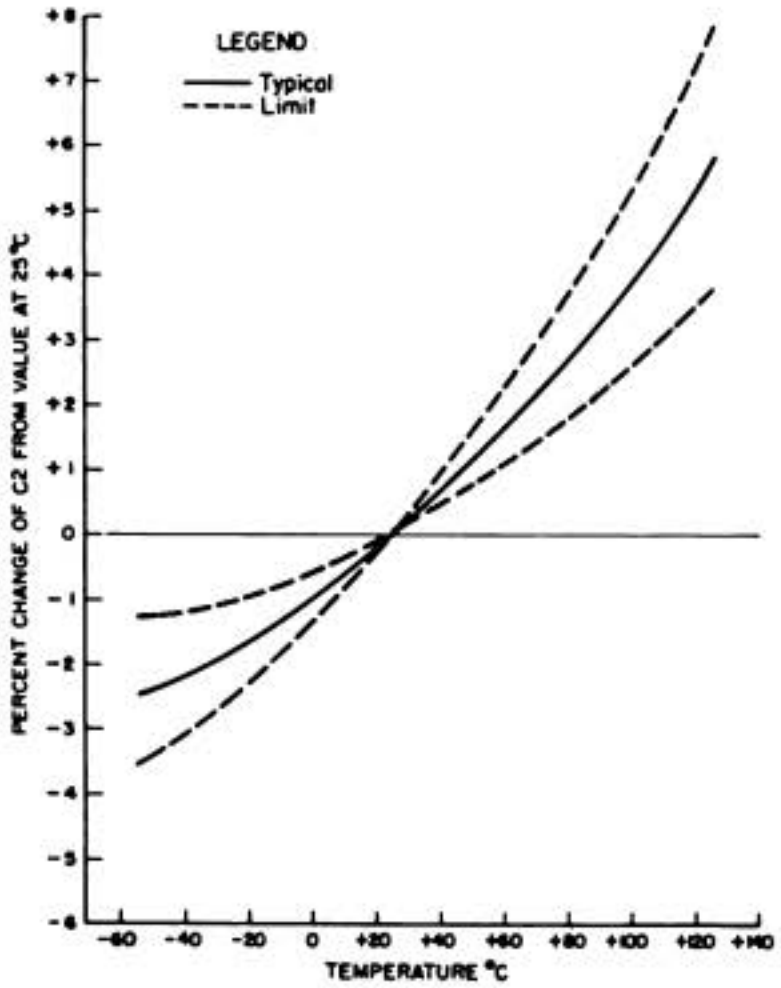


Figure 16–3.—Temperature characteristic of C2 required to compensate for temperature changes in remainder of circuit.

ing the maximum temperature excursion to +100°C will increase gate width accuracy to ±1.5%. Independent linearity over the temperature range is obtained by adding the ±1% linearity at 25°C to the ±2% maximum variation with temperature. Percentage changes in supply voltage are reduced by a factor of 10 in their percentage effect on gate width.

The voltage amplitude of the output gate at 25°C is approximately 12.5 volts, depending upon the exact value of Z2 breakdown voltage. Once determined for a particular circuit, the amplitude is accurate to ±3% over the temperature range. Percentage variation in supply voltage causes an equal percentage variation in the output gate amplitude.

Rise and fall times of the output gate may be reduced 50% by using a 2N697 in place of the 2N657 in the emitter follower stage, Q3. Both rise and fall times are longest at the low temperature extreme, −55°C.

Circuit recovery time varies with the value of timing capacitor C2. Expressed as a function of gate width, the recovery time is less than 0.85 T_{max}, where T_{max} is the maximum gate width which may be generated (R1=100K) with any particular value of C2.

Resistive loading of the output is limited to 8KΩ or more over the range of R1 from 10KΩ to 100KΩ. Loading down to 5KΩ is possible when the minimum setting of R1 is 30KΩ. Capacitive loading up to 500 pf will have little effect on gate fall time, but 220 pf is maximum to preserve the 1.0-μsec rise time limit indicated on the specification sheet, p. 16–3.

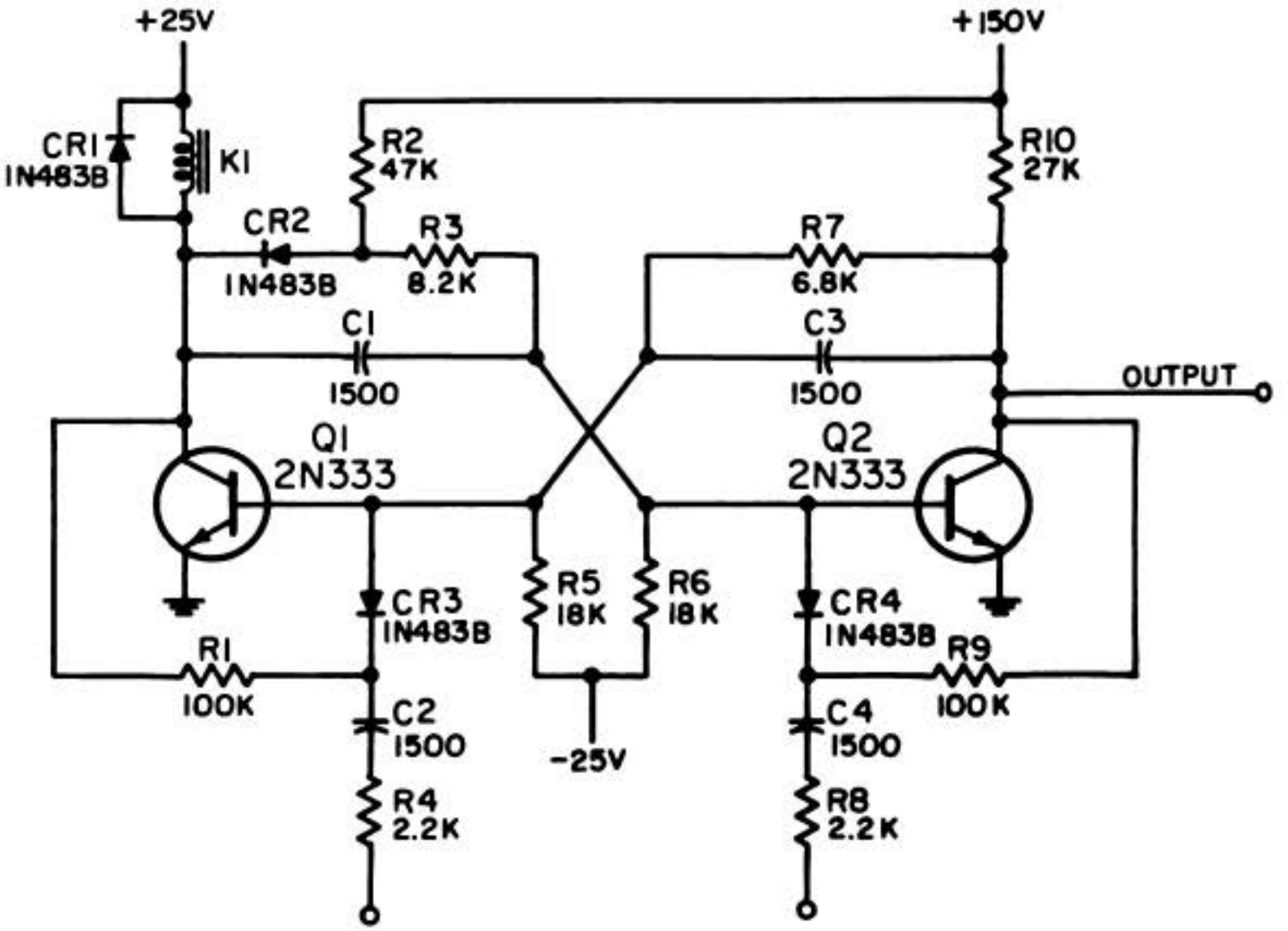
3.2 *Input:* Any input variations within the limits specified on page 16–3 will have negligible effect (less than 0.1%) on the output gate width. The output gate width is sensitive to a positive-going wave front which occurs at or near the end of the gate. For this reason the maximum trigger duration is limited to less than 50% of the gate width.

Notes

PREFERRED CIRCUIT NO. PSC 17
RELAY CONTROL SATURATING MULTIVIBRATOR

(Originally published as PC 251)

PREFERRED CIRCUIT NO. PSC 17
RELAY CONTROL SATURATING MULTIVIBRATOR



SET INPUT (RELAY DE-ENERGIZED) **RESET INPUT (RELAY ENERGIZED)**

Unless otherwise stated: R in ohms; C in pf

Components:

Q1, Q2: See Note 1.

K1: Winding resistance 2.7KΩ±10%; maximum pull in power: 100 mw.

Maximum power dissipation (Note 2): R1, R4, R8, R9: <50 mw; R2: 1 watt; R3: 100 mw; R5, R6: 70 mw; R7: 500 mw; R10: 1.5 watts.

Limits (these are not tolerances; see Note 3): R2, R10: ±5%; all other R: ±10%. All C: ±20%.

Operating characteristics:

Temperature range: −65°C to +125°C.

Input: 20-volt negative-going waveform or pulse with 10-μsec maximum rise time and minimum duration at −20-volt level of 3 μsec.

Input impedance: 2.5KΩ, or 400Ω with R4 and R8 omitted.

Outputs: Relay K1 energized by 8 ma (on); de-energized by 0.5 ma (off).

Voltage output: 30 ±6 volts.

Power requirement: 150 volts dc ±10% at 10 ma; 25 volts dc ±10% at 10 ma; −25 volts dc ±10% at 3 ma.

(For Notes, see bottom of next page)

PSC 17 RELAY CONTROL SATURATING MULTIVIBRATOR

1. APPLICATION

PSC 17 is intended for on-off control of electromechanical devices such as relays where the current ratio must be 10 between the on and off condition. The rate usually is limited by the response time of the controlled device. If desired, the control current can be reversed in direction between the on-off states.

2. DESIGN CONSIDERATIONS

This circuit is a modification of the saturating multivibrator PSC 14. The diode CR2 and resistors R2,R3 are added to isolate the load K1 when Q1 is off. If the values of the resistors are chosen within the proper limits, the off current through the relay is the sum of the leakage currents through Q1 and CR2, or less than 0.5 ma at 125°C. This provides a relay current ratio from on to off of at least 15. For comparison, PSC 14 using 2N333 transistors has an on-off ratio of less than 5 for the load currents. The modifications provide an improvement of three times in the current resolution.

2.1 *Circuit Operation:* The circuit operation is that of an ordinary transistor Eccles-Jordan, except that the current drive to hold Q2 in the on state is furnished through R2 and R3 rather than through Q1 collector load. Diode CR2 is nonconducting.

The collector power dissipation limit and the high saturation resistance of the 2N333 require that the collector current not exceed approximately 11 ma for operation to 125°C. Collector resistors of lower value than that shown will cause the collector currents to exceed this limit and will reduce the temperature range accordingly. An increase of impedances would be desirable to decrease dissipation, but the relay coil resistance would have to be increased.

2.2 *Transistor Type:* The high forward resistance of grown junction silicon transistors is incompatible with subminiature relays. The circuit power efficiency falls off sharply as the current is increased above a few milliamperes. Small relays usually require from 5 to 15 ma at a low voltage. The 2N333 was specified as a moderately priced unit in large quantity use. A diffused junction transistor such as the 2N550 has a lower resistance and higher dissipation rating but is more expensive. Lower circuit impedance could be achieved with transistors similar to the 2N550 with a resulting improvement in circuit power efficiency because of the lower permissible collector and base supply voltages.

2.3 *Relay Type:* The relay or other electromechanical device under control must have the characteristic of being energized by 8 ma coil current and being de-energized when the current drops to 0.5 ma. This specification is based on the dc load presented to the multivibrator and the power furnished to the relay winding. The inductance of the coil is unimportant, even though the rise and fall times are somewhat increased. The speed of response depends only on the relay response time.

NOTES:

1. The 2N333 has been dropped from the Preferred and Guidance List of Transistors (MIL-STD-701) since this circuit was first published in 1959. The 2N335, which appears on the current Preferred List, is similar to the 2N333 in all important respects except beta. If the 2N335 is used in PSC 17, the 70% higher beta will result in the "on" transistor being driven further into saturation with a resulting increase in transition time. This is not detrimental to the operation of the circuit, since the transition time is much less than the response time of the relay, but it may require that the trigger amplitude be increased to assure triggering at the high beta limit.

2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

The maximum power dissipation rating of the coil should be not less than 250 milliwatts.

3. PERFORMANCE

3.1 *Trigger Input:* The input signal required for triggering is approximately the same as that for PSC 14, the simple saturating multivibrator. Since a high repetition frequency is not a major consideration, the coupling capacitors C2 and C4 have been increased.

A trigger of 14 volts with a rise time of 10 μsec is usually adequate, but with high h_{FE} transistors at the high limit temperature, a level of about 20 volts provides more dependable operation. The input circuit should be allowed at least 5 milliseconds to recover from a positive signal before the next trigger is applied.

If the source impedance is low enough, R4 and R8 may be omitted. The input impedance is then approximately 400 ohms. Capacitors C2 and C4 should be increased to 4700 pf to maintain the proper trigger pulse duration at the base of the transistor.

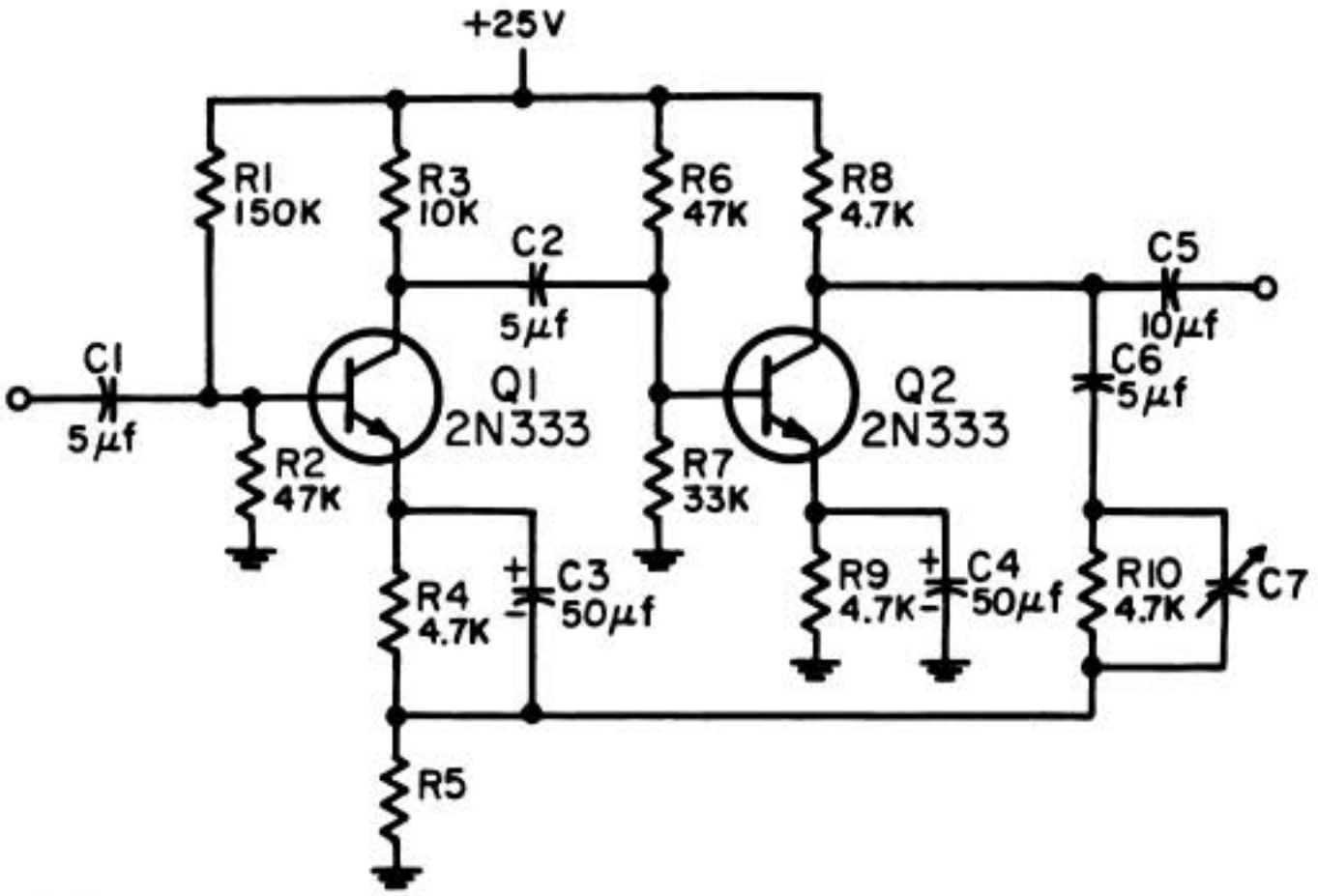
3.2 *Voltage Output:* A voltage output in phase with the relay closing may be taken from the collector of Q2. The level will be 30 volts, and a 10% variation in the 150-volt supply and the variability of transistors and resistors will cause a variation of about 6 volts. The source impedance at this output is 5KΩ for the positive excursion and is the saturation resistance of Q2 for the negative excursion.

Notes

PREFERRED CIRCUIT NO. PSC 18
LOW LEVEL VIDEO AMPLIFIER

(Originally published as PC 201)

PREFERRED CIRCUIT NO. PSC 18
LOW LEVEL VIDEO AMPLIFIER



Components:

Q1, Q2: See Note 1.

R5: Select for desired voltage amplification (see table below).

C7: Between 4 and 30 pf; to be selected after total output capacitance is determined.

Maximum power dissipation (Note 2): All R<50 mw.

Limits (these are not tolerances; see Note 3): R5, R10: ±1%; all other R: ±10%.
All C: ±20%.

Operating characteristics:

Temperature range: −50°C to +150°C.

R5	100Ω	220Ω	470Ω
Input impedance	22KΩ	27KΩ	32KΩ
Maximum input amplitude	±45 mv peak	±100 mv peak	±200 mv peak
Amplification:			
Nominal	45	20	10
Maximum variation with transistor replacement (Note 4)	±5%	±3%	±2%
Maximum variation from 25°C value (Note 4):			
at 125°C	+5%	+4%	+2%
at −50°C	−10%	−7%	−7%
Maximum output amplitude	±2 v peak	±2 v peak	±2 v peak
Rise time (Note 5):			
at 25°C	0.5 μsec	0.4 μsec	0.35 μsec
at 150°C	1.0 μsec	0.9 μsec	0.7 μsec
Droop for 500-μsec pulse at −50°C	3.0%	1.5%	1.0%
Output impedance	250Ω	210Ω	180Ω
Minimum load resistance	10KΩ	10KΩ	10KΩ

Power requirements: 25 volts dc ±10% at 3.5 ma.

(For Notes, see bottom of next page)

PSC 18 LOW LEVEL VIDEO AMPLIFIER

1. APPLICATION

PSC 18 is a high-gain low-level (±2.0 volts maximum output) transistor video amplifier for use in applications where stability of gain and a wide temperature range are important. It is non-inverting, has an input impedance of 20KΩ, and will operate into loads of 10KΩ or larger. Impedance levels are such that several of these circuits may be cascaded for additional voltage gain.

2. DESIGN CONSIDERATIONS

Silicon transistors are used to obtain a wide temperature range. Negative feedback of 20 db extends the frequency range and stabilizes the voltage amplification against temperature changes and transistor replacement. Selection of R5 provides for a choice of voltage gain.

Either raising the value of R5 or lowering the value of R10 will decrease the voltage amplification with only slight accompanying change in bandwidth. This situation results from the fact that changing either R5 or R10 in a direction to decrease voltage amplification decreases the open loop voltage gain, A_o, while increasing the feedback factor, b. Thus the change in magnitude of negative feedback, bA_o, is slight, resulting in only a slight increase in bandwidth at the lower gain. Changing R5 is preferred since it will not derate the maximum output voltage that may be obtained.

The major limitation on circuit bandwidth and temperature range is imposed by the transistor itself. The input impedance, current amplification and, to a lesser extent, the output impedance of the transistor all have an effect on the voltage amplification. The limitation is imposed because the variation of these parameters with frequency or with temperature is much more severe than the variation in component values. Since all three parameters are interdependent in determining voltage gain, there is no one parameter measurement which will gauge operation of the transistor at extreme temperatures or at high frequency. For this reason the alpha cutoff frequency, $f_{\alpha_{ce}}$, though a good indication of high frequency performance, is not directly related to the rise time that may be achieved with any particular transistor.

Resistors R4 and R9, in conjunction with the biasing resistors, serve to minimize the change in quiescent operating point accompanying temperature variation and transistor replacement. A ratio indicating the relative amount of stabilization may be computed for each stage with the value of unity indicating perfect operating point stabilization. The stabilization ratio for Q1 is

$$\frac{h_{fe}}{h_{fe}+1+\dfrac{1}{\text{R4/R1}+\text{R4/R2}}}$$

where h_{fe} is the common emitter forward current transfer ratio. A similar expression applies to Q2 with R9, R6, and R7 substituted for R4, R1, and R2. The stabilization ratios are 0.8 and 0.87 for Q1 and Q2 respectively.

The value of R8 is low enough so that the total capacitance of the output terminals is driven without a significant increase in rise

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NOTES:

1. The 2N333 has been dropped from the Preferred and Guidance List of Transistors (MIL-STD-701) since this circuit was first published in 1959. The same circuit configuration can be used with the 2N335, which is on the current Prefered List, if the component values are changed to adjust the operating point to the higher beta.
2. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.
3. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.
4. Load resistance 10KΩ.
5. Total output capacitance 30 pf.

time and yet high enough to provide sufficient open-loop gain for the circuit.

Capacitor C7 compensates for overshoot produced by the total capacitance at the output terminals and is to be selected after that capacitance is determined. Its value will be between 4 and 30 pf for output capacitance values up to 100 pf.

An important aspect of the circuit design is the ability to cascade feedback pairs for additional voltage amplification. This is possible due to the high input impedance and low output impedance resulting from negative voltage feedback.

3. PERFORMANCE

Voltage amplifications of 45, 20 or 10 are obtained for R5=100Ω, 220Ω, or 470Ω, respectively. For each, an output extending plus and minus 2 volts from the average voltage of the waveform may be obtained.

For any 2N333 transistors within the specified limits of beta (18 to 40), the maximum variation of voltage amplification with transistor replacement is given in Figure 18–1 for

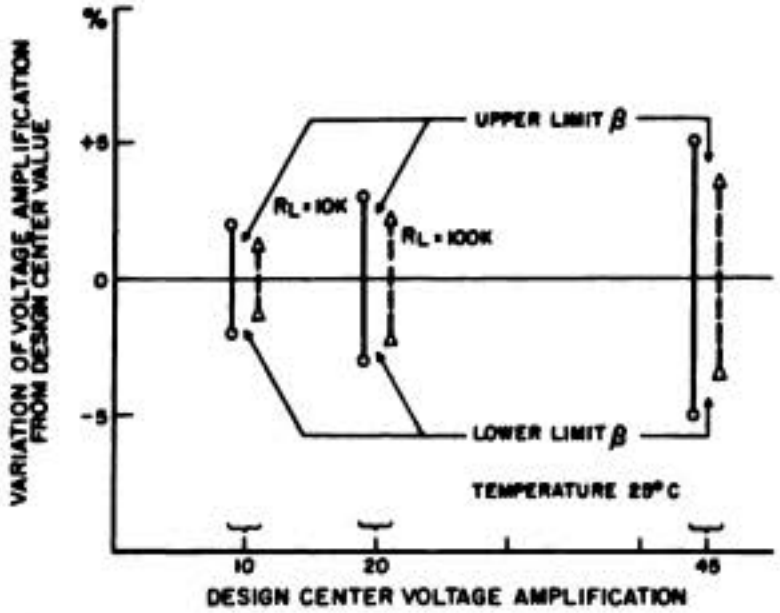


Figure 18–1.—Variation of voltage amplification from design center value with transistor replacement.

the three alternate values of voltage gain. Improved stabilization is obtained with higher values of load resistance. Replacement of transistor Q2 has considerably more effect on the voltage amplification than replacement of Q1. At 10KΩ load and R5=100Ω, maximum amplification variation with replacement of Q1 is only ±0.5%.

The maximum variation of voltage amplification with temperature is given in Figure 18–2 for the three alternate values of voltage amplification. Here again, improved stabilization is obtained with higher values of load resistance. Voltage amplification variation with temperature is primarily due to transistor parameter variations. Relatively few 2N333 transistors have the poor temperature characteristics shown in Figure 18–2. For the highest gain circuit, percentage variations of +2 and −6% would cover the great majority of cases with proportionately smaller changes for the lower gain circuits.

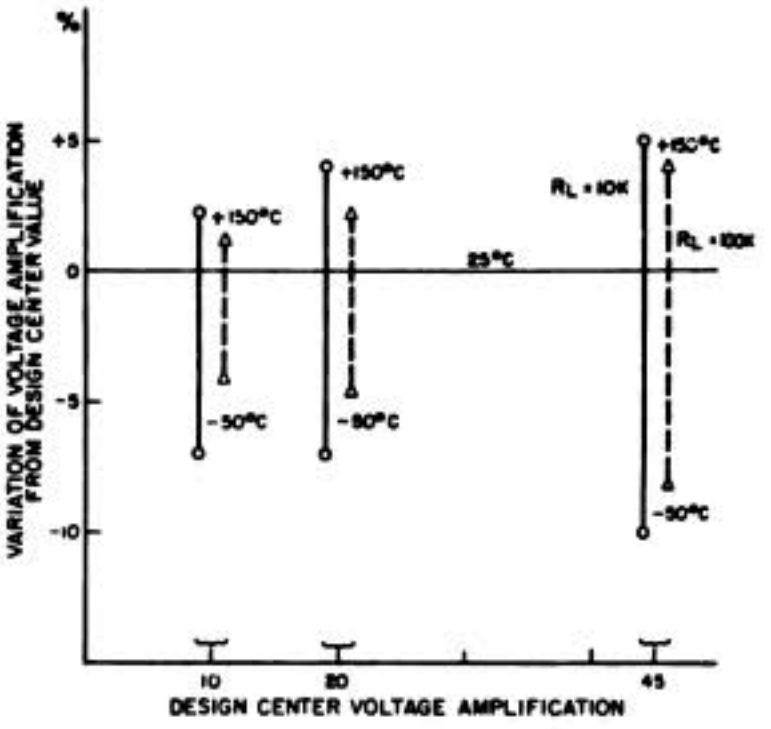


Figure 18–2.—Variation of voltage amplification from design center value with temperature.

Though the circuit will operate into loads less than 10KΩ, the voltage amplification stabilization is poor due to reduced open-loop gain. As the load resistance is increased above 10KΩ, the open-loop gain becomes larger and the stabilization of voltage amplification is

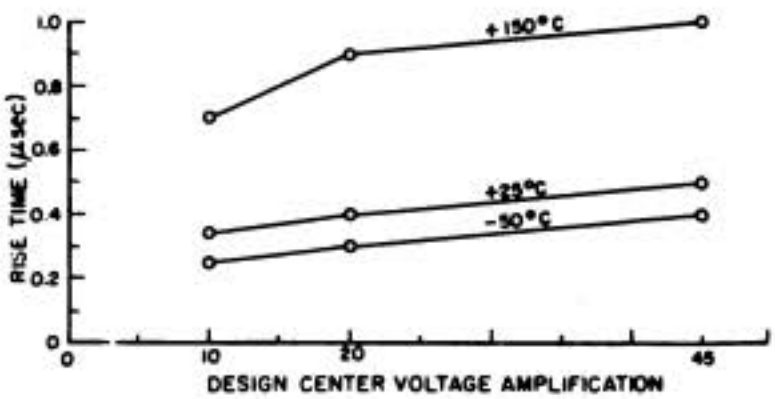


Figure 18–3.—Maximum pulse rise time as a function of temperature and design center voltage amplification.

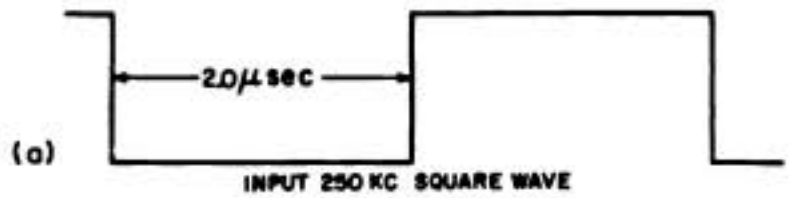


Figure 18-4—. Waveforms for two sample pairs of transistors. R5=100Ω. Output=4 volts peak to peak. Total output capacitance=30pf. Compensation for overshoot by C7.

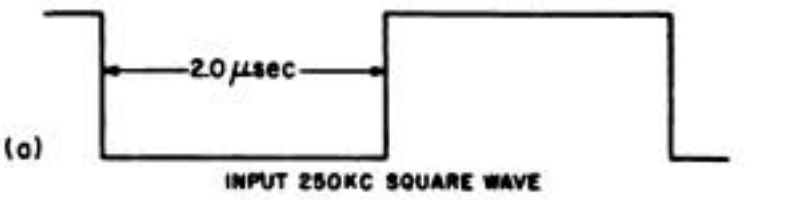


Figure 18-5.—Waveforms for two sample pairs of transistors. R5=100Ω. Output=4 volts peak to peak. Total output capacitance=30pf. No compensation for overshoot.

improved. Values of load equal to 100KΩ or larger appear as no load, beyond which the open-loop gain cannot be increased.

For R5=100Ω (voltage amplification of 45) the maximum droop, occurring at low temperature, is 3% for a 500 μsec pulse. At reduced gain the droop decreases to 1.5% for R5=220Ω and 1.0% for R5=470Ω.

The rise time of PSC 18 will vary, depending on the transistor in the output stage and the ambient temperature. Rise times given on the circuit sheet and in Figure 18-3 are the worst that may be expected.

Output waveforms at 25°C, 150°C, and −50°C for two sample pairs of transistors are shown in Figures 18-4 and 18-5. The input is a 250-kc square wave having a rise time of 0.02 μsec. The waveforms of Figure 18-4 have been compensated by C7 for overshoot, while those of Figure 18-5 are the same waveforms not compensated. The two sample pairs chosen are not intended to represent the best or worst waveforms that may be obtained.

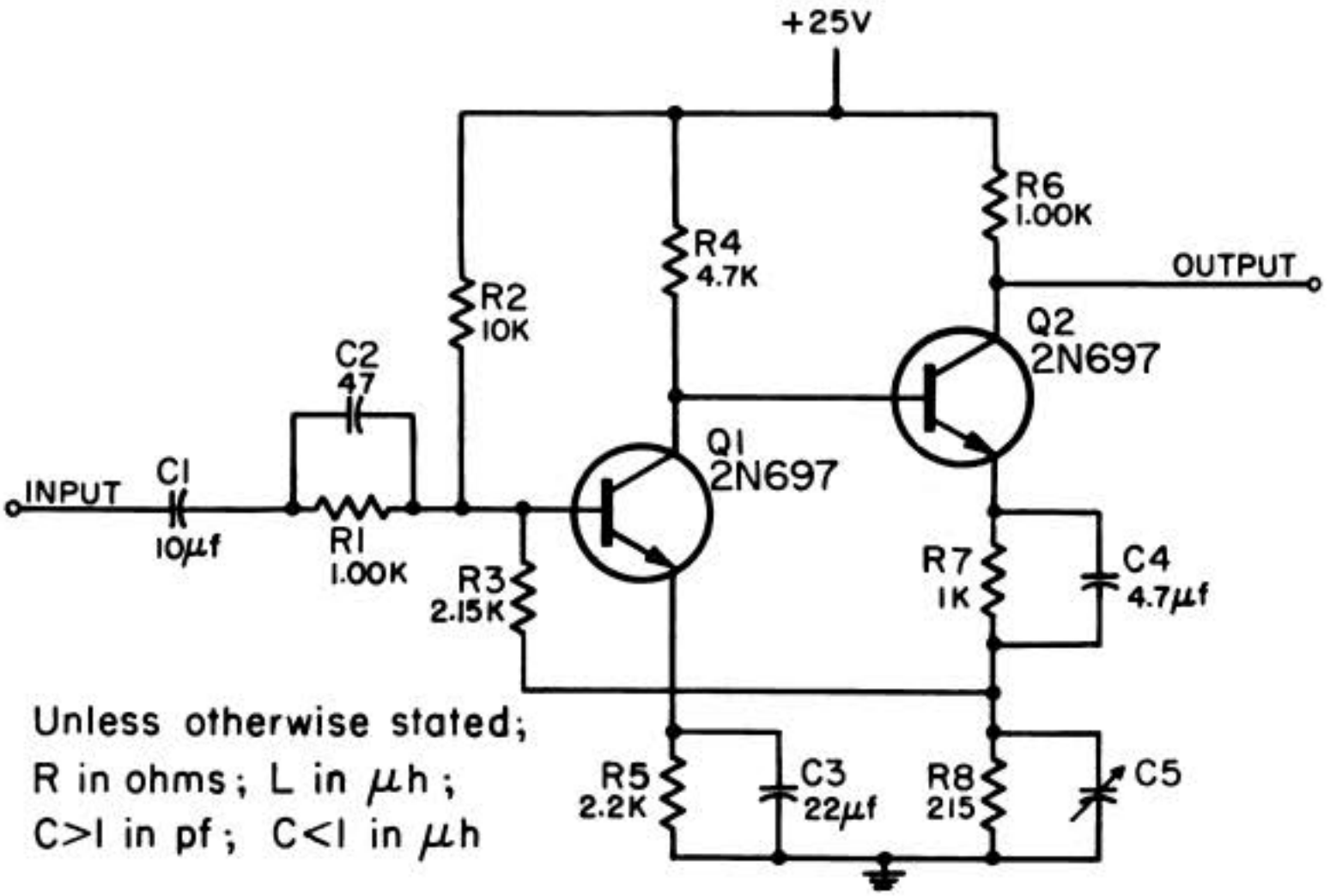
Supply voltage variations of ±10% will affect the voltage amplification by ±1%.

Notes

PREFERRED CIRCUIT NO. PSC 19
INTERMEDIATE LEVEL VIDEO AMPLIFIER

(Originally published as PC 219)

PREFERRED CIRCUIT NO. PSC 19
INTERMEDIATE LEVEL VIDEO AMPLIFIER



Components:

R1,R3,R6,R8: High stability film-type resistors.

C5: Variable 5–140 pf capacitor in parallel with a fixed capacitor to be selected in relation to external load capacitance (see Figure 19–1).

Maximum power dissipation (Note 1): R1: <10 mw; R2,R4,R8: 0.1 watt; R3: 20 mw; R5: 50 mw; R6: 0.4 watt; R7: 0.2 watt.

Capacitor dc working voltage (Note 1): C3,C4: 20 volts; C1: Dependent upon the dc voltage level present at the input terminal. The dc voltage at the junction of C1 and R1 is approximately 6 volts.

Life stability (Note 2): R1,R3,R6,R8: ±1%. C2,C5: ±2%.

Limits (these are not tolerances; see Note 3): R2,R4,R5,R7: ±10%. C1,C3,C4: +100%, −30%.

Operating characteristics:

Temperature range: −55°C to +125°C.

Signal polarity: Positive input, positive output.

Maximum input voltage: 0.6 volts.

Maximum duty factor (Note 4): 0.4.

Amplification:

Nominal (25°C): 10.5 ±5% (Note 5).

Maximum variation from 25°C value at +125°C and −55°C, respectively: +3%, −5%.

(Specifications continued on next page.)

PSC 19 INTERMEDIATE LEVEL VIDEO AMPLIFIER

1. APPLICATION

PSC 19 is a non-inverting, linear, pulse voltage amplifier for use in applications where stability of amplification over a wide temperature range is important. Minimum bandwidth and maximum output are 3 mc and 6 volts, respectively.

In a typical application, PSC 19 may follow the radar second detector; with provision for limiting large input signals, it may also act as a driver for a high-level video amplifier, such as PSC 20. In applications where intervening circuitry is not required, it may be coupled directly to PSC 20 without loss of amplification. The maximum driving voltage of PSC 19 is twice that required by PSC 20 for maximum output, hence emitter followers and/or video mixer circuits which reduce the signal level as much as 50% may be inserted between the two amplifiers, if required.

2. DESIGN CONSIDERATIONS

2.1 *Bandwidth Limitations:* Transistor video amplifiers are limited in bandwidth by either or both of two factors: (1) the variation of transistor parameter values with increasing frequency, and (2) the RC time constant of the load on each stage. Since the frequency at which parameter variation becomes important depends upon the transistor, and since factors

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Operating characteristics—*Continued*
- Output pulse characteristics:
  - Maximum amplitude: 6 volts.
  - Maximum droop for 100 μsec pulse: 2%.
  - Rise time (Note 6): 130 nsec (longest).
  - Fall time (Note 6): 100 nsec (longest).
  - Maximum overshoot: 10%.
- Terminal characteristics:
  - Maximum external load capacitance: 50 pf.
  - Resistive loading effects: See Figure 19–4.
  - Output impedance: 1KΩ.
  - Input impedance: 1KΩ in parallel with 50 pf.
- Delay: 20 to 40 nsec (start of input to start of output).

Power requirements: 25 volts ±5% at 15 ma.

NOTES:

1. The values specified are the maximum that should be encountered under any operating conditions, including those conditions applied after possible failure of one or more other components. For increased reliability, however, an additional safety factor is recommended.
2. The performance specifications are based on component values which do not deviate from nominal by more than a specified amount. For the components listed here, the initial value is less important than stability. The initial tolerance may be ±5% but the life stability (drifts from the initial value due to environmental changes or aging) must be held to the percentage specified.
3. The performance specifications are based on component values which do not deviate from nominal by more than a specified amount. For the compnoents listed here, only the total deviation from nominal is important. Thus the specified maximum deviation, termed "limits," includes initial tolerance plus drifts caused by environmental changes or aging.
4. Maximum output cannot be obtained if the input duty factor is greater than that stated.
5. 10.5 is the no-load value. Nominal amplification decreases to 10.0 at 20KΩ load and to 9.55 at 10KΩ load (see Figure 19–4). At 25°C the maximum deviation of amplification from the nominal specified is ±5% if 1% initial tolerance resistors are used for R1, R3, R6, and R8. A larger initial tolerance for the above named resistors (up to ±5% allowed) may result in a larger deviation.
6. The rise and fall times are relatively independent of external load capacitance up to 50 pf when C5 is properly selected.

that limit the extent to which the RC time constant of the load may be reduced (maximum transistor power dissipation and collector-junction barrier capacitance) also depend upon the transistor, the choice of transistor largely determines the extent and relative effect of the two bandwidth limitations.

2.2 *Selection of Transistor Types:* A silicon transistor must be used in PSC 19 because of the wide range of operating temperature. Of the high-frequency types currently available on the Military Preferred and Guidance List of Transistors (MIL–STD–701), the 2N697 has the power dissipation required at +125°C for a fast-rise 6-volt pulse output. The relative effects of the bandwidth limitations mentioned above are approximately equal for this transistor. Each will be considered in the following section.

2.3 *Increasing Bandwidth and Stability:* As pointed out previously, transistor parameter variation with increase in frequency places a limit on the maximum amplifier bandwidth. Additional parameter variation with temperature and between transistors of the same type places a limit on the stability and predictability of the amplification. Thus for a transistor amplifier to have a wide bandwidth plus stability and predictability of amplification over a wide temperature range, a large amount of negative feedback is needed to reduce the effect of parameter values on amplification. The result is a decrease in over-all circuit amplification but an increase in both bandwidth and stability.

Negative feedback in PSC 19 is applied over a common-emitter amplifier two-stage loop from the second emitter to the first base. Common-emitter stages provide the highest voltage amplification, allowing more negative feedback for a given amplification. The desirable effects of feedback are best realized when the feedback is applied over a two-stage loop. Although a given amplification can be maintained more constant if the number of stages in the feedback loop is increased, more than two stages may produce instability due to excessive phase shift. Phase correcting networks in the feedback path are cumbersome and are likely to result in loss of bandwidth.

Of the two possible negative feedback paths over a common-emitter amplifier two-stage loop, the one used offers the more desirable impedance match, since both emitter and base present a low impedance to ground. The other alternative, feedback from second-stage collector to first-stage emitter, gives the advantage of relatively high input impedance, enabling two or more loops to be cascaded for additional voltage amplification (as in PSC 18), but results in a less effective trade of amplification for bandwidth due to the loading effect on the second-stage collector.

With negative feedback applied, the major limitation on bandwidth, i.e., output pulse rise time, becomes the RC time constant of the load on transistor Q2. (The signal level at the output of Q1 is insufficient to result in significant rise time limiting.) Transistor Q2 collector-junction barrier capacitance, hereafter referred to merely as collector capacitance, or Cc, adds to wiring and external load capacitance, increasing the load time constant and resulting in a longer pulse rise time. To help reduce the time constant, R6 should be as low as possible, the value chosen being a compromise between short rise time and excessive power dissipation in Q2.

For further reduction of output rise time, peaking capacitor C5 must be added across R8. The capacitor decreases negative feedback at high frequencies, the accompanying rise in amplification canceling the fall produced by load capacitance. Since collector capacitance varies from one transistor to the next, C5 should be variable so that it can be adjusted for the particular transistors in the circuit. Too large a value produces overshoot in the output pulse and too small a value results in a longer rise time.

It should be noted that although external load resistance reduces the time constant of the load on transistor Q2 (since this resistance parallels R6 for ac signal analysis), PSC 19 is designed to feed external loads of 10KΩ or larger. External load resistance of this value will have little effect compared to the 1KΩ resistance of R6.

Figure 19–1 gives the approximate range of C5 capacitance required to adjust the output pulse for shortest rise time and minimum overshoot at various values of external load capacitance. External load resistance is assumed larger than 10KΩ. Since a variable capacitor with the wide range necessary is not sufficiently

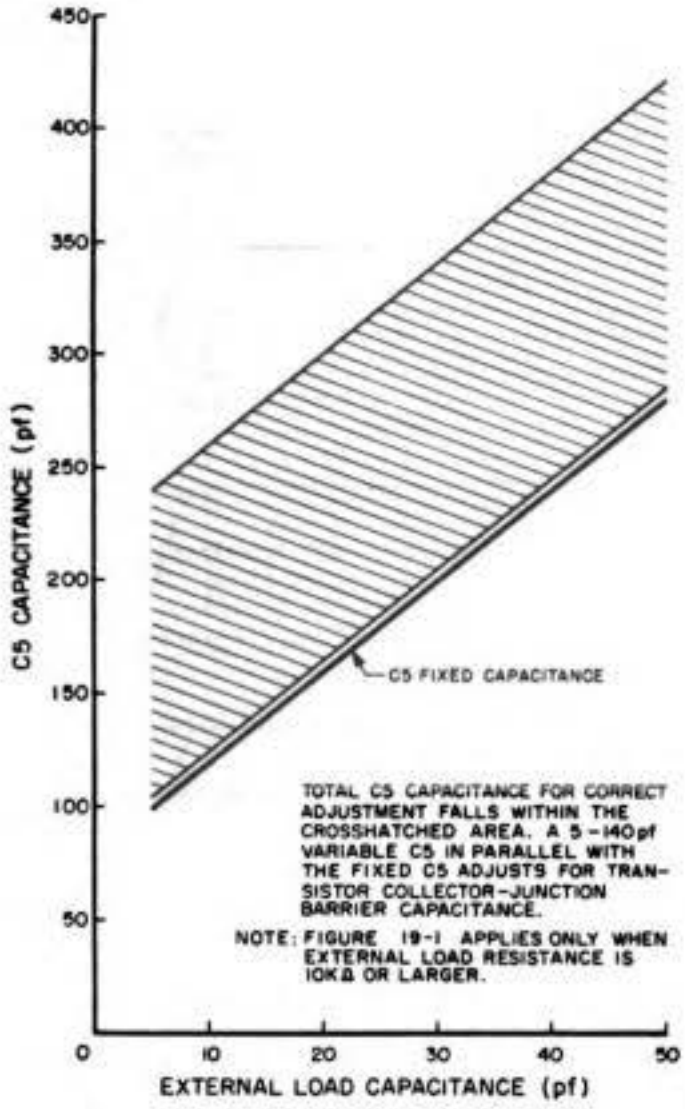


Figure 19-1.—Approximate C5 capacitance to adjust output for shortest rise time and minimum overshoot.

stable, C5 is actually a parallel combination of a fixed capacitor and a small range variable capacitor. The fixed capacitor is chosen relative to the external load capacitance (heavy solid line of Figure 19-1), which is generally known, and the variable capacitor adjusts for transistor collector capacitance, which is generally not known.

The variable capacitor may be omitted if the circuit application will tolerate rise times which may be as long as 0.25 μsec. In this case the fixed capacitor is selected relative to the external load capacitance as before, but capacitance added by the transistor is left uncompensated, thereby producing the longer rise time.

Peaking capacitor C2 frequency-compensates the input attenuator consisting of R1 and the input impedance of Q1. For correct compensation, the product of R1,C2 should equal the product of Q1 input resistance and Q1 input capacitance.

2.4 *Voltage Amplification:* PSC 19 is designed for a voltage amplification of 10, although a moderate increase or decrease may be obtained by changing the value of R1. The midband voltage amplification of a generalized feedback amplifier is given by $A=A_o/(1-bA_o)$, where A_o is the open loop amplification and b is the feedback factor. With bA_o much greater than unity, the amplification is determined by $-1/b$. For PSC 19 the feedback factor and hence circuit amplification are determined approximately by R1, R3, R6, and R8 as shown below.

$$b \approx -\frac{(R1)}{(R6)}\frac{(R8)}{(R3)}$$

$$A \approx -\frac{1}{b} \approx \frac{(R6)}{(R1)}\frac{(R3)}{(R8)}$$

Each of these resistors must have stability against environmental changes and aging of $\pm 1\%$ or better to preserve the specified stability of amplification.

The initial tolerance of R1, R3, R6, and R8 determines the maximum deviation of no-load amplification at 25°C from the nominal value (10.5) specified on page 19-2. Considering the above approximate formula for determining voltage amplification, if R3 and R6 are initially 1% in excess of their nominal resistance and R1 and R8 are initially 1% below their nominal resistance, the resulting amplification will be approximately 4% in excess of the amplification computed by using nominal resistance values for R1, R3, R6, and R8. By the same reasoning, if resistors with an initial tolerance of $\pm 2\%$ are used, the resulting amplification could be 8% above or below the nominal value.

Of the resistors which determine amplification, only R1 may be changed without redesign of the circuit. Both R3 and R6 play a large part in determining dc bias conditions with R6 also affecting output pulse rise time and Q2 power dissipation. Resistor R8 largely determines the relative amplification of Q1 and Q2, this factor having been optimized in PSC 19 for best over-all amplification stability. On the other hand, R1 determines input impedance, a circuit characteristic that may be varied depending upon the application. Reducing R1 to 464Ω gives a voltage amplification of 20 and an input impedance of approximately 464Ω, satis-

factory for use with a low impedance source. The product R1C2 must remain approximately the same however, so that if R1 is reduced to, 464Ω, C2 must be increased to 100 pf.

2.5 *General:* Internally PSC 19 is dc coupled to eliminate coupling capacitors and biasing resistors, and to extend the usefulness of the two-stage negative-feedback loop to dc bias stabilization. Emitter resistors R5 and R7 provide additional single-stage dc negative feedback, so that bias stabilization is extremely good over a range of transistor betas from 20 to 300 and for a collector-base reverse current not exceeding 20 μa. These limits will not be exceeded for the 2N697 as applied in PSC 19 anywhere over the −55°C to +125°C temperature range.

Biasing for polarized input and output reduces transistor quiescent power dissipation and increases maximum output voltage from that which may be obtained with the same circuit biased for bi-polar operation. A majority of uses are expected to be satisfied by the positive input and output polarities. Negative input and output may be obtained by replacing the 2N697 with its PNP equivalent, the 2N1132, and using a negative 25-volt supply. Due to the higher collector capacitance of this transistor, peaking capacitors C2 and C5 will need to be increased in value, and the minimum bandwidth may be somewhat less than that specified for the 2N697.

Regenerative coupling may exist between stages of the amplifier if the power supply impedance is not low. A capacitor of about 8 μf between the supply line and ground will prevent oscillation at low and medium frequencies.

3. PERFORMANCE

3.1 *Pulse Response:* Typical output-pulse rise time, with C5 adjusted for the collector capacity of the particular transistors in the circuit, is 70 nsec at 25°C and 90 nsec at 125°C. Under minimum performance conditions (both Q1 and Q2 having high Cc), the rise time may be 110 nsec at 25°C and 130 nsec at 125°C. With C5 fixed and not adjustable for transistor collector capacitance, the output rise time may be as long as 250 nsec. In either case, whether C5 is variable or not, external load capacitance has negligible effect on either rise or fall time, provided C5 is selected according to Figure 19–1.

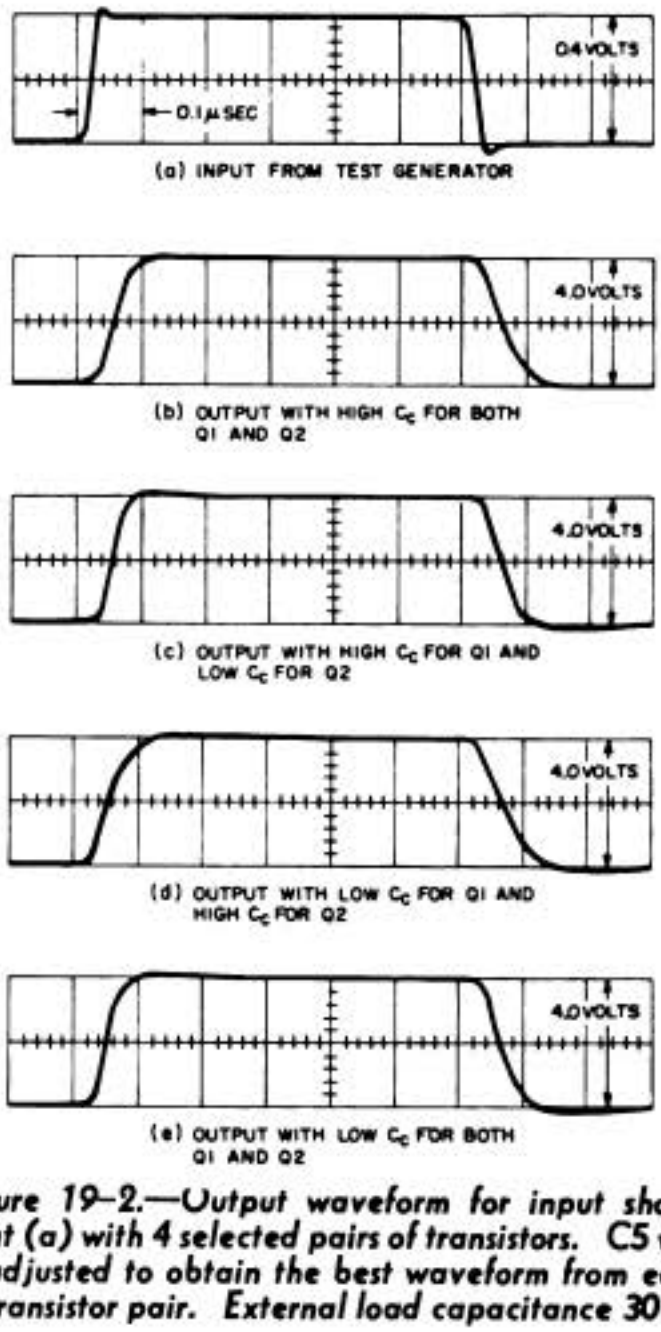


Figure 19–2.—Output waveform for input shown at (a) with 4 selected pairs of transistors. C5 was adjusted to obtain the best waveform from each transistor pair. External load capacitance 30 pf.

Figure 19–2 shows a 4-volt output from PSC 19 for each of four selected pairs of transistors (waveforms b, c, d, and e). The transistors were selected to obtain a range of collector capacitance. External load capacitance is equal to 30 pf and C5 is adjusted for best waveform with each pair. The input from the test generator is shown by waveform (a). The time relationship between the waveforms is correct, so that the time delay from start of the input to start of the output may be determined from the figure. Figure 19–3 shows the output waveforms from the same four selected pairs of transistors when C5 is fixed at 220 pf, a value slightly larger than that suggested by Figure 19–1 to compensate for an external load capacitance of 30 pf. Waveform (b) of Figure 19–3 indicates the increased rise time resulting with high Cc for both Q1 and Q2. Waveform (e) shows the slight overshoot

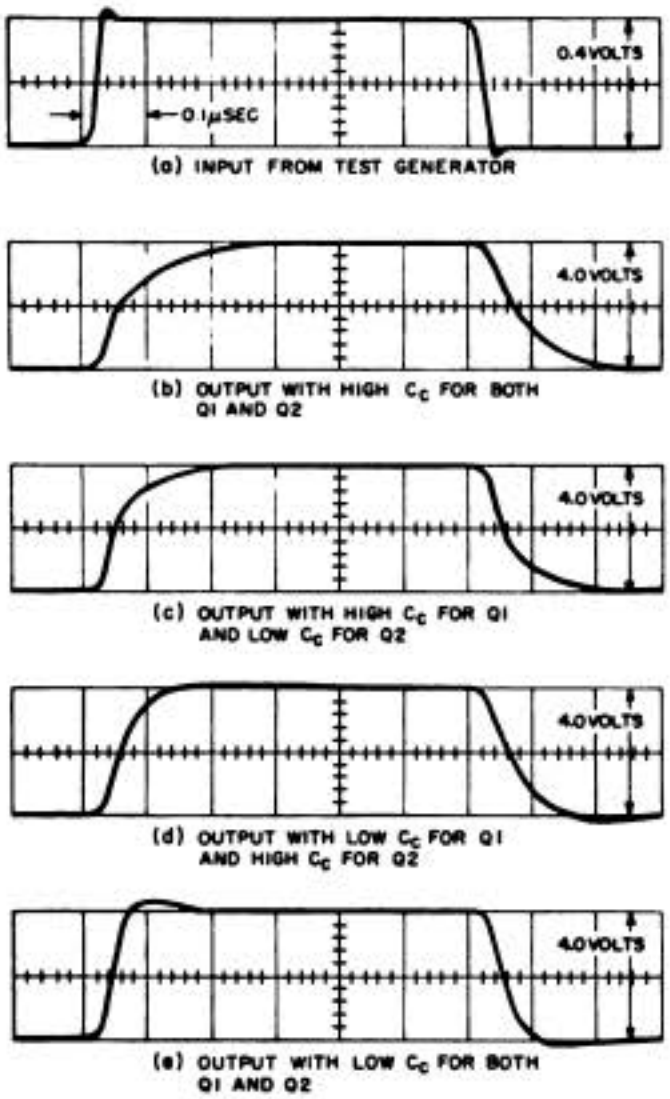


Figure 19–3.—Output waveform for input shown at (a) with 4 selected pairs of transistors. C5 fixed at 220 pf, external load capacitance 30 pf.

resulting with the Cc of both Q1 and Q2 at a low value. In waveform (c), the Cc of Q1 is high and that of Q2 is low, while in waveform (d) the reverse is true.

Output pulse fall time is generally equal to or less than rise time. Temperature effects on output waveshape are limited to a possible slight increase in rise or fall times at high temperature. Output voltage level has very little effect on pulse response.

Percentage droop depends upon the value of capacitors C1, C3, and C4. Larger capacitance results in less droop, although the point of diminishing return has been reached with the values chosen.

3.2 *Amplification and Maximum Output:* Nominal amplification (amplification at 25°C with design center component values) depends somewhat upon the external load resistance as shown by Figure 19–4. The nominal amplification at no load is 10.5; at 20KΩ load, 10.0; and at 10KΩ load, 9.55. Load resistance less than 10KΩ is not recommended because amplification begins to decrease more rapidly with load, and because maximum output voltage may be limited to less than 6 volts at higher operating temperatures. With load resistance 10KΩ or larger, an output of at least 6 volts may be obtained under any operating conditions.

It should be noted that amplification at 25°C may vary from the nominal values specified in Figure 19–4 by an amount that depends upon the initial tolerance of resistors R1, R3, R6, and R8 (see Section 2.4). If 1% resistors are used and each is off 1% from its nominal value, a 4% difference between the actual and specified voltage amplification is possible. The ±5% tolerance specified on page 19–2 includes possible detrimental effects of transistor betas which are at the high or low end of their specified range.

No matter what the 25°C amplification, however, its maximum variation at the temperature extremes of +125°C and −55°C will be +3% and −5%, respectively. In many cases, the percentage variation with temperature will be considerably less. Supply voltage variation no greater than ±5% has negligible effect on amplification.

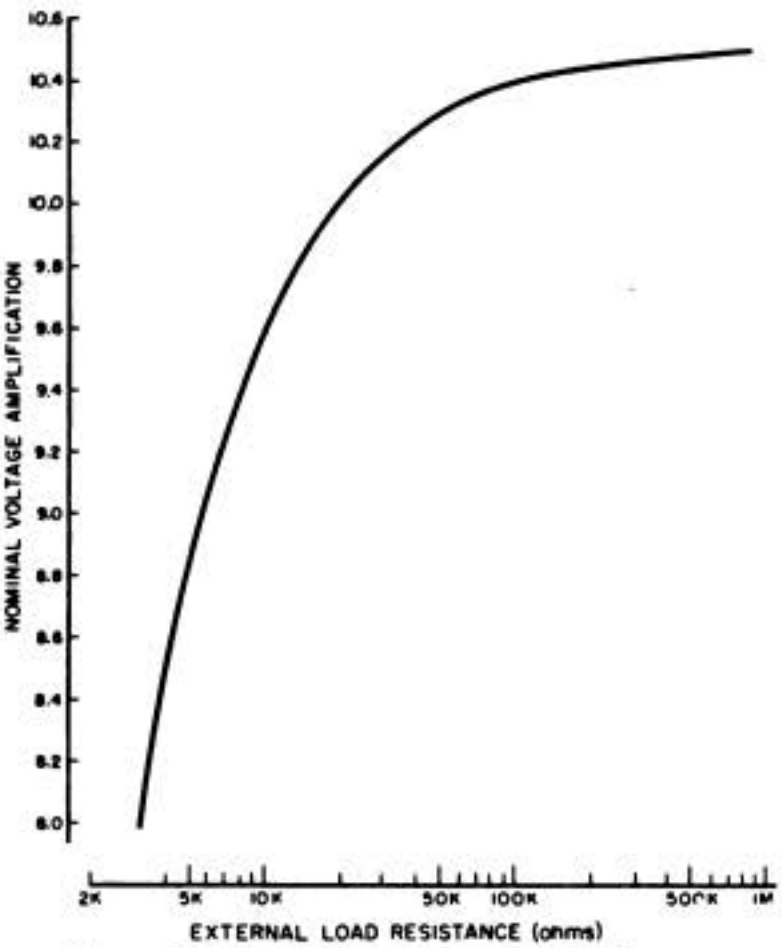


Figure 19–4.—Effect of resistive loading on amplification.

3.3 *Input Voltage Limits:* The maximum input voltage is determined by the maximum output obtainable from the circuit. An input voltage larger than that specified (approximately 0.6 volt) will cause PSC 19 to become partially paralyzed, increasing both pulse length and pulse fall time. If limiting is desired, it must be accomplished before the signal is fed to PSC 19.

No definite limit is placed on minimum input voltage, since PSC 19 is not intended as a low-level amplifier, and an accurate limit would require extensive measurement of amplifier noise figure plus a knowledge of source noise and power-supply ripple. An estimate of minimum input voltage was obtained by measuring the output noise with the input terminals open and the supply voltage furnished by a battery. The output noise was less than 1 mv, and therefore the minimum discernible input was conservatively estimated to be 100 μvolts, assuming a signal source with negligible noise.

3.4 *General:* Source impedance should be low for optimum performance. The input impedance of PSC 19 is approximately 1KΩ and is determined primarily by the resistance of R1. Thus the stability of the input impedance depends on the stability of R1.

Cascading of intermediate-level video amplifiers is possible, but because the IKΩ input impedance of one unit loads the output of the preceding one, the voltage amplification per unit will decrease to 5 for all units except the last. The pulse response of the final unit will be degraded somewhat due to its relatively large source impedance, i.e., the 1KΩ output impedance of the preceding unit. For all units except the last, the peaking capacitor, C5, will need to be reduced thirty to fifty percent from

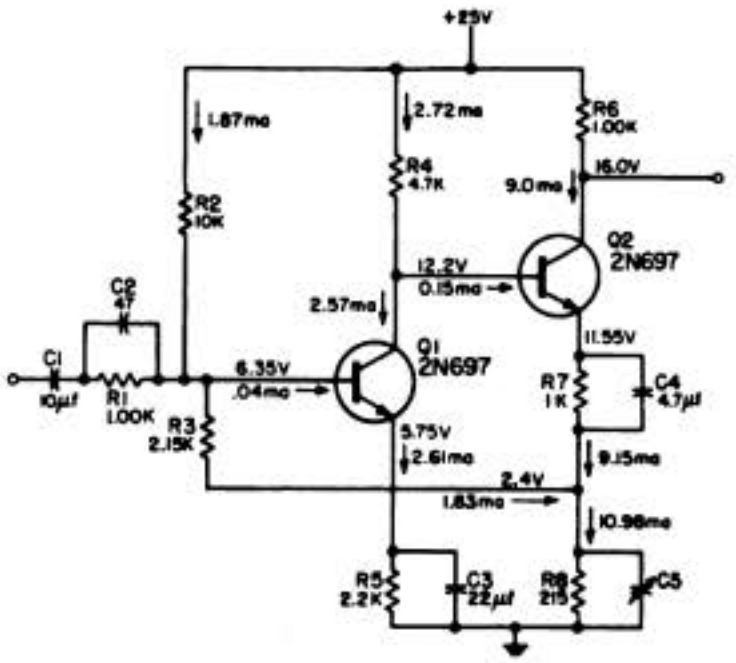


Figure 19–5.—Typical dc voltages and currents.

the value determined from Figure 19–1 since the figure applies only when the external load resistance is 10K or larger. Two cascaded amplifiers feeding a load of 10KΩ or larger will have an approximate voltage amplification of 50, a 6-volt maximum output, and a 2.5 mc minimum bandwidth.

PSC 19 may be cascaded with high-level video amplifier PSC 20 without loss of amplification or bandwidth, giving an over-all voltage amplification of 200 and minimum bandwidth of 3 mc for the two circuits. When PSC 19 external load capacitance is determined by the input of PSC 20, the fixed value of C5 should equal approximately 220 pf.

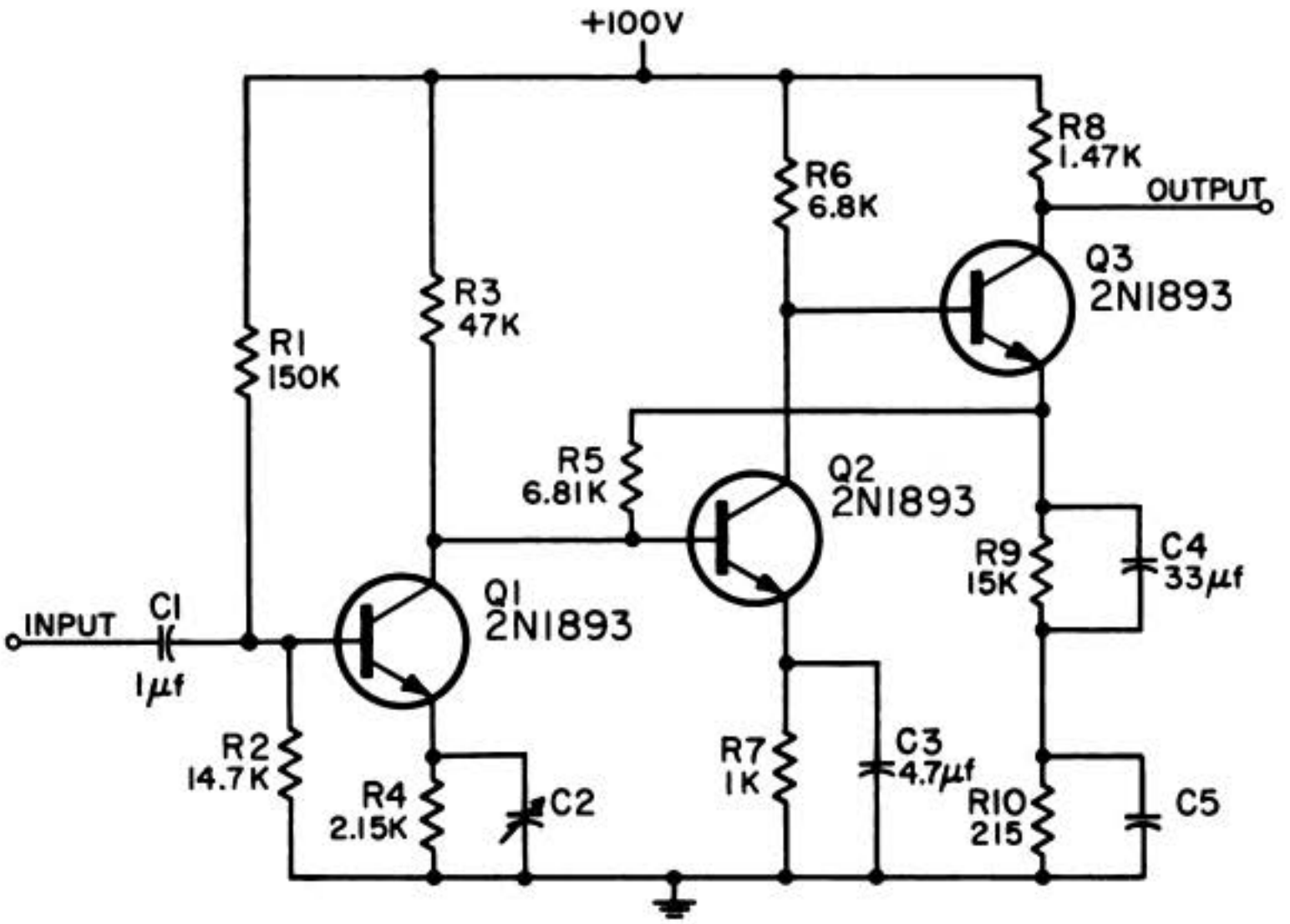
For convenience in trouble shooting, typical quiescent dc voltages and currents are given in Figure 19–5. Voltages and collector currents are practically independent of transistor beta. Base currents are shown for a transistor beta approximately equal to 60.

Notes

PREFERRED CIRCUIT NO. PSC 20
HIGH LEVEL VIDEO AMPLIFIER

(Originally published as PC 220)

PREFERRED CIRCUIT NO. PSC 20
HIGH LEVEL VIDEO AMPLIFIER



Unless otherwise stated: R in ohms; C>1 in pf; C<1 in μf; L in μh

Components:

Q2,Q3: Mounted on heat sink of thermal resistance not greater than 50°C/watt (Note 1).

R2,R4,R5,R8,R10: High stability film-type resistors.

C2: Variable 7–45 pf capacitor in parallel with a fixed 33 pf capacitor.

C5: Selected in relation to external load capacitance (see Figure 20–1).

Maximum power dissipation (Note 2): R1,R4,R5: 0.1 watt; R2: <10 mw; R3, R8: 0.25 watt; R6: 2.0 watts; R7,R9: 0.5 watt; R10: 50 mw.

Capacitor dc working voltage (Note 2): C3,C4: 35 volts; C1: Dependent upon the dc voltage level present at the input terminal. The dc voltage at the base of Q1 is approximately 8 volts.

Life stability (Note 3): R2,R4,R5,R8,R10: ±1%. C2,C5: ±2%.

Limits (these are not tolerances; see Note 4): R1,R3,R6,R7: ±6%; R9: ±20%. C1,C3,C4: +100%, −30%.

(Specifications continued on next page.)

Operating characteristics:
- Temperature range: −55°C to +125°C.
- Signal polarity: Positive input, negative output.
- Maximum input voltage: 3 volts.
- Maximum duty factor (Note 5): 0.1.
- Amplification:
  - Nominal (25°C): 20.5±5% (Note 6).
  - Maximum variation from 25°C value at +125°C and −55°C, respectively: +5%, −10%.
- Output pulse characteristics:
  - Maximum amplitude: 55 volts.
  - Maximum droop for 100 μsec pulse: 4%.
  - Rise time (Note 7): 100 nsec (longest).
  - Fall time (external load capacitance=30 pf): 150 nsec.
  - Maximum overshoot: 10% (Note 8).
- Terminal characteristics:
  - Maximum external load capacitance: 30 pf.
  - Output impedance: 1.5KΩ.
  - Input impedance:
    - Nominal (25°C): 12.3KΩ ±10% in parallel with 37 pf ±20%.
    - Maximum variation from 25°C value at temperature of +125°C and −55°C, respectively:
      R: +6%, −12%; C: +20%, −20%.
- Delay: 20 to 40 nsec (start of input to start of output).

Power requirements: 100 volts ±5% at 20 ma.

NOTES:

1. The heat sink provides for a dissipation of 400 mw at 125°C ambient.

2. The values specified are the maximum that should be encountered under any operating conditions, including those conditions applied after possible failure of one or more other components. For increased reliability, however, an additional safety factor is recommended.

3. The performance specifications are based on component values which do not deviate from nominal by more than a specified amount. For the components listed here, initial value is less important than stability. The initial tolerance may be ±5%, but the life stability (drifts from the initial value due to environmental changes or aging) must be held to the percentage specified.

4. The performance specifications are based on component values which do not deviate from nominal by more than a specified amount. For the components listed here, only the total deviation from nominal is important. Thus the specified maximum deviation, termed "limits", includes initial tolerance plus drifts caused by environmental changes or aging.

5. If the input duty factor is greater than that stated, maximum output cannot be obtained, and the power dissipation of Q3 may be exceeded at high temperature.

6. 20.5 is the no-load value. Nominal amplification decreases to 20.0 at 60KΩ load and to 19.1 at 20KΩ load. The maximum deviation of amplification at 25°C from the nominal specified is ±5% if 1% initial tolerance resistors are used for R4, R5, R8, and R10. A larger initial tolerance for the above named resistors (up to ±5% allowed) may result in a larger deviation.

7. The rise time is relatively independent of external load capacitance up to 30 pf if C5 is properly selected.

8. This figure assumes suppression of positive overshoot at trailing end of pulse (see Section 2.4).

PSC 20 HIGH LEVEL VIDEO AMPLIFIER

1. APPLICATION

PSC 20 is a linear pulse voltage amplifier with a minimum bandwidth of 3 mc, designed primarily for use as a CRT intensity modulation device in applications where stability of amplification over a wide temperature range is important. The circuit is designed for positive input pulses and will give a maximum negative output of 55 volts.

In a typical application PSC 20 may be driven by an intermediate-level video amplifier such as PSC 19. Because of its relatively high input impedance (10KΩ minimum), it may be connected directly to the output of PSC 19 without reducing the amplification of that circuit. Since the maximum driving voltage of PSC 19 is twice that required by PSC 20 for maximum output, emitter followers and/or video mixer circuits which reduce the signal level as much as 50% may be inserted between the two amplifiers, if required.

In some radar applications, signals direct from the second detector, when amplified by PSC 20, are sufficient to drive the CRT. Impedance matching may be necessary, however, and provision must be made for limiting the input signal to less than 3 volts.

2. DESIGN CONSIDERATIONS

2.1 *Bandwidth Limitations:* Transistor video amplifiers are limited in bandwidth by either or both of two factors: (1) the variation of transistor parameter values with increasing frequency, and (2) the RC time constant of the load on each stage. Since the frequency at which parameter variation becomes important depends upon the transistor, and since factors that limit the extent to which the RC time constant of the load may be reduced (maximum transistor power dissipation and collector-junction barrier capacitance) also depend upon the transistor, the choice of transistor largely determines the extent and relative effect of the two bandwidth limitations.

2.2 *Selection of Transistor Type:* A silicon transistor must be used in PSC 20 because of the wide range of operating temperatures. Of the high-frequency types currently available on the Military Preferred and Guidance List of Transistors (MIL–STD–701), the 2N1893 has both the voltage rating and available power dissipation required for a high-level output at 125°C. It is used in all three stages, although a 2N697 could be used in Q1 and Q2 where the voltage levels during normal operation do not exceed the voltage rating of this transistor. Should Q3 become open-circuited, however, the maximum breakdown voltage of a 2N697 in Q2 would be greatly exceeded. The same consideration applies for a 2N697 in Q1, should Q2 become open-circuited. Thus use of the 2N1893 in all three stages guards against possible multiple transistor failure. The relative effects of the two bandwidth limitations mentioned in the preceding section are approximately equal for this transistor. Each will be considered in the following section.

2.3 *Increasing Bandwidth and Stability:* As pointed out previously, transistor parameter variation with increase in frequency places a limit on the maximum amplifier bandwidth. Additional parameter variation with temperature and between transistors of the same type places a limit on the stability and predictability of the amplification. Thus for a transistor amplifer to have a wide bandwidth plus stability and predictability of amplification over a wide temperature range, a large amount of negative feedback is needed to reduce the effect of parameter values on amplification. The result is a decrease in over-all circuit amplification, but an increase in both bandwidth and stability.

Negative feedback is applied over a common-emitter amplifier two-stage loop from the emitter of the second stage in the loop (Q3) to the base of the first stage in the loop (Q2). Input stage Q1 is added to provide signal inversion (impossible to accomplish using two-stage common-emitter feedback loops) and relatively high input impedance, both of which are necessary if the circuit is to satisfy a majority of its applications and be compatible with PSC 19.

Common-emitter stages are used in the feedback loop because they provide the highest voltage amplification per stage, allowing more negative feedback for a given amplification. The desirable effects of feedback are best realized when the feedback is applied over a two-stage

loop. Although a given amplification can be maintained more constant if the number of stages in the feedback loop is increased, more than two stages may produce instability due to excessive phase shift. Phase-correcting networks in the feedback path are cumbersome and are likely to result in loss of bandwith.

Of the two possible negative feedback paths over a common-emitter amplifier two-stage loop, the one used not only presents the more desirable impedance match, since both emitter and base present a low impedance to ground, but lends itself more readily for use with an input inverting stage. The other alternative, feedback from second-stage collector to first-stage emitter, produces relatively high input impedance, but the trade of amplification for bandwidth is less effective due to loading of the output stage collector.

A large amount of single-stage feedback in Q1, introduced by emitter resistor R4, provides the required high input impedance and practically eliminates any effect of Q1 transistor parameters on circuit amplification.

With negative feedback applied, the major limitation on bandwith, i.e., output pulse rise time, becomes the RC time constant of the transistor load. Transistor collector-junction barrier capacitance, hereafter referred to merely as collector capacitance, or Cc, adds to wiring and external load capacitance, increasing the time constant of the load and resulting in a longer pulse rise time. To help reduce the time constants of the loads on Q2 and Q3, R6 and R8 should be as low as possible. The values chosen are a compromise between short rise time and excessive power dissipation in these transistors.

For further reduction of output rise time, peaking capacitors C2 and C5 must be added across R4 and R10, respectively. These capacitors decrease negative feedback at high frequencies, the accompanying rise in amplification canceling the fall produced by load capacitance. C2 compensates mainly for the collector capacitance of Q1, while C5 compensates for external load capacitance and the collector capacitance of Q3. Either C2 or C5 will compensate for the collector capacitance of Q2. Since collector capacitance varies from one transistor to the next, ideally both C2 and C5 should be variable so that they can be adjusted for the particular

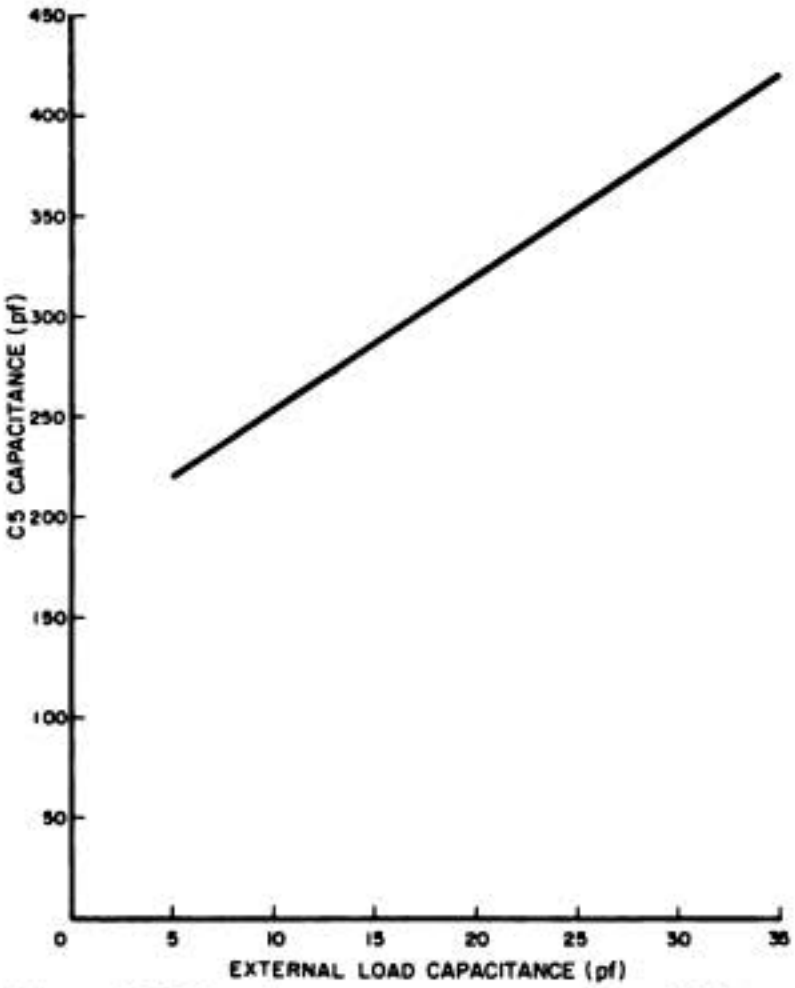


Figure 20–1.—Approximate capacitance of C5 required to adjust the output pulse for shortest rise time and minimum overshoot.

transistors in the circuit. However, equally good results are obtained if C5 is a fixed capacitor selected according to the approximate external load capacitance (see Figure 20–1), and if C2 is variable to compensate for different values of Q1, Q2, and Q3 collector capacitance.

To enable adjustment for the range of collector capacitance encountered with the 2N1893, C2 should be variable between approximately 40 and 80 pf. To reduce possible adjustment error, C2 is actually a parallel combination of a fixed 33 pf capacitor and a variable 7–45 pf capacitor.

2.4 *Overshoot:* Positive overshoot following the trailing edge of the output pulse is generated by the discharge of peaking capacitors C2 and C5 after termination of the input pulse. If this overshoot (see Figure 20–2a) is detrimental to operation of associated circuitry, it may be reduced (see Figure 20–2b) by addition of a capacitor and forward-biased diode in series from output terminal to ground. A capacitor with a value of 4 μf or larger should be used with a diode having low capacitance and a reverse voltage rating of at least 100 volts.

2.5 *Input Resistance:* Input resistance is approximately equal to bias resistors R1 and R2 in parallel with $h_{ie_1}+\beta_1 R4$, where h_{ie_1} and β_1 are small-signal parameters indicating the input resistance and current amplification, respectively, of Q1. If we neglect h_{ie_1}, which is

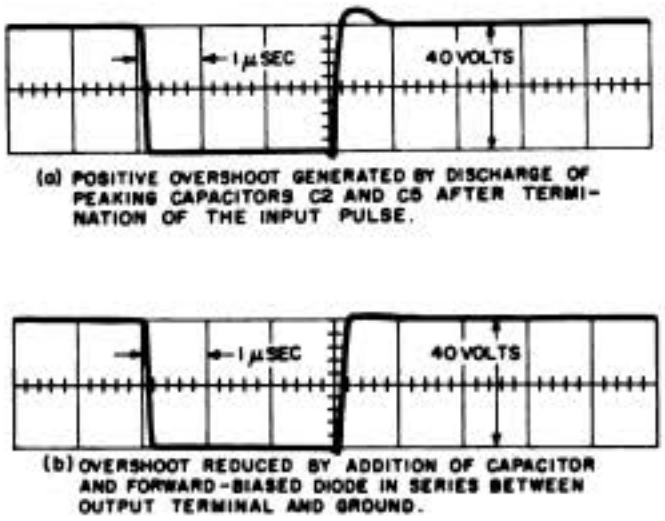


Figure 20–2.—Typical output waveforms.

generally equal to only a few hundred ohms, the input resistance becomes

$$R_{in} \approx \frac{1}{\frac{1}{\beta_1 R4}+\frac{R1+R2}{R1R2}}.$$

Resistor R4 is large enough so that $1/\beta_{1\,min}$ R4 is much smaller than (R1+R2)/R1R2. Variations of input resistance due to Q1 beta variation with temperature are thus greatly reduced. Stability of input resistance with temperature depends primarily upon the stability of R1 and R2 in parallel. Since R2 is considerably smaller, its stability against environmental changes is the controlling factor.

2.6 *Voltage Amplification:* PSC 20 is designed for a voltage amplification of 20. The midband voltage amplification of a generalized feedback amplifier is given by

$$A=\frac{A_o}{1-bA_o},$$

where A_o is the open loop amplification, and b is the feedback factor. With bA_o much greater than unity, the amplification is determined by $-1/b$. For PSC 20, the feedback factor and hence the circuit amplification are determined approximately by R4, R5, R8, and R10 as shown below.

$$b \approx -\left(\frac{R4}{R8}\right)\left(\frac{R10}{R5}\right)$$

$$A \approx -\frac{1}{b} \approx \left(\frac{R8}{R4}\right)\left(\frac{R5}{R10}\right)$$

Each of these resistors must have stability against environmental changes and aging of ±1% or better to preserve the specified stability of amplification.

The initial tolerance of R4, R5, R8, and R10 determines the maximum deviation of no-load amplification at 25°C from the nominal value (20.5) specified on page 20–3. Considering the above approximate formula for determining voltage amplification, if R5 and R8 are initially 1% in excess of their nominal resistance and R4 and R10 are initially 1% below their nominal resistance, the resulting amplification will be approximately 4% in excess of the value computed by using the nominal resistance values for R4, R5, R8, and R10. By the same reasoning, if resistors with an initial tolerance of ±2% are used, the resulting amplification could feasibly be ±8% above or below the nominal value.

None of the resistors which determine amplification may be changed without redesign of the circuit. Resistors R4, R5, and R8 play a large part in determining dc bias conditions, with R8 also affecting output-pulse rise time and Q3 power dissipation. Resistor R10 largely determines the relative amplification of Q2 to Q3, this factor having been optimized for best overall amplification stability.

2.7 *General:* Internally PSC 20 is dc coupled to eliminate coupling capacitors and biasing resistors and to extend the usefulness of the two-stage negative feedback loop to dc bias stabilization. Emitter resistors R4, R7, and R9 provide additional single-stage dc negative feedback so that bias stabilization is extremely good over a range of betas from 20 to 300 and for a collector-base reverse current not exceeding 100 μa. These limits will not be exceeded for the 2N1893 as applied in PSC 20 anywhere over the −55°C to +125°C temperature range.

Biasing for polarized input and output reduces transistor quiescent power dissipation

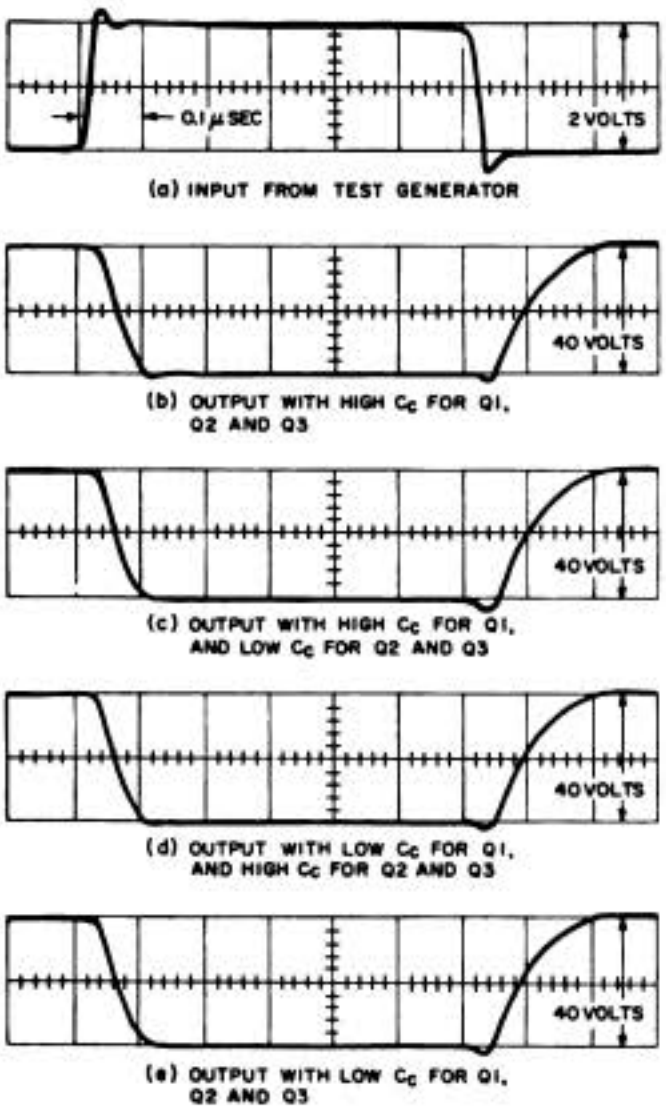


Figure 20–3.—Output waveform for input shown at (a) with 4 selected combinations of transistors. C2 was adjusted to obtain the best waveform from each combination. External load capacitance 30 pf, C5, 390 pf.

and increases maximum output voltage over that which may be obtained with the same circuit biased for bi-polar operation. A majority of uses are expected to be satisfied by the positive input and negative output polarities. In addition, biasing the output stage for negative polarity significantly reduces the quiescent current drawn from the power supply. Output stage Q3 biased for an equally large positive output, with the time constant of the load unchanged, would draw up to 50 ma quiescent current.

Regenerative coupling may exist between stages of the amplifier if the power supply impedance is not low. A capacitor of about 8 μf between the supply line and ground will prevent oscillation at low and medium frequencies.

3. PERFORMANCE

3.1 *Pulse Response:* The longest output pulse rise time under minimum performance conditions is 100 nsec, with proper C5 selection for external load capacitance and C2 adjustment for the collector capacitance of the particular transistors in the circuit. Depending somewhat upon the transistors, rise times of 50 nsec to 80 nsec are typical. Output fall time is dependent upon the external load capacitance, being approximately 60 nsec for 8 pf and 1.3 μsec for 30 pf.

Figure 20–3 shows the test generator input, along with a 40-volt output for each of four selected combinations of transistors. External load capacitance is 30 pf, C5 equals 390 pf, and C2 is adjusted for best waveform with each combination. In (b) all three transistors have high Cc. In (c) the Cc of Q1 is high, while that of Q2 and Q3 is low. In (d) the Cc of Q1 is low, while that of Q2 and Q3 is high. In (e) all three transistors have low Cc.

Figure 20–4 shows what happens to the waveforms of Figure 20–3 if both C2 and C5 are

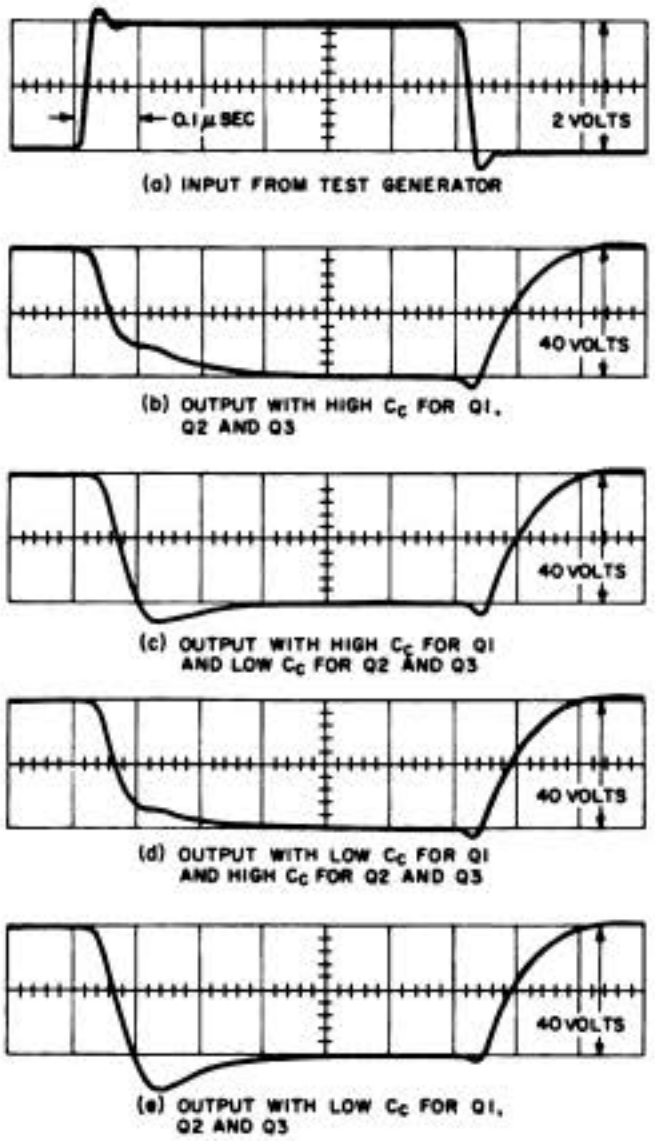


Figure 20–4.—Output waveform for input shown at (a) with 4 selected combinations of transistors. C2 fixed at 56 pf, C5, 390 pf, external load capacitance 30 pf.

fixed capacitors, in other words, when C2 is not adjustable for the Cc of the particular transistors in the circuit. For purposes of illustration, the value of the fixed C2 is chosen as 56 pf, approximately midway in the suggested range of a variable C2. With all three transistors having high Cc as in (b), the rise time is increased considerably. With all three transistors having low Cc as in (e), a considerable overshoot is noted. If the value of a fixed C2 is selected to give no overshoot for three transistors with low Cc, the rise time may be as long as 0.4 μsec with three high Cc transistors.

Output voltage level has some effect on pulse response due to the inverse variation of transitor collector capacitance with collector-to-emitter voltage. In output stage Q3 there may be considerable change in collector capacitance between low and high outputs. At low outputs, Q3 collector-to-emitter voltage is high, resulting in a low collector capacitance and faster response time. At high outputs, Q3 collector-to-emitter voltage is low, resulting in high collector capacitance and longer response time. The longest rise time specified (100 nsec) occurs at maximum output. Temperature effects on response time are generally negligible.

Percentage droop depends upon the value of capacitors C1, C3, and C4. Larger capacitance results in less droop, although the point of diminishing return has been reached with the values chosen.

3.2 *Amplification and Maximum Output:* Nominal amplification (amplification at 25°C with design center component values) is 20.5 at no-load; it decreases to 20.0 at a 60KΩ load and to 19.1 at a 20KΩ load. Since the circuit is used as a CRT intensity modulation device, however, a no-load condition is essentially realized. An output of at least 55 volts may be obtained under any operating conditions.

It should be noted that amplification at 25°C may vary from the value specified (20.5) by an amount that depends upon the initial tolerance of resistors R4, R5, R8, and R10 (see Section 2.6). If 1% resistors are used and each is off 1% from its nominal value, a 4% difference between the actual and specified nominal voltage amplification is possible. The 5% amplification tolerance specified on page 20–3 includes possible detrimental effects of transistor betas which are at the high or low end of their specified range.

No matter what the 25°C amplification, however, its maximum variation at the temperature extremes of +125°C and −55°C will be +5% and −10%, respectively. In many cases, this percentage variation with temperature will be considerably less. Supply voltage variation no greater than ±5% has negligible effect on amplification.

3.3 *Input Impedance:* The nominal value of input resistance is 12.3KΩ ±10%, with a possible variation of +6% and −12% at the temperature extremes of +125°C and −55°C, respectively. The nominal value of input capacitance is 37 pf ±20%, with a possible variation of +20% and −20% at the temperature extremes of +125°C and −55°C, respectively.

3.4 *Input Voltage Limits:* The maximum input voltage is determined by the maximum output obtainable from the circuit. An input voltage larger than that specified (approximately 3 volts) results in saturation of either or both Q1 and Q3 and in failure of the circuit to provide an output even resembling the input. If limiting is

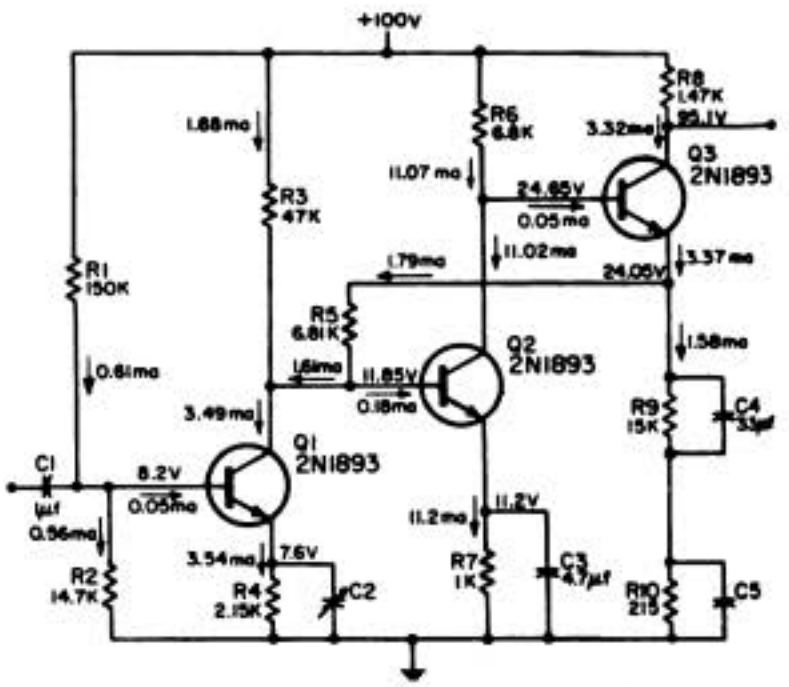


Figure 20–5.—Typical dc voltages and currents.

desired it must be accomplished before the signal is fed to PSC 20.

No definite limit is placed on minimum input voltage. The circuit was tested to have a linear input-output voltage relationship down to an input of 2 mv, a value considerably lower than necessary for the intended application.

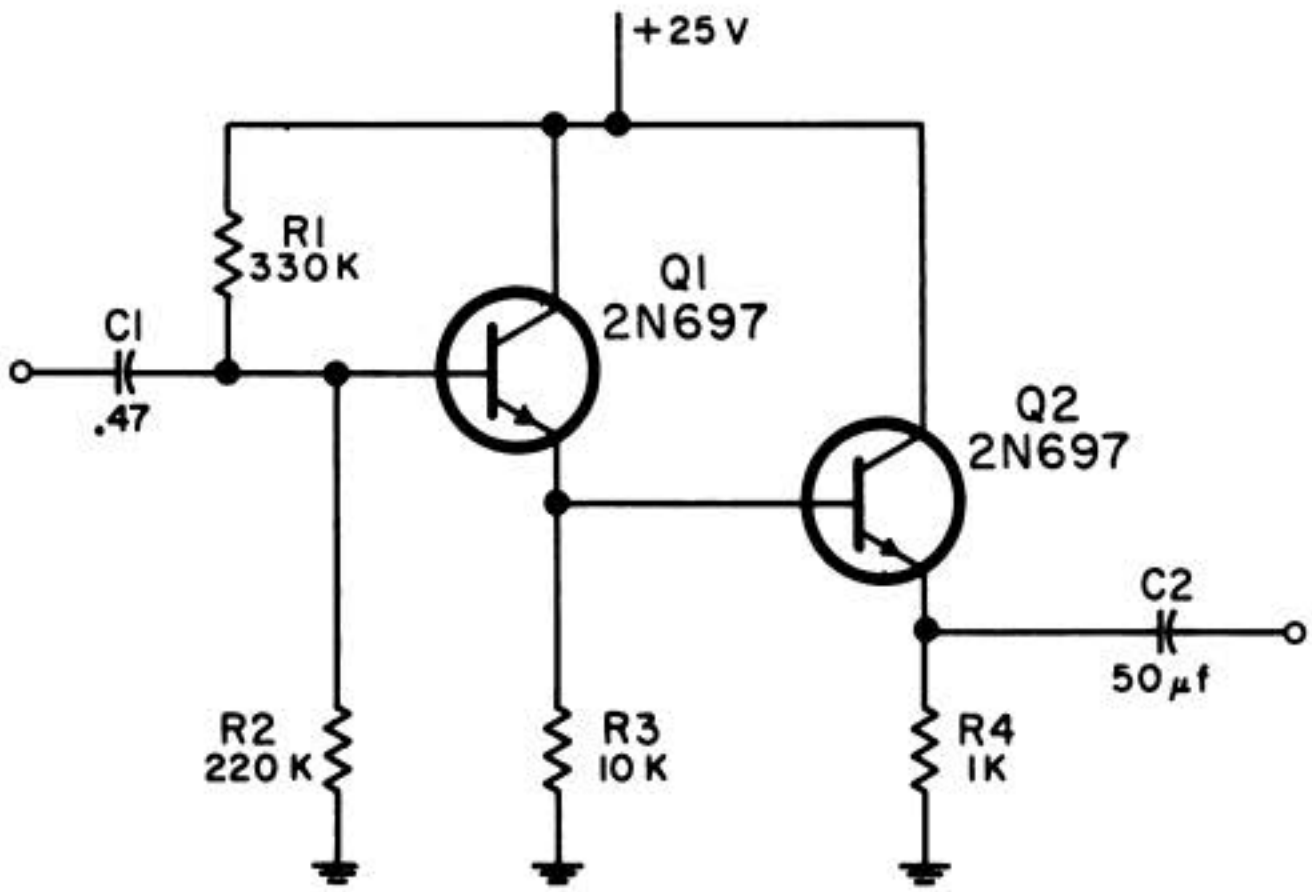
3.5 *DC Voltages and Currents:* For convenience in trouble shooting, typical quiescent dc voltages and currents are given in Figure 20–5. Voltages and collector currents are practically independent of transistor beta. Base currents are shown for a transistor beta approximately equal to 60.

Notes

PREFERRED CIRCUIT NO. PSC 21
PULSE EMITTER FOLLOWER

(Originally published as PC 221)

PREFERRED CIRCUIT NO. PSC 21
PULSE EMITTER FOLLOWER



Unless otherwise stated: R in ohms;
C>1 in pf; C<1 in μf; L in μh

Components:

Maximum power dissipation (Note 1): R1: 1 mw; R2: <1 mw; R3: 7 mw; R4: 60 mw.

Maximum capacitor voltage: C2: 8 volts; C1: select voltage rating for particular coupling application.

Limits (these are not tolerances; see Note 2): All R: ±10%. All C: ±20%.

Operating characteristics (Note 3):

Temperature range: −55°C to +125°C.

Load resistance: 100 ohms.

Input:

Resistance: 80KΩ.

Capacitance: 25 pf.

Signal polarity: Positive (Note 4).

Maximum signal amplitude: 17 volts peak (Note 5).

Voltage amplification: 0.975.

Power gain: 30 db.

Droop for 100 μsec pulse (Note 6): 2%.

Output impedance (independent of load): 2 ohms.

Maximum power requirements: 25 volts dc±10% at 8 ma.

(For Notes, see bottom of next page.)

PSC 21 PULSE EMITTER FOLLOWER

1. APPLICATION

PSC 21 is a two-stage cascaded emitter follower intended primarily as a video line driver for positive pulses. It has a nominal input impedance of about 80KΩ in parallel with 25 pf and will drive loads with impedances as low as 50 ohms. It may be modified for negative inputs by replacing Q1 and Q2 with their complementary PNP types and reversing the polarity of the collector supply. Cascading two emitter followers provides the advantages of a very high input impedance and a constant output impedance which is practically independent of the source impedance and approximately equal to the internal emitter resistance r_e.[1]

Single-stage emitter followers are used extensively for the purpose of isolation or impedance matching. These circuits are usually designed for a particular system, with the choice of transistor type and impedance levels dictated by the system requirements. While they are used extensively within a single system, they cannot be classed as preferred circuits because their applicability is limited outside the system for which they were designed. For this reason, no single-stage emitter follower is included as a preferred circuit.

[1] $R_{out} \approx r_e + \frac{R_s}{\beta_1\beta_2}$, where R_s is the source impedance, which should be less than 2KΩ for a 4 mc bandwidth, and β_1 and β_2 are the dc forward current transfer ratios of Q1 and Q2.

2. DESIGN CONSIDERATIONS

The circuit utilizes silicon, high-speed, medium-power transistors to obtain high-frequency response to video signals, adequate driving power into low impedance loads, and a wide temperature range of operation. The low output impedance, about 2 ohms, makes it possible to drive rather high capacitance loads and more than one terminated line without degrading the signal.

R1, in conjunction with R2 and R3, establishes the quiescent operating bias points. A compromise must be made between a low idling current and a high beta for the stage. The first stage is biased for class B operation with a quiescent collector current of about 0.5 ma to avoid the non-linearities and low beta that are characteristic of lower collector currents. The second stage is biased for class AB operation with a collector current of about 6 ma.

The relative stability of the first stage is 0.84 and is given by the equation

$$S_1 = \frac{\beta_1}{(\beta_1+1)+\dfrac{1}{R3/R1+R3/R2}}.$$

Perfect stabilization occurs as the expression approaches 1. As the ratios R3/R1 and R3/R2 are made large, perfect stabilization is approached; however, it is desirable to keep R1 and R2 high to minimize their shunting effect on the input impedance. The relative stability of the second stage, determined from a similar

NOTES:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. Thus the term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

3. The operating characteristics are based on operation at 25°C with a 100Ω load and on transistors with betas of 75 (see Section 3).

4. For negative inputs see Section 2.

5. The 17-volt absolute maximum input voltage is limited by the collector-to-emitter voltage of the transistor. For a particular load and duty factor it may be necessary to reduce the input voltage as described in Section 3.2.

6. The droop may be improved by increasing coupling capacitor C2. The droop in percent for any pulse width, τ, is approximately $100\tau/R_LC2$, where R_L is the load resistance.

equation, is about 0.90. The operating point of Q2 is determined by R4 and the voltage drop across R3.

The fall time of the output signal increases with signal amplitude and increased output capacitance. The response of the circuit to the negative-going trailing edge of the input waveform is slower than it is to the positive-going leading edge because transistor Q2 tends to turn off and increase the effective output impedance during the fall of the pulse. The fall time can be slightly improved by returning emitter resistor R4 to a negative supply. The circuit may be adapted to negative-going signals by replacing Q1 and Q2 with their complementary PNP type, 2N1132, and by reversing the collector supply polarity.

3. PERFORMANCE

The circuit will retain its operating point and performance characteristics (except for input impedance) throughout a large beta spread. The voltage amplification will remain well above 0.90 for loads down to 50 ohms.

3.1 *Input Impedance:* The input impedance is a function of the load and is highly dependent upon transistor beta, which, in addition to the three-to-one spread in acceptance limits, may vary 50% at the extremes of the temperature range from its value at 25°C. The load impedance, R_L, is transferred through Q2 and appears across R3 in the form of $\beta_2 R_L$. This parallel combination, multiplied by β_1, gives the input impedance of Q1 which is shunted by R1 and R2 and by the input capacitance, which is about 25 pf. Because of the shunting effect of the input capacitance, the source impedance should not exceed 2KΩ to preserve at least a 4 mc bandwidth.

The 80KΩ input impedance specified in the performance specifications (p. 21–2) is based on operation at 25°C with a 100Ω load and on transistors with betas of 75, which is a typical value for the 2N697. A total beta spread from 20 to 180 may be expected from the 2N697 due to random choice and an operating temperature range from −55°C to +125°C. For a beta of 20 and the lowest specified load resistance, 50 ohms, the input impedance will fall to 16KΩ. If a source impedance of 2KΩ is used to preserve the bandwidth, the change in signal amplitude caused by changes in input impedance will be less than 10% for any load specified for PSC 21 and for any 2N697 within MIL acceptance limits.

3.2 *Input Voltage:* Three factors limit the maximum amplitude of the input signal: the collector-to-emitter voltage of each stage, the average and instantaneous power dissipation in each of the transistors, and the effect of the output coupling circuit on the bias of the output stage. The latter is usually the limiting factor for loads less than 150 ohms and duty factors above approximately 0.05. At lower duty factors or higher loads the 17-volt collector-to-emitter voltage of Q1 and Q2 limits the peak voltage of the signal.

The effect of the output coupling circuit on the bias of the final stage is a function both of the signal amplitude and of the duty factor. The positive output pulse adds charge to coupling capacitor C2. During the interval between

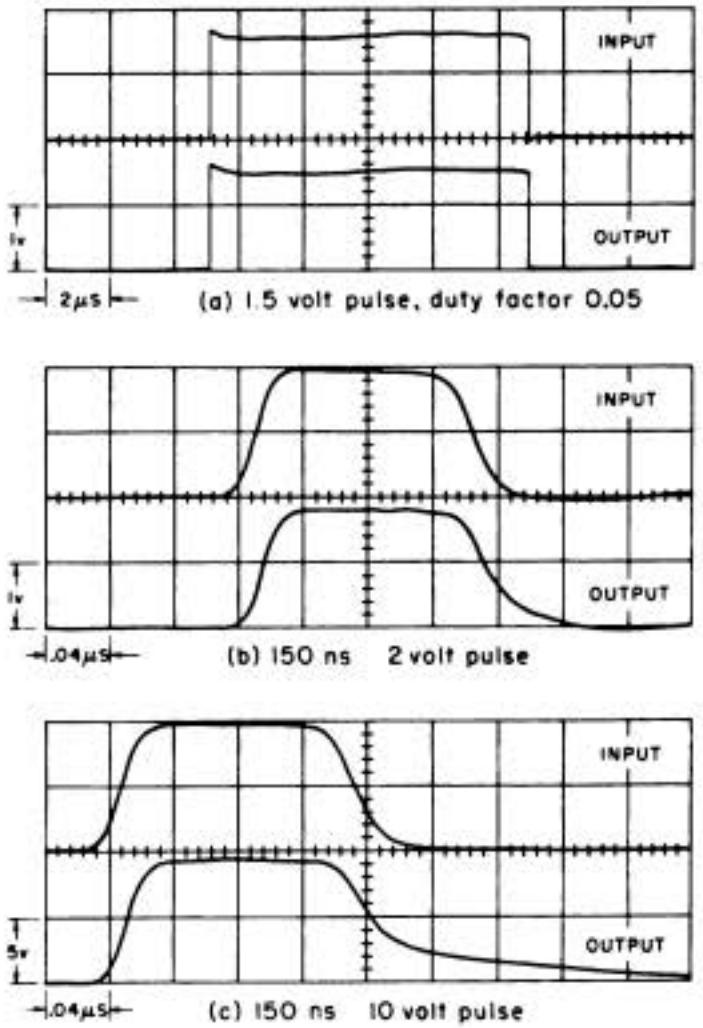


Figure 21–1.—Pulse response at 25°C with a 50-ohm resistive load. Pulse source impedance 270 ohms; capacitance of probes 14 pf.

pulses, the C2 discharge current produces a voltage drop across R4 of such polarity that it tends to reduce the forward bias of Q2, and in extreme cases, to reverse bias the base-emitter junction. The interval between pulses must be long enough to permit restoration of the bias to normal before the succeeding pulse. This condition will be satisfied if the average signal current through the load does not exceed the 6 ma dc emitter current through R4, from which the maximum permissible output pulse amplitude is

$$V_{o_{max}} = \frac{0.006\ R_L}{D},$$

where $V_{o_{max}}$ is the maximum voltage of the output pulse, R_L is the load resistance, and D is the duty factor of the signal. Since the voltage amplification of PSC 21 is approximately 1, the input voltage should be no greater than $0.006\ R_L/D$, or 17 volts, whichever is smaller.

3.3 *Typical Waveforms:* Figure 21-1a shows the pulse response of the amplifier to a 1.5-volt 0.05 duty factor signal with a 50-ohm resistive load and no added capacitance other than the oscilloscope probe. The output follows the input very closely with no overshoot or undershoot; the voltage amplification is 0.95. In *b* and *c* of Figure 21-1, the input and output pulses for 2-volt and 10-volt 150-nanosecond signals with a 50-ohm resistive load and no added capacitance are compared.

The rise time is unaffected by the pulse amplitude. The fall time is about 20 nsec per volt of amplitude, and in the case of the 10-volt 150-nanosecond pulse (Fig. 21-1c) is longer than the pulse width itself.

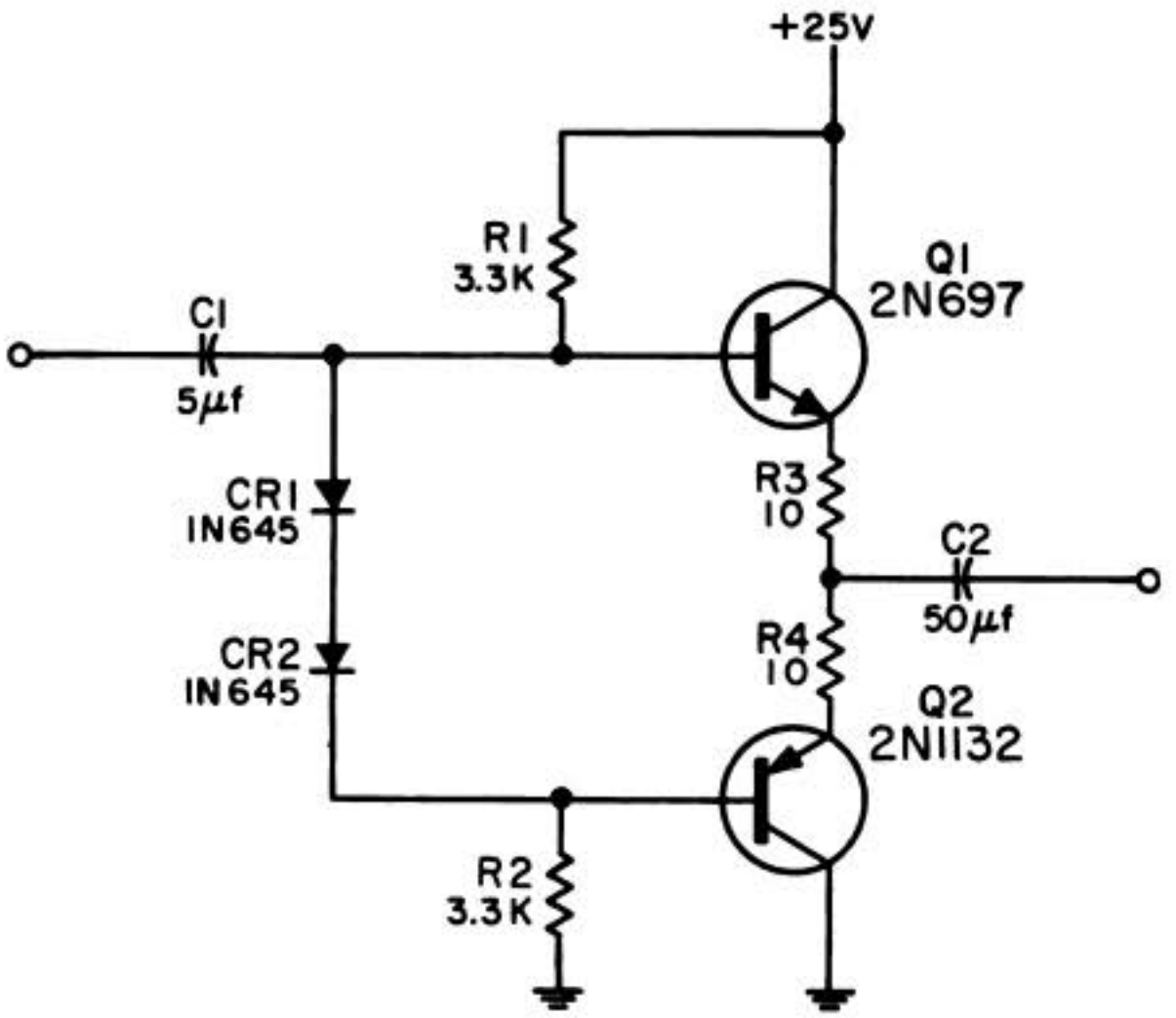
The pulse response will remain essentially the same as shown in the figure from $-55°C$ to $+125°C$. A $\pm 10\%$ variation in supply voltage has little effect on the performance.

Notes

PREFERRED CIRCUIT NO. PSC 22
COMPLEMENTARY SYMMETRY EMITTER FOLLOWER

(Originally published as PC 222)

PREFERRED CIRCUIT NO. PSC 22
COMPLEMENTARY SYMMETRY EMITTER FOLLOWER



Unless otherwise stated: R in ohms;
C>1 in pf; C<1 in μf; L in μh

Components:

Maximum power dissipation (Note 1): R1,R2: 50 mw; R3,R4: 25 mw.

Maximum capacitor voltage: C2: 12 volts; C1: Select for particular coupling application.

Limits (these are not tolerances; see Note 2): R1,R2: ±5%; R3,R4: ±20%. All C: ±20%.

Operating characteristics (Note 3):

Temperature range: −55°C to +125°C.

Load resistance: 50Ω.

Input:

Impedance: 1KΩ.

Signal polarity: Positive or negative.

Maximum signal amplitude: See Figures 22–2 and 22–3.

Bandwidth (600Ω source impedance): 50 cps to 3.5 mc.

Voltage amplification: 0.8.

Power gain: 12 db.

Output impedance: <100Ω for any source resistance (Note 4).

Power requirements: 25 volts dc ±10% at 50 ma.

(For Notes, see bottom of next page.)

PSC 22 COMPLEMENTARY SYMMETRY EMITTER FOLLOWER

1. APPLICATION

PSC 22 is a complementary symmetry emitter follower used to match a high-impedance circuit to a low-impedance load. The circuit has certain advantages over PSC 21: it will accept both positive and negative pulses, or a sinusoidal input, and its low output impedance to both positive and negative pulses results in a higher operating speed into capacitive loads.

Compensating elements must be used in PSC 22 to stabilize the performance against temperature changes, and the input capacitance is higher than that of PSC 21, since the bases of Q1 and Q2 are in parallel. In addition, because each transistor acts as a dc load for the other, failure of one transistor will usually cause failure of the other.

Single-stage emitter followers are used extensively for the purpose of isolation or impedance matching. These circuits are usually designed for a particular system, with the choice of transistor type and impedance levels dictated by the system requirements. While they are used extensively within a single system, they cannot be classed as preferred circuits because their applicability is limited outside the system for which they were designed. For this reason, no single-stage emitter follower is included as a preferred circuit.

2. DESIGN CONSIDERATIONS

In PSC 22 the principle of complementary symmetry[1] is used to obtain an emitter follower capable of handling signals of either polarity. The circuit functions in the following manner. The rise of a positive pulse will cause the NPN transistor, Q1, to conduct. When the pulse falls to zero, the output lags the input signal. This biases the PNP transistor, Q2, in a forward mode so that it conducts during the trailing edge of the pulse and thereby decreases the fall time. The response to a negative pulse is similar except that the negative-going leading edge will cause Q2 to conduct, and Q1 will conduct during the trailing edge. The circuit is therefore capable of responding rapidly to signals of either polarity.

The transistors are biased for Class B operation. Although maximum efficiency is attained at zero collector current, use of zero bias would be impractical because the nonlinearities in the small-signal region would cause crossover distortion. The transistors are biased at the projected cutoff of the I_C vs. I_B transfer curve. A quiescent collector current of about 1 ma results

[1] A coupling capacitor coupled from the input to the base of Q2 will complete the symmetry of the amplifier. Since the diodes are operated at a point such that their dynamic resistance is low, however, a second coupling capacitor is unnecessary.

NOTES:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. Thus the term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. The operating characteristics are a function of the load; those specified are based on a 50Ω load resistance (see Section 3).

4. $$R_{out} \approx \frac{R_s}{\beta\left[1+R_s\frac{(R1+R2)}{R1R2}\right]}+R3,$$

where R_s is the source resistance and β is the dc forward current transfer ratio of the conducting transistor.

in a compromise between low crossover distortion and minimum idling current.

R1 and R2 provide the necessary bias current and are usually made equal in order to bias both transistors equally. Provided R1 and R2 are equal, the equation governing the quiescent collector current is

$$I_{C1} \approx \beta_1 \left[\frac{V_{CC}}{2R1} - I_{CR1} \right],$$

where β_1 is the dc forward current transfer ratio of Q1, and I_{CR1} is the current which flows through CR1 at $0.6 + I_{C1}R3$ volts.

Temperature compensation is provided for by operating two silicon diodes, CR1 and CR2, in the forward mode. A reduction in V_{BE} of about 2 mv per degree C temperature rise per transistor is necessary for a constant collector current. Two forward-biased diodes of the same material as the transistors provide better compensation than other types of non-linear circuit elements.

Feedback voltage developed across R3 and R4 also serves to compensate for temperature variations. However, the main purpose of R3 and R4 is to prevent thermal runaway. When the transistors are operating near maximum output, the heat dissipated in the transistors will cause the quiescent collector current to increase, which in turn will result in thermal runaway if degeneration is not provided in the emitter circuit. Connecting CR1 and CR2 thermally to Q1 and Q2 would increase the thermal stability, but the result would be a cumbersome arrangement of circuit components.

3. PERFORMANCE

PSC 22 is designed for transistor interchangeability and thermal stability. Figure 22–1 shows the variation of quiescent collector current with ambient temperature and with limit transistors and diodes. When a signal results in operation near maximum transistor dissipation, the transistors will heat more than the diodes will, and since the transistors and diodes are not thermally connected, the compensation will be less effective. This will result in an upward shift of the curves of Figure 22–1; however, even with maximum dissipation the quiescent collector current at any temperature within the operating range will usually not exceed 4 ma.

The power delivered to the load is limited by the maximum collector dissipation of each of the transistors. Both the 2N697 and the 2N1132 will dissipate approximately 0.6 watts at 25°C and 0.2 watts at 125°C in free air with no heat sinks. The input voltage may be limited by

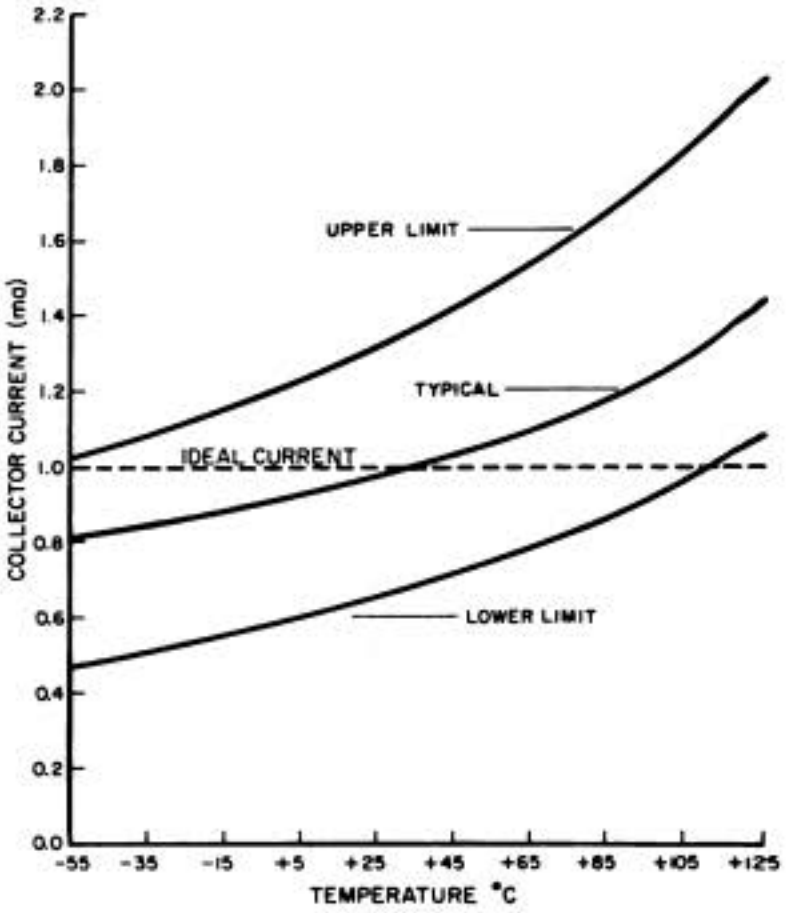


Figure 22–1.—Variation of quiescent collector current with temperature and with transistor and diode limit characteristics.

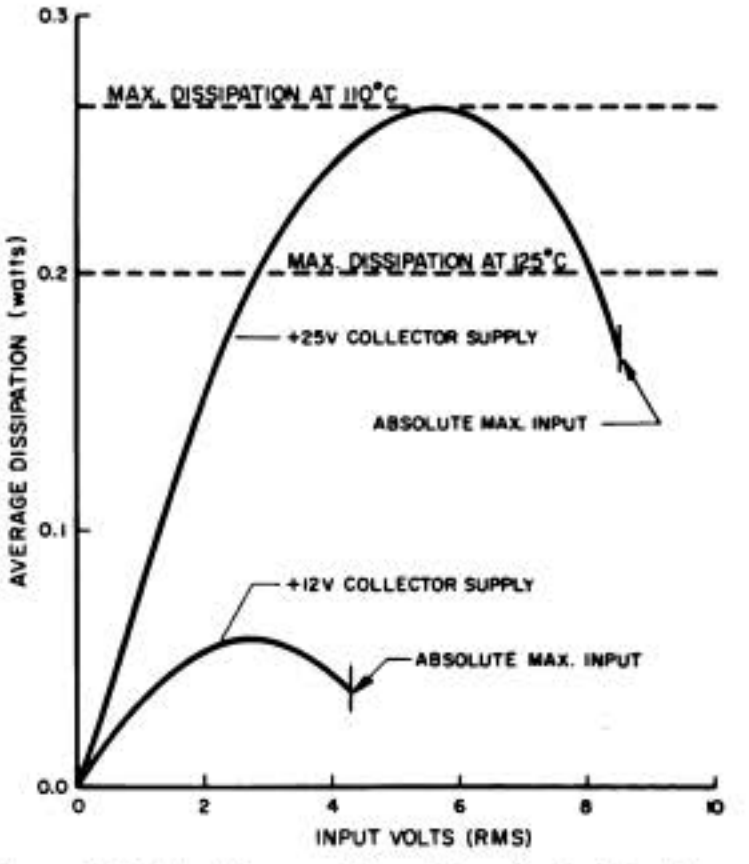


Figure 22–2.—Average transistor dissipation for sine wave operation into a 50-ohm load.

either the power dissipation or by the collector-to-emitter voltage, as indicated by Figures 22-2 and 22-3.

For sinusoidal inputs and operation into a 50Ω load at 125°C, the maximum input voltage is limited to 2.8 volts rms by the average power dissipation of the transistors. If the maximum ambient temperature is limited to 110°C, or if heat sinks are used to increase the dissipation ratings of the transistors, any input voltage up to the maximum of 8.5 volts rms is permissible. If the load is changed to 70Ω, any input voltage up to the 8.5 volts rms maximum may be used without exceeding the maximum dissipation of the transistor at 125°C. The maximum dissipation could be decreased by reducing the collector supply voltage to 12 volts, but the input signal would then be limited to 4.4 volts rms by the collector-to-emitter voltage. Assuming negligible dissipation from the quiescent current, the average power dissipation per transistor for a sine wave is

$$P_D = \frac{V_{cc} V_P}{2(R_L + R3)} \left[\frac{1}{\pi} - \frac{V_P}{2V_{cc}} \right],$$

where V_P is the peak voltage of the input sine wave.

For pulse operation, the duty factor of the signal is also considered in determining the average transistor dissipation as shown in Figure 22-3. For a square wave input (duty factor =0.5) and a 50Ω load, the input voltage is limited principally by the permissible average power dissipation of the transistor. If the duty factor is less than 0.3, however, the input voltage is limited only by the collector-to-emitter voltage of the transistor. If the load resistance is larger than 90Ω, the 12-volt peak input is permissible for any duty factor less than 0.5. For a given load resistance and duty factor, the average dissipation per transistor may be determined from the equation

$$P_D = D \frac{V_P}{R_L + R3} \left[\frac{V_{cc}}{2} - V_P \right],$$

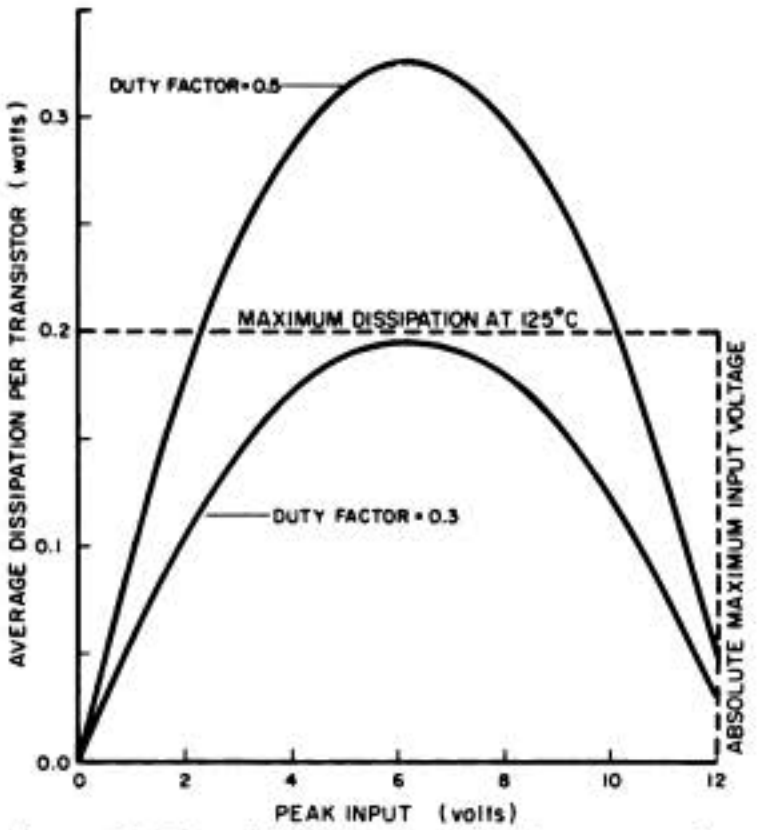


Figure 22-3.—Average transistor dissipation for pulse operation into a 50-ohm load.

where V_P is the peak voltage and D the duty factor of the input signal. The maximum instantaneous and average dissipations occur at a peak input voltage equal to half the collector-to-emitter voltage of the transistor. The thermal time constants of the transistors are large enough so that the average dissipation is exceeded before the maximum permissible instantaneous dissipation is reached.

The low-frequency response is a function of the input and output coupling capacitors, C1 and C2, which have been chosen for a 50-cycle response into a 50Ω load.

The over-all voltage amplification and power gain in db of PSC 22 as a function of load resistance may be determined approximately by the following expressions:

$$A \approx \frac{R_L}{R_L + R3}$$

$$G \approx 10 \log A^2 \frac{R_{in}}{R_L}.$$

Notes

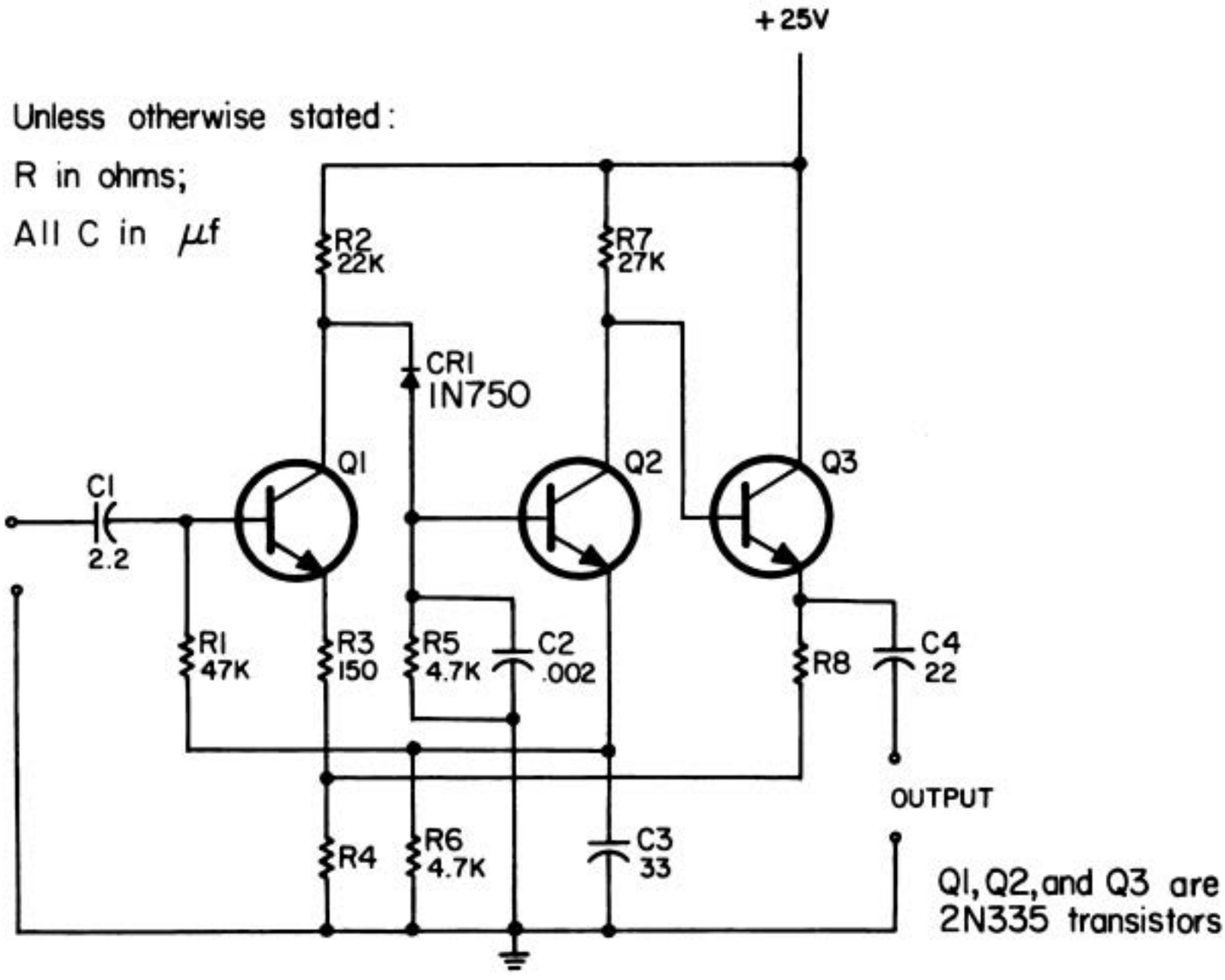
CIRCUIT INDEX

U. S. GOVERNMENT PRINTING OFFICE

PREFERRED CIRCUIT NO. PSC 23
AUDIO PREAMPLIFIER

PREFERRED CIRCUIT NO. PSC 23

AUDIO PREAMPLIFIER



Components:

R4 is chosen for a specified amplifier gain (see Operating Characteristics).

R8 = 2.7kΩ for 85°C operation and 6.8kΩ for 125°C operation.

Resistor power dissipation (Note 1): R5, R6,: <1 mw; R1, R3, R4, R7: <5 mw; R2: 22 mw; R8: 87 mw.

Limits (these are not tolerances; see note 2): R4, R8: ±10%; R1, R2, R3, R5, R6, R7: ±20%. C2: ±20%; all other C: +50%, −20%.

Operating characteristics:

Minimum input impedance: 5kΩ

Frequency response: 10 cps to 10,000 cps ±1 db.

Total harmonic distortion (25°C): less than 3%

	Operating temperature −55°C to +85°C	−55°C to +125°C
R8	2.7kΩ	6.8kΩ
Maximum signal output to 1,000Ω load	2 volts rms	1 volt rms
R4	10Ω to 60Ω	25Ω to 175Ω
Voltage gain (dependent upon R4)	50 to 250	50 to 250

Power requirements: +25 volts ±10% at 6 ma (maximum).

(For Notes, see bottom of next page)

PSC 23 AUDIO PREAMPLIFIER

1. APPLICATION

This audio preamplifier may be used to amplify audio signals in communications or other equipment to the level necessary to drive an output stage. Of importance is the gain and frequency-response stability achieved by feedback paths. The use of silicon devices permits circuit operation over the temperature range −55°C to +125°C. The amplifier may be used to drive Preferred Circuit No. PSC 24, Audio Driver.

2. DESIGN CONSIDERATIONS

The preamplifier consists of two common-emitter stages driving an emitter-follower. All stages are direct-coupled.

Direct coupling in transistor amplifiers is generally avoided because the amplification of dc current variations due to temperature variations may shift the operating point. However, this circuit makes use of both dc coupling and feedback to maintain a fairly stable operating point over a wide temperature range. In addition, the ac feedback path afforded by R4 may be used to control the gain of the amplifier.

Coupling between the first two stages is achieved by means of the 1N750 zener diode, a 4.7-volt device. The diode affords a very low ac impedance between the collector of the first stage and the base of the second stage. The 4.7-volt drop between collector and base is sufficient, with the aid of R5, to establish bias for transistor Q2. Because the output stage, Q3, is connected as an emitter follower, the base dc potential is close to that of the collector of the previous stage and direct coupling is possible. In addition, the emitter-follower stage permits the output to be coupled to a wide variety of loads.

3. PERFORMANCE

The frequency response of a typical amplifier is shown in figure 23-1. For this test, a load resistance of 1000Ω was used and the input signal was held constant at 1 millivolt rms over a wide range of frequencies and temperatures. The plot indicates the typical frequency response of 10 cps to 10,000 cps, ±1 db over the specified temperature range of −55°C to +125°C.

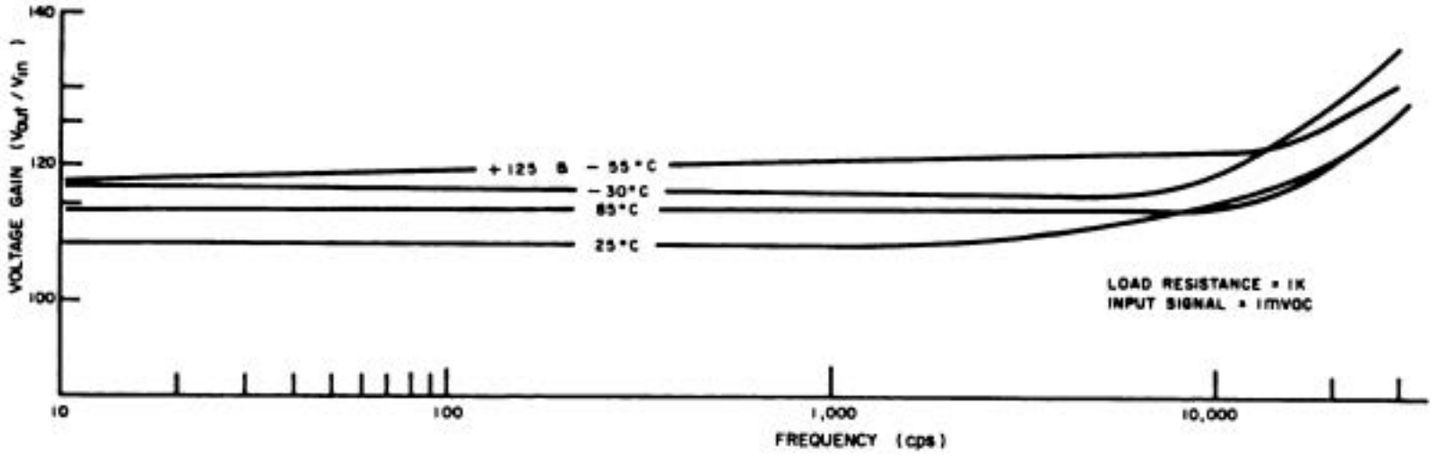


Figure 23-1.—Typical Frequency Response for Ambient Temperature Range −55°C to +125°C

Notes:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

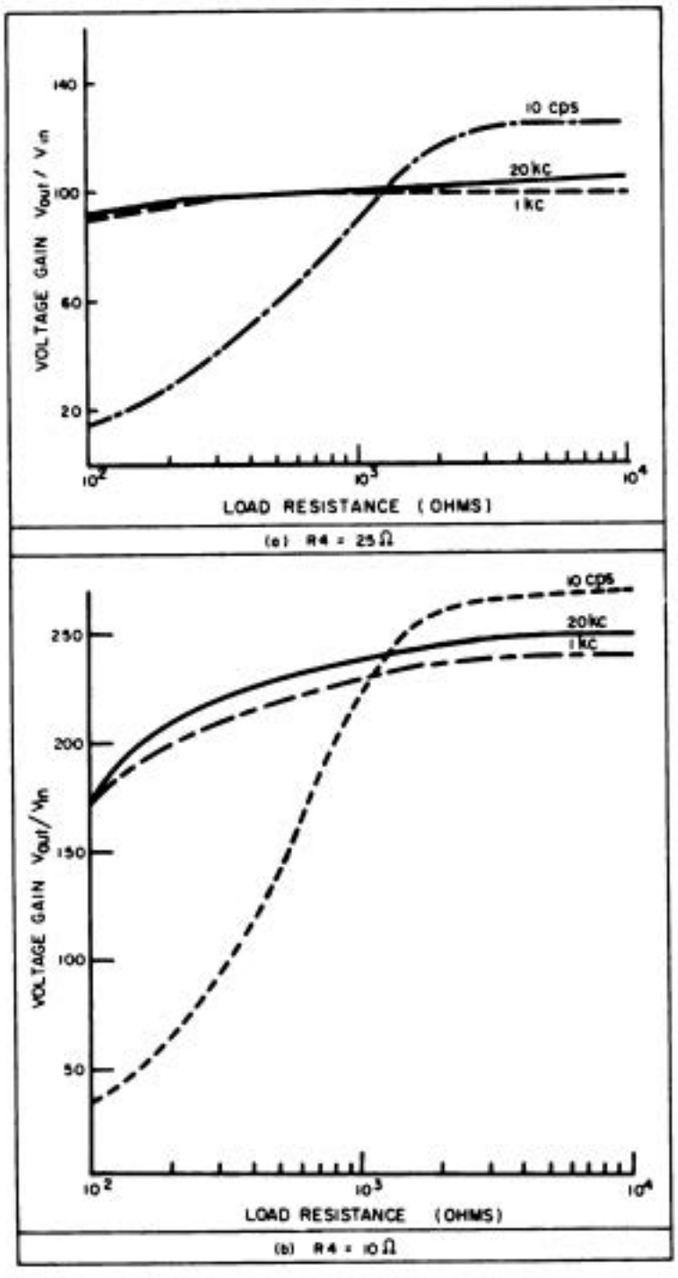


Figure 23-2.—Voltage Gain vs. Output Load for Two Values of R4. V_{cc} = +25V. T_A = 25°C. $R_{(generator)}$ = 600Ω. Input Signal = 1mVac

When the load resistance is increased, the gain increases as shown in figure 23-2. Decreasing the feedback resistance, R4, both increases the gain (figure 23-3) and decreases the gain stability with respect to load variations. (Compare figs. 23-2a and 23-2b.) When R8 is 2.7kΩ, with a variation of feedback resistance from 10Ω to 60Ω the voltage gain decreases from 250 to 50.

An indication of useful output signal can be determined from figure 23-4, wherein total distortion and output signal level are plotted as a function of input signal. The same figure also shows that voltage gain is relatively constant with respect to variations in input signal levels below 40mVac. Gain variation is less than ±0.5% for a supply voltage of 25 ± 5 volts.

Using various combinations of transistors, including units having limit values of h_{FE}, it was found that circuit gain at 1 KC remains within ±0.5 db over the temperature range of 25°C to 125°C, and is within +0.5 and −1.0 db of the median 25°C value at −55°C. Under the same test conditions, the majority of transistor combinations resulted in distortion measurements less than 1%. The worst-case distortion measurement at 125°C was 2.9%; at −25°C it was less than 5%; and at −55°C, it was approximately 11%.

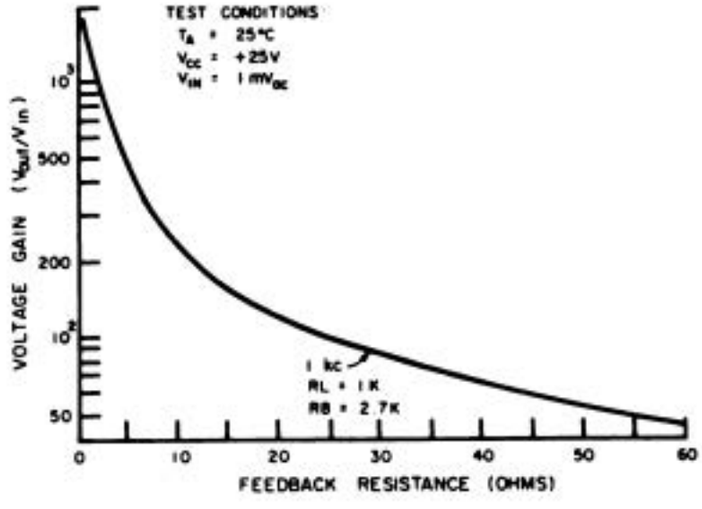


Figure 23-3.—Voltage Gain vs. Feedback Resistance (R4)

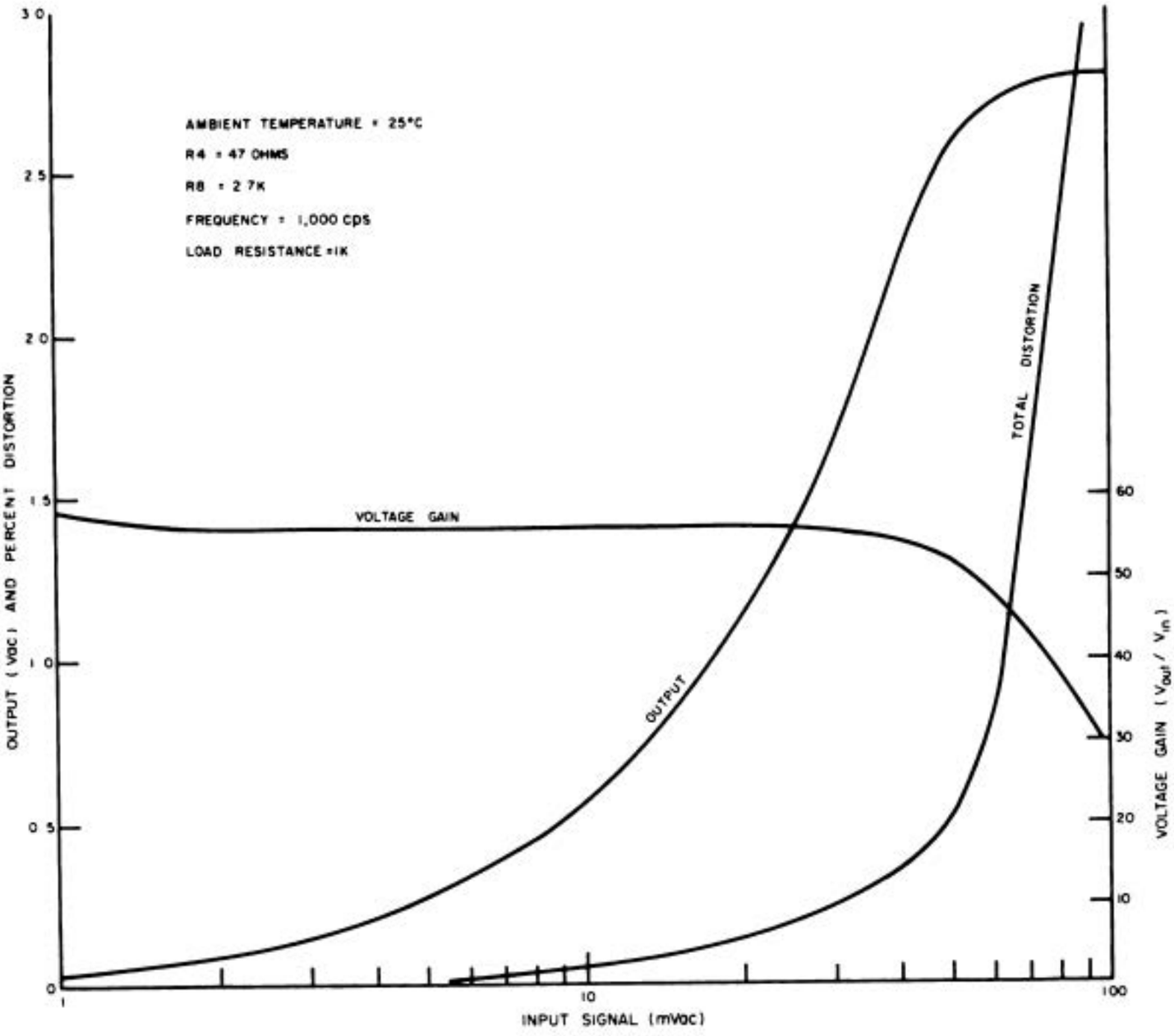


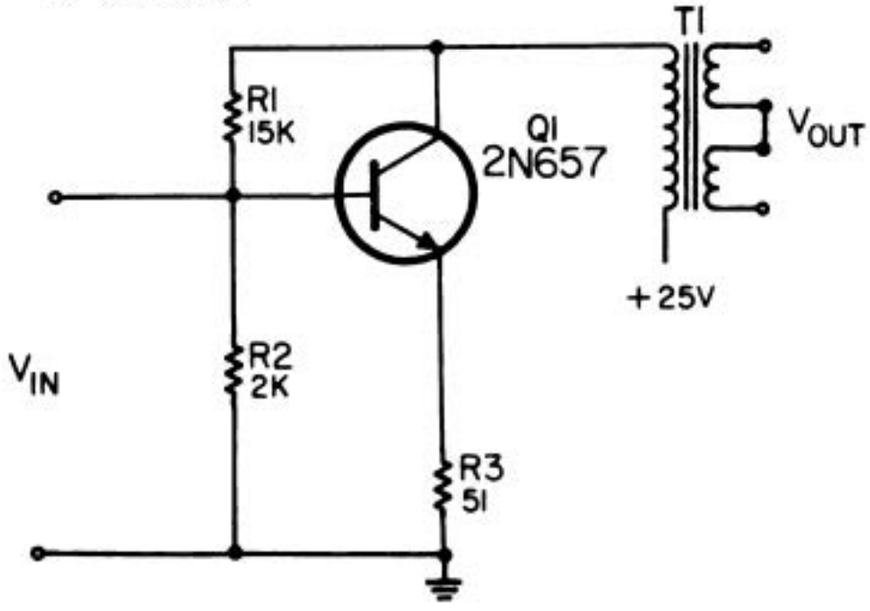
Figure 23-4.—Typical Input-Output Characteristics

Notes

PREFERRED CIRCUIT NO. PSC 24
AUDIO DRIVER, 150 MW

PREFERRED CIRCUIT NO. PSC 24

AUDIO DRIVER, 150 MW



Components:

Transformer:

Primary impedance: 500Ω.

Primary resistance: 35Ω.

Secondary impedance (Note 1): Dependent upon load.

Resistor power dissipation (Note 2): R1, R2, R3: <0.1 watt. T1 primary: 20mw at 125°C

Limits (these are not tolerances; see note 3): All R: ±10%.

Operating characteristics (Note 4):

Maximum signal required for 150 mw output: 1.2 Vac.

Maximum distortion at 150 mw output: 9%.

Typical distortion at 150 mw output: 3.5%.

Typical signal required for 150 mw output: 1.1 Vac.

Frequency response (Note 5): 60 to 24,000 cps, ±3 db.

Input impedance: 550Ω.

Typical power gain: 18 db.

Operating temperature (Note 6): −55°C to +125°C with a transistor heat sink of 3 x 3 x ⅛ inch aluminum.

Power requirements:

+25 volts ±10% at 25 ma (maximum).

(For Notes, see bottom of next page)

PSC 24 AUDIO DRIVER, 150 MW

1. APPLICATION

This audio amplifier is designed to deliver about 150 mw of audio signal with less than 10% total distortion at 125°C. The circuit has a typical power gain of 18 db. It can be used with the preamplifier, circuit PSC 23, and may be used to drive a push-pull power amplifier, earphones, or a loudspeaker.

2. DESIGN CONSIDERATIONS

Transistor types 2N656 and 2N498 are frequently found in the audio circuits of naval communications equipment. The circuit considered here employs a related device, the 2N657, which appears in MIL-STD-701B. This device is used in the common-emitter configuration for maximum power gain.

The driver stage is biased for Class A operation, and is reasonably stable for wide variations in ambient temperature. The dc operating point is established by the voltage divider R1 and R2. The use of unbypassed emitter resistor R3 and connection of R1 to the collector provide stabilization of the operating point.

Figure 24-1 is a plot of output power and total distortion vs. load resistance using a transistor with nominal dc current gain and the UTC H-27 transformer. Increasing the load resistance above 16Ω effectively increases the collector load, thereby increasing the gain of the circuit. Under the conditions stated, the transistor reaches saturation at a load of approximately 35Ω. This indicates that optimum

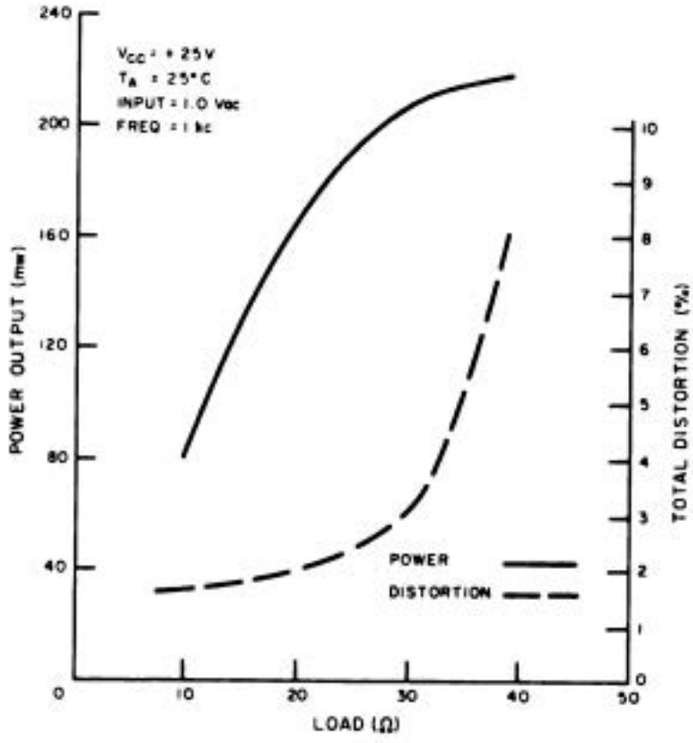


Figure 24-1.—Power Output and Total Distortion vs. Load, Using a Nominal Transistor and Transformer UTC Type H-27

Notes:

1. The load impedances of driver stages in naval airborne equipments vary; therefore the secondary impedance of the output transformer is not given. Its value may be chosen to suit the user's needs. The transformer used in all tests of the circuit has a secondary impedance of 16Ω (UTC Type H-27 or equivalent).

2. These are maximum powers dissipated in the resistors and transformer primary winding. In determining these values, allowance has been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based upon component values which do not deviate from nominal by more than the limits specified. The term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. Operating characteristics are based on a load resistance of 16Ω and an ambient temperature of 25°C. Refer to figure 24-1 for output characteristics obtained with a mismatched load.

5. The frequency response depends upon the design of the transformer. The response given was achieved with the commercially available type mentioned in Note 1.

6. The transistor dissipates about 550 mw in this circuit, and a heat sink is recommended. The 2N657 is rated for 875 mw dissipation at 125°C, using the indicated heat sink.

primary impedance of the transformer for maximum gain should be approximately 1,000Ω. Circuit gain would be increased approximately 3 db. However, a suitable transformer with a 1,000Ω primary impedance cannot presently be procured as a standard part. Figure 24–1 indicates that a load to secondary mismatch of 2 to 1 will provide 2 db of additional gain and only 3% increase in distortion with the economical advantage of the standard transformer. If optimum gain and distortion characteristics are required, a non-standard transformer with a 1,000Ω primary impedance and a secondary impedance equal to that of the load may be procured.

3. PERFORMANCE

3.1 *Power Output:* When a transistor with nominal h_{FE} is employed, clipping of the output waveform at 25°C begins when the input signal reaches a level of about 1.0 volt rms. At this level, total distortion approaches 2%. The power output at that point is approximately 125 mw. Figure 24–2 is a plot of output power and total distortion vs. input voltage for two 2N657 transistors—one having a high dc current gain (h_{FE}=80), and the other having a low gain (h_{FE}=30). The narrow spreads of the two curves for output and of the two curves for distortion indicate the effectiveness of the feedback design in reducing the effects of transistor product variability.

The maximum power output over the rated temperature range is determined by the transistor characteristics, supply voltage, and load resistance. With the transformer used in this test, a load resistance of 16Ω, nominal transistor h_{FE}, and Vcc of 25 volts, the maximum output is 175 mw at 5% total distortion.

3.2 *Frequency Response:* A frequency range of 60 cps to 24,000 cps was obtained at 25°C within ±3 db of the 1,000 cps output level. The response curve is shown in figure 24–3.

3.3 *Temperature and Voltage Stability:* Over

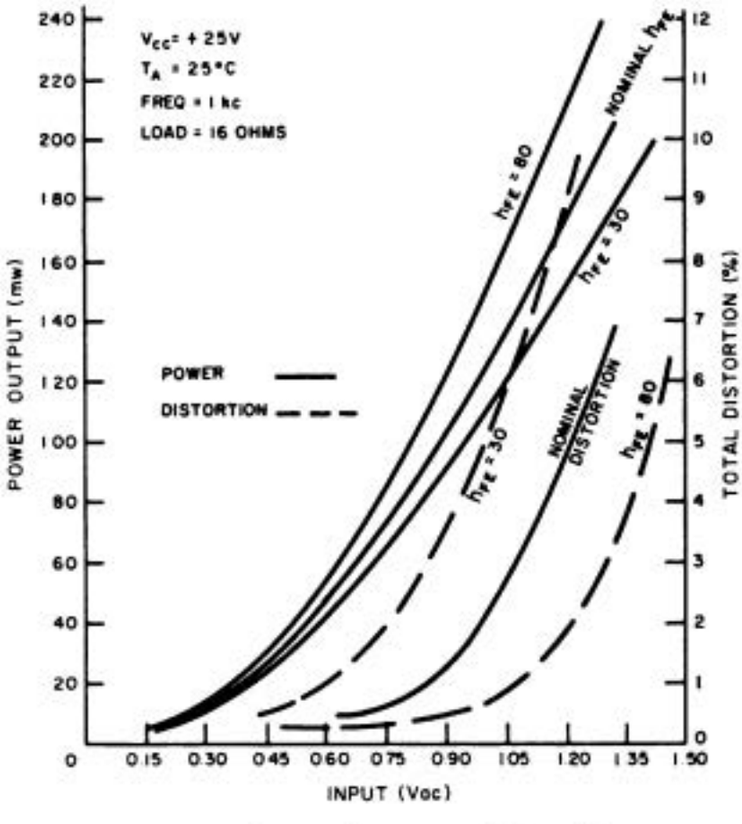


Figure 24–2.—Power Output and Total Distortion vs. Input Signal Voltage with Transistors Having Limit Values of h_{FE}

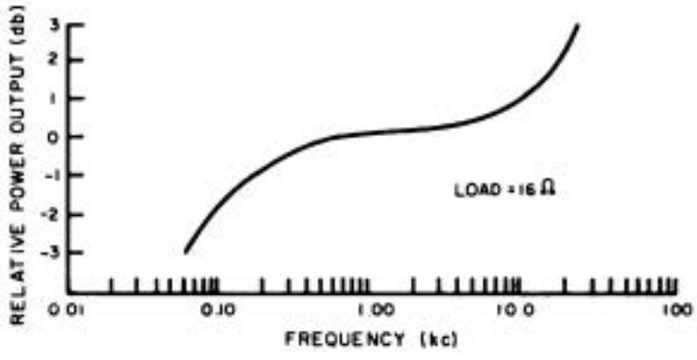


Figure 24–3.—Typical Frequency Response at 25°C. Input Signal Level=0.53 Vac. Output Reference Level, 0 db=37 mw

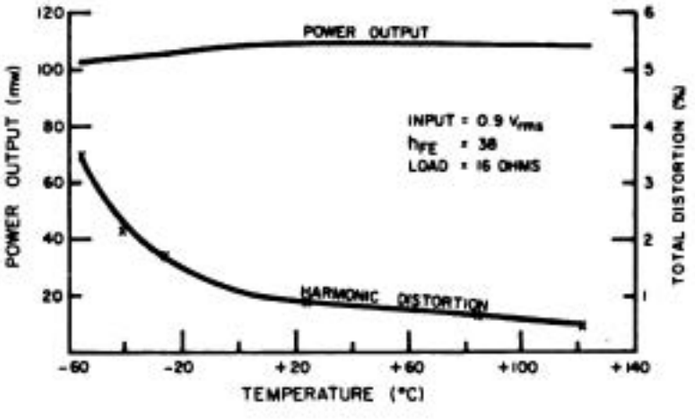


Figure 24–4—Power Output and Total Distortion vs. Ambient Temperature

the specified temperature range, the output remained reasonably constant. Total distortion decreased as the operating temperature increased. Figure 24-4 provides curves of output power and distortion versus ambient temperature for a typical amplifier.

A 10% reduction in supply voltage from 25 volts will reduce the output power by only 2%.

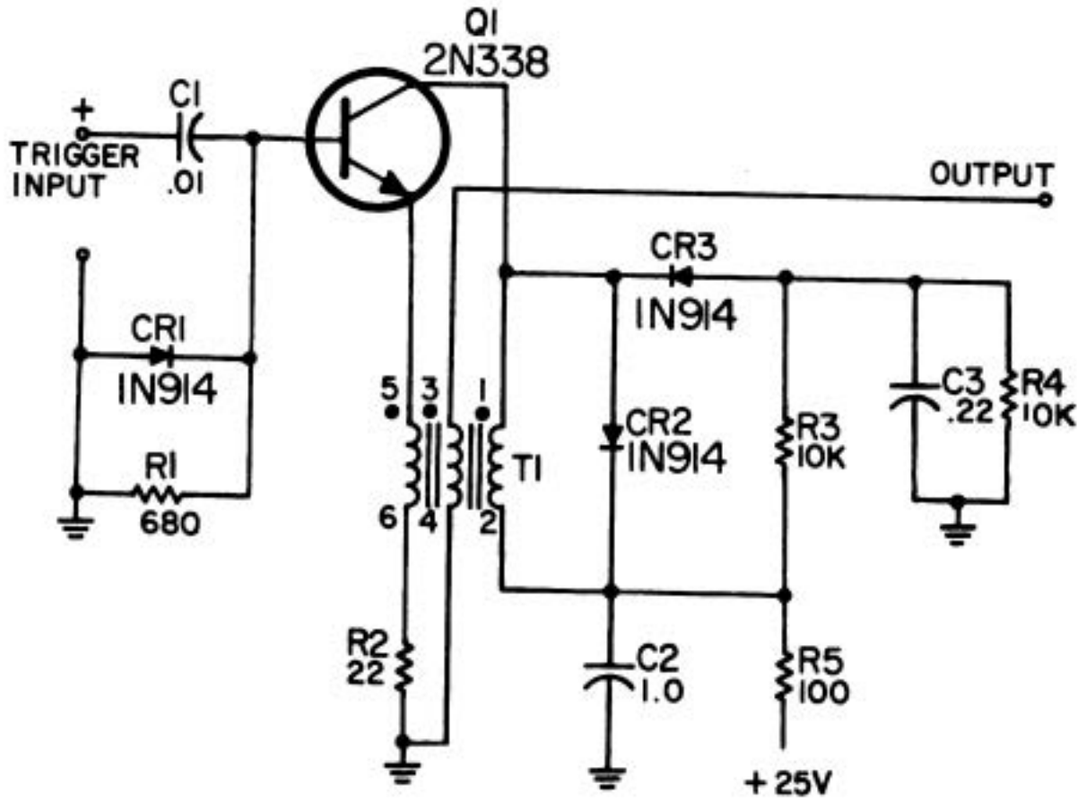
3.4 *Input Impedance:* Over the specified temperature range, the input impedance at 1,000 cps remained within ±10% of its 25°C value of 550Ω.

Notes

PREFERRED CIRCUIT NO. PSC 25
TRIGGERED BLOCKING OSCILLATOR

PREFERRED CIRCUIT NO. PSC 25
TRIGGERED BLOCKING OSCILLATOR

Unless otherwise stated:
R in ohms; C < 1 in μf



Components:

T1: See note 1.

Resistor power dissipation (Note 2): R1, R4, R5: 0.04 watt; R2: 0.1 watt; R3: 0.5 watt.

Limits (these are not tolerances; see note 3): All R: ±10%; C1 and C3: ±20%; C2: +50%, −20%.

Operating characteristics:

Input:

Trigger polarity: positive.

Trigger amplitude (Note 4): 1.5 to 10 volts peak.

Maximum trigger prf (Note 5):

Nominal Output Pulse Width	*Temp °C*	*Max prf pps*
2 μs	25°C	15,000
	125°C	3,000
6 μs	25°C	5,000
	125°C	1,000

Impedance: approximately 600Ω at 25°C.

Output (Note 6):

Transformer turns ratio	3:2:1	3:2:1
Transformer primary inductance, OCL, (mh)	0.5	3
Pulse width (μsec)	1.7–2.6	4.6–6.8
Rise time (μsec)	0.05–0.11	0.1–0.14
Decay time (μsec)	0.04–0.1	0.2–0.3
Amplitude (volts peak)	8.0	8.0
Resistive load	1,500Ω	1,500Ω

Polarity:

positive with terminal 3 grounded.

negative with terminal 4 gounded.

Delay (Note 7): 0.02 to 0.12 μsec with OCL=3 mh; 0.04 to 0.26 with OCL=0.5 mh.

Operating temperature: −55°C to +125°C.

Power requirements:

+25 volts ±10% at 2 ma (maximum).

Notes:

1. The pulse transformers used in evaluating this circuit were PCA Electronics Company types TT 321–0.5 and TT 321–3, or equivalent. The turns ratios of windings 1–2, 3–4, and 5–6 are 3:2:1, respectively. The open circuit inductance in mh of the primary winding (1–2) is designated by the dash number following the three-digit number that indicates the turns ratio.

2. These are the maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

4. The minimum trigger of 1.5 volts peak is required for worst-case conditions with a 10 μsec pulse width.

5. A method of calculating the maximum allowable prf is given in section 2.

6. The output characteristics shown are typical for a trigger pulse amplitude of 1.5 volts peak and a repetition frequency of 1,000 pps at 25°C. The spread of values is due to product variability of the transistors. The characteristics also vary with changes in trigger-pulse rise time and amplitude, in temperature, and in supply voltage.

7. Delays between input and output pulses were measured between the 10%-of-maximum-amplitude points on their leading edges. Delay time varies with primary open circuit inductance, input trigger waveform and amplitude, temperature, and transistor product variability.

PSC 25 TRIGGERED BLOCKING OSCILLATOR

1. APPLICATION

This triggered blocking oscillator may be used in applications where pulses longer than 1 μsec with amplitudes to 8 volts are required. Because the circuit employs silicon devices, operation over the temperature range −55°C to +125°C is possible.

2. DESIGN CONSIDERATIONS

The transistor, 2N338, and the 1N914 diode are preferred types listed on MIL–STD–701B. The 2N338 was chosen for its relatively low capacitance, high-frequency capability, and low power requirements. Reverse base-to-emitter voltage protection is provided by diode CR1. In addition, diode CR1 presents a low impedance path in the base circuit when triggering action has begun, thus improving triggering sensitivity and decreasing rise time. Diodes CR2 and CR3 clamp the collector voltage swing to safe values, thus protecting the collector junction from transformer inductive kick-back, and keeping the transistor from saturating. Avoidance of transistor saturation reduces fall time.

A tertiary winding on the transformer provides a means of coupling to the load with dc isolation, and furnishing pulses of either polarity. The core type, winding-ratios, and inherent capacitances and inductances of the transformer govern the output pulse characteristics obtained with a given transistor. Transformers with lower open circuit primary inductance provide output pulses with shorter pulse widths and shorter rise and fall times.

The maximum allowable prf is limited by the power-handling capacity of the transistor. To calculate the maximum prf, the maximum ambient temperature is determined, and the rated maximum power dissipation at that temperature is obtained from the derating curve given in the applicable military specification, MIL–S–19500/69B (Navy). The maximum allowable prf can be calculated as follows:

$$\text{prf}_{max} = \frac{P_c}{T_w \times P_{pk}}$$

where:

prf is in pulses per second, pps

P_c is rated collector-power dissipation in watts at the maximum ambient temperature (a 50% derating factor is recommended)

T_w is the pulse width in seconds

P_{pk} is the peak pulse collector power dissipation in watts. This is calculable as $P_{pk} = (\hat{e}_c - \hat{e}_E)\hat{i}_c$, where $\hat{e}_c$ is the collector voltage during the pulse, $\hat{e}_E$ is the peak emitter voltage, and $\hat{i}_c$ is calculated from the measured peak voltage across R2. The peak voltages can be measured with a suitable calibrated oscilloscope. (See "Operating characteristics.")

3. PERFORMANCE

The characteristics of the output pulse of the blocking oscillator are described in terms of rise time, pulse width, and amplitude. Rise time is measured between the 10 and 90% points of the initial slope of the pulse. The pulse width is measured at 50% of the maximum amplitude. For these measurements, the initial slope and plateau region of the pulse are approximated by straight lines. The amplitude is taken at the point of intersection of the slope and plateau lines.

Performance data on this circuit were obtained under typical, best-case, and worst-case conditions of temperature, trigger amplitude, supply-voltage variations, and transistor product variability. Among the samples of 2N338 transistors tried were those having minimum and maximum values of h_{FE} and saturation resistance. The circuit performance is also subject to changes due to possible variations in transistor and pulse transformer characteristics. As the load resistance is reduced below about 500Ω, the pulse width and amplitude decrease sharply, and rise time increases rapidly. With load resistances exceeding about 1,500Ω, the pulse characteristics are essentially independent of load variations.

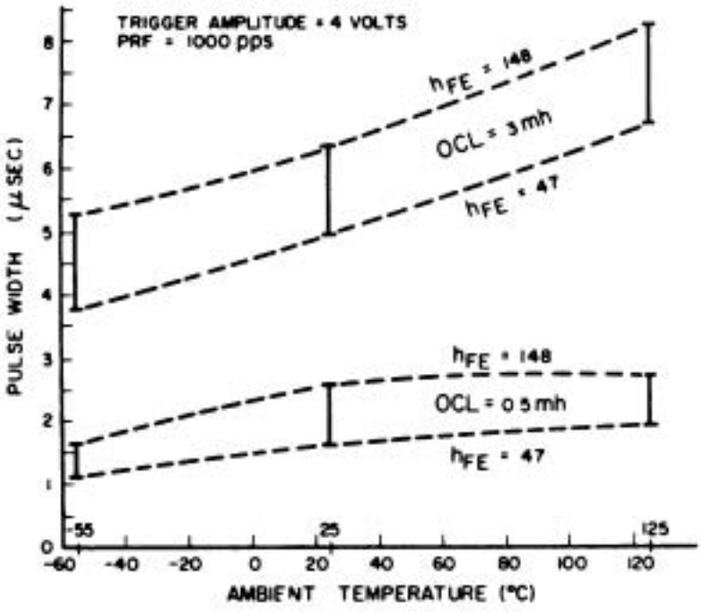


Figure 25–1.—Pulse Width vs. Ambient Temperature (for Transistors Having Limit Values of h_{FE})

Pulse-width variation over the temperature range of −55°C to 125°C is shown in figure 25–1 for transistors having limit values of h_{FE} when used with transformers having primary open circuit inductance values of 0.5 and 3.0 mh, respectively.

Pulse width is quite stable with changes in trigger pulse repetition frequencies below the maximum value referenced under Operating Characteristics. Below 1,000 pps, the pulse width is constant under a given set of conditions. Above 1,000 pps, the pulse width increases only about 5% for each 1,000 pps increase in pulse rate.

Nominal pulse width may be controlled by limiting the trigger amplitude. Figure 25–2 shows typical wave forms obtained with a primary OCL of 3 mh at 25°C by varying the trigger pulse amplitude. Note that at an input of 4 volts, there is an initial positive spike of about 2 volts preceding the negative output pulse. The positive spike increases as input trigger voltage increases until, at an input level of 10 volts, the spike is 8 volts in amplitude. Limiting the input trigger pulse to between 1.5 and 4 volts is therefore recommended. Figure 25–3 shows the effects of higher input trigger amplitudes on both pulse width and decay time when the primary OCL is 0.5 mh.

Changes in supply potential of ±10% will change the pulse widths a maximum of +8 and −5% respectively. Output pulse amplitudes will change a maximum of ±12% for the same changes in supply potential. Changes of ±10% in the supply potential have little effect on the other output pulse characteristics.

Output pulse rise time is a function of the combined effects of transistor and transformer product variability, temperature, and trigger pulse rise time and magnitude. Table 25–1 shows typical rise time vs. trigger pulse amplitude for both the wide and narrow pulse transformers.

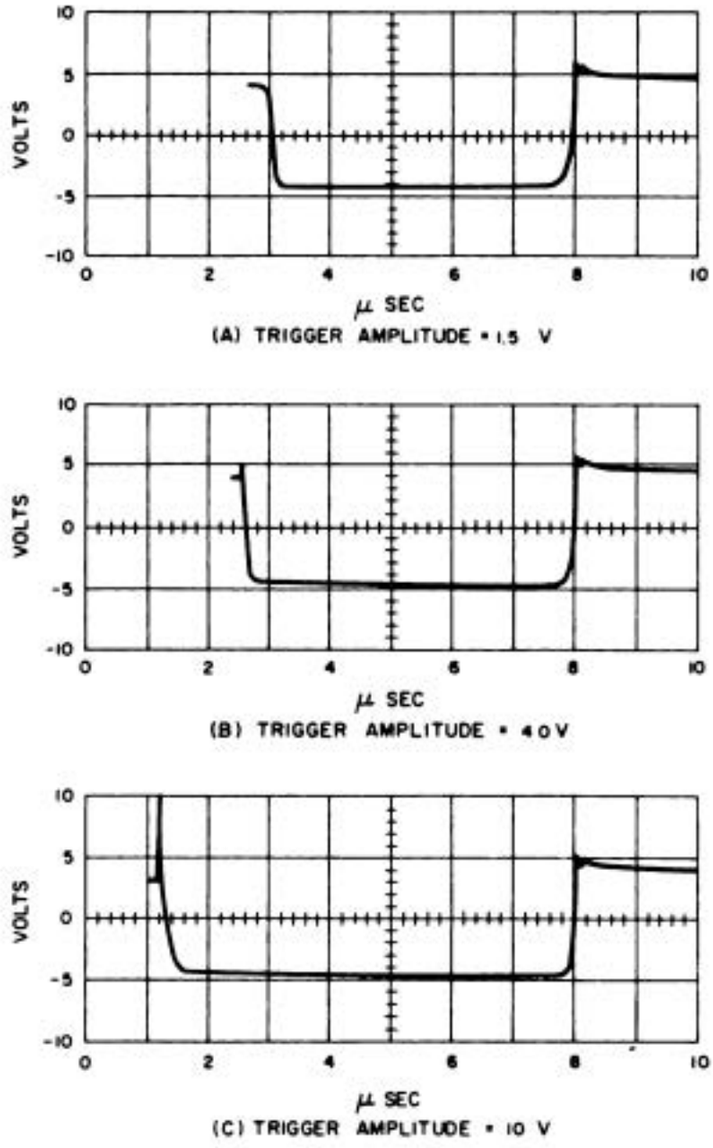


Figure 25–2.—Typical Output Waveforms for Three Trigger Pulse Levels at 25°C, OCL = 3 mh

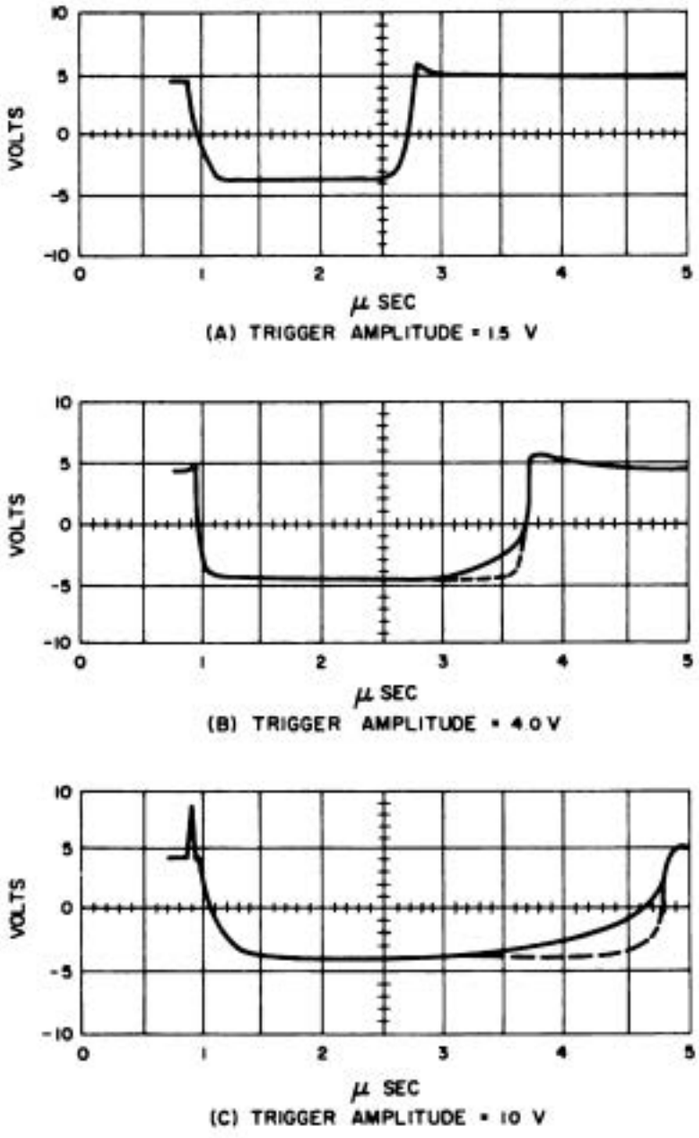


Figure 25–3.—Typical Output Waveforms for Three Trigger Pulse Levels at 25°C, OCL =0.5 mh

TABLE 25–1.—*Relationship of trigger voltage and ambient temperature to rise time for transistors having limit values of* h_{FE}

Trigger amplitude (volts)	Rise time (μsec)		
	−55°C	25°C	125°C
1. 5	0. 06–0. 15	0. 06–0. 11	0. 08–0. 10
10. 0	0. 03–0. 05	0. 10–0. 30	0. 07–0. 16

Fall time for the circuit varies with transistor product variability (chiefly saturation resistance), trigger amplitude, and temperature. Transistors with very low saturation resistance gave very low fall times, less than 0.3 μsec and generally on the order of 0.1 μsec, regardless-of temperature or pulse amplitude. (See figure 25–3.) At −55°C, measured fall times were also on the order of 0.1 μsec for all transistors regardless of trigger voltage; however, at 25°C and 125°C, with the exception of transistors having low saturation resistance, temperature and trigger amplitude influenced fall times as measured on transistors having limit values of h_{FE}, as shown in table 25–2.

TABLE 25–2.—*Relationship of trigger voltage and ambient temperature to circuit fall time for transistors having limit values of* h_{FE}

Trigger amplitude (volts)	Fall time (μsec)		
	−55°C	25°C	125°C
1. 5	0. 07–0. 10	0. 04–0. 11	0. 1–1. 1
10. 0	0. 06–0. 12	0. 3 –1. 6	0. 1–1. 1

Values of fall time for both wide and narrow pulse transformers are comparable.

A factor in the determination of maximum safe prf is the range of peak collector dissipations to be expected. Table 25–3 is representative of data taken with a supply voltage of 25 volts, prf=1,000 pps, and a pulse width of 2 μsec.

Increasing the supply voltage by 10% results in an approximate increase of 10% in the peak collector dissipation for most transistors. An exception was observed in transistors with low saturation resistance, which experienced an increase in collector dissipation to nearly 20% with the 10-volt trigger.

Using the method outlined in section 2, the maximum recommended prf was calculated on the assumption of a 50% derating of the maximum rated collector dissipation and a worst-case assumption of 4 watts peak collector dissipation.

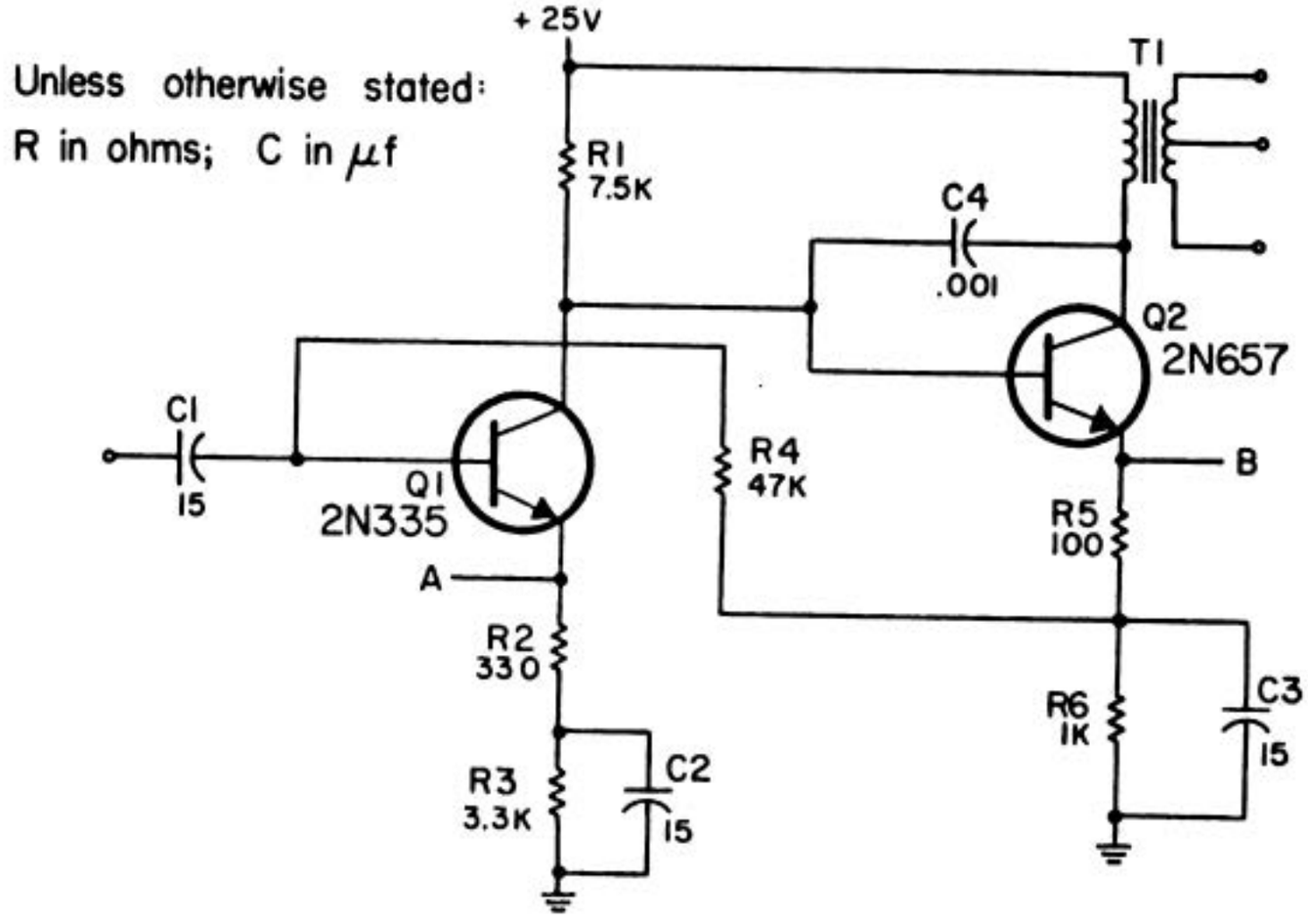
TABLE 25–3.—*Typical peak power measurements as functions of trigger voltage, transistor characteristics, and ambient temperature*

Trigger voltage (volts)	Transistor characteristic	Peak power (watts)		
		−55°C	25°C	125°C
1.5	h_{FE}=47	0. 7	0. 9	0. 7
10.0	h_{FE}=47	1. 7	2. 8	1. 65
1.5	h_{FE}=148	0. 8	1. 3	0. 75
10.0	h_{FE}=148	1. 8	3. 2	1. 8
1.5	V_{CE}(sat)=0.37V.	0. 8	1. 3	0. 9
10.0	V_{CE}(sat)=0.37V.	2. 1	3. 8	1. 9

Notes

PREFERRED CIRCUIT NO. PSC 26
INSTRUMENT CONTROL PREAMPLIFIER

PREFERRED CIRCUIT NO. PSC 26
INSTRUMENT CONTROL PREAMPLIFIER



Components:

Output transformer T1:

DC resistance of primary: 100Ω.

Maximum primary current: 8 ma.

AC impedance: primary 1,500Ω; secondary 500Ω center-tapped.

Resistor power dissipation (Note 1): All R: <125 mw.

Limits (these are not tolerances; see note 2): R1, R2, R5: ±10%; R3, R4, R6: ±20%. C4: ±20%; other C: +50%, −20%.

Operating characteristics (Note 3):

Signal frequency: 400 ±20 cps.

Voltage amplification: 60.

Input impedance: 10KΩ.

Input signal, maximum output, 5% distortion: 80 mVac.

Maximum output, 5% distortion: 4.5 Vac.

Phase shift (Note 4): open loop: +55°; closed loop: +35°

Transistor heat sink requirements at 125°C: None.

Temperature range: −55°C to +125°C.

Power requirements: +25 volts ±10% at 6 ma (maximum)

(For Notes, see bottom of next page)

PSC 26 INSTRUMENT CONTROL PREAMPLIFIER

1. APPLICATION

This circuit is ideally suited for use as a voltage amplifier and driver for PSC 27, Instrument Control Power Amplifier. Provisions have been made to introduce degenerative feedback between the two circuits when required, and specific information regarding such application is included in the text. Other uses include relay operation as well as amplifier and driver for circuits similar to PSC 27 requiring a −55°C to +125°C temperature range and high gain stability. If the circuit is to be used to drive a servo power amplifier feeding a two-phase servo motor, provision must be made to acquire the appropriate phase shift.

2. DESIGN CONSIDERATIONS

This preamplifier is a modified form of a circuit that is frequently used in Naval equipment. The operating characteristics and performance of this circuit are within the regions required both by present equipments and by equipments currently under development.

The basic modification was to adapt the circuit for MIL–STD–701B silicon transistors and to provide for degenerative feedback from a power amplifier.

Direct coupling is employed to reduce the phase shift through the amplifier and thereby increase the phase margin for degenerative feedback. This type of coupling also permits the use of a large bias resistor, R4, for Q1, in order that a substantial input impedance may be maintained while still retaining operating point stability through the use of dc degeneration. AC degeneration is provided by emitter resistors R2 and R5, and is substantially increased when feedback loops are connected to points A and B. Provision for two feedback loops has been incorporated in the preamplifier because it is anticipated that the primary application of the circuit will be to drive a push-pull power amplifier similar to PSC 27. Because of transformer imperfections and transistor mismatch, the individual collector waveforms of a Class B push-pull amplifier show considerable distortion. However, since the two waveforms are similar (with the exception of amplitude when the two transistors are unmatched in ac beta), and are 180° out of phase, marked improvement in feedback characteristics is obtained when degeneration is applied to the preamplifier from both power amplifier collectors.

Maximum ac degeneration will be required when circuit application warrants high input impedance. Practically all error signal applications will require a minimum amplifier input impedance of 10KΩ. This level of impedance will require maximum feedback if operation over a −55°C to +125°C temperature range is required.

Notes:

1. These are maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

3. Output loaded with a 500Ω resistor. All output voltage measurements taken across the 500Ω load resistor. All performance specifications are based on data taken at 25°C and employing nominal value transistors.

4. Measured between input of PSC 26 and output of PSC 27 with input level at 10 mVac. Because phase shift is dependent upon load and is significant only when the application involves a two-phase motor, phase-shift data concerning the individual circuits are not presented. "Closed loop" designates external feedback from PSC 27 using a 330KΩ resistor between points labeled "A" on PSC 26 and PSC 27, and a 6.8KΩ resistor between points labeled "B". "Open loop" indicates no external feedback from PSC 27.

The 90° phase shift required by two-phase servo motors is often incorporated in similar circuits, but was omitted from PSC 26 for the following reasons: Such phase shift may result in regeneration when high degenerative feedback is employed; also, R–C phase-shift networks substantially reduce the gain at the error signal frequency while providing little attenuation to undesired harmonics unless elaborate network schemes are employed. For these reasons it is generally preferable to incorporate phase shift in the fixed-phase winding of the motor. However, in those applications that can tolerate the above-described conditions, as well as increased gain instability, degenerative feedback from the power amplifier may be omitted and a simple R–C network can be inserted at the amplifier input. Network attenuation will be compensated to a large extent by the reduced feedback, and high level input impedance will be maintained by the series impedance of the network. The essential details of such an application are included in section 3.

The base-to-collector capacitor, C4, serves to decrease the amplitude of signals above 1,000 cps by 6 db per octave as a precaution against high-frequency regeneration.

3. Performance

Variations from the stated operating characteristics have been minimized in PSC 26 so far as was considered practical. However, as with most transistor circuits, substantial variations attributable to temperature and transistor product variability still exist.

This section summarizes performance data on the major circuit characteristics of gain, input impedance, and phase shift over the temperature range of −55°C to +125°C. Variations of these three major characteristics resulting from use of transistors with minimum and maximum values of dc current gain are also presented in detail. The higher limit values of current gain for transistors Q1 and Q2 were 73 and 62, respectively. The lower limit transistors had a current gain of 31 and 30. These values approximate the upper and lower limits set by the applicable military specifications for these devices.

Comparison between open and closed loop phase shift characteristics when the preamplifier is used to drive PSC 27 is shown graphically. PSC 27 was loaded with a two-phase servo motor, as described in the text relating to that circuit. Points A on the two circuits were connected with a 330KΩ resistor and points B with a 6.8KΩ resistor. This amount of feedback resulted in a preamplifier gain reduction of approximately 50%.

Variations within the stated allowable change in either supply voltage or signal frequency, or both, result in negligible changes in circuit performance, even with the absence of external feedback.

Circuit gain is essentially constant with respect to input level up to approximately 4.5 volts output when employing transistors with nominal values of h_{FE}. At this point limiting action begins to take place in transistor Q2. Figure 26–1 shows preamplifier output volts at 25°C for a given input level at the two possible extremes of transistor dc current gain allowable under the appropriate military specification.

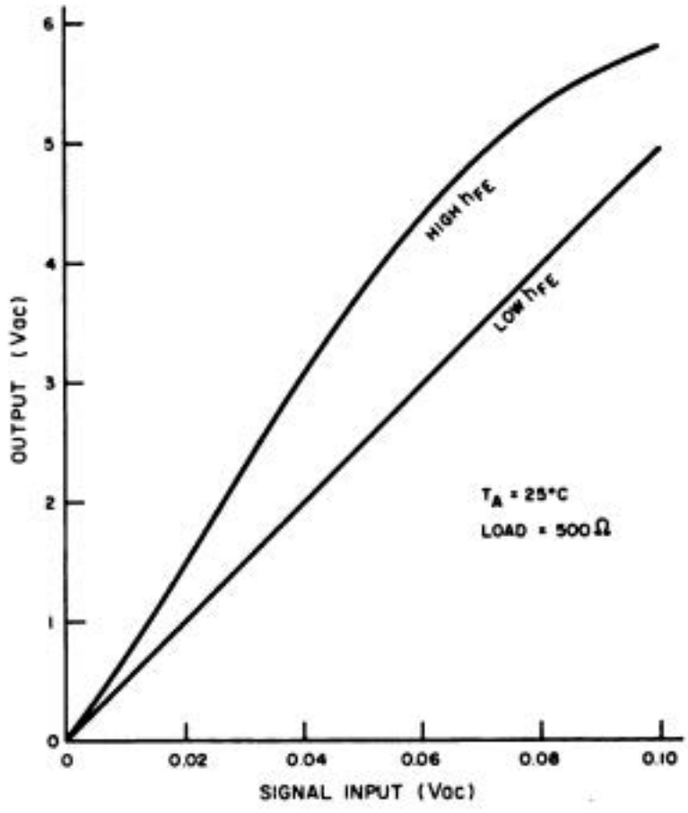


Figure 26–1.—Output Voltage vs. Input Signal Voltage for Upper and Lower Limit Values of h_{FE} at 25°C

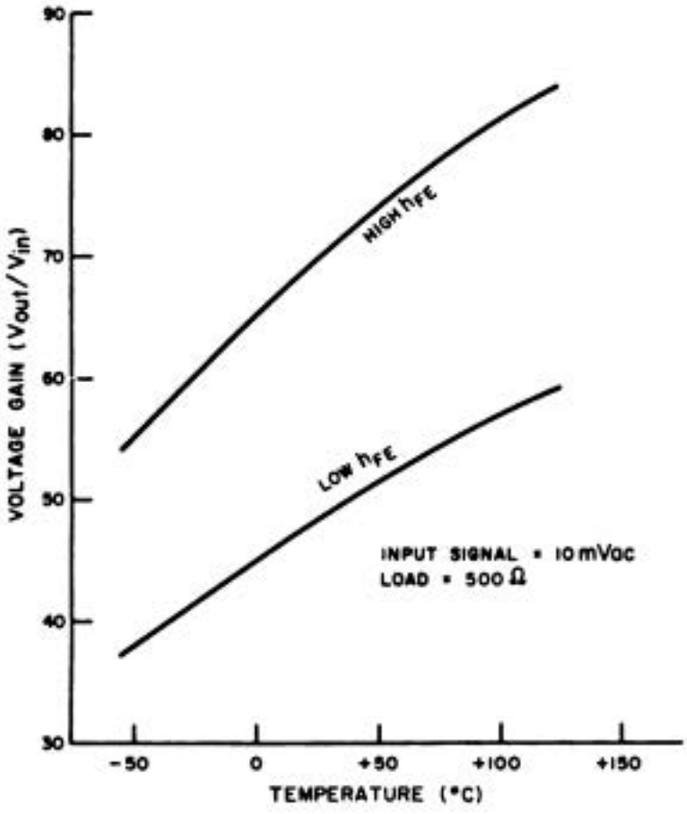


Figure 26–2.—Voltage Gain vs. Temperature for Upper and Lower Limit Values of h_{FE}

Additional gain variations due to temperature changes are expressed graphically in figure 26–2. Accumulative effects due to temperature and product variability could vary circuit gain by a factor of 2.3 to 1 with no external feedback. The addition of external feedback from PSC 27 would reduce this variability to a maximum of 1.1 to 1.

Figure 26–3 shows variations in input impedance vs. temperature. Close control of input impedance over wide temperature ranges is difficult since the impedance varies directly with transistor ac current gain. The current gain not only drops sharply at low temperatures but also has wide product variability limits. However, the input impedance of PSC 26 at worst-case conditions is still very nearly 10KΩ. Data for figure 26–3 were taken at a constant output distortion level of 5%. This is considered the maximum useful output level of the circuit.

Figures 26–4 and 26–5 show overall phase-shift variations encountered when PSC 26 is used to drive PSC 27. Phase shift was measured between the input to the preamplifier and the output of the power amplifier. External phase-shift networks must be used to acquire the 90° phase difference required between the control and fixed-phase windings of a two-phase servo motor. Substantial phase shift occurs within the two amplifiers, its extent varying markedly with operating conditions. Caution must therefore be observed in selecting the amount of additional phase shift required. Torque loss resulting from a phase difference of other than 90° should be at a minimum level at low amplitude inputs. The exact value of phase shift necessary to complement the inherent shift is dictated by maximum allowable error and required ambient temperature range. Motor torque is a function of the sine of the phase-shift angle which indicates that a phase difference of 60° between the motor windings would result in a 13.4% loss in available torque obtainable with a phase difference of 90°.

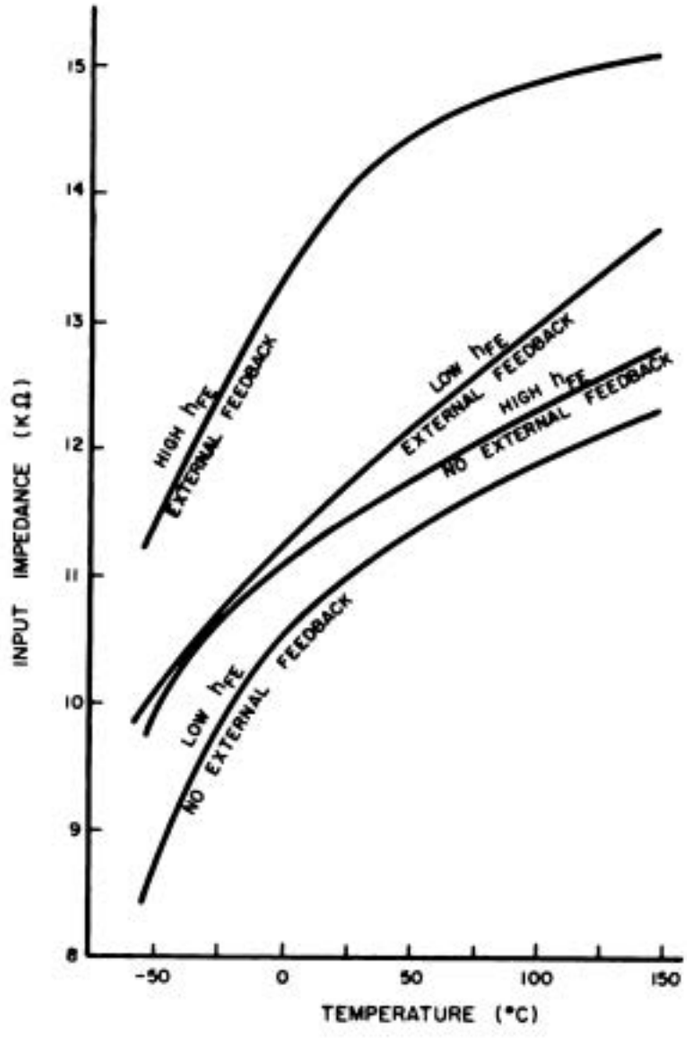


Figure 26–3.—Input Impedance vs. Temperature for Upper and Lower Limit Values of h_{FE}, with and without External Feedback

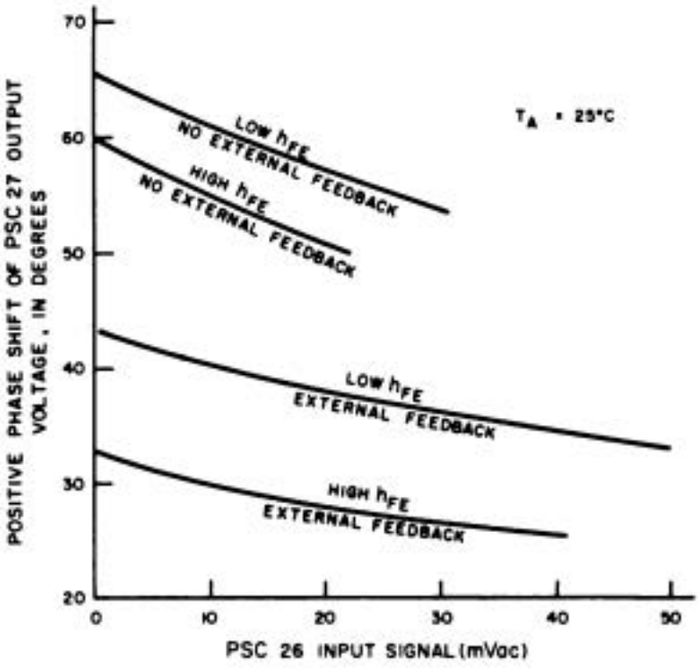


Figure 26-4.—Limits of Overall Phase Shift of Voltage Output of Power Amplifier PSC 27 vs. Input Signal Voltage of Preamplifier PSC 26, with and without External Feedback

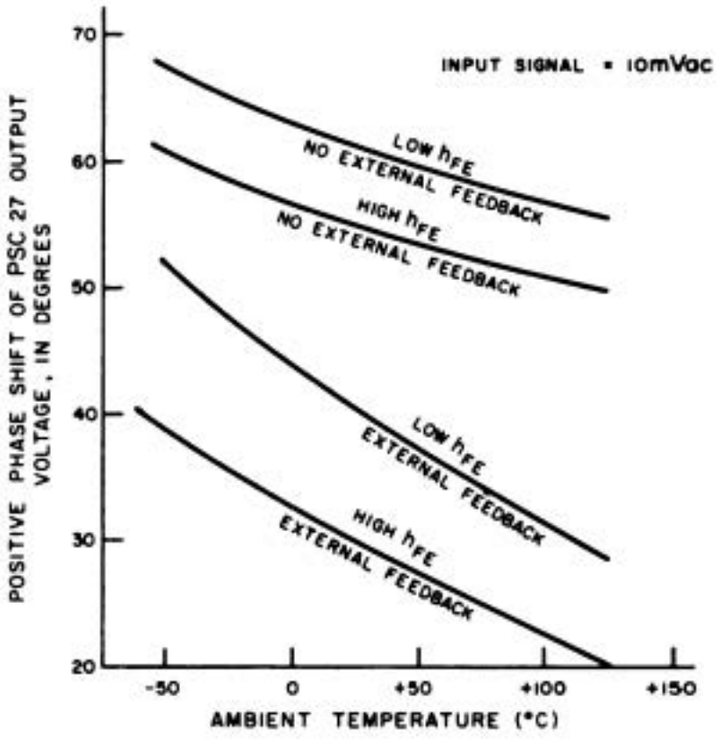
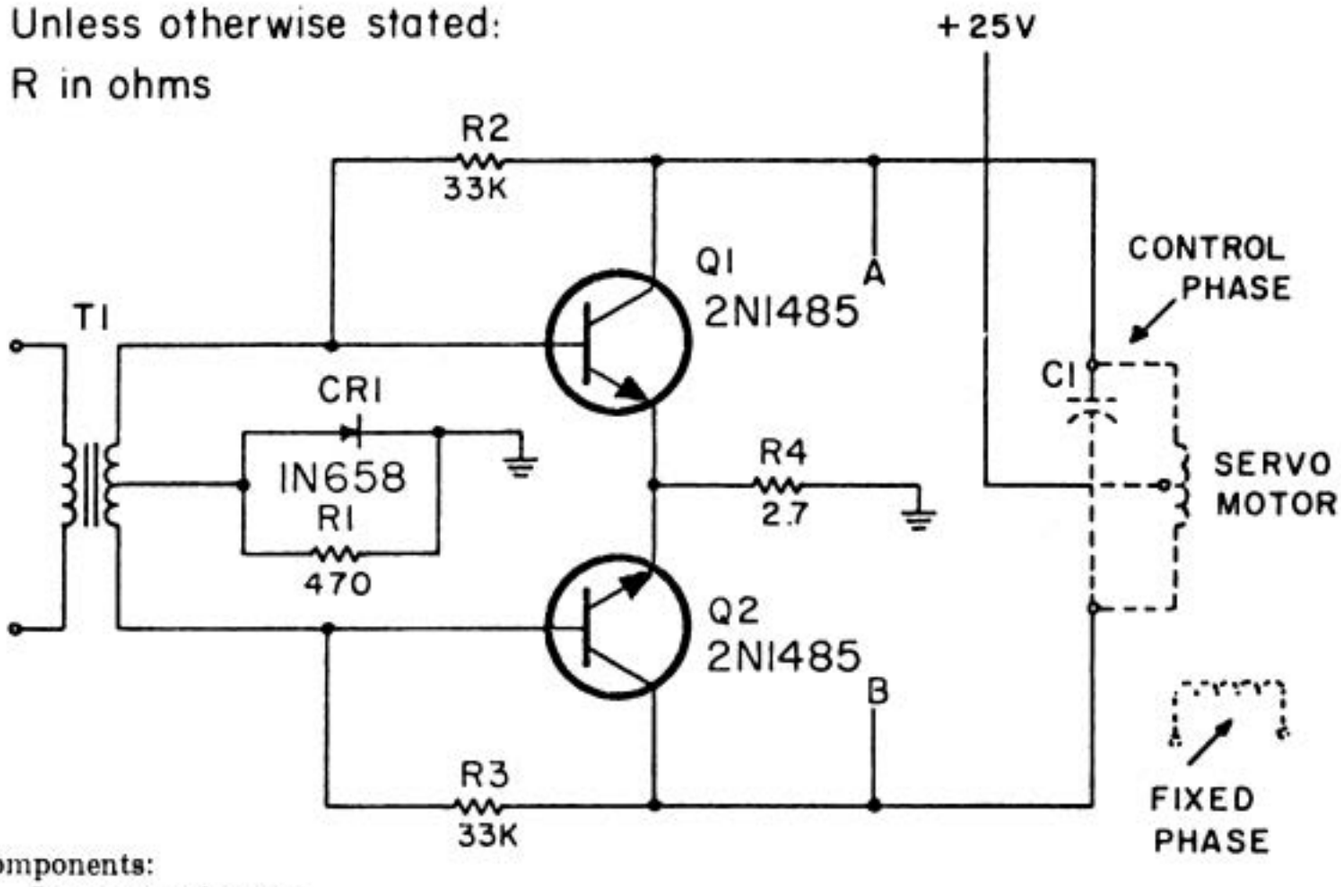


Figure 26-5.—Limits of Overall Phase Shift of Voltage Output of Power Amplifier PSC 27 vs. Temperature with Respect to Input Signal of Preamplifier PSC 26, with and without External Feedback

Notes

PREFERRED CIRCUIT NO. PSC 27
INSTRUMENT CONTROL POWER AMPLIFIER, 400 CYCLE

PREFERRED CIRCUIT NO. PSC 27
INSTRUMENT CONTROL POWER AMPLIFIER, 400 CYCLE



Components:

Input transformer:

DC resistance of primary: 100Ω.

Maximum primary current: 8 ma.

AC impedance: primary: 1,500Ω; secondary: 500Ω center-tapped.

C1: Capacitance chosen for a unity power factor with the servo motor under stall conditions.

Resistor power dissipation (Note 1): R4: 0.125 watt; R1, R2, R3: 0.1 watt.

Limits (these are not tolerances; see note 2): R1: ±10%; R2, R3, R4: ±20%.

Operating characteristics (Note 3):

Signal frequency: 380 to 420 cps.

Effective input impedance: Approximately 6KΩ.

Nominal power gain: 25 db.

Nominal power output at 5% distortion: 2.5 watts.

Effective load resistance: Approximately 80Ω collector to collector.

Operating temperature: −55°C to +125°C.

Transistor power dissipation: 1.0 watt maximum per transistor at 125°C and 5% distortion.

Transistor heat sink requirements (based on a safety factor of 2 to 1):

At temperatures to 85°C (Note 4): Ambient air to heat sink thermal resistivity <50°C/W.

At temperatures to 125°C (Note 4): Ambient air to heat sink thermal resistivity <30°C/W.

Power requirements:

Voltage: +25 volts ±10%

Current: Zero signal requires 20 ma maximum at 85°C and 30 ma maximum at 125°C. Maximum signal requires 235 ma at −55°C, 200 ma at +25°C, 190 ma maximum at +85°C and at +125°C.

(For Notes, see bottom of next page)

PSC 27 INSTRUMENT CONTROL POWER AMPLIFIER, 400 CYCLE

1. APPLICATION

The circuit provides up to 2.5 watts to drive the center-tapped control winding of a two-phase servo motor or other 400-cycle-powered electromechanical devices. The circuit functions at temperatures from −55°C to +125°C. The amplifier is designed to be driven by PSC 26, Instrument Control Preamplifier.

2. DESIGN CONSIDERATIONS

The 2N1485 silicon transistor is a guidance type on MIL-STD-701B. It was chosen for its low saturation resistance and high power-dissipation capability.

The input transformer serves both as an impedance matching device and a split-phase driver for the push-pull transistors.

The push-pull amplifier is operated near Class B with a slight forward bias. A bias potential of about 0.5 volt is developed across R1, with the dual effect of an increase in the gain of the circuit at low signal levels and a decrease in cross-over distortion. This result is accomplished by having each transistor conduct about 4 ma of collector current at zero signal level. To maintain this value of collector current at zero signal level as the ambient temperature changes, the base-emitter potential should vary with temperature. This variation is approximated by the use of a silicon diode-resistor combination in the bias circuit.

AC degeneration is provided by collector-to-base resistors, R2 and R3, that substantially reduce performance variations resulting from temperature changes and transistor product variability.

The control winding of a servo motor is the usual load on the push-pull stage. This load is tuned, by means of C1, for a power factor of 1 at 400 cps. A 90° phase shift between control signal and fixed-phase voltage is generally accomplished by a capacitor of appropriate size in series with the fixed-phase winding.

Transistor collector power dissipation, P_c, is computed as follows:

At maximum output:

$P_c = I^2 R_s/4$ where I is the peak current delivered to the load and R_s is the saturation resistance of the transistor.

At zero output:

$P_c = I_b V_{cc}$, where I_b is the collector current due to base-emitter bias and and V_{cc} is the supply potential.

3. PERFORMANCE

Input signal frequency variations within the stated allowable limits have no significant effects on circuit performance. A $\pm 10\%$ change in supply voltage will have negligible effect on performance, provided that the input signal is below that required to produce limiting action in the two transistors. When limiting is involved, output power is a function of the square of the supply voltage for a given level of distortion.

Notes:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

3. Obtained with Type ACC-10-A-4 Servo Motor (Clifton Precision Products Company) or equivalent, used as a load under stall conditions. The value of C1 was set at 1.5 mf to approximate unity power factor. The values given are typical at +25°C unless otherwise stated.

4. Any commercially available heat dissipating device will normally possess a thermal resistivity to air that is substantially below that required in this application. The thermal resistivity to air of a 2″ x 2″ x 3/32″ piece of aluminum is approximately 8°C/W.

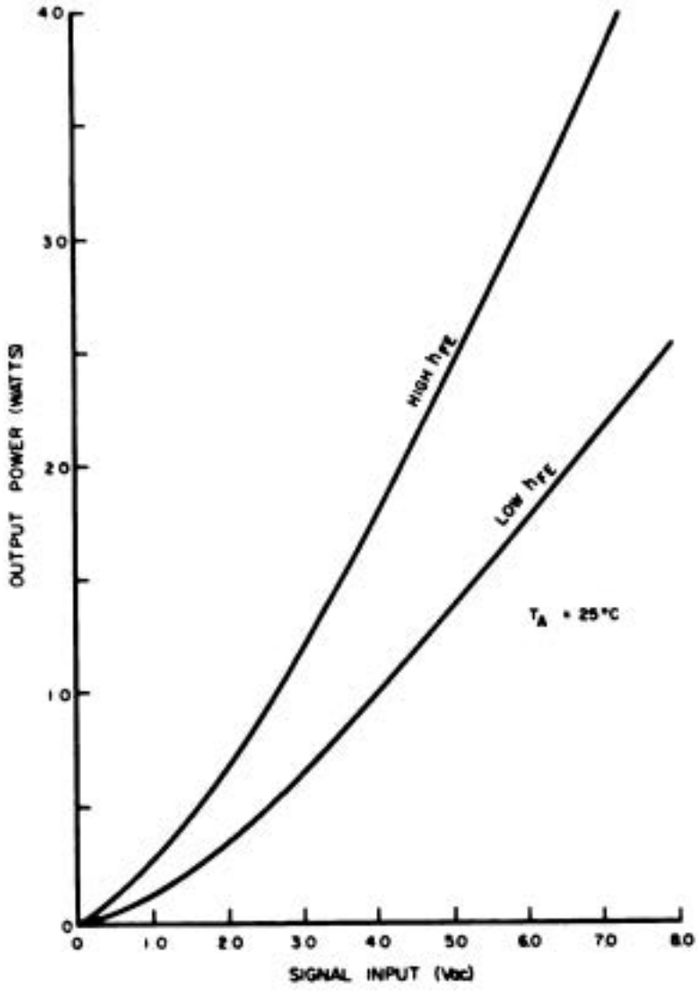


Figure 27-1.—Output Power vs. Input Signal at 25°C with High and Low Limit Values of DC Current Gain

Output power as a function of input voltage is shown graphically in figure 27-1 for approximate upper and lower Military Specification limit values of transistor dc current gain at 25°C. The high-limit transistors used in obtaining performance data had a matched current gain of 100, and the low-limit transistors had a matched current gain of 37. For a given temperature, output power is approximately a linear function of input rms voltage. The 5% distortion point is reached at approximately 2.75 watts of output for both the high- and low-gain transistors at 25°C. This fact is not apparent in figure 27-1, because the relationship of output current and voltage is such that output power increases linearly over the region shown. The distortion in question is due primarily to clipping rather than nonlinearity.

Figure 27-2 shows output power as a function of temperature for a signal input level of 6.5 Vac (approximately 7 mw). Variation in power gain is approximately 1 db over the stated ambient temperature range for a given amplifier. Worst-case power gain variation between any two amplifiers is less than 3.5 db, which includes the cumulative effects of temperature change and product variability.

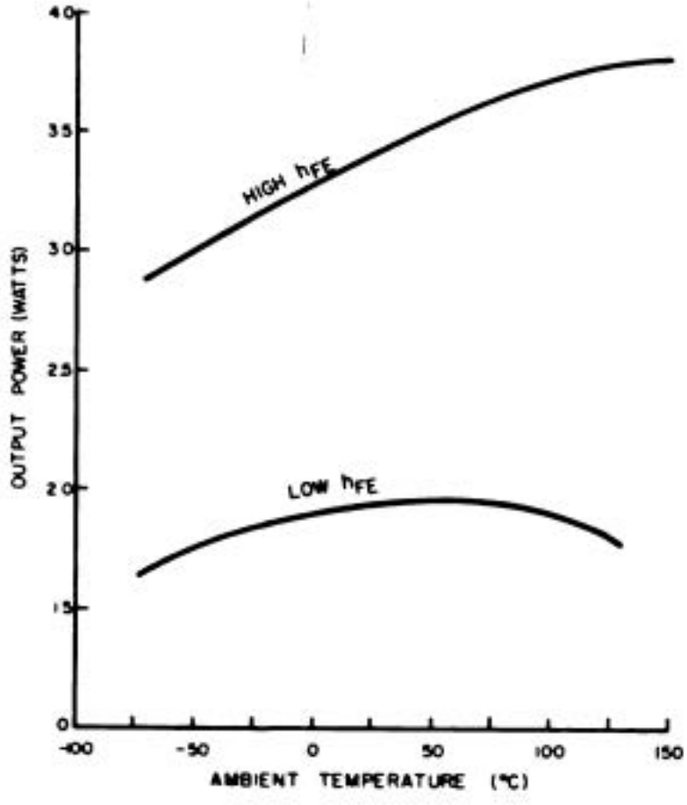
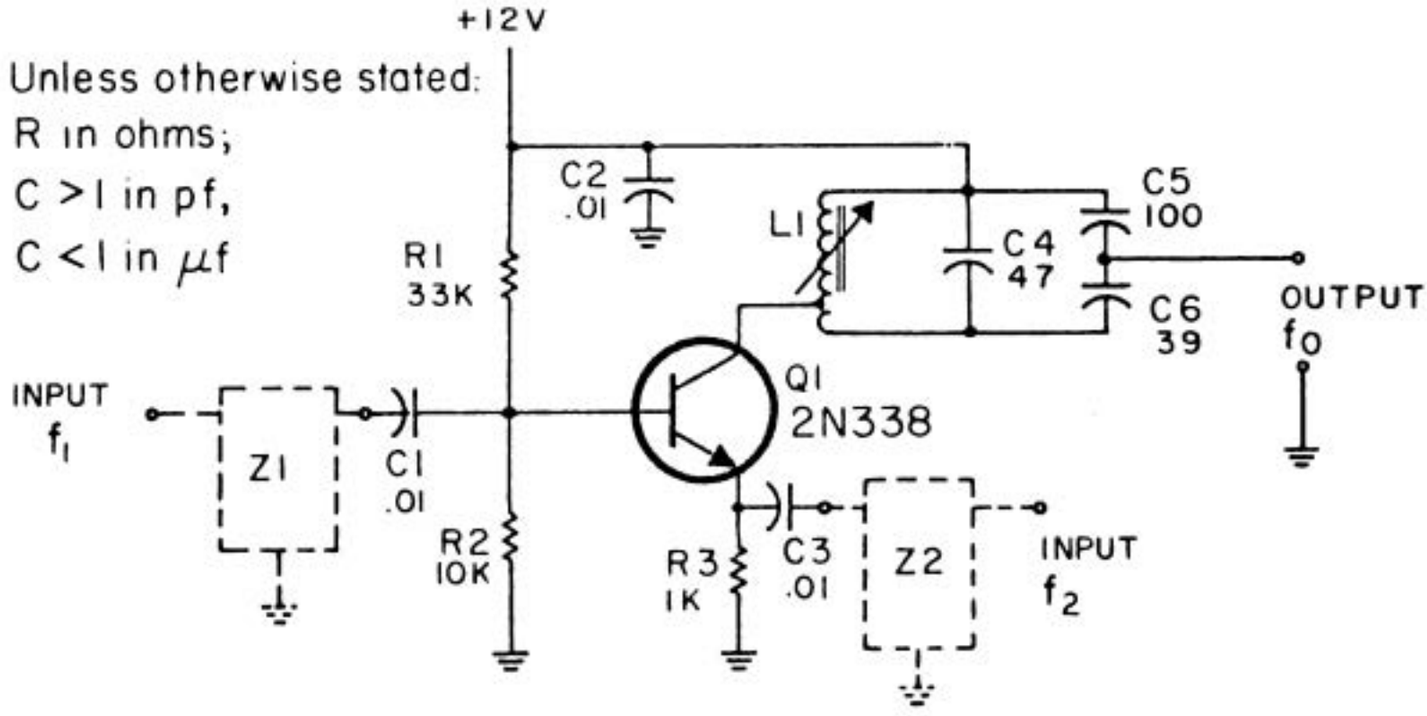


Figure 27-2.—Output Power vs. Ambient Temperature at Input Signal Level of 6.5 Vac with High and Low Values of DC Current Gain

Notes

PREFERRED CIRCUIT NO. PSC 28
RF MIXER

PREFERRED CIRCUIT NO. PSC 28
RF MIXER



Components:

L1: Inductor: Permeability tuned, 178–300 μh, tapped ⅛ down from "hot" end (Note 1).

Z1: Impedance transforming network for matching source impedance to input impedance. See section 2.

Z2: Impedance transforming network to match impedances at f_2 and to provide a low impedance at f_0. See section 2.

Resistor power dissipation (Note 2): All R: <0.1 watt.

Limits (these are not tolerances; see note 3): All R: ±10%. C1, C2, C3: ±20%; C4, C5, C6: ±10%.

Operating characteristics at 25°C:

Input frequencies: f_1=3 mc; f_2=2 mc.

Input impedance at f_1: 2,000Ω (Note 4).

Input impedance at f_2: 1,000Ω.

Output frequency, f_0: 1 mc.

Optimum load resistance at f_0: 1,000–2,000Ω (Note 5).

Conversion power gain: 30±2 db (see figure 28-1).

Local oscillator injection power level: 1 mw.

Power requirements: +12 volts ±10% at 2.5 ma (maximum) (Note 6).

(For Notes, see bottom of next page)

PSC 28 RF MIXER

1. APPLICATION

This circuit may be used as an RF mixer or as a frequency synthesizer. The input and output circuits can be tailored to accommodate specific input and output frequency requirements within the capability of the chosen transistor type. The use of a silicon transistor permits circuit operation over the temperature range of −55°C to +125°C.

2. DESIGN CONSIDERATIONS

The RF mixer (or frequency synthesizer) is essentially an RF amplifier which mixes two input frequencies to obtain an output frequency equal to either the sum or difference of the input frequencies, as desired. In an optimum design, the maximum conversion power gain will be about 3 db less than that achieved when the transistor is used as an RF amplifier at the highest input frequency.

If the circuit is to be used as an RF mixer, the same considerations necessary for the design of a high-performance RF or IF amplifier are required, and it may be desirable to accept a reasonable trade-off between maximum conversion gain, circuit stability, and selectivity. The procedure involves connecting the collector of the transistor to a suitable tap on the inductor in the output circuit. For the type 2N338 transistor, it was found that approximately 3–4 db of additional gain was possible by moving the tap ⅛ of the total number of turns down from the "hot" end of the output tank inductor. For higher-gain transistor types (such as the type 2N706), it may be necessary to move the tap even closer to the ground end of the inductor to prevent oscillation. Improved selectivity can be achieved by moving the tap closer to the RF ground end of the inductor than is required for maximum circuit gain. Selectivity can be improved through the use of high-Q inductors or transformers, and relatively high values of capacity in the tank circuits, consistent with resonance requirements.

The output circuit uses a capacitor-impedance-matching network, which is easier to work with in construction and adjustment than the generally used link-coupling or tapped-tank methods. The output circuit gives a good match to a range of resistive loads from 1,000Ω to 2,000Ω.

The input circuits may use tapped-tank, link-coupling, or capacitor-impedance-matching methods, whichever is most suitable for the individual application. In the design of an RF communications mixer using emitter injection of the local oscillator signal, it is particularly important that the coupling capacitor and the inductive coupling to the local oscillator present a very low impedance to the output frequency, f_0. In the design of very-high-frequency mixers, the base-to-emitter impedance must be low at the IF frequency to avoid degeneration. If link coupling or a tapped input RF-to-mixer in-

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Notes:

1. Electrically similar to No. 4315, J. W. Miller Co. (See section 2 regarding collector tap.)
2. In determining maximum power dissipation, allowances have been made for variation in component values, power supply voltages, and transistor characteristics.
3. The performance specifications are based on component values which do not deviate from the nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.
4. The input impedance varies with individual transistors and with ambient temperature. Typical values for r_{ieb} for the type 2N338 are of the order of 2,000Ω to 2,500Ω; C_{ieb} values are of the order of 18 pf.
5. Conversion gain for both high-gain and low-gain transistors varies less than 0.5 db when a resistive load is varied from 1,000–2,000Ω.
6. This circuit may be supplied from a +25-volt source using a 5,600Ω, ½-watt series dropping resistor.

terstage transformer is used, this requirement usually can be met; however, if a capacitor matching circuit is used, it may be necessary to insert a trap between base and emitter, series-tuned to the IF frequency, to meet this requirement.

In some frequency synthesizer applications, where optimum conversion gain and selectivity are not required, both input signals are injected at the base of the transistor, one by means of an impedance transforming network, and the other by a small coupling capacitor on the order of 10–15 pf for purposes of isolation. Some applications have permitted the use of small coupling capacitors for both inputs. The emitter bias circuit, however, must be adequately by-passed for all frequencies; f_1, f_2, and f_0.

3. PERFORMANCE

The effects of the variability of electrical characteristics between transistors on conversion power gain and output power, as related to ambient temperature and to the f_1 base drive voltage, are shown in figure 28–1. For this test, a load resistance of 1,000Ω was used. The f_2 emitter injection power was held constant at 1 mw. (It was found that there was little difference in conversion gain for f_2 emitter injection levels of 0.8 to 1.4 mw.) The transistors used in the test, representative of a typical production spread, had measured gains of 33–36 db when used in a typical RF amplifier at 1 mc, and 28–31 db at 3 mc.

The effect of reducing the supply voltage by 10% resulted in less than 0.5 db drop in conversion gain at −55°C, 25°C, and 125°C; increasing the supply voltage by 10% resulted in less than 1 db increase in conversion gain at these ambient temperatures.

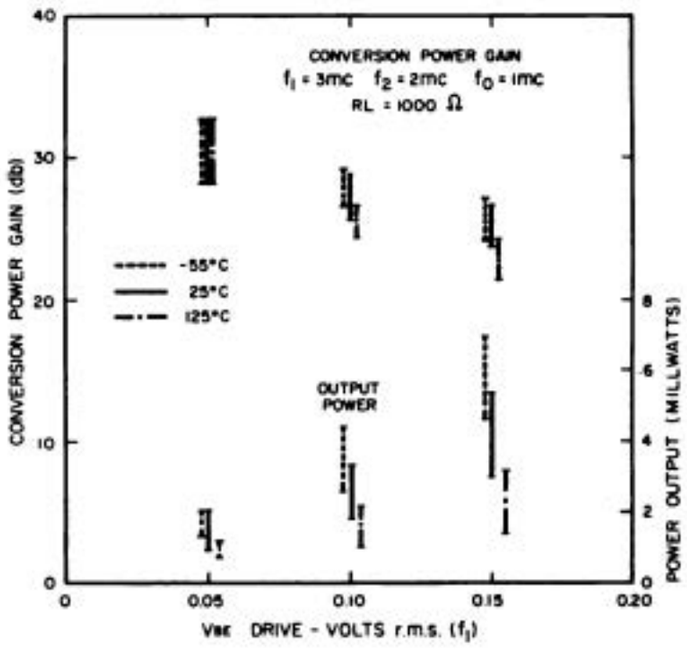


Figure 28–1.—Effect of Transistor Variability on Conversion Power Gain and Output Power as Related to f_1 Drive Voltage [P(f_2)=1 mw]

Notes

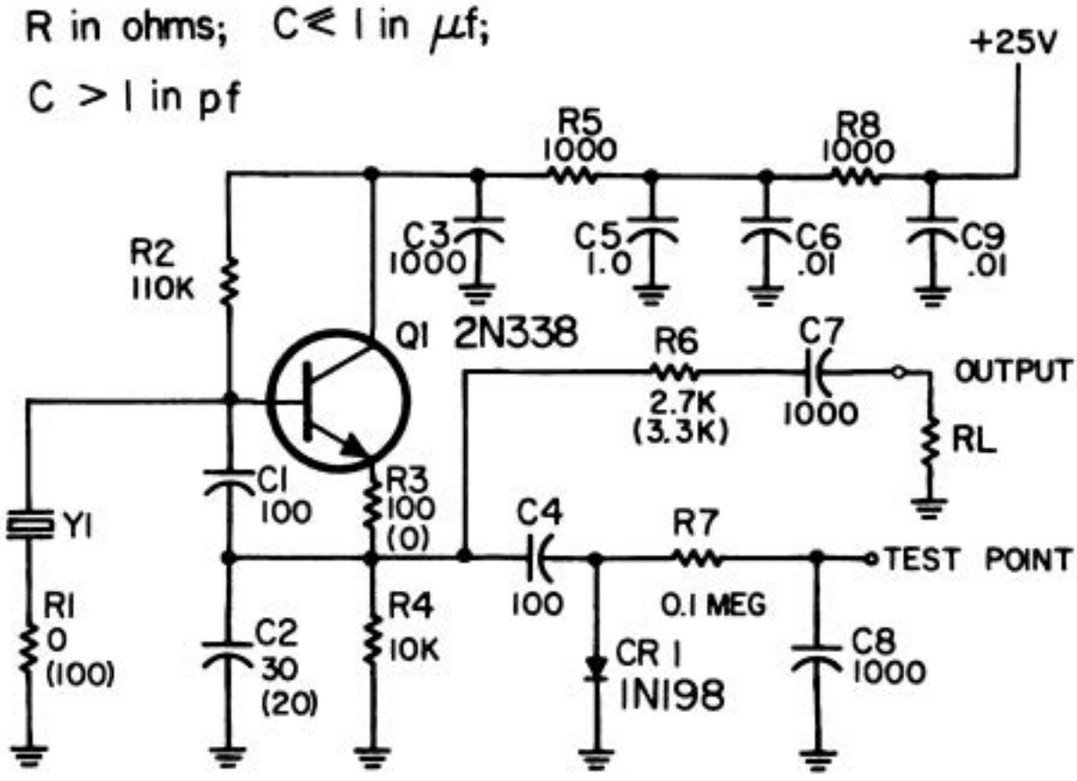
PREFERRED CIRCUITS NOS. PSC 29A, PSC 29B
CRYSTAL OSCILLATORS, 2.4 TO 5.0 mc

PREFERRED CIRCUITS NOS. PSC 29A, PSC 29B
CRYSTAL OSCILLATORS, 2.4 TO 5.0 mc

Unless otherwise stated:

R in ohms; C ≤ 1 in μf;

C > 1 in pf



(PARTS VALUES IN PARENTHESES ARE CHANGES FOR PSC 29B)

Components:

Y1: see note 1.

Resistor power dissipation (Note 2): R1, R2, R4, R5, R6, R7: <3 mw; R3: 22.5 mw.

Limits (these are not tolerances; see note 3): R2: ±2%; R1, R3, R4: ±10%; all others ±20%. C1, C2: ±10%; all others: ±20%.

Operating characteristics:

Temperature range: −55°C to +105°C (Note 1).

Output voltage (Note 4): 0.5 to 1.2 volts peak at 2.4 mc, 0.4 to 0.9 volt peak at 5 mc, with a load resistance of 1,000Ω over the required temperature range.

Frequency stability vs. ambient temperature (ref. temp.=25°C):

PSC 29A: 49 ppm (maximum) over the temperature range of −55°C to +125°C at 2.4 mc; 32 ppm (maximum) over the temperature range of −55°C to +125°C at 5.0 mc.

PSC 29B: 41 ppm (maximum) over the temperature range of −55°C to +125°C at 2.4 mc; 39 ppm (maximum) over the temperature range of −55°C to +125°C at 5.0 mc.

Frequency stability vs. supply voltage variations of ±10%:

PSC 29A: 2 ppm (maximum) from −55°C to 85°C at 2.4 mc; 5 ppm (maximum) at +125°C and 2.4 mc; 3 ppm (maximum) from −55°C to +85°C at 5.0 mc; 24 ppm (maximum) at +125°C and 5.0 mc.

PSC 29B: 4 ppm (maximum) from −55°C to +85°C at 2.4 mc; 5 ppm (maximum) at +125°C and 2.4 mc; 6 ppm (maximum) from −55°C to +85°C at 5.0 mc; 8 ppm (maximum) at +125°C and 5.0 mc.

Frequency stability vs. change in value of C1 or C2 of ±10% (Note 5):

PSC 29A: 13 ppm (maximum) for a ±10% change in C1; 25 ppm (maximum) for a ±10% change in C2.

PSC 29B: 19 ppm (maximum) for a ±10% change in C1; 25 ppm (maximum) for a ±10% change in C2.

Frequency stability vs. transistor product variability (Note 5):
PSC 29A: 8 ppm (maximum).
PSC 29B: 15 ppm (maximum).
Test point voltage range at 25°C: −3 to −6 volts.
Power requirements: +25 volts ±10% at 1.5 ma (maximum).

Notes:

1. Crystal type CR-18A/U is rated at −55°C to +105°C ±3°C in MIL-STD-683, 3 February 1961. Manufacturers can supply them on special order for operation at temperatures from −55°C to +125°C. The operating characteristics specified herein at +125°C are based on units procured under such special order to the manufacturer. Except for the extended temperature range, these units are identical to stock CR-18A/U crystals.

2. These are the maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

4. Output voltage will vary with temperature, load impedance, effective crystal series resistance, and transistor characteristics. The maximum and minimum output values were measured with transistors having dc betas of 118 and 60, respectively, to represent a typical range of values. The maximum dc beta of this type is rated at 150, the typical value is 80, and the minimum is 45.

5. Stated frequency shift is the maximum attributed to the effects of C_1 and C_2 but does not include any shift attributable to temperature.

PSC 29A, PSC 29B CRYSTAL OSCILLATOR, 2.4 TO 5.0 MC

1. APPLICATION

1.1 *Circuit PSC 29A, sine wave output:* This oscillator serves as the source of a reasonably good sine wave of sufficient stability to be usable in frequency synthesizer and local oscillator circuits. The principal advantage of this Colpitts type of circuit is that its frequency can be changed by the substitution of crystals without the necessity of changing or adjusting a tank circuit. This feature is important in subminiature equipments where band switching is required. The PSC 29A circuit may be used with PSC 28, R–F Mixer Circuit.

1.2 *Circuit PSC 29B, harmonic output:* This modification of PSC 29A provides a distorted sine wave for use in driving frequency multiplier circuits.

1.3 *Higher frequency operation:* For sine wave output at 4.5 to 18 mc, see Preferred Circuit PSC 30. The latter is another version of the Colpitts circuit.

2. DESIGN CONSIDERATIONS

2.1 *Circuit configuration:* The common-collector circuit permits operation with the highest input impedance of the three common configurations. The impedance is roughly beta times the load resistance. The crystal operates in the antiresonant mode as a high inductance in series with a very small capacitor, both being paralleled by the circuit capacitances C1, C2, by input capacitance of the 2N338, and by stray capacitances. The higher input impedance of this circuit does not load the crystal circuit as much as would the common-base or common-emitter configurations.

2.2 *Frequency range:* Several limiting factors are encountered in the design of an oscillator of this type for use over a wide temperature range. At frequencies below about 2 mc, it is difficult to achieve reliable starting with all crystal samples under all conditions. The circuit will still operate at 1 mc, providing no subnormal temperatures are encountered. As frequency increases up to 5 mc, the crystal activity improves generally but the transistor gain drops, producing a limiting condition for any single circuit configuration.

The lower frequency limit of 2.4 mc was chosen to insure build-up of oscillations at a supply voltage 10% lower than the 25-volt nominal over the temperature range of −55°C to +125°C. The 5 mc upper limit was established because of rapid reduction in output with the chosen transistor type at higher frequencies, and the greater effects of transistor and crystal product variabilities.

The frequencies of a number of transistorized oscillators currently being used in military aircraft equipments fall within this selected range. Where lower-frequency oscillators are used, they usually consist of two transistors in a multivibrator or a modified Butler oscillator using the crystal in series resonance.

2.3 *Choice of transistors*: The type 2N338 transistor was selected for this circuit because it permits operation at 2.4 to 5 mc over a wide temperature range, and provides adequate output and reliable starting up to at least 5 mc. It is a preferred type in MIL–STD–701B, and is available from several sources.

2.4 *Choice of crystal unit:* The type CR–18A/U crystal unit was chosen because it has the widest temperature range of the preferred crystal types that are antiresonant over the desired frequency range. Its frequency range is 0.8 to 20 mc, and its temperature range is −55°C to +105°C. It has a frequency tolerance of ±0.005% (50 ppm). The type CR–36A/U unit may also be used. It has similar characteristics, but is designed for temperature-controlled operation at 80°C to 90°C, and has a tolerance of ±0.002% (20 ppm). Crystal manufacturers can deliver CR–18A/U units for operation over the temperature range of −55°C to +125°C. The values of circuit frequency stability listed under Operating Characteristics are for the most adverse combinations of these higher-temperature crystals and transistors having a wide spread of characteristics.

Note that the product variability of the transistors contributes materially to the fre-

quency deviation. This is due mainly to wide variations in their input capacitances. Values measured by one manufacturer for the type 2N338 with fixed parameters showed a spread of 16 to 42 pf at 1 mc, and a spread of 6 to 23 pf at 10 mc.

The output voltage level of the circuit is dependent, in part, on the effective series re-resistance of the crystal and, hence, on the crystal's activity. A wide tolerance on the series-resistance characteristic is permitted by MIL-C-3098B.

Crystal drive power, measured in the circuit, is less than 2 mw. The level used in measuring crystal characteristics on the standard test set is 10 ± 2 mw up to 10 mc. This difference in drive power will cause some minor differences in frequency of operation and equivalent series resistance, as used in the circuit, from the values obtained on the standard test set.

2.5 *Crystal loading capacitance:* The standard crystal units of type CR-18/AU are required to operate with a maximum frequency deviation of 50 ppm over the specified temperature range when shunted by a capacitive load of 32 pf. The experimental subassemblies used for testing of the PSC 29A and PSC 29B circuits did not employ rotary switching for the changing of crystals. Stray capacitance across the crystals was therefore not of the value required, in combination with C1, C2, and the input capacitance of the transistor, to provide 32 pf. The result was operation at frequencies somewhat higher than specified. In actual applications, bandswitching is usually required, and provides the additional capacitance. If a single frequency circuit is required, a small trimmer capacitor connected across the crystal will provide the additional load capacitance.

2.6 *Parasitic suppression:* The resistor, R1, in series with the grounded leg of the crystal in PSC 29B serves to eliminate parasitic oscillations that can occur with some combinations of crystals and transistors.

2.7 *Feedback voltage divider:* The capacitive feedback voltage divider, C1 and C2, has optimum values for each capacitor at each frequency, and for each combination of crystal, transistor, and stray capacitance. The values chosen are not necessarily optimum for each frequency, but will give satisfactory performance over the specified frequency range. The effects of $\pm 10\%$ changes in C1 or C2 are listed under Operating Characteristics.

2.8 *Supply voltage filter:* The double-pi RC filter is used in some airborne communications receivers, but may not be necessary in other applications.

2.9 *Test point:* The test-point circuit provides a negative dc voltage to indicate the presence and relative level of oscillator output. The voltage varies with frequency, transistor characteristics, and crystal activity. This test circuit has negligible effect on the performance of the oscillator.

2.10 *Distortion:* The amount and type of distortion in the output waveform varies as some function of frequency, temperature, transistor product variability, and load. In PSC 29A, an attempt is made to minimize distortion by means of negative feedback provided by R3.

2.11 *Load impedance:* To assure reasonably high load impedance, resistor R6 is inserted in series with the output. Its value of 3,300Ω in PSC 29B may be reduced to 2,700Ω, as used in PSC 29A, to increase output. As load resistance is increased, distortion is decreased. The optimum value for maximum power transfer is dependent upon frequency. The value of 1,000Ω for R_L was employed for measurements of the the circuit's characteristics. This value, chosen as typical of the loads actually used, is somewhat lower than optimum but high enough to give results similar to those obtained with optimum values.

3. PERFORMANCE OF PSC 29A

3.1 *Frequency stability:* Figure 29-1 shows that the frequency stability of the circuit over the temperature range of −55°C to +125°C was within the MIL-STD-683 stability requirement for the crystal of 50 ppm over the temperature range of −55°C to +105°C.

3.2 *Output voltage vs. temperature:* At −55°C, the output falls to about 70% or 80% of the 25°C level. The output voltage at 125°C is approximately 50 to 60% of the output voltage

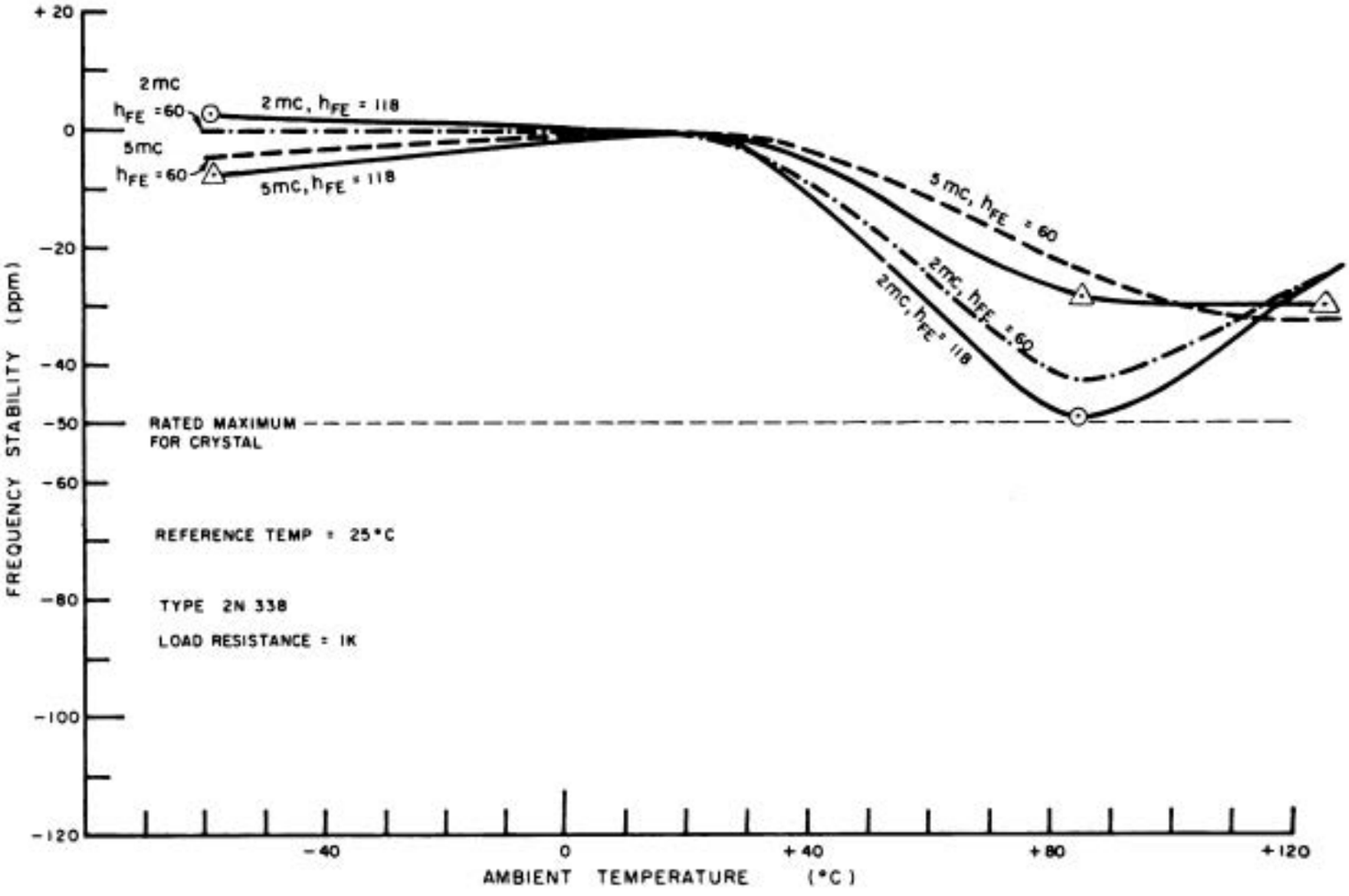


Figure 29–1.—Frequency Stability with Temperature for Sine Wave Output Circuit (PSC 29A)

at 25°C. Figure 29–2 shows the variation obtained in output voltage by use of a low-dc-beta transistor and a high-dc-beta transistor at 2.4 and 5.0 mc. Voltage measurements were made across a load of 950Ω with an oscilloscope and a high impedance probe having a shunt capacitance of 14 pf. This shunt capacitance serves to simulate the input capacitance of a following transistor stage.

3.3 *Output power vs. load:* At room temperature, with the high-beta transistor and a load of 2,650Ω, the circuit provided an output power at 2.4 mc of 1.3 mw. This was more than twice the output obtained with a load of 950Ω and the same transistor. As shown in figure 29–3, the output at 5.0 mc with either transistor, and at 2.4 mc with the low-beta transistor, was more constant with changes in load resistance. This was due to the shunt capacitance of the measuring instrument which gave a maximum impedance of 2KΩ at the highest frequency.

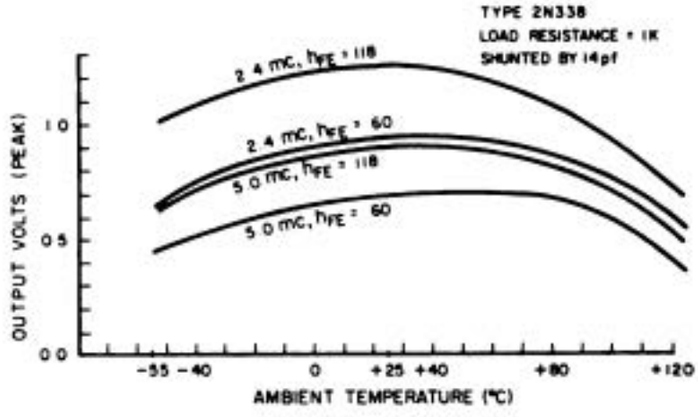


Figure 29–2.—Output Voltage vs. Temperature for Sine Wave Output Circuit (PSC 29A)

3.4 *Output waveform:* For a particular transistor and crystal combination in these oscillators, the output waveform at a fixed frequency may be made almost purely sinusoidal by careful adjustment of the values of C1 and C2 and the bias. For a range of frequencies, however slight distortion must be tolerated with fixed values of C1 and C2 to assure starting under

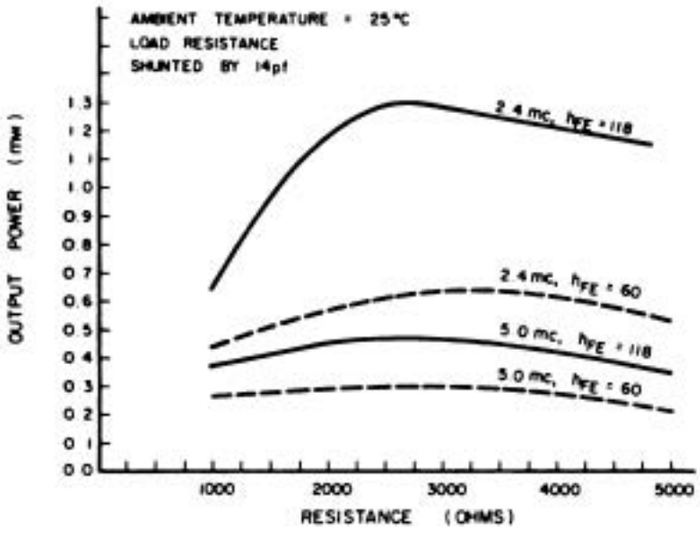


Figure 29–3.—Output Power vs. Load Resistance for Sine Wave Output Circuit (PSC 29A)

adverse product variability, supply voltage, and temperature conditions. The amount of distortion present increases slightly with temperature changes. PSC 29A provides good waveform from −55°C to 125°C. The amount of distortion decreases with an increase in frequency. In figure 29–4, the output waveforms at three frequencies at room temperature are shown for a typical transistor and crystal combination used in this circuit.

4. PERFORMANCE OF PSC 29B

4.1 *Frequency stability:* Figure 29–5 shows that, for circuit PSC 29B, the maximum deviation in frequency occurs at about 85°C. The stability vs. temperature curves are similar to those for PSC 29A.

4.2 *Output voltage vs. temperature:* In figure 29–6, output voltage is seen to be reasonably constant, for a given transistor and crystal, as temperature is raised above 25°C. The output levels are somewhat lower than those of PSC 29A, mainly because of the larger value of R6 used in series with the output.

4.3 *Output power vs. load resistance:* The curves in figure 29–7 indicate that, for maximum power output at 2.4 mc, a load resistance of

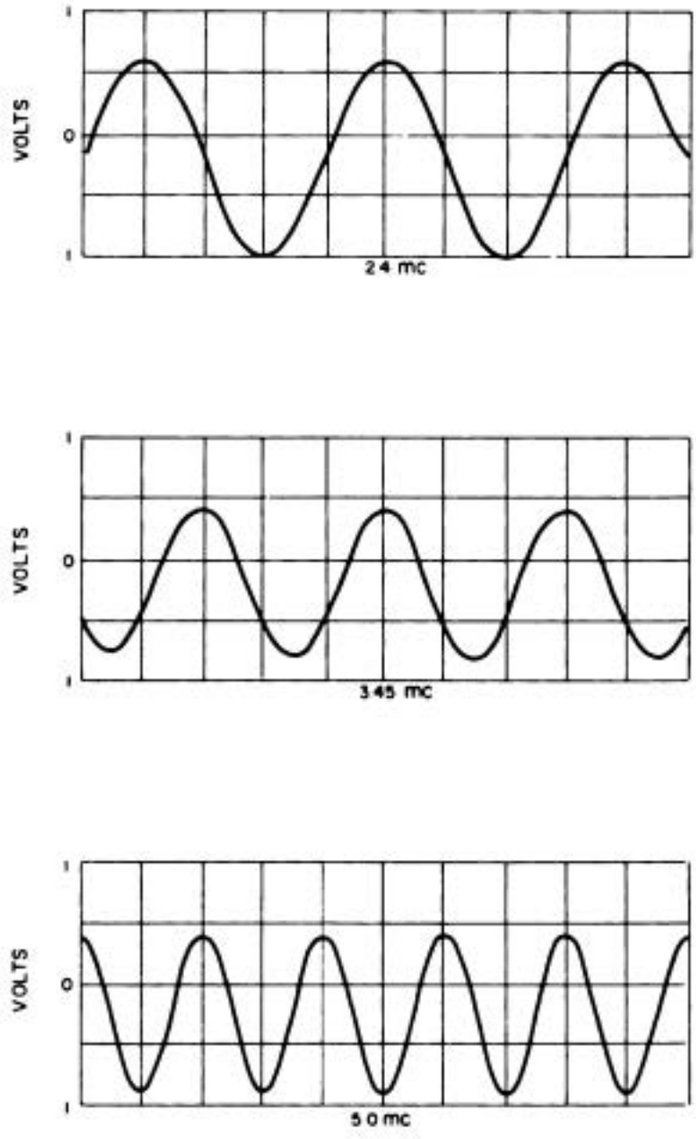


Figure 29–4.—Output Waveform at 25°C for Sine Wave Output Circuit (PSC 29A)

3,000Ω to 4,000Ω is required. The output power at 5 mc is maximum with a load of from 1,000Ω to 2,000Ω.

4.4 *Output waveform:* Figure 29–8, showing typical output waveforms for PSC 29B, illustrates the distortion resulting from omission of R3 from this circuit, as compared to PSC 29A. The measurements were made at 25°C with a load resistance of 2,000Ω. The waveforms obtained with a load of 1,000Ω are almost identical, but output levels are lower and distortion is slightly greater.

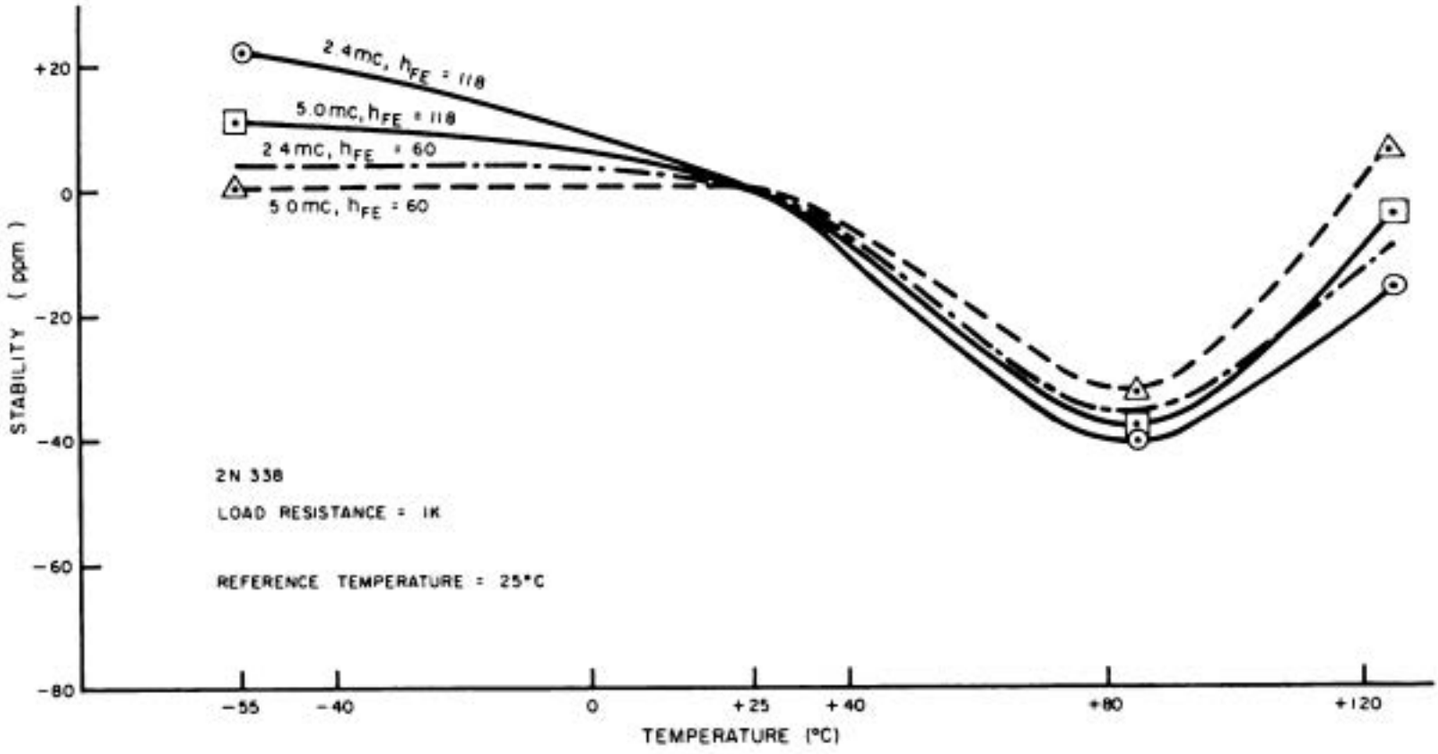


Figure 29–5.—Frequency Stability vs. Temperature for Harmonic Output Circuit (PSC 29B)

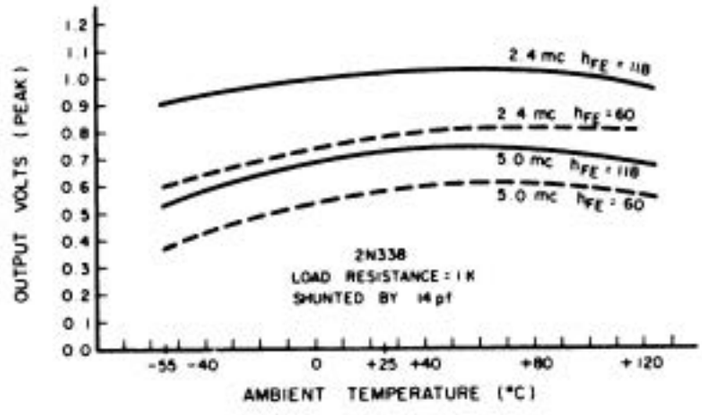


Figure 29–6.—Output Voltage vs. Ambient Temperature for Harmonic Output Circuit (PSC 29B)

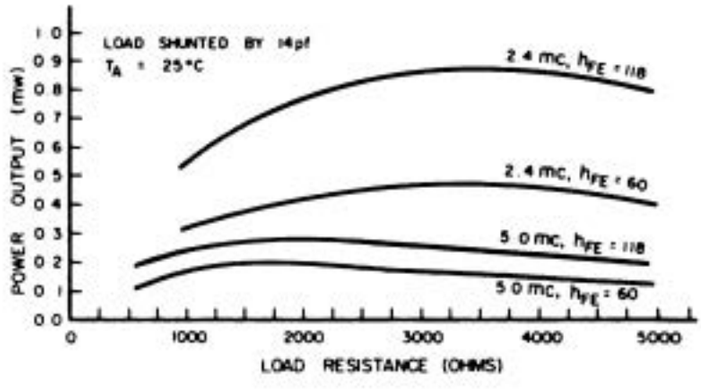


Figure 29–7.—Power Output vs. Load Resistance for Harmonic Output Circuit (PSC 29B)

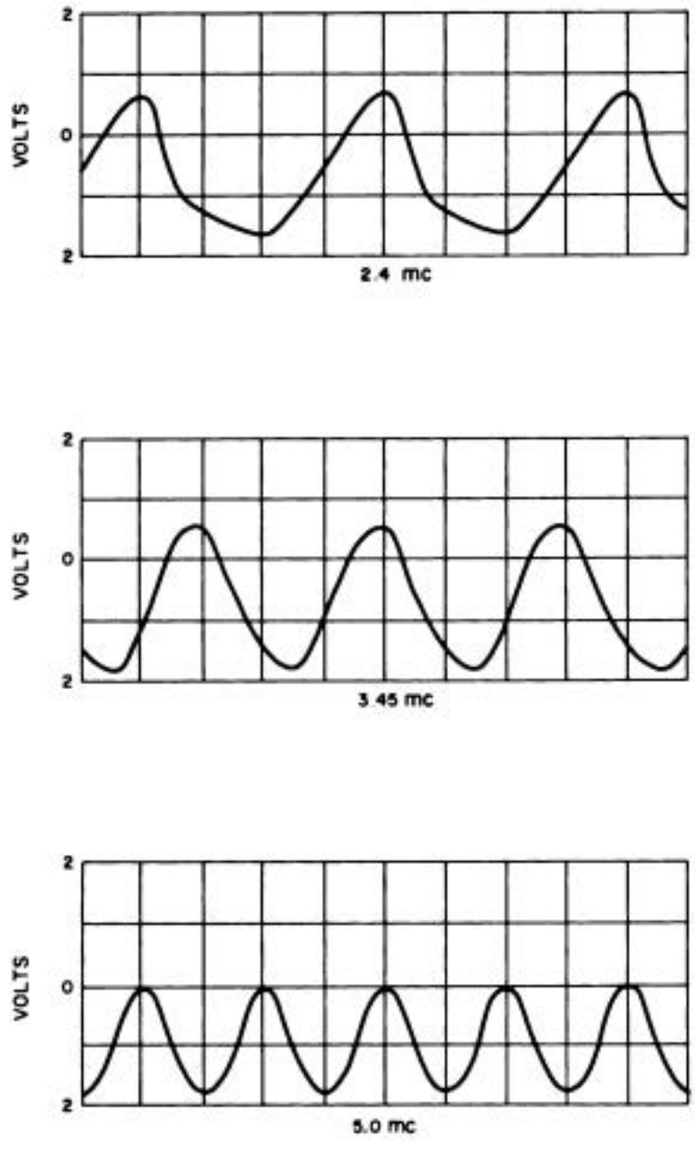


Figure 29-8.—Output Waveform at 25°C for Harmonic Output Circuit (PSC 29B)

679-962 O—63——4

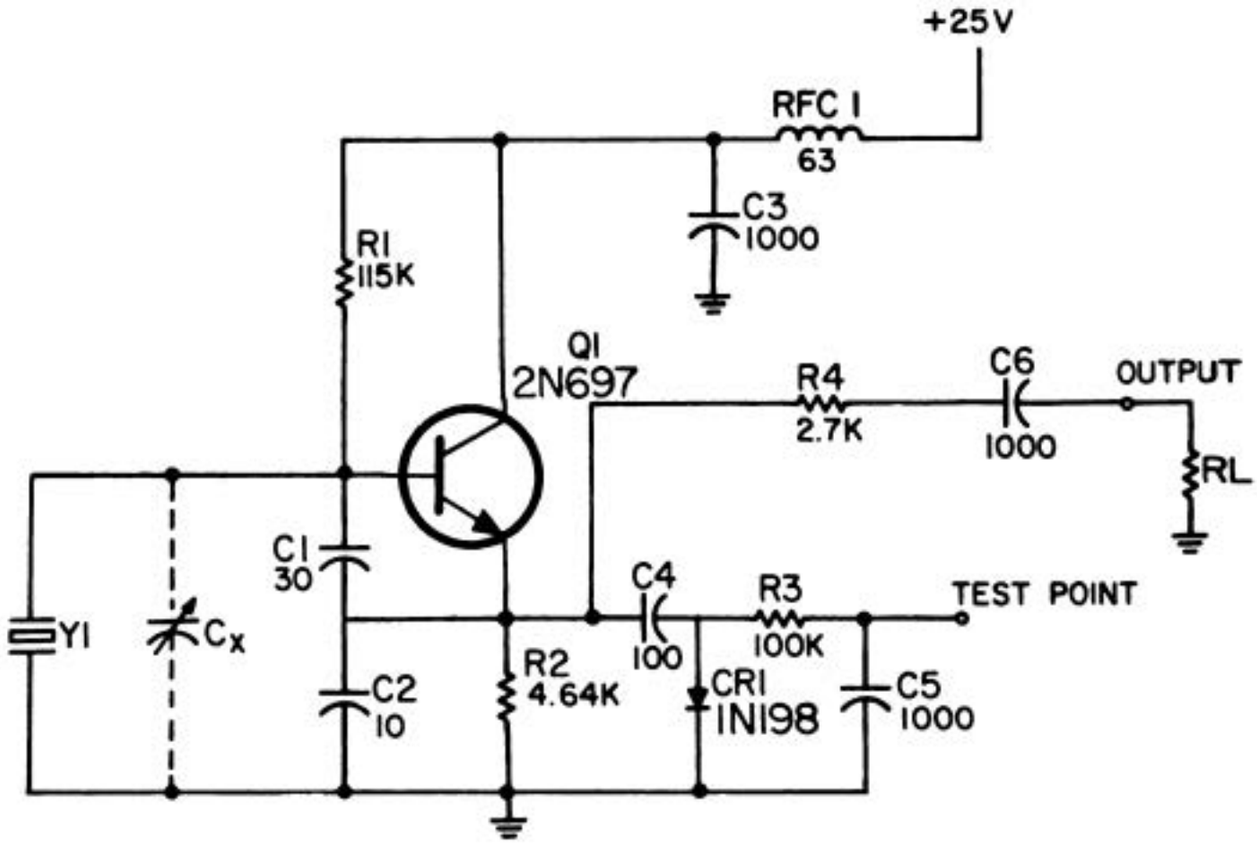
PREFERRED CIRCUIT NO. PSC 30
CRYSTAL OSCILLATOR, 4.5 TO 18 MC

PREFERRED CIRCUIT NO. PSC 30
CRYSTAL OSCILLATOR, 4.5 TO 18 MC

Unless otherwise stated:

R in ohms; C > 1 in pf

L in μh



Components:

Y1: See note 1.

Cx: See section 2.4.

Resistor power dissipation (Note 2): R1, R3: <0.1 mw; R4: <10 mw; R2: 42 mw.

Limits (these are not tolerances; see note 3): R1, R2: ±2%; R3, R4: ±20%; C1, C2: ±10%; all others ±20%.

Operating characteristics:

Temperature range: −55°C to +105°C with standard crystals (Note 1).

Output voltage (Note 4): 0.6 to 1.4-volt peak at 4.5 mc and 0.2 to 0.6-volt peak at 18 mc, with a load resistance of 1,000Ω over the required temperature range.

Frequency stability vs. ambient temperature: 44 ppm (Note 5).

Frequency stability vs. supply voltage change of ±10%:

Ambient Temperature (°C)	*Frequency (mc)*	*Stability (ppm)*
−55	4.5	7
−55	18.0	5
25	4.5	9
25	18.0	6
125	4.5	9
125	18.0	16

Frequency stability vs. transistor product variability (Note 6):

4.5 mc: 95 ppm maximum.

18.0 mc: 94 ppm maximum.

Typical test point voltage at 25°C: −7 volts at 4.5 mc; −5 volts at 18 mc.

Power requirements: +25 volts ±10% at 3 ma (maximum).

Notes:

1. Crystal type CR-18A/U is rated at −55°C to +105°C ±3°C in MIL-STD-683, 3 February 1961. Manufacturers can supply them on special order for operation at temperatures from −55°C to +125°C. The operating characteristics specified herein at +125°C are based on units procured under such special order to the manufacturer. Other than the extended temperature range, these units are identical to stock CR-18A/U crystals.

2. These are the maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

3. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

4. Output voltage varies widely with transistor product variability and with temperature, as well as with load resistance. The values given are the limits measured among 14 transistors supplied by two manufacturers, including limit values of dc beta. The supply voltage was +25 volts.

5. Stability vs. temperature is dependent upon frequency, change in input capacitance of the transistor with temperature, and transistor product variability. More specific information on variation with temperature is shown in figure 30-1.

6. The values given were obtained from measurements at 25°C of 7 samples from one manufacturer and 5 samples from another manufacturer. The reference frequency was the average for the 12 transistors, including those with upper and lower limit values of dc beta.

PSC 30 CRYSTAL OSCILLATOR, 4.5 TO 18 MC

1. APPLICATION

This oscillator may be used with a buffer amplifier to drive a power amplifier. It will also function directly as a local oscillator, or it may be used to drive a frequency synthesizer or multiplier stage. The chief advantages of the circuit are its simplicity and small volume, attributable to the absence of an LC tank circuit. The operating frequency may be changed, over a reasonable band of frequencies, by substituting crystals. This circuit may be used with PSC 28, RF Mixer.

2. DESIGN CONSIDERATIONS

2.1 *Circuit Configuration:* The Colpitts type of circuit was chosen for its simplicity. The common collector connection of the transistor provides the highest input impedance of the three common configurations. It is approximately beta times the load resistance, and provides lighter loading of the parallel resonant crystal circuit.

2.2 *Frequency Range:* The frequency range for this circuit was chosen to complement that of PSC 29A and PSC 29B, which extends from 2.4 to 5.0 mc. Although the upper frequency limit of the standard CR-18/AU crystal is 20 mc, the upper limit of the circuit is set at 18 mc. Output at the higher frequencies is much reduced in a circuit of this type, and starting under extremes of temperature or at reduced supply voltage may be erratic.

2.3 *Transistor Type:* The type 2N697 is a preferred silicon transistor, listed in MIL-STD-701B, that easily permits the extension of the frequency range of the Colpitts circuit to 18 mc. It operates safely in the circuit at 125 °C with the standard supply voltage of +25 volts ±10%.

2.4 *Crystal Unit:* The type CR-18A/U is a preferred type of antiresonant fundamental mode crystal. It is rated up to 105°C in MIL-STD-683, but may be procured for 125°C operation. For good frequency correlation—which means operation in the circuit at very nearly the same frequency as in a standard crystal test set—the crystal should have a parallel load of 32 pf. Unless there is sufficient additional stray capacitance, a small trimmer capacitor, Cx, will be needed across the crystal. The trimmer is also useful for compensation required by transistor or crystal product variability.

2.5 *Feedback Voltage Divider:* The values of feedback capacitors C1 and C2 are critical with respect to frequency, waveform, output and starting under extreme temperature or reduced voltage conditions. Optimum values are also dependent upon effective crystal resistance and transistor characteristics. The values chosen are effective over the specified frequency and temperature range.

2.6 *Test Point:* The test point circuit provides an indication of the operating condition of the oscillator. The value of the negative voltage is a relative measure of the rf output. The test point is useful during equipment production testing as well as during maintenance and service operations. Test point voltage should be read only with a high impedance vacuum tube instrument. Typical readings are given under Operating Characteristics.

2.7 *Supply Voltage Filter:* An LC decoupling filter is used to obtain maximum collector-to-emitter voltage. This minimizes the variations of transistor input capacitance with temperature, and thus provides improved frequency stability.

2.8 *Load Impedance:* To assure a high input impedance, the total load impedance is kept high by means of resistor R4 in series with the load that is simulated here by resistor RL.

3. PERFORMANCE

3.1 *Frequency Stability vs. Temperature:* The circuit provides good stability over the entire temperature range. Figure 30-1 shows the variations in frequency using a typical transistor at 4.5 mc, 9 mc, and 18 mc. Maximum deviations from 25°C frequency values occur at about 85°C. They do not, however, exceed the rated maximum of 50 ppm of the crystals.

3.2 *Output Voltage vs. Temperature:* Figure 30-2 shows the dependency of output voltage upon temperature for a given load impedance. Output voltage at a frequency of 4.5 mc will

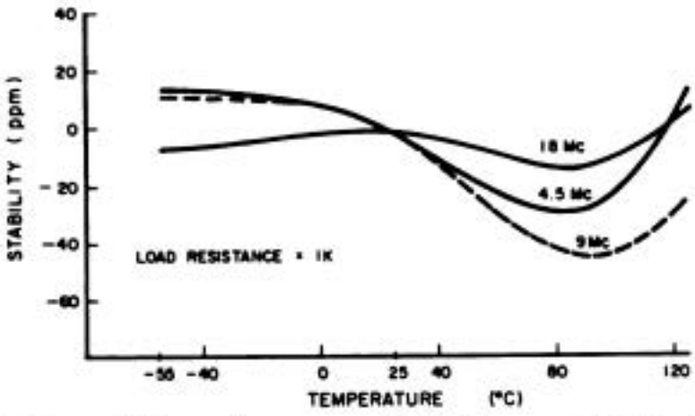


Figure 30-1.—Frequency Stability vs. Ambient Temperature

increase approximately 65% as the temperature increases from −55°C to +25°C and decreases approximately 40% as the temperature increases from +25°C to +125°C. At a frequency of 18 mc, output voltage increases approximately 50% as the temperature increases from −55°C to +25°C and decreases approximately 65% as the temperature increases from +25°C to +125°C.

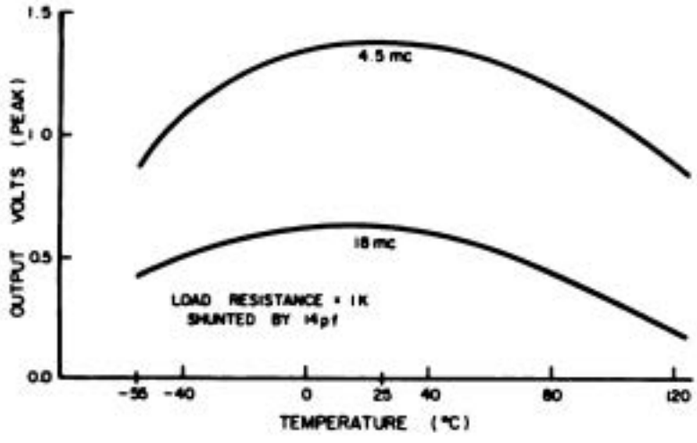
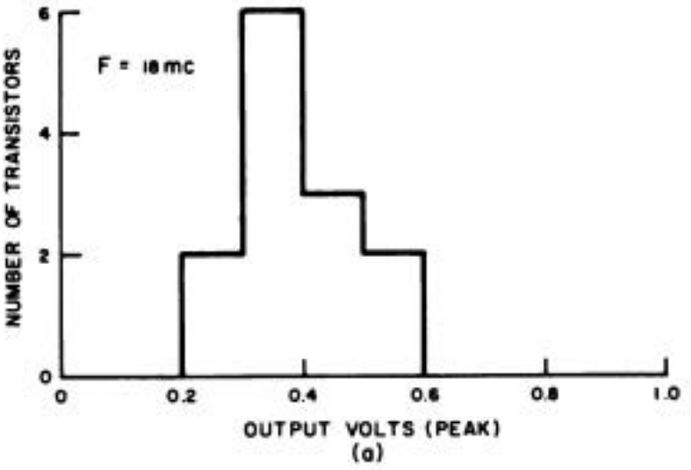


Figure 30-2.—Output Voltage vs. Ambient Temperature

3.3 *Output Voltage vs. Transistor Product Variability:* Figure 30-3 shows the distribution of output voltages obtained from a sample size of 14 transistors.

3.4 *Output Power vs. Load:* Figure 30-4 shows the variations in output with changes in load resistance. A complex impedance match to resonate the output shunt capacitance would be required to obtain higher output at the higher frequencies. Under the test conditions indicated, the optimum load resistance at 4.5 mc is approximately 2,600Ω. At 18 mc, the shunt capacity of 14 pf in the nonresonant



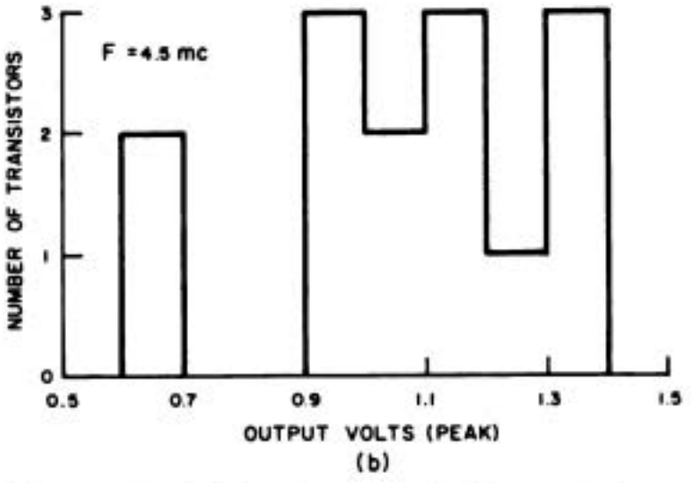


Figure 30-3.—Distribution of Output Voltage Resulting from Transistor Product Variability at 25°C

load circuit limits the maximum impedance to about 650Ω.

3.5 *Output Waveform:* Above 5 mc the waveform is essentially sinusoidal. Below 5 mc a small amount of distortion is noticeable.

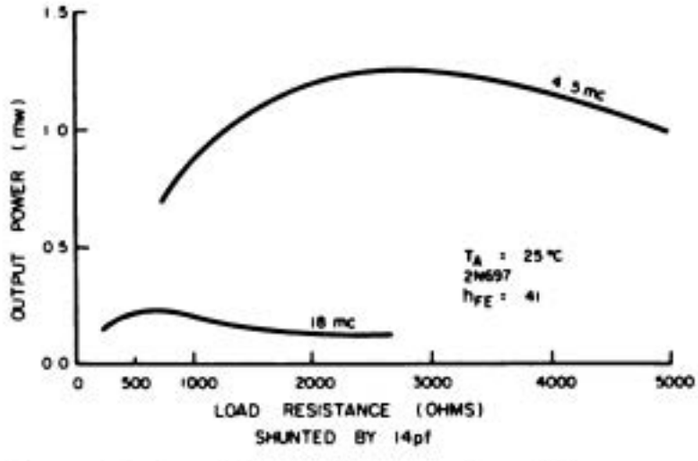
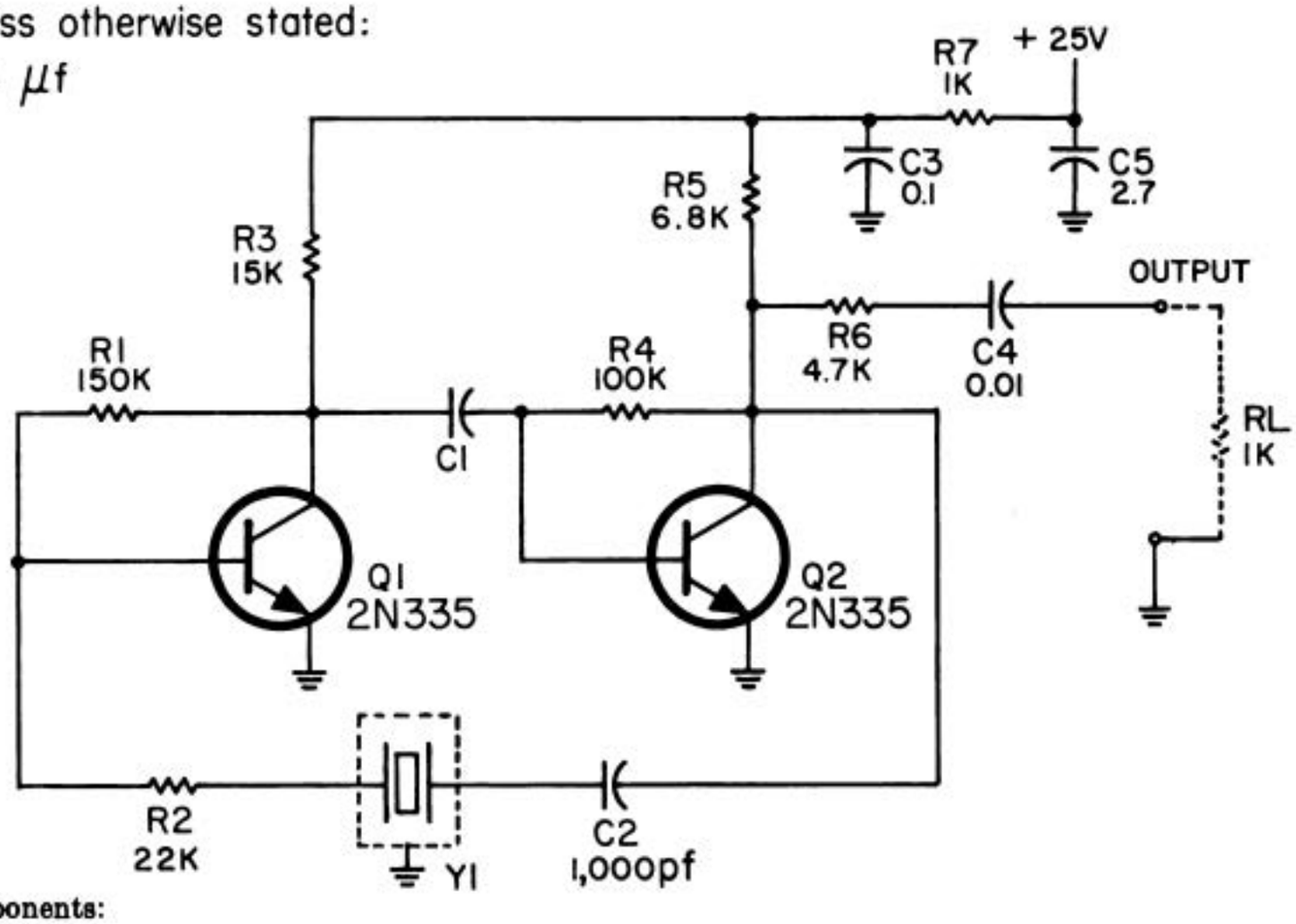


Figure 30-4.—Output Power vs. Load Resistance for Transistors Having Low Limit Value for h_{FE}

PREFERRED CIRCUIT NO. PSC 31
CRYSTAL OSCILLATOR, 25 TO 100 KC

PREFERRED CIRCUIT NO. PSC 31
CRYSTAL OSCILLATOR, 25 TO 100 KC

Unless otherwise stated:
C in μf



Components:

Y1: CR-50A/U

C1: 100 to 10,000 pf (see figure 31-1).

Resistor power dissipation (Note 1): R1, R2, R3, R4, R6: $<$10 mw; R5: 40 mw; R7: 15 mw.

Limits (these are not tolerances; see note 2): R1, R3, R4, R5: $\pm 10\%$; R2, R6, R7: $\pm 20\%$; C1, C2: $\pm 10\%$; C3, C4: $\pm 20\%$; C5: $+50\%$, -20%.

Operating characteristics:

Temperature range: $-40°C$ to $+70°C$ (Note 3).

Output voltage: 1 volt peak across a 1KΩ load.

Output power: 1 mw across a 1KΩ load.

Frequency stability vs. ambient temperature: 100 ppm (maximum).

Frequency stability vs. supply voltage change of $\pm 10\%$: no measurable change.

Frequency stability vs. transistor product variability: 40 ppm (maximum).

Power requirements: $+25$ volts $\pm 10\%$ at 4 ma (maximum).

Notes:

1. These are maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes the initial tolerances plus drifts caused by environmental changes or aging.

3. The operating characteristics specified herein are limited to the temperature range of the type CR-50A/U crystal. The rated temperature range of the circuit is $-55°C$ to $+125°C$ provided an appropriate non-standard crystal is used. Such non-standard crystals are available from some manufacturers; however, a substantial degradation in frequency stability from that allowed under MIL-STD-683 is generally specified.

PSC 31 CRYSTAL OSCILLATOR, 25 TO 100 KC

1. APPLICATION

Crystal oscillators with squared wave outputs operating within this frequency range are to be found in some airborne navigational aid equipments. They are useful as clock pulse generators and can supply inputs to frequency-synthesizer or multiplier circuits.

Since no tuned circuits are used, the operating frequency may be changed by merely changing the crystal and capacitor C1 (see figure 31-1). This simplifies problems of band switching by eliminating space and weight requirements of tuned circuits.

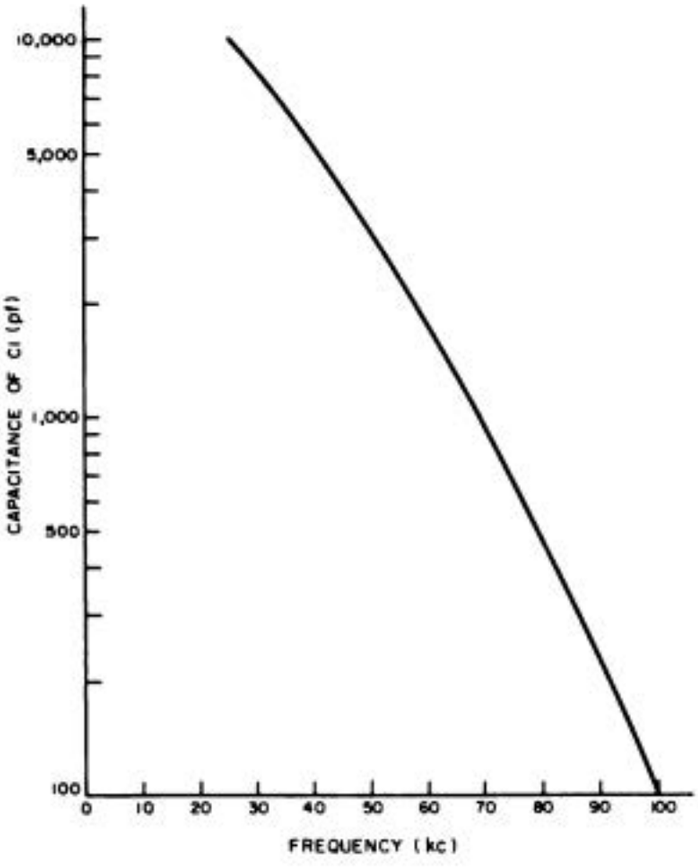


Figure 31-1.—Values of C1 for Different Frequencies of Operation (Use Nearest Standard Value)

2. DESIGN CONSIDERATIONS

2.1 *Circuit Configuration:* The circuit is an amplified feedback type of oscillator in which the feedback path is from the collector of Q2 to the base of Q1 through a crystal. The impedance of the crystal at series resonance is low enough to permit feedback of sufficient amplitude to start and maintain oscillations over the temperature range of −55°C to +125°C. Resistor R2 limits the power dissipated in the crystal to well under its rated maximum.

2.2 *Transistor Type:* A transistor with high gain over the specified frequency range is required in order to assure circuit operation over the temperature range of −55°C to +125°C with V_{cc} 10% below normal. The 2N335 is a preferred type listed in MIL-STD-701B. It adequately meets the gain, temperature, and power dissipation requirements of the circuit.

2.3 *Frequency Range:* The nominal frequency range was established as 25 to 100 kc, although the crystal, type CR-50A/U, covers the range of 16 to 100 kc. The selected range covers most of the applications below 100 kc commonly found in naval airborne equipments. The CR-50A/U crystal is the only preferred type on MIL-STD-683 specified for series resonance below 100 kc.

3. PERFORMANCE

3.1 *Frequency Stability vs. Temperature:* The circuit frequency stability stays within the 0.012% (120 ppm) limit of the crystal itself as long as the rated crystal temperature range of −40°C to +70°C is not exceeded by more than about 10°C at either extreme. As shown in figure 31-2, as the operating temperature

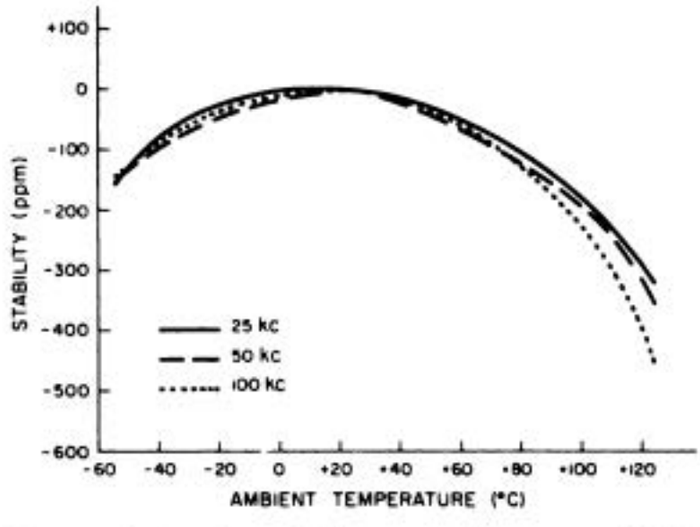


Figure 31-2.—Typical Frequency Deviations With Changes in Temperature (Reference Ambient Temperature = 25°C; Load Resistance = 1KΩ)

exceeds 80°C, the frequency decreases rapidly. At 125°C the deviation from the frequency at 25°C reached a value of 0.045% (450 ppm) for a typical circuit operating at a nominal frequency of 100 kc. As stated in Note 3, non-standard crystals are available with a specified frequency stability which is typically consistent with figure 31–2. The deviation is attributable mainly to the greater effect of temperature upon lower-frequency crystals of figure 31–2 than upon the higher-frequency types used in the Preferred Crystal Oscillators, PSC 29 and PSC 33. The crystal types used therein maintain, up to 125°C, circuit frequency stabilities comparable to those rated for the crystals alone in MIL–STD–683 over their nominal temperature ranges.

3.2 *Output Voltage vs. Temperature:* The output voltage is reasonably constant with changes in temperature. It decreases slightly as temperature is raised. At 125°C a reduction of 10% is typical, using the value at 25°C as a reference.

3.3 *Output Voltage vs. Change in Supply Voltage:* Changes in supply potential of ±10% cause corresponding changes in the level of output voltage of a typical circuit.

3.4 *Output Voltage vs. Transistor Product Variability:* The output voltage will change a maximum of ±12% due to transistor product variability at room temperature.

3.5 *Output Voltage vs. Load Resistance:* Usable output (0.3 volt peak) is available from a typical 100 kc circuit with a load resistance as low as 220Ω. The typical output across a resistive load of 3.3KΩ is 2.6 volts peak, while the no-load output is 9.0 volts peak at a frequency of 100 kc.

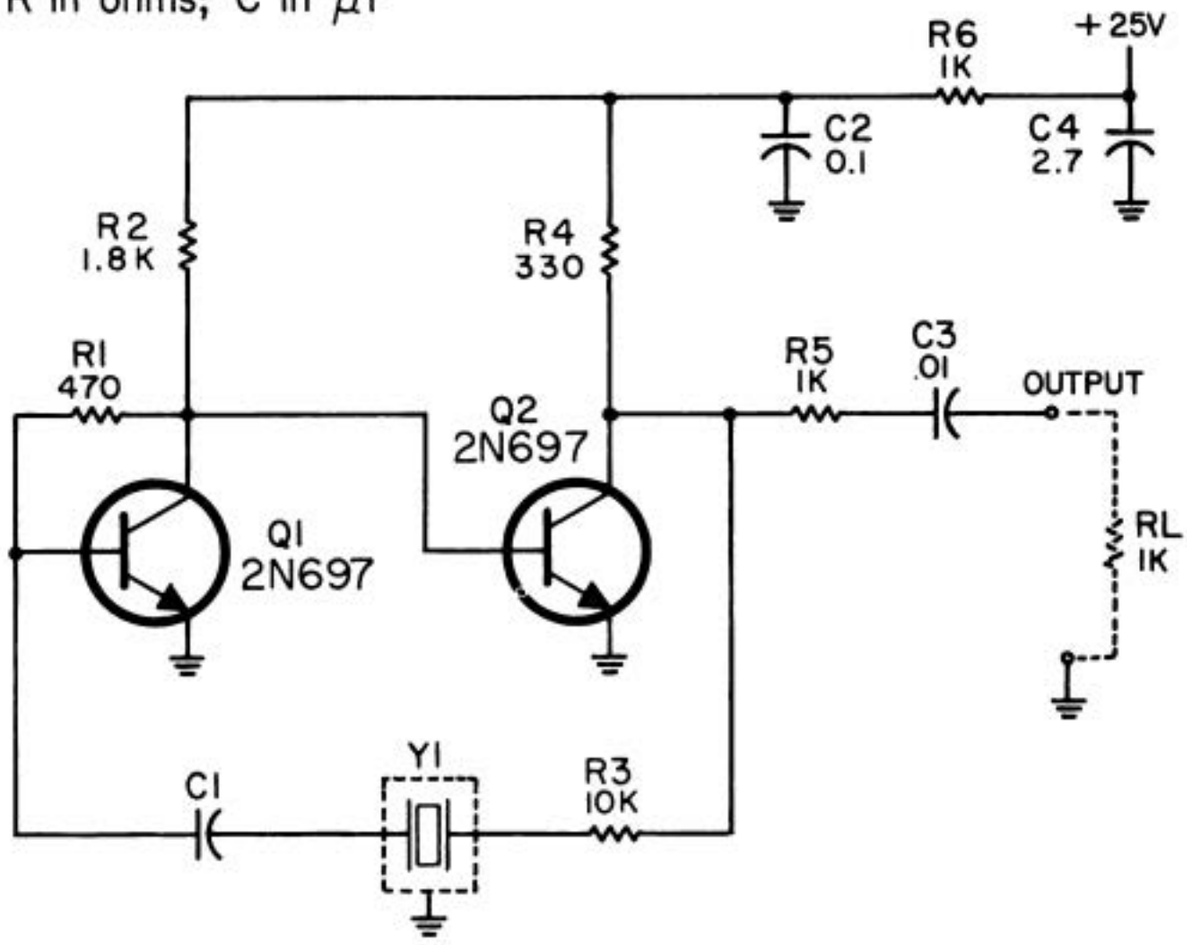
Notes

PREFERRED CIRCUIT NO. PSC 32
CRYSTAL OSCILLATOR, 200 TO 500 KC

PREFERRED CIRCUIT NO. PSC 32
CRYSTAL OSCILLATOR, 200 TO 500 KC

Unless otherwise stated:

R in ohms; C in μf



Components:

Y1: CR-25A/U.

C1: 51 to 100 pf (see figure 32-1).

Resistor power dissipation (Note 1): R1, R3, R4, R5: <30 mw; R2: 100 mw; R6: 0.3w.

Limits (these are not tolerances; see note 2): R1, R2, R4: ±10%; R3, R5, R6: ±20%; C1: ±10%; C2, C3: ±20%; C4: +50%, −20%.

Operating characteristics:

Temperature range: −40°C to +85°C (Note 3).

Output voltage: 1.3 volts peak (typical) across a load resistance of 1KΩ.

Output power: approximately 2 mw across 1KΩ.

Frequency stability vs. supply voltage change of ±10%: 10 ppm over the temperature range of −40°C to +85°C.

Frequency stability vs. transistor product variability: 85 ppm (maximum) at 25°C.

Power requirements: +25 volts at 20 ma (maximum).

(For Notes, see bottom of next page)

PSC 32 CRYSTAL OSCILLATOR, 200 TO 500 KC

1. APPLICATION

Crystal oscillators in this frequency range are used as frequency generators in airborne computers and other circuits in airborne navigational-aid equipments. The squared output waveform permits pulse-shaping, and provides harmonics for frequency multiplication in frequency synthesizer circuits.

Since the circuit requires no tuned elements, its frequency may be changed, within the limits tolerable for a given value of C1, by merely changing crystals. Alternatively, the simultaneous switching of C1 and the crystal will preserve the operational capability throughout the 200 kc to 500 kc band; or C1 may be a variable used as a fine frequency control (see par. 2.1).

2. DESIGN CONSIDERATIONS

2.1 *Circuit Configuration:* The circuit is essentially an amplified-feedback type of oscillator. The series-resonant crystal supplies feedback of sufficient magnitude to support oscillations at only the crystal frequency. Resistor R3 provides current-limiting in the feedback path to protect the crystal from overloads. The capacitance of C1 is selected from figure 32-1 to provide operation at close to the nominal frequency of the crystal. A variable capacitor may be substituted where needed for accurate trimming, but a fixed value will usually cover satisfactorily a useful band of frequencies within the range.

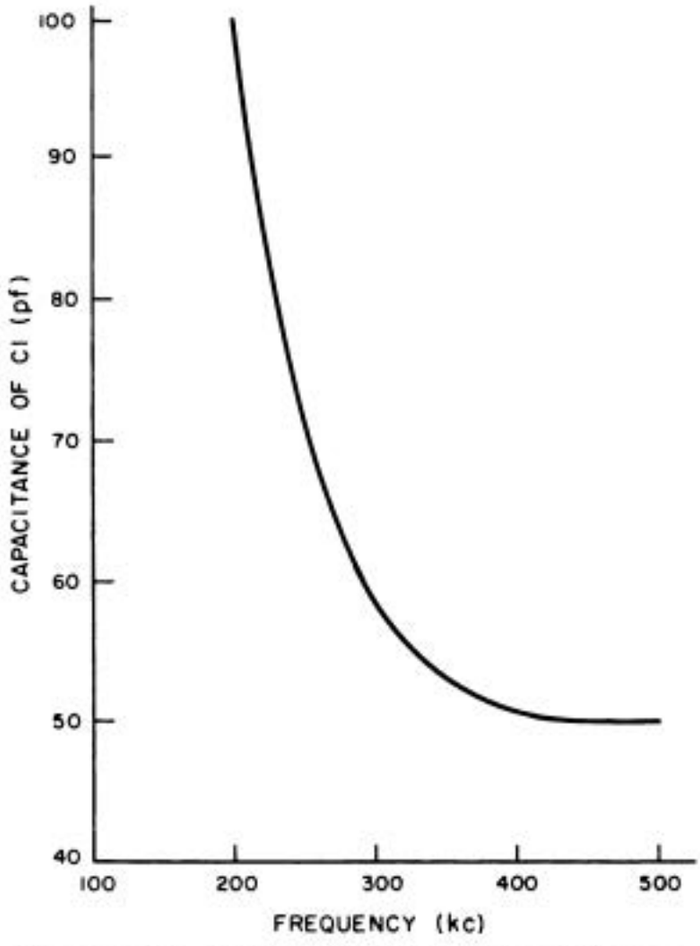


Figure 32-1.—Values of C1 for Different Frequencies of Operation

2.2 *Frequency Range:* The gap between the 500 kc upper frequency limit of this circuit and the 800 kc lower limit of PSC 33 is due to the lack of standard crystal frequencies in that range. A similar gap exists for the same reason between the 200 kc lower limit of this circuit

---

Notes:

1. These are maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. The operating characteristics specified herein are limited to the temperature range of the type CR-25A/U crystal. The rated temperature range of the circuit is −55°C to +125°C provided an appropriate non-standard crystal is used. Such non,standard crystals are available from some manufacturers; however, a substantial degradation in frequency stability from that allowed under MIL-C-3098/7 is generally specified.

and the 100 kc upper limit of PSC 31. When necessary, these oscillators can operate at the non-standard frequencies with little or no modification.

2.3 *Transistor Type:* The type 2N697 silicon transistor is a preferred type on MIL–STD–701B. It was chosen for its high gain at high frequencies. This characteristic was found necessary to assure adequate feedback through the high-resistance crystals. The effective series resistance of type CR–25A/U crystals can be as high as 7.5KΩ.

3. PERFORMANCE

3.1 *Frequency Stability vs. Temperature:* Figure 32-2 shows typical frequency deviations due to temperature changes. Between −55°C and +85°C, the frequency deviation is within 0.01% (100 ppm); above +85°C, the frequency continues to decrease with increasing temperature. PSC 32 will operate over an extended temperature range of from −55°C to +125°C

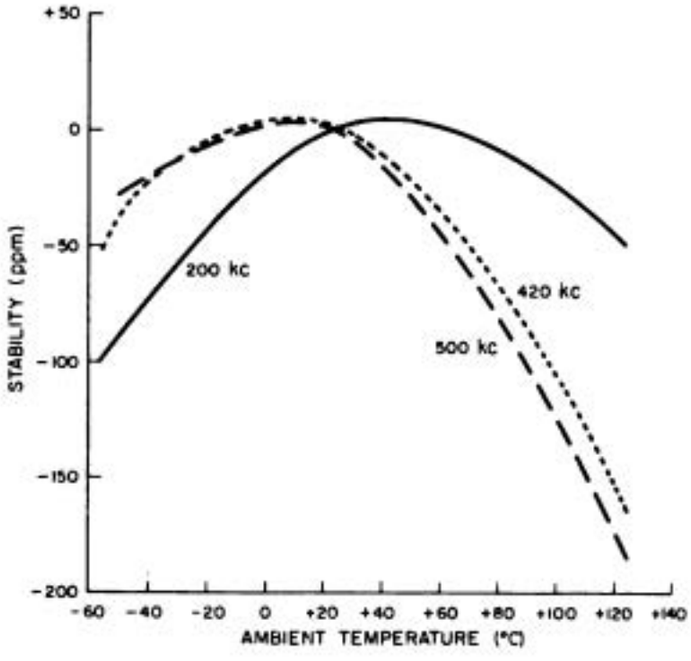


Figure 32-2.—Typical Frequency Deviations With Changes in Temperature (Load Resistance = 1KΩ)

provided an appropriate non-standard crystal is used as stated in Note 3. However, because of the temperature characteristics of crystals within the frequency range of PSC 32, the specified frequency stabilities of the non-standard crystals will generally be significantly in excess of the stability specified in MIL–C–3098/7 for the CR–25A/U type. Frequency stabilities as stated in the appropriate military specifications can be obtained with non-standard crystals over the temperature range of −55°C to +125°C in PSC 29 and PSC 30, the reason being that these two circuits use higher-frequency crystal types possessing better temperature characteristics.

3.2 *Output Voltage vs. Temperature:* The output voltage across a 1KΩ resistive load remains essentially constant, with a given combination of transistors and crystals, over the range of −40°C to +85°C. Over the range of −55°C to +125°C a typical range of output values is 1.2 to 1.3 volts peak at any frequency.

3.3 *Output Voltage vs. Change in Supply Voltage:* Changes in V_{cc} of ±10% result in corresponding percentage changes in output voltage.

3.4 *Output Voltage vs. Transistor Product Variability:* Transistor product variability has considerable effect upon output signal level. At room temperature, output levels of 0.25 to 1.65 volts peak were recorded when the circuit was tested with 12 randomly-selected pairs of 2N697's. The samples were procured from four manufacturers, and included those having limit values of dc beta and saturation resistance specified in MIL–S–19500/99A(Sig C). The transposition of any pair of transistors in the circuit caused a significant change in output. Each pair was therefore tested in both positions, so that 24 tests were run at each of three frequencies (200 kc, 420 kc, and 500 kc). About 70% of the measured outputs were between 1.3 and 1.6 volts peak, and 87% of the output voltages were 1.0 volt peak or more.

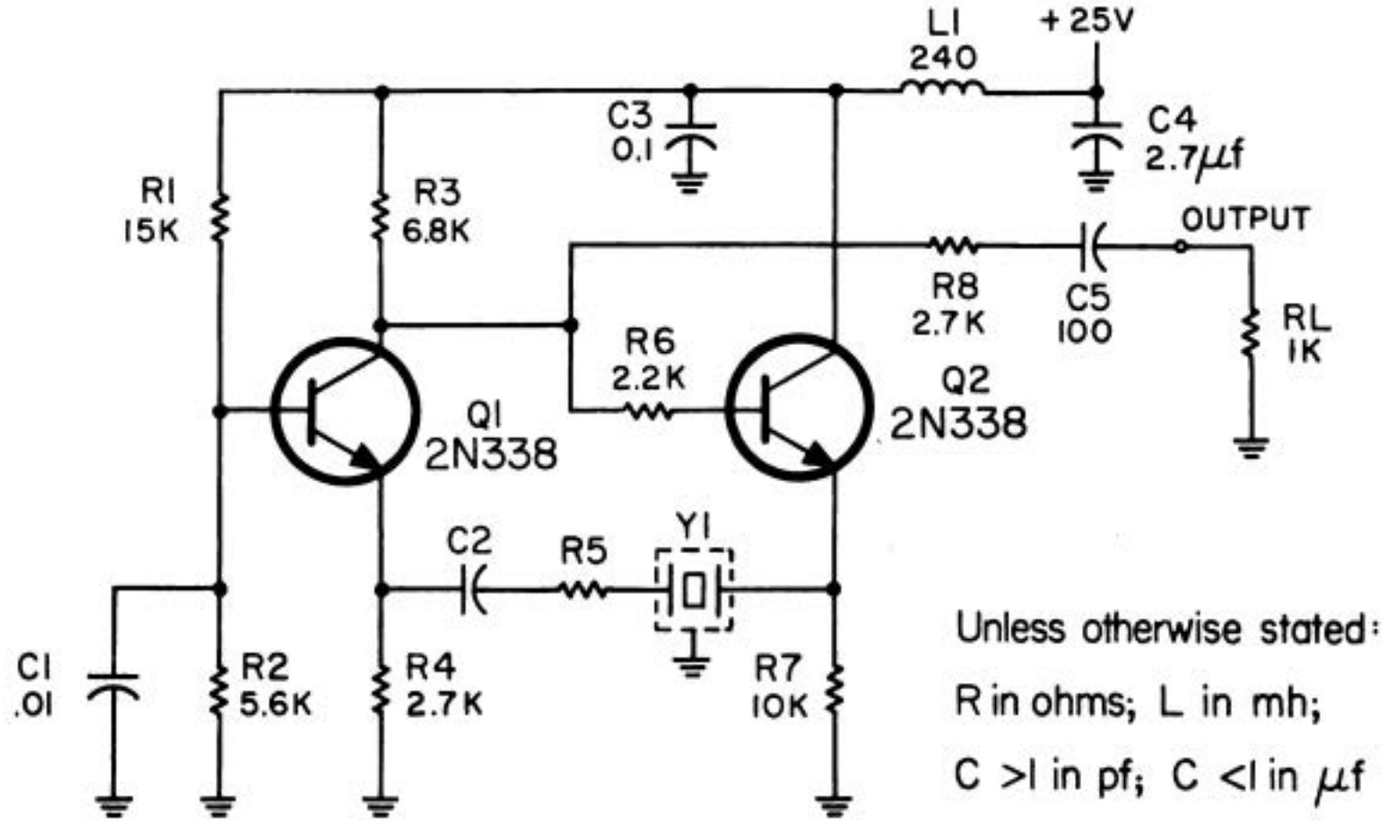
3.5 *Output Voltage vs. Load Resistance:* The output level varies from about 0.4 volt peak across a load of 220Ω to about 2.0 volts peak across a load of 3.3KΩ. The no-load output voltage is about 3.0 volts peak.

Notes

PREFERRED CIRCUIT NO. PSC 33
CRYSTAL OSCILLATOR, 0.8 TO 2.5 MC

679-962 O—63——5

PREFERRED CIRCUIT NO. PSC 33
CRYSTAL OSCILLATOR, 0.8 TO 2.5 MC



Components:

Y1: CR-19 A/U.

C2: 39 to 91 pf (see figure 33-1).

R5: 0Ω at or below 1 mc; 100Ω above 1 mc.

Resistor power dissipation (Note 1): R1, R2, R3, R4, R7: <50 mw; R5, R6, R8: <5 mw.

Limits (these are not tolerances; see note 2):

R1, R2, R3, R4, R6: ±10%; R5, R8: ±20%.

C1, C3, C5: ±20%; C2: ±10%; C4: +50%, −20%.

Operating characteristics:

Temperature range (Note 3): −55°C to +105°C with standard crystals.

Output voltage (Note 4): 0.5 to 1.0 volt peak to peak with a load resistance of 1 KΩ.

Output power: Approximately 1 mw into a 1 KΩ load at 25°C.

Frequency stability vs. supply voltage change of ±10%: 3 ppm (maximum).

Frequency stability vs. transistor product variability: 20 ppm (maximum) at 25°C.

Power requirements: +25 volts ±10% at 3.5 ma (maximum).

Notes:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes the initial tolerance plus drifts caused by environmental changes or aging.

3. MIL-STD-683, 3 February 1961, specifies an operating temperature range for the type CR-19A/U crystal of −55°C to +105°C. Suppliers of these crystals, however, have been able to deliver units that perform satisfactorily at temperatures up to +125°C.

4. Output voltage for a given load is dependent primarily upon transistor product variability.

PSC 33 CRYSTAL OSCILLATOR, 0.8 TO 2.5 MC

1. APPLICATION

This oscillator provides ample output, over a wide operating temperature range, for use as a local oscillator in communications equipments, and as a frequency source in navigation equipment. Since it uses no tuned circuits, frequency changing can be accomplished, within the limits of the circuit, by merely changing crystals and, if necessary, C2. Its output waveform is essentially sinusoidal, containing about 10% harmonic distortion.

2. DESIGN CONSIDERATIONS

2.1 *Circuit Configuration:* The circuit is a modified Butler type of oscillator. The crystal operates in series resonance to provide an emitter-to-emitter feedback path.

Resistor R5 is needed to keep crystal dissipation at a safe level when the circuit is operated at frequencies of 1 mc or above.

Capacitor C2 serves to adjust the frequency to a value closer to the nominal of the crystal used. If a variable capacitor is used, closer adjustment is possible. Figure 33-1 is useful in selecting the proper value of C2 for a given frequency of operation. If crystal switching is desired, a mid-band value will be satisfactory, but not over a range greater than 1 mc.

2.2 *Frequency Range:* The 2.5 mc upper frequency limit of this circuit was chosen to provide slight overlapping of its range with that of PSC 29. (PSC 29 oscillates between 2.4 mc and 5.0 mc). The 0.8 mc lower limit is determined by the fact that it is the lower frequency limit of the type CR-19A/U crystal. There are no military standard crystals for frequencies between 0.5 mc and 0.8 mc.

2.3 *Transistor Type:* The 2N338 is a preferred type on MIL-STD-701B. It has ample gain over the desired frequency and temperature range, and requires reasonably low operating power.

3. PERFORMANCE

3.1 *Frequency Stability vs. Temperature:* Typical temperature stability characteristics of this circuit are quite good. Transistors having approximate limit values of dc beta and saturation resistance were used with a small sample of crystals in testing the circuit. The majority of combinations showed stability well within the 50 ppm deviation allowed by MIL-STD-683 for the crystal. In general, the deviation from the frequency at 25°C is a maximum at about 85°C. Typical stability curves are shown in figure 33-2.

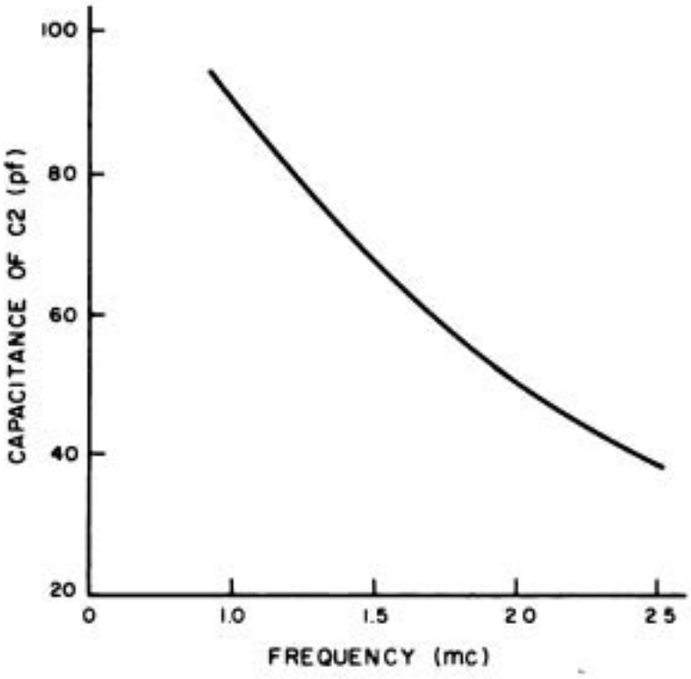


Figure 33-1.—Proper Value of C2 for Each Frequency (Use nearest standard value)

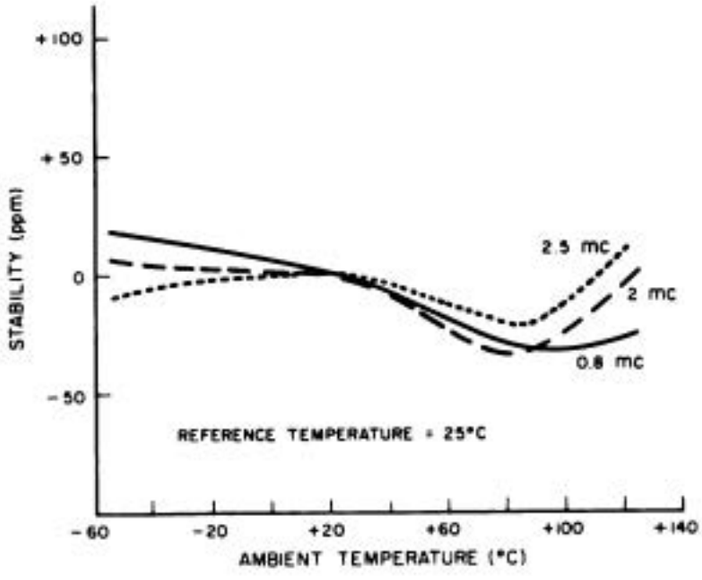


Figure 33-2.—Typical Frequency Deviations With Changes in Operating Temperature. Load Resistance = 1KΩ

3.2 *Output Voltage vs. Temperature:* For any given combination of active and passive parts, the output is reasonably constant over the temperature range of −55°C to +125°C. Typical variations in output are shown in figure 33-3. Transistors that were used in determining the spread of output values included those having upper and lower limit values of dc current gain and also of saturation resistance, as specified in MIL-S-19500/69C (Navy).

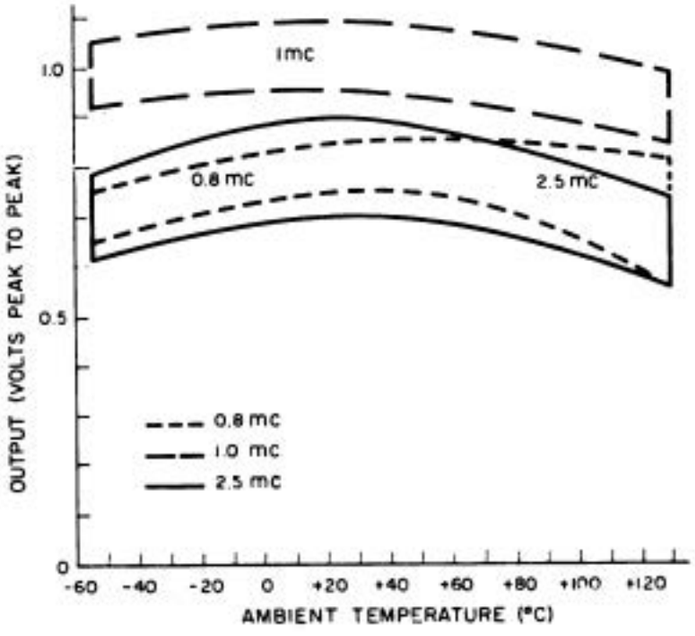


Figure 33-3.—Output Voltage vs. Ambient Temperature, Showing Effect of Transistor Product Variability. Load Resistance = 1KΩ

3.3 *Output Voltage vs. Change in Supply Voltage:* A change in supply voltage of ±10% results in a variation in output signal voltage of ±11%.

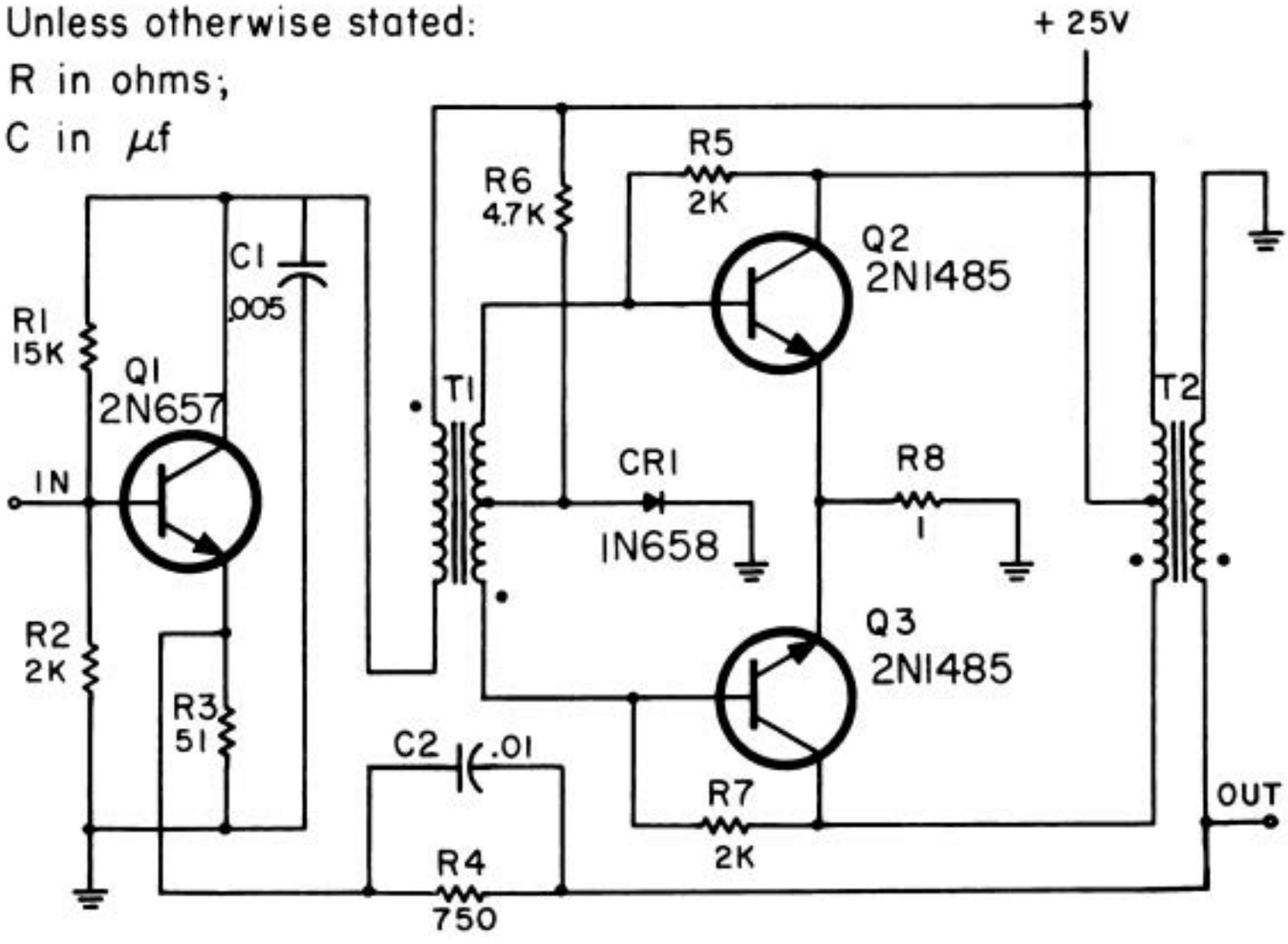
3.4 *Output Voltage vs. Transistor Product Variability:* Tests were run at room temperature using 12 pairs of randomly selected samples of type 2N338 transistors, including those with the limit values mentioned in 3.2. Since the transposition of each pair in the circuit affects the output voltage, 24 tests were made with the 12 pairs at each of four frequencies (0.8 mc, 1.0 mc, 2.0 mc, and 2.5 mc). The deviations from the average output were greatest at 2.0 mc. The output at that frequency varied from 24% below to 14% above the average value of 0.85 volt peak to peak.

3.5 *Output Voltage vs. Load Resistance:* The typical output voltage at room temperature, over the specified frequency range, varies from a value of 0.2 volts peak to peak across a load of 220Ω to about 1.8 volts peak to peak with a load resistance of 3.3 KΩ.

Notes

PREFERRED CIRCUIT NO. PSC 34
AUDIO POWER AMPLIFIER, 5 WATTS

PREFERRED CIRCUIT NO. PSC 34
AUDIO POWER AMPLIFIER, 5 WATTS



Components:

Transformer T1:

DC resistance of primary: 35Ω.

AC impedance: primary: 500Ω; secondary: 16Ω center-tapped.

Transformer T2:

DC resistance of primary: 3Ω.

AC impedance: primary: 64Ω center-tapped; secondary: 16Ω.

Resistor power dissipation (Note 1): R1, R2, R3: <0.1 watt; R4, R5, R7: 0.3 watt; R6: 0.125 watt; R8: 0.8 watt.

Limits (these are not tolerances; see note 2): R1, R2, R3, R5, R7: ±10%; R4, R6, R8: ±20%. All C: ±20%.

Operating characteristics (Note 3):

Frequency response: down 3 db at 40 cps and 22 kc.

Input impedance: 550Ω ±10%.

Maximum input level: 1.0 Vac.

Output impedance: 16Ω.

Typical power output for 3% total distortion from −55°C to +125°C: 5 watts.

Maximum power output at 5% total distortion: 7.5 watts at 125°C; 10 watts at 85°C; 11.5 watts at 25°C.

Typical power gain: 37 db.

Operating temperature: −55°C to +125°C.

Power transistor heat sink requirements (Note 4): Q1: None; Q2 and Q3: Ambient air-to-heat-sink thermal resistivity for operation to 85°C: $\leq$15°C per watt per transistor (maximum); ambient air-to-heat-sink thermal resistivity for operation to 125°C: $\leq$5°C per watt per transistor (maximum).

Power requirements:

+25 volts $\pm$10% at 1 ampere (maximum).

Notes:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

3. Unless otherwise stated, the values given are based on data taken at 25°C and 1,000 cps, using nominal-value active and passive components.

4. Heat sink thermal resistivity specified is absolute maximum for continuous operation at rated output. The anodized mounting surface or 2-mil mica transistor mounting insulation should not have a thermal resistivity exceeding 0.5°C per watt with silicon grease on interfaces. A 3" $\times$ 3" $\times$ 3/16" piece of aluminum mounted in a vertical position has a thermal resistivity of approximately 5°C per watt at sea level.[1] Commercial heat sinks with the required thermal resistivity are readily available. Correction factors should be used in calculating the dimensions of heat sinks for various altitudes, orientations, and obstructed paths of radiation and convection, as well as in the design of forced-air cooling.[2]

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[1] J. Eimbinder, "Determining Permissible Dissipation for Silicon Power Transistors," Electronic Design, Vol. 9, No. 17, August 16, 1961, pp. 44–49.

[2] W. Luft, "Taking the Heat Off Semiconductor Devices," Electronics, Vol. 32, No. 24, June 12, 1959, pp. 53–56.

PSC 34 AUDIO POWER AMPLIFIER, 5 WATTS

1. APPLICATION

This circuit will provide a nominal output power of from 5 to 10 watts for either public address or communications receiver systems when used in conjunction with PSC 23, or any similar preamplifier. If the appropriate change is made in the output transformer, the circuit may be used as a transmitter modulator. The first stage is a modification of PSC 24, Audio Driver, to permit loop feedback.

2. DESIGN CONSIDERATIONS

PSC 34 is similar in design and performance to amplifiers in many Naval airborne equipments now in use or under development. The primary difference is the use of silicon transistors to permit operation over an ambient temperature range of $-55°C$ to $+125°C$.

A special effort has been made to provide stabilization through the use of degenerative feedback, as a means of reducing performance changes attributable to temperature and transistor product variability. In addition to a feedback loop from the output transformer secondary to the emitter of the input stage, several modes of feedback are used to stabilize each stage individually. Emitter resistors R3 and R8 supply emitter-to-base degeneration in the input and output stages. R5 and R7 provide collector-to-base feedback in the final stage. The liberal use of such feedback provides the additional advantage of a low distortion level until limiting action begins to take place in the transistors at maximum rated output power.

Operation of the push-pull output stage is essentially Class B. A slight amount of positive bias is required to reduce crossover distortion. PSC 34 utilizes the forward voltage drop of a silicon diode to supply the bias needed to stabilize the quiescent collector current over the required ambient temperature range. The resistance to forward currents through a silicon p-n junction will increase with decreasing temperatures. In the case of the transistor, this means that an increase in bias voltage will be required if the quiescent collector current is to remain constant. This variation in bias voltage is approximated by the use of a silicon diode in parallel with the base-to-emitter junction of the transistor.

High frequency regeneration is suppressed at the collector of Q1 by capacitor C1. Capacitor C2 provides the necessary phase shift at the higher frequencies for degenerative feedback. If other than a 16Ω secondary winding impedance is used for matching to other load resistances, the values of R4 and C2 will change accordingly.

3. PERFORMANCE

Supply voltage variations within the stated limits produce a negligible effect on circuit performance provided the input level is below that required to produce limiting action in the transistors. This level occurs at approximately 0.85 Vac input and 7.0 watts output at 25°C with nominal transistors. Output power will vary as the square of the supply voltage if the circuit is driven to the point of limiting action.

The relatively linear relationship between output power and input signals above 0.5 Vac, as shown in figure 34–1, continues well beyond the point at which limiting begins to take place. However, distortion of the output waveform increases severely as the input level rises above 1.0 Vac. Total distortion is typically less than 3% when the circuit is operating within the Class AB limits. This class of operation at 25° C occurs between output levels of approximately 200 mw and 7.5 watts. Operation in the Class A region, below 200 mw, reduces the total distortion to less than 0.5%.

Performance variations due to product variability are shown graphically in figures 34–1 and 34–2. The graphs are based on data obtained in tests employing transistors with maximum and minimum values of dc current gain. Low h_{FE} values of Q1, Q2, and Q3 are 36, 37, and 37 respectively; high h_{FE} values are 83, 100, and 100. The values approximate the minimum and maximum limits of dc current gain specified in the appropriate military specifications. Figure 34–1 shows that, with maximum rated input at 25° C, the variation in power output attributable to dc current gain variability is less than 0.5 db.

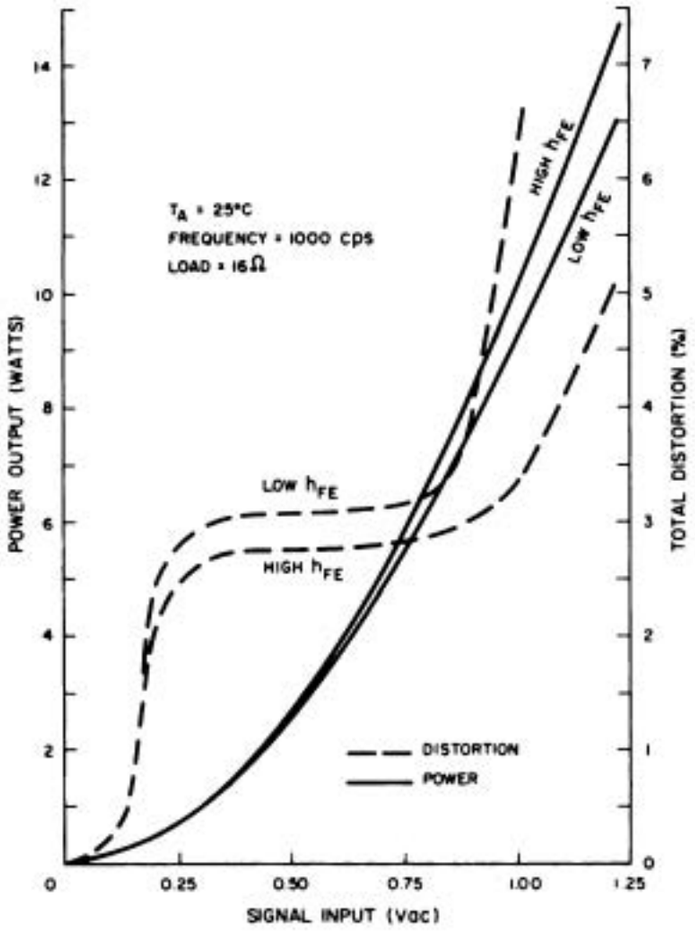


Figure 34-1.—Power Output and Total Distortion vs. Signal Input, Showing Effects of Transistor Product Variability

Figure 34-2 shows that the maximum variation in power output attributable to the cumulative effects of maximum changes in temperature and transistor dc current gain is less than 2 watts.

Figure 34-3 shows typical frequency response of approximately 40 cycles to 22 kilocycles at the half-power points. Variation in frequency response attributable to temperature and product variability is negligible primarily because of the generous use of degenerative feedback.

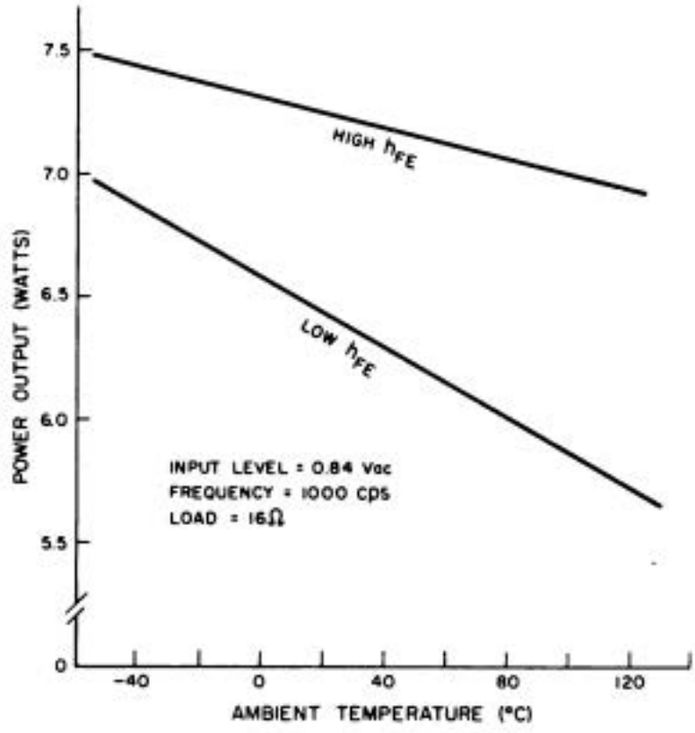


Figure 34-2.—Power Output vs. Ambient Temperature, Showing Effects of Transistor Product Variability

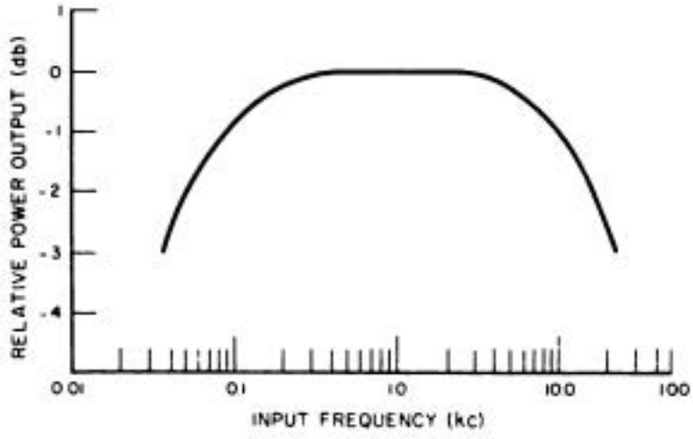


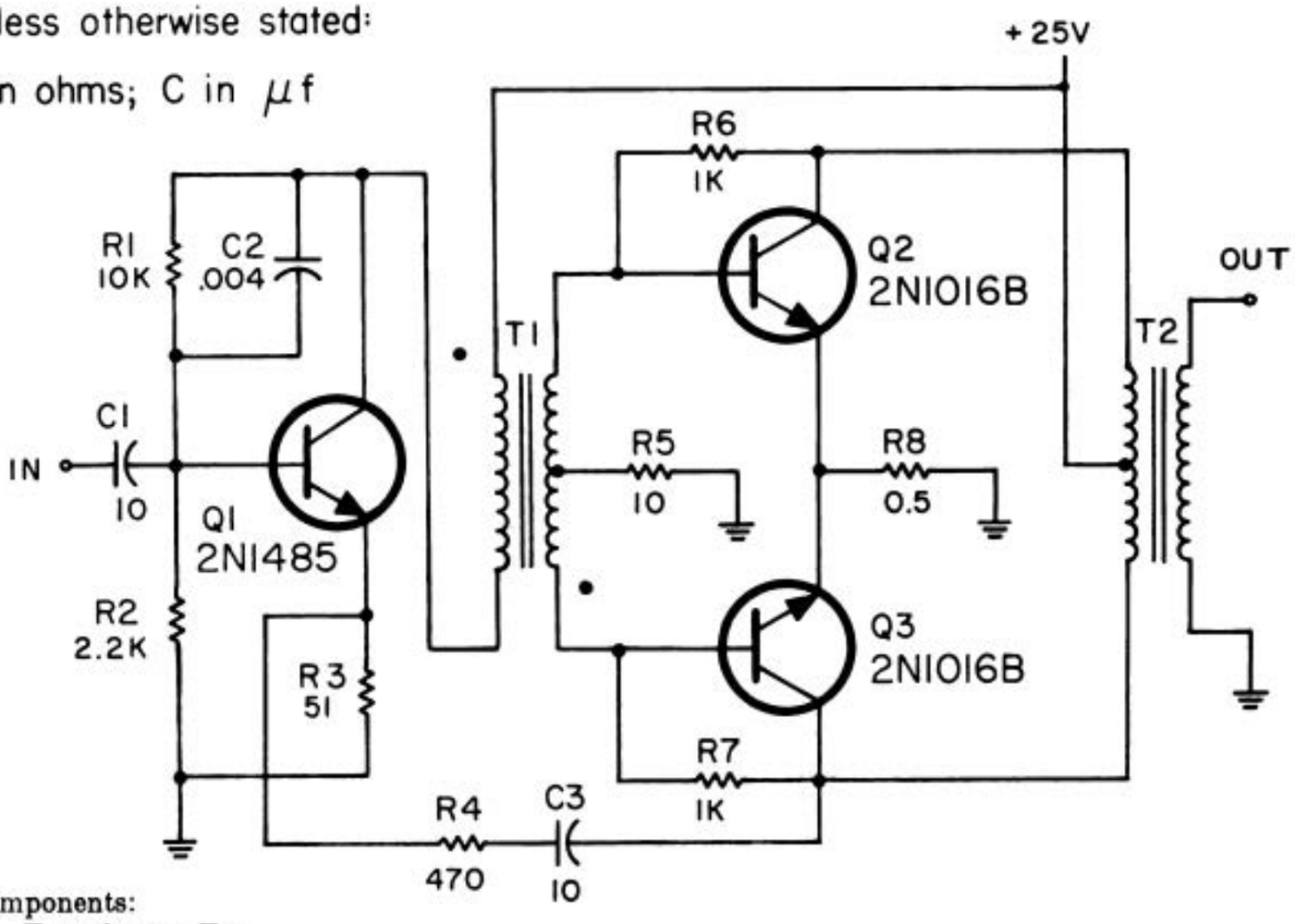
Figure 34-3.—Typical Frequency Response at 25°C. Constant Input Signal Level=0.62 Vac. Output Reference Level, 0 db=4 watts

PREFERRED CIRCUIT NO. PSC 35
AUDIO AMPLIFIER-MODULATOR, 20 WATTS

PREFERRED CIRCUIT NO. PSC 35
AUDIO AMPLIFIER-MODULATOR, 20 WATTS

Unless otherwise stated:

R in ohms; C in μf



Components:

Transformer T1:

DC resistance of primary: 9Ω.

AC impedance: primary: 180Ω; secondary: 160Ω center tapped.

Transformer T2:

DC resistance of primary: 2Ω.

AC impedance: primary: 50Ω center-tapped; secondary: 3,000Ω.

Resistor power dissipation (Note 1): R1, R2, R7: $<$0.1 watt; R3: 0.13 watt; R4, R5, R6: 0.65 watt; R8: 2 watts.

Limits (these are not tolerances; see note 2): R1, R2, R3, R5, R6: $\pm$20%; R4, R7, R8: $\pm$10%.

C1, C3: +50%, −20%; C2: $\pm$20%.

Operating characteristics (Note 3):

Frequency response: Down 3 db from 1,000 cps at 95 cps and 17 kc.

Input Impedance: 1KΩ.

Maximum continuous input level: 3.5 Vac.

Output impedance (primary of transformer T2): 50Ω collector-to-collector.

Maximum continuous power output: 20 watts.

Power gain: 33 db.

Total distortion: 5% at rated output.

Operating temperature: −55°C to +125°C.

Maximum power dissipated in output transistors (Note 4): 8.75 watts per transistor.

Heat sink requirements (ambient air-to-heat-sink thermal resistivity; see note 5): Q1: None; Q2 and Q3: to 85°C, $\leq$7°C/watt; to 125°C, $\leq$2°C/watt.

Power requirements: +25 volts $\pm$10% at 2.5 amperes.

PSC 35 AUDIO AMPLIFIER-MODULATOR, 20 WATTS

1. APPLICATION

This circuit will provide a nominal power of 20 watts throughout the audio frequency range, and can be used as a transmitter modulator or power amplifier for public address systems. Although the circuit is shown with an output transformer secondary impedance of 3KΩ, an appropriate secondary impedance may be substituted to match the required load of a particular application.

Notable features of PSC 35 are its high power-gain, relatively low distortion and power consumption, and wide frequency-range.

2. DESIGN CONSIDERATIONS

The use of the 2N1016B transistors in the output stages of PSC 35 was dictated by the high output-power and temperature requirements of the circuit. It is otherwise similar in design and performance to high-power audio amplifiers in several Naval airborne equipments now in use, but which have a more limited operational temperature range.

Variations in power gain, total distortion, and frequency response attributable to temperature changes, supply voltage fluctuations and transistor product variability are substantially reduced through the liberal use of degenerative feedback. Degeneration is developed in the input and output stages by R3 and R8, respectively. In addition, 6 db of feedback is introduced between the output transformer primary and the emitter of Q1 through R4 and C3.

Cross-over distortion is minimized through the use of R5, which provides a small positive bias for output transistors Q2 and Q3.

3. PERFORMANCE

PSC 35 will produce 20 watts continuously at 125°C. However, the junction temperature of the two 2N1016B power transistors will be very near their rated maximum under such conditions. It is assumed that this condition is rarely, if ever, required by voice communications equipments. Normally, operation will be of an intermittent nature and a substantial margin of safety will exist with respect to the the junction temperature of the power transistors.

Variations of the collector supply voltage at output power levels greater than 15 watts will affect the distortion and gain characteristics of the circuit, as shown in figures 35-1 and 35-2. If the supply voltage is allowed to drop 2.5 volts from nominal at 20 watts output, total distortion will increase from 5% to 9%, and power gain will decrease 1.1 db. If, at the same output, the supply voltage is increased 10% to 27.5 volts, distortion will decrease by 0.2% and power gain will increase by 0.4 db.

Gain and distortion are degraded by a decrease in supply voltage because the power transistor collector swing is almost 25 volts peak at rated output; consequently, a decrease in supply voltage will result in limiting action by the power transistors. An increase in supply

---

Notes:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

3. Unless otherwise stated, the operating characteristics are based on data taken at 25°C using nominal-value active and passive components. All signal input and impedance characteristics are based on a 1000 cps sine wave.

4. This amount of power is dissipated in each transistor when approximately 13 watts are being supplied to the load. This includes a 10% increase in collector supply voltage.

5. For applicable information and references on heat sinks, refer to Note 4, PSC 34.

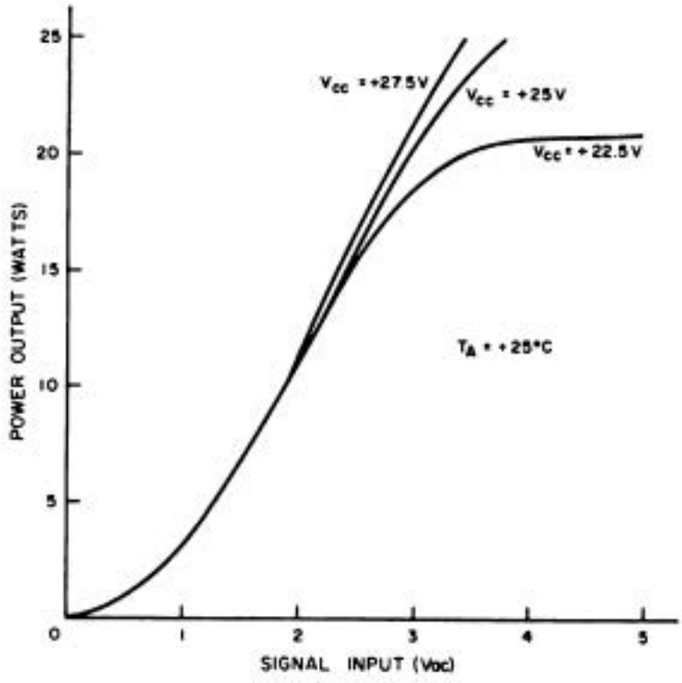


Figure 35–1.—Power Output vs. Signal Input, Showing Effect of Supply Voltage Variation

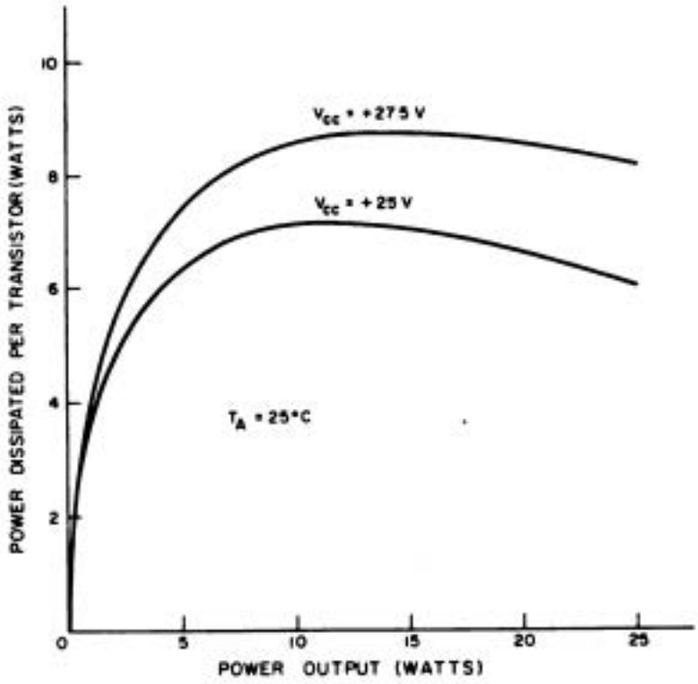


Figure 35–3.—Collector Power Dissipation Per Output Transistor vs. Power Output, Showing Effect of Supply Voltage Variation

voltage will result in improved gain and distortion characteristics, because transistor operation is further removed from the region of limiting action. However, power dissipation in the 2N1016B transistor increases appreciably at all input levels with a 10% increase in supply voltage, as shown in figure 35–3. Therefore, care must be taken that the collector supply potential does not exceed 27.5 volts at high ambient temperatures, or the output transistors may be damaged.

Transistor power dissipation levels as referenced in figure 35–3 were derived by the following process:

(1) The total current delivered to the circuit from the power supply was monitored

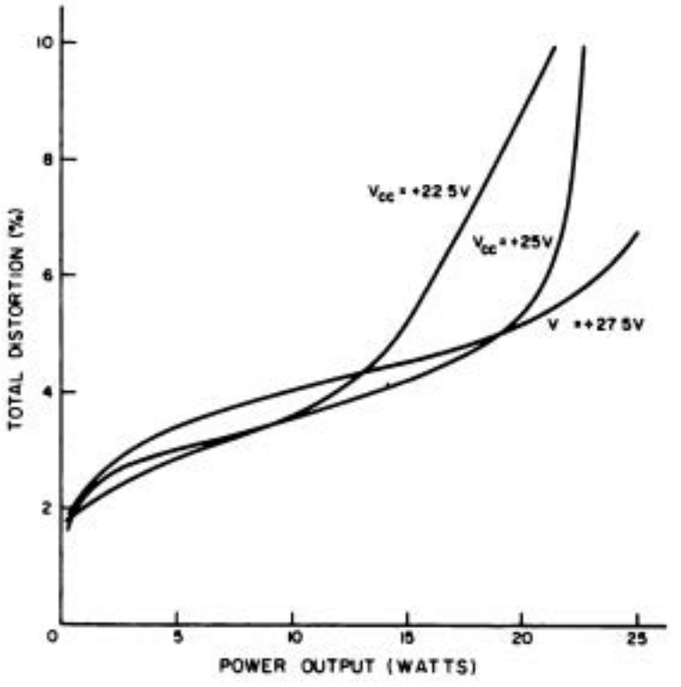


Figure 35–2.—Total Distortion vs. Power Output, Showing Effect of Supply Voltage Variation

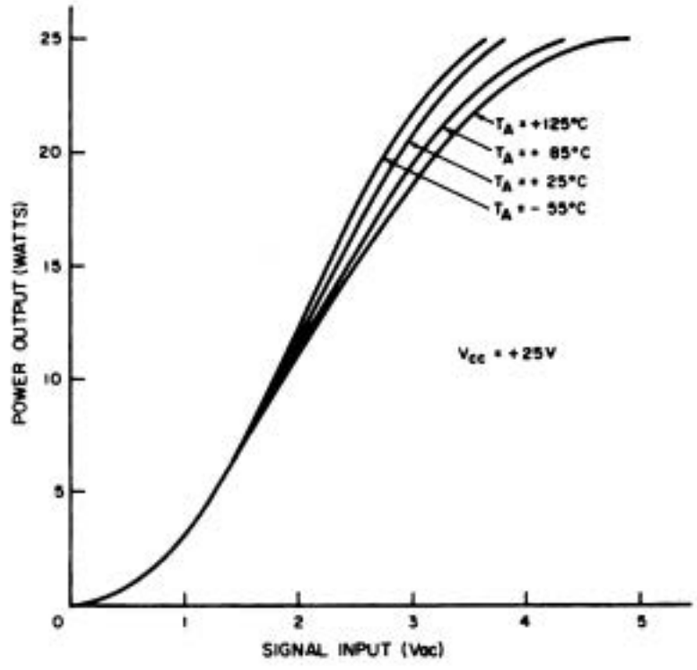


Figure 35–4.—Power Output vs. Signal Input, Showing Effect of Temperature Change

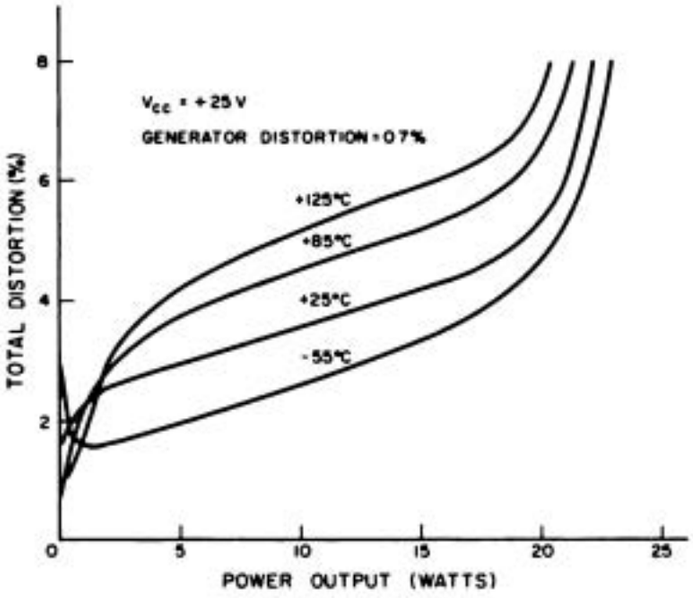


Figure 35-5.—Total Distortion vs. Power Output, Showing Effect of Temperature Change

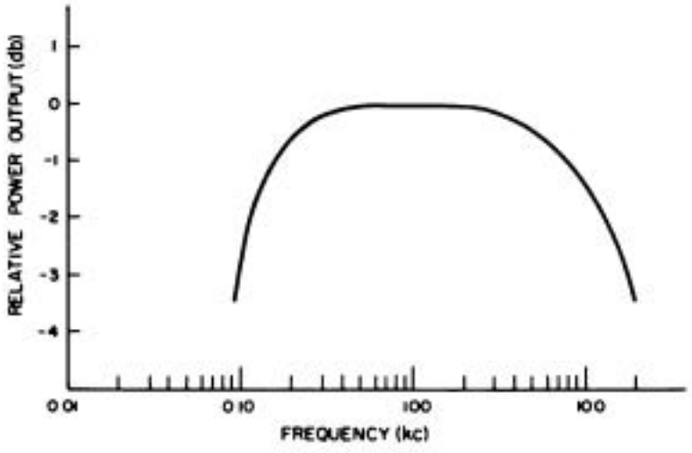


Figure 35-6.—Typical Frequency Response at 25°C (Constant Input Signal Level = 1.9 Vac; Reference Output Level, 0 db = 10 watts)

with a dc ammeter. The ammeter indicated the average value of a composite current consisting of a constant dc current to the class A driver and a pulsating dc current to the class B push-pull amplifier.

(2) The constant dc driver current was subtracted from the ammeter reading of step 1. The remainder was converted to an RMS value by the following relation:

$$I_{RMS} = \frac{\Pi}{2\sqrt{2}} I_{AVE}$$

(3) The total power delivered to the final stage was then calculated by multiplying the RMS current by the supply voltage. Power dissipated in load, feedback circuit, biasing, and emitter resistors was then subtracted from the total power. The remainder is the power dissipated in the two transistors and output transformer. Figure 35-3 assumes a transformer efficiency of 100%. Actual transformer losses therefore will provide a slight margin of safety beyond the transistor dissipation levels referenced in figure 35-3.

Figure 35-4 shows that the power gain of the circuit is reasonably constant with regard to ambient temperature change, particularly at levels below 10 watts. The total variation in power gain from −55°C to ±125°C is approximately 1.4 db at 20 watts of output power, and diminishes to 0 db at 7 watts.

Total distortion increases with temperature, as can be seen from figure 35-5. For an output of 20 watts, distortion approaches 8% at +125°C, and is down to less than 5% at +25°C. The quiescent collector current level maintained by biasing resistor R5, to reduce cross-over distortion, varies with temperature. It decreases from a maximum of 175 ma per transistor (Q2 and Q3) at +125°C to 0 at −55°C. Consequently, the −55°C curve of figure 35-5 shows a slight increase as power output falls below 1 watt. Cross-over distortion is evident due to the lack of a quiescent collector current at this temperature. However, as can be seen, the distortion is not severe.

The frequency response of PSC 35, as noted in figure 35-6, is essentially flat between 400 cps and 2 kc. The output power is down 3 db from 1,000 cps at 95 cps and 17 kc. Temperature and supply voltage variations have only a negligible effect on the frequency response.

PREFERRED CIRCUIT NO. PSC 36
IF AMPLIFIER, COMMUNICATIONS

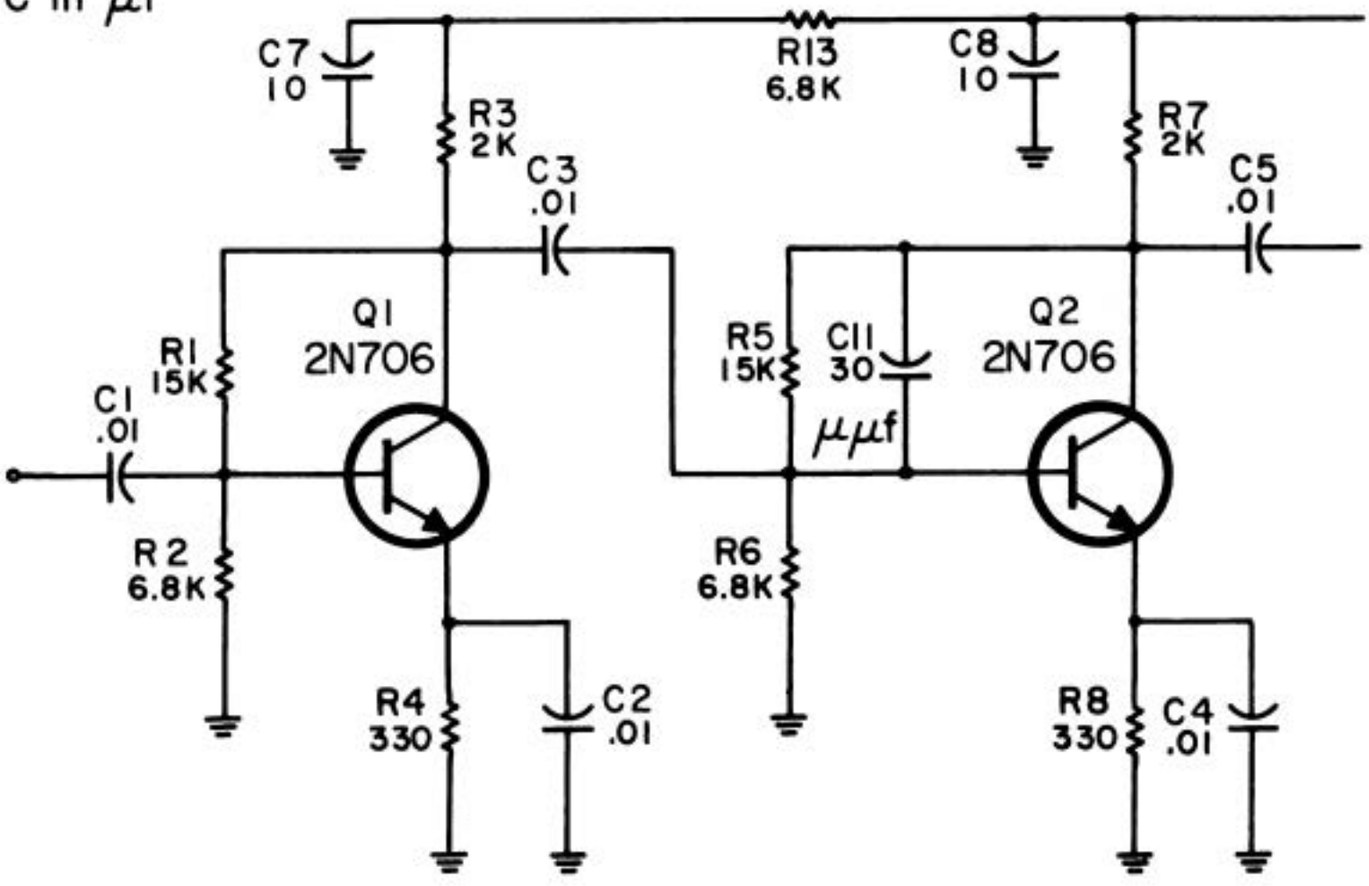
679-962 O—63——6

PREFERRED CIRCUIT NO. PSC 36
IF AMPLIFIER, COMMUNICATIONS

Unless otherwise stated:

R in ohms;

C in μf



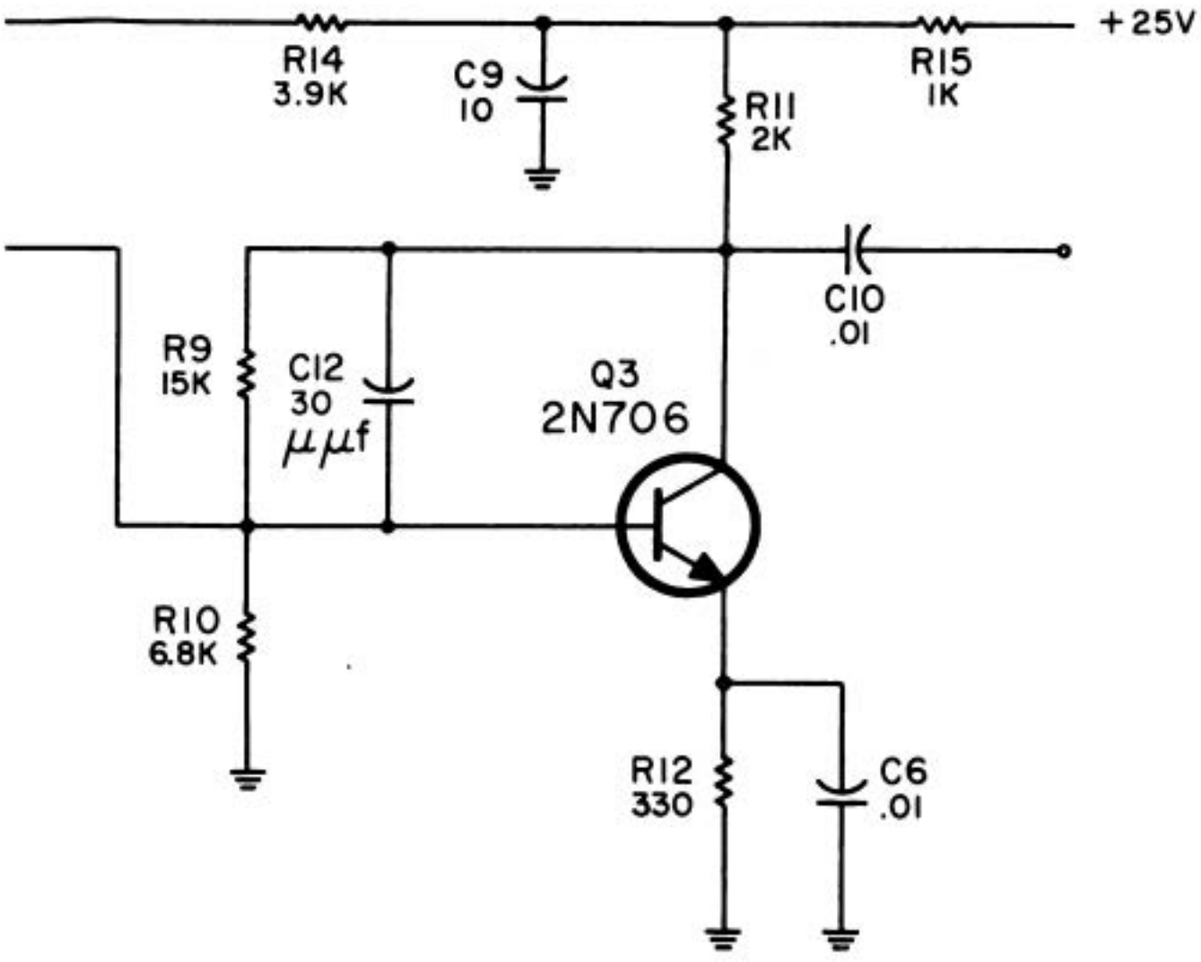
Components:

Resistor power dissipation (Note 1): R1, R2, R3, R4, R6: <1 mw; R5, R8, R9, R10: <5 mw; R7, R12, R13: <15 mw; R11, R14, R15: <75 mw.
Limits (these are not tolerances; see note 2): All R: ±20%; all C: +50%, −20%.

Operating characteristics (Note 3):

Center frequency: 500 kc.
Bandwidth: down 3 db at 240 kc and 1200 kc.
Maximum voltage gain (output unloaded): 800.
Maximum power gain (550Ω load): 55 db.
Input impedance: 1000Ω.
Output impedance: 550Ω.
Minimum discernible signal: <10 microvolts.
Maximum input signal without AGC: 5 mVac.
Output noise level: 20 mV peak to peak (maximum).
Operating temperature: −55°C to +125°C.

ower requirements: +25 volts ±10% at 10 ma (maximum).



Notes:

1. These are maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

3. Operating characteristics as listed are based on data taken in a test at 25°C, employing transistors of nominal parameters at a supply voltage of +25 volts. Unless stated otherwise, output is loaded with a 5.6KΩ resistor. Output shunt capacitance attributable to test equipment and connecting cable is 25 pf.

PSC 36 IF AMPLIFIER, COMMUNICATIONS

1. APPLICATION

This circuit may be employed as the final IF amplifier in a multiple conversion communications receiver as well as in those systems requiring only single conversion. Through the use of an appropriate input filter, the user is permitted considerable latitude in selection of bandwidth and center frequency. Maximum gain occurs at approximately 500 kc and is down only 1 db at 350 kc and 850 kc. Automatic gain control is not included as an integral part of the circuit; however, one method of applying AGC to the circuit is discussed in section 3, and the range of control is shown graphically.

2. DESIGN CONSIDERATIONS

The 2N706 transistor used in the circuit is listed as a preferred type in MIL–STD–701C. It was chosen because of its high frequency characteristics and ability to operate at a high ambient temperature.*

The circuit is an untuned wide band amplifier which must be used with an input filter to provide the desired frequency response. This technique is frequently employed in military transistorized receivers. The alternate method, which determines frequency response through the use of individually tuned circuits, suffers from the serious disadvantage of a shift in response, with variations in ambient temperature and the application of automatic gain control. If the desired response is determined through the utilization of an external filter, a considerable shift in the frequency response of a wide band amplifier is immaterial.

The circuit configuration is similar to several used at present in naval airborne VHF receivers, and is considered the simplest possible arrangement consistent with good stability and the required parameters.

To minimize transistor noise, collector current and voltage are maintained at the lowest level consistent with the required gain. The nominal quiescent collector voltage and current of the first stage are 2.5 volts and 0.35 ma, respectively.

Except for capacitors C11 and C12, which limit the high frequency response of the amplifier, the three stages are identical. Consequently the following description of the first stage will serve adequately for all three.

Q1 is operated as a class A, common emitter, RC-coupled amplifier. The quiescent operating point is established by R1 and R2, the desired collector voltage by the series voltage-dropping resistor R13. R3 is the collector load resistor and, in conjunction with C7, provides the necessary RF decoupling to prevent regeneration. The emitter resistor, R4, provides adequate dc stabilization. Bypass capacitor C2 is low enough in value to provide ample degenerative feedback consistent with required circuit gain. Additional degeneration is also supplied through R1. Such degeneration minimizes variations in gain which are attributable to temperature and supply voltage changes, as well as to transistor product variability.

The value of capacitors C11 and C12, which limit the high frequency response of the amplifier, were chosen to provide maximum circuit gain at approximately 500 kc.

3. PERFORMANCE

Graphic presentations of performance—specifically, circuit gain, frequency response, and application of automatic gain control—are given in this section. Also illustrated are those deviations from the nominal values listed under "Operating characteristics" which are attributable to changes in load and temperature as well as to transistor product variability.

DC current gain is used as a measure of transistor product variability. Curves labeled High h_{FE} and Low h_{FE} are based on data taken while employing two sets of three transistors whose dc current gains are 105 and 32, respectively.

As indicated in figure 36–1, overall circuit gain is constant for a given transistor h_{FE} and temperature. Voltage gain at 25°C with a load resistance of 5.6KΩ varies from 600 with low gain transistors to 900 with high gain transistors. This is the maximum variation in gain

*ARINC Research Corporation, "Reliability and Application Data for Transistors Used in Missile Electronic Systems," Publication No. 145–11–271.

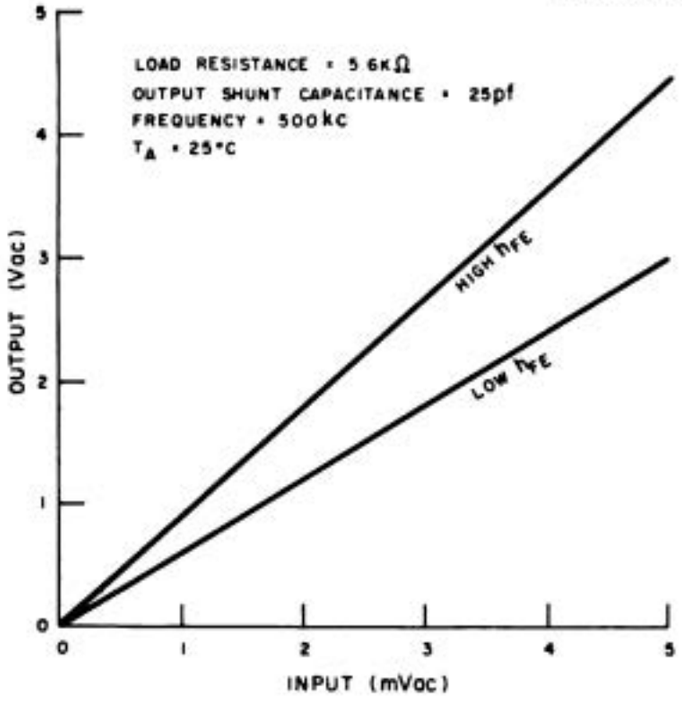


Figure 36-1.—Output Volts vs. Input Signal for Upper and Lower Limit Values of h_{FE}

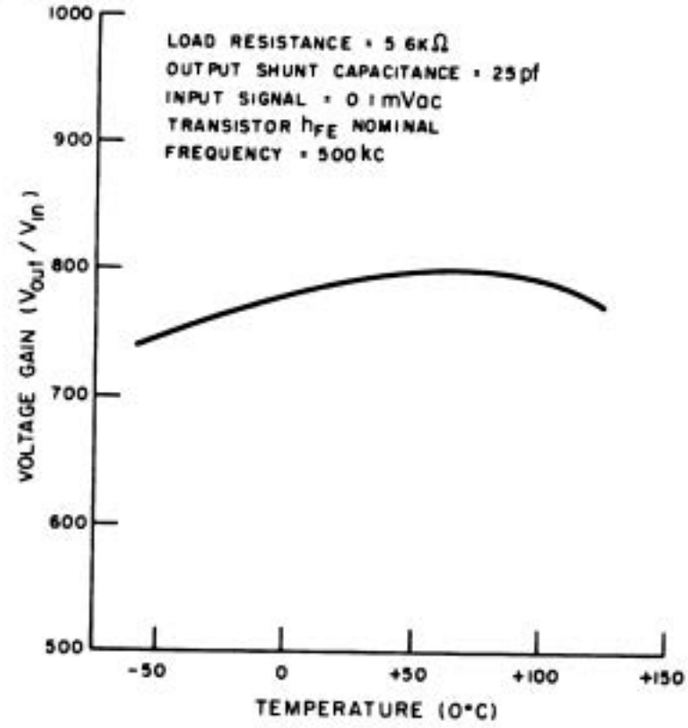


Figure 36-3.—Voltage Gain vs. Temperature

which is attributable to transistor product variability. The limit values of h_{FE}, as demonstrated in figure 36-1, have a ratio of approximately 5 to 1.

As shown in figure 36-2, voltage gain with a resistive load of 560Ω is approximately one-half of the open circuit value. The output cabling and test equipment used to acquire the data for all of the figures in the text had a shunt capacitance of approximately 25 pf. At 500 kc, this amount of capacitance has a reactance of approximately 12.7KΩ. The result will be a complex load impedance with a magnitude of approximately 5.1KΩ when a 5.6KΩ resistor is placed across the output terminals. Note in figure 36-2 that when the circuit is so loaded, voltage gain is almost that obtained at open circuit (25 pf).

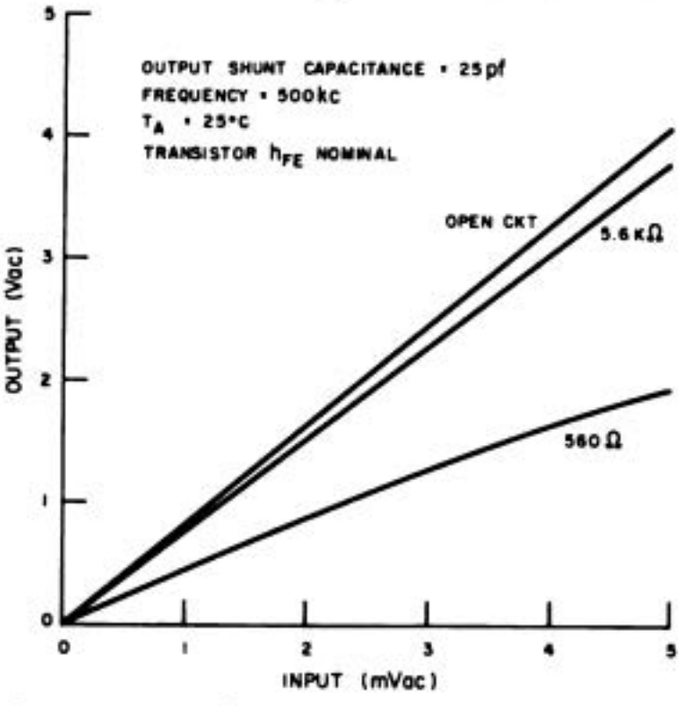


Figure 36-2.—Output Volts vs. Input Signal for Three Different Load Conditions

Figure 36-3 indicates that voltage gain can be expected to increase approximately 8% when the ambient temperature increases from −55°C to +50°C, and to decrease 4% when the temperature increases from +50°C to +125°C. These percentages are based on data taken while using three transistors of nominal h_{FE}. The actual h_{FE} of each of these transistors is 42; they were used in the acquisition of all data presented in the text that refer to nominal transistor h_{FE}. Voltage gain will vary approximately 15% with a ±10% supply voltage change, regardless of transistor h_{FE}.

Figures 36-4 and 36-5 show the shift in bandwidth that is attributable to transistor product variability and temperature. Neither figure reflects the difference in gain at a given frequency which is attributable per se to product variability and temperature. This variation at a frequency of 500 kc is illustrated in figures 36-1 and 36-3.

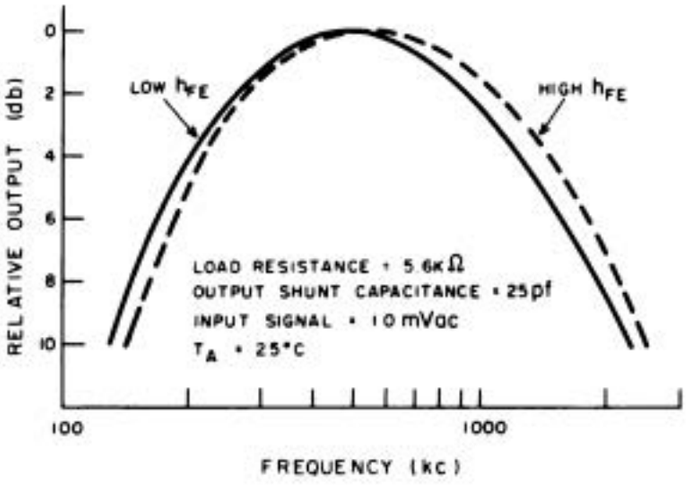


Figure 36-4.—Relative Output vs. Frequency of Input Signal with Upper and Lower Limit Values of h_{FE}

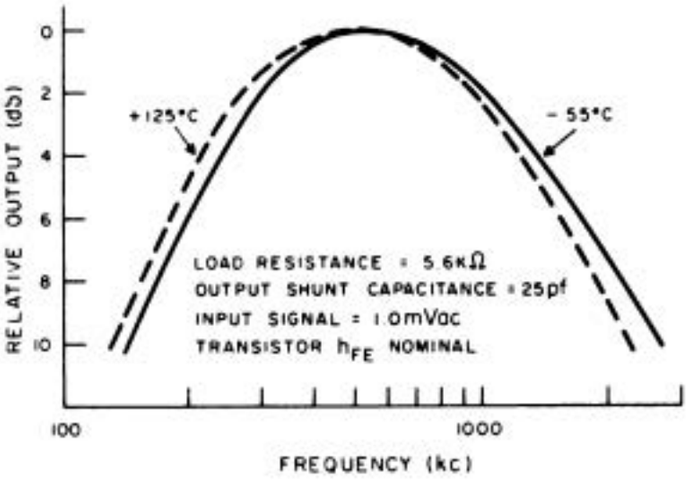


Figure 36-5.—Relative Output vs. Frequency of Input Signal at the Upper and Lower Limits of the Ambient Operating Temperature Range

Automatic gain control may be applied to the amplifier by removing the emitter circuits of Q1 and Q2 from ground and returning them to a variable dc voltage. The ac signal current must be adequately bypassed to ground at this point with a 10 UF capacitor. Figure 36-6 indicates the voltage gain obtained as a function of positive dc voltage ranging from 0 to 1.5V applied to this point. Under the conditions stated in figure 36-6, when the dc level reaches 1.5V, transistor Q1 will be cut off. The minimum cut-off level for Q1 is 1.3V.

Figure 36-7 indicates the shift in response attributable to automatic gain control action under the conditions stated on the figure, normalized for purposes of comparison. The actual difference in relative output between the

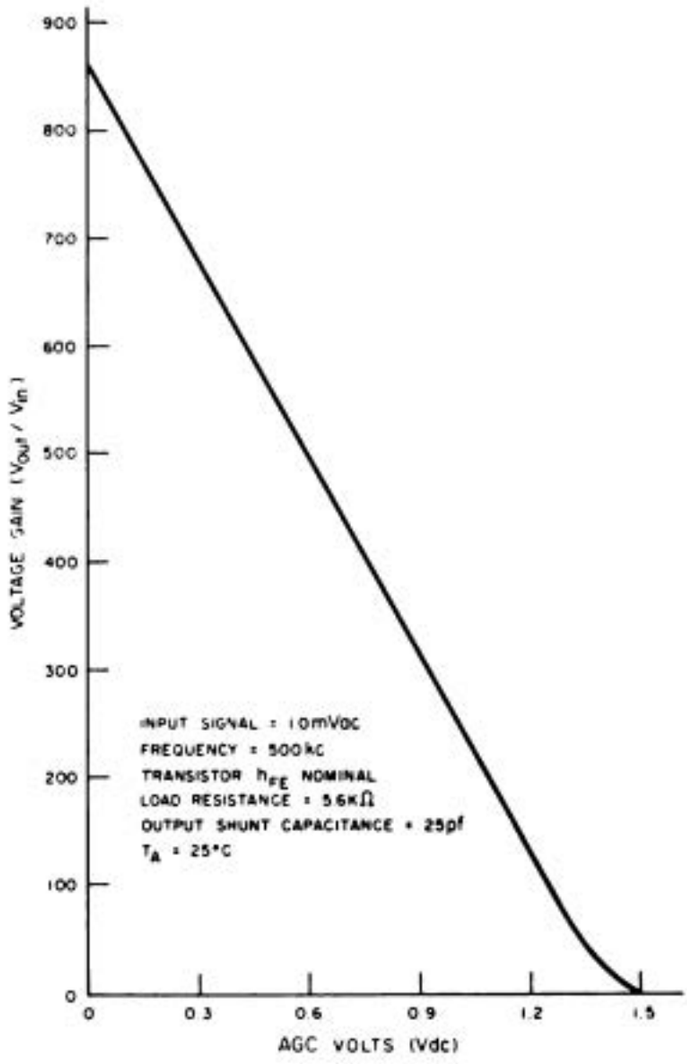


Figure 36-6.—Voltage Gain vs. AGC Voltage with Emitter Circuits of First Two Stages Returned to AGC Source

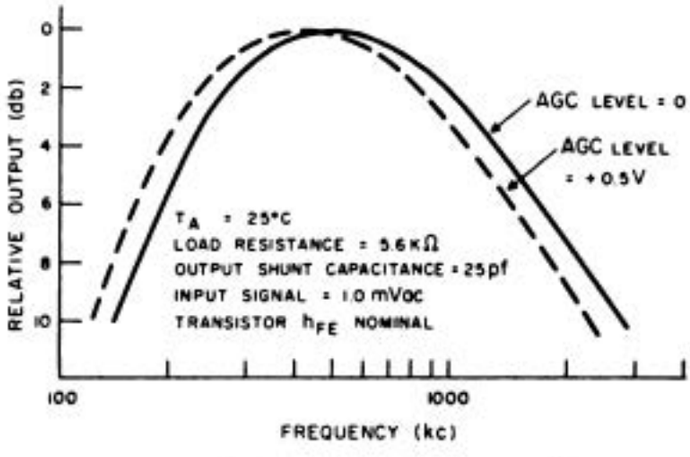


Figure 36-7.—Relative Outputs vs. Frequency Showing the Effects of AGC on Frequency Response

0 and 0.5V levels of automatic gain control can be obtained from figure 36-6 for the frequency of 500 kc.

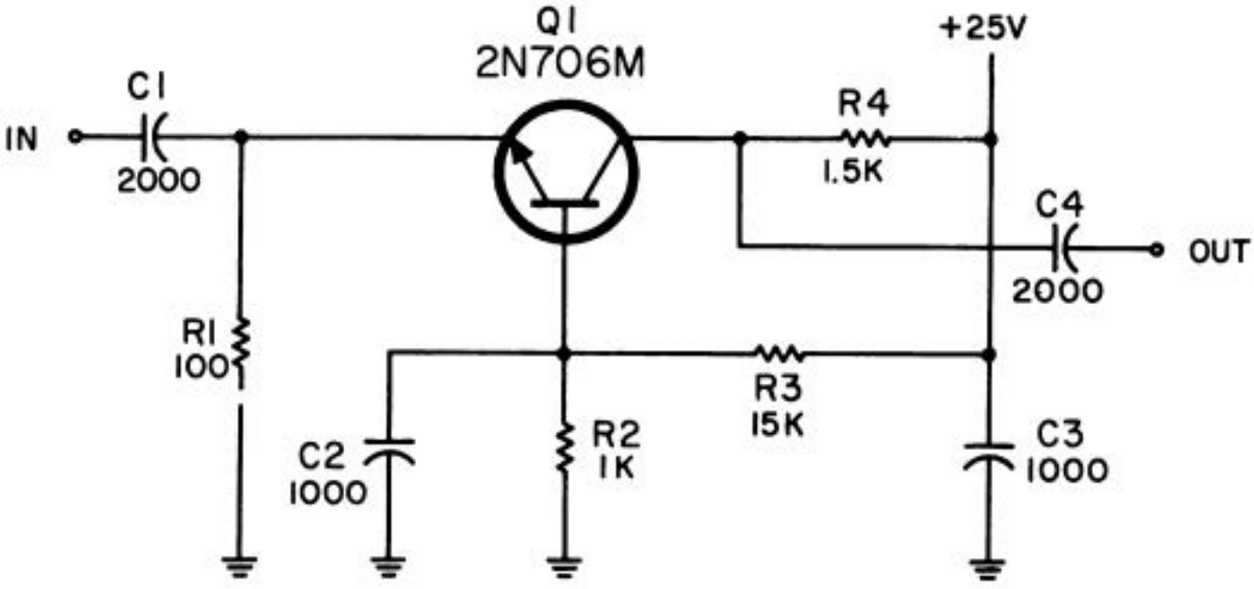
Notes

PREFERRED CIRCUIT NO. PSC 37
RF AMPLIFIER, 1 TO 100 MC

PREFERRED CIRCUIT NO. PSC 37
RF AMPLIFIER, 1 TO 100 MC

Unless otherwise stated:

C in pf; R in ohms



Components:

Resistor power dissipation (Note 1): R1: <10 mw; R2: <5 mw; R3: <50 mw; R4: <100 mw.

Limits (these are not tolerances; see note 2): All R: ±20%; all C: +50%, −20%.

Operating characteristics (Note 3):

Frequency response (Note 4): Voltage gain in excess of unity from <1 mc to >100 mc.

Maximum voltage gain (Note 4): 53 at 6 mc.

Noise figure: 7 db maximum.

Input impedance (Note 5): 78Ω at 1 mc; 20Ω at 10 mc; 32Ω at 100 mc.

Output impedance (Note 5): 1.3KΩ at 1 mc; 865Ω at 10 mc; 155Ω at 100 mc.

Operating temperature: −55°C to +125°C.

Heat sink requirements: none.

Power requirements: +25 volts ±10% at 10 ma.

Notes:

1. These are the maximum powers dissipated in the resistors. In determining these values, allowances have been made for variations in component values, power supply voltages, and transistor characteristics.

2. The performance specifications are based on component values which do not deviate from nominal by more than the limits specified. The term "limits" includes initial tolerance plus drifts caused by environmental changes or aging.

3. Those operating characteristics involving circuit impedance and gain are averages resulting from circuit measurements made with the use of 20 randomly selected transistors from 3 manufacturers.

4. Circuit gain is dependent on signal frequency, transistor product variability, supply voltage, temperature, and source and load impedances.

5. Impedance values shown are absolute. Refer to text for complex impedance.

PSC 37 RF AMPLIIFIER, 1 TO 100 MC

1. APPLICATION

This circuit is suitable for use in any application that requires small signal amplification or buffer action over the frequency range of 1 to 100 mc. No tuning is employed, the purpose of this feature being to enable the user to incorporate any desired frequency rejection through the use of appropriate input and output coupling circuitry. Input and output impedance variations with frequency are presented in graphical form to simplify the design of coupling circuitry. The circuit will provide an average voltage gain of 18 at 1 mc, increasing to a maximum of 50 at 6 mc, and decreasing to a minimum of 4 at 100 mc. Two or more stages may be connected in cascade with appropriate coupling circuitry to provide additional amplification when required.

2. DESIGN CONSIDERATIONS

With the exception of the fact that PSC 37 is not tuned to a particular passband, this circuit is similar in performance to RF amplifiers presently used in many Naval airborne equipments. Tuning is deliberately avoided in order to provide circuit utility over a broad frequency range. It is anticipated that individual passband requirements will be accomplished through the use of appropriate coupling circuitry.

The 2N706M transistor was selected for use in PSC 37 because of its high frequency characteristics and relatively large power-dissipating capacity. The 2N706M is a silicon, NPN transistor listed as a preferred type in MIL-STD 701C dated 9 July 1962.

The common base configuration is employed to provide a high voltage gain over a wide frequency range with maximum isolation between the input and output.

The input signal is applied to the emitter through coupling capacitor C1. Emitter resistor R1 provides the necessary dc ground return and is of sufficient value to prevent thermal runaway at the maximum operating temperature of 125°C. The circuit is biased by the voltage dividing network consisting of R2 and R3. The collector load resistor, R4, limits collector current and voltage to values consistent with the power-dissipation capability of the transistor. Bypass capacitors C2 and C3 provide the necessary AC ground return and limit the circuit gain at low frequencies.

Coupling capacitors C1 and C4, as well as bypass capacitors C2 and C3, were fixed at values appropriate for displaying circuit performance over a wide frequency range. In some applications, particularly at the extremes of the frequency range, it may be desirable to adjust the values of the coupling capacitors and the base bypass capacitor to provide optimum gain. The impedance of the base bypass capacitor is 100Ω, or 10% of the base biasing resistor R2, at approximately 1.5 mc.

3. PERFORMANCE

This section summarizes the performance of PSC 37 through the presentation of data taken by direct measurement. Amplifiers operating within the frequency range of this circuit are significantly affected by stray reactances. These reactances are in turn determined to a large extent by the construction techniques employed as well as by the type of components used.

All quantitative information in this section is based upon measurements made on a circuit constructed in the following manner:

> A teflon transistor socket was mounted in the center of a 3" x 2.5" sheet of copper ground plate. Three BNC female panel connectors, type UG-290/U, were soldered to the ground plate to accommodate the input and output signals and the supply voltage. The two bypass capacitors, of the high frequency button type, were soldered directly to the ground plate. Lead lengths were made as short as possible, and all components were mounted close to the plate. All resistors were of the deposited carbon film type.

Figure 37-1 shows the component layout.

Figure 37-2 shows the frequency response of PSC 37 over the range from 1 to 100 mc. The circuit load consists only of the RF voltmeter used to monitor the output level. The voltmeter probe, which has a shunt capacitance of 1.5 pf and a resistance of 10MΩ, was con-

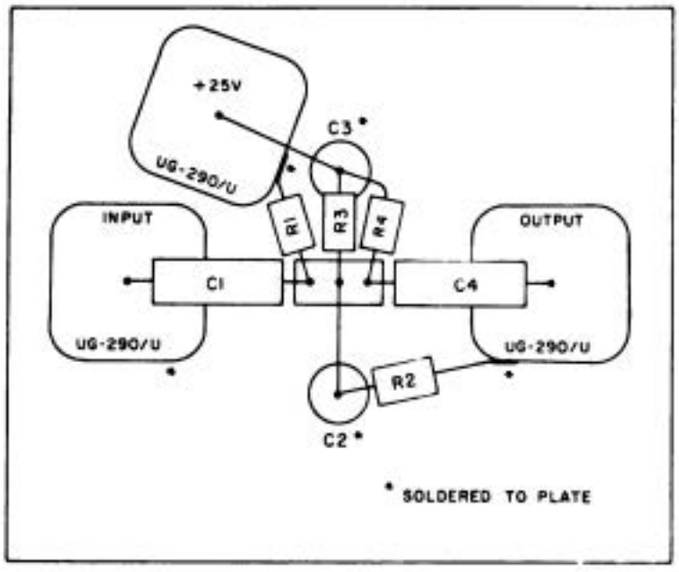


Figure 37–1.—Circuit Layout Used for Performance Measurements (Actual Size)

nected directly to the low side of the output coupling capacitor. The vertical lines define the voltage gain limits obtained from 20 transistors randomly selected from 3 manufacturers. The voltage gain of the circuit with respect to a particular transistor may fall near the lower limit at a given frequency and near the maximum limit at some other frequency. The variation shown is approximately 3 to 1 above 10 mc. The variation decreases for frequencies below 10 mc as the reactance of the base bypass capacitor increases sufficiently to provide an increasing degree of degenerative feedback with a decrease in frequency.

Typical voltage gain variations over the operating temperature range are shown in figure 37–3 at various frequencies between 1 and 100 mc. The output level was monitored through a shielded cable of approximately 8 pf shunt capacity. The circuit load consisted of the cable shunt capacity and the voltmeter probe previously described. The maximum gain variation shown is a decrease of approximately 20% from −55°C to +125°C at 10 mc.

Collector supply voltage variations of ±10% will result in gain variations of ±15% at frequencies of approximately 10 mc and above. The variation in gain decreases at frequencies below 10 mc and becomes negligible at 1 mc.

Figure 37–4 shows output signal vs. input signal at frequencies of 5 and 50 mc. The curves are based on data taken with a transistor whose gain characteristics may be classed as average. The output load consisted only of the voltmeter probe previously described. The two curves show that, regardless of frequency, output signal is a linear function of input signal until the input level is approximately 100 mVac. The sharp knee seen in curve (b) results from limiting action by the transistor as the collector voltage swing approaches its maximum limit. At higher frequencies, as indicated in curve (a), ac current gain of the transistor has decreased to the extent that the collector voltage swing is well below that required to produce limiting action in the output.

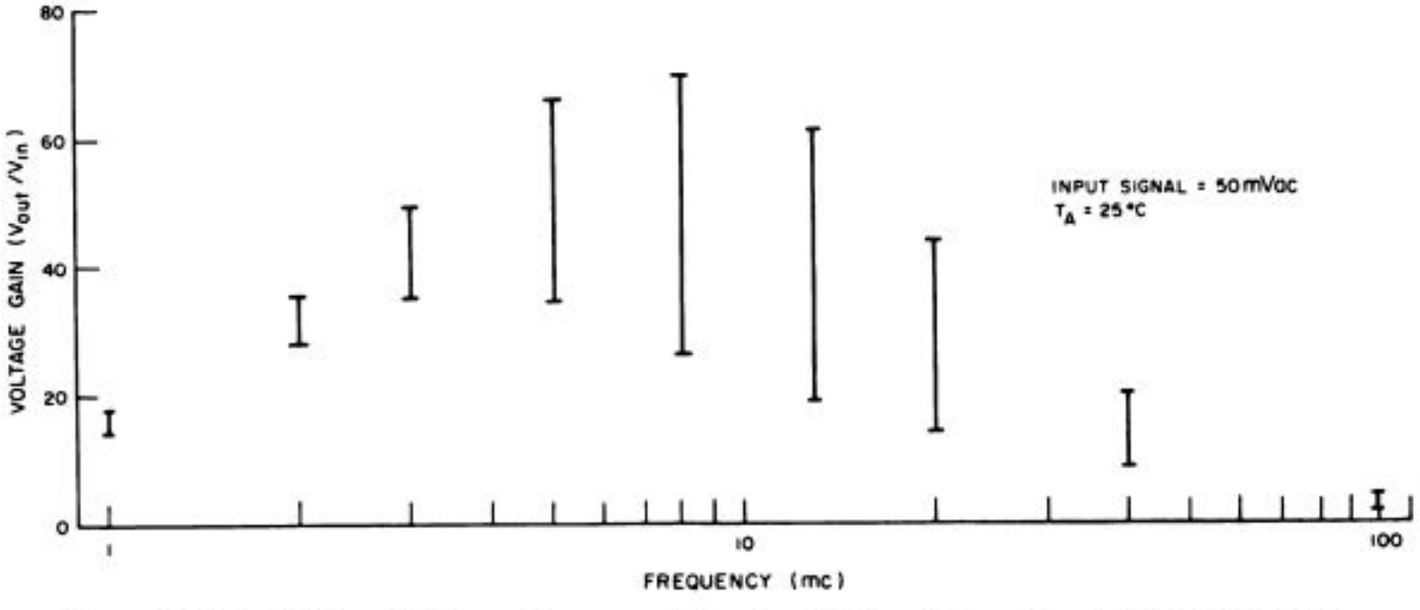


Figure 37–2.—Voltage Gain vs. Frequency, Showing Effects of Transistor Product Variability

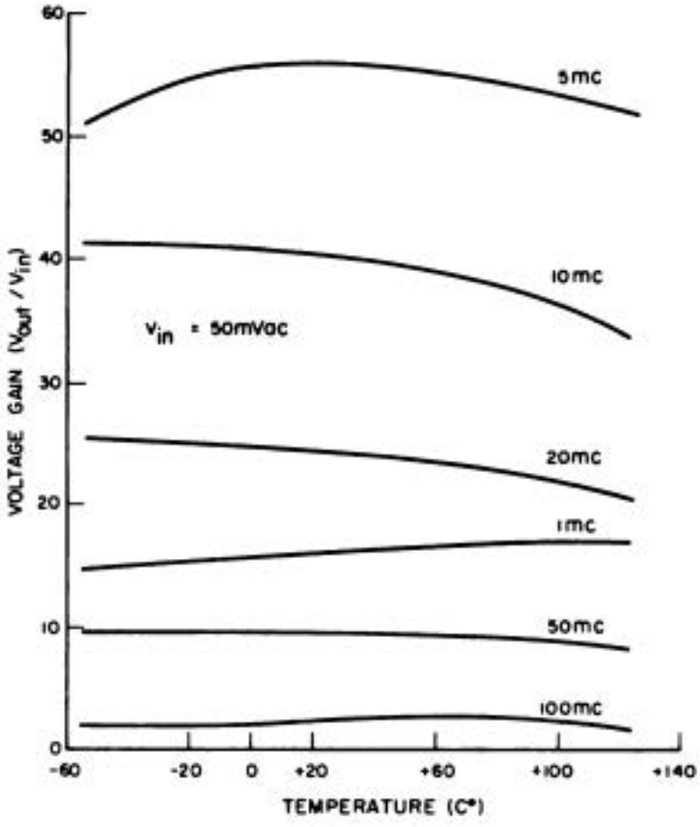


Figure 37-3.—Voltage Gain vs. Temperature at Various Frequencies, Employing a Transistor With Typical Gain Characteristics

The equivalent parallel capacitance and resistance that appear across the input terminals with the output open-circuited are shown in figures 37-5 and 37-6 respectively. The capacitance at 1 mc of 2100 pf is determined by the value of the input coupling capacitor and diminishes, as the inductive reactance increases, to 0 at approximately 10 mc. Between 10 and 100 mc, the mean equivalent parallel reactance is inductive, as indicated by negative values of c_p in figure 37-5. The vertical lines define the limits produced by 20 randomly selected transistors from 3 manufacturers. The complex input impedance may be calculated by extracting the values of r_p and c_p, at the frequency of interest, from figures 37-5 and 37-6 and applying the following formula:

$$Z=\frac{r_p-j\omega r_p^2 c_p}{1+\omega^2 r_p^2 c_p^2}$$

where: $\omega=2\pi f$

$j=\sqrt{-1}$

Figures 37-7 and 37-8 show, respectively, equivalent output parallel capacitance and resistance. The method for calculating output complex impedance is identical to that described above for the input impedance.

The input and output parameters of r_p and c_p associated with a particular transistor may fall near the minimum limit at a given frequency and near the maximum limit at some other frequency.

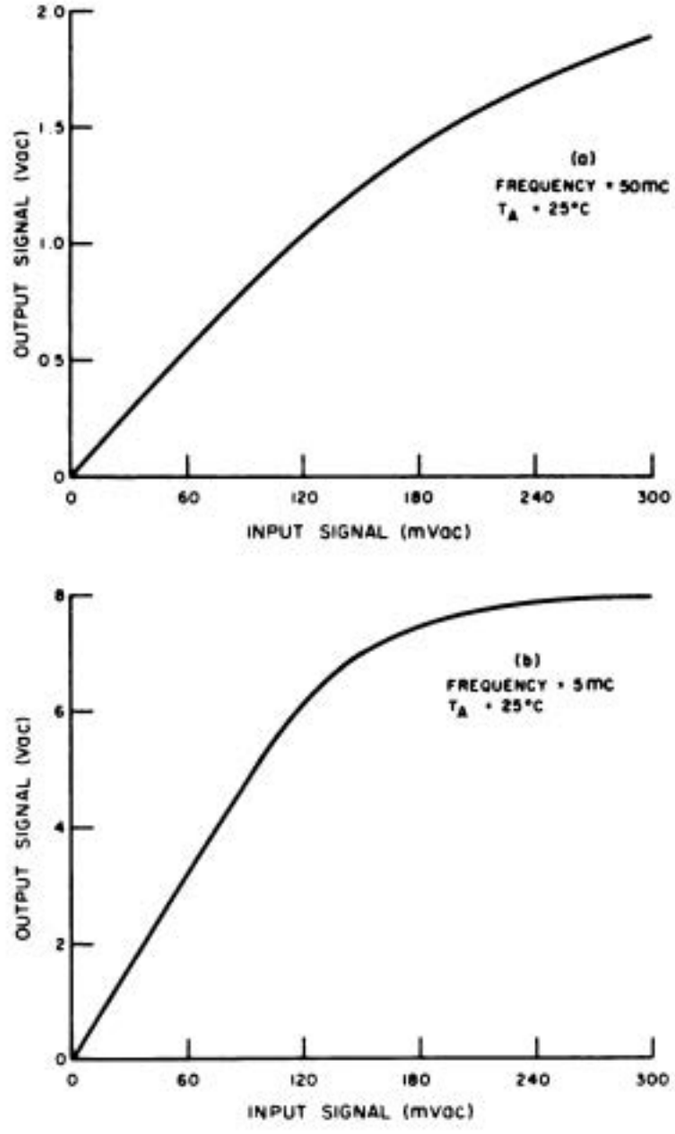


Figure 37-4.—Output Signal vs. Input Signal

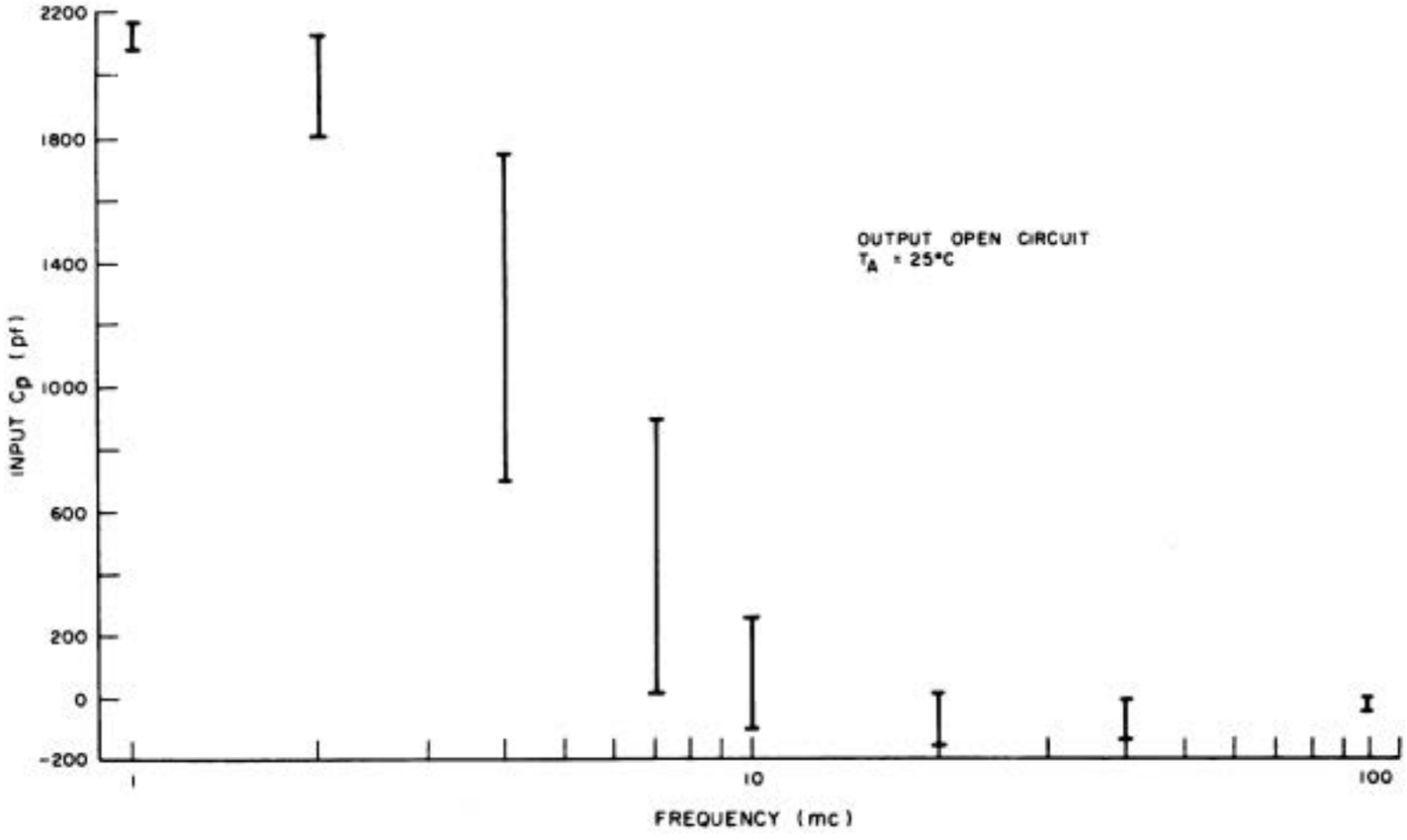


Figure 37–5.—Input Parallel Capacitance vs. Frequency, Showing Effects of Transistor Product Variability

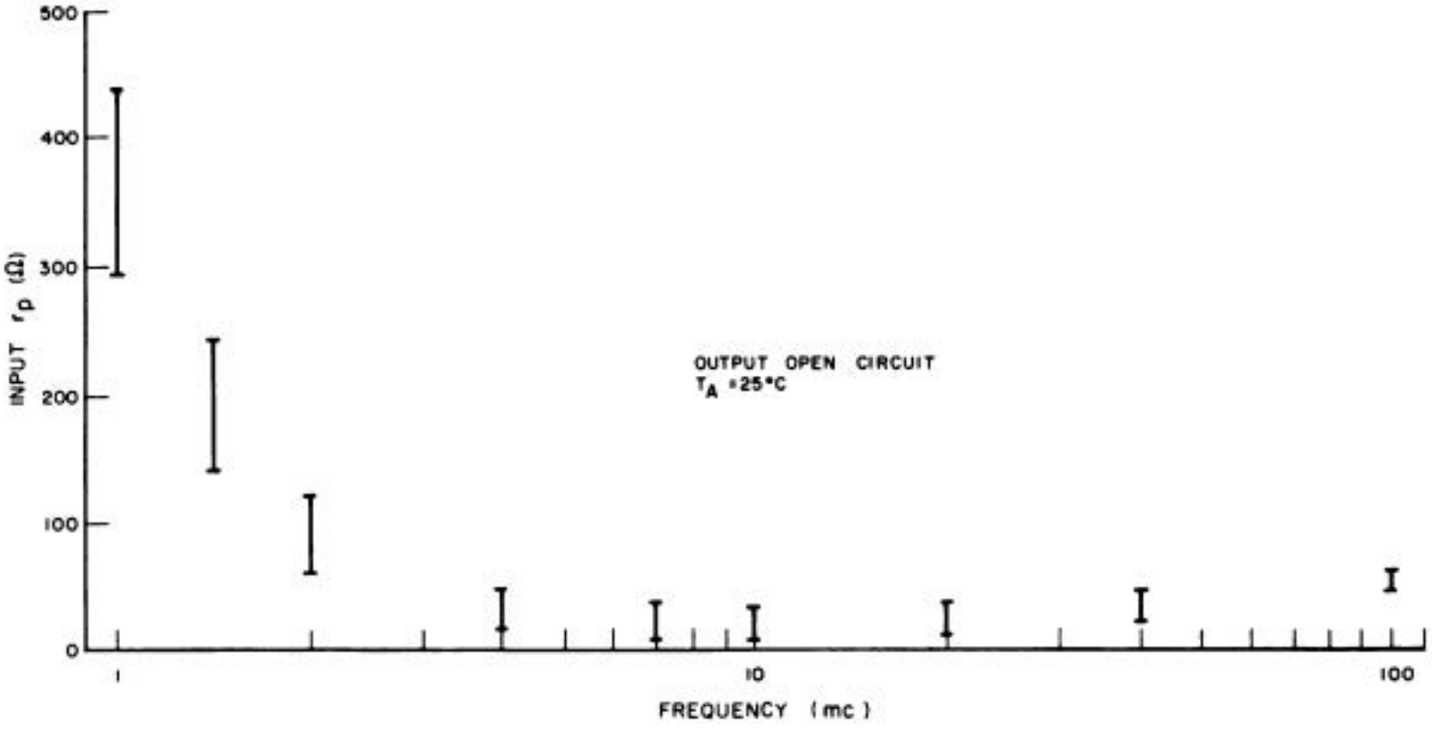


Figure 37–6.—Input Parallel Resistance vs. Frequency, Showing Effects of Transistor Product Variability

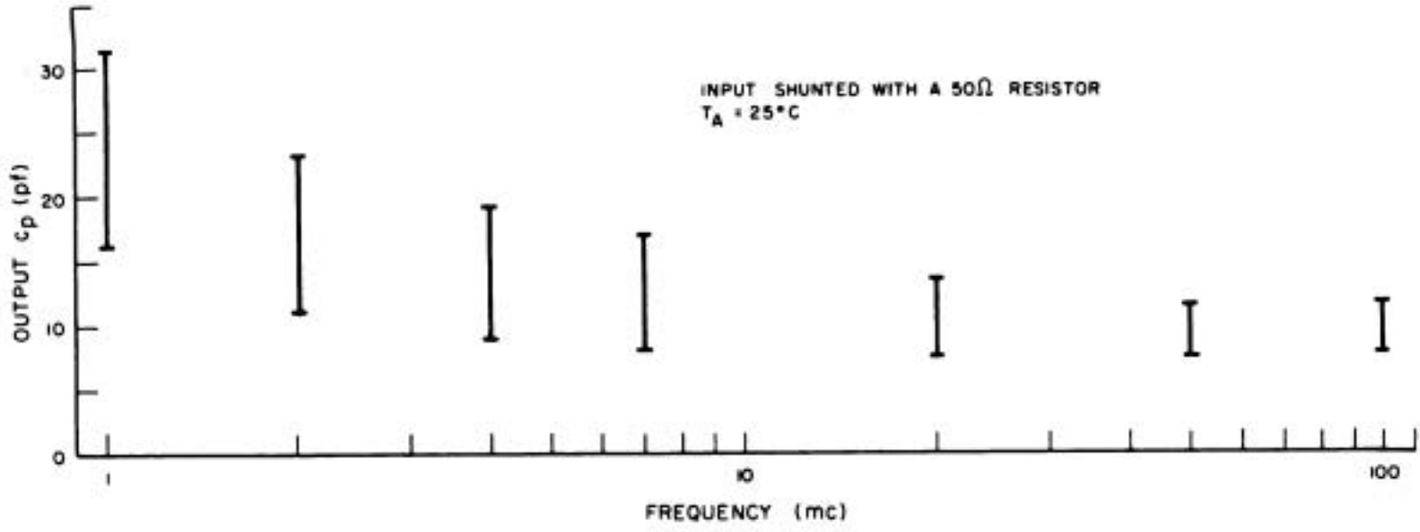


Figure 37-7.—Output Parallel Capacitance vs. Frequency, Showing Effects of Transistor Product Variability

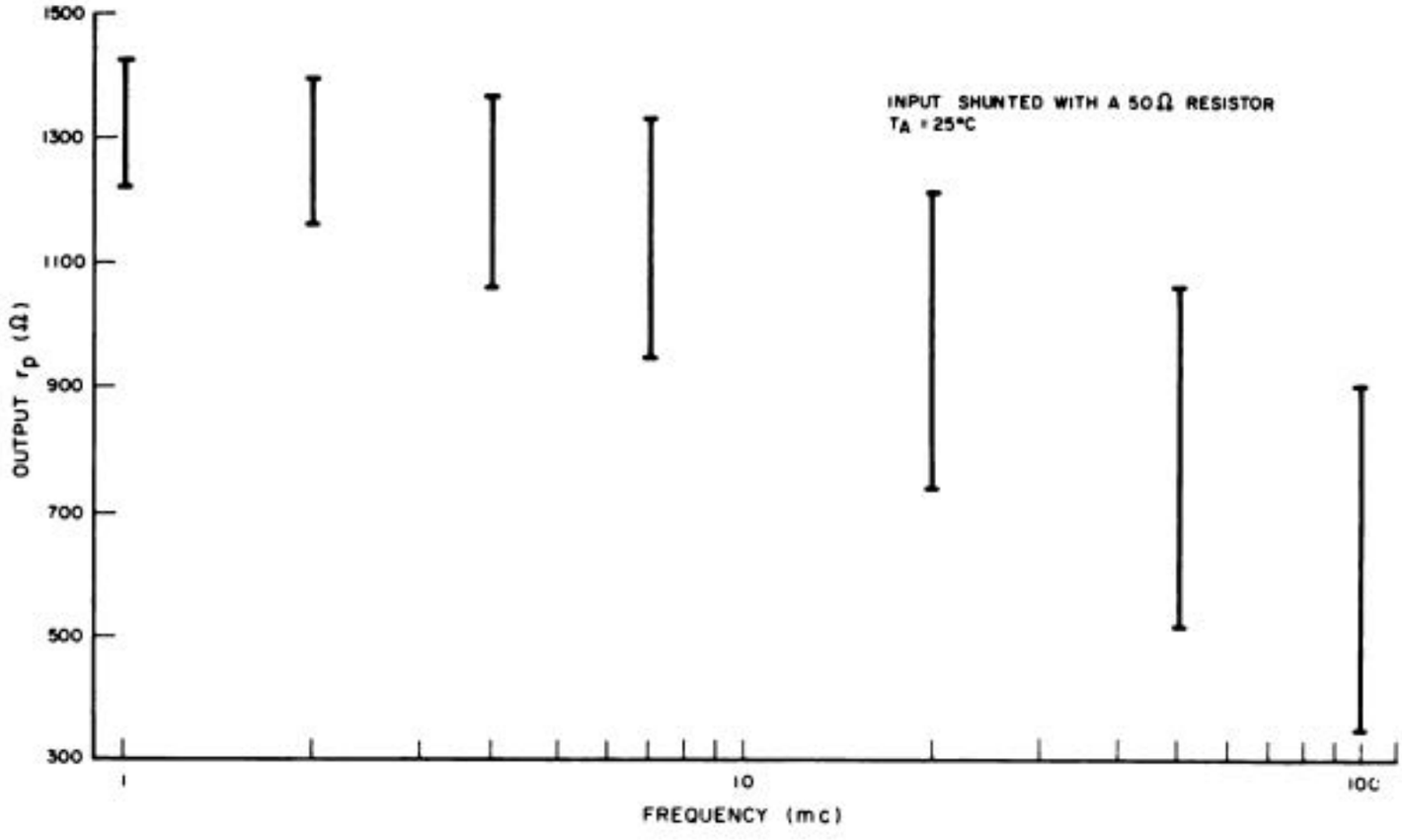


Figure 37-8.—Output Parallel Resistance vs. Frequency, Showing Effects of Transistor Product Variability

CIRCUIT INDEX

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