

SECTION 19**LOGIC CIRCUITS****PART A. ELECTRON-TUBE CIRCUITS**

Part A of this section is reserved for electron tube logic circuits, which may be included in a later revision of the Handbook. No electron tube circuits are discussed in this issue.

PART B. SEMICONDUCTOR CIRCUITS

LOGIC POLARITY.

Computer logic is expressed by a form of two-value logic which is easily adaptable to the binary number system. Thus computer elements (circuits) have only two states, such as: the conduction or nonconduction of a circuit, the presence or absence of a hole on a card or paper, or the presence or absence of a magnetic field. The use of two-value logic also means that, basically, these states may assume a value of either 0 or 1. (While **true** or **false** could also be used, the numeric values lend themselves readily to computations and algebraic manipulations.)

In any electrical circuit, any two distinct voltages or currents can be used to represent the two logic states of 0 and 1. For example, a negative voltage could indicate 0 and a positive voltage could indicate 1, or vice versa. Likewise, current flow into the circuit could indicate 0, and current flow out of the circuit could indicate 1. Similar results could be obtained with amplitude control, using small and large voltages or currents. Pulses could also be used in a like fashion, with a negative pulse indicating 0 and a positive pulse indicating 1; or 0 could be indicated by the absence of a pulse, in which case the presence of a pulse could signify 1. Many combinations of logic expressions are possible; they can also be used interchangeably, since each logic element (circuit) or operating entity can actually function independently as long as the desired result is achieved. Mixed logic systems are not used in large computers, however, since this practice would cause expensive circuit complications. Most present-day logic systems utilize **polarity** to define the circuit state, since positive and negative voltages are easily obtained and manipulated, regardless of whether the actual logic element (circuit) employs relays, switches, diodes, or transistors. Logic circuits can be divided into two general classes, according to polarity, namely positive and negative logic. As employed on logic diagrams, a signal may assume either the "active (or true)" state (logic 1), or the "inactive (or false)" state (logic 0). The electrical signal levels used and a statement concerning whether positive or negative logic applies are usually specified explicitly on the individual logic diagrams by the manufacturer or the logic designer.

In practice, many variations of logic polarity are employed: for example, from a high-positive to a low-positive voltage, or from positive to ground; from a high-negative to a low-negative voltage, or from negative to ground; and mixed polarity, from a high positive to a negative (below ground) potential, and vice versa. A brief discussion of the two general classes of polarity is presented in the following paragraphs. Each of the logic circuit discussions also given in this section will be based upon the form of logic polarity best suited for simple explanation of the circuit action. Diode logic circuits will be discussed separately from transistor logic circuits in Part B of this section, and purely mechanical circuits

involving only switches and relays will be covered under "Mechanical Circuits", Part C of this section.

POSITIVE LOGIC.

APPLICATION.

Positive logic polarity is usually more adaptable to the use of NPN type transistors.

CHARACTERISTICS.

The input activates the logic element only when it is of positive polarity.

The output of the logic element is also of positive polarity (except when it is purposely inverted).

Operation may be from a high positive to a low positive voltage or current, or positive against ground (the high positive voltage or current usually activates the circuit).

CIRCUIT OPERATION.

Positive logic polarity is defined as follows: When the logic 1 state has relatively more **positive** electrical level than the logic 0 state, and the circuit is **activated** (operated) by the logic 1 signal, the logic polarity is considered to be positive. The following typical examples illustrate the manner in which positive logic may be employed.

Example 1: Logic 1 = +10 volts

Logic 0 = 0 volts

Example 2: Logic 1 = 0 volts

Logic 0 = -10 volts

In both examples the logic 1 state is always more positive than the logic 0 state, even though in example 2 the logic 0 state is negative. The previous statements and definitions are particularly appropriate for d-c switching circuits, but also apply to a-c circuits as well. For example, a positive pulse can be used to simulate a positive voltage, and a negative pulse can be used to simulate a negative voltage. However, such complexity is unnecessary, since the absence of a pulse can signify the logic 0 state and the original definition of positive polarity will still apply. That is, the logic 1 state is more positive than the no signal (or logic 0) state.

As normally used, positive logic is more adaptable to NPN type transistors because of the (NPN) polarity requirements. Since a positive collector voltage is required to reverse-bias the NPN transistor, operation of the transistor produces either a low or a high positive output voltage. Thus by using direct coupling, a fully transistorized positively polarized d-c system can be developed, thereby eliminating interstage coupling capacitors and any possible waveform distortion effects. The functioning of direct-coupled transistor logic (DCTL) circuits is discussed later in this section. The use of positive logic, however, is not restricted to NPN transistors, since PNP transistors can be used in a-c systems using the common-emitter (CE) configuration, which inverts the input polarity in the output circuit. The use of NPN transistors merely makes the design of d-c positive logic

circuits easier and simpler, so that normally positive logic is associated with NPN transistors, while negative logic is associated with PNP transistors. At present, however, it is unimportant which type of logic polarity (positive or negative) is used, since logic components and circuits are available for all types. In fact, by using a form of mnemonic (symbolic) notation, such as H for the high or active state (1), and L for the low or inactive state (0), logic design may be completed and circuitry devised without concern for the polarity or levels used. Once the logic design is completed, standard circuits of the proper type and polarity for the components and level to be used are selected, and the unit is constructed.

FAILURE ANALYSIS.

Since positive logic polarity involves the operation of circuits by means of a more positive voltage or signal, it is evident that under normal operation such circuits would be activated by a positive signal and would produce a positive output. However, while the previous statement is generally true, it may not apply to a particular circuit because of special design considerations. Reference should be made to the proper logic circuit (schematic) and flow diagrams to determine the polarity and levels that activate the suspected circuit.

NEGATIVE LOGIC.

APPLICATION.

Negative logic polarity is usually more adaptable to the use of PNP type transistors.

CHARACTERISTICS.

The input activates the logic element only when it is of negative polarity.

The output of the logic element is also of negative polarity (except when it is purposely inverted).

Operation may be from a high negative to a low negative voltage or current, or negative against ground (the high negative voltage or current usually activates the circuit).

CIRCUIT OPERATION.

Negative logic polarity is defined as follows: when the logic 1 state has relatively more negative electrical level than the logic 0 state, and the circuit is activated (operated) by the logic 1 signal, the logic polarity is considered to be negative. The following typical examples illustrate the manner in which negative logic can be employed.

Example 1: Logic 1 = 0 volts
Logic 0 = +10 volts

Example 2: Logic 1 = -10 volts
Logic 0 = 0 volts

In both examples the logic 1 state is always more negative than the logic 0 state, even though in example

1 both states are in the positive region. While the above definitions of logic polarity are particularly applicable for d-c switching circuits, they also apply to a-c circuits as well. For example, a negative pulse can be used to simulate a negative voltage, and a positive pulse can be used to simulate a positive voltage. Such complexity is unnecessary, however, since the absence of a pulse can be assumed to indicate the logic 0 state. Thus only a negative pulse is necessary, and the above definitions will still apply.

As normally used, negative logic is more adaptable to PNP type transistors because of the PNP polarity requirements. Since a negative collector voltage is required to reverse-bias the PNP transistor, operation of the transistor produces either a low or a high negative output voltage. By using direct coupling, a completely negatively polarized d-c system can be developed, and interstage coupling capacitors can be eliminated. Thus, besides the saving of the cost of a component, waveform distortion due to phase shift through the coupling capacitor can be minimized. Operation may also be speeded up, since it is no longer necessary to wait for the charge and discharge of the capacitor. Direct-coupled transistor logic (DCTL) circuits are discussed later in this section. Negative logic is not limited to PNP transistors, since the common emitter configuration (in an a-c coupled circuit) can invert the polarity of the input signal and provide a negative output from an NPN transistor. The use of PNP transistors merely makes the design of d-c negative logic circuits easier and simpler, so that negative logic is normally associated with PNP transistors, while positive logic is associated with NPN transistors. Since logic circuits and components are available for all types of polarity, there is no particular reason why negative logic should be used in preference to positive logic. In fact, for design reasons some special computers use both (mixed) positive and negative polarity. The usual practice is to design the logic without regard to polarity or levels. Once designed, the proper type of polarity and levels for the standard logic circuit and components to be used is selected, and the unit is constructed.

FAILURE ANALYSIS.

Since negative logic polarity involves the operation of circuits by means of a more negative voltage or signal, it can be reasoned that under normal operation the logic circuit must be activated by a negative signal and that the output must also be negative. However, since special design considerations sometimes negate this reasoning, it is necessary to refer to the schematic and flow diagrams to determine the actual polarity and levels which activate the suspected circuit.

DIODE LOGIC.

Diode logic (DL) concerns basic logic circuits utilizing the diode as the operating element. Functionally, logic circuits are broken down into simple basic circuits such as the OR gate, and the AND gate, which have their counterparts for each type of logic. Thus transistor logic also has its OR gate and AND gate, plus additional circuits such as the NOR gate and NAND gate. Combinations of these basic circuit building blocks, in turn, form additional but more complex configurations. For example, a combination of AND and OR circuits forms a **half-adder**, and two half-adders form a **full-adder or adder**. Thus the logic blocks are arranged to perform the desired circuit functions of the final computer design. In addition to diode and transistor logic, other forms of logic utilizing diodes or transistors are encountered. For example, where only d-c is involved, direct-coupled transistor logic (DCTL) is usually employed to avoid losses in coupling circuits. Where a-c pulses are employed resistor-transistor logic circuits (RTL) or resistance-capacitance transistor logic (RCTL) are usually used (this is similar to the resistance coupling used in audio amplifiers). Therefore, each basic logic group has its simple basic OR and AND circuits, plus any other circuits peculiar to that type of logic. In most cases, the more involved circuits are made up of combinations of OR, AND, and NOT circuits. While the operation of these basic circuits may be slightly different, they are similar: For example, transistor logic can easily be visualized by considering the emitter-base junction as an input diode and base-collector junction as the output diode.

Diode logic is the simplest type of logic, corresponding, in general, to switch operation. Either the switch is ON (diode conducting) or it is OFF (diode non-conducting). It is usually used where signals of only two levels are involved (the off level and the on level) although three-level circuits may be arranged, if desired. Either negative or positive logic may be used with the same circuit arrangements, except that the diode connections must be reversed. While it is important that the forward resistance of the diode be low, it is more important that the reverse resistance be very high. Thus when diodes are parallel-connected their parallel reverse-resistance is still high, and leakage and operating power requirements are low, also, false triggering will not occur. Another advantage to the use of diode logic is that no inversion of the output signal occurs. Thus it is unnecessary to add an inverter circuit to return the signal to its original polarity; this helps simplify computer design.

The diode also lends itself to multiple arrangements where a combination of inputs is used to produce a single output, usually called a **decoding matrix** or matrix. Conversely, an arrangement with single inputs producing a multiple output is known as an **encoder matrix** or matrix. In general, when arranged in a rectangular arrangement the matrix becomes a **rectangular matrix**, regardless of function, that is, it may be either an encoder or decoder. Each of these basic circuits and arrangements are fully discussed in the following paragraphs.

OR GATE.

APPLICATION.

The diode OR gate is a basic logic circuit which produces an output when either input is activated, and when both inputs are simultaneously activated (inclusive OR). It replaces the relays and electron tubes used in earlier computers.

CHARACTERISTICS.

May use either positive or negative logic.

May be operated by short duration pulses, or by static d-c voltage levels representing inputs and outputs.

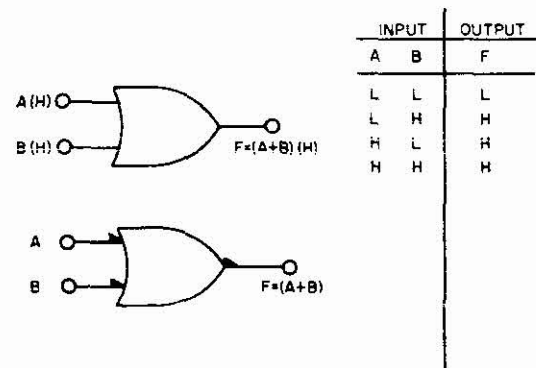
Represents logic addition ($1+0=1$).

Corresponds to an oppositely polarized AND gate.

Output never exceeds the input (no amplification is obtained.)

CIRCUIT ANALYSIS.

General. Logic circuits differ from basic electronic circuits in their general treatment. Through the use of standard logic symbols (see MIL STD 00806C (NAVY) for a complete list), a block-diagram type of presentation may be used, instead of the conventional schematic representation with which the ET is more familiar. Thus the signal path and operation can be followed, or considered, without regard to the actual electronic circuit operation. Typical standard symbols used to represent a **positive** logic OR circuit are shown below, accompanied by a truth table of possible combinations.

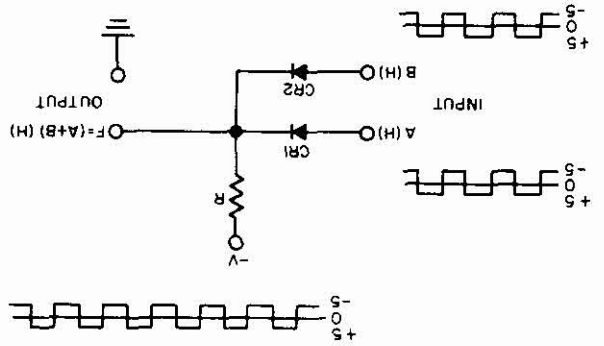


Positive OR Gate Symbols Table of Combinations

The (H) notation means high level or positive logic and in the lower symbol this is indicated by the filled-in (or solid) right triangles. The inputs are A or B. The output, F shows in Boolean algebra notation the result $(A + B)$, where the + sign indicates OR (addition). The table of combinations shows every possible combination of input and output and is therefore, called a truth table. When either input A or input B (or both) are at a relatively high level, the output, F, is also at a relatively high level. When both A and B are at a low level, so is output F.

When the OR gate is inactive (no inputs) it is forward biased by the large negative voltage applied to the cathode, and usually a small negative voltage, representing 0, is applied to the anode and a small current flows through either CR1 or CR2. Actually, a reverse current may also flow depending upon the reverse leakage of the diode, this current, however, is so small in most cases that it may be neglected. Thus with sufficient diode current flow through R to drop the bias supply to zero, no output is produced at F. When an input is applied to either A or B, more current flows through R and depending upon the amount of voltage applied, and its polarity, if a voltage of exactly -V is applied, both sides of the

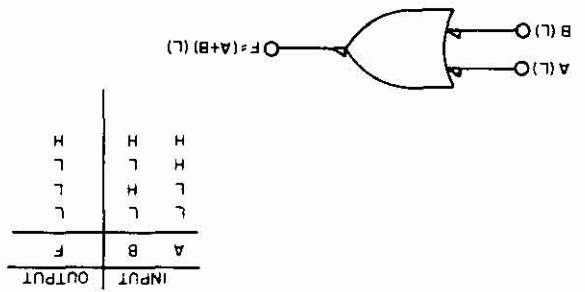
Two Input Positive OR Gate



The (L) notation means low level or negative logic, and the small open right triangle at the inputs and outputs on the symbol indicates they are low (if filled-in they are high). When the triangles are used the parenthetical (L) notation may be omitted. The table of combinations shows that for all inputs but one, the output is low. When both inputs are high, then the output is also high.

Circuit Operation. A two-input positive OR gate is shown in the accompanying illustration. The gate consists of two diodes, CR1 and CR2, and current limiting resistor, R, connected as shown in the schematic.

Negative OR Gate Symbol Table of Combinations



When negative logic is used, the symbol shown below and truth table apply.

The positive OR circuit is sometimes referred to as a negative AND circuit, because if the polarity of the input trigger is reversed so that a negative signal represents a 1 and a positive signal a zero, a combined input will produce a negative output, but separate inputs will not. Because of the interchangeability of the OR and AND functions with polarity, it is necessary to adopt certain conventions to avoid confusion. Therefore, if we assume that relatively positive signals produce a 1, and relatively negative signals produce a 0, we may call the OR circuit previously discussed above a **positive OR gate**. Unless otherwise noted, we shall assume this convention throughout the remainder of the circuit discussions in this Chapter of the Handbook.

A two input **negative OR gate** is shown in the accompanying illustration. The gate consists of two diodes, CR1 and CR2, with current limiting resistor, R, connected as shown in the schematic.

The positive OR circuit is sometimes referred to as a negative AND circuit, because if the polarity of the input trigger is reversed so that a negative signal represents a 1 and a positive signal a zero, a combined input will produce a negative output, but separate inputs will not. Because of the interchangeability of the OR and AND functions with polarity, it is necessary to adopt certain conventions to avoid confusion. Therefore, if we assume that relatively positive signals produce a 1, and relatively negative signals produce a 0, we may call the OR circuit previously discussed above a **positive OR gate**. Unless otherwise noted, we shall assume this convention throughout the remainder of the circuit discussions in this Chapter of the Handbook.

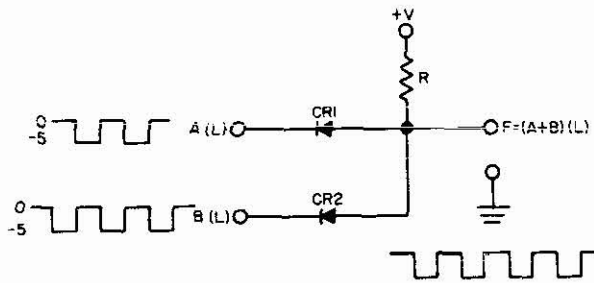
A two input **negative OR gate** is shown in the accompanying illustration. The gate consists of two diodes, CR1 and CR2, with current limiting resistor, R, connected as shown in the schematic.

When both diodes are activated simultaneously, the output will be the highest voltage applied to CR1 or CR2. Since in every case a positive input signal is required to produce an output, positive logic is used. The output pulse will conform to the duration of the trigger pulse and be of approximately the same shape. Because the input pulse appears as a reverse bias of this value is applied to the output pulse, a reverse bias, when signals are applied to inputs A and B, simultaneously, the larger amplitude signal determines which diode shall conduct. For exactly equal amplitude signals, both diodes will conduct. The difference between logic circuits and conventional electronic circuits is that in the logic circuit, distortion which would be intolerable in the communications circuit is acceptable. Thus it is only necessary for the logic circuit to provide a signal of sufficient amplitude and of the proper phase (or polarity) for actuating the next logic circuit.

The positive OR circuit is sometimes referred to as a negative AND circuit, because if the polarity of the input trigger is reversed so that a negative signal represents a 1 and a positive signal a zero, a combined input will produce a negative output, but separate inputs will not. Because of the interchangeability of the OR and AND functions with polarity, it is necessary to adopt certain conventions to avoid confusion. Therefore, if we assume that relatively positive signals produce a 1, and relatively negative signals produce a 0, we may call the OR circuit previously discussed above a **positive OR gate**. Unless otherwise noted, we shall assume this convention throughout the remainder of the circuit discussions in this Chapter of the Handbook.

A two input **negative OR gate** is shown in the accompanying illustration. The gate consists of two diodes, CR1 and CR2, with current limiting resistor, R, connected as shown in the schematic.

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Two Input Negative OR Gate

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The **negative** OR gate operates inversely to the positive OR gate. Thus, when inactive, it is held so by inputs approximately equal to +V and no conduction occurs. This represents the 0 state. When a negative 1 is applied either A or B, the respective diode is forward biased and current flows through R. Electron flow is in such a direction that the output end of resistor R is negative, and the input signal appears as the output. While one diode is conducting, the other diode is reverse biased by the amount of the output signal; thus it cannot conduct unless a greater negative voltage is applied its input. When both inputs are simultaneously activated with a negative signal, it equal in amplitude both diodes conduct. This is the case of the inclusive OR. If the polarities of the 0 and 1 are reversed, the negative OR gate will function as a positive AND gate. Thus the proper conventions must be used to produce the desired function. When the 1 input is relatively more negative than the 0 input, the above discussion, the symbol, the schematic, and the truth table for the **negative** OR gate apply.

FAILURE ANALYSIS.

General. In the basic OR circuit only three parts are involved and it is a simple matter to make a resistance and continuity check with an ohmmeter to quickly determine if the parts are defective. Military computers are usually made self indicating—that is, for a given module, normal operation is shown by a lamp operating in synchronism with the input or by a test signal inserted at specific intervals. Thus the operator can quickly determine if the module is working properly and substitute a new one when needed. In some instances it may be considered economical to throw away the module, in other instances, local or factory repair is made and the following trouble analysis will be applicable.

No Output. If no output is obtained from either the positive or negative OR gate when an input voltage or pulse is applied to either A or B terminal, the associated diode is defective. Use an ohmmeter to check the forward and reverse resistance of either CR1 or CR2. A high reverse resistance and a low forward resistance are normal. If the resistance is the same in both directions replace the diode with a known good diode.

Continuous Output. When a diode is short-circuited, the 0 level will appear continuously at the output. That is a constant d-c level will appear at the output, because a d-c current path exists from the supply through resistor R, through the diode, and through the input impedance or voltage supply impedance to ground. Thus the output will be a constant and oppositely polarized voltage to that normally produced. The output amplitude will be either higher or lower than normal depending upon voltage divider action of R and the input resistance. When the input portion presents a high resistance the output will be near the supply voltage. If equal to the value of resistor R, the output will be half the supply voltage. If lower than R the output voltage will also be low.

Erratic Operation or Reduced Output. If resistor R is open, no forward bias will be applied to the diodes and they will be in a floating condition, subject to operation by random noise pulses, or any signal that makes the anode more positive than the cathode (or the cathode more negative than the anode). Make a resistance check of resistor, R, with an ohmmeter when erratic operation occurs, and replace it if it reads outside the tolerance range.

AND GATE.

APPLICATION.

The diode AND gate is a basic logic circuit which produces an output only if all of its inputs are simultaneously activated. It represents the basic logic circuit for binary multiplication, and the dot symbol is used to indicate this ($A \cdot B = C$). It replaces the relays and electron tubes used in earlier computers.

CHARACTERISTICS.

- May use either positive or negative logic.
- May be operated by short duration pulses, or by static d-c voltage levels representing inputs and outputs.
- Corresponds to an oppositely polarized OR gate.
- Output never exceeds the input (no amplification is obtained).

CIRCUIT ANALYSIS.

General. Logic circuits differ from basic electronic circuits in their general treatment. Through the use of standard logic symbols (see MIL STD 883C (NAVY) for a complete list), a block diagram type of presentation may be used, instead of the conventional schematic circuit representation with which the ET is more familiar. Thus the signal path or operation may be followed, or considered without regard to the actual electronic circuit operation. A typical standard symbol used to represent a positive logic AND circuit is shown below, accompanied by a truth table of possible combinations.

INPUT		OUTPUT
A	B	F
L	L	L
L	H	L
H	L	L
H	H	H

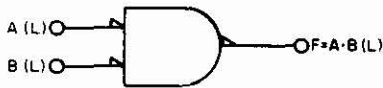


Positive AND Gate Symbol Table of Combinations

The (H) notation means high level or positive logic and is indicated in the symbol by the filled-in right triangle (when the triangles are used the parenthetical notation may be omitted). The inputs are A and B. The output, F, shows in Boolean algebra notation the result ($A \cdot B$), where the dot sign indicates AND (multiplication). The table of combinations shows every possible combination of input and output, and is, therefore, called a truth table. When inputs A and B are both at a relatively high level, the output, F, is also at a relatively high level. When both A and B are at a low level, so is F. For a single input the gate remains inactive.

When negative logic is used, the symbol shown below and accompanying truth table apply.

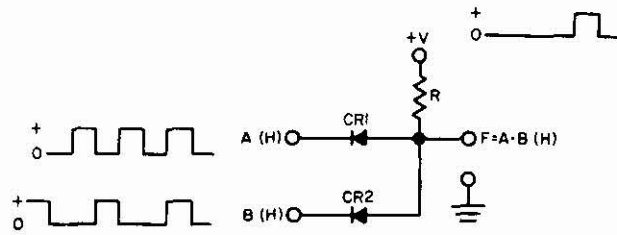
INPUT		OUTPUT
A	B	F
L	L	L
L	H	H
H	L	H
H	H	H



Negative AND Gate Symbol Table of Combinations

The (L) notation means low level or negative logic, and the small open right triangle at the inputs and outputs of the symbol indicates they are low (if filled in they are high). When the triangles are used, the parenthetical (L) notation may be omitted. The table of combinations shows that for all inputs but one, the output is high. When both inputs are low, the output also is low. For a single input the gate remains inactive and rests in the high state.

Circuit Operation. A two-input positive AND gate is shown in the accompanying illustration. The gate consists of two diodes, CR1 and CR2, and current limiting resistor, R, connected as shown in the schematic.



Two-Input Positive AND Gate

When the gate is inactive (no output is applied) the cathodes of CR1 and CR2 are at a relatively low level with respect to their anode. Thus the cathodes are effectively negative with respect to the anode and the diodes conduct. The diode current flowing through resistor R produces a voltage drop equal to that of the supply and of opposite polarity. Therefore, at the output end of R the potential is zero, and no output signal exists between F and ground.

Should a positive input be applied to either A or B alone, either CR1 or CR2 will cease conducting. However, the other diode will then conduct more heavily and keep output F at zero. Thus if only one input is activated there will be no output. On the other hand, if both A and B inputs are activated simultaneously by a high level or positive signal, the cathodes become more positive than the anodes and both diodes cease conducting. When conduction ceases, the voltage drop across resistor R no longer exists, and output F rises to the full value of the supply voltage (becomes highly positive). Thus a positive output is produced when both inputs are simultaneously activated by a relatively high level input representing a 1.

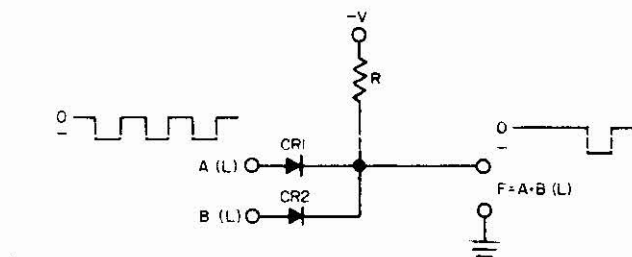
A positive AND gate is sometimes referred to as a negative OR gate, because if the polarity of the input trigger is reversed so that a negative signal represents a 1, and a positive signal represents a zero, a single input will produce a negative output, but combined inputs will not. Refer to the OR gate schematic in the previous discussion earlier in this Chapter and observe they are identical. Because of the interchangeability of the AND and OR functions with polarity it is necessary to adopt certain conventions to avoid confusion. Therefore, if we assume that relatively positive signals produce a 1, and relatively negative signals a 0, we may call the AND circuit discussed previously above a **positive AND gate**. Unless otherwise noted, we shall assume this convention throughout the remainder of the circuit discussions in this Chapter of the Handbook.

In some systems, 0's and 1's are represented by the absence or presence of a pulse. If the pulse is absent it represents a 0, if present, a 1. The AND gate must produce a pulse at its output only when all inputs are activated. Thus in a three input AND gate, inputs A, B, and C must all be activated before an output can be produced. Likewise, where both d-c and pulse levels are used, all must be activated. Where two levels are d-c and the third is a pulse, both d-c levels must be positive and a positive pulse must

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appear at the third level before the circuit will operate. Absence of the pulse would be a 0 exactly as though a negative signal were applied instead, and the circuit would not operate.

A two input **negative AND gate** is shown in the accompanying illustration. The gate consists of two diodes, CR1 and CR2, with current limiting resistor, R, connected as shown in the schematic.



Two Input Negative AND Gate

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The negative AND gate operates inversely to the positive AND gate. Thus, when inactive, the anodes are at a relatively high level (positive) with respect to the cathodes, which are connected to the negative supply through R, and they conduct. The voltage drop across R is opposite the supply and equal so that no voltage exists at the output end of resistor R, thus no output is obtained from F. When either input A or B is activated (with a negative 1 signal) the associated diode stops conduction, but the other diode maintains the output at zero. However, when both inputs are simultaneously activated by a low level or relatively negative input the anodes become more negative than the cathode and the diodes cease conduction. Since no current now flows through R, the voltage at the output terminal rises to the value of the supply voltage, and a negative output representing a 1 is produced. When the inputs cease, the output again terminates and the gate is considered inactive, even though this is the period during which the diodes are active and conducting.

If the polarities of the 0 and 1 are reversed, the negative AND gate will function as a positive OR gate (see schematic in previous OR gate discussion in this section of the Handbook). Thus the proper conventions must be used to produce the desired function. When the 1 input is relatively more negative than the 0 input, the above discussion, the symbol, the schematic and the truth table for the **negative AND gate** apply.

FAILURE ANALYSIS.

General. Since only three parts are used in the basic AND gate, it is a simple matter to make resistance and continuity checks with an ohmmeter to determine if these parts are defective. Military computers are usually self-indicating—that is, for a given module, normal operation is shown by a lamp operating in synchronism with the input,

or by a test signal inserted at specific intervals. Thus the operator can determine if the module is working properly and substitute a new one when needed. In some instances it may be considered economical to throw away the defective module, in other instances, local or factory repair is made and the following trouble analysis will be applicable.

No Output. If no output is obtained from either the positive or negative AND gate when an input voltage or pulse of the proper polarity and amplitude is applied simultaneously to both inputs A and B, both diodes are defective or resistor R is open. Use an ohmmeter to check the forward and reverse resistances of CR1 and CR2. A high reverse resistance and a low forward resistance are normal. If the resistance is the same in both directions replace the diode with a known good one. If resistor R is outside its tolerance range, replace it.

Continuous Output. If either the positive or negative AND gate produces an output with no input applied, both diodes are defective, or resistor R is shorted. Check the diodes with an ohmmeter for forward and reverse resistance, and the value of R. Replace the defective parts.

Erratic Operation. If an output is obtained when only one input is activated, the diode associated with the other input is open. Check the diodes for forward and reverse resistance with an ohmmeter, and replace the defective diode. If an output is obtained when either A or B are activated individually or simultaneously, resistor R is probably open and the diodes are free floating, subject to operation by any trigger or noise signal which makes the anodes more positive than the cathode, (or the cathodes more negative than the anodes). A resistance check of R will reveal the trouble.

RECTANGULAR MATRICES.

APPLICATION.

A rectangular diode matrix (matrix) is used in computers to perform a specific function, such as supplying a single output when supplied with multi-inputs or vice versa. It may also be known by its functional name instead. Thus, although arranged as a rectangular array it may be known as an encoding or decoding matrix. Actually it is a generic name for a class of circuits which are also named for the function they represent.

CHARACTERISTICS.

May use positive or negative logic.

Consists of an orderly rectangular array of diodes.

When many inputs are supplied only one or a very few outputs are produced, and vice versa.

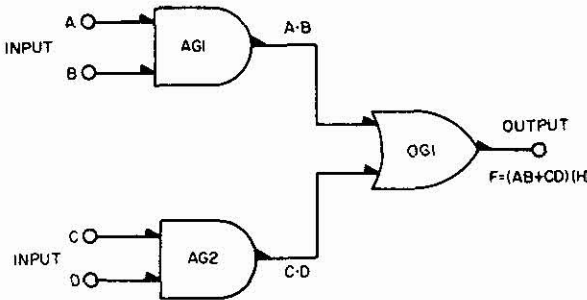
Gain is less than 1 (no amplification is provided).

CIRCUIT ANALYSIS.

General. Rectangular diode matrices have no special characteristics or functions of their own other than an ordered array of diodes. The matrix arrangement does not make it a logic circuit. It is the manner in which the matrix

elements are connected that determines the logic function produced. Thus to describe a computer as containing a rectangular matrice is of no significance unless the associated function is also described.

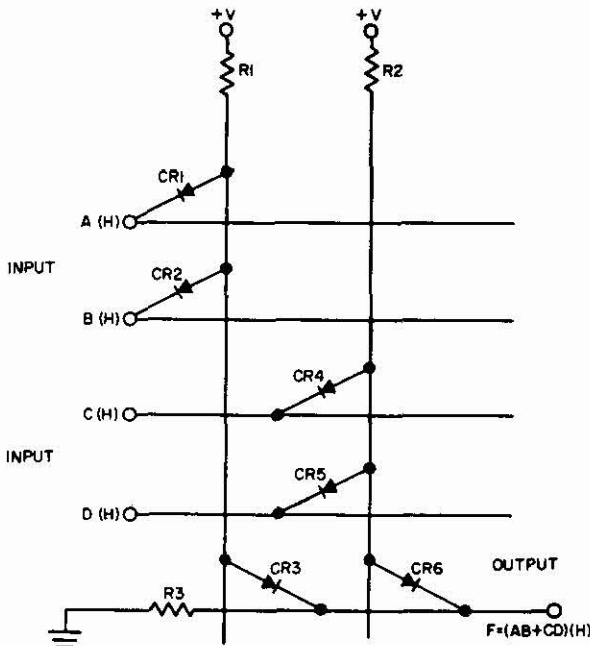
Circuit Operation. A simple rectangular matrice composed of two AND gates and one OR gate, which perform the logic function $(AB + CD)$ are first shown symbolically, then as a matrix diagram, and finally, in schematic diagram form.



Logic Diagram of Matrice

As shown in the logic diagram, the diode AND gates are AG1 and AG2, and the diode OR gate is OG1. Inputs A and B are provided for AG1, and C and D for AG2; the output of both circuits is combined by the OR gate at F. Thus output F is active whenever AG1 output ($A \cdot B$) is active, or when AG2 output ($C \cdot D$) is active, or when both AG1 and AG2 are active. The output function is written symbolically as $AB+CD$, which is read as A and B, or C and D, or both A AND B and C AND D. The last mentioned condition is the inclusive OR function.

The diode matrix representation of the function, $F = AB + CD$ is shown in the following illustration. AND gate AG1 consists of diodes CR1 and CR2, with current limiting



Matrix Representation

resistor R1. AND gate AG2 consists of diodes CR4 and CR5, with current limiting resistor R2. OR gate OG1 consists of diodes CR3 and CR6, with current limiting resistor R3. In the drawing, zero volts represents a logic 0 and +V volts represents a logic 1, thus positive logic is used, and output F is active (logic 1) when it is at +V volts relative to ground. It is inactive (logic 0) when it is at zero volts relative to ground.

Assume that all inputs (A,B,C, and D) are at zero volts (logic 0). With the anodes of CR1, CR2, and CR4, CR5 connected to the positive bias supply through R1 and R2, respectively, the diodes are forward biased and conduct. The supply voltage is dropped across resistors R1 and R2 so that the anodes of OR gate diodes CR3 and CR6 are also at approximately zero volts. Because the cathodes of the OR gate diodes connect to ground via R3, there is no difference in potential across these diodes and no conduction occurs. Thus, the output of the OR gate remains at zero volts (a logic 0). The conditions stated above are shown on line 1 of the table of combinations shown below, that is, all inputs and the output are at a low level (L).

LINE NO	INPUT				OUTPUT
	A	B	C	D	$F = (AB+CD)(H)$
1	L	L	L	L	L
2	L	L	L	H	L
3	L	L	H	L	L
4	L	L	H	H	H
5	L	H	L	L	L
6	L	H	L	H	L
7	L	H	H	L	L
8	L	H	H	H	H
9	H	L	L	L	L
10	H	L	L	H	L
11	H	L	H	L	L
12	H	L	H	H	H
* 13	H	H	L	L	H
14	H	H	L	H	H
15	H	H	H	L	H
16	H	H	H	H	H

Table of Combinations

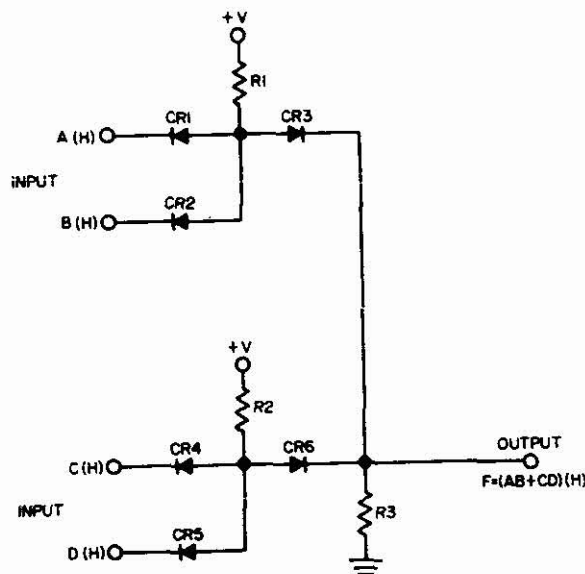
Assume now that the condition on line 13 is true. That is, inputs A and B are active at +V volts (relatively high), and inputs C and D are inactive at zero volts (relatively low). With inputs A and B both at +V volts, diodes CR1 and CR2 are held in the non-conducting state (reverse biased), while CR3 anode is positive with respect to ground and conducts, current flow is from ground through R3, diode CR3, and R1 to the supply. Thus, output F is equal to the supply voltage minus the drop across R1, and the small drop through the diode, or approximately +V volts, a logic 1. Meanwhile, inputs C and D are inactive at zero volts, and diodes CR4 and CR5 conduct because of the high positive anode potential. The current flow through R2 drops the supply voltage to zero, with respect to ground, at the

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anode of diode CR6 (the OR gate). With the cathode of CR6 connected to ground through R3, no potential exists across the diode, it is reverse biased by the positive output voltage across R3, therefore CR6 does not conduct.

Assume now, that conditions are reversed, that is, inputs C and D are activated by a positive voltage, and inputs A and B are inactive at zero volts, this is combination number 4 in the table above. OR gate diode CR6 now conducts, while CR3 remains nonconducting, and the output at F is again at +V volts, and produces a logic 1 while in this active state. It is evident from the table of combinations, above, that if each of the input combinations is performed, only combinations number 4, 8, 12, 13, 14, 15, and 16 will cause an active (high) output to be produced at F.

The schematic representation of the circuit described above is shown in the accompanying illustration. While this drawing and the matrix representation are identical, the



Schematic Circuit

arrangement is slightly different. Thus the schematic representation shows the more familiar AND and OR gate arrangements at a glance. However, the matrix drawing is usually used for matrices because it essentially conforms to the physical and wiring arrangement of the matrix, and it is clearer and easier to follow signal path flow when a large number of cascaded circuits are used. Both circuits are identical, however, so you may use whichever seems easier to follow or understand. The circuit explanation is applicable to both drawings. To fully understand operation of this circuit, you should apply each input condition shown in the table of combinations and verify that an identical result is obtained. Once established, the truth table makes it necessary to know how the circuit operates in determining a particular result. If the inputs are known, then the output can be determined at a glance.

FAILURE ANALYSIS.

General. The simple rectangular matrix discussed above only contains three times as many parts as the basic AND or OR circuits, so that a resistance and continuity check with an ohmmeter will quickly determine if the parts are defective. Usually in Military computers, the module is made self indicating so the operator can determine quickly if the entire module is working and replace it when necessary. The defective module is then repaired either at a local activity or at the factory, or is discarded if it is considered economically feasible. In large computer repair centers test jigs are usually available, and the module is inserted in the jig and simulated test signals are applied to the inputs, and the outputs or lack of outputs are noted. Thus the defective part and circuit is quickly located. For small computers, when authorized, a similar procedure may be followed. The computer can be used to supply the necessary inputs, and the outputs can be observed on either a voltmeter, a VTVM, or an oscilloscope. Lack of output when the proper trigger is applied, or a continuous output with no trigger applied will usually isolate the trouble to the circuit and part at fault.

No Output. With a trigger applied to either diode CR3, or CR6, if no output is obtained, the associated diode is probably open. Check the forward and reverse resistance with an ohmmeter, if it indicates the same resistance in both directions and is a high value the diode is open. If no output is obtained with an input to both A and B, or C and D, diodes CR1 and CR2, or CR4 and CR5, respectively, are open, or either R1 or R2 is open. A resistance check will determine which is at fault.

If both AND gate diodes are shorted, the associated AND gate will not operate, but the matrix can be operated by the other AND gate. However, if both AND gates are inoperative no output will be obtained from the matrix, and all diodes must be defective. If R3 is shorted, no output will be obtained; check R3 with an ohmmeter.

Continuous Output. If a continuous output is obtained and remains unaffected by any input trigger combination, either diode CR3, or CR6 is shorted. Checking the reverse resistance of either diode will indicate which one is defective (if low, the diode under test is defective; if high the other diode is defective).

If both AND gate diodes are open, their associated OR gate will be triggered and a continuous output will occur. A reverse resistance check will reveal this condition. Similarly, if R1 or R2 are shorted, their associated OR gate diodes CR3 or CR6 will conduct continuously, and produce a larger than normal output across R3. A resistance check of the resistors with an ohmmeter will determine the defective part.

ENCODING MATRICES.

APPLICATION.

Encoding matrices (matrix) are used to change data from one form into another. For example, the conversion

of conventional decimal or english notation into a form usable in a digital computer. The decimal numbers, letters, and punctuation marks are converted to binary form for use in the digital computer.

CHARACTERISTICS.

Consists of many input lines, but only a few output lines.

Only one input line is activated at a time to produce a unique output.

May use positive or negative logic, or combined logic. Gain is less than 1 (no amplification is provided).

The matrix may be arranged in any suitable geometric form (rectangular, square, pyramid etc.).

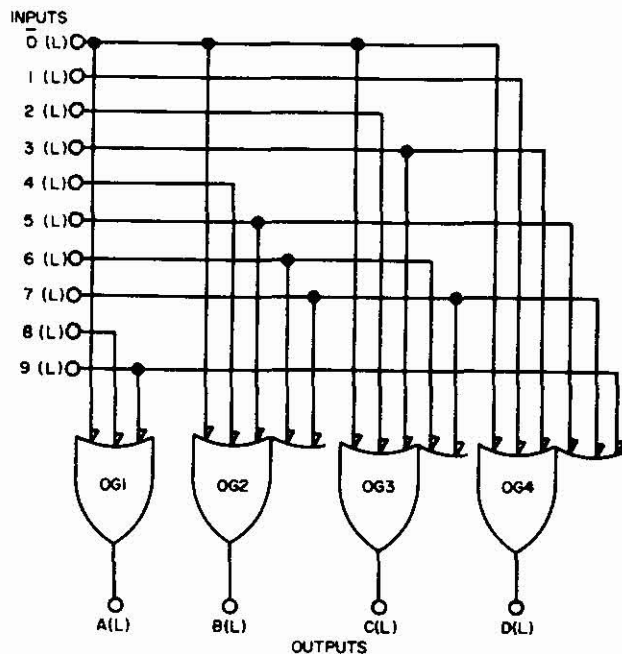
CIRCUIT ANALYSIS.

General. A decimal-to-binary encoder matrix changes a voltage level which represents a specific decimal number into a unique set of voltage levels representing the binary form of the decimal number. The following table shows decimal numbers from 0 through 9 with their binary equivalents.

DECIMAL NUMBER	BINARY NUMBER
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1

Note that the decimal digit requires four binary digits (or bits) to represent it. Therefore, the circuit which performs the decimal to binary encoding must have 10 input lines, one for each decimal digit input, and 4 output lines, one for each binary output.

Circuit Operation. The logic diagram for a typical decimal-to-binary encoder is shown in the accompanying illustration.



Decimal to Binary Encoder Logic Diagram

Examination of the logic diagram reveals that four OR gates are employed. OR gate number 1 has three inputs and one output. OR gates numbers 2 and 3 have five inputs and one output, and OR gate number 4 has six inputs with one output. The open triangles indicate that negative logic is used. Therefore, a logic 0 (inactive state) is represented by a relatively high voltage level (H), while logic 1 (the active state) is represented by a relatively low voltage level (L).

The following table of combinations shows the specific decimal number input and level, and the unique output level for each of the inputs.

INPUT	OUTPUT			
	A	B	C	D
0	L	L	L	L
1	H	H	H	L
2	H	H	L	H
3	H	H	L	L
4	H	L	H	H
5	H	L	H	L
6	H	L	L	H
7	H	L	L	L
8	L	H	H	H
9	L	H	H	L

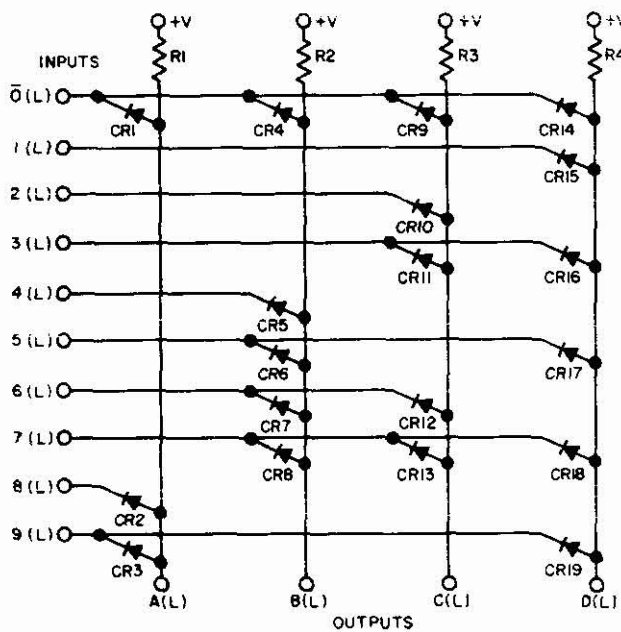
Table of Combinations (Truth Table)

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Examination of the table of combinations reveals that the listed gate output is activated when the input is the decimal number(s) shown in the following matrix truth table; note that the number of inputs correspond to those shown on the logic diagram.

A = 0, 8, 9
 B = 0, 4, 5, 6, 7
 C = 0, 2, 3, 6, 7
 D = 0, 1, 3, 5, 7, 9

The following illustration shows the complete matrix schematic representation of the encoder.



Matrix Representation

Examination of the matrix schematic reveals that OR gate number 1 (output A) consists of diodes CR1 through CR3, with current limiting resistor R1. OR gate number 2 (output B) consists of diodes CR4 through CR8, with current limiting resistor R2. OR gate number 3 (output C) consists of diodes CR9 through CR13, with current limiting resistor R3. And OR gate number 4 (output D) consists of diodes CR14 through CR19, with current limiting resistor R4. As shown in the schematic, the anodes of all diodes are connected to a positive bias supply through the current limiting resistors. When their cathodes are connected to a less positive voltage, or placed at zero (ground) potential they will conduct. When left unterminated (no input) the circuit from the supply through the diode to ground is open, and no conduction occurs. When

no conduction occurs, no current flows through the associated current limiting resistor and the gate output is +V, the supply voltage. Since negative logic is employed, a positive (relatively high) output represents a 0 and the circuit is then considered inactive. When a zero voltage (negative or relatively low) input is applied, all diodes on this line will conduct. The normally high (positive) output will be dropped to zero by the current flowing through the associated current limiting resistor, thus zero voltage or no output represents a 1, that is, an active negative output.

For example, assume the decimal number 7 is applied by grounding that input line (a relatively low (L) input is applied). The cathodes of diodes CR8, CR13, and CR18 are, therefore, more negative than their anodes, and these diodes will conduct. Thus at gate outputs B, C, and D, no voltage will appear, and these OR gates will all be at a relatively low (L) output. At the same time, since gate A output is not connected to line 7 it will remain highly positive at +V volts creating a relatively high (H) output. Thus by activating the number 7 line (through grounding it) the output will be HLLL, representing 0111 or the binary number 7. By following the table of combinations, number for number, in a similar fashion and applying each input in turn, the outputs shown in the table of combinations will be obtained. Only one decimal number input at a time is permitted, with all the remaining lines resting in the inactive state. If two or more input lines were simultaneously activated, one of the numbers might be produced correctly and the others masked out, or else the wrong number would be produced. Thus in an encoder of this type a series input must be used, since a parallel input would produce a false indication. Conversely, the decoder which works just the opposite, requires a parallel input. Thus the coding time for a series of decimal digits in a simple computer represents a finite time, since only one can be produced at a time. However, the operating time for each digit is only a few microseconds, so that the coding is usually accomplished as fast as the information can be inserted, and appears to be instantaneous.

While the above explanation assumes the use of d-c voltage levels, the same action can be obtained with pulses using appropriate coupling circuits, when needed. Because of the inherent loss in the diode, although assumed zero for ease of discussion in these paragraphs, when large numbers of diodes are used considerable power is required. Thus diode logic is usually used together with transistors, and diode-transistor logic (DTL) circuits are used in large computers.

FAILURE ANALYSIS.

General. In large matrices one has a choice of making a resistance check of the numerous components of the module, or applying an operational check using the truth table and a matrix schematic to analyze the outputs. In large computer repair shops this is accomplished quickly by prepared test jigs into which the module may be plugged. The trouble is thereby pin-pointed to a few associated com-

ponents which are then checked individually. The following paragraphs indicates a systematic method of analyzing failures for trouble localization.

Gate Output Always High. If a particular gate output always remains in the high state regardless of the inputs to the matrix, it can be assumed that all the diodes associated with that gate are probably open circuited, or the associated current limiting resistor is shorted. Make a forward resistance check of the diodes with an ohmmeter, if the resistance is the same in both directions and high, the diodes are open. Check the resistance of the resistor. With a shorted current limiting resistor, the heavy current through the diode will usually be sufficient to cause the diode to heat, smoke, and eventually burn out, or to blow the supply fuse.

Gates Outputs Always Low. If a particular gate output always remains in the low state, regardless of the inputs to the matrix, all of the diodes associated with that gate are probably short circuited, or the associated current limiting resistor is open. Make a reverse resistance check of the diodes with an ohmmeter, if they read the same in both directions and it is very low, the diodes are shorted. Check the resistor value.

Incorrect Output. By using the truth table and the proper input, each input line can be checked individually for proper operation. For example, if input line 0 (decimal zero) is active and low (L) and the outputs are: A high (H), B low (L), C low (L), and D low (L) it indicates that diode CR1 is open circuited. This is indicated by outputs B, C, and D being normal, and output A abnormal when compared with the proper outputs listed in the table of combinations. Note that while diodes CR2 and CR3 are also connected to output line A, they can only be activated when lines 8 or 9, respectively, are activated. Thus, since only one line may be active at a time only the diodes associated with that line need be considered. It is evident that if three diodes are concerned, and two outputs are wrong, two of the diodes must be at fault.

DECODING MATRICES.

APPLICATION.

Decoding matrices (matrix) are used to change data from machine (computer) language to ordinary decimal or english notation. The binary representation of a decimal or an english character (machine language) is automatically converted by the matrix into a straight-forward reading character or digit easily recognized by the reader.

CHARACTERISTICS.

Consists of many input lines, and many more output lines.

Several inputs are activated simultaneously to produce a unique output.

May use positive or negative logic, or combined logic.

Gain is less than 1 (no amplification is provided).

The matrix may be arranged in any suitable geometric form (rectangular, square etc.).

CIRCUIT ANALYSIS.

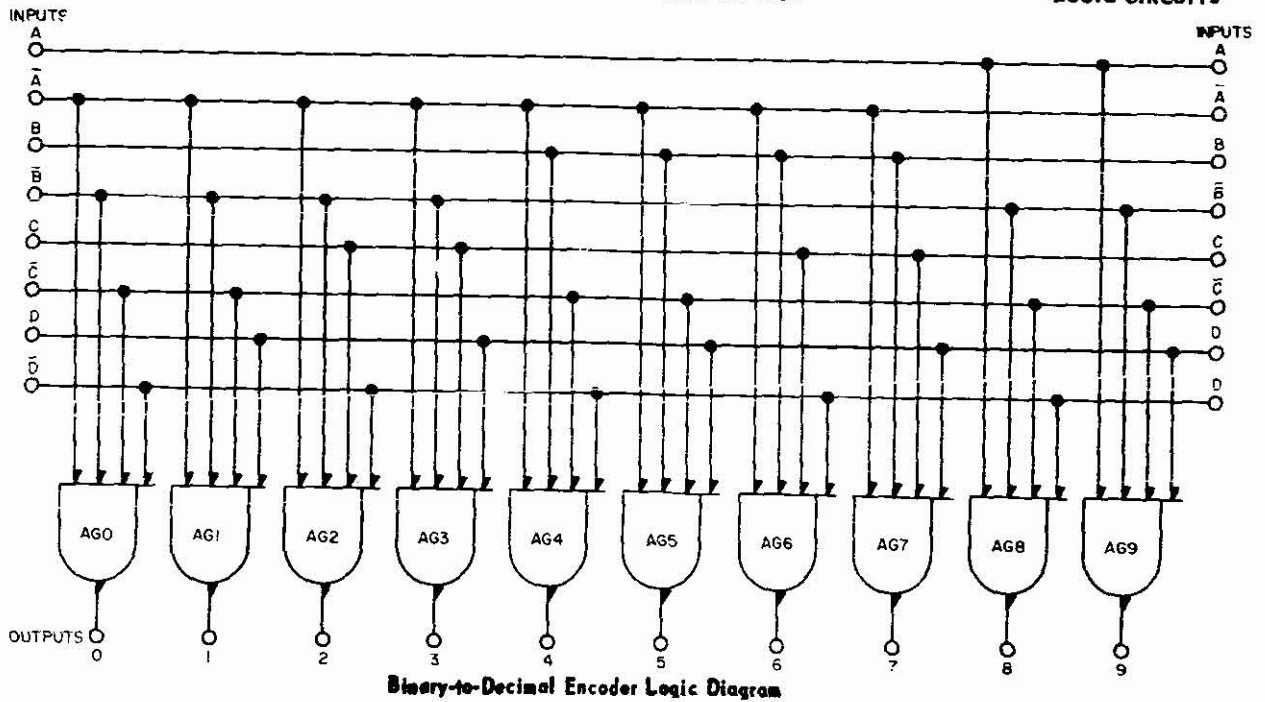
General. A binary-to-decimal decoder matrix changes a unique set of input voltage levels representing a binary number into an output which represents a single decimal number. The following table shows binary numbers from 0 through 9, with their decimal equivalents.

BINARY NUMBER	DECIMAL NUMBER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9

Note that each decimal digit requires four binary digits (bits) to represent it. Thus this type of decoder is sometimes called a "many-to-one" decoder, since many inputs are converted to a single output. To perform the binary decoding 8 inputs are required (four inputs for binary 1's and four inputs for their complement, binary 0), with 10 outputs representing the decimals from 0 through 9.

Circuit Operation. A logic diagram for a typical binary-to-decimal decoder is shown in the accompanying illustration.

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Examination of the logic diagram shows that 10-AND gates having 4-inputs and four diodes in each gate (AG0 through AG9) are used. The closed triangles indicate that positive logic is employed. Therefore, the inactive state (a logic 0) is represented by a relatively low voltage level (L), while the active state (a logic 1) is represented by a relatively high level (H).

The following table of combinations shows the various binary input levels and the unique output level for each of the possible input combinations.

BINARY INPUT				DECIMAL OUTPUT	
A	B	C	D	F	
L	L	L	L	H	(0)
L	L	L	H	H	(1)
L	L	H	L	H	(2)
L	L	H	H	H	(3)
L	H	L	L	H	(4)
L	H	L	H	H	(5)
L	H	H	L	H	(6)
L	H	H	H	H	(7)
* H	L	L	L	H	(8)
H	L	L	H	H	(9)

Table of Combinations

Examining the table of combinations, we find that if the binary inputs A, B, C, D are activated (H, L, L, L), gate AG8 is activated to produce a high (H) output, which indicates that the matrix has decoded a binary 8. While the gate that is activated for each binary input is shown by the table of combinations, if it is converted into a Truth Table by substituting the 0 and 1's corresponding to the decimal number as shown below, operation becomes easier to

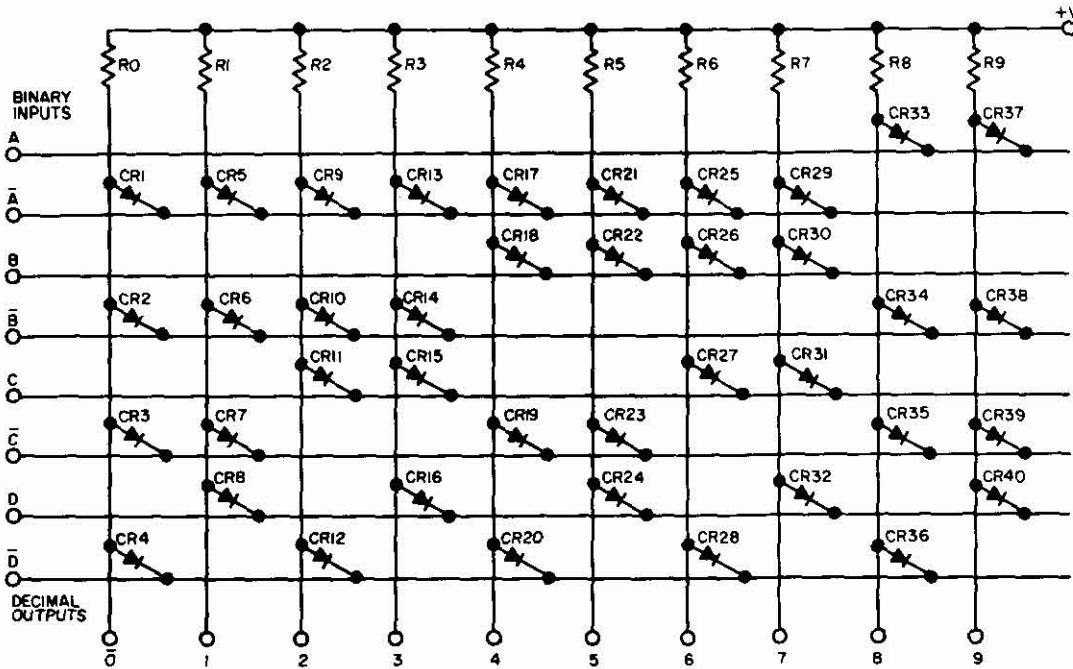
BINARY NUMBER				DECIMAL NUMBER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

follow. It is also evident that this is the same as the binary-decimal equivalent numbers previously listed. When the gates are activated it is by means of a logic 1 signal. In the logic zero state the gate remains inactivated. When the gate input is activated, the input signal stops the

associated gate diodes from conducting, and an output is produced as the output level rises to the +V supply voltage. When the gate input is inactivated, the cathode of the associated diode is at a lower potential than the anode and the diode conducts. The current flow through the associated current limiting resistor drops the supply voltage to zero so that no output is obtained. Thus when input A is activated a positive voltage is applied to block off or reverse

bias any diodes connected to that line. When \bar{A} (A-bar) is activated it is a "NOT A"; thus, it is not a logic 1 but a logic 0, and all the diodes associated with that line conduct because of the forward bias applied by the relatively-low (L) input signal.

This operation may be followed more easily if the accompanying matrix schematic is examined in conjunction with the truth table inputs as the discussion continues.



Decoder Matrix Schematic

For example, assume that inputs \bar{A} , B, \bar{C} , and D are active high (H), and are at +V volts. The truth table shows that the corresponding combination 0101 must activate gate number 5 and produce a high positive output. Examination of the matrix schematic shows that gate 5 consists of CR21 through CR24 with current limiting resistor R5. When input line \bar{A} is activated, made high (H), diode CR21 ceases conduction; likewise, as B, \bar{C} and D, respectively, are also made high the diodes CR22, CR23, and CR24 are also reverse biased. Thus all the diodes of AND gate 5 stop conduction simultaneously, and output F which is assigned the decimal number 5 rises to the supply voltage level creating a positive output pulse, as required by the table. Note that if any one of these inputs were not activated (H), but were low (L) instead, then that one diode would conduct and the high output could not occur. Thus one, and only one particular combination will activate each of the AND gates. To prove this, examine each of the input lines which are not activated and are at a relatively low value. We find, then, that line A forward biases diodes CR33 and CR37 and decimal outputs 8 and 9 are, therefore, at zero. Likewise, for input line \bar{B} diodes CR2, CR6, CR10, and

CR14 conduct and outputs $\bar{0}$, 1, 2, and 3 are low or zero. For line C diodes CR11, CR15, CR27, and CR31 conduct so that outputs 2, 3, 6, and 7 are zero. Finally, input \bar{D} inactive causes conduction of diodes CR4, CR12, CR20, CR28, and CR36, with outputs $\bar{0}$, 2, 4, 6, and 8 at zero. Thus, while gate 5 is high, all the other outputs are low or zero since at least one of the associated diodes is conducting. Sometimes two or more diodes will be conducting, but only one is necessary to prevent the gate from operating, and producing an output.

If you follow the truth table combinations, applying high and low inputs as indicated and noting the output, or lack of output, you will see that the truth table shows the proper combination for the desired output, and no other combination will produce the same results.

FAILURE ANALYSIS.

General. In large matrices one has a choice of making a resistance check of the numerous components of the module, or applying an operational check using the truth table and a matrix schematic to analyze the outputs. In large computer repair shops this is accomplished quickly by

prepared test jigs into which the module may be plugged. The tests are then run sequentially (using the proper input) until the wrong response is obtained. The trouble is thereby pin-pointed to a few associated components, which are then checked individually. The following paragraphs indicate a systematic method of analyzing failures for trouble localization.

Gate Output Always High. If a particular gate output always remains in the high state regardless of the inputs to the matrix, it can usually be assumed that all the diodes associated with that gate are probably open circuited, or the associated current limiting resistor is shorted. Make a forward and reverse resistance check of the diodes in that gate with an ohmmeter. If the resistance is the same in both directions and high, the diodes are open. Check the resistance of the current limiting resistor with an ohmmeter. Usually with a shorted current limiting resistor, the heavy current through the diodes will be sufficient to cause the diodes to heat, smoke, and eventually burn out, or to blow the supply fuse.

Gate Output Always Low. If a particular gate output always remains in the low state, regardless of the inputs to the matrix, one of the diodes associated with that gate is probably short circuited, or the associated current limiting resistor is open. Make a reverse resistance check of the diodes with an ohmmeter. If the resistance is the same in both directions, and it is very low, the diode is shorted. Check the resistor value with an ohmmeter.

Incorrect Output. By using the truth table and the proper input, each input line can be checked individually for proper operation. For example, if diode CR1 of gate AGO were open-circuited, AGO would become active whenever inputs \bar{B} , \bar{C} , and \bar{D} were high. The table of combinations shows that inputs \bar{B} , \bar{C} , and \bar{D} must be active to produce an output from gates AGO and AG8 under these conditions (\bar{A} input is not connected to AG8, and A input is not connected to AGO). Therefore, both AGO and AG8 would become active when the AG8 inputs are correct, and AGO would also become active when its inputs are correct. Thus the open circuited CR1 diode would not be detected unless it was noted that BOTH AGO and AG8 outputs were active when **only** the AG8 output should be active. It is evident, then, that the logical procedure is to apply the proper inputs separately, as listed in the table of combinations, while checking the output lines to be certain that only one gate (the correct gate) is activated for a particular input combination.

TWO-LEVEL AND-OR GATE

APPLICATION

Combinations of AND-OR gates which form a two-level logic circuit can be used to apply the outputs of two or more logic circuits to the input of another logic circuit to produce logic addition, subtraction and other functional operations.

CHARACTERISTICS.

May use positive or negative logic, or combined logic.

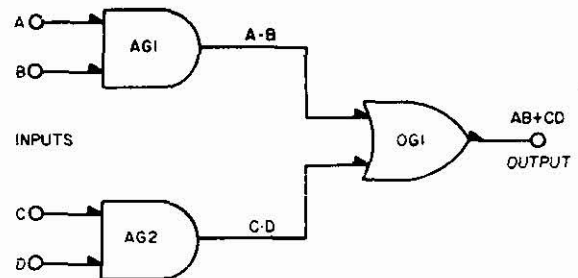
Has not less than four inputs for one output, and may have six or eight inputs with only one output, if desired.

The actual input levels may be different, however, the outputs are always at the same level.

Output never exceed the input (no amplification is obtained).

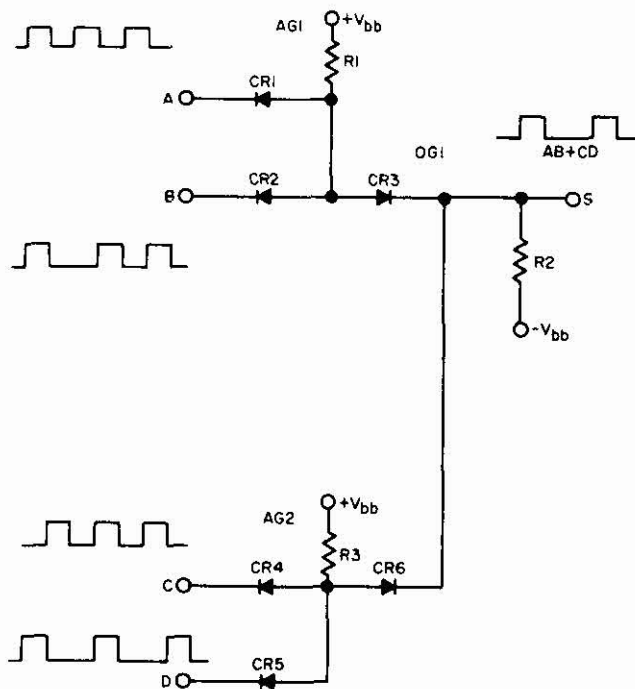
CIRCUIT ANALYSIS

General. Two-level logic circuits have two basic input circuits and a single output circuit. The input circuits may have a number of input lines, each controlled by a diode, but there is only one output line. Thus it is common practice to make the input circuits AND gates, and the output circuit an OR gate. Although this logic may be changed to exactly the opposite by applying negative logic inputs. Thus, the AND gates become OR gates, and the OR gate becomes an AND gate without changing any circuitry. This allows complete flexibility in combining logic operations, and, therefore, two-level logic circuits are universally used throughout computers. The logic diagram for a combination of two positive AND gates, and a positive OR gate is shown in the following illustration.



Two-Level Positive AND-OR Gate

Circuit Operation. The schematic for a typical two-level AND-OR gate is shown in the accompanying illustration. Although only two inputs are shown for each branch circuit for ease of discussion, a larger number of inputs may be accommodated.



Two-Level AND-OR Gate Schematic

It is evident from the schematic that AND gate number 1 (AG1) is identical to AG2. Two different inputs are applied to each AND gate. The output of the AND gates are applied through CR3 and CR6, and are summed across R2. A table of combinations shows that the following truth table is applicable, where 0 is ground or zero level, and 1 is a +5.

INPUTS				OUTPUT
A	B	C	D	S
0	0	0	0	0
0	1	0	1	0
1	0	1	0	0
1	1	1	1	1

Truth Table

Thus with no input applied, diodes CR1, CR2 and CR4, CR5 conduct since they are forward biased, and the voltage across R1 and R3 is dropped to zero. OR diodes CR3 and CR6 are also conducting (anode is more positive than cathode) so that this output is also zero. When either A or B, or C or D is made a 1 (by applying plus 5 volts) the associated diode is reverse-biased and stops conducting. However, circuit operation remains unaffected since the other diode of the pair still conducts and holds the gate

in the zero state. However, whenever both inputs are applied simultaneously to either AND gate, both diodes are reverse biased, conduction ceases, and the voltage at the bottom end of R1 or R3 is the same as the supply, if the reverse bias is equal to or greater than the supply. If the reverse bias is only a portion of the supply voltage, (as is the case) conduction above that level holds the output at the value of the reverse bias. Thus with a 10 volt supply and a 5-volt reverse bias, the output is +5 volts. This output of the AND gate when applied to the OR gate passes through either CR3 or CR6 and appears as the output sum (AB + CD). When +5 volts appears at the output the inactive OR diode is reverse-biased by that same amount, so that the other AND output has no effect. That is the exclusive OR function is represented, where either one or the other (AG1 or AG2) appears but not both. In this respect, the truth table appears erroneous. However, it is just the manner in which it is arranged. Thus this circuit is sometimes called a **one-quarter adder**, since it only represents the sum of two digits. When another AND gate is added to indicate the carry where both OR gate inputs are present simultaneously, the circuit then is known as a half-adder (discussed separately later in this section of the Handbook).

FAILURE ANALYSIS.

General. Since the two-level gate is composed of AND and OR circuits, the failure analysis for each of these circuits can be applied individually (see separate discussion of AND and OR circuits in this section of the Handbook) after it has been determined which is at fault. To determine which is at fault, proceed generally as follows.

No Output. Use a vacuum tube voltmeter or an oscilloscope as an indicator and apply a simulated "1" signal to input A, B, C, and D separately; no output should be observed at the OR input. However, if both A and B, or C and D inputs are activated and no output appears at the OR gate, the AND gate portion of the circuit is defective. Check the diodes for a short circuit or resistor R1 or R3 with an ohmmeter. If no outputs occurs from the OR gate portion, with an input appearing on the anode of CR3 or CR6, either the diode or R2 is open. Make a check of forward diode resistance and check the resistor with an ohmmeter.

Wrong Output. Usually with a wrong output, it will be found that the diode associated with that circuit is either inoperative or shorted. A forward and reverse resistance check of the diodes with an ohmmeter will usually locate this form of failure.

Continuous output. Usually in the case of a continuous output you will find that the diode associated with that output is shorted. The key to determining which is at fault is to study the circuit

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operation. If the circuit requires that the diode conduct to produce the desired output, then the diode is shorted. If the diode must cease conduction, then the diode is open. Because of the few parts involved in a simple basic circuit a resistance analysis is usually easy to make, requiring only an ohmmeter.

HALF-ADDER CIRCUITS.

APPLICATION.

Half-adders are used to form the sum of two incident binary digits. They are used as the basic circuit for a full-adder (two half-adders make a full-adder). Thus full binary adding networks used in computers consist of a number of half-adders, and associated circuitry.

CHARACTERISTICS.

May use either positive or negative logic, or combined logic.

Usually has four input lines with two output lines.

Consists of three AND gates and one OR gate.

Gain is less than 1 (no amplification is provided.)

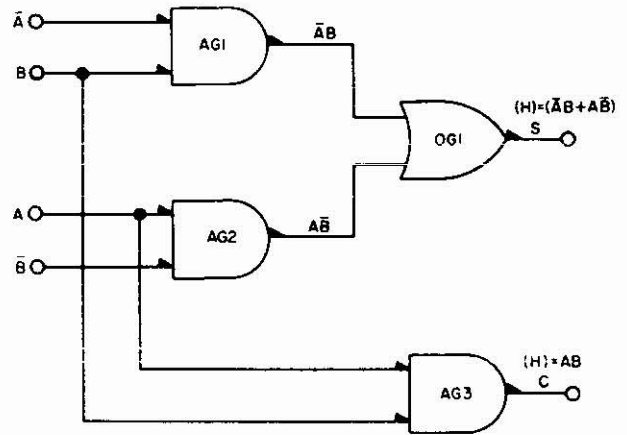
CIRCUIT ANALYSIS.

General. Since the half-adder performs binary (arithmetic) addition it is necessary that its output be identical to the results of the binary addition table as follows:

	A	0	0	1	1
	B	0	1	0	1
SUM		0	1	1	0
CARRY		0	0	0	1

We see from the table that two outputs are needed, since there is a carry of 1 when two 1's are added. It is evident that to add three binary numbers another carry output is needed. Hence to add more than two binary bits it is necessary to employ more than one half adder so that full-adders (consisting of two or more half-adders) are usually used in adder networks.

Circuit Operation. A typical half-adder is shown in the accompanying logic diagram.



Half-Adder Logic Diagram

Examining the diagram we see that three two-diode AND gates AG1, AG2, and AG3 are used, together with a single two-diode OR gate OG1. The logic equation at the output shows that the sum output (S) is high (H), and active whenever the two inputs A and B are unlike, and is inactive low (L) whenever the two inputs are alike. The output equation $S = \bar{A}B + A\bar{B}$ is read as "A or B, but not both"; this is the **exclusive OR** function. The carry output is active and high (H) whenever the two inputs A and B are equal to binary 1's, and is inactive low (L) for all other conditions. The table of combinations below shows the proper output for any particular input combination.

INPUTS		OUTPUTS	
A	B	S	C
L	L	L	L
L	H	H	L
H	L	H	L
H	H	L	H

TABLE OF COMBINATIONS FOR HALF-ADDER

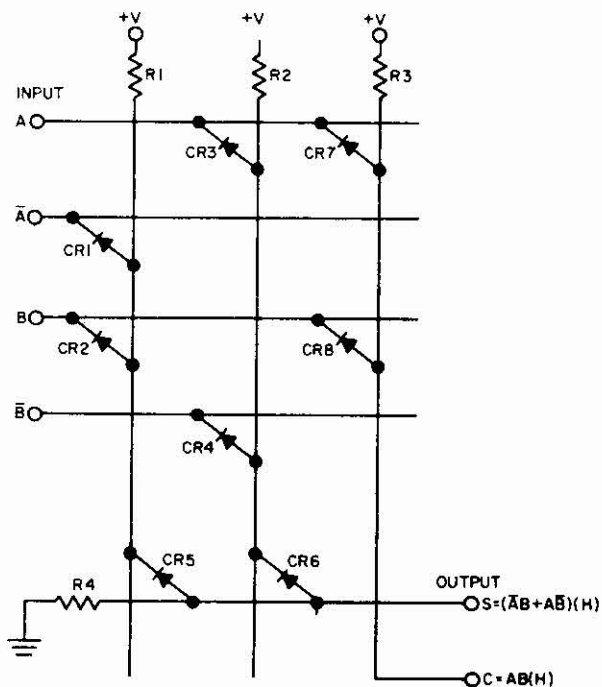
When the table of combinations is converted into a truth table by substituting the 0's and 1's, as shown below, it is evident that it corresponds to the binary addition table previously shown above, and that the circuit is performing the desired function.

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

HALF-ADDER TRUTH TABLE

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Circuit details are as shown in the accompanying matrix schematic (the half-adder may also be considered as a rectangular or square matrice).



Half Adder Matrix Diagram

Examination of the matrix diagram reveals that AND gate number 1 consists of diodes CR1 and CR2 with current limiting resistor R1; AND gate number 2 consists of diodes CR3 and CR4, with current limiting resistor R2, and the carry gate is AND gate number 3 with diodes CR7 and CR8, and current limiting resistor R3. The OR gate consists of diodes CR5 and CR6, with current limiting resistor R4. Zero volts represents logic 0 (L), and +V volts represents logic 1 (H).

Assume that inputs A and B are logic 1's, thus their input line is at a high level (H). Therefore, associated diodes, CR3, CR7 on line A, and CR2, CR8 on line B are reverse-biased and will stop conduction. Thus output C of AND gate number 3 (the carry gate) will rise to +V volts and also be at a high level, which is the output expressed by the formula $C=AB$.

With inputs A and B high, their complement inputs \bar{A} and \bar{B} (NOT A and NOT B) are low, causing diodes CR1 and CR4 to conduct. Therefore, OR gate diodes CR5 and CR6 will not conduct, since the potential at the anode end of R1 and R2 will be zero, and with the diode cathodes connected to ground through R4 no potential exists across these diodes. Thus there is no output from the S output line, and it is a logic 0.

In a similar manner, it is evident that for the sum output (S) to be high (H), inputs $\bar{A}B$ or $A\bar{B}$ but **not both** must be a logic 1 (H). For these conditions, either diode CR7 or

diode CR8 is held inoperative by reverse bias from the logic 1 input, while the other diode conducts because of the lack of an input (both diodes must be reverse biased to produce an output). Therefore, carry output, C, remains inactive and low or a logic 0. By following the table of combinations (or truth table) for each input condition, and by using the matrix diagram to determine which diodes are activated and which are not, you can verify operation of the circuit against each unique output listed in the table. Normally, when inputs A and B are alike, the sum output is always 0 (L), and when unlike it is always 1 (H). The carry output, C, is always 0 (low) except when both A and B inputs are high (1), in which case it is also high (H), and a logic 1.

FAILURE ANALYSIS.

General. Large computers are usually designed with built-in test circuits, signals, and alarms which indicate when a section or module is operating incorrectly. The offending board or chassis may then be replaced quickly to keep the computer operating. In large computer repair shops, test jigs are provided into which the module may be plugged and the necessary inputs applied to locate the defective circuit. Once the circuit is located the individual parts are easily checked by resistance or voltage measurements to find the defective part. Once the module is located, a systematic procedure such as indicated in the following paragraphs will help isolate the failure.

No Output. Loss of output can be caused by loss of input signals, loss of bias supply, or open diodes. When no output is obtained from any of the gates with the proper input supplied, it is most probable that the bias supply is defective. No output from a single gate usually involves the diodes and current limiting resistor for that gate only. Refer to the discussion of failure analysis for the AND gate (or the OR gate, as applicable) and which were previously explained in this section of the Handbook.

Continuous Output. A continuous output regardless of the type of input signal applied may be caused by a shorted OR gate diode, or by AND gate outputs occurring at the wrong time. Follow the procedure discussed in the following paragraph for an incorrect output to locate the defective circuit and part.

Incorrect Output. The sum output, S, and carry output C, must be active only as indicated in the table of combinations (or the truth table). Any other output for a specified set of inputs indicates a change in circuit logic caused by a defective part. Therefore, it is usually easier to set up specific inputs (preferably inputs which yield incorrect outputs) and check the output of each gate with a voltmeter or an oscilloscope. For example, assume that both A and B inputs are made high (H), and the sum and carry outputs both show high (H). Checking against the truth table reveals that for such an input the sum output is a logic 0, and the carry output is a logic 1. In this case the C output is correct, but the S output is not (it should be a logic 0). This indicates that OR gate number 1 is being activated when it should not be (both inputs should be low). Con-

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necting the test equipment to the OR gate input lines (separately) will show which AND gate (AG1 or AG2) is activated. The trouble is then localized by checking the defective AND gate with an ohmmeter, as described in the failure analysis for the AND Gate circuit previously discussed in this section of the Handbook. (The AND gate diodes are most likely open, check for a high forward resistance with an ohmmeter.)

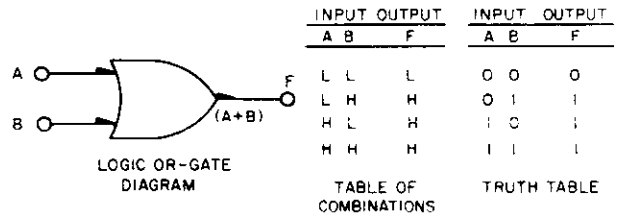
TRANSISTOR LOGIC.

Like the diode, the transistor may be employed in logic circuits. While some of the basic circuits such as the AND and the OR circuit perform the same operation as in diode logic, numerous advantages are obtained, and in addition, circuits not possible with diodes can be utilized, such as NAND, NOR, and similar *not* operations. The additional element in the transistor provides the ability to provide an inherent inversion similar to that normally obtained in the electron tube. Of much greater importance, however, are the improvement in operating speed possible with the transistor, plus the possibility of obtaining a gain through the circuit. For stages that require a heavy current output for operating relays and other electronic devices the transistor emitter-follower connection provides power output with reduced gain. Because of the high input and output impedances possible with the transistor, the shunting effect of parallel inputs or outputs is not as great a problem as it is with diodes. Thus an entire new field of logic circuits and application is open by the use of transistors. In turn, other new circuitry is developed by combining diode and transistor logic (DTL), or by using direct coupling (DCTL). Basic circuits concerning transistor logic will be discussed in the following paragraphs of this section of the Handbook. In later sections DTL, DCTL, RTL, TR and other versions of transistor circuits using other forms of logic will each be discussed.

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has the same polarity at input and output, but falls within the class of EMITTER-FOLLOWER circuits which are separately discussed. Thus the common-base connected OR circuit is the only remaining circuit which does not fall within another circuit classification and has the same polarity output as input. Consequently, the following discussion mainly concerns the common-base circuit, though other representative OR circuits may be briefly shown for completeness. It should be realized that in logic operations identical logic circuits have many forms which vary with design. For example, where one designer may use a single transistor OR gate to perform logic addition, another designer may use three or four transistors to accomplish the same purpose. This is why the logic designer usually uses the block diagram type of logic diagram representation rather than the schematic, since the function performed denotes the type of circuit, while the parts and actual circuit connections or arrangement are of no consequence as long as the desired logic operation is performed.

The symbolic logic representation of a positive transistor OR circuit is shown in the following illustration, together with a table of combinations. When the values of 0 and 1 are substituted in the table of combinations for L and H, respectively it is recognized as a standard OR truth table. Thus it is clear that in logic notation and representation both the diode and the transistor OR circuits are identical (see discussion of DIODE OR-GATE in this section of the Handbook).



TRANSISTOR "OR" GATE.

APPLICATION.

The transistor OR gate is used in computers to perform logic addition with increased speed and gain.

CHARACTERISTICS.

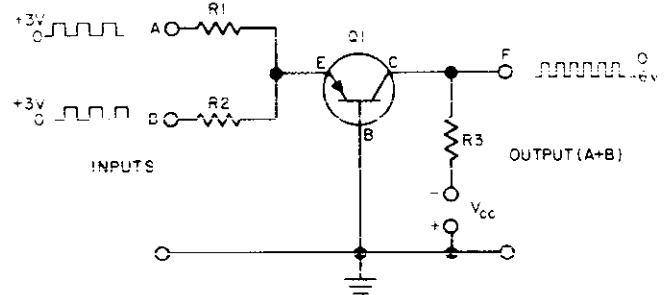
- May use positive, negative, or combined logic.
- Provides additional gain.
- May be either single transistor or multiple transistor type (multiple type provides a transistor for each input).
- Represents logic addition ($1 + 0 = 1$).

CIRCUIT ANALYSIS.

General. There are many types of transistor OR gates. When the common-emitter configuration is used, the circuit usually becomes a NOR circuit because of the polarity inversion. The common-collector configuration

The filled-in triangle indicates high level operation or positive logic. With a positive signal representing 1, a positive output is obtained.

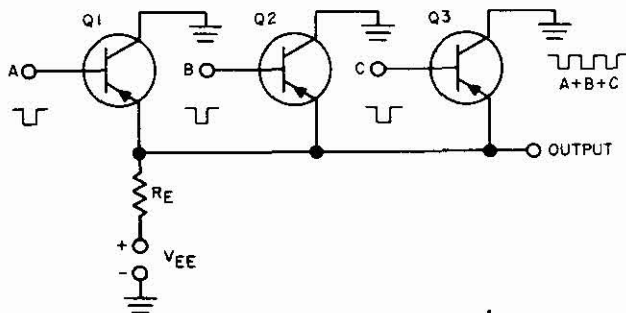
Circuit Operation. The schematic diagram of a typical two-input, positive, single-transistor OR-gate is shown in the following illustration.



Two-Input, Common-Base, Positive OR Gate

In the circuit shown, the emitter is left floating and reverse bias is applied to the collector. Therefore, with no signal applied either R1 or R2, simulating a 0, transistor Q1 rests in the cutoff condition. Collector current cannot flow (because of reverse collector bias) and the output voltage is the same as the collector supply voltage (-6 volts as shown on the waveform). When a +3-volt signal is applied either R1 or R2 simulating a 1, forward bias is applied to the emitter, and collector current flows through R3 producing a positive-going output. In this case it is assumed that the input voltage is sufficient to drop the collector potential to 0, and a 6-volt positive output is obtained. When the input signal is removed, the transistor returns to its quiescent state, with no collector current flowing and the 0 level at -6 volts. There is, of course, a reverse current flow (ICBO) due to thermal effects inherent in transistor operation. However, this reverse current is so small (usually less than a few microamperes) that it may be neglected. Since there is no signal inversion in the common base circuit, the output signal is an amplified replica of the input signal (except for distortion produced during turn-off). This circuit will not operate as a negative OR gate by reversing the polarity of the input signal since it is already at cutoff. The circuit is only slightly affected when both OR signals are applied simultaneously (the case of the inclusive OR). In this instance, the application of both input signals merely increases the minority carriers released in the transistor and it takes Q1 longer to recover from the operating pulse, thus producing a slightly longer output pulse than when individually triggered. Input resistors R1 and R2 are large valued and are used to isolate the two inputs, since they are both connected to the same emitter.

Circuit Variations. A typical 3-transistor OR gate is shown for comparison in the accompanying illustration.



Three-Stage OR Gate

A study of the schematic reveals that the circuit arrangement is that of the emitter-follower, and that the three outputs are parallel connected using common load and bias resistor RE. In the 0 or inactive state a positive voltage is applied to the base of Q1, Q2, and Q3 and they rest

in a cutoff state. When a 1 signal, consisting of a negative voltage is applied to any transistor, the base is forward biased and emitter current flows. The emitter current flow through RE develops a negative output signal, and the emitter resistor also determines maximum current flow in the triggered transistor. Once the input signal is removed, the stage again resumes its cutoff condition. An output trigger results when any of the inputs are energized or when all of the inputs are energized, simultaneously, representing inclusive OR function. Since a negative input produces a negative output, negative logic is employed.

FAILURE ANALYSIS.

General. Because of the few components involved, simple resistance and voltage checks using a high resistance voltohmmeter will usually reveal the source of trouble. If the input voltage, and the supply and collector voltage are normal, and the resistor values are correct, faulty operation can only be caused by a defective transistor.

No Output. An open input or output resistor, or a defective transistor will cause a no-output condition. Check the supply and collector voltage with a high resistance voltmeter. If the collector voltage is the same as the supply voltage with no input applied, load resistor R3 is probably satisfactory. If no output is obtained with normal collector voltage and the proper input applied, input resistors R1 and R2 are both open or Q1 is defective. Replace the transistor with a known good one and check the resistance of R1 and R2 with an ohmmeter.

Partial Output. If an output is obtained when either A or B inputs are applied but not when both are applied, check R1 and R2. If a reduced output is obtained with either input activated, the supply voltage, the transistor or R3 are defective. Replace the transistor with a known good one, check the value of R3 with an ohmmeter, and check the supply voltage with a voltmeter. If the outputs are normal with a "1" input applied but a partial output occurs with no input applied, either Q1 is defective or there is a low resistance shunt across one of the inputs.

Continuous Output. If a continuous output occurs whether or not an input is applied, Q1 is defective. Replace it with a known good transistor.

TRANSISTOR "AND" GATE

APPLICATION.

The transistor AND gate is used in digital computers to perform logic multiplication with high speed and gain.

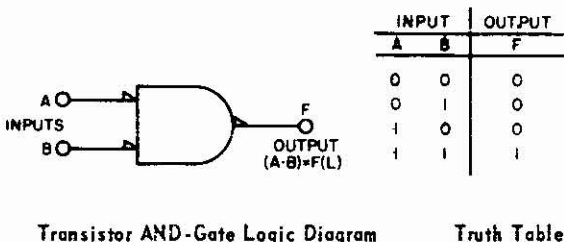
CHARACTERISTICS.

- May use either positive, negative, or combined logic.
- Provides higher speed and gain than the diode.
- Performs logic multiplication ($1 \cdot 1 = 1$).
- Single-stage gate uses common-base configuration, multi-stage gate uses any configuration.

CIRCUIT ANALYSIS.

General. The AND gate, like the OR gate previously discussed in this section of the Handbook, can consist of a single stage with multiple inputs, or a number of similar stages with separate inputs. The AND logic function requires that an output be produced only when all the inputs are applied simultaneously. No output is obtained for any other combination of inputs.

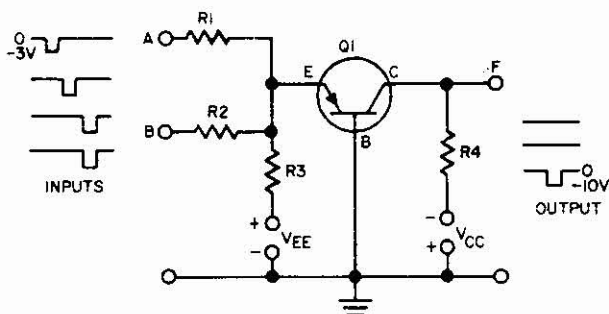
Circuit Operation. The logic diagram for a typical AND circuit using the common-base configuration is shown in the accompanying diagram, together with a truth table.



Transistor AND-Gate Logic Diagram

Truth Table

The open triangles indicate that negative logic is used, and the symbol for the transistor AND gate is the same as that for the diode AND gate. The truth table is recognized as a standard AND table, where an output only occurs when both inputs are applied simultaneously. The schematic for this negative AND-gate is shown in the accompanying figure.

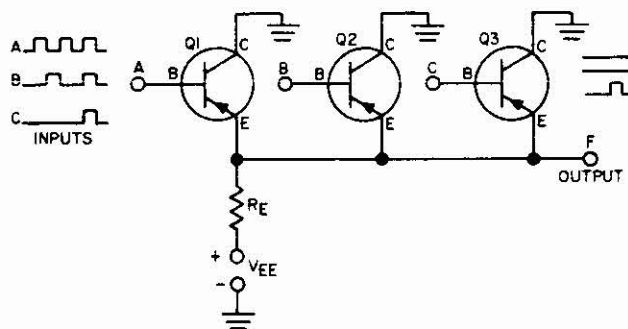


Negative Transistor AND-Gate Schematic, Common-base Circuit

As shown in the schematic, transistor Q1 is forward biased by the positive voltage applied to the emitter. Thus with a reverse collector bias applied through R4, and a forward bias applied through R3, the transistor conducts heavily in the quiescent or inactive state, and the collector voltage is dropped to zero across load resistor R4. Thus, there is no output and a logic zero is represented. When an input signal such as a negative pulse or step-voltage is applied to either input A or B, but not to both, the forward bias is reduced. This slight reduction in bias changes the collector current very little so that the input still remains

effectively at the zero output level. When the negative input is applied to both inputs simultaneously, twice the current produced by a single input flows through base resistor R3 and drops the forward base-bias to below the cutoff point. Collector current now ceases flowing through R4 and since the voltage drop across R4 is now zero, full reverse collector voltage appears at the collector, producing a negative output voltage. When the input signal ceases, collector current flow through R4 resumes, and again drops the collector voltage to zero. Thus, the output voltage rises and falls as both inputs rise and fall together.

Circuit Variations. A typical schematic for a three-input AND-gate, using separate transistors for each input is shown in the accompanying illustration.



Three-Stage AND Gate

Examination of the schematic reveals that the emitter-follower connection is used, with the transistor outputs connected in parallel across a common load and bias (emitter) resistor. Since the emitters are connected to a positive bias voltage, forward bias causes each of the transistors to conduct. With no input applied, emitter current flow through resistor RE (because of forward biased emitter) drops the output voltage to zero. Thus, the emitter voltage is effectively reduced to zero level. When a "1" signal of say +5 volts is applied to either Q1, Q2, or Q3 the transistor is reverse biased and ceases conduction, meanwhile, the other two transistors continue to conduct and keep the output at zero level. When all three inputs are applied simultaneously, current flow through them is reduced and the emitter voltage rises toward the bias supply, creating a positive output voltage. When the positive output voltage rises to +5 volts, the emitter voltage is again at zero bias level and stays at this point until the input pulse ceases, whereupon once again heavy forward conduction causes the emitter voltage to be reduced to zero. Thus any positive input signal level less than the total emitter bias voltage, will effectively pass through the transistor(s) and appear as the output voltage (the actual output amplitude is a fractional amount less than the full amplitude of the input signal because of ohmic drop in the transistor, however, this drop is so low as to be considered negligible).

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FAILURE ANALYSIS.

General. Because of the few components involved, simple resistance and voltage checks using a high resistance volt-ohmmeter will usually reveal the source of trouble. If the input voltage, and the supply and emitter voltages are normal, and the resistor values are correct, faulty operation can only be caused by a defective transistor.

No Output. An open emitter or collector resistor, lack of emitter voltage, or a defective transistor as well as an open input resistor will cause a no-output condition. Check the supply and emitter voltage with a high resistance voltmeter. Check the voltage from input A and B to ground; it should be approximately the same as that measured for the emitter voltage, (emitter to ground) indicating that resistors R1 or R2 are not open. With no signal applied, the collector voltage to ground should be zero. If a negative value of collector voltage is indicated, either the transistor is defective, or insufficient forward bias is applied to the emitter to cause saturation. Replace the transistor with a known good one and check the value of R3 with an ohmmeter. Check collector resistor R4 for continuity and proper resistance with an ohmmeter.

Partial Output. If a reduced output is obtained with all inputs activated, either the bias voltage, the transistor or R4 are defective. Replace the transistor with a known good one, check the value of the bias voltage with a voltmeter, and measure the resistance of R4 with an ohmmeter.

Continuous Output. If a continuous output occurs regardless of whether or not an input is applied, Q1 is defective. Replace it with a known good transistor.

TRANSISTOR "NOT" CIRCUIT.**APPLICATION.**

The transistor NOT circuit is used in computer and high speed switching circuits to provide signal inversion and high gain.

CHARACTERISTICS.

Either positive, negative, or combined logic may be used. High voltage or power gain is possible. Fixed-bias is usually employed. Output signal is inverted in phase and polarity from input signal.

On a logic basis, the output is the complement of the input.

Usually has one input and one output.

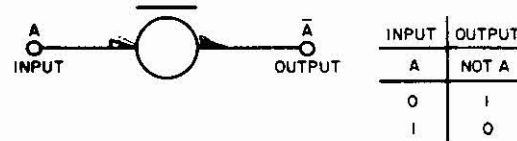
Input resistance is high and the output resistance is relatively low.

CIRCUIT ANALYSIS.

General. When the common-emitter configuration is used, the output polarity is always inverted by inherent transistor action similar to the electron tube grounded cathode circuit. In logic operation it is sometimes desired to produce a signal which is identical but opposite that of the input signal. This is the logical NOT operation, and the circuit

is also known as an **inverter**, which produces the **complement** of the input signal. Either a single stage of inversion is used, or the common-emitter version of a circuit is used to provide the desired logic operation and inversion simultaneously. This discussion will be limited to the use of a single stage operating as an inverter or NOT circuit. Other circuit variations will be discussed with the other circuits in which they are employed. The voltage gain obtained through this circuit also makes it useful as a level restorer.

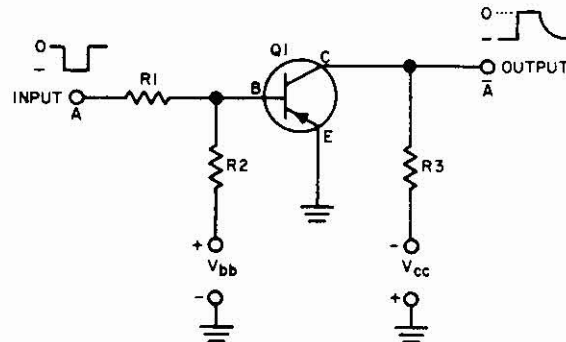
Circuit Operation. The logic representation of a typical NOT (inverter) circuit is shown in the accompanying illustration.



Logic Inversion
Diagram and
Symbol

Inverter Truth
Table

The open triangle on the input side and the closed triangle on the output side indicate that with a negative input, an inverted or positive output is produced. The actual schematic of a typical inverter is shown in the following figure.

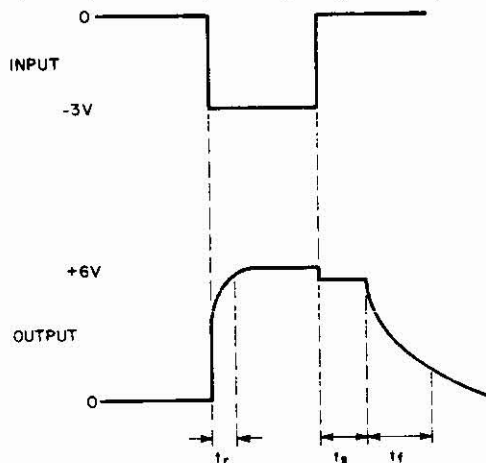


Transistor NOT Circuit

In the quiescent condition (the "0" state) with a positive base bias applied, transistor Q1 is at cutoff and no current flows (reverse collector current flow, I_{ceo} , is considered negligible). Since no collector current flows through R3, there is no voltage drop to oppose the supply and the collector and output voltage fall to almost the value of the negative supply, representing a logic zero output. When a negative (1) input signal is applied, the base bias

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is changed from a reverse to a forward bias and causes emitter current to flow. Collector current flow through R3 drops the negative supply voltage to approximately zero so that a positive going output is developed. With sufficient forward base bias (drive) to cause saturation, the output rests at the zero voltage level until the input signal is terminated. When the input signal stops, the collector voltage does not change immediately because of the minority carriers inserted into the base during saturation (in the PNP transistor these are holes). Therefore, collector current flow continues for the duration of the storage delay time until the minority carriers are drained out, whereupon the collector voltage becomes negative-going and falls to approximately the same value as the supply voltage. The relationships between input pulse and rise and fall times (t_r and t_f) on the output pulse and storage delay time (t_s) are shown in the following waveforms. The output waveform is slightly exaggerated to clearly show the delayed and deformed pulse which is produced. Since the circuit function is merely that of on or off, the pulse distortion is of no consequence except for the slight delay in operating time which ensues. Resistors R1 and R2 function as a base bias divider, with R1 also acting as a base current isolating resistor, so that the base cannot be shorted by connecting the input to ground when producing a logic zero input.



Input and Output Waveform Relationships

Rise time, t_r , is also known as **turn-on time** and is defined as the period from the start of the square wave until it reaches 90 percent of steady state amplitude. The turn-on delay is caused by the finite time it takes the carriers produced by emitter action to travel to the collector. The fall time, t_f , is also known as the **turn-off time**, and is the time which elapses from the start of the falling off period until it falls to within 10 percent of the final signal level. Storage relay time, t_s , is defined as the time from the ending of the input pulse to the start of the trailing edge of the output pulse.

Fixed bias and large driving pulses are usually used to produce a sharp turn-on time, and other forms of logic such as DTL and RCTL are used to decrease the turn-off times.

These circuit variations will be discussed in more detail with the appropriate logic and in the circuits in which they occur. Since the transistor design also determines the turn-on and turn-off characteristics, a special group of transistors of various types classified as "switching transistors" are employed to obtain greater speed and cleaner switching operation.

FAILURE ANALYSIS.

General. Because of the few parts involved, a resistance and voltage analysis, performed with a volt-ohmmeter, will usually locate the faulty component without any loss of time.

No Output. If either R1, R2, or R3 are open, or if Q1 is defective, no output will be obtained. With no input signal applied, check the base bias and collector voltage with a high resistance voltmeter, and measure the voltage from the input terminal to ground. Normal bias and collector voltage readings will indicate all resistors have continuity and probably are of correct value. Therefore, the fault must be with the transistor. Replace it with a known good one.

Low Output. A defective transistor, improper bias, or low collector voltage can reduce the normal output. Check the bias, collector, and supply voltages with a voltmeter. Replace Q1 if all voltage readings are normal.

TRANSISTOR NOR GATE.

APPLICATION.

The transistor NOR gate is used in computers and switching devices to supply an inverted OR (that is a complemented OR) output.

CHARACTERISTICS.

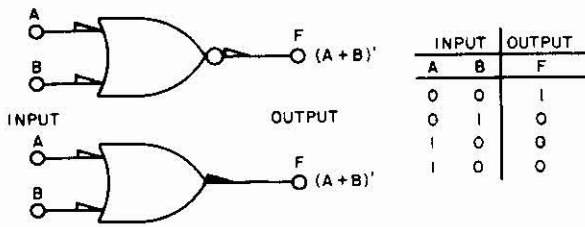
- May use positive, negative, or combined logic.
- Usually uses fixed bias.
- Provides an inverted or complemented output.
- Accomplishes logic addition and complementation simultaneously.
- Has a high impedance and a low output impedance.

CIRCUIT ANALYSIS.

General. The NOR gate provides a standard OR output but in inverted or complemented form. Thus a NOT OR output is supplied from a single stage. Since the transistor common-emitter configuration produces an inverted output signal, it is only necessary to change the common-base OR circuit to a common-emitter arrangement to produce a NOR circuit. While the basic need for the NOR circuit is to complement a number, its primary use is to accomplish arithmetic subtraction by addition. Thus complicated circuitry is avoided in the digital computer.

Circuit Operation. The logic diagram for a typical NOR circuit its associated truth table is shown in the following illustration.

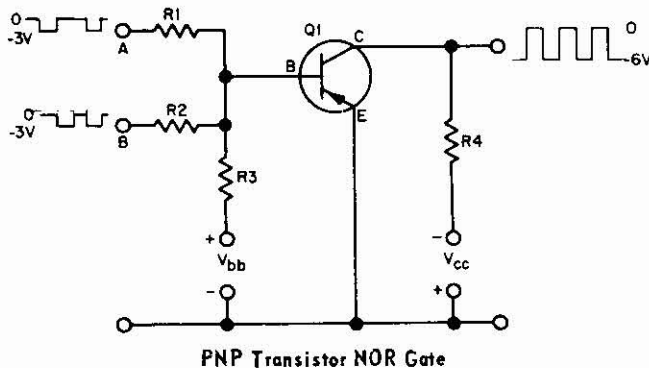
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NOR Logic Diagrams Truth Table

The open triangles in the logic diagrams denotes that negative logic is used. Thus the 1-state requires a negative input signal for activation. Since the output is inverted in the NOR circuit, this is indicated by the small circle (in the upper diagram) adjacent to the triangular output level indicator. This indicates that with a negative input a positive output is obtained. The same condition could also be indicated by omitting the small circle and using a filled-in triangle at the output as shown in the lower (alternate) diagram. In this case the input and output levels are indicated as being different or inverted, and since the input is indicated as negative in the activated state by the open triangles, the logic is also negative. It should be noticed that the circle when used to express inversion must be located at the symbol. The small circles at the input and output terminals represent terminal connections and have no logic significance.

The schematic for a typical single stage transistor NOR circuit is shown in the accompanying illustration. Note that the PNP common-emitter configuration is used.



A positive (reverse) fixed bias is applied to the base to keep the transistor cut off in the inactive state. With no input applied, and reverse bias applied to the base and to the collector no conduction occurs, therefore, the collector and output voltage is approximately the same as the collector supply value. Since a negative "1" or high signal is re-

quired to activate the circuit, the zero input represents a low, and the consequent negative output a high, or inverted low signal. Thus the first combination in the truth table is verified. When a negative input is applied to A, or B, or to both A and B, it forward biases the base and causes collector current flow. The voltage drop caused by collector current flow through R4 reduces the collector voltage (and the output to zero. Thus a high input signal produces an inverted or low (positive) output signal. Resistors R1 and R2 function as isolation resistors to prevent loading on the separate inputs A and B. Since the input resistors are connected in series with R3 to ground, they form a voltage divider which places the larger voltage across R3 and the base of Q1. Both R3 and either R1 or R2 also protect against shorting of the base bias or input circuit respectively, when a zero level input is applied. The high resistance of the input resistors requires that a relatively high voltage be used to cause base current to flow. Hence, operation of this type is known as **voltage mode** operation. (In DCTL logic the resistors and bias are omitted and only a fraction of a volt input is necessary to drive the base into conduction, and this is called the **current mode** of operation.)

When both inputs are simultaneously applied, the larger negative input assumes control. When Q1 is driven into collector saturation by the activating signal, excess carriers are inserted into the base and the turn off time is extended by the storage time needed to drain the transistor of these excess holes. Because the full operating range of the transistor from cutoff to saturation is available, relatively high and power output can be obtained from this common-emitter arrangement.

FAILURE ANALYSIS.

General. Because of the few parts involved, a resistance and voltage analysis may be quickly made with a voltmeter. Obvious symptoms may also be used to locate the failure and are discussed in the following paragraphs.

No Output. Lack of supply voltage, no input signal, an open collector resistor, or a defective transistor will cause a no-output condition. Measure the collector and bias voltages with a high resistance voltmeter, and measure also from the input terminals to ground. This will prove that R1 and R2 have continuity and also roughly check their approximate value. If voltage readings are normal and the no-output condition persists, replace Q1.

Reduced Output. A defective transistor, low collector voltage, insufficient input drive or a change in the value of R4 can produce a reduced output. Check the value of R4 with an ohmmeter, and the supply and collector voltages with an ohmmeter, and the supply and collector voltages with a high resistance voltmeter. Replace the transistor with a known good one. If a reduced output still exists check the input signal amplitude with a vacuum-tube voltmeter or an oscilloscope.

Continuous Output. If a continuous output occurs with or without a signal input the transistor is defective, replace it with a known good transistor.

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TRANSISTOR NAND GATE.

APPLICATION.

The transistor NAND gate is used in computers and switching devices to supply an inverted AND (a complemented AND) output.

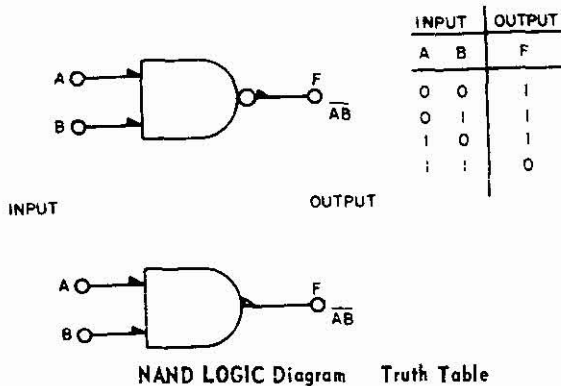
CHARACTERISTICS.

- May use positive, negative, or combined logic.
- Usually uses fixed bias.
- Provides an inverted or complemented output.
- Accomplishes logic multiplication and complementation simultaneously.
- Has a high input impedance, and a low output impedance.

CIRCUIT ANALYSIS.

General. The NAND gate provides a standard AND output but in inverted or complemented form. Thus a NOT AND output is supplied from a single stage. Since the transistor common-emitter configuration produces an inverted output signal, it is only necessary to change the common-base AND circuit to a common-emitter arrangement to produce a NAND circuit. Its primary use is accomplish arithmetic division by multiplication and addition and thus avoid the necessity for more complicated circuitry. This circuit is also sometimes referred to as a coincidence circuit or an *all* circuit in other publications.

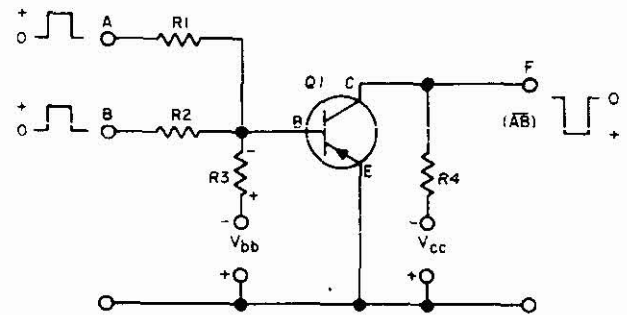
Circuit Operation. The logic diagram for a typical NAND circuit, with its associated truth table is shown in the following illustration.



The closed triangles in the logic diagrams indicate that positive logic is employed. That is a positive input signal represents an active 1. The inversion of output produced by the NAND circuit is indicated by the small circle (in the upper diagram) adjacent to the triangular output level indicator. This shows that with a positive input a negative output is obtained. When the level indicators alone are used, the inversion is shown by using an open triangle at the output (as shown in the lower (alternate) logic diagram) and omitting the circle. Since the input levels in the activated state are shown as closed triangles, positive logic is indicated, and

with an open triangle as the output level indicator a negative or inverted output is indicated. Note that when the circle is used to indicate inversion it must be placed at the symbol, and before the level indicator. The small circles at the input and output terminals represent terminal connections and have no logic significance.

The schematic of a two-input, single-stage transistor NAND gate is shown in the accompanying illustration. Note that the common-emitter configuration is used.



PNP Transistor NAND Gate

A negative, fixed base bias is applied to transistor Q1 to provide forward bias, and make the transistor conduct heavily in the so-called inactive state. With no input signal applied, and with forward base bias the transistor operates in the saturation region. Heavy collector current flow through R4 produces a voltage drop which reduces the negative collector voltage to zero. Since reverse collector bias is applied, a positive output is produced (absence of the input signal in this case represents a zero input). Thus the first combination in the truth table is verified. When a positive (one) input signal is applied to either input A or B, but not both, the voltage developed across R1 or R2 by base current flow is insufficient to stop conduction, and a zero or positive output still occurs. However, when the input signal is applied simultaneously to both A and B terminals, base current flow through R3 is twice that produced by single input signal, and, since it is in a direction which produces a polarity opposite to the forward base it cancels the bias, reducing it to zero. With no forward bias applied to the base and a reverse bias applied to the collector, transistor Q1 ceases conduction. With no collector current flow through R4, no voltage drop is produced, and the collector voltages falls to approximately the negative supply value. Thus a negative output is produced indicating a zero. Input resistor R1 and R2 act as isolating resistors for the separate AND inputs, and together with base resistor R3, preventing shorting of either the base or the bias when zero (grounded) input is applied. Since Q1 normally operates in the saturation region, excess carriers are inserted into the base, and the turnoff time is extended by the storage time needed to drain the transistor of these excess holes. Because the full operating range of the transistor from saturation to cutoff is available, relatively

high gain and power output can be obtained from this common-emitter arrangement.

FAILURE ANALYSIS.

General. Because of the few parts involved, a resistance and voltage analysis may be quickly made with a volt-ohmmeter. Obvious symptoms may also be used to locate the failure and are discussed in the following paragraphs.

No Output. To produce no output the transistor must continuously conduct. Such conduction may be stopped by loss of base bias or by the opening of R3, which has the same effect, or by lack of supply voltage or collector voltage by the opening of R4. Checking the bias and base to ground voltage, and that of the supply and the collector to ground voltage with a high resistance voltmeter will clear R3 or R4 from suspicion, and if the trouble still exists, Q1 is defective and should be replaced with a known good transistor. If Q1 conducts, but no output is obtained when simultaneous inputs are applied terminals A and B, either resistor R1 or R2 is open. An ohmmeter check of the resistors will locate the defective one. However, by checking the bias voltage from base to ground, and from A and then B to ground (when making voltage checks) the continuity of these resistors can be verified without performing the resistance measurement.

Reduced Output. A defective transistor, low collector voltage, insufficient input drive, or a change in the value of R4 can produce a reduced output. Check the value of R4 with an ohmmeter, and the supply and collector voltages with a voltmeter. Replace the transistor with a known good one if R4 and the voltage checks are normal. If a reduced output still exists, check the input signal amplitude with a vacuum-tube voltmeter or an oscilloscope.

Continuous Output. If a continuous positive-or-negative output is obtained regardless of whether or not inputs are applied, the transistor is defective. Replace it with a known good transistor.

TRANSISTOR FLIP-FLOP CIRCUIT.

APPLICATION.

The transistor flip-flop is used in electronic computers to supply an output and its complement simultaneously, as an off-on trigger, and for storage purposes. It forms the basic circuit used in most registers.

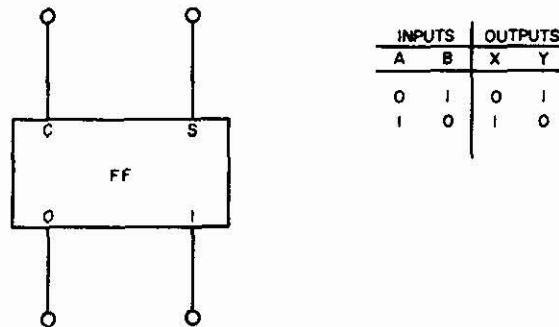
CHARACTERISTICS.

- May use positive, negative, or combined logic.
- Usually employs self-bias.
- Provides two outputs (one is the inverse of the other).
- Requires a turn-off or reset trigger to change state.
- Has two stable states, sometimes called off and on (or 0 and 1).

CIRCUIT ANALYSIS.

General. The basic transistor flip-flop is sometimes considered as two transistor inverters placed back-to-back.

However, by far the simplest arrangement, the d-c flip-flop uses a minimum of parts and corresponds closely to the mechanical form of "relay flip-flop" described in part C of this section of the Handbook. Actually, the flip-flop is considered to be a multivibrator, and the various types of transistor multivibrators are fully discussed in Section 8 of this Handbook (including the binary M.V.). The flip-flop circuit is included here for the sake of completeness of the logic section since most computers contain many flip-flops. Consequently, logic considerations will be stressed, and the overall operation may not be as detailed as might be found in Section 8 circuit discussions. However, sufficient detail will be given to satisfy the logic student. The symbolic logic diagram and truth table are shown below.



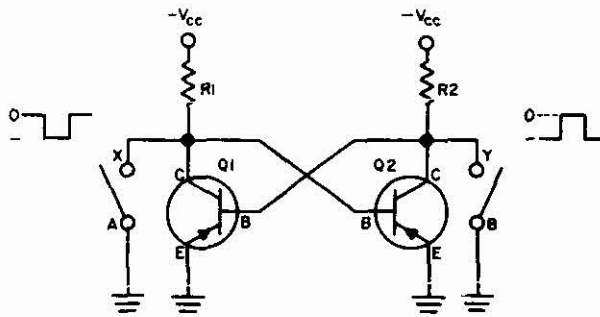
Flip-Flop Logic Diagram Truth Table

Like the other logic symbols, the flip-flop logic symbol is functional and is the same regardless of internal circuit. Thus any number of types of multivibrator may be indicated by the same logic symbol. Input and output level indicators are not shown since, in most instances, they may be determined from the levels shown on the outputs of driving or following circuits. The designation of clear (reset) or (C) and set (S) inputs are not required to be shown. However, the C input is always placed on the left of the diagram with the 0 output terminal, and the S input is placed on the right of the diagram with the 1 output in accordance with American and Military Standard usage (other arrangements may be found in other texts). The truth table shows inputs A and B with outputs X and Y. In most instances, these are the same terminals, and the table merely indicates that when one transistor is in the zero state the other transistor of the flip-flop is in the 1 state, and vice versa.

Circuit Operation. The schematic of a simple d-c transistor flip-flop is shown in the accompanying illustration. Outputs are taken from points X and Y, and inputs are represented by A and B switches which temporarily ground these points when the input is considered to be applied. The manner in which the trigger is applied is of no immediate concern since it may be a number of ways, such as by diodes, transistors, relays, switches, or otherwise (in some instances these triggers may form a part of the circuit

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and are included in the discussion, see the Diode-Transistor Flip-Flop).



Basic Transistor (PNP) Flip-Flop

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Assume for ease of discussion that initially transistor Q2 is conducting, and Q1 is cut off. With Q2 operating in the saturation region, heavy collector current flows and the collector voltage is dropped to almost zero by current flow through R_2 , and the Y output is zero. Since the collector of Q2 is also connected to the base of Q1, the base of Q1 is also held at zero bias or practically at cut off, and no collector current flows through Q1. With no collector current flow through R_1 , the collector voltage on Q1 is almost the full value of the negative bias supply. Since Q2 is directly connected to the collector of Q1, this negative collector voltage places a large forward bias on the base of Q2 and holds it in heavy conduction. As long as the heavy collector current flows through Q2, transistor Q1 remains in the inactive state. Thus, the Y output is held at zero, representing a logic 0, while the X output is a large negative voltage, representing a 1. If switch A is now temporarily closed (simulating a set input), the forward bias is removed from the base of Q2, because the collector of Q1 is shunted to ground by contact A, therefore, collector current ceases flowing through Q2. As the collector current through Q2 ceases, the collector voltage of Q2 rises toward the negative bias source value, and places a forward bias on the base of transistor Q1. Consequently, Q1 conducts heavily, and the voltage drop across collector resistor R_1 places the base of Q2 at zero and prevents the flow of collector current in Q2. Now, Q2 remains in the nonconducting condition, while Q1 continues to conduct heavily. Meanwhile, the Y output is a large negative voltage, representing a 1. When switch B is temporarily closed (simulating a clear input), the base of Q1 is grounded, and causes it to stop conducting. The rising collector voltage on Q1 places a negative (forward) bias on the base of Q2 and causes it to conduct heavily, and gain resume the original state assumed at the beginning of the discussion. This action again produces an 0 output at Y, while the X output is a 1. Thus when Q2 conducts, the X output is a 1 and the Y output is an 0, and when Q1 conducts, the Y output is a 1 and the X output is an 0. The alternate X and Y outputs of 0 and 1 con-

tinue as the flip-flop is triggered off and on by closing switch contacts A and B. Although relay triggering is assumed in this discussion, modern circuits use switching diodes or transistors, which operate at much greater speeds than relays to produce high speed operation. It is also possible to provide self-triggering action and have the flip-flop operate at a specific repetition rate, in which case it is a true multivibrator (see Section 8, part B of this Handbook for the complete discussion of semiconductor multivibrator circuits).

FAILURE ANALYSIS.

If either Q1 or Q2 is defective, either both outputs will be zero, or the outputs will be apparently normal and opposite, but cannot be triggered into the other state. Similarly, if both R1 and R2 are open no outputs will be obtained; but if only one resistor is open, the flip-flop will rest in one stable condition and be impossible to trigger into the other condition. Check the collector voltage to ground with a voltmeter, and manipulate switches A and B manually, observing if the collector voltage changes; if it does, the other transistor and associated collector resistor are probably at fault. If in doubt, measure the resistance of R1 and R2 with an ohmmeter. If R1 and R2 resistance is normal the transistor(s) are at fault. To determine which transistor is defective, connect the base of the conducting transistor temporarily to ground. If the collector voltage becomes more negative indicating that conduction has ceased, the transistor can be presumed to be satisfactory. Check the other transistor similarly, if defective it will not stop conducting and the collector voltage will remain near zero. If switches A and B are relay contacts, it is possible that poor or dirty contacts will prevent the flip-flop from changing state. Such condition can be determined by temporarily connecting the collector to ground (shunt the doubtful contact) and observe if operation is then normal. If in doubt, replace both transistors with good ones.

EMITTER-FOLLOWER CIRCUITS.

APPLICATION.

The transistor emitter-follower circuit is usually used in computers and switching circuits to provide a high output current to drive other transistor circuits. This circuit is also used for impedance matching, driving coaxial lines, and for isolating input and output stages.

CHARACTERISTICS.

May use either positive, negative, or combined logic.
May use either fixed or self bias, depending on the circuit arrangement.

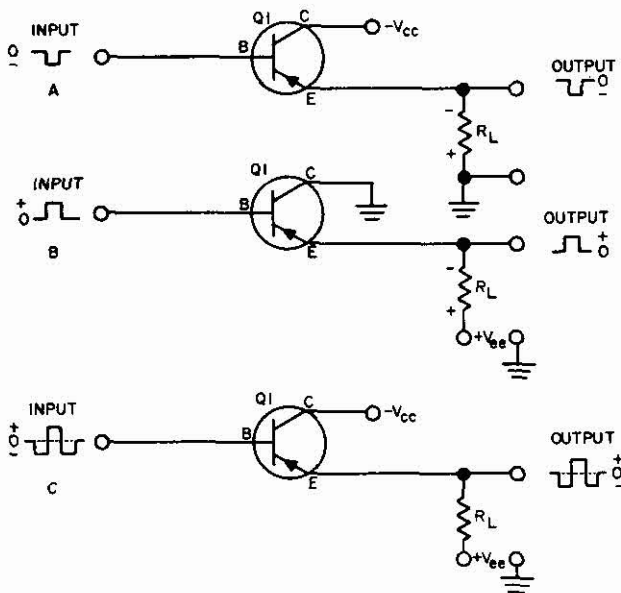
Because of the low output impedance, a high current gain is obtained, but the voltage gain is always less than 1 (output smaller than input).

CIRCUIT ANALYSIS.

General. The emitter-follower or common-collector transistor configuration is usually (but not always) operated in the active region. Bias is normally such that the stage operates as a class A amplifier, as opposed to operating in the entirely saturated or cutoff region. Thus the emitter-follower will usually respond to either a positive or a negative input signal. Since the output is in-phase with the input a negative input will produce a negative output, and a positive input will produce a positive output. Operation is similar to the cathode-follower type of electron tube circuit. In the electron tube cathode-follower, there is a large difference in voltage between the grid input level and the cathode output level. However, in the emitter-follower, there is only a slight difference in d-c input and output levels (usually less than 0.5 volt). Therefore, the emitter-follower makes a very useful dc current-amplifier, capable of large current amplification without shifting the level between the two stages to any noticeable extent.

Circuit Operation. There is no special symbolic representation for an emitter-follower circuit. The logic diagram uses functional symbols only, regardless of circuit configuration. Thus an OR gate (or AND gate) may be formed of either common-base, common-emitter, or emitter follower (common-collector) arrangements, and they would be drawn identically in the logic diagram, although the schematic representation would be different. Operation of the common-collector circuit is described for a sinusoidal input in section 3, paragraph 3.5 of this Handbook. Operation of the emitter-follower in response to pulse input is discussed in the following paragraphs, and then typical OR and AND circuits are analyzed.

In the accompanying figure, three emitter-follower types of operation are illustrated. Part A shows a negative bias applied to the collector and no bias applied to the base, the emitter is returned to ground through load resistor R_L .

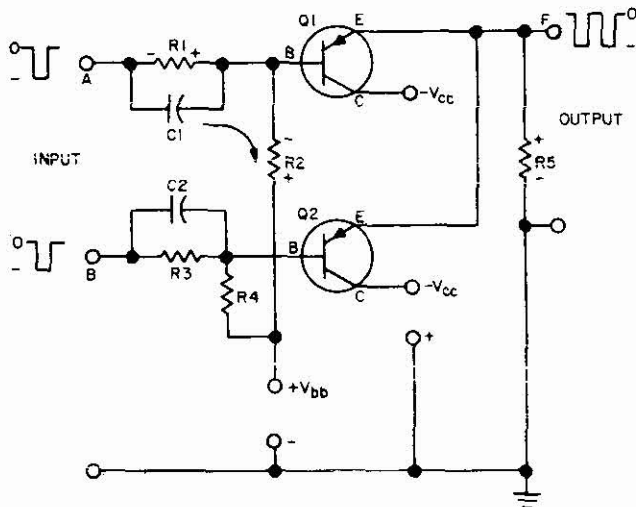


Emitter-Follower Circuits

With a reverse collector bias and no forward base bias the transistor rests in an essentially cutoff condition with no collector current flow. With no input there is no output. A positive input signal would only bias the base further in a reverse direction and no output would occur. However, with a negative input signal the base is quickly driven into conduction by the forward bias, and both emitter and collector currents flow. Electron flow is from the emitter through R_L and back to the collector, and a negative output voltage is developed across load resistor R_L . Thus the output voltage follows the input voltage. When the input signal is terminated the transistor stops conducting and the output pulse is completed as shown by the waveforms in the illustration. In Part B of the figure the opposite condition is shown, the collector is connected to ground and the base is again left open, but the emitter is forward-biased by a positive voltage to ground. With no base bias, and forward emitter bias, heavy emitter current flows and produces a voltage drop across R_L which opposes the forward bias and drops the output to approximately zero. Application of a negative input signal cannot increase the emitter current any appreciable amount so the output remains at zero. However, when a positive input pulse is applied, the base is biased more positive than the emitter (reverse bias), and collector and emitter current flow ceases. As a result, the output voltage rises to the value of the positive emitter bias, since no voltage drop is produced across R_L to reduce the output. In part C of the figure, both forward emitter bias and negative (reverse) collector bias are applied, and the transistor is biased at the center of its active region (Class A operation). With no signal applied, the quiescent value of collector current represents zero level. When a negative input is applied, the forward bias is increased, a larger collector current flows, and a negative voltage drop appears across R_L and at the output. In a similar manner, when a positive input signal is applied, collector current flow is reduced by the increasing reverse bias, and the emitter voltage rises towards the bias value, producing a positive output. Thus the emitter output follows the input signal, and operates entirely in the active region (this is the same operation as occurs in regular amplifier operation).

A typical emitter-follower OR-Gate is shown schematically in the accompanying illustration. The inputs are separate and the outputs are connected in parallel. In the quiescent condition, with no signal applied, both $Q1$ and $Q2$ are nonconducting since collector current is prevented from flowing by reverse base bias applied through $R2$ and $R4$ from a fixed bias source. When the A input is activated by a negative one signal, $Q1$ is forward biased and emitter current flow through $R5$ develops a negative going output voltage across $R5$. The output voltage is slightly less than the input voltage by the base-

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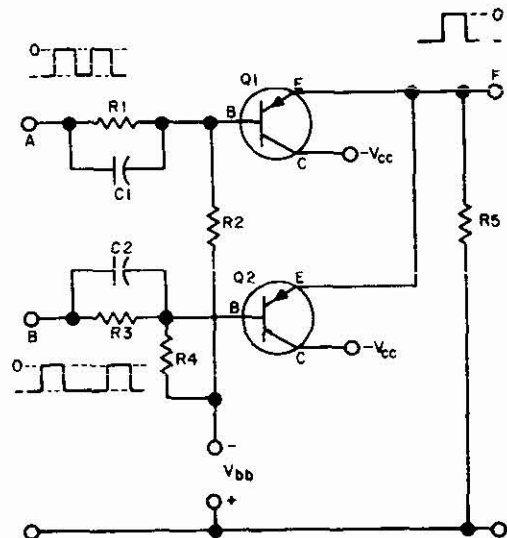


Emitter-Follower OR Gate

emitter voltage. Capacitor C1 helps speed up action by applying the leading and trailing edges of the pulse trigger instantly to the base, bypassing R1 so that only the low frequency components representing the flat-top portion of the pulse are attenuated by R1. In addition, R1 and R2 form a dual voltage divider. When input A is at ground potential representing a zero input, the base is isolated from the input by R1 preventing it from being shunted to ground, and maintaining the desired high input impedance. When Q1 is conducting the base-collector resistance is low, but is prevented from shunting the bias source by R2. Thus the bias remains unaffected by any input signal shunting effect. As a result of base current flow through R1 a negative input voltage is developed, and the bias and signal voltages add algebraically, to produce a forward (negative) bias. When the input signal is removed, the fixed positive bias again resumes control, biasing the base in a reverse direction and stopping conduction.

When an input signal is applied to input B, identical operation occurs. Capacitor C2 now passes the leading (and later the trailing) edges to Q2, while resistors R3 and R4 form a similar input voltage divider and bias divider as explained for R1 and R2 previously. When Q2 conducts, the output voltage is developed across emitter load resistor R5. A negative input produces a negative output. When the input signal is removed the transistor again returns to its normal cutoff condition and output ceases. When an output is developed by either Q1 or Q2, this negative voltage is applied as a reverse emitter bias to the non-conducting transistor so that it is prevented from being triggered. Should an input be applied to both A and B simultaneously, the signal with the larger negative amplitude will prevail and cause only that circuit to operate.

By reversing the input polarity and bias an emitter-follower AND gate is obtained, as shown in the accompanying schematic.



Emitter-Follower AND Gate

By comparing the emitter follower OR-Gate schematic shown previously with the emitter-follower AND-gate shown above, it is seen that the circuits are identical. By changing the base bias to a forward bias, Q1 and Q2 conduct in the absence of an input signal, and emitter current flow through R5 develops a negative voltage drop which holds the output to a steady negative level and produces a zero. When a signal is applied to either A or B but not to both inputs simultaneously, the input to which no signal is applied continues conduction and holds the output at zero. However, when an input is simultaneously applied to both A and B, both transistors are cut off and Q1 and Q2 stop conduction. The output rises in a positive direction to zero and produces an equivalent positive (one) output. When the input pulse ceases, both transistors resume conduction, and the output falls to the normal steady negative output level representing a zero.

Although the emitter-follower output voltage is always smaller in amplitude by the amount of base-emitter bias, a current and power gain are achieved. Current amplification is obtained by using a small amount of base current (usually in the microampere range) to control the large emitter current flow (usually in the millampere range). Average current gains on the order of 25, or more, are obtained. Since the power output is the voltage times the current, it is easily seen why a power gain is obtained even though voltage amplification is not produced. Although the common-base and common-emitter connections also can provide a power gain, the emitter-follower arrangement is unique in that it provides a low impedance and high current output. Therefore, it is usually employed as a driver stage capable of operating two or three other

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transistor stages without dropping to a very low level, or for operating relays, or lamps, which require high current at low voltage.

FAILURE ANALYSIS.

The emitter-follower AND, NAND, NOR, and OR gates are almost identical with respect to failure analysis with the previously discussed circuits of the same name, if it is remembered that the output signal is developed across the emitter load resistor (instead of the collector resistor), and that the collector is usually grounded without any series (load) resistor. Thus loss of output can be due to an open emitter resistor, a defective transistor, no emitter or collector voltage, or due to lack of an input signal. A voltage check of the base, emitter, and collector potentials will reveal if the source is normal, and whether or not any series resistance is open (or shorted). In case of any doubt, a simple resistance check will determine if the resistance is normal. Any continuous output which is not changed by an input signal indicates a defective transistor.

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LAMP DRIVERS AND RELAY PULLERS.**APPLICATION.**

Lamp drivers and relay puller circuits are used in computers and switching circuits to supply the power and voltage necessary to drive indicator lamps and operate relays indirectly by triggering a transistor.

CHARACTERISTICS.

Provides large voltage or power output, as needed.

Is controlled by a small voltage or current.

May be self-biased or fixed biased.

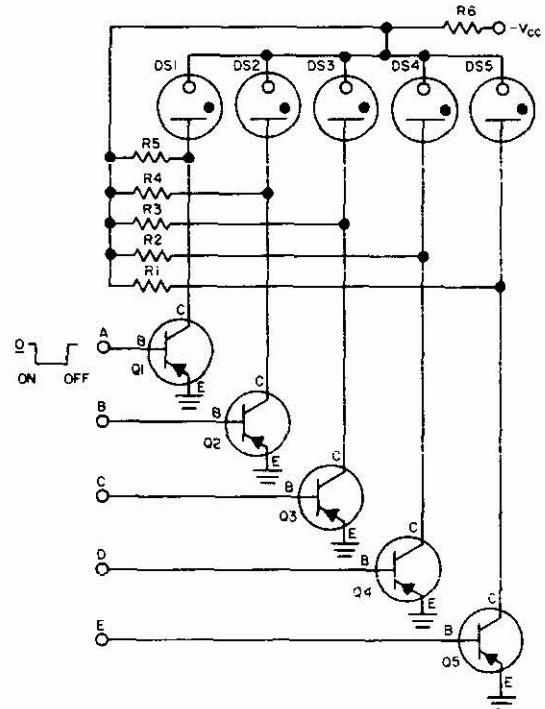
Usually provides a high input impedance and a moderate or low output impedance.

CIRCUIT ANALYSIS.

General. There are a number of circuits used to control the indicator lamps and relays used in computers and switching circuits. It is rather difficult to specify a basic circuit since there are so many variations. Therefore, a circuit capable of controlling high voltage and low current devices, and another one capable of controlling low-voltage, high-current devices are selected as typical circuits for discussion. The single transistor type of circuit usually requires that the trigger hold the stage in the "off" or the "on" state, whereas the two transistor circuit requires only an "off-on" trigger be applied to change its state. Since the advent of thyatron semiconductor devices, using pnpn four layer diodes or similar controlled rectifier devices, it is possible to have a single stage trigger itself in a "holding" condition until the shut-off trigger arrives. While it is also possible to use diodes for control elements, the transistor finds universal use since it may easily be "turned on" or "turned off" without elaborate circuitry.

Circuit Operation. The schematic for a typical high-voltage circuit capable of operating neon indicator lamps is shown in the accompanying schematic. The source of collector voltage is also used to supply the neon indicators. Each of the lamps is controlled by a separate transistor, and resistors R1 through R5 are collector voltage dropping resistors. Resistor R6 is a current limiter, and is also used to drop the lamp voltage during operation to avoid overload on the transistors. Normally, when no input is applied, the transistors rest in a cut-off state. No collector or emitter current flows (except that due to reverse current flow) and the neon indicator lamps remain out because they are only connected to one side of the line. The "cut-off" condition is obtained by leaving the transistor base floating, and applying reverse collector bias. Because there is no forward-bias, and the collector is reverse-biased no emitter current may flow. In the active state, a negative input signal is applied which produces a forward bias on the base of the activated transistor. Assume for the sake of discussion that Q1 is activated and that emitter current flows. Current flow through resistors R6 and R5 keep the collector voltage within transistor ratings, while heavy conduction to ground through Q1 offers a low resistance path for indicator lamp DS1. As long as the voltage across the lamp is high enough to ionize the lamp (55 to 65V for

neon), it is illuminated. Once illuminated, the lamp continues to glow until the voltage across it drops below 15 volts, or transistor Q1 stops conducting. When the forward bias is removed from the base of Q1 by turning off the trigger pulse, conduction through Q1 ceases, lamp DS1 is disconnected from ground, and is extinguished.

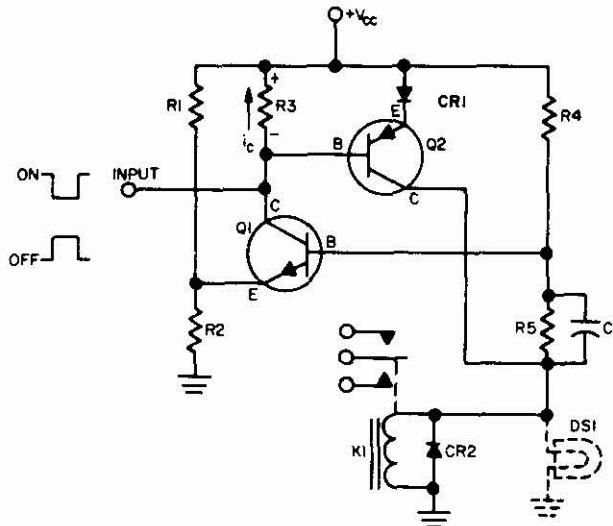


High-Voltage Neon Lamp Driver

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Each of the lamps may be illuminated by applying a negative trigger. Note that this circuit is designed for sequential operation of the lamps, and once conduction is produced in any lamp, the voltage across all lamps will drop to a low value (just above 15 volts) because of the shunting effect of the lamp being triggered. For parallel operation, R6 is eliminated and a separate resistor is connected in series with each indicator lamp, thus allowing the full source voltage to ionize each lamp when triggered.

A typical schematic of a relay puller or lamp driver circuit for low-voltage, high-current applications is shown in the accompanying illustration. Two transistors and a diode are employed in a bi-stable arrangement where the relay or lamp is turned on by a negative trigger and then held in that position until turned off by a positive trigger.



Relay Puller-Lamp Driver Circuit

Transistor Q1 is used to control Q2. Resistors R1 and R2 are emitter bias resistors, while R4 and R5 are base bias resistors for Q1. Bias values are such that in the "off" condition Q1 is held at cutoff, so no current flows through collector resistor R3. Thus the base of Q2 is held positive, which produces a reverse bias for the PNP transistor and prevents emitter current from flowing and actuating the relay or lamp. When a negative trigger is applied, the base of Q2 is driven negative and this forward bias causes emitter current flow through Q2 thereby operating relay K1 or illuminating indicator lamp DS1, whichever is used. In the quiescent condition, complementary NPN transistor Q1 is held in the nonconducting state because the base bias voltage produced across voltage divider R4 and R5 is smaller than the emitter bias produced by divider R1 and R2, thus the base is effectively reverse biased and Q1 does not conduct. Since relay K1, or lamp DS1, are connected in series with the base voltage divider consisting of R4 and R5, whenever Q2 conducts the voltage across this load raises the bias on Q1 base by a like amount and thus supplies a forward bias. With the forward bias con-

trolling Q1, it now conducts and produces a collector current flow through R3. Electron flow is in the direction which produces a negative drop across R3, which holds the base of Q2 in a forward biased condition, and keeps collector current flowing when the input trigger ceases. Operation is initiated by a negative trigger, causing Q1 to conduct, and, in turn, Q1 holds Q2 in the conducting state; this action continues until a positive trigger is applied to the input to turn it "off".

When a positive "off" trigger is applied to the base of transistor Q2, it momentarily produces a reverse bias, and causes Q2 to stop conduction. Immediately, the voltage developed across the relay or lamp by Q2 collector current flow drops to zero, and the base of transistor Q1 drops to a lower voltage (that produced across R5) than the emitter, to produce an effective negative or reverse base bias for the NPN unit. Thus conduction through Q1 is stopped, and both transistors rest in the cutoff state. Diode CR1 ensures that current may only flow in the proper direction and prevents initiation of a reverse current flow during switching operations. Diode CR2 operates as a discharge diode across the windings of relay K1, so that any transients caused by the inductive kick in the coil when it is turned off cannot harm the transistor. Capacitor C1 bypasses R5 so that any load change is reflected immediately as a bias change on the base of Q1, and produces quicker turn-on and turn-off operation.

FAILURE ANALYSIS.

High Voltage Circuit. Lack of supply voltage, too low a supply voltage, or a defective transistor or lamp will make the circuit inoperative. Check the supply voltage with a high resistance voltmeter, and the voltage from R6 to ground. The voltage at R6 should be 65 volts or more to ionize the lamps, and once they are ionized it may drop to about 15 volts. Measure the collector to ground voltage also with unit inoperative. An indication of almost the full supply value indicates the associated resistor (R1 through R5) is probably satisfactory. If no voltage exists from the collector to ground, the resistor is open and should be replaced. After the voltage measurements are made, if a lamp still will not illuminate when the appropriate trigger is applied, the transistor is defective and should be replaced (replace lamp if trouble persists).

Low Voltage Circuit. Failure of the transistors, diode CR1, and lack of supply voltage or improper bias can prevent the circuit from operating. With the circuit in the "off" condition the emitter voltage of Q1 should be larger than the base voltage and the collector of Q1 and base of Q2 should be almost the full supply voltage value. With normal voltages and the proper trigger applied, lack of circuit operation indicates that Q2 and possibly Q1 are defective. Replace them with known good ones. If the circuit still does not operate and the load is a relay, check diode CR2 with an ohmmeter for a short. If shorted the coil of the relay will be shunted out of the circuit and the relay cannot operate. If the circuit operates but does not hold until the next trigger resets it, check capacitor C1 for a short circuit. Use an ohmmeter or a capacitor checker.

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PART C. MECHANICAL CIRCUITS

SWITCH LOGIC.

Switch logic presents basically two states of action; that is, a switch is either **off** or it is **on**. Thus the connected circuit is either inactive or it is activated, and it can represent either the logic state of 0 or 1. When the switch is off, the circuit is not energized (no voltage or current is present), and it represents the inactive state of 0. When the switch is turned on, the circuit is energized (voltage or current is present), and it represents the active state of 1. The opposite condition may also be assumed, if desired.

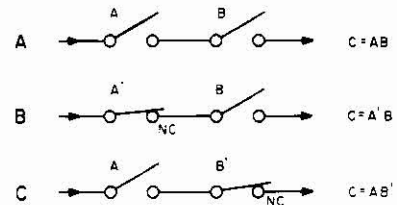
Actually, switching logic has been used for years prior to the advent of computers and logic circuits. For example, when lights at different locations are operated by one-way, two-way, or three-way switches, a form of elementary switch control logic is represented. Likewise, elevators have been controlled for years by instructions from switches located on different floors. Not only is the elevator started and stopped, it is directed to go up or down and to proceed to different floors. When called upon to operate in two different directions, it selects a sequence of operation and carries it out, in turn, as each command is sequentially followed in accordance with the basic design.

Basically, there are three forms of switching used in logic circuits; the manually operated switch, the mechanically operated switch, and the electromagnetically operated switch. Manually operated switches included knife switches, toggle switches, push-button switches, key switches, rotary switches, and many other variations. Mechanically operated switches are similar to manually operated switches, but are operated by mechanisms such as cams, linkages, hydraulic or pneumatic cylinders, and other means. These are generally used in analog computers where the state of some physical quantity is indicated when the quantity is at a maximum or a minimum, or as it reaches a series of predetermined values. The electromagnetically operated switch is simply a mechanical switch operated by the passage of electric current through a magnet coil. This type of switch commonly known as a relay, finds widespread use today, if an additional set of contacts is added, it can also be used to control another relay; thus numerous combinations of open and closed circuits can be contrived and automatically controlled to produce logic operations. Relays and switches used in logic circuits differ from the basic electrical relay in construction and size because they need not carry heavy currents or break high voltages; they are usually operated at very low currents and voltages. As normally constructed, the armature of the relay is held in the open position by spring action and closed by the magnetic attraction of the coil for the armature when current is applied. The contacts may be numerous, either normally open or normally closed, or the relay may consist of a stack of contacts containing various combinations. While the selection of the type of coil and relay is basically an engineering problem, the logical designer must be familiar with the types of contacts and coils available for efficient design. There are about five standard types of contact arrangements available (types A, B, C, D, and E which are make, break, break and make, make before break, and break

before make continuity-transfer, respectively). Similarly, there are about five different combinations of coils, such as the single coil, the two or more independent winding type, the two or more cooperative type (two or more windings must be energized simultaneously for operation), other combinations with holding windings, and differential types which can alternately energize or simultaneously de-energize the relay. Since this article is devoted to switch logic rather than component design, it is suggested that the interested reader obtain further data on relays and contacts by consulting manufacturers' catalogs containing design and operating specifications. Further mention of contacts and coils will be made only when pertinent to the logic design or circuit operation.

Let us now consider simple switch logic. First, it must be understood that in applying switch logic all operations are treated first in elementary form, that is, as simple make and break contacts. Later, after the logic is firmed up, the contacts are counted and various relay contact stack arrangements are considered in order to determine the minimum number and types of contacts and relays. This summation is known as **simplification**, which will be discussed later in the section.

Examine the simple series switching circuit formed by two relay contacts connected in series, as shown in the following figure. For simplicity, actuating coils are not



Series Switching Circuit

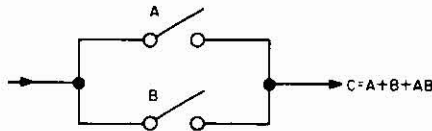
shown. Part A of the figure shows an elementary normally open circuit; when the coil of each contact is actuated, the relay switch is closed. Thus, in order for current to flow in the load circuit, coils A and B must both be actuated, thereby, closing contacts A and B and completing the circuit. If contact A is closed and contact B is open, no current flows. The same condition follows with B closed and A open (the closed condition is indicated by priming the contact, e.g., B' instead of B). With both contacts open a similar condition exists, so that one, and only one, condition will produce current flow into the load, namely when both contacts are closed. Let us tabulate these conditions using 0 to represent open contacts and 1 to represent closed contacts. Such a table, commonly called a **truth table** or a **table of combinations** is shown below. This truth table

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

AND Truth Table

is easily identified as the typical AND logic operation (multiplication). In part B of the figure, contact A is normally closed when the relay is de-energized, and, since it is closed it is represented in logic notation by priming the letter, thus making it A' (indicating "not" open) instead of A. Forgetting for the present whether the coils are energized or not, consider only the contacts. For each opening and closing combination the AND truth table still applies. A similar condition exists for part C of the figure, except that B' is the primed contact (normally closed). Thus, we may say in general that a series arrangement of relay contacts produces the AND logical function. The circuit of part A is simpler to comprehend and follow in logic design, since the circuit operates only to produce current when both relay coils are energized; in parts B and C only one relay need be energized at a time to produce the desired condition.

Consider now a parallel arrangement of contacts, as shown in the following figure. It is evident from an ex-



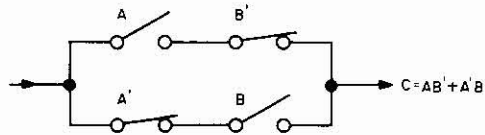
Parallel Switching Circuit

amination of the figure that current flows in the load circuit when either contact A or contact B is closed, or when both contacts A and B are closed. Note that current will flow when A is closed, regardless of whether B is closed, and vice versa. This action is indicated by logic notation as follows: $C = B(A + A') + A(B + B')$ which can be reduced to: $C = AB + A'B + AB + AB'$. As interpreted logically, this expression says that the load will draw current if A and B are closed, or if B is closed and A is not closed, or if A and B are closed, or if A is closed and B is not closed. Since $AB + AB = AB$, the expression for C may be simplified to: $C = A'B + AB' + AB$. A truth table for the preceding function follows: This table is

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Inclusive OR Truth Table

recognized as a typical OR table. Since it includes operation when A and B are both closed, it also represents the inclusive OR logic state. In general, then, we may say that parallel switching contacts represent the logic OR state (addition). The exclusive OR logic state is indicated when either A or B activate the circuit, but the circuit remains inactive when both A and B are operated. Such a condition is shown schematically in the following figure.



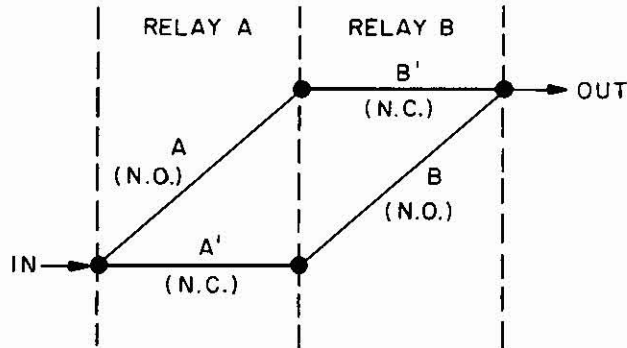
Exclusive OR Circuit

A truth table for the circuit above is shown below. It is recognized as the classic exclusive OR truth table, proving our contention that the schematic is that of the exclusive OR circuit by perfect induction.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive OR Truth Table

In addition to the schematic form of relay circuit drawings shown above, a kind of short-hand notation (diagram) is sometimes used, as shown in the following figure. In



Relay Logic Notation Diagram

this form of notation the horizontal lines represent normally closed (or primed) contacts, while the diagonal lines represent the normally open (or unprimed) contacts. The contacts shown in a particular column are all operated by the same relay. The figure illustrates relay logic notation as applied to the circuit of the series-parallel switch contacts representing the exclusive OR circuit shown by the preceding schematic. The abbreviations N.C. (normally closed) and N.O. (normally open), shown in parentheses in the diagram, are not normally included.

While this discussion of switching logic has presented the basic AND and OR switching circuits, the discussion is limited to logic concepts alone. The circuit action of specific logic circuits is discussed in the latter part of this section.

OR CIRCUITS.

APPLICATION.

The OR circuit is used in mechanical computers and switching circuits to perform logic addition.

CHARACTERISTICS.

May use positive, negative, or combined logic.

Consists of a series of switching contacts connected in parallel.

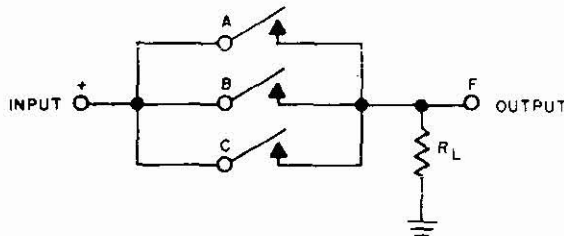
Performs logic addition.

Switch may be electrically or mechanically operated, usually consists of a group of relays.

No amplification is produced.

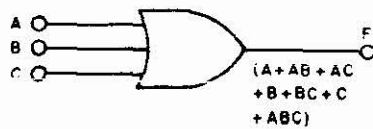
CIRCUIT ANALYSIS.

General. In switch logic, a basic OR circuit consists of a group of parallel connected single pole, single throw switches connecting the power source to the output load, as shown in the accompanying schematic.



Basic OR Switching Circuit

As can be seen from a study of the schematic, in the inactive condition all switches are open, and since the load and output are not connected to the power source there is no output, representing a logic 0. Conversely, when any of the switches are turned on, either separately or in combination, the power is connected to the load and the output voltage is the same as the input voltage, representing a logic 1. The logic diagram for this circuit is shown symbolically in the following illustration, with a truth table.



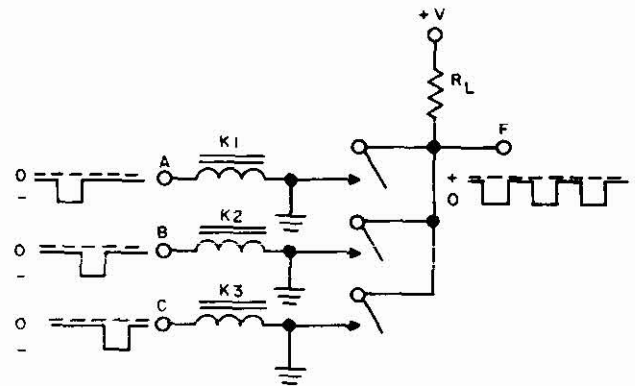
OR Logic Diagram

INPUTS			OUTPUTS
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Truth Table

From the symbolic logic diagram it is evident that there is no difference between the mechanical and electronic circuit, the symbol is functional. Since it is necessary to operate each switch by hand in the example given, and switches are not affected by polarity, the level indicators are omitted from the logic diagram. Because little advantage is obtained by requiring manual manipulation of the switches, the mechanical computer uses relays. Applying the proper potential to the relay coil pulls in the relay armature and closes the circuit. Thus by using another relay to control a series of switching operations, performed by groups of relays arranged in the proper switching sequence, electro-mechanical computers which operate at high rates of speed are formed. Speed of operation is limited by the time it takes the relays to open and close. Since relays are expensive and require more power and space than transistors or diodes, these types of computers find limited use.

Circuit Operation. The schematic of a typical relay-type of OR switching circuit is shown in the following illustration.

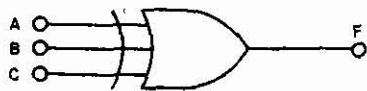


Three-Input OR Relay Circuit

The inputs are applied to the coils of relays K1, K2, and K3. When energized, these relays close and complete the circuit from the power source through common load resistor RL to ground. When no input signal is applied either A, B, or C, the circuit through the load resistor to ground is open, no current flows through RL, and the potential at the output is the relatively high positive level of the power source. Assuming a negative voltage (a positive voltage could also be used) representing a logic 1 is applied to input terminal A, relay K1 closes and the current flowing through RL to ground produces a voltage drop which lowers the output to the zero level. The output stays at the zero level for the duration of the input pulse and then returns to the normal high positive level when the input signal ceases and K1 opens. Thus, a negative output pulse is generated. If inputs B or C are activated the same sequence of operation occurs, except that relays K2 or K3 are energized instead of K1. In either case a negative output is developed. If two inputs are activated simultaneously, an output will

also be generated. This represents the case of the inclusive OR where the output is $A + B + C + AB + AC + BC + ABC$. This type of OR circuit allows several independent signals of different origins to perform the same switching function without any interaction between the signal sources. The relay in the OR circuit thus acts as a buffer or isolating element. To perform logic addition, this circuit must be used together with other OR or AND circuits arranged to produce the desired logic function. Should inversion or the NOR type of operation be desired, it is only necessary to control these relays with another relay, which when activated temporarily shorts the second relay coil causing it to deactivate. In this special case, the input signal does not produce an output signal.

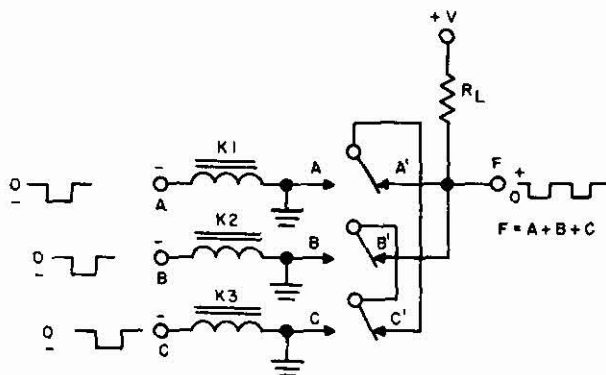
To accomplish the exclusive OR operation it is necessary to prevent operation of the other two relays when one of the relays is already activated. This is accomplished by adding a back contact on each relay which is normally closed. The logic symbol and truth diagram for this circuit is shown in the following illustration.



INPUTS			OUTPUTS
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

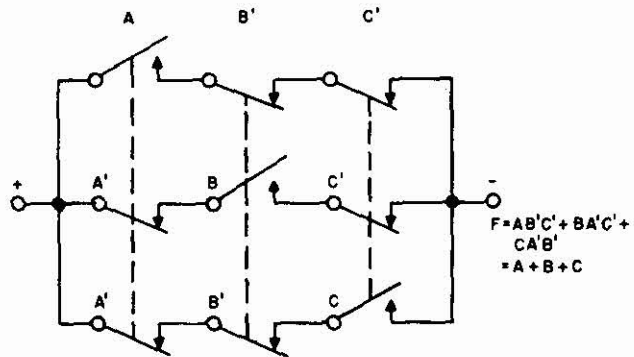
Exclusive-OR Logic Diagram Truth Table

In this instance, the logic symbol changes slightly to indicate that this is the **exclusive-OR** function and not the inclusive OR function. The circuitry, however, may be solid state, electron tube, or mechanical without change of symbol as long as the same function is achieved. The schematic of the mechanical exclusive-OR circuit is shown in the following illustration.



Exclusive-OR Relay Circuit

A simplified schematic of this circuit showing only the relay contacts is illustrated below to simplify the discussion. Note that for any circuit to produce an output, the other two relays must be resting in the normally closed position, as indicated by the primed symbols. Thus, when input A is activated, relay K1 closes and produces an output only if contacts B' and C' are closed.



Simplified Contact Arrangement

Likewise, when B is activated relay K2 closes and produces an output only if contacts A' and C' are closed. When C is activated, relay K3 closes and produces an output only if contacts B' and A' are closed. Since activating the relay opens the normally closed contact, whenever two relays are activated the circuit to the power supply, load, and output will be opened and an output cannot be produced. Thus, a negative pulse is generated only when one of the inputs is activated at a time, and never when more than one is activated simultaneously. Thus, the exclusive OR function is accomplished as shown in the truth table.

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FAILURE ANALYSIS.

Since a relay must be activated to produce an output, if there is no output, either the supply voltage is open, the relay coil is defective or open, or the relay contacts are defective or in need of cleaning. The relay can be observed and checked visually for operation by applying an external voltage to the coil. If the armature operates, then the fault must lie in the circuit controlling the relay, or in the relay contacts. The contacts can be checked by operating the relay manually, with a pencil, stick, or piece of insulating material (for voltages of 30 or more) and noting if there is an output when the armature is operated. If not, check the power source with a voltmeter to be certain sufficient voltage is present, and then follow through the circuit, looking for any normally closed contacts which may be open. Checking through the contacts can be quickly performed by using a voltmeter to measure the voltage from contact to ground.

In relay operation, knowledge of how the circuit operates is important for quick trouble shooting, since key relays may be manipulated manually to determine which portions

of the circuit are operating or are at fault. In this fashion, the failure can be quickly isolated to a particular group of relays or contacts.

AND CIRCUITS.

APPLICATION.

The AND circuit is used in mechanical computers and switching circuits to perform logic multiplication. It is sometimes called a coincidence circuit in other publications.

CHARACTERISTICS.

May use positive, negative, or combined logic.

Consists of a group of switching contacts connected in series.

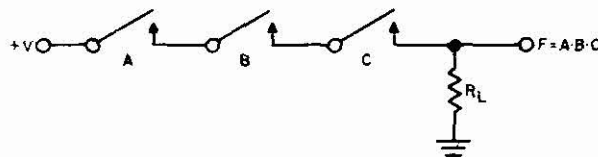
Switch may be mechanically or electrically operated, usually consists of a group of relays.

No amplification is provided.

Performs logic multiplication.

CIRCUIT ANALYSIS.

General. In switch logic, a basic AND circuit consists of a group of single pole, single throw switches connected in series, as shown in the accompanying schematic.



Basic AND Switching Circuit

As can be seen from the schematic, in the inactive condition all switches are open, and since the load and output are not connected to the power source there is not output, representing a logic 0. Conversely, when all the switches are turned on, the load is connected to the power source, and an output is developed across load resistor R_L by the current flowing through the circuit, representing a logic 1. The logic diagram for this circuit is shown symbolically in the following illustration, with a truth table.



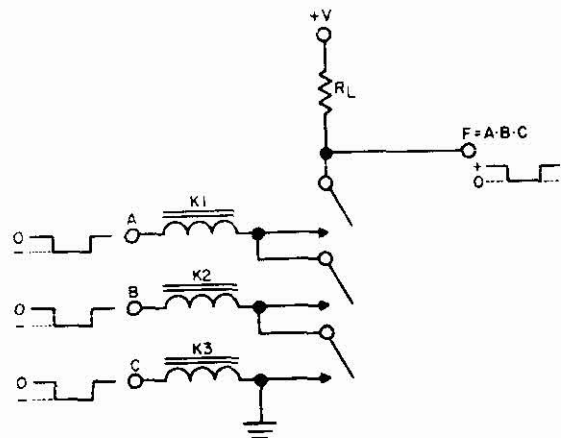
AND Logic Diagram

Truth Table

INPUTS			OUTPUTS
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

From the symbolic logic diagram, it is evident that there is no difference between the mechanical and electronic circuit, the symbol is functional. Since it is necessary to operate each switch by hand in the example shown, and switches are not affected by polarity, the level indicators are omitted from the logic diagram. Because advantage is obtained by requiring manual manipulation of the switches, the mechanical computer uses relays. Applying the proper potential to the relay coil pulls in the relay armature and closes the circuit. By using one relay to control a series of switching operations performed by groups of relays arranged in the proper switching sequence, electro-mechanical computers which operate at high rates of speed are formed. Operating speed is determined by the time it takes the relays to open and close (from 1 to milliseconds on the average). Since relays are expensive and require more power and space than transistors or diodes, these types of computers find limited use.

Circuit Operation. The schematic of a typical relay-type of AND switching circuit is shown in the following illustration.



Three-Input AND Relay Circuit

The inputs are applied to the coils of relays K1, K2, and K3. When closed, these relays connect common load resistor R_L to ground. In the deenergized position, the load circuit and output float at the supply voltage, and this high positive output level is considered to represent a logic 0. When all three inputs are activated simultaneously, relays K1, K2, and K3 close and connect the load resistor and output to ground. The high positive output voltage is dropped to zero by the current flowing through the load resistor and the output is effectively a large negative-going pulse. For the duration of the input signal or pulse, the output remains at zero and then rises to its normal high positive level when the input terminates, completing the negative output pulse.

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Because of the series arrangement of relay contacts the circuit is only completed when all contacts are closed. Thus, as shown in the truth table previously, all outputs are zero, except when all the inputs are simultaneously activated to produce a "one" signal.

FAILURE ANALYSIS.

Loss of supply voltage, an open load resistor, or defective relay can cause lack of output. Checking the voltage from the output to ground with a high resistance voltmeter and no input signal will determine if source voltage exists, and if the load resistor has continuity. Now apply an input signal to each relay, K1, K2, and K3 in turn, and observe that they operate. If the relays operate and no output is obtained with all inputs simultaneously activated, the relay contacts must be defective. Clean the contacts and adjust the spring tension for a satisfactory contact. If no voltage is obtained in the inactive state when measuring from output to ground, but the source voltage is normal, load resistor RL is open and should be replaced.

When cleaning relay contacts use a burnishing tool and avoid use of sandpaper or files to prevent removal of excess contact material. If the contacts are excessively pitted replace them with new contacts. Dirty contacts may be cleaned with approved electrical solvent. Apply a drop to a toothpick, clean the contact, allow it to dry and dress with a burnishing tool.

FLIP-FLOP CIRCUITS.

APPLICATION.

Relay type flip-flop circuits are used in mechanical computers and switching circuits to supply off-on triggering pulses and provide a signal and its complement simultaneously, they are also used as storage elements. It forms the basic circuit used in most registers.

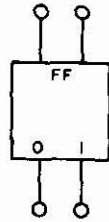
CHARACTERISTICS.

- May use positive, negative, or combined logic.
- No amplification is produced.
- Consists of two operating and two control relays.
- Provides two output signals (one is the inverse of the other).
- Usually requires two inputs (an "off" trigger and an "on" trigger).

CIRCUIT ANALYSIS.

General. The relay type of flip-flop is the mechanical switching equivalent of the transistor or electron tube bistable multivibrator (it is sometimes known as a "toggle switch" circuit). It has two stable states, one the inactive or zero-state, and the other the active or one-state. Once triggered, one relay is held in the active position until it is released, meanwhile the other relay rests in the inactive condition until a trigger appears. Thus, this type of cir-

cuit provides a limited amount of storage. It will retain either a zero or a one indefinitely, and without attention, until it is triggered into the opposite state of operation. The logic diagram for this circuit is shown symbolically in the following illustration, together with a truth table.



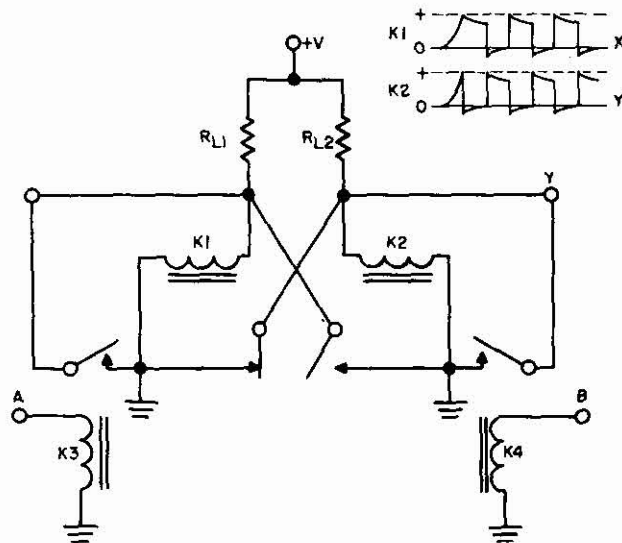
INPUTS		OUTPUTS	
A	B	X	Y
0	1	0	1
1	0	1	0

Flip-Flop Logic Diagram Truth Table

It is evident there is no difference in the logic symbol between electronic and mechanical flip-flops, since the symbol is functional. When the symbol bears the designations C and S on the unidentified leads it indicates a clear (reset) input for C and a set input for S. The clear input always returns the flip-flop to the zero or inactive state, while the set input always triggers the flip-flop into the active or one condition. It is not necessary to label these inputs, but they may be labelled, if desired.

Circuit Operation. The schematic of a typical relay flip-flop is shown in the accompanying illustration. The outputs are X and Y, and the inputs are A and B which operate control relays K3 and K4. The flip-flop operating relays are K1 and K2.

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Relay Flip-Flop Circuit

When no power is applied, both relays K1 and K2 rest in the deenergized position and no output is produced. When power is applied, both relays will try to close since their coil is connected between the power source and ground. The first relay to close will lock out the other relay and prevent it from closing, and the circuit will rest in one of the two possible conditions. Assume for the moment that relay K1 is closed, then relay K2 is open and output Y is connected to ground via the contacts of K1. Current flow to ground through RL_2 will drop the voltage at terminal Y to zero and simulate a 0. Meanwhile, RL_1 and the coil resistance of K1 form a voltage divider from +V to ground, and output X will be a positive voltage determined by the ratio of the resistances in the voltage divider, but is always less than the supply voltage. As long as K1 remains closed, the X output will be a positive voltage representing a 1. When input A is activated by a "set" signal, relay K3 closes and grounds the coil of K1 by shunting it to ground and causing K1 to open. As soon as K1 opens, current flow through RL_2 and the coil of K2 to ground pulls in relay K2. The output of terminal X is now 0, since it is grounded, while the Y output is the voltage developed across K2 coil (K2 and RL_2 form a voltage divider between +V and ground). The conditions are now exactly reversed, and the Y output is a positive voltage less than the source value, while the X output is 0. When a "clear" pulse is applied to relay K4 by energizing B input terminal, relay K2 is shorted out and K1 operates and resumes control. Thus the flip-flop may be made to change state by alternately energizing control terminals A and B. (The trigger is only momentary it is not continuous). As a result, the flip-flop produces two outputs, one the inverse of the other as shown in the waveforms, and will rest in one state until triggered into the opposite state.

Circuit arrangements may be made to produce negative output voltages if desired, and the control relays may be triggered by either positive or negative voltages, since the relays are not polarized. The output voltage will be determined by the values of relay coil resistance and load resistance used for a specific source voltage and will never exceed the source, except possibly for the switching transients shown by the pips on the output waveforms. With proper design these transients can be practically eliminated.

FAILURE ANALYSIS.

If any relays are defective, or the load resistor(s) are open, either no output or an improper output will be obtained. Operation of control relays K3 or K4 can be checked visually to determine if they close when a pulse is applied. Operation of relays K1 and K2 can also be checked by using a pencil or piece of insulation to mechanically close the armature and observe if the other associated relay drops out. If mechanical operation causes proper outputs and functioning to occur, either the relay coil involved is open, or the contacts are dirty and offer a high resistance path to ground. Clean the contacts, and if the trouble persists replace the relay. If both load resistors are open, no output will be obtained even though the relays operate properly (if only

one is open a single output will be obtained). Check the source voltage to ground with a voltmeter, and the coil to ground voltage. Knowing the proper resistance division between them will enable you to determine if they are operating normally by means of a voltage check. For example, if the load resistance is 10 times that of the relay coil, the relay voltage should be 1/11th of the source voltage ($10 + 1$). In mechanical relay operation the simplest and quickest method of trouble shooting is to manually operate the relays, and locate one which does not produce the proper result. The trouble then exists in the circuit controlled by this relay. If none of the relays seem to operate properly, the power source is at fault, since it is the only part of the circuit common to all relays. Thus it can be appreciated that a clear understanding of how the circuits operate is necessary to intelligently service multiple relay equipments.

TWO-WAY AND THREE-WAY CIRCUITS.

APPLICATION.

Two-way and three-way circuits are used in computers and switching devices to apply to outputs of two or three other logic circuits to the input of a single logic circuit, and control its output.

CHARACTERISTICS.

May use positive, negative, or combined logic.

Uses combinations of OR and AND circuits.

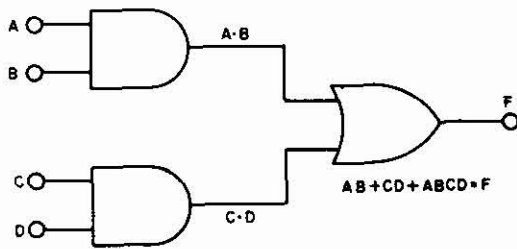
Has a number of inputs, but only a single output.

CIRCUIT ANALYSIS.

General. Two-way and three-way circuits provide a means of combining logical operations so that the result can be handled by simple off-on switching circuits. Combinations of AND and OR gates offer a convenient and easy method of fanning-in a large number of inputs to a single output line. Besides being convenient for binary and digital use they are also useful for control functions. For example, if it is necessary for three switches to be placed "on" before another switch can be operated, a simple three-input AND circuit will control this operation. Likewise, the turning on of a transmitter from two separate locations is accomplished by a simple OR gate. In digital logic it is the arrangement of these two-way and three-way circuits (or four- or five-way circuits) which form the arithmetical or logic circuit used as an adder or subtractor, or otherwise to produce the desired function(s).

Circuit Operation. A basic two-way circuit consisting of two AND gates and an OR gate is shown in the following logic diagram.

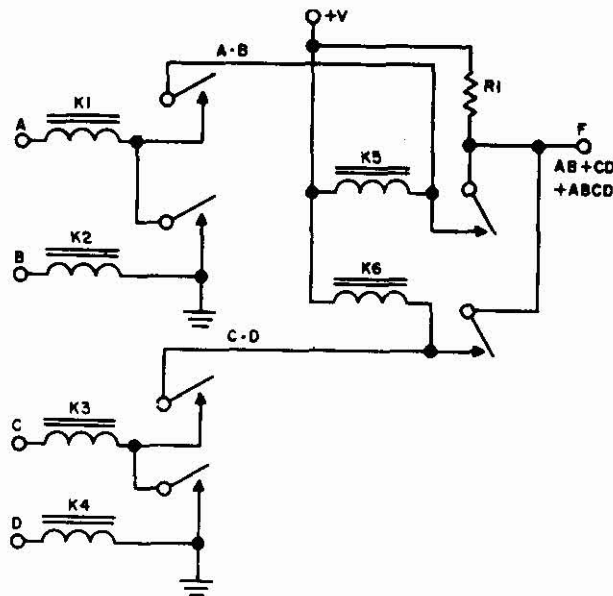
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Two-Way Circuit Logic Diagram

Note that the logic diagram is functional and does not indicate the actual circuit, so that diodes, transistors, relays or switches could be used as long as the proper function was performed. Note also, that the actual circuit diagram or schematic is not needed in understanding circuit logic. When inputs A AND B exist the first AND gate produces output AB. Likewise, when inputs C AND D exist the second AND gate produces output CD. These inputs can be at two different levels and supplied from separate logic circuits. When either input combination is applied to the OR gate a single output is produced, and, since it also represents the inclusive OR function, when both combinations simultaneously exist an output is also produced from the OR gate. Thus the output of this circuit is $AB + CD + ABCD$, and the two level input is expressed as a single-level output.

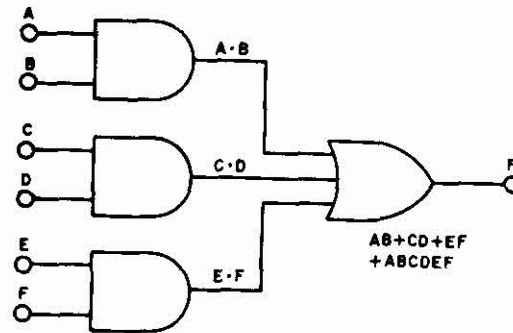
A typical schematic diagram using relay switching to accomplish the logic explained above is shown in the accompanying illustration.



Two-Way Circuit Schematic

Relays K1 and K2 form one AND gate, while relays K3 and K4 form the other AND gate. Both AND gate relay contacts are connected in series to ground, and actuate relays K5 and K6 of the OR gate when appropriate inputs are applied. When either K1, K2, K3, or K4 alone are actuated, the circuit to ground for the OR gate relay coil is open since only one set of contacts is closed. However, when both K1 and K2, or K3 and K4, or all relays are activated simultaneously, the OR gate is activated. Therefore, when an output such as AB is obtained from the AND gate by closing relays K1 AND K2, relay K5 is closed and output F is at ground potential. Normally, with K5 and K6 open, output F is at a high positive level since no voltage drop occurs across R1. However, when K5 AND K6, or K5, or K6 is closed, current flow to ground through R1 drops the output to zero. When these relays are released, output F again assumes a high positive level. Thus the OR gate output effectively is a negative pulse representing a 1, and negative logic is employed.

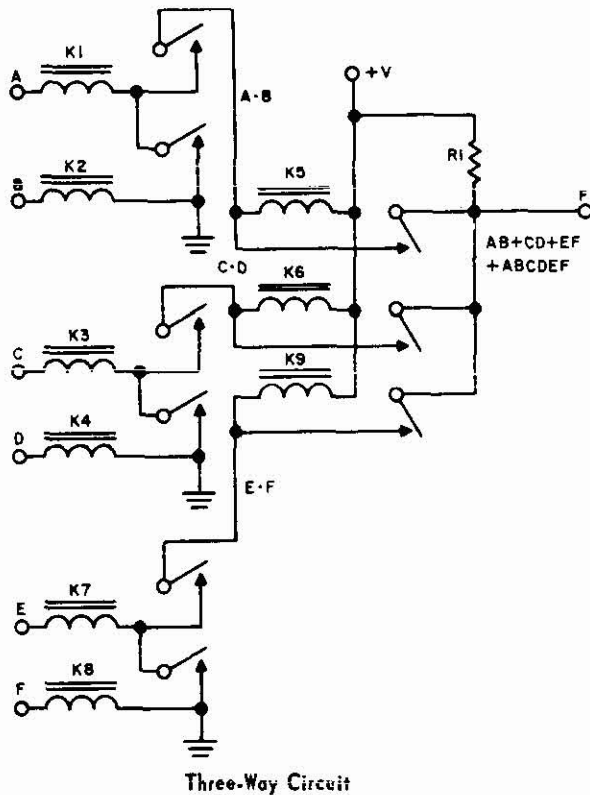
A three-way or three-level logic circuit merely provides an additional input level over the two-way circuit. Therefore, by adding another AND circuit as shown in the accompanying logic diagram, a three-way circuit is obtained.



Three-Way Circuit Logic Diagram

Examination of the new logic diagram reveals that when input A AND B exist, the first AND gate produces output AB. Similarly, when inputs C AND D are present the second AND gate produces output CD; and finally, when inputs E AND F are present, the third AND gate produces output EF. When any of the AND gate outputs are applied to the OR Gate input a single output is produced. Since, this circuit also includes the inclusive OR function, when all combinations simultaneously exist an output is also produced from the OR gate. Thus the output of the three-way circuit is $AB + CD + EF + ABCDEF$, and the three-level input is expressed as a single-level output. The schematic diagram for the three-way circuit is shown in the accompanying illustration, using relay switching to accomplish the logic indicated and explained above.

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Relays K1, K2, K3, and K4 operate identically with the previously described two-way circuit and the new relays K7 and K8 have their contacts connected in series to ground, controlling new OR gate relay K9. Since the contacts of K9 are connected in parallel with those of K5 and K6, operation of the OR gate drops output F to zero level when K9 is closed. Therefore, when relays K7 and K8 are simultaneously activated, relay K9 is closed, producing an effective negative output for a logic 1.

FAILURE ANALYSIS.

Check the output with a voltmeter, normally it should indicate a relatively high positive voltage to ground, if not, the power supply source is at fault or resistor R1 is open (check R1 with an ohmmeter when in doubt). Apply inputs to terminals A and B, C and D, and EF, meanwhile observing that relays K5, K6, and K9, respectively, are actuated. The output should drop to zero when relay K5, K6, or K9 are actuated, if not, the associated relay contacts may be dirty. If they are sufficiently dirty to produce a poor contact and high resistance, the output voltage will not be zero, but will be some intermediate value depending upon the resistance of the contacts. Each of the relays can be checked manually, by operating it with a pencil or insulating rod (for voltages over 30 volts) to quickly determine which relay or group of contacts are not functioning. By proceeding from output to input, a fewer number of contacts

are checked out first. When the circuit functions under manual operation but not under normal operation, the relay coil is defective and the relay or coil should be replaced.

SIMPLIFICATION PRINCIPLES.

APPLICATION.

Simplification is used to reduce the number of logic or switching circuits necessary to obtain a desired functional result.

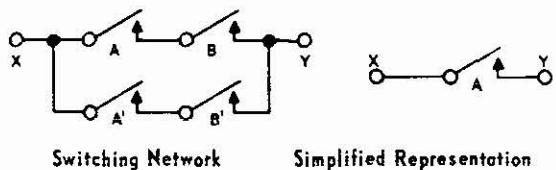
CHARACTERISTICS.

- Circuit is reduced to simplest form.
- Unnecessary or excessive components are eliminated.
- Usually employs Boolean Algebra.
- Function is not changed.

CIRCUIT ANALYSIS.

General. The process of simplification is generally to reduce any given circuit to its simplest form without changing the logic. This is accomplished by eliminating unnecessary switches or by substituting one switch for duplicate switching. There are two basic methods which can be used; the first method involves pure reasoning, while the second method uses the mathematical manipulations of Boolean Algebra to reduce the unsimplified expression to its simplest form. Examples of each method will be given. Since simplification and the intricacies of Boolean logic are mainly of use to the logic designer, and the equipment encountered in Naval use will already be in simplified form, the subject is only briefly discussed in this Handbook in elementary form. For more information on this subject the interested technician should consult the text books on logic design available from commercial sources and public libraries.

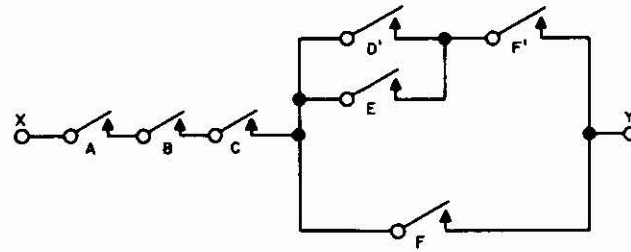
Procedures. A simple switching circuit involving AND and OR operations is shown in the accompanying illustration, with its simplified equivalent.



Since switch NOT B (B') is normally closed, while switch B is normally open, the path from X to Y will always be completed when switch A is closed. Thus both B and B' switches may be removed and a closed wire connection made between switch A and output Y, leaving switch A as the only one in the circuit. When represented in Boolean notation, multiplication of A AND B or A AND B' is indicated because of the series ANDing of the switches, and the summing of these quantities is also indicated because of the parallel connection (ORing) of switches.

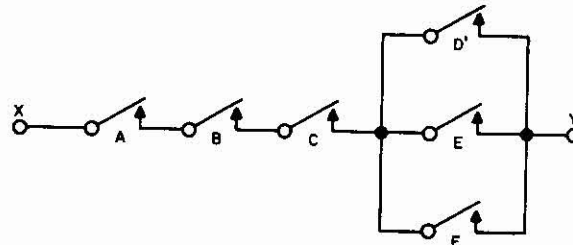
Thus the original expression is $(A \cdot B) + (A \cdot B')$. If we factor A from both terms we can rewrite the expression as $A \cdot (B + B')$. However, the quantity $(B + B')$ is equal to 1 by the first law of complementation in the Boolean postulates. Therefore, we write expression as $A(1)$ which is equal to A, proving the simplified version and reasoning are correct.

Let us now take a more complex switching arrangement where it is desired that point X be connected to point Y through independent elements A, B, C, D, E, AND F, as shown in the accompanying illustration.



Second Simplification

Finally, we may reason that switch F provides an independent path, which if F is open has an alternative path offered through D' or E AND F'. Therefore, D' and E may be directly wired to Y and F' disposed of. Thus the final circuit version is obtained as shown below, consisting of an AND gate feeding an OR gate.



Final Simplification

By elementary reasoning the 13 switch circuit is reduced to 6 switches and retains the original desired function. This is proven with Boolean algebra as follows. The overall expression for the unsimplified network is:

$$A(A' + BC) [(D' + E) \cdot C \cdot F' + DA'F + BF] = F,$$

and $F = 1$

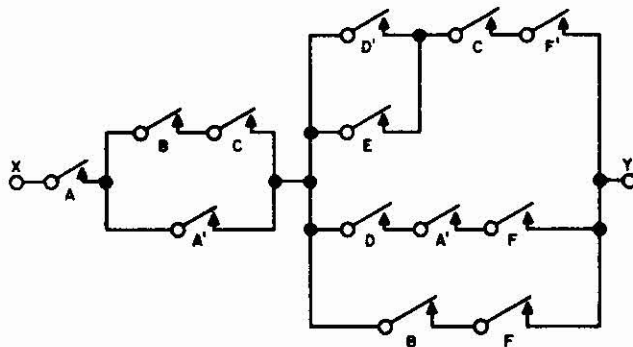
Combine the terms in the following manner:

$$(AA' + ABC) [D'CF' + ECF' + DA'F + BF] = F$$

since AA' in the first expression is equal to 0, therefore

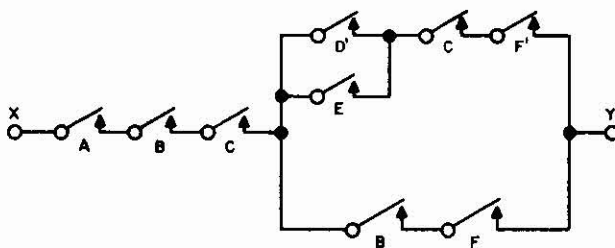
$$(ABC) [D'CF' + ECF' + DA'F + BF] = F$$

and we have by further combining



Complex Switching Circuit

We may now reason as follows. Since switch A' is normally closed and any path between X and Y must have switch A closed, switch A' will always be open and may be eliminated to produce the simpler circuit shown below.



First Simplification

Note that the circuit now consists of a series group of switches forming an AND circuit, and feeding a group of series and parallel switches. Further simplification is desirable. Since B and C switches must be closed for the AND gate to operate, duplicate switches B and C may be eliminated and wired across, producing the second simplified circuit shown below.

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$$ABCD'F + ABCEF' + AA'BCDF + ABCF = F$$

but AA' in the third term is equal to 0 eliminating the term, and

$$ABCD'F + ABCEF' + ABCF = F$$

combining the last two terms gives

$$ABCD'F' + ABC(F + F'E) = F$$

since $F + F'$ equals 1 we have

$$ABCD'F' + ABC(F + E) = F$$

eliminating the parentheses we get

$$ABCD'F' + ABCF + ABCE = F$$

combining the first two terms gives

$$ABC(F + F'D') + ABCE = F$$

since $F + F'$ equals 1 we have

$$ABC(F + D') + ABCE = F$$

recombining terms we get

$$ABCF + ABCD' + ABCE = F$$

which can be written as

$ABC(F + D' + E) = F$, which agrees with the final simplification

arrived at by a simple reasoning.

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