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TECHNICAL MANUAL

for

RADIO TRANSMITTING SET AN/FRT-24A

DEPARTMENT OF THE NAVY

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SECTION 4

TROUBLE SHOOTING

4-1. LOGICAL TROUBLE SHOOTING.

a. GENERAL. - Certain techniques are very useful when trouble shooting the radio set. The first step is to check front-panel controls and indicators in an effort to localize the trouble. Check all test meter indications for every test meter switch position on applicable units and compare the results with the normal indications listed in tables 3-11 through 3-15. Begin the search for the cause of a trouble with a thorough inspection of the power supply units. Measure the voltages at all power supply front-panel test points. If a voltage reading is outside the specified limits, proceed to localize the cause to a defective assembly or part within the defective power supply. If all the power supply output voltages are normal, proceed to check each unit comprising the radio set. If the trouble is caused by improper synthesizer outputs, check the 1-MC frequency standard in the amplifier because it is a likely cause of this trouble. If the 1-MC frequency standard is found to be operative, check the internal circuits of the synthesizer by using its built-in test facilities. Table 4-1 is a cross reference index of the trouble shooting and maintenance paragraphs.

If the trouble is present while operating in the automatic mode, change to manual operation and observe results. If the trouble is eliminated, it is probably caused by a defective autotune system or switching assembly and all subsequent trouble shooting should be in this area. If the trouble persists, follow the instructions given in this section to localize and remedy the cause.

b. SYMPTOM RECOGNITION. - This is the first step in the trouble-shooting procedure and is based on a complete knowledge and understanding of equipment operating characteristics. All equipment troubles are not the direct result of component failure and all conditions of less than peak performance are not always apparent. Therefore, a trouble in an equipment is not always easy to recognize. This type of equipment trouble is usually discovered while accomplishing preventive maintenance procedures, such as the POMSEE checks. It is important that the "not so apparent" troubles, as well as the apparent troubles, be recognized.

c. SYMPTOM ELABORATION. - After an equipment trouble has been "recognized", all available aids designed into the equipment should be used to further elaborate on the original trouble symptom. Use of front-panel controls and other built-in indicating or testing aids should provide better identification of the original trouble symptom. Also, checking or otherwise manipulating the operating controls may eliminate the trouble.

d. LISTING PROBABLE FAULTY FUNCTION. - The next step in logical trouble shooting is to formulate a number of "logical choices" as to the cause and likely location (functional section) of the trouble. The "logical choices" are mental decisions which are based on knowledge of the equipment operation, a full identification of the trouble symptom, and information contained in this manual. The overall functional description and its associated block diagram should be referred to when selecting possible faulty functional sections.

e. LOCALIZING THE FAULTY FUNCTION. - For the greatest efficiency in localizing trouble, the functional sections which have been selected by the "logical choice" method should be tested in an order that will require the least time. This requires a mental selection to determine which section to test first. The selection should be based on the validity of the "logical choice" and the difficulties in making the necessary tests. If the tests do not prove that functional section to be at fault, the next selection should be tested, and so on until the faulty functional section is located. As aids in this process, the manual contains a functional description and a servicing block diagram for each functional section. Waveforms (or other pertinent indications) are included at significant check points on servicing block diagrams to aid in isolating the faulty section. Also, test data (such as information on control settings, critical adjustments, and required test equipment) are supplied to augment the functional description and servicing block diagram for each functional section.

f. LOCALIZING TROUBLE TO THE CIRCUIT. - After the faulty functional section has been isolated, it is often necessary to make additional "logical choices" as to which group of circuits or circuit (within the functional section) is at fault. Servicing block diagrams for each functional section and individual functional circuit groups (when required) provide the signal flow and test location needed to bracket and then isolate the faulty circuit. Functional descriptions, simplified schematics, and pertinent test data for individual circuits or groups of circuits comprising the functional section are all placed together in one area of the manual.

g. FAILURE ANALYSIS. — After the trouble (faulty component, misalignment, etc.) has been located (but prior to performing corrective action), the procedures followed up to this point should be reviewed to determine exactly why the fault affected the equipment in the manner it did. This review is usually necessary to make certain that the fault discovered is actually the cause of the malfunction, and not just the result of the malfunction.

4-2. RADIO TRANSMITTING SET AN/FRT-24A, OVERALL FUNCTIONAL DESCRIPTION.

a. Radio Transmitting Set AN/FRT-24A (see figure 4-1) is a general purpose, quick shift, remotely controlled single sideband radio transmitter which operates over the 2- to 30-MC frequency range. The transmitter covers this range in eight bands. The transmitter can operate in any of five modes of emission: continuous wave telegraph (CW, A1); amplitude modulated telephony (compatible AM upper sideband with carrier, A3a); double sideband (two independent sidebands, A3b); single sideband (upper or lower sideband suppressed carrier, A3j), and frequency shift keying (FSK, F1). Mode and frequency selection can be accomplished automatically by dialing the correct sequence on a telephone-type dial switch at the transmitter controls during remote operation, or manually by operating the appropriate front-panel controls and switches. Automatic antenna programming is also provided.

b. The RF carrier signals are generated in synthesizer 1A6. The synthesizer produces main output signals in the 17.75- to 35.6-MC frequency range and auxiliary signals of 1.75 MC and 100 KC. The synthesizer outputs are locked to a stable (1 part in 10^8 per day) 1-MC frequency standard signal generated in amplifier 1A2. Provisions are incorporated, at the bottom of the right-hand rack, for direct connections of an external 1-MC or 5-MC reference signal. The three synthesizer outputs are applied to converter 1A3. The 17.75- to 35.6-MC input to the converter is properly divided to produce the transmitter operating frequency range of 2 to 30 MC. The 1.75-MC input to the converter is applied to two balanced modulators; one for the upper sideband and the other for the lower sideband. Each balanced modulator also receives the applicable upper or lower sideband speech or keying signals from the amplifier. The modulated 1.75-MC output of each balanced modulator is applied to two separate sideband combiners. The outputs of the combiners are applied to a balanced mixer together with the 2- to 30-MC carrier frequency. The modulated carrier frequency is amplified and applied through patch panel 1A13A3, to RF assembly 1A8 for final amplification and eventual application to the antenna.

c. Amplifier 1A2 receives mode selection information and provides the required speech or keying signals to converter 1A3. During remote operation, the mode selection and speech or keying signals are supplied to the amplifier from transmitter controls 2 and 3. During local operation, all speech signals are produced in the amplifier in accordance with the selected mode of emission. Two front-panel audio voltmeters continuously monitor the level of modulating signals applied to the converter.

d. Tuning, mode selection, and frequency selection can be accomplished automatically or manually. During remote automatic operation, control of the transmitter is from the transmitter controls. Automatic tuning is achieved by a single motor in the autotune system of RF assembly 1A8 which responds to dial pulse information from the transmitter controls through dial control 1A1. The motor operates a series of single turn drive heads which operate the various controls accordingly. Automatic mode selection is accomplished by a series of relays in the converter, amplifier, transmitter cabinet and dial control, which activate in response to the dial pulse information. Automatic frequency selection is accomplished at the transmitter controls by dialing the correct sequence for the desired frequency channel. Selection of any 10 preset frequencies (channels) can be achieved in this manner. Visual indication of the selected channel is provided at the synthesizer front panel. During local automatic operation, channel selection is made by a front-panel switch on the RF assembly. Remote/local selection is made at power control 1A9. During manual operation, the automatic system is de-activated and the transmitter tuning, mode, and frequency selection is accomplished by proper operation of the front-panel controls and switches.

e. Operating and control voltages are provided by four separate power supplies. Exciter power supply 1A7 supplies DC, filament, and control voltages to amplifier 1A2 and converter 1A3. Synthesizer power supply 1A4 supplies operating voltages to synthesizer 1A6. LV supply 1A11 provides +620 VDC and +83V to the low level stages of RF assembly 1A8, and HV supply 1A10 provides +3000 VDC and +630 VDC to the high level output stages of the RF assembly. Forced air cooling of the high level stages is provided by the blower. Power control 1A9 applies the primary input power to the HV supply, LV supply, blower and service supply. The service supply applies power to the synthesizer and exciter supplies. The power control also supplies power to the autotune system in the RF assembly and provides facilities for selecting remote or local operation.

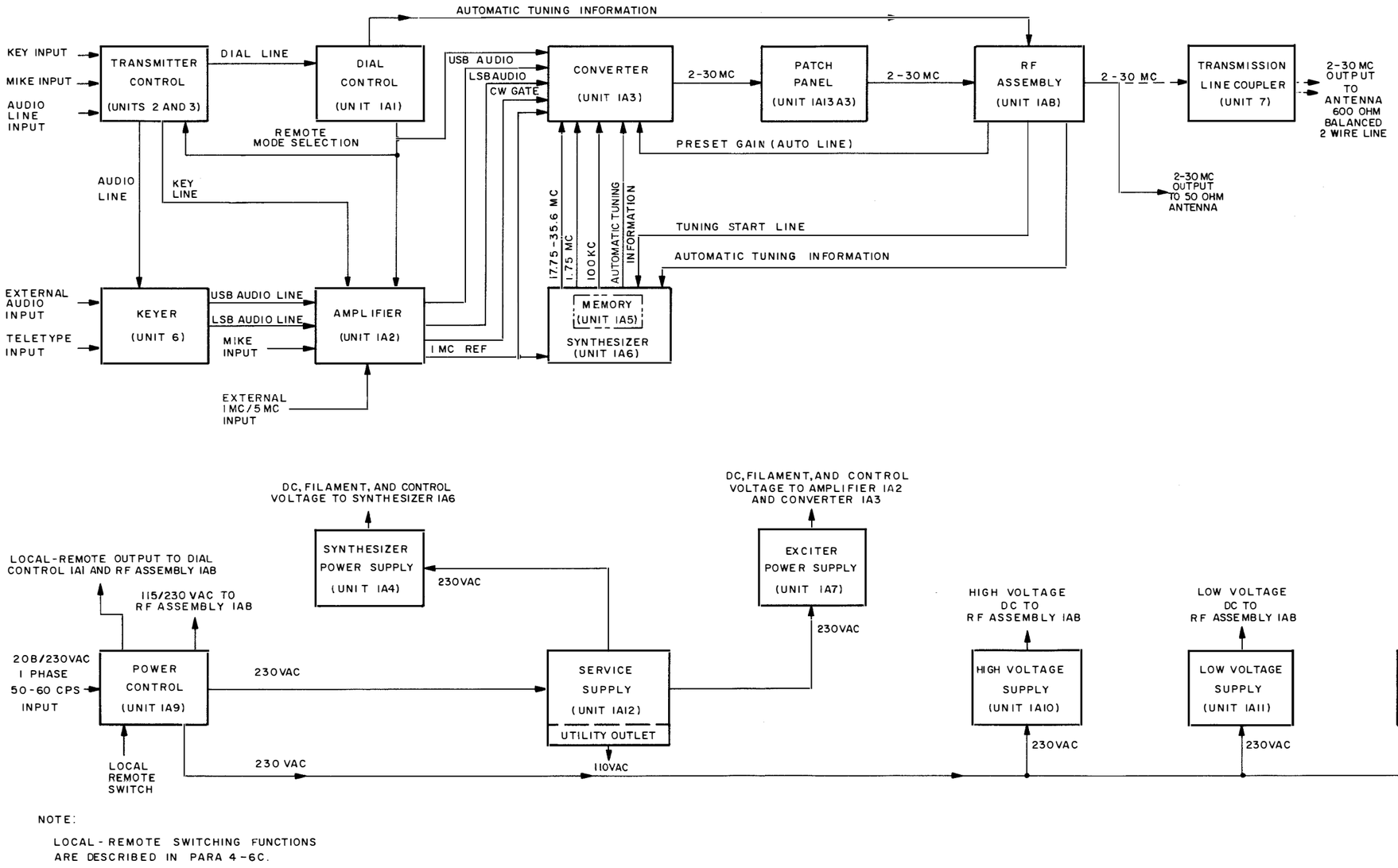


Figure 4-1. Radio Transmitting Set AN/FRT-24A, Overall Functional Block Diagram

TABLE 4-1. REFERENCE DESIGNATION INDEX

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1	Transmitter, Radio T-973/FRT-24A	Transmitter	5-163	5-141 to 5-146	--	4-6	--
1A1		Dial control	5-167	5-34	--	4-6c	--
1A2	Amplifier, Audio Frequency AM-4242/FRT-24A	Amplifier	--	--	--	4-4	4-71
1A2A1		Amplifier inner case	5-168	5-35; 5-36 5-37	5-4	--	4-71
1A2A2		Amplifier outer case	--	5-51	--	--	
1A2A1A1		AGC and audio amplifier assembly	5-170	5-38	--	4-4c(3)	4-71
1A2A1A2		Audio voltmeter assembly	5-171	5-39	--	4-4c(5)	4-71
1A2A1A3		CW assembly	5-172	5-40	--	4-4c(7)	4-71
1A2A1A4		AGC and audio amplifier assembly	5-170	5-38	--	4-4c(3)	4-71
1A2A1A5		Audio volt meter assembly	5-171	5-39	--	4-4c(5)	4-71
1A2A1A6		Voltage regulator assembly	5-173	5-41	5-4a	4-4d(7)	4-71

TABLE 4-1. (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1A2A1A7	Ampifier, Audio Frequency AM-4242/FRT-24A (cont)	Phase detector assembly	5-174	5-42, 5-43	5-4b	4-4d(5)	4-71
1A2A1A7A1		Squelch and emitter follower assembly	5-174	5-44	--	4-4d(5)	4-71
1A2A1A7A2		1-MC oscillator assembly	5-174	5-45	5-4b	4-4d(3)	4-71
1A2A1A7A3		Phase detector assembly	5-174	5-46	5-4b	4-4d(5)	4-71
1A2A1A8		1-MC oscillator assembly	5-175	5-47, 5-48	5-4c	4-4d(3)	4-71
1A2A1A8A1		1-MC oscillator subassembly	5-175	5-49	--	4-4d(3)	4-71
1A2A1A9 thru 1A2A1A13		Audio attenuator assemblies	5-176	5-50	5-4d	4-4c	4-71
1A3	Converter, Amplitude-Single Side-Band CV-1846/FRT-24A	Converter	--	--	--	4-5	4-72
1A3A1		Converter inner case	5-177	5-52 to 5-55, 5-69	5-5	--	

TABLE 4-1. (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1A3A2	Converter, Amplitude-Single Band CV-1846/ FRT/24A (cont)	Converter outer case	--	5-69	--	--	--
1A3A1A1		Frequency offset and band selector assembly	5-179	5-56	--	4-5b	4-72
1A3A1A2		Binary divider assembly	5-180	5-57	--	4-5d	4-72
1A3A1A3		Balanced modulator and crystal filter assembly	5-181	5-58, 5-59	5-5e	4-5h	4-72
1A3A1A4		IF amplifier assembly	5-182	5-60, 5-61	5-5d	4-5j	4-72
1A3A1A4A1		1300-KC generator assembly	5-183	5-62	5-5c	4-5j(3)	4-72
1A3A1A4A2		300-KC generator assembly	5-184	5-63	5-5b	4-5j(3)	4-72
1A3A1A4A3		1.75-MC buffer amplifier assembly	5-185	5-64	5-5a	4-5j(1)	4-72
1A3A1A5		RF linear amplifier assembly	5-186	5-65, 5-66	5-5f	4-51	4-72

TABLE 4-1. (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1A3A1A6	Converter, Amplitude-Single Side-Band CV-1846/FRT-24A (cont)	Buffer and driver assembly	5-187	5-67	--	4-5f	4-72
1A3A1A7		Carrier and gain control assembly	5-177	5-68	5-5i	4-5m	--
1A3A1A8		SSB carrier insert assembly	5-177	5-55	5-5h	--	--
1A4	Power Supply PP-4242/FRT-24A	Synthesizer power supply	--	--	--	4-10	4-73
1A4		Synthesizer power supply inner case	5-188	5-70, 5-71, 5-77	--	--	4-73
1A4A2		High voltage power supply assembly	5-189	5-72, 5-73, 5-74	5-2a	4-10c	4-73
1A4A3		Low voltage power supply assembly	5-188	5-76	5-2b	4-10a	4-73
1A5/1A6	Synthesizer, Electrical Frequency O-1251/FRT-24A	Synthesizer	--	--	--	4-3	4-74 thru 4-81

TABLE 4-1. (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1A5	Synthesizer, Electrical Frequency O-1251 FRT-24A (cont)	Analog memory section	5-190	5-81, 5-82	--	4-3i	--
1A6A1		Synthesizer inner case	5-191	5-78 to 5-81, 5-118	--		--
1A6A2		Synthesizer outer case	--	5-118	--		--
1A6A1A2A1		Incremental relay assembly (10-KC loop)	5-195	5-83	--	4-3d(3)	--
1A6A1A2A2		Incremental relay assembly (1-KC loop)	5-195	5-84	--	4-3f(3)	--
1A6A1A2A3		Incremental relay assembly (100-CPS loop)	5-195	5-85	--	4-3e(3)	--
1A6A1A2A4		Relay board	5-193	5-86	--	4-3i(3)	--
1A6A1A3		Programmer assembly (digital memory)	5-194	5-79	--	4-3i(3)	4-81
1A6A1A3A1		Trigger assembly	5-194	5-87	--	4-3i(3)	4-81

TABLE 4-1. (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1A6A1A3A2	Synthesizer Electrical Frequency O-1251/FRT-24A (cont)	Timer assembly	5-194	5-88	--	4-3i(3)	4-81
1A6A1A3A3		Coder assembly	5-194	5-89	--	4-3i(3)	4-81
1A6A1A4		Front IF assembly	5-195	5-90, 5-91	5-3b, 5-3c 5-3d, 5-3f	4-3b(9), 4-3d, 4-3d(5), 4-3d(7), 4-3e, 4-3e(5), 4-3e(7), 4-3f, 4-3f(5), 4-3f(7), 4-3h(9), 4-3h(11)	4-75 to 4-79
1A6A1A4A1		Phase detector subassembly (10-KC loop)	5-195	5-90	5-3b	4-3d(9)	4-75
1A6A1A4A2		Phase detector subassembly (1-KC loop)	5-195	5-90	5-3c	4-3e(9)	4-76
1A6A1A4A3		Incremental oscillator subassembly (10-KC loop)	5-195	5-91	5-3b	4-3d(3)	4-75
1A6A1A4A4		Incremental oscillator subassembly (100-cycle loop)	5-195	5-91	5-3d	4-3f(3)	4-77

TABLE 4-1. (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1A6A1A4A5	Synthesizer, Electrical Frequency O-1251/FRT-24A (cont)	Incremental oscillator subassembly (1-KC loop)	5-195	5-91	5-3c	4-3e(3)	4-76
1A6A1A5		Rear IF assembly	5-196	5-96, 5-97	5-3d,5-3f	4-3f(7), 4-3f(9)	4-77
1A6A1A5A1		Phase detector subassembly (100-cycle loop)		5-92,5-93	5-3d	4-3f(9)	4-77
1A6A1A6		VFO and spectrum generator assembly	5-197	5-98, 5-99, 5-100	5-3f	4-3b(7), 4-3h, 4-3h(3)	4-79
1A6A1A7		Gear box assembly	5-191	5-79, 5-80	--	4-3i(4)	--
1A6A1A8		Reference assembly	5-198	5-101	5-3a	4-3b	4-74
1A6A1A8A3		10 to 1 locked divider subassembly	5-198	5-102	5-3a	4-3b(3)	4-74
1A6A1A8A4		100-KC amplifier subassembly	5-198	5-103	5-3a	4-3g(1)	4-74
1A6A1A8A5		X4 multiplier subassembly	5-198	5-104	5-3a	4-3b(5)	4-74

TABLE 4-1. (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1A6A1A9	Synthesizer, Electrical Frequency O-1251/ FRT-24A (cont)	Servo amplifier assembly	5-191	5-79	--	4-3i(4)	--
1A6A1A9A1		Differential chopper and preamplifier assembly	5-199	5-105	--	4-3i(4)	--
1A6A1A9A2		Driver and null detector assembly	5-200	5-106	--	4-3i(4)	--
1A6A1A10		Incremental dividers assembly	5-201	5-79	5-3e	4-3g	4-78
1A6A1A10A1		4 to 1 Locked divider assembly	5-201	5-107	5-3e	4-3g(3)	4-78
1A6A1A10A2		Third mixer assembly	5-201	5-108	5-3e	4-3g(5)	4-78
1A6A1A10A3		5 to 1 locked divider assembly	5-201	5-109	5-3e	4-3g(7)	4-78
1A6A1A10A4		Fourth mixer assembly	5-201	5-110	5-3e	4-3g(9)	4-78
1A6A1A10A5		2 to 1 locked divider assembly	5-201	5-111	5-3e	4-3g(11)	4-78

TABLE 4-1. (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1A6A1A11	Synthesizer, Electrical Frequency O-1251/FRT-24A (cont)	First mixer assembly	5-202	5-112	5-3f	4-3h(7)	4-79
1A6A1A12		1.75-MC assembly	5-203	5-113, 5-114	5-3g	4-3c	4-80
1A6A1A12A1		4 to 1 locked divider sub-assembly	5-203	5-115	5-3g	4-3c	4-80
1A6A1A13		Wide band amplifier assembly	5-204	5-116	5-3f	4-3h(5)	4-79
1A6A1A14		Meter circuit	5-205	5-117			--
1A7	Power Supply PP-4243/FRT-24A	Exciter power supply	5-206	5-119 to 5-122	--	4-11	4-82
1A7A1		Low voltage power supply assembly	5-206	5-121	--	4-11	4-82
1A8		RF assembly	5-207	5-123 to 5-130	5-6a to 5-6h	4-6b	4-83
1A8A1		Directional coupler assembly	5-209	5-131	--	4-6b	--

TABLE 4-1 (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
1A9	Power Supply PP-4243/FRT-24A (cont)	Power control	5-210	5-132, 5-133, 5-134	5-6i	4-6d	--
1A10		HV supply	5-211	5-135, 5-136, 5-137	--	4-6f	4-84
1A11		LV supply	5-212	5-138	--	4-6e	4-84
1A12		Service supply	5-213	5-139	--	4-6g	4-84
1A13		Cabinet	5-163	5-140 to 5-146	--	--	--
2 and 3	Control, Transmitter C-6466/FRT-24A	Transmitter control unit	5-214	5-147, 5-148, 5-149	5-7a to 5-7d	4-8	4-85
6	Keyer, Frequency Shift KY-557/URT	Keyer unit	5-215	5-150, 5-151, 5-152	--	4-9	4-86
6A1		Power supply assembly	5-216	5-153	--	4-9f	4-86
6A2		Key gate and 1-KC oscillator assembly	5-217	5-154	5-8a	4-9c 4-9d	4-86

TABLE 4-1. (Continued)

ASSEMBLY/SUBASSEMBLY			SCHEMATIC DIAGRAM (FIGURE)	PARTS LOCATION (FIGURE)	ALIGNMENT (PARAGRAPH)	TROUBLE SHOOTING (PARAGRAPH)	SERVICING BLOCK DIAGRAM (FIGURE)
REF. DESIG.	NOMENCLATURE	FUNCTION					
6A3	Keyer, Frequency Shift KY-557/URT (cont)	Crystal oscillator assembly (2550 cycles)	5-218	5-155	--	4-9	4-86
6A4		Crystal oscillator assembly (2000 cycles)	5-218	5-155	--	4-9c(3)	4-86
6A5		Trigger and binary gate assembly	5-219	5-156	--	4-9c(7)	4-86
6A6		Divider assembly	5-220	5-157	5-8b	4-c(9)	4-86
6A7		Output and suppression gate sembly	5-221	5-158	--	4-9d(1) 4-9	4-86
6A8		Audio metering assembly	5-222	5-159	--	4-9e(5)	4-86
7	Coupler, Transmission Line CU-390/FRT-24A	Transmission line coupler	5-223	5-161	--	4-7	--

4-3. SYNTHESIZER, ELECTRICAL FREQUENCY O-1251/FRT-24A, (1A6), FUNCTIONAL DESCRIPTION.

a. OVERALL FUNCTIONAL DESCRIPTION.

(1) The synthesizer is an automatically tuned, precision frequency generator capable of producing a large number of output frequencies in the 17.75- to 35.60-MC frequency range with a stability of 1 part in 10^8 per day. The synthesizer is composed of two main parts: analog memory 1A5 and synthesizer 1A6. Analog memory 1A5 receives channel frequency information from the autotune system in RF assembly 1A8. The information is deciphered to produce signals corresponding to the selected frequency channel which are used to activate various relays and a servo motor. Activation of the proper relays selects the necessary synthesizer circuits required to produce the desired output frequency. Any of ten preset frequency channels can be selected in this manner. The frequency of the ten channels is programmed in the memory control section by insertion of shorting plugs in designated apertures. Proper insertion of the plugs sets up circuit conditions that activate certain relays when the proper channel selection information is received from RF assembly 1A8.

(2) The synthesizer section (see figure 4-2) consists of four variable frequency oscillators (VFO's), completely enclosed in phase locked loops, and associated circuitry. The four loops are designated: 10-KC loop, 1-KC loop, 100-CPS loop, and 100-KC (main) loop. The 10-KC, 1-KC, and 100-CPS loops are referred to as secondary loops and their function is to control or change the frequency of the main loop VFO in the proper increments. The 10-KC loop changes the frequency of the main loop VFO in 10-KC steps, the 1-KC loop in 1-KC steps, and the 100-CPS loop in 100-CPS steps. The secondary loop VFO's are tuned automatically by inserting the proper values of inductance in the oscillator tank circuits. This is accomplished by activation of the appropriate secondary loop incremental relays which are operated by relay circuits in analog memory 1A5.

(3) Each secondary loop contains a VFO, a multiplier circuit, a phase detector circuit, and a reactance control circuit. The VFO generates the frequencies necessary to change the main loop frequency in the proper increments. The output of the VFO is multiplied and applied to the phase detector circuit. Each phase detector circuit receives 100-KC reference pulses from pulse generator circuit A4L1 and A4CR1. The phase detector circuit constantly compares the phase relationship between the VFO frequency and the 100-KC reference pulses. Any phase difference between the two inputs to the phase detector circuit produces a DC error voltage that is applied to a reactance control circuit. The reactance control circuit transforms the DC error voltage to a varying capacitance across the VFO tank circuit to constantly correct the VFO frequency to maintain phase lock to the 100-KC pulses. The output of the 100-CPS loop VFO is divided by 4 to 1 locked divider and applied to the third mixer where it is combined with the output of the 1-KC loop VFO. The combined output of the third mixer is divided by a 5 to 1 locked divider and applied to the fourth mixer where it is combined with the output of the 10-KC loop X2 multiplier. The output of the fourth mixer is divided by a 2 to 1 locked divider and applied to the second mixer of the main loop.

(4) The main loop is composed of a VFO, two mixer circuits, a limiter, a discriminator circuit, and a reactance control circuit. The VFO generates the selected frequency in the 17.75- to 35.60-MC range. The output of the VFO is amplified by the wideband amplifier and combined in the first mixer with a selected spectrum, in the 22.1- to 40.0-MC frequency range, from the spectrum generator. The spectrum selection filter in the spectrum generator and the main loop VFO tuning controls are ganged. The output of the first mixer, in the 4.3001- to 4.4000-MC frequency range, is amplified by the first IF amplifier and applied to the second mixer. The second mixer combines the 4.3001- to 4.4000-MC output with the 3.9001 to 4.000-MC from the 2 to 1 locked divider. The 0.400-MC output of the second mixer is amplified by the second IF amplifier, set at a constant amplitude level by the limiter, and applied to the discriminator. This input represents the combined output of the three secondary loops plus the main loop VFO output. The discriminator also receives a 0.400-MC reference signal produced by dividing the 1-MC reference signal from amplifier 1A2 by ten and then multiplying it by four. The discriminator compares the two 0.400-MC inputs and detects any difference in frequency. If a difference in frequency is evident, a DC error voltage is applied to the main loop reactance control circuit. The reactance control circuit transforms the DC error voltage to a proportional varying across the main loop VFO tank circuit to change the VFO frequency to the selected value and phase locks it to the 0.400-MC reference signal. The output of the main loop VFO, in the 17.75- to 35.60-MC frequency range, is amplified by the output amplifier and applied to converter 1A3.

(5) The synthesizer also supplies 100-KC and 1.75-MC auxiliary signals to converter 1A3. The 1-MC reference signal from amplifier 1A2 is divided by ten to produce the 100-KC signal applied to the converter. The 1-MC reference signal is also divided by four to produce a 250-KC signal which is then multiplied by seven. The resulting 1.75-MC signal is applied to converter 1A3.

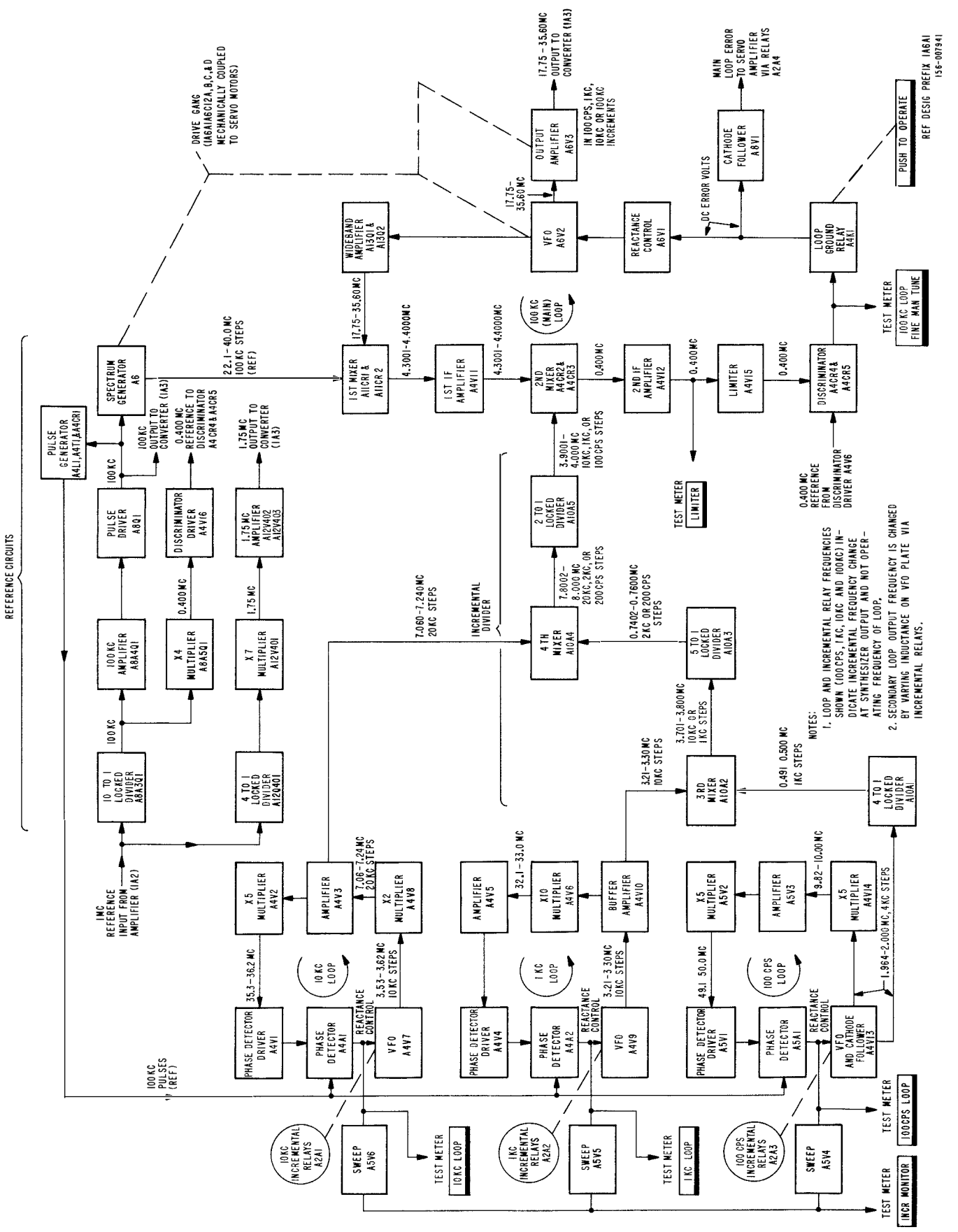


Figure 4-2. Synthesizer 1A6, Overall Functional Block Diagram

(6) Table 4-2 lists the output frequencies of the various circuits within the synthesizer when the MANUAL SETTING digital switch is in positions 160055 through 160944. The output of the first mixer is the difference frequency of the spectrum generator and main loop VFO; the output of the second mixer is the difference frequency of the first mixer and the 2 to 1 locked divider. The output of the third mixer is the sum of the 1-KC loop VFO and the 4 to 1 locked divider; the output of the fourth mixer is the sum of the 10-KC loop X2 multiplier and the 5 to 1 locked divider. For example, when the MANUAL SETTING digital switch is in the 160055 position, the 22.1-MC spectrum generator output is combined in the first mixer with the 17.7555-MC main loop VFO signal to produce a first IF frequency of 4.3445 MC. The 1.980-MC output of the 100-cycle loop VFO is divided to 0.495 MC and combined in the third mixer with the 3.25-MC output of the 1-KC loop VFO to produce a 3.745-MC output. The 3.745-MC output of the third mixer is divided to 0.7490 MC and then combined in the fourth mixer with the 7.14-MC output of the 10-KC loop X2 multiplier to produce a 7.8890-MC output. The 7.8890-MC output of the fourth mixer is divided to 3.9445 MC and combined in the second mixer with the 4.3445-MC first IF frequency to produce a second IF frequency of 0.400 MC. The 0.400-MC second IF frequency is compared in the discriminator with a 0.400-MC reference signal derived from the 1-MC reference input.

b. REFERENCE CIRCUITS, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. — The reference circuits functional section (see figures 4-74 and 5-198) consists of a 10 to 1 locked divider, 100-KC amplifier, X4 multiplier, pulse driver, pulse generator, spectrum generator, and discriminator driver. The reference circuits receive the 1-MC reference signal from amplifier 1A2 and supply a 100-KC sine wave signal to converter 1A3, 100-KC pulses to the secondary loop phase detectors, 22.1- to 40.0-MC reference signal to the main loop first mixer, and a 0.400-MC reference signal to the main loop discriminator. The 1-MC reference signal is applied to the 10 to 1 locked divider. The 10 to 1 locked divider is a free running oscillator at a frequency slightly above 100 KC. The 1-MC input signal phase-locks the oscillator and the result is an extremely stable 100-KC output. The output of the locked divider is frequency multiplied by the X4 multiplier. The output of the locked divider is also amplified by the 100-KC amplifier and applied to the pulse driver, and converter 1A3. The 100-KC sine wave is multiplied to 0.400 MC by the X4 multiplier, amplified by the discriminator driver, and compared with the composite secondary loop plus main loop signal in the main loop discriminator. The output of the pulse driver is amplified and applied to the pulse generator and the spectrum generator. The pulse generator converts the 100-KC sine wave input to corresponding 100-KC pulses. The 100-KC pulses are applied to the secondary loop phase detectors to phase lock the secondary loop VFO outputs. The spectrum generator receives the 100-KC sine wave signal from the pulse driver and produces a 22.1- to 40.0-MC signal at a 100-KC repetition rate. The 22.1- to 40.0-MC signal is applied to the main loop first mixer along with the output of the main loop VFO. The main loop VFO and the spectrum generator tuned filter are gang-tuned so that a change in frequency of one is always accompanied by a proportional change in frequency of the other.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. — Information follows which will be helpful in determining the overall performance of the reference circuits. Refer to figure 4-74 for the circuit location and to figures 5-101 through 5-104, 5-118 and 5-122 for the physical location of test points. The test equipment required is an electronic counter, and a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1J2) (36) : 100 KC at 1 VRMS into 50 ohms. If correct, 10 to 1 locked divider 1A6A1A8A3 and 100-KC amplifier 1A6A1A8A4 are operating properly.

(b) RF output (1A6A1A8XA5-9) (AE) : 400 KC at 0.18 VRMS minimum. If correct, X4 multiplier 1A6A1A8A5 is operating properly.

(c) RF output (1A6A1A8Q1, collector) (AI) : 100 KC at 12 VRMS minimum. If correct, pulse driver 1A6A1A8Q1 is operating properly.

(d) RF input (1A6A1J1) (37) : 1 MC at 1 VRMS minimum 1.5 VRMS maximum. If frequency is unstable or incorrect, refer to paragraph 4-4d(3).

(e) Main loop input (1A6A1A8 XV1-6): ±0.5 VDC. If voltage is greater than ±0.5 VDC, refer to paragraph 4-3h.

(f) DC input voltage: +180 VDC, +28 VDC, and 6.3 VDC.

(3) 10 to 1 LOCKED DIVIDER 1A6A1A8A3, CIRCUIT DESCRIPTION. — The 10 to 1 locked divider is a grounded base oscillator (common emitter configuration) which is free running at a frequency of approximately 100 KC. The collector tuned circuit consists of inductor L1 and capacitors C2 and C3. Positive feedback

TABLE 4-2. CIRCUIT FREQUENCY VS. SETTING = N (f_{ant} + f_{off}) -1.75 MC SWITCH POSITIONS*

MANUAL SETTING	SPECTRUM GENERATOR (MC)	MAIN LOOP VFO (MC)	1ST MIXER (MC)	10-KC LOOP VFO (MC)	10-KC LOOP X2 MULT (MC)	100-CPS LOOP VFO (MC)	4 to 1 DIVIDER (MC)	1-KC LOOP VFO (MC)	3rd MIXER (MC)	5 to 1 DIVIDER (MC)	4th MIXER (MC)	2 to 1 DIVIDER (MC)	2nd MIXER (MC)
16.005500	22.1	17.755500	4.3445	3.57	7.14	1.980	.495	3.25	3.745	.7490	7.8890	3.9445	.400
16.016600	22.1	17.766600	4.3334	3.56	7.12	1.976	.494	3.24	3.734	.7468	7.8668	3.9334	.400
16.027700	22.1	17.777700	4.3223	3.55	7.10	1.972	.493	3.23	3.723	.7446	7.8446	3.9223	.400
16.038800	22.1	17.788800	4.3112	3.54	7.08	1.968	.492	3.22	3.712	.7424	7.8224	3.9112	.400
16.049900	22.1	17.799900	4.3001	3.53	7.06	1.964	.491	3.21	3.701	.7402	7.8002	3.9001	.400
16.050000	22.2	17.800000	4.4000	3.62	7.24	2.000	.500	3.30	3.800	.7600	8.0000	4.0000	.400
16.061100	22.2	17.811100	4.3889	3.61	7.22	1.996	.499	3.29	3.789	.7578	7.9778	3.9889	.400
16.072200	22.2	17.822200	4.3778	3.60	7.20	1.992	.498	3.28	3.778	.7556	7.9556	3.9778	.400
16.083300	22.2	17.833300	4.3667	3.59	7.18	1.988	.497	3.27	3.767	.7534	7.9334	3.9667	.400
16.094400	22.2	17.844400	4.3556	3.58	7.16	1.984	.496	3.26	3.756	.7512	7.9112	3.9556	.400

*Actual output frequency is 1.75 MC greater than digital switch position

is from collector to emitter. The 1-MC reference signal is applied to the base of transistor Q1. Every tenth cycle of the 1-MC signal synchronizes (phase locks) the oscillator fundamental frequency. The 100-KC output has a stability comparable to that of the 1-MC reference signal. The 100-KC output from the emitter of Q1 is multiplied by X4 multiplier A8A5 and amplified by 100-KC amplifier A8A4, the output of which is applied to pulse driver 1A6A1A8Q1.

(4) 10 to 1 LOCKED DIVIDER 1A6A1A8A3, TEST DATA. — Information follows which will be helpful in determining the performance of the 10 to 1 locked divider. Refer to figure 4-74 for the circuit location and to figures 5-101 and 5-102 for the physical location of test points. The test equipment required is an electronic counter and a VTVM, (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A8XA3-7) (AG): 100 KC at 1.8 VRMS minimum. If frequency is stable, 10 to 1 locked divider is operating properly.

(b) DC input voltage (1A6A1A8 XA3-4): +26.5 VDC.

(c) Refer to figure 5-198 for transistor voltage measurements.

(d) Refer to paragraph 5-3 for general information and to paragraph 5-3a for specific alignment procedure of 1A6A1A8A3L1.

(5) 100-KC AMPLIFIER 1A6A1A8A4 AND PULSE DRIVER 1A6A1A8Q1, CIRCUIT DESCRIPTION. — The 100-KC amplifier A8A4 receives the output of 10 to 1 locked divider A8A3, amplifies it and applies it to pulse driver A8Q1 and to converter 1A3 through front panel connector 1A6A1J2. Transformer T1 tunes 100-KC amplifier A8A4. Pulse driver A8Q1 supplies a high level 100-KC sine wave signal to pulse generator A4T1, A4L1 and A4CR1, and to spectrum generator A6.

(6) 100-KC AMPLIFIER 1A6A1A8A4 AND PULSE DRIVER 1A6A1A8Q1, TEST DATA. - Information follows which will be helpful in determining the performance of the 100-KC amplifier and pulse driver. Refer to figure 4-74 for the circuit location and to figures 5-101 and 5-103 for the physical location of test points. The test equipment required is an electronic counter and a VTVM (refer to Section 1 for type designation).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A8Q1-C) (AI): 100 KC at 12 VRMS minimum. If correct, 100-KC amplifier and pulse driver are operating properly.

(b) RF Input (1A6A1A8XA4-2) (AG): 100 KC at 1.8 VRMS minimum. If frequency is unstable, refer to paragraph 4-3b(3).

(c) DC input voltage -100-KC amplifier (1A6A1A8XA4-1): 21 VDC; pulse driver (1A6A1A8E17): +28 VDC.

(d) Refer to figure 5-198 for transistor voltage measurement.

(e) Refer to paragraph 5-3 for general information and to paragraph 5-3a for specific information concerning alignment of 1A6A1A8A4T1.

(7) X4 MULTIPLIER 1A6A1A8A5 AND DISCRIMINATOR DRIVER 1A6A1A4V16, CIRCUIT DESCRIPTION. — The X4 multiplier receives the 100-KC input from 10 to 1 locked divider 1A6A1A8A3, multiplies it to 400 KC, and supplies it to discriminator driver 1A6A1A4V16. With no input signal present, the emitter to base junction of transistor Q1 is reversed biased by proper division of the +28-VDC supply voltage; therefore, transistor Q1 is biased for class C operation. The correct ratio of supply voltage division is determined by resistors R1 and R2. During normal operation, the positive peak of the input signal exceeds the reverse bias, permitting collector current to flow. This clipping action produces harmonics of the 100-KC fundamental frequency. The secondary of transformer T1 and capacitor C2 forms a parallel resonant circuit (tank circuit) tuned to the fourth harmonic (400 KC) of the 100-KC input. The output of the tank circuit is amplified by discriminator driver 1A6A1A4V16 and applied to the discriminator.

(8) X4 MULTIPLIER 1A6A1A8A5 AND DISCRIMINATOR DRIVER 1A6A1A4V16, TEST DATA. — Information follows which will be helpful in determining the performance of the X4 multiplier and discriminator driver 1A6A1A6V16. Refer to figure 4-74 for the circuit location and to figures 5-101 and 5-104 for the physical location of test points. The test equipment required is an electronic counter and a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

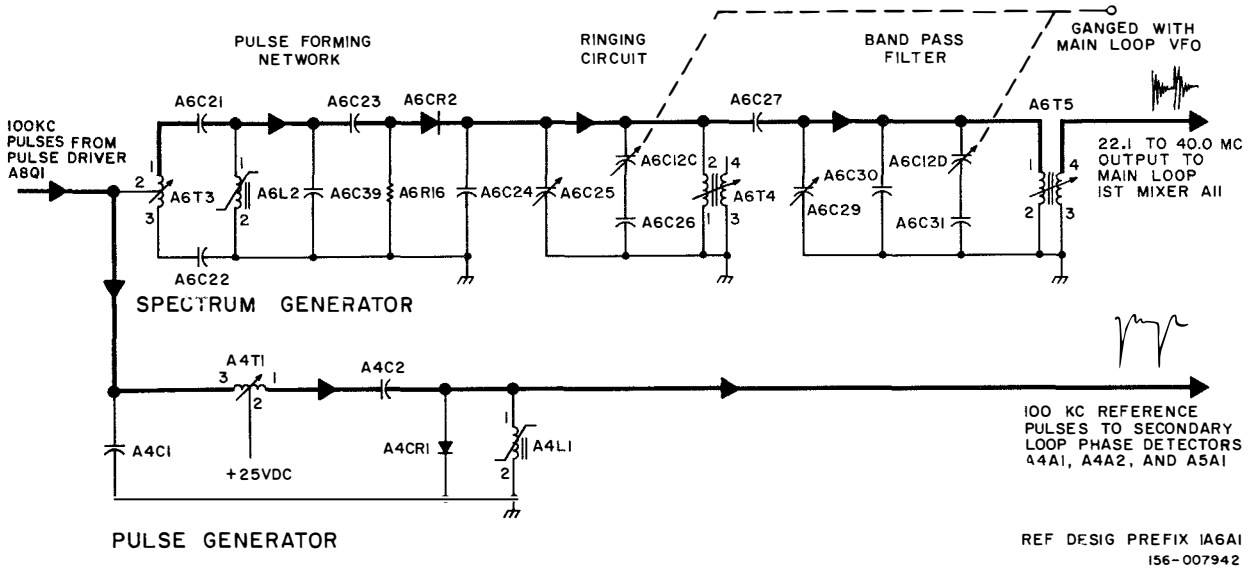


Figure 4-3. Synthesizer 1A6, Spectrum Generator, Simplified Schematic Diagram

(a) RF output (1A6A1A8XA5-9) (AE): 400 KC at 0.18 VRMS minimum. If frequency is stable, X4 multiplier is operating properly.

(b) RF input (1A6A1A8XA5-2) (AG): 100 KC at 1.8 VRMS minimum. If frequency is unstable, refer to paragraph 4-3b(3).

(c) DC input voltage (1A6A1A8 XA5-1): +27 VDC.

(d) Refer to figure 5-198 for transistor voltage measurements.

(e) Refer to paragraph 5-3 for general information and to paragraph 5-3a for specific alignment procedure of 1A6A1A8A5T1.

(9) SPECTRUM GENERATOR 1A6A1A6, CIRCUIT DESCRIPTION. — The spectrum generator (see figure 4-3) consists of a pulse forming network, ringing circuit, and bandpass filter. The spectrum generator receives a 100-KC sine wave from pulse driver 1A6A1A8Q1. The sine wave is changed to pulses by the pulse forming network. The output of the pulse forming network is applied to the ringing circuit tuned to ring at multiples of the 100-KC pulses. The band pass filter selects a spectrum of frequencies in the 22.1- to 40-MC frequency range and applies them to first mixer 1A6A1A11 in the main loop. The 100-KC input is converted to a 22.1- to 40.0-MC output as follows. During the negative peak of the input signal, saturable core reactor L2 is saturated; the low inductive reactance of L2 at saturation appears as a short circuit. As the input signal starts to swing in the positive direction the reactor core begins to unsaturate. As the positive swing increases a point is reached where the reactor core is completely unsaturated. During the unsaturated condition, the high inductive reactance of L2 appears as an open circuit. At this point, capacitor C23 begins to charge. As the input signal increases to its maximum positive level, the reactor core again becomes fully saturated. When this condition is reached, capacitor C23 begins to discharge through the low DC resistance of L2. When the input signal begins to swing in the negative direction, the reactor begins to unsaturate in the opposite polarity. Capacitor C23 begins charging again until it is completely charged when the reactor is fully unsaturated. Further decrease of the input signal in the negative direction causes the reactor to again saturate, thereby repeating the cycle. This operation of the pulse forming network produces positive and negative pulses for each cycle of the input signal. The pulse characteristics are functions of the 100-KC input signal and the saturation parameters of reactor L2. The ringing circuit is a parallel resonant circuit consisting of the primary winding of transformer T4 and capacitors C12, C24, C25, and C26.

The circuit is tuned to ring at multiples of 100 KC and to pass frequencies in the 22.1- to 40.0-MC range. Tuning is accomplished by capacitor C12C. Diode CR2 isolates the ringing circuit from the pulse forming network. The damped 22.1- to 40.0-MC output of the ringing circuit is applied to the bandpass filter consisting of transformer T5 and capacitors C12D, C27, C29, C30, and C31. The band-pass filter and ringing circuit tuning controls C12C, and C12D are ganged with the main loop VFO tuning control, thereby allowing proper tracking by the spectrum generator when the main loop VFO frequency is changed. The output of the bandpass filter is applied to the main loop first mixer.

(10) SPECTRUM GENERATOR, 1A6A1A6, TEST DATA. — Information follows which will be helpful in determining the performance of the spectrum generator. Refer to figure 4-74 for the circuit location and to figures 5-98 and 5-101 for the physical location of test points. The test equipment required is an electronic counter and an RF VTVM, (refer to Section 1 for type designations).

Note

Refer to the servicing diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A6T5, pin 4) (AH): 22.1 to 40.0 MC at 0.2 VRMS minimum. If correct, spectrum generator is operating properly.

(b) RF input (1A6A1A6T3, pin 2) (AI): 100 KC at 12 VRMS minimum. If frequency is unstable, refer to paragraph 4-3b(3).

(c) Refer to paragraph 5-3 for general information and paragraph 5-3f for specific alignment procedures of 1A6A1A6T3, 1A6A1A6C25, 1A6A1A6T4, 1A6A1A6C29, and 1A6A1A6T5.

(11) PULSE GENERATOR 1A6A1A4, CIRCUIT DESCRIPTION. — The pulse generator (see figure 4-3) receives a high level 100-KC sine wave input from pulse driver 1A6A1A8Q1 and supplies negative going 100-KC pulses to the secondary loop phase detectors. The operation of the pulse generator is similar to the operation of the spectrum generator pulse forming network discussed in paragraph 4-3b(7).

(12) PULSE GENERATOR 1A6A1A4, TEST DATA. — Information follows which will be helpful in determining the performance of the pulse generator. Refer to figure 4-74 for the circuit location and to figures 5-90 and 5-101 for the physical location of test points. The test equipment required is an electronic counter, an oscilloscope, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A4L1, pin 1) (AJ): 100-KC pulses at 40 VP-P minimum. If correct, refer to paragraph 4-3d.

(b) RF input (1A6A1A4T1, pin 3) (AI): 100 KC at 12 VRMS minimum. If frequency is unstable refer to paragraph 4-3b(3).

(c) Refer to paragraph 5-3 for general information and to paragraph 5-3d for specific adjustment of 1A6A1A4T1.

c. 1.75-MC CIRCUIT 1A6A1A12, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. — The 1.75-MC circuits functional section (see figures 4-80 and 5-203) consists of a 4 to 1 locked divider, an X7 multiplier, and two 1.75-MC amplifiers. The 1.75-MC circuits receive a 1-MC input signal from amplifier 1A2 and supplies a 1.75-MC signal to converter 1A3. The 1-MC input signal is applied to the base of locked divider A1Q401. The operation of locked divider A1Q401 is similar to the operation of locked divider 1A6A1A8A3 discussed in paragraph 4-3b(3). The 250-KC output of the locked divider is applied to X7 multiplier V401 which clips the positive peaks, thereby producing harmonics. The plate circuit of V401 is tuned to the seventh harmonic of the 250-KC fundamental frequency by capacitor C407 and inductor L402. The 1.75-MC output of V401 is amplified by amplifiers V402 and V403, and applied to the converter unit.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. — Information follows which will be helpful in determining the overall performance of the 1.75-MC circuits. Refer to figure 4-80 for the circuit location and figures 5-113, 5-114, and 5-118 for the physical location of test points. The test equipment required is an electronic counter, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A12: center-tap R421) (38) 1.75-MC at 1.5 VRMS minimum. If correct, 1.75-MC circuits are operating properly.

(b) RF input (1A6A1A12; junction R418 and R419) (39) 1 MC at 1.2 VRMS minimum. If frequency is unstable or incorrect refer to paragraph 4-4d(3).

(c) 4 to 1 locked divider output (1A6A1A2XV401-1) (AM) : 250 KC at 1.9 VRMS minimum. If frequency is unstable or incorrect 4 to 1 locked divider is defective.

(d) 4 to 1 locked divider lock-in range: 6 KC.

(e) 1.75 MC amplifier output (1A6-A1A12XV402-5) (AL) : 1.75 MC at 3.0 VRMS minimum. If frequency is unstable or incorrect 4 to 1 divider or X7 multiplier is defective.

(f) Refer to figure 5-203 for voltage and resistance measurements.

(g) Refer to paragraph 5-3 for general information and paragraph 5-3g for specific alignment procedures of 1A6A1A12A1L401, 1A6A1A12L402, 1A6A1A12T401, 1A6A1A12T402, and 1A6A1A12R421.

d. 10-KC LOOP CIRCUITS 1A6A1A4 AND 1A6A1A5, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. — The 10-KC loop functional section tunes the synthesizer output frequency in 10-KC steps. The 10-KC loop functional section (see figures 4-75 and 5-195) consists of a variable frequency oscillator (VFO), a reactance control circuit, a phase detector, a phase detector driver, an amplifier, two multipliers, and a sweep multivibrator. The VFO A4V7 operates at a frequency in the 3.53- to 3.62-MC range, in 10 steps of 10-KC increments, depending on the selected synthesizer frequency. A change of the 10-KC increment in the synthesizer output frequency energizes appropriate relays which insert the correct value of inductance in the VFO tank circuit changing the VFO frequency accordingly. The output of the VFO is doubled by X2 multiplier A4V8 and applied to amplifier A4V3. The amplified output of A4V3, in the 7.06- to 7.24-MC frequency range, is combined with the composite 1-KC and 100-cycle loop output in the fourth mixer 1A6A1A10A4. The output of A4V3 is also applied to X5 multiplier A4V2. The output of the multiplier, at a frequency ten times the VFO frequency, is amplified by phase detector driver A4V1. The phase detector also receives harmonics, developed by 100-KC reference pulses from the reference circuits functional section. The two signals are compared in the phase detector to produce a DC error voltage when the phase difference is other than 90 degrees. The DC error output is applied to the reactance control circuit which translates the error to a varying capacitance across the VFO tank circuit, thus correcting the error and phase locking the oscillator to the 100-KC reference signal. The frequency deviation range over which the VFO can be maintained in phase lock is defined as "hold-in"; the frequency error range over which the VFO can drift out of lock and be brought back into phase lock is defined as "pull-in". The phase detector and reactance control circuits have a pull-in range of ±2 KC (a 1-VDC output from the phase detector corresponds to a 1-KC change in the VFO frequency). If the error is beyond this range, sweep multivibrator A5V6 operates and extends the pull-in range of the phase detector. The output of the sweep multivibrator is applied to TEST METER 1A5A1M1 which provides visual indication of the "out of lock" condition.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. — Information follows which will be helpful in determining the overall operation of the 10-KC loop circuits functional section. Refer to figure 4-75 for the circuit location and to figures 5-90 and 5-91 for the physical location of test points. The test equipment required is an electronic counter, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

To change the synthesizer frequency manually, first set the desired frequency on the MANUAL SETTING digital switch. Remember that the actual output frequency of the synthesizer is 1.75 MC higher than the switch setting. Then set the SERVO MODE switch to MANUAL CHANNEL AUTO and throw the MOTOR DRIVE ON switch to ON. Press the START switch and after completion of tuning cycle throw MOTOR DRIVE ON switch off. To change incremental frequencies of 10 KC, 1 KC, and 100 cycles, it is only necessary to set the applicable digit on the MANUAL SETTING digital switch.

Note

RF output of 10-KC loop changes in 20-KC steps because of X2 multiplier 1A6A1A4V8.

(a) RF output (1A6A1A4E36) (AN) : 7.06 to 7.24 MC in 20-KC steps at 0.2 VRMS minimum. If correct, 10-KC loop is operating properly.

(b) RF input (1A6A1A4T1, pin 2) (AS) : 100 KC at 10 VRMS minimum. If frequency is unstable, refer to paragraph 4-3b(3).

(c) Check front panel TEST METER reading with TEST METER switch in 10-KC loop and 180V B+ positions. Refer to table 3-12 for typical meter readings.

(3) VFO 1A6A1A4V7 AND REACTANCE CONTROL CIRCUIT 1A6A1A4A3, CIRCUIT DESCRIPTION. — The 10-KC loop VFO, V7 and associated circuitry (see figure 4-4), is a Colpitts oscillator operating in the 3.53- to

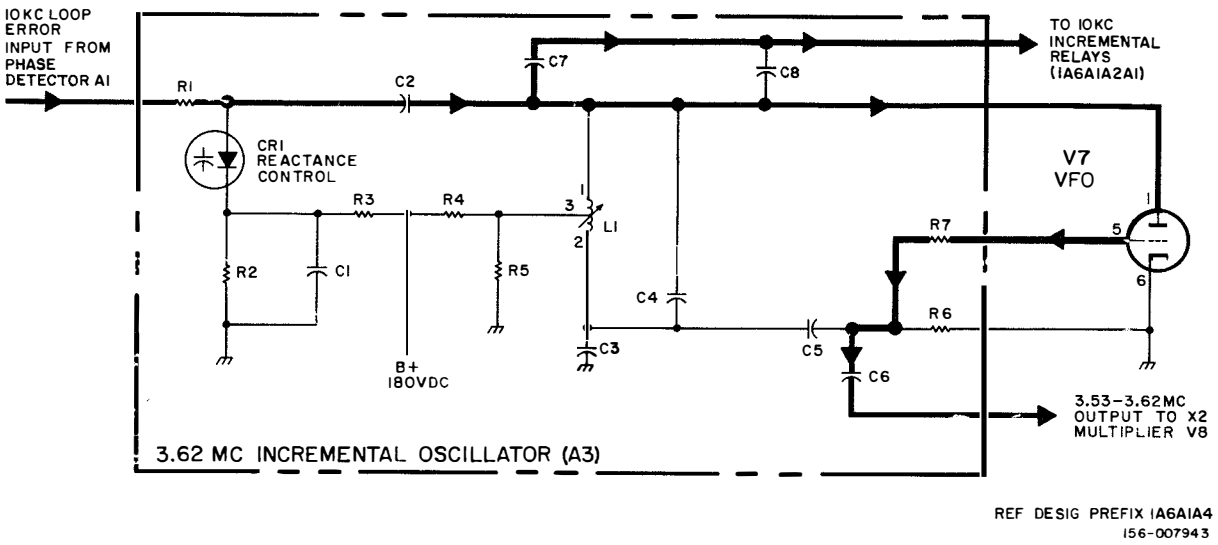


Figure 4-4. Synthesizer 1A6, 10-KC Loop VFO and Reactance Control Circuits, Simplified Schematic Diagram

3.62-MC frequency range. The exact oscillator frequency is determined by the synthesizer operating frequency. When the synthesizer frequency is changed, proper values of inductance are inserted in the VFO tank circuit changing the frequency accordingly. See NAVSHIPS 900,000.102 for a description of the Colpitts oscillator. The DC error input from the phase detector, representing a change in the VFO frequency, is applied to the anode of reactance control diode A3CR1. Diode A3CR1 is reversed biased at +12 VDC by voltage divider A3R3, A3R2. With no error voltage present, the junction capacitance of diode A3CR1 is approximately 30 PF and is effectively across the VFO tank circuit. When an error voltage is present, the junction capacitance of diode A3CR1 changes, thereby changing the overall capacitance of the VFO tank circuit and the VFO frequency. The input error voltage has a range of ±2 VDC. If the VFO frequency drifts to an increased value, the resulting negative error voltage increases the reverse bias of A3CR1, thereby increasing its junction capacitance. Since diode A3CR1 is in parallel with one half of VFO tank circuit inductor A3L1, the increase in capacitance reduces the resonant frequency of the tank circuit, resulting in a decrease of the VFO frequency. If the VFO frequency drifts to a decreased value, the resulting positive error voltage reduces the reverse bias on diode A3CR1, thereby decreasing its junction capacitance. The decrease of capacitance in the VFO tank circuit increases its resonant frequency. The output from the grid of the 10-KC loop VFO is applied to X2 multiplier 1A6A1A4V8.

(4) VFO 1A6A1A4V7 AND REACTANCE CONTROL CIRCUIT 1A6A1A4A3, TEST DATA. — Information follows which will be helpful in determining the operation of the 10-KC loop VFO and reactance control circuit. Refer to figure 4-75 for the circuit location and figure 5-91 for the physical location of test points.

Note

Because operational tests cannot be made without loading the oscillator circuits, voltage and resistance measurements are recommended only.

The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) DC input voltage (1A6A1A4E5): +180 VDC.

(b) Refer to figure 5-195 for voltage and resistance measurements.

(c) Refer to paragraph 5-3 for general information and to paragraph 5-3b for specific alignment procedures of 1A6A1A4A3L1.

(5) X2 MULTIPLIER 1A6A1A4V8 AND AMPLIFIER 1A6A1A4V3, CIRCUIT DESCRIPTION. — The X2 multiplier (see figure 4-5) receives the 3.53- to 3.62-MC output of 10-KC loop VFO 1A6A1A4V7. The signal is multiplied by two, amplified, and applied to X5 multiplier 1A6A1A4V2 and to the fourth mixer A10A4. The input signal is applied to the grid of X2 multiplier V8. The multiplier operates as a class C amplifier; the input signal drives the tube to cutoff by grid leak bias. Class C operation distorts the input signal to produce harmonics of the fundamental frequency. For more efficient production of harmonics, X2 multiplier V8 is operated as a tetrode. The plate circuit of V8 is tuned to the second harmonic frequency by the tank circuit inductor L25 and variable capacitor C61. The output from the tank circuit is applied to the grid of amplifier V3. Plate tuning of amplifier V3 is accomplished by inductor L4 and capacitors C15 and C16. The output from the plate of V3, in the 7.06- to 7.24-MC frequency range, is applied to X5 multiplier 1A6A1A4V2 and to the fourth mixer A10A4. See Handbook of Electronic Circuits NAVSHIPS 900,000.102 for a description of grid leak bias, class C amplifier, and amplifier circuits.

(6) X2 MULTIPLIER 1A6A1A4V8 AND AMPLIFIER 1A6A1A4V3, TEST DATA. — Information follows which will be helpful in determining the performance of X2 multiplier V8 and amplifier V3. Refer to figure 4-75 for the circuit location and figures 5-90 and 5-91 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160000.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Bias voltage (1A6A1A4XV3-7): -14 VDC minimum.

(b) DC input voltage (1A6A1A4-C55): +180 VDC.

(c) Refer to figure 5-195 for voltage and resistance measurements.

(d) Refer to paragraph 5-3 for general information and paragraph 5-3b for specific alignment procedures of 1A6A1A4C61 and 1A6A1A4L4.

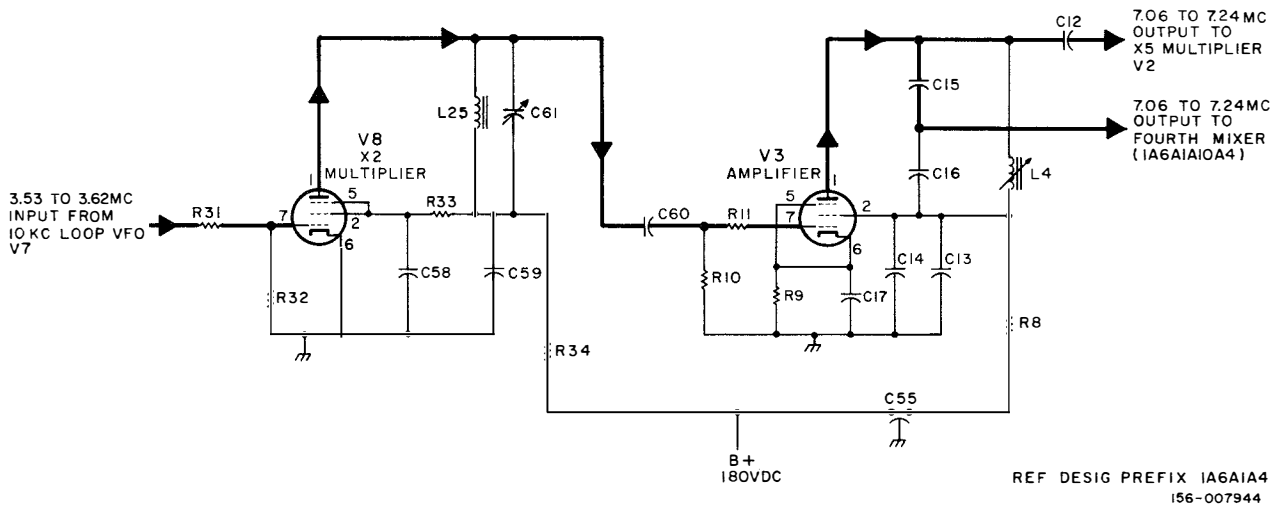


Figure 4-5. Synthesizer 1A6, 10-KC Loop X2 Multiplier and Amplifier, Simplified Schematic Diagram

(7) X5 MULTIPLIER 1A6A1A4V2 AND PHASE DETECTOR DRIVER 1A6A1A4V1, CIRCUIT DESCRIPTION. - The X5 multiplier, V2 and associated circuitry (see figure 4-6), receives the 7.06- to 7.24-MC signal from amplifier 1A6A1A4V3, multiplies the frequency to 35.3 to 36.2 MC and applies it to phase detector driver V1. The 7.06 to 7.24-MC signal is applied to the grid of V2. Multiplier V2 is a class C amplifier; the input signal driving the tube to cutoff by grid leak bias. Class C operation distorts the input signal to produce harmonics of the fundamental frequency. Capacitor C10 and inductor L3 form a plate tank circuit which is tuned to resonate at the fifth harmonic of the fundamental input frequency. The output from the tank circuit is applied to the grid of phase detector driver V1. Plate tuning of the phase detector driver is accomplished by capacitors A1C5, A1C6, and the primary winding of transformer A1T1. The output of V1 is coupled through transformer A1T1 to the phase detector. See Handbook of Electronic Circuits, NAVSHIPS 900,000.102, for a description of grid leak bias, class C amplifiers, and driver circuits.

(8) X5 MULTIPLIER 1A6A1A4V2 AND PHASE DETECTOR DRIVER 1A6A1A4V1, TEST DATA. - Information follows which will be helpful in determining the performance of X5 multiplier V2 and phase detector driver V1. Refer to figure 4-75 for the circuit location of test points and figure 5-90 for the physical location. The test equipment required is a VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160000.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Bias voltage (1A6A1A4XV1-7): -7.5 VDC minimum.

(b) DC input voltage (1A6A1A4-C55): +180 VDC.

(c) Refer to figure 5-195 for voltage and resistance measurements.

(d) Refer to paragraph 5-3 for general information and paragraph 5-3 b for for specific alignment procedures of 1A6A1A4L3 and 1A6A1A4A1C5.

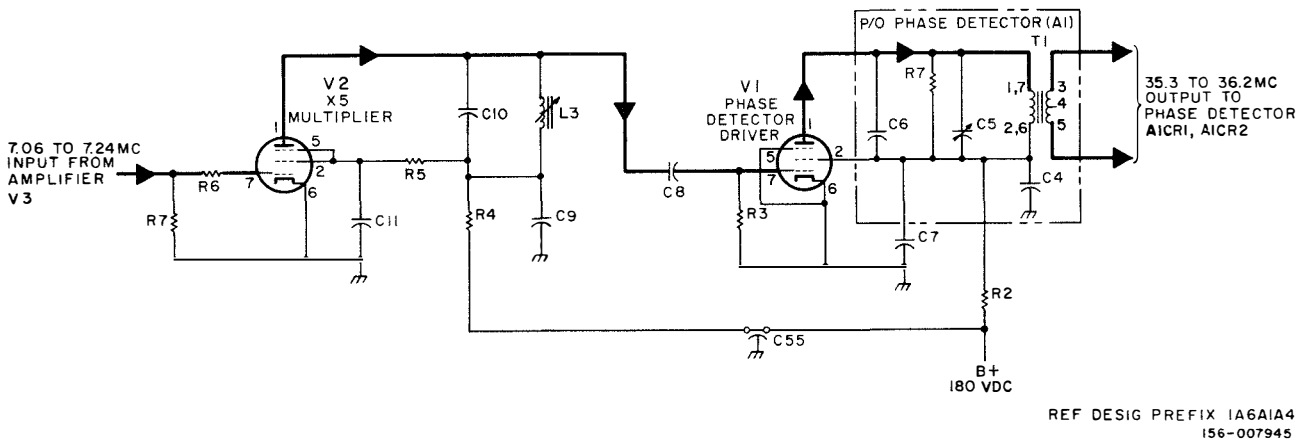


Figure 4-6. Synthesizer 1A6, 10-KC Loop X5 Multiplier and Phase Detector Driver, Simplified Schematic Diagram

(9) PHASE DETECTOR 1A6A1A4A1 AND SWEEP MULTIVIBRATOR 1A6A1A5V6, CIRCUIT DESCRIPTION. - Phase detector diodes A4A1CR1, A4A1CR2 and associated circuitry (see figure 4-7) receive the 35.3- to 36.2-MC signal from phase detector driver 1A6A1A4V1 and harmonics of the 100-KC reference pulses from the pulse generator 1A6A1A4L1, CR1. The two signals are compared to produce a DC error voltage corresponding to phase error. The 35.3- to 36.2-MC sine wave input signal appears at the secondary winding of transformer A4A1T1. The 100-KC reference pulses are applied to the secondary winding center tap. With no 100-KC pulses present, diodes A4A1CR1 and A4A1CR2 alternately conduct during opposite halves of the input signal cycle. The conduction of the diodes charges capacitors A4A1C1 and A4A1C2 equally in opposite polarities and the phase detector output is zero. The 100-KC input pulses are composed of a damped spectrum of frequencies occurring at 100-KC intervals. The spectrum of frequencies includes 35.3 to 36.2 MC; therefore, comparison is achieved on a cycle-by-cycle basis. When the sine wave input signal from the phase detector driver is 90 degrees out of phase with the reference signal, diodes A4A1CR1 and A4A1CR2 conduct equally, resulting in equal charging of capacitors A4A1C1 and A4A1C2. This corresponds to a no error condition and the phase detector output is zero. If the phase difference is other than 90 degrees, one diode conducts more than the other. The unequal conduction of the diodes charges capacitors A4A1C1 and A4A1C2 to unequal levels, thus producing a DC error voltage whose amplitude and polarity is proportional to the amount and direction of the phase error. The DC error voltage is applied to the reactance control circuit to produce a variable capacitance which corrects (locks) the VFO frequency. Inductor 1A6A1A4L2 and capacitor 1A6A1A4C5 form a 100-KC filter which traps and eliminates the 100-KC pulses. Capacitors 1A6A1A4C3, 1A6A1A4C4, and 1A6A1A4C6 and resistor 1A6A1A4R1 form a low-pass filter with a 10-KC cutoff frequency. The filter stops the RF frequencies from appearing at the phase detector output. If the VFO breaks lock, sweep multivibrator A5V6 sweeps the VFO through zero error thus causing the VFO to lock to the harmonic of the 10 KC reference pulse. Sweep multivibrator A5V6 is a cathode-coupled, astable multivibrator operating at a frequency of 2 to 10 CPS. Since the grid resistance of the multivibrator is the effective resistance of the phase detector, the multivibrator frequency is proportional to the phase detector error voltage output. See Handbook of Electronic Circuits NAVSHIPS 900,000.102 for a description of the multivibrator. The output of the multivibrator is applied to the reactance control circuit which attempts to restore (lock) the VFO frequency. If the frequency is corrected sufficiently to allow for further correction by the phase detector, it commences normal operation. If sufficient correction cannot be attained, an out-of-lock condition exists. The multivibrator output is also applied to the test meter which provides visual indication of the out-of-lock condition.

(10) PHASE DETECTOR 1A6A1A4A1 AND SWEEP MULTIVIBRATOR 1A6A1A5V6, TEST DATA. - Information follows which will be helpful in determining the operation of phase detector A4A1 and sweep multivibrator A5V6. Refer to figure 4-75 for the circuit location and figures 5-90 and 5-96 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Voltage at junction of capacitors 1A6A1A4A1C1 and 1A6A1A4A1C2: -10 VDC minimum. If voltage is low, refer to paragraph 4-3d(3).

(b) Refer to paragraph 5-3 for general information and paragraph 5-3b for specific alignment procedures of 1A6A1A4A1C5.

e. 1-KC LOOP CIRCUITS 1A6A1A4 AND 1A6A1A5, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. - The 1-KC loop functional section (see figures 4-76 and 5-195) tunes the synthesizer output frequency in 1-KC steps. It consists of a variable frequency oscillator (VFO), a reactance control circuit, a phase detector, phase detector driver, an amplifier, a multiplier, and a buffer amplifier. The functional operation of the 1-KC loop circuits is similar to the operation of the 10-KC loop circuits functional section described in paragraph 4-3d. The output of the 1-KC loop circuits, in the frequency range of 3.21 to 3.30 MC is applied to the incremental dividers functional section where it is combined with the 100-CPS loop output.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. - Information follows which will be helpful in determining the overall performance of the 1-KC loop circuits functional section. Refer to figure 4-76 for the circuit location and figures 5-90 and 5-91 for the physical location of test points. The test equipment required is an electronic counter, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

To change the synthesizer frequency manually, first set the desired frequency on the MANUAL SETTING digital switch. Remember that the actual output frequency of the synthesizer is 1.75 MC higher than the switch setting. Then set the SERVO MODE switch to MANUAL CHANNEL AUTO and throw the MOTOR DRIVE ON switch to ON. Press the START switch, and after completion of tuning cycle, throw MOTOR DRIVE ON switch off. To change incremental frequencies of 10 KC, 1 KC, and 100 cycles, it is only necessary to set the applicable digit on the MANUAL SETTING digital switch.

(a) RF output (1A6A1A4E37) (AT) 3.21 to 3.30 MC in 10-KC steps at 0.3 VRMS minimum. If correct, 1KC loop is operating properly.

(b) RF input (1A6A1A4T1, pin 2) (AX): 100 KC at 7 VRMS minimum. If frequency is unstable, refer to paragraph 4-3b(3).

(c) Check front panel TEST METER reading with TEST METER switch in 1-KC loop and 180V B+ positions. Refer to table 3-12 for typical meter readings.

(3) VFO 1A6A1A4V9 AND REACTANCE CONTROL CIRCUIT 1A6A1A4A5, CIRCUIT DESCRIPTION. - The operation of the 1-KC loop VFO and reactance control circuit (see figure 4-4) is identical to the operation of the 10-KC loop VFO and reactance control circuit described in paragraph 4-3d(3).

(4) VFO 1A6A1A4V9 AND REACTANCE CONTROL CIRCUIT 1A6A1A4A5, TEST DATA. - Information follows which will be helpful in determining the performance of the 1-KC loop VFO and reactance control circuit. Refer to figure 4-76 for the circuit location and figure 5-90 for the physical location of test points.

Note

Because operational tests cannot be made without loading the oscillator circuits, voltage and resistance measurements are recommended only.

The test equipment is a VTVM (refer to Section 1 for type designations).

NOTE

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) DC input voltage (1A6A1A4-E5): +180 VDC.

(b) Refer to figure 5-195 for voltage and resistance measurements.

(c) Refer to paragraph 5-3 for general information and paragraph 5-3c for specific alignment procedure of 1A6A1A4A5L1.

(5) BUFFER AMPLIFIER 1A6A1A4-V10 AND X10 MULTIPLIER 1A6A1A4V6, CIRCUIT DESCRIPTION. - The buffer amplifier V10 and associated circuitry (see figure 4-8) receives the 3.21- to 3.30-MC signal from the VFO. The output from the cathode of V10 is applied to the third mixer 1A6A1A10A2 and the output from the plate of V10 is applied to X10 multiplier V6. See Handbook of Electronic Circuits, NAVSHIPS 900,000.102, for a description of the buffer amplifier. The operation of X10 multiplier V6 is similar to X5 multiplier 1A6A1A4V2 described in paragraph 4-3d(7); the difference is that the plate tank circuit (L7 and C31) of V6 is tuned to resonate at the tenth harmonic frequency of the fundamental input frequency. The output of X10 multiplier V6 is applied to amplifier 1A6A1A4V5.

(6) BUFFER AMPLIFIER 1A6A1A-4V10 AND X10 MULTIPLIER 1A6A1A4V6, TEST DATA. — Information which will be helpful in determining the performance of buffer amplifier V10 and X10 multiplier V6 is listed below. Refer to figure 4-76 for the circuit location and figures 5-90 and 5-91 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160055.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Bias voltage (1A6A1A4XV6-7): 25 VDC minimum.

(b) DC input voltage (1A6A1A4-E5): +180 VDC.

(c) Refer to figure 5-195 for voltage and resistance measurements.

(d) Refer to paragraph 5-3 for general information and paragraph 5-3c for specific alignment procedures of 1A6A1A4L7 and 1A6A1A4C73.

(7) AMPLIFIER 1A6A1A4V5 AND PHASE DETECTOR DRIVER 1A6A1A4V4, CIRCUIT DESCRIPTION. - Amplifier V5 (see figure 4-9) amplifies the 32.1- to 33.0-MC signal from X10 multiplier 1A6A1A4V6, and applies it to phase detector driver V4. The output of phase

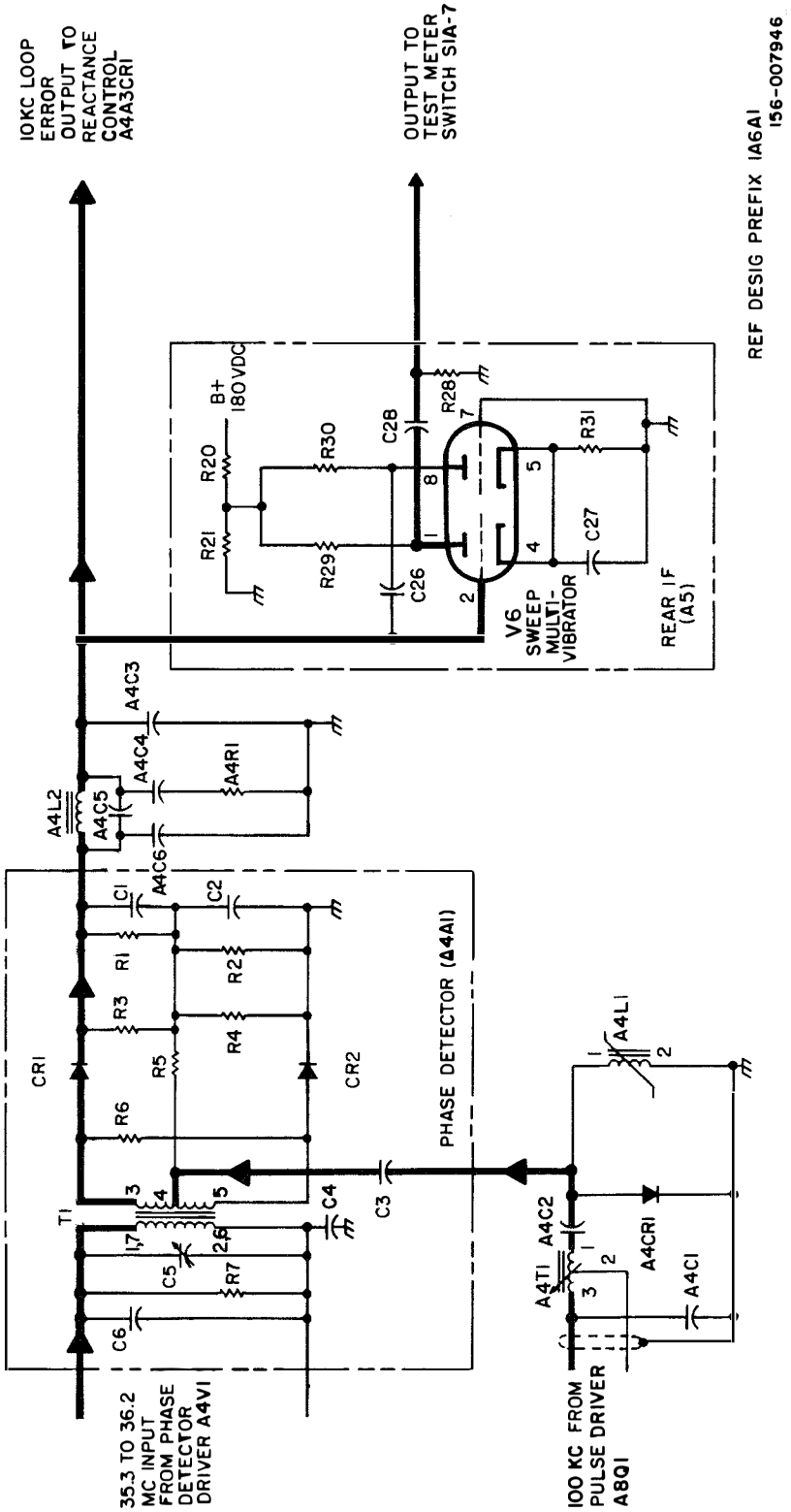


Figure 4-7. Synthesizer 1A6, 10-KC Loop Phase Detector and Sweep Multivibrator, Simplified Schematic Diagram

detector driver V4 is applied to phase detector 1A6A1A4A2 where it is compared with 100-KC reference pulses. Amplifier V5 is similar to 10-KC loop amplifier 1A6A1A4V3 described in paragraph 4-3d(5) and phase detector driver V4 is similar to 10-KC loop phase detector driver 1A6A1A4V1 described in paragraph 4-3d(7).

(8) AMPLIFIER 1A6A1A4V5 AND PHASE DETECTOR DRIVER 1A6A1A4V4, TEST DATA. - Information follows which will be helpful in determining the operation of amplifier V5 and phase detector driver V4. Refer to figure 4-76 for the circuit location and figure 5-90 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160055.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Bias voltage (1A6A1A4XV4-7): -10 VDC minimum.

(b) DC input voltage (1A6A1A4-C56); +180 VDC.

(c) Refer to figure 5-195 for voltage and resistance measurements.

(d) Refer to paragraph 5-3 for general information and paragraph 5-3c for specific alignment procedures of 1A6A1A4L6 and 1A6A1A4A2C5.

(9) PHASE DETECTOR 1A6A1A4A2 AND SWEEP MULTIVIBRATOR 1A6A1A5V5, CIRCUIT DESCRIPTION. - The phase detector, diodes A4A2CR1, A4A2CR2 and associated circuitry, receives the 32.1- to 33.0-MC signal from phase detector driver 1A6A1A4V4 and 100-KC reference pulses from the reference circuits functional section. The two signals are compared to produce a DC error voltage corresponding to the phase error. The error voltage is applied to the 1-KC loop reactance control circuit. The operation of phase detector A4A2 and sweep multivibrator A5V5 is similar to the operation of phase detector 1A6A1A4A1CR1 and 1A6A1A4A1-CR2 and sweep multivibrator A5V6 described in paragraph 4-3d(9).

(10) PHASE DETECTOR 1A6A1A4A2 AND SWEEP MULTIVIBRATOR 1A6A1A5V5, TEST DATA. - Information follows which will be helpful in determining the operation of phase detector A4A2 and sweep multivibrator A5V5. Refer to figure 4-76 for the circuit location and figures 5-90 and 5-91 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Voltage at junction of capacitors 1A6A1A4A2C1 and 1A6A1A4A2C2; -10 VDC minimum. If voltage is low refer to paragraph 4-3e(3).

(b) Refer to paragraph 5-3 for general information and paragraph 5-3c for specific alignment procedure of 1A6A1A4A2C5.

f. 100-CPS LOOP CIRCUITS 1A6A1A4 AND 1A6A1A5 FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. - The 100-CPS loop functional section (see figures 4-77 and 5-195) tunes the synthesizer output frequency in 100-cycle steps. It consists of a variable frequency oscillator (VFO), a reactance control circuit, a phase detector, a phase detector driver, an amplifier, and two X5 multipliers. The functional operation of the 100-CPS loop circuits is similar to the operation of the 10-KC loop circuits functional section described in paragraph 4-3d. The output of the 100-CPS loop circuits, in the 1.964- to 2.000-MC frequency range, is applied to the incremental divider's functional section where it is combined with the 1-KC loop output.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. - Information follows which will be helpful in determining the overall operation of the 100-CPS loop circuits functional section. Refer to figure 4-77 for the circuit location and figures 5-90, 5-96 and 5-97 for the physical location of test points. The test equipment required is an electronic counter and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

To change the synthesizer frequency manually, first set the desired frequency on the MANUAL SETTING digital switch. Remember that the actual output frequency of the synthesizer is 1.75 MC higher than the switch setting.

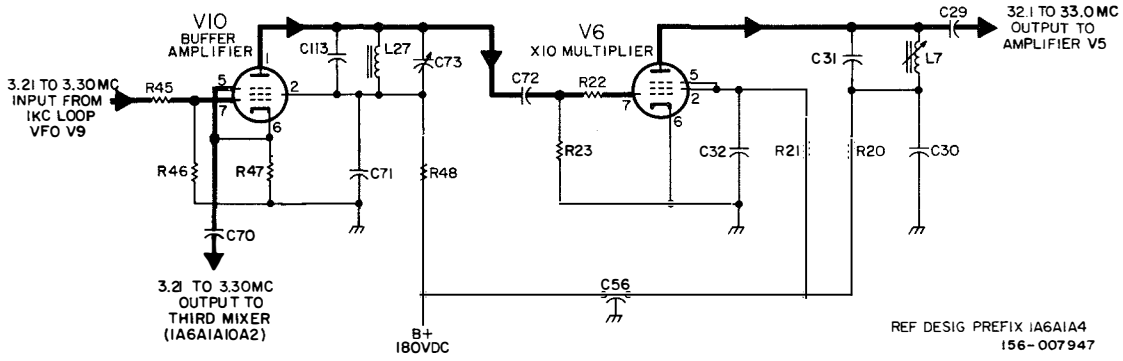


Figure 4-8. Synthesizer 1A6, 1-KC Loop Buffer Amplifier and X10 Multiplier, Simplified Schematic Diagram

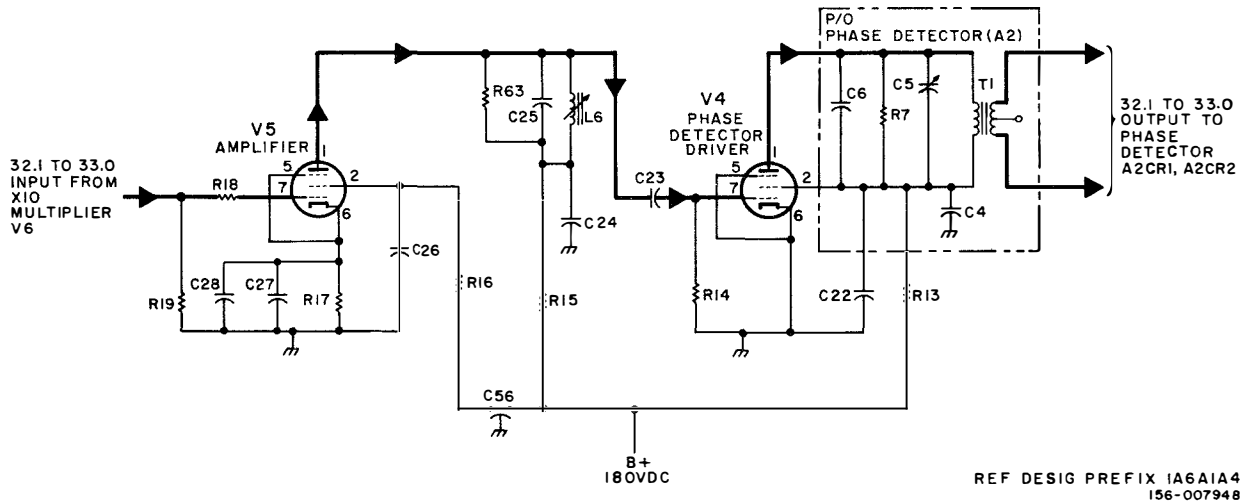


Figure 4-9. Synthesizer 1A6, 1-KC Loop Amplifier and Phase Detector Driver, Simplified Schematic Diagram

Then set the SERVO MODE switch to MANUAL CHANNEL AUTO and throw the MOTOR DRIVE ON switch to ON. Press the START switch and after completion of tuning cycle throw MOTOR DRIVE ON switch off. To change incremental frequencies of 10 KC, 1 KC, and 100 cycles, it is only necessary to set the applicable digit on the MANUAL SETTING digital switch.

(a) RF output (1A6A1A4E38) (AY) : 1.964 to 2.000 MC in 4-KC steps at 0.5 VRMS minimum. If correct, 100-cycle loop is operating properly.

(b) RF input (1A6A1A5T1, pin 4) (BB) : 100 KC at 9 VRMS minimum. If frequency is unstable, refer to paragraph 4-3b(3).

(c) Check front panel TEST METER reading with TEST METER switch in 100-CPS LOOP and 180-V B+ positions. Refer to table 3-12 for typical meter readings.

(3) VFO CATHODE FOLLOWER 1A6A1A4V13 AND REACTANCE CONTROL CIRCUIT 1A6A1A4A4, CIRCUIT DESCRIPTION. - The operation of the 100-CPS loop VFO cathode follower and reactance control circuits (see figure 4-10) is similar to the operation to the 10-KC loop VFO and reactance control circuits described in paragraph 4-3d(3). The output of the VFO is applied to X5 multiplier 1A6A1A4V14. A portion of the VFO output is also applied to the grid of the cathode follower section of V13. The output of the cathode follower is applied to the 4 to 1 locked divider 1A6A1A10A1 in the incremental divider functional section. See Handbook of Electronic Circuits NAVSHIPS 900,000.102 for the description of a cathode follower.

(4) VFO CATHODE FOLLOWER 1A6A1A4V13 AND REACTANCE CONTROL CIRCUIT A4A4, TEST DATA. — Information follows which will be helpful in determining the operation of the 100-CPS loop VFO cathode follower and reactance control circuits. Refer to figure 4-77 for the circuit location and figure 5-91 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Because operational tests cannot be made without loading the oscillator circuits, voltage and resistance measurements are recommended only.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) DC input voltage (1A6A1A-4E5): +180 VDC.

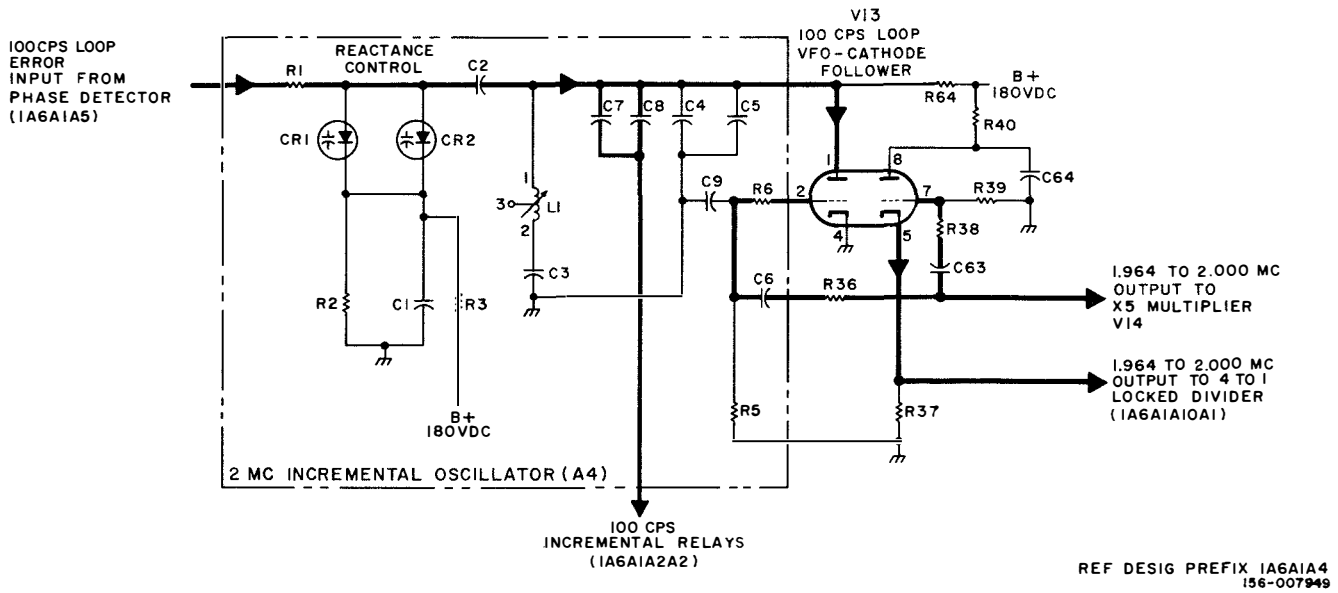


Figure 4-10. Synthesizer 1A6, 100-Cycle Loop VFO, Cathode Follower, and Reactance Control Circuits, Simplified Schematic Diagram

(b) Refer to figure 5-195 for voltage and resistance measurements.

(c) Refer to paragraph 5-3 for general information and paragraph 5-3d for specific alignment procedure of 1A6A1A4A4L1.

(5) X5 MULTIPLIER 1A6A1A4V14 AND AMPLIFIER 1A6A1A5V3, CIRCUIT DESCRIPTION. — The X5 multiplier, A4V14 and associated circuitry (see figure 4-11), receives the 1.964- to 2.000-MC signal from 100-CPS loop VFO 1A6A1A4V13, multiplies it to 9.82 to 10.000 MC, and applies it to the grid of amplifier A5V3. The output of amplifier A5V3 is applied to multiplier 1A6A1A5V2. The operation of 100-CPS loop X5 multiplier A4V14 and amplifier A5V3 is similar to the operation of 10-KC loop X2 multiplier A4V8 and amplifier A4V3 described in paragraph 4-3d(5).

(6) X5 MULTIPLIER 1A6A1A4V14 AND AMPLIFIER 1A6A1A5V3, TEST DATA. — Information follows which will be helpful in determining the operation of 100-CPS loop multiplier A4V14 and amplifier A5V3. Refer to figure 4-77 for the circuit location and figures 5-91, 5-96 and 5-97 for the physical location of test points. The test equipment required is an electronic counter, a VTVM and an RF VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160055.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Bias voltage (1A6A1A5V2-7) (AZ): -18 VDC minimum.

(b) DC input voltage (1A6A1A4E5): +180 VDC.

(c) Refer to figure 5-195 for voltage and resistance measurements.

(d) Refer to paragraph 5-3 for general information and paragraph 5-3d for specific alignment procedures of 1A6A1A4C66 and 1A6A1A5L3.

(7) X5 MULTIPLIER 1A6A1A5V2 AND PHASE DETECTOR DRIVER 1A6A1A5V1, CIRCUIT DESCRIPTION. — The X5 multiplier V2 and associated circuitry (see figure 4-12), receive the 9.82- to 10.00-MC signal from amplifier 1A6A1A5V3, multiply it to 49.1 to 50.0 MC, and apply it to the grid of phase detector driver V1. The output of phase detector driver V1 is applied to phase detector 1A6A1A5A1. The operation of 100-CPS loop X5 multiplier V2 and phase detector driver V1 is identical to the operation of 10-KC loop X5 multiplier 1A6A1A4V2 and phase detector driver 1A6A1A4V1 described in paragraph 4-3d(7).

(8) X5 MULTIPLIER 1A6A1A5V2 AND PHASE DETECTOR DRIVER 1A6A1A5V1, TEST DATA. — Information which will be helpful in determining the operation of 100-CPS loop X5 multiplier V2 and phase detector driver V1 is listed below. Refer to figure 4-77 for the circuit location and figure 5-96 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160055.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Bias voltage (1A6A1A5XV1-7): -5 VDC minimum.

(b) DC input voltage (1A6A1A-5C19): +180 VDC.

(c) Refer to figure 5-196 for voltage and resistance measurements.

(d) Refer to paragraph 5-3 for general information and paragraph 5-3d for specific alignment procedures of 1A6A1A5L2 and 1A6A1A5A1C5

(9) PHASE DETECTOR 1A6A1A5A1 AND SWEEP MULTIVIBRATOR 1A6A1A5V4, CIRCUIT DESCRIPTION. — The phase detector, diodes CR1 and CR2 and associated circuitry, receives the 49.1- to 50.0-MC signal from phase detector driver 1A6A1A5V1 and 100-KC reference pulses from the reference circuits functional section. The two signals are compared to produce a DC error voltage corresponding to the phase error. The error voltage is applied to the 100-CPS loop reactance control circuit. The operation of 100-CPS loop phase detector A1 and sweep multivibrator V4 is similar to the operation of 10-KC loop phase detector 1A6A1A4A1 and sweep multivibrator 1A6A1A5V6 described in paragraph 4-3d(9).

(10) PHASE DETECTOR 1A6A1A5A1 AND SWEEP MULTIVIBRATOR 1A6A1A5V4, TEST DATA. — Information follows which will be helpful in determining the operation of 100-CPS loop phase detector A1 and sweep multivibrator V4. Refer to figure 4-77 for the circuit location and figures 5-96 and 5-97 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Voltage at junction of capacitors 1A6A1A5A1C1 and 1A6A1A5A1C2: -6 VDC minimum. If voltage is low, refer to paragraph 4-3f(3).

(b) Refer to paragraph 5-3 for general information and paragraph 5-3d for specific alignment procedures of 1A6A1A5A1C5.

g. INCREMENTAL DIVIDER CIRCUITS 1A6A1A10, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. — The incremental dividers functional section (see figure 4-78) consists of three locked dividers and two mixers. The incremental divider receives signals from the 10-KC loop functional section, the 1-KC loop functional section, and the 100-CPS loop functional section. It combines and divides these signals and applies the resultant composite secondary loop signal to the main loop functional section. The 1.964- to 2.000-MC input from the 100-CPS functional section is divided to a 0.491- to 0.500-MC signal by 4 to 1 locked divider A1 and combined in third mixer A2 with the 3.21- to 3.30-MC input signal from the 1-KC loop functional section. The 3.701- to 3.800-MC output of the third mixer is divided to a 0.7402- to 0.7600-MC signal by 5 to 1 locked divider A3 and combined in fourth mixer A4 with the 7.06- to 7.24-MC input from the 10-KC loop functional section. The composite secondary loop output of the fourth mixer, in the 7.8002- to 8.0000 MC frequency range, is divided to a 3.9001- to 4.0000-MC signal by 2 to 1 locked divider A5 and applied to the main loop functional section.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. — Information follows which will be helpful in determining the overall performance of the incremental dividers functional section. Refer to figure 4-78 for the circuit location and figures 5-80 and 5-107 through 5-111 for the physical location of test points. The test equipment required is an electronic counter and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

To change the synthesizer frequency manually, first set the desired frequency on the MANUAL SETTING digital switch. Remember that the actual output frequency of the synthesizer is 1.75 MC higher than the switch setting. Then set the SERVO MODE switch to MANUAL CHANNEL AUTO and throw the MOTOR DRIVE ON switch to ON. Press the START switch and after completion of tuning cycle throw MOTOR DRIVE ON switch off. To change incremental frequencies of 10 KC, 1 KC, and 100 cycles, it is only necessary to set the applicable digit on the MANUAL SETTING digital switch.

(a) RF output (1A6A1A10XA5-9) (BC) : 3.9001 to 4.0000 MC in 10-KC steps for incremental changes in 10-KC loop frequency, 1-KC steps for incremental changes in 1-KC loop frequency, and 100-cycle steps for incremental changes in 100-cycle loop frequency, at 1.5 VRMS minimum. If correct, incremental divider functional section is operating properly.

(b) RF input from 10-KC loop (1A6A1A10E3) (BD) : 7.06 to 7.24 MC in 20-KC steps at 0.2 VRMS minimum at 7.14 MC. If frequency is unstable or incorrect, refer to paragraph 4-3d.

(c) RF input from 1-KC loop (1A6A1A10E4) (BH) : 3.21 to 3.30 MC in 10-KC steps at 0.3 VP-P minimum at 3.25 MC. If frequency is unstable or incorrect, refer to paragraph 4-3e.

(d) RF input from 100-cycle loop (1A6A1A10E5) (BG) : 1.964 to 2.000 MC in 4-KC steps at 0.5 VRMS minimum at 1.980 MC. If frequency is unstable or incorrect, refer to paragraph 4-3f.

(e) DC input voltage (1A6A1A10-E6): +28 VDC.

(3) 4 to 1 LOCKED DIVIDER 1A6A1-A10A1, CIRCUIT DESCRIPTION. — The 4 to 1 locked divider (see figure 4-13) is a grounded base oscillator, in a common emitter configuration, which is free running at a frequency slightly above 500 KC. Resistors R1 and R2 set the base operating parameters for transistor Q1. The collector tuned circuit consists of inductor L1 and capacitors C1 and C3. Positive feedback is from collector to emitter. The 1.964- to 2.000-MC, 100-CPS loop input signal is applied to the base of transistor Q1. Every fourth cycle of the input signal synchronizes (phase locks) the oscillator fundamental frequency and provides for a stable output. The 0.491- to 0.500-MC output of transistor Q1 is combined in third mixer 1A6A1A10A2 with the 1-KC loop signal.

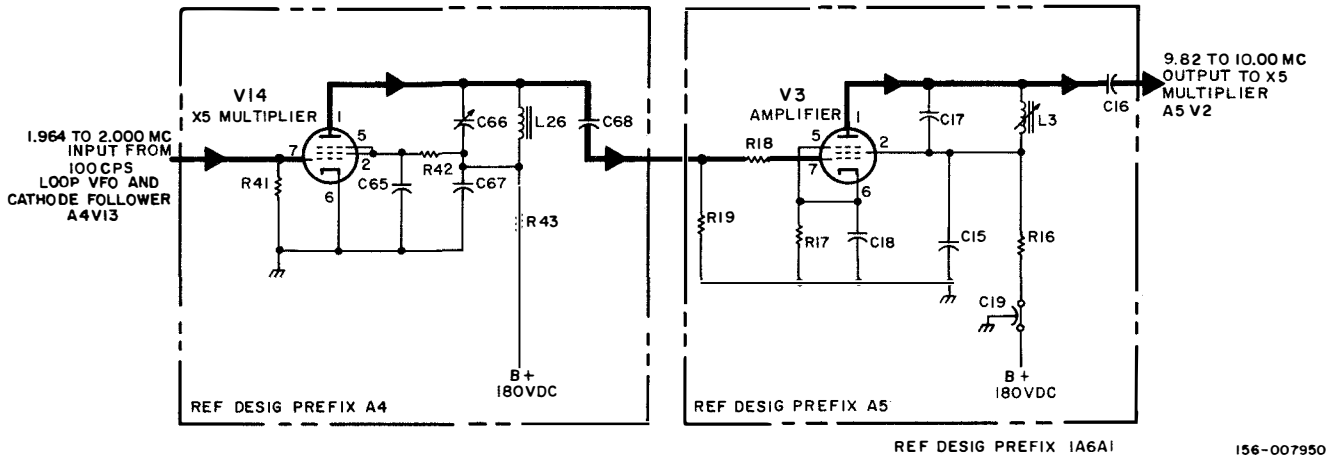


Figure 4-11. Synthesizer 1A6, 100-Cycle Loop X5 Multiplier and Amplifier, Simplified Schematic Diagram

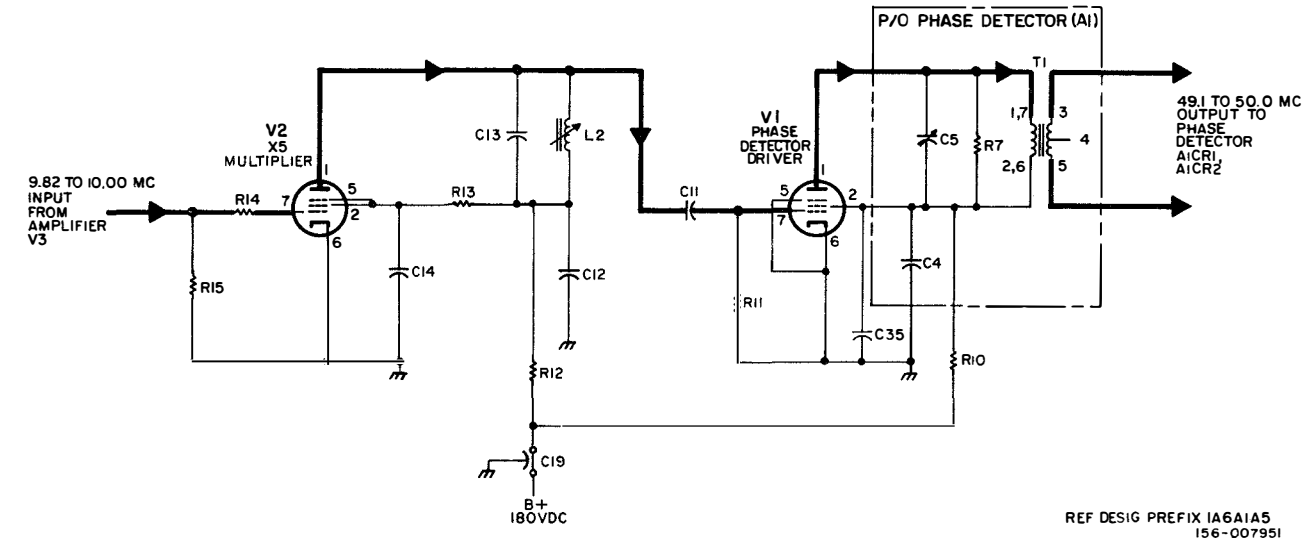


Figure 4-12. Synthesizer 1A6, 100-Cylce Loop X5 Multiplier and Phase Detector Driver, Simplified Schematic Diagram

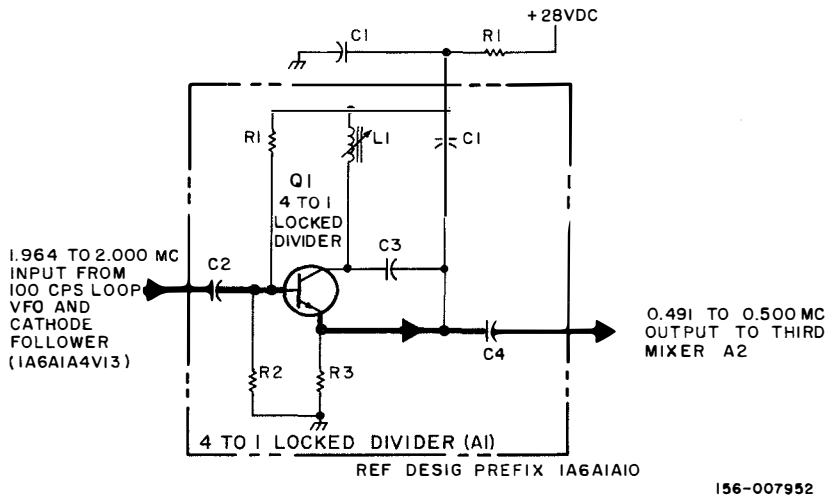


Figure 4-13. 4 to 1 Locked Divider, Simplified Schematic Diagram

(4) 4 to 1 LOCKED DIVIDER 1A6A1-A10A1, TEST DATA. - Information follows which will be helpful in determining the performance of 4 to 1 locked divider A1. Refer to figure 4-78 for the circuit location and figures 5-80 and 5-107 for the physical location of test points. The test equipment required is an electronic counter, a VTVM and an RF VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160055.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A10XA1-9) (BI): 0.491 to 0.500-MC in 1-KC steps for incremental changes of 100 cycles at 1.7 VRMS minimum. If correct, 4 to 1 locked divider is operating properly.

(b) RF input (1A6A1A10XA1-2) (BG): 1.964 to 2.000 MC in 4-KC steps at 0.5 VRMS minimum. If frequency is unstable or incorrect refer to paragraph 4-3i.

(c) DC input voltage (1A6A1A-10XA1-1): +21 VDC.

(d) Refer to figure 5-201 for transistor voltage measurements.

(e) Refer to paragraph 5-3 for general information and paragraph 5-3e for specific alignment procedure of 1A6A1A10A1L1.

(5) THIRD MIXER 1A6A1A10A2, CIRCUIT DESCRIPTION. - The third mixer (see figure 4-14) consists of diode mixer CR1 and CR2 and amplifier Q1. The inputs to the diode mixer are the 0.491- to 0.500-MC signal from 4 to 1 locked divider 1A6A1A10A1 and the 3.21- to 3.30-MC signal from the 1-KC loop functional section. The output of the diode mixer is a large number of signals including the sum and difference of the two inputs. Inductor L1 and capacitors C1 and C2 form a tank circuit tuned to resonate at a frequency corresponding to the sum of the two input signals. The 3.701- to 3.800-MC output of the tank circuit is applied to the base of common emitter amplifier Q1. The collector circuit of transistor Q1 is tuned to a frequency in the 3.701- to 3.800-MC range by a tank circuit consisting of the secondary winding of transformer T2 and capacitor C3. The output from the secondary

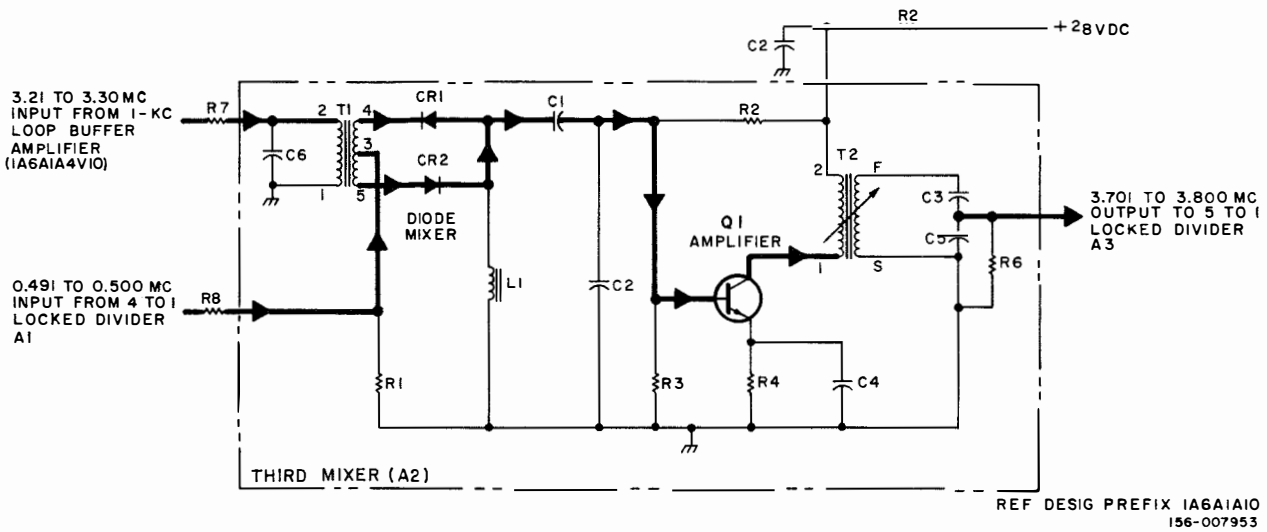


Figure 4-14. Synthesizer 1A6, Third Mixer, Simplified Schematic Diagram

winding of T2 is applied to 5 to 1 locked divider 1A6A1A10A3. See Handbook of Electronic Circuits, NAVSHIPS 900,000.102 for a description of the diode mixer and common emitter amplifier circuits.

(6) THIRD MIXER 1A6A1A10A2, TEST DATA. - Information follows which will be helpful in determining the performance of third mixer A2. Refer to figure 4-78 for the circuit location and figure 5-80 and 5-108 for the physical location of test points. The test equipment required is an electronic counter, a VTVM and an RF VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160055.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A10XA2-9) (BF) : 3.701 to 3.800-MC in 10-KC steps for incremental changes in 10-KC loop frequency and 1-KC steps for incremental changes in 100-cycle loop frequency at 1.0 VRMS minimum. If correct, third mixer is operating properly.

(b) RF input from 1-KC loop (1A6A1A10XA2-5) (BH) :3.21 to 3.30 MC in 10-KC steps at 0.3 VP-P minimum. If unstable or incorrect, refer to paragraph 4-3e.

(c) RF input from 4 to 1 locked divider (1A6A1A10XA2-2) (BI) : 0.491 to 0.500 MC in 1-KC steps at 1.7 VRMS minimum. If unstable or incorrect, refer to paragraph 4-3g(2).

(d) DC input voltage (1A6A1A-10XA2-1): +13 VDC.

(e) Refer to figure 5-201 for transistor voltage measurements.

(f) Refer to paragraph 5-3 for general information and paragraph 5-3e for specific alignment procedures of 1A6A1A10A2T2.

(7) 5 to 1 LOCKED DIVIDER 1A6A1A10A3, CIRCUIT DESCRIPTION. - The 5 to 1 locked divider receives the 3.701- to 3.800-MC signal from third mixer 1A6A1A10A2, divides it by a factor of five, and applies the resultant 0.7402- to 0.7600-MC signal to fourth mixer

1A6A1A10A4. The operation of 5 to 1 locked divider A3 is identical to the operation of 4 to 1 locked divider 1A6A1A10A1 described in paragraph 4-3g(3).

(8) 5 to 1 LOCKED DIVIDER 1A6A1A10A3, TEST DATA. - Information follows which will be helpful in determining the performance of 5 to 1 locked divider A3. Refer to figure 4-78 for the circuit location and figures 5-80 and 5-109 for the physical location of test points. The test equipment required is an electronic counter, a VTVM and an RF VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160055.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A10XA3-9) (BE): 0.7402 to 0.7600 MC in 2-KC steps for incremental changes in 1-KC loop frequency and 200-cycle steps for incremental changes in 100-cycle loop frequency at 2.0 VRMS minimum. If correct, 5 to 1 locked divider is operating properly.

(b) RF input (1A6A1A10XA3-2) (BF): 3.701 to 3.800 MC in 10-KC steps for incremental changes in 1-KC loop frequency and 1-KC steps for incremental changes in 100-cycle loop frequency at 1.0 VRMS minimum. If frequency is unstable or incorrect, refer to paragraph 4-3g(5).

(c) DC input voltage (1A6A1A-10XA3-1): +20 VDC.

(d) Refer to figure 5-201 for transistor voltage measurements.

(e) Refer to paragraph 5-3 for general information and paragraph 5-3e for specific alignment procedures of 1A6A1A10A3L1.

(9) FOURTH MIXER 1A6A1A10A4, CIRCUIT DESCRIPTION. - The fourth mixer receives the 0.7402- to 0.7600-MC signal from 5 to 1 locked divider 1A6A1A10A3 (combined 100-CPS loop and 1-KC loop signal) and the 7.06- to 7.24-MC signal from the 10-KC loop functional section. The two signals are combined to produce a composite secondary loop signal in the 7.8002- to 8.0000-MC frequency range. The output of the fourth mixer is applied to 2 to 1 locked divider 1A6A1A10A5. The operation of fourth mixer A4 is identical to the operation of third mixer 1A6A1A10A2 described in paragraph 4-3g(5).

(10) FOURTH MIXER 1A6A1A10A4, TEST DATA. - Information follows which will be helpful in determining the performance of fourth mixer A4. Refer to figure 4-78 for the circuit location and figure 5-80 and 5-110 for the physical location of test points. The test equipment required is an electronic counter, a VTVM, and an RF VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160055.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A10XA4-9) (BJ): 7.8002 to 8.0000 MC in 20-KC steps for incremental changes in 10-KC loop frequency; 2-KC steps for incremental changes in 1-KC loop frequency, and 200-cycle steps for incremental changes in 100-cycle loop frequency at 0.3 VRMS minimum. If correct, fourth mixer is operating properly.

(b) RF input from 10-KC loop (1A6A1A10XA4-5) (BD): 7.06 to 7.24 MC in 20-KC steps at 0.2 VRMS minimum. If frequency is unstable or incorrect refer to paragraph 4-3d.

(c) RF input from 5 to 1 locked divider (1A6A1A10XA4-2) (BE): 0.7402 to 0.7600 MC in 2-KC steps for incremental changes in 1-KC loop frequency and 200-cycle steps for incremental changes in 100-cycle loop frequency at 2 VRMS minimum. If frequency is unstable or incorrect, refer to paragraph 4-3g(7).

(d) DC input voltage (1A6A1A-10XA4-1): +12.5 VDC.

(e) Refer to figure 5-201 for transistor voltage measurements.

(f) Refer to paragraph 5-3 for general information and paragraph 5-3e for specific alignment procedure of 1A6A1A10A4T2.

(11) 2 to 1 LOCKED DIVIDER 1A6A-1A10A5, CIRCUIT DESCRIPTION. - The 2 to 1 locked divider receives the 7.8002- to 8.0000-MC signal from fourth mixer 1A6A1A10A4, divides it by a factor of two, and applies the resultant 3.9001- to 4.0000-MC signal to the main loop functional section. The operation of 2 to 1 locked divider A2 is identical to the operation of 4 to 1 locked divider 1A6A1A10A1 described in paragraph 4-3g(3).

(12) 2 to 1 LOCKED DIVIDER 1A6A1-A10A5, TEST DATA. - Information follows which will be helpful in determining the performance of 2 to 1 locked divider A5. Refer to figure 4-78 for the circuit location and figure 5-80 and 5-111 for the physical location of test points. The test equipment required is an electronic counter, a VTVM and an RF VTVM (refer to Section 1 for type designations). Set MANUAL SETTING digital switch to 160055.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A6A1A10XA5-9) (BC): 3.9001 to 4.0000 MC in 10-KC steps for incremental changes in 10-KC loop frequency, 1-KC step for incremental changes in 1-KC loop frequency, and 100-cycle steps for incremental changes in 100-cycle loop frequency at 1.5 VRMS minimum. If correct, 2 to 1 locked divider is operating properly.

(b) RF input (1A6A1A10XA5-2) (BJ): 7.8002 to 8.0000 MC in 20-KC steps for incremental changes in 10-KC loop frequency, 2-KC steps for incremental changes in 1-KC loop frequency, and 200-cycle steps for incremental changes in 100-cycle loop frequency at 0.3 VRMS minimum. If frequency is unstable or incorrect, refer to paragraph 4-3g(a).

(c) DC input voltage (1A6A1A-10XA5-1): +19 VDC.

(d) Refer to figure 5-201 for transistor voltage measurements.

(e) Refer to paragraph 5-3 for general information and paragraph 5-3e for specific alignment procedures of 1A6A1A10A5L1.

h. MAIN LOOP CIRCUITS 1A6A1A4, 1A6A1A6, 1A6A1A11, AND 1A6A1A13, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. - The main loop functional section (see figure 4-79) produces the main 17.75- to 35.60-MC synthesizer output signal which is applied to converter 1A3. It consists of a reactance controlled VFO, a wideband amplifier, two mixers, two IF amplifiers, a limiter, and a discriminator. The VFO generates the selected frequency in the 17.75- to 35.60-MC range. During automatic operation the main loop VFO is tuned by a servo which responds to analog information from the memory-control. During emergency manual operation, the main loop VFO is tuned by front-panel MANUAL TUNE control. The output of the VFO is amplified by wideband amplifier A13 and applied to first mixer A11. The first mixer combines the VFO signal with the 22.1- to 40.0-MC spectrum generator signal from the reference circuits functional section to produce the 4.3001- to 4.4000-MC first IF signal. The spectrum generator tuning controls and the main loop tuning controls are ganged; therefore, a change in the main loop VFO frequency results in a spectrum generator frequency change. However, the changes in the two frequencies are not the same. The spectrum generator frequency is changed in 100-KC steps, but the main loop VFO frequency is changed (by the secondary loops) in 10-KC, 1-KC, and 100-CPS steps. The resulting first mixer output varies over a range of 99.9 KC from 4.4000 to 4.3001 MC. The output of the first mixer is amplified by first IF amplifier A4V11 and applied to the second mixer. The second mixer combines the 4.4000- to 4.3001-MC signal with the 3.9001- to 4.0000-MC composite secondary loop signal from the loop combiner functional section at a frequency of 400-KC. The output of the second mixer is amplified by second IF amplifier A4V12, set at a constant level by limiter A4V15, and applied to the discriminator. The discriminator compares this 400-KC signal with the 400-KC reference signal from the reference circuits functional section. If a frequency or phase difference exists, a DC error voltage is produced. The DC error voltage is applied to the main loop reactance control circuit to correct the main loop VFO frequency. The output of the main loop is amplified by output amplifier A6V3 and supplied to the converter unit.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. - Information follows which is helpful in determining the performance of the main loop circuits. Refer to figure 4-79 for the circuit location and figures 5-91, 5-99 and 5-100 for the physical location of test points. The test equipment required is an electronic counter, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

To change the synthesizer frequency manually, first set the desired frequency on the MANUAL SETTING digital switch. Remember that the actual output frequency of the synthesizer is 1.75 MC higher than the switch setting. Then set the SERVO MODE switch to MANUAL CHANNEL AUTO and throw the MOTOR DRIVE ON switch to ON. Press the START switch and after completion of tuning cycle throw MOTOR DRIVE ON switch off. To change incremental frequencies of 10 KC, 1 KC, and 100 cycles, it is

only necessary to set the applicable digit on the MANUAL SETTING digital switch.

(a) RF output (1A6A1J3 (35)) 17.75- to 35.60-MC in 100-cycle steps at 1.0 VRMS minimum. If correct, main loop circuits are operating properly.

(b) RF input from discriminator driver 1A6A1A4V16-1 (AC): 400 KC at 9.0 VRMS minimum. If frequency is unstable or incorrect, refer to paragraph 4-3b.

(c) RF input from incremental divider circuits (1A6A1A4E35) (Z): 3.9001 to 4.0000 MC in 10-KC steps for incremental changes in 10-KC loop frequency, 1-KC steps for incremental changes in 1-KC loop frequency, and 100-cycle steps for incremental changes in 100-cycle loop frequency at 0.23 VRMS minimum. If frequency is unstable or incorrect, refer to paragraph 4-3g.

(d) Check front panel TEST METER reading with TEST METER switch in LIMITER, 180V B+, 100-KC LOOP FINE MAN TUNE positions. Refer to table 3-12 for typical meter readings.

(3) VFO AND REACTANCE CONTROL CIRCUITS 1A6A1A6, CIRCUIT DESCRIPTION. - The main loop VFO and associated circuitry (see figure 4-15), is a reverse feedback oscillator which generates frequencies in the 17.75- to 35.60-MC range. The oscillator is similar to a tuned plate Armstrong oscillator. Regenerative feedback is provided by capacitor C13 and transformer T1. Refer to NAVSHIPS 900,000.102 for a description of the tuned plate Armstrong oscillator. The oscillator is coarsely tuned by capacitor C12A which is ganged with the spectrum generator and output amplifier tuning controls. During automatic operation, capacitor C12A is motor driven in response to information from the automatic tuning circuits. During emergency manual operation, tuning is accomplished with front-panel MANUAL TUNE control. Fine tuning of the oscillator in 10-KC, 1-KC, and 100-cycle increments is accomplished by reactance control V1. The DC error voltage input from the discriminator is converted to a varying inductive reactance by the reactance tube. The reactance tube

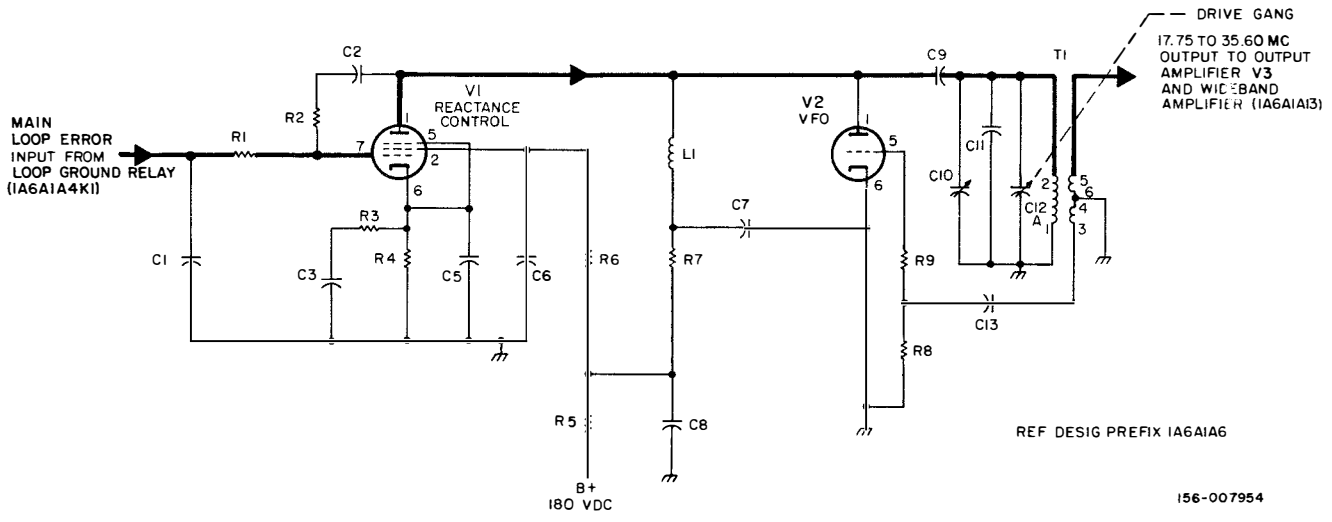


Figure 4-15. Synthesizer 1A6, Main Loop VFO and Reactance Control Circuits, Simplified Schematic Diagram

shunts the VFO and is part of its resonant circuit. The RF current from V1 also flows through the VFO tank. Voltage of the VFO also appears at the plate of V1, and the phase shifting network, capacitor C2 and resistor R2, shifts the phase of the voltage fed to the grid of V1 by 90 degrees. Since the resistance of R2 is large (10:1) compared to the reactance of the grid to cathode interelectrode capacitance of V1, the RF current flowing through R2 and C2 is in phase with the main loop VFO tank voltage. Therefore, the grid voltage of V1 is 90 degrees out of phase with the plate voltage. The plate current of V1 is in phase with the grid voltage and lags the plate voltage by 90 degrees; the current through V1 appears inductive and the tube acts as a shunting reactance across the main loop VFO tank circuit. The amount of reactance is inversely proportional to the Gm of the tube, and is determined by the bias or error voltage applied to the grid.

(4) VFO AND REACTANCE CONTROL CIRCUITS 1A6A1A6, TEST DATA. — Information follows which will be helpful in determining the performance of the VFO and reactance control. Refer to figure 4-79 for the circuit location and figures 5-91 and 5-100 for the physical location of test points.

Note

Because operational tests cannot be made without loading the oscillator circuits, voltage and resistance measurements are recommended only.

The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) DC input voltage (1A6A1A6E6): +180 VDC.

(b) Refer to figure 5-197 for voltage and resistance measurements.

(c) Refer to paragraph 5-3 for general information and paragraph 5-3f(3) for specific alignment procedure of 1A6A1A6C10.

(5) WIDEBAND AMPLIFIER 1A6A1A13, CIRCUIT DESCRIPTION. — The wideband amplifier (see figure 5-197) receives the 17.75- to 35.60-MC output of main loop VFO 1A6A1A6V2. The signal is amplified and applied to first mixer 1A6A1A11. The 17.75- to 35.60-MC signal is applied to the base of common emitter amplifier Q1. The base bias of Q1 is set by resistors R2 and R4. The output from the collector of Q1 is coupled through capacitor C4 to the base of common emitter amplifier Q2. The base bias of Q2 is set by resistors R6 and R8. The output from the collector of Q2 is coupled through transformer T1 to first mixer 1A6A1A11. The collector circuit of Q2 is tuned by capacitor C7.

(6) WIDEBAND AMPLIFIER 1A6A1A13, TEST DATA. — Information follows which will be helpful in determining the performance of the wideband amplifier. Refer to figure 4-79 for the circuit location and figure 5-116 for the physical location of test points. The test equipment required is an electronic counter, a VTVM, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of section 4 for additional test data.

(a) RF output (1A6A1A13E1) (W): 17.75- to 35.60-MC in 100-cycle steps at 1.5 VRMS minimum at 24 MC. If correct, wideband amplifier is operating properly.

(b) RF input (1A6A1A13E3): 17.75- to 35.60-MC in 100-cycle steps at 0.11 VRMS minimum. If frequency is unstable or incorrect refer to paragraph 4-3h(3).

(c) DC input voltage (1A6A1A13E2): +28 VDC.

(d) Refer to figure 5-204 for transistor voltage measurements.

(e) Refer to paragraph 5-3 for general information and paragraph 5-3f(4) for specific alignment procedure of 1A6A1A13C7.

(7) FIRST MIXER 1A6A1A11, CIRCUIT DESCRIPTION. — The first mixer receives the 22.1- to 40.0-MC signal from the spectrum generator section of 1A6A1A6 and the 17.75- to 35.60-MC main loop VFO signal from wideband amplifier 1A6A1A13 (see figure 5-202). The 22.1- to 40.0-MC signal is applied to the primary winding of transformer T1 and the 17.75- to 35.60-MC signal is applied to the secondary center tap. The two signals are mixed by diode mixer CR1 and CR2. Variable resistor R3 balances the DC currents flowing through the circuit. The output of the mixer is coupled to the primary winding of transformer T2. The secondary of T2 and capacitor C3 form a parallel resonant (tank) circuit tuned to the difference of the two input signals. The output of T2 is coupled by capacitor C2 to transformer T3. Transformer T3 is also tuned to

the difference of the two input signals. The output of transformer T3 is applied to first IF amplifier 1A6A1A4V11.

(8) FIRST MIXER 1A6A1A11, TEST DATA. — Information follows which will be helpful in determining the performance of the first mixer. Refer to figure 4-79 for the circuit location and figures 5-112 and 5-116 for the physical location of test points. The test equipment required is an electronic counter, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF input from wideband amplifier (1A6A1A11E1) (W) : 17.75- to 35.60-MC in 100-cycle steps at 1.5 VRMS minimum. If frequency is unstable or incorrect, refer to paragraph 4-3h(5).

(b) Refer to paragraph 5-3 for general information and paragraph 5-3f(6) for specific alignment procedures of 1A6A1A11R3, 1A6A1A11T2, and 1A6A1A11T3.

(9) FIRST AND SECOND IF AMPLIFIERS, SECOND MIXER, AND LIMITER 1A6A1A4. — First IF amplifier V11 (see figure 5-195) receives the 4.3001- to 4.4000-MC signal from first mixer 1A6A1A11. The signal is amplified by V11 and coupled through transformer T2 to second mixer CR2 and CR3. The second mixer also receives the 3.9001- to 4.0000-MC signal from 2 to 1 locked divider 1A6A1A10A5. The two signals are combined to produce a difference frequency and are applied to the grid of second IF amplifier V12. The plate circuit of V12 is tuned to 400 KC (difference frequency) by capacitor C74 and the primary winding of transformer T3. The 400 KC output of V12 is coupled through T3 to the grid of limiter V15. Grid leak limiter V15 clips the negative and positive peaks of the input signal at a predetermined level. During the positive peak of the input signal, grid current flows and capacitor C76 charges through the low cathode-to-grid resistance of V15 and the secondary of T3. This clips the positive peak. As the input signal swings negative, grid current ceases to flow and C76 discharges through resistor R49. The resistance of R49 is large compared to the charging resistance; therefore, the capacitor cannot fully discharge. This results in an average bias level on the grid of V15 sufficient to cut off the tube during the negative peaks of the input signal. This clips the negative peaks. The output of the limiter is applied to the discriminator. The average bias level at the junction of capacitor C76 and resistor R49 is applied to the TEST METER for monitoring.

(10) FIRST AND SECOND IF AMPLIFIERS, SECOND MIXER, AND LIMITER 1A6A1A4, TEST DATA. — Information follows which will be helpful in determining the performance of the first and second IF amplifiers, second mixer, and limiter. Refer to figure 4-79 for the circuit location and figures 5-90 and 5-91 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF input from 2 to 1 locked divider (1A6A1A4E35) (Z): 3.9001 to 4.000 MC in 100-CPS steps for incremental changes in 10-KC loop frequency, 1-KC steps for incremental changes in 1-KC loop frequency, and 100-cycle steps for incremental changes in 100-cycle loop frequency at 0.23 VRMS minimum. If frequency is unstable or incorrect, refer to paragraph 4-3g.

(b) Bias voltage (1A6A1A4XV15-7): -10 VDC minimum.

(c) Refer to figure 5-195 for voltage and resistance measurements.

(d) Refer to paragraph 5-3 for general information and paragraph 5-3f(5), and (8), (10) and (11) for specific alignment procedures of 1A6A1A4C35, 1A6A1A4T3, and 1A6A1A4T4.

(11) DISCRIMINATOR 1A6A1A4, CIRCUIT DESCRIPTION. — Discriminator CR4 and CR5 (see figure 4-16) receives the 400-KC composite loop signal from the limiter. It also receives a 400-KC reference signal from the reference circuits functional section discriminator driver. The signals are compared to produce a DC error voltage corresponding to phase or frequency difference. Discriminator CR4 and CR5 is a modified Foster-Seeley circuit providing simultaneous frequency and phase comparison. The 400-KC signal from the limiter appears across the secondary winding of transformer T4. When T4 is tuned to 400-KC, a 90-degree phase shift occurs between the primary and secondary windings. If the input frequency from the limiter is the same as the tuned frequency of the discriminator, diodes CR4 and CR5 alternately conduct on opposite halves of the input signal cycle. Equal conduction of the diodes charges capacitors C84 and C85 equally with opposite polarities, resulting in zero output from the discriminator. If the input frequency from the limiter is below the discriminator frequency, diode CR4 conducts more than CR5 and capacitor C84 charges more than C85. This results in a

negative output from the discriminator. If the input frequency is above the discriminator frequency, the opposite occurs and the discriminator output is positive. The phase detector portion of the circuit operates in a manner similar to the 10-KC loop phase detector described in paragraph 4-3d(9). The signal from the discriminator driver appears at the discriminator together with the signal from the limiter. The two signals are phase compared and the output sweeps the limiter signal through phase coincidence with the discriminator driver signal. The phase discriminator operates when the limiter signal is swept through frequency coincidence so that the DC output of the phase discriminator can phase lock the limiter signal to the discriminator driver signal. The output of the discriminator is supplied to the main loop reactance control A6V1.

(12) DISCRIMINATOR 1A6A1A4, TEST DATA. — Information which follows will be helpful in determining the performance of the discriminator. Refer to figure 4-79 for the circuit location and figure 5-91 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) DC error output (1A6A1A4E22) (CM) : ±0.5 VDC. If error voltage is large, refer to paragraphs 4-3b and 4-3h(9).

(b) Check front panel TEST METER reading with TEST METER switch in 100-KC LOOP-FINE MAN TUNE position. Refer to table 3-12 for typical meter reading.

(c) Refer to paragraph 5-3 for general information and paragraph 5-3f(9), (10) and (11) for specific alignment procedures of 1A6A1A4T4 and 1A6A1A4T5.

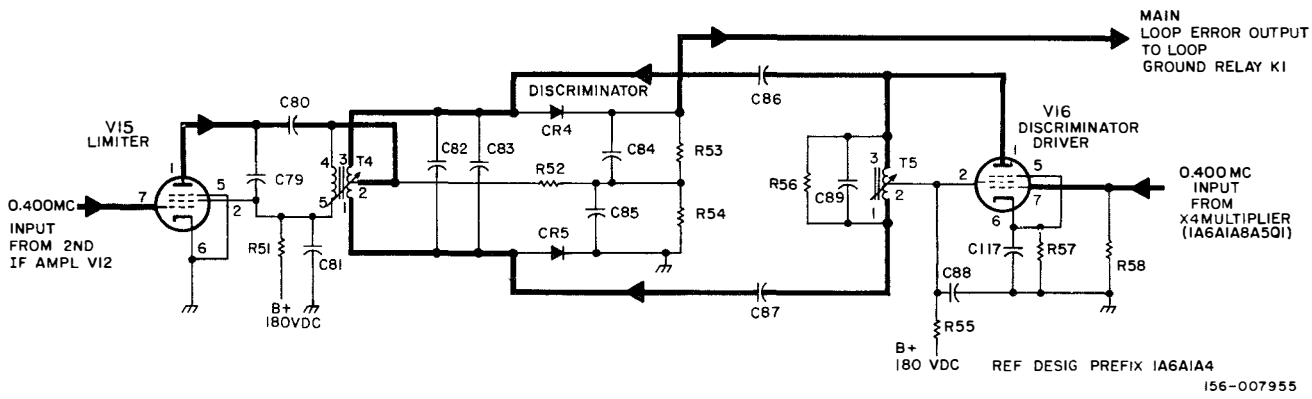


Figure 4-16. Synthesizer 1A6, Discriminator, Simplified Schematic Diagram

i. MEMORY CONTROL SECTION, FUNCTIONAL DESCRIPTION.

(1) OVERALL FUNCTIONAL DESCRIPTION. — The memory control section is composed of three subsections: an analog memory (mounted on top of the synthesizer and referred to as 1A5) which provides band and frequency selection, a digital timing memory (programmer located in synthesizer 1A6) which provides a three-slot time sequence program, and servo amplifiers which control servo motors in synthesizer 1A6 and converter 1A3. The analog memory subsection (1A5) contains seven matrix sections which are programmed for ten preset frequency channels. The first matrix section is programmed to select the operating bands, the second matrix section is programmed to select the first significant figure of the synthesizer output frequency, and the remaining five matrix sections are programmed to select the operating frequency. The digital timing memory (programmer) consists of trigger, timer, and coder circuits which operate applicable relays that determine the correct sequence of synthesizer and converter tuning. When a new frequency channel is selected at transmitter control units 2 and 3 or RF assembly 1A8, a pulse is applied to the trigger circuits of the programmer. This starts the timing sequence which coarse-tunes the synthesizer in the proper order. The timing sequence of operation of the synthesizer and converter is the same for all channels. The servo amplifier subsection converts the analog information from the analog memory subsection to motor control information which determines the direction of rotation of the servo motors in the synthesizer and converter units. The time sequence of operation of the servo motors is determined by the programmer timing sequence.

(2) ANALOG MEMORY SUBSECTION, CIRCUIT DESCRIPTION. — The analog memory subsection consists of matrix sections, relays, digital switches, and channel indicator lamps. This subsection provides an analog output voltage which is applied to the servo amplifier subsection together with an analog voltage from servo motor driven potentiometer 1A6A1A7R1 (see figure 4-17). When the radio set is energized and a frequency channel is selected, the autotune system in RF assembly 1A8 begins its sequence of operation (refer to paragraphs 4-6b(11)(a) through 4-6b(11)(a)(3)). At the end of the first direction of rotation of the autotune system, channel control switch 1A8S240B in the RF assembly completes the circuit to a set of relays (1A5A1K1 through 1A5A1K22) in the analog memory subsection. At the same time it sends a start pulse to the programmer subsection to initiate the digital three-slot timing sequence. To understand the functional operation of the analog memory subsection, assume that synthesizer 1A6 is being tuned to an output frequency of 23.854100 MC on channel 1 (see figure 4-17). (Remember that the output frequency of synthesizer 1A6 is 1.75-MC higher than the tuning digits selected.) At the end of the first direction of rotation of the autotune system, a ground from channel control switch 1A8S240B is applied to relays 1A5A1K1 and 1A5A1K2 to actuate them. Shorting plugs are inserted in the 10-MC matrix 20-MC hole, 1-MC matrix 2-MC hole, 100-KC matrix 100-KC hole, 10-KC matrix 0-KC hole, 1-KC matrix 4-KC hole, and 100-CPS matrix 100-CPS hole. The series circuit for the first four significant figures is through resistors 1A5A1R6 and 1A5A1R5, 20-MC shorting plug, contacts 8 and 7 of relay 1A5A1K1, resistors 1A5A1R7 and 1A5A1R8, 1-MC shorting plug, contacts 6 and 5 of relay 1A5A1K1, resistor 1A5A1R16, 100-KC shorting plug, contacts 10 and 9 of relay 1A5A1K1, contacts 4 and 3 of relay 1A5A1K32 (which is actuated by a shorting plug in the 10-KC matrix 0-KC hole), and relays 1A6A1K1 and 1A6A1K3 to the servo amplifier subsection. The 10-KC matrix (0 digit) shorting plug provides a 28-VDC input from relay 1A5A1K2 to incremental relay 1A6A1A2A1K1. By adding the resistance of resistors 1A5A1R6, 1A5A1R5, 1A5A1R7, 1A5A1R8, and 1A5A1R16, the total value adds up to 2385 which corresponds to the first four significant figures of the synthesizer output frequency (not the selected tuning digits). An analog voltage from the junction of contact 3 of relay 1A5A1K32 and resistor 1A5A1R1 is applied as the low input to the servo amplifier subsection. A high input from the arm of potentiometer 1A6A1A7R1 is also applied to the servo amplifier subsection (see figure 4-17). When the programmed subsection is in sequence 1, the high and low inputs to the servo amplifier subsection cause servo motor 1A6A1A7B1, which is mechanically coupled to potentiometer 1A6A1-A7R1, to rotate until the high and low inputs are equal. Servo motor 1A6A1A7B1 is also mechanically coupled to the main loop VFO and spectrum generator gang (1A6A1A6) to coarse tune the synthesizer output frequency. The 1-KC and 100-cycle digits of the synthesizer are selected by parallel 28-VDC inputs to the 1-KC and 100-cycle matrices from relay 1A5A1K2. In the 1-KC matrix, 28-VDC is fed from contacts 5 and 6 of relay 1A5A1K2 through the 1-KC (4 digit) shorting plug to incremental relay 1A6A1A2A3K5, to select the 4-KC digit of the operating frequency. In the 100-cycle matrix, +28-VDC is fed from

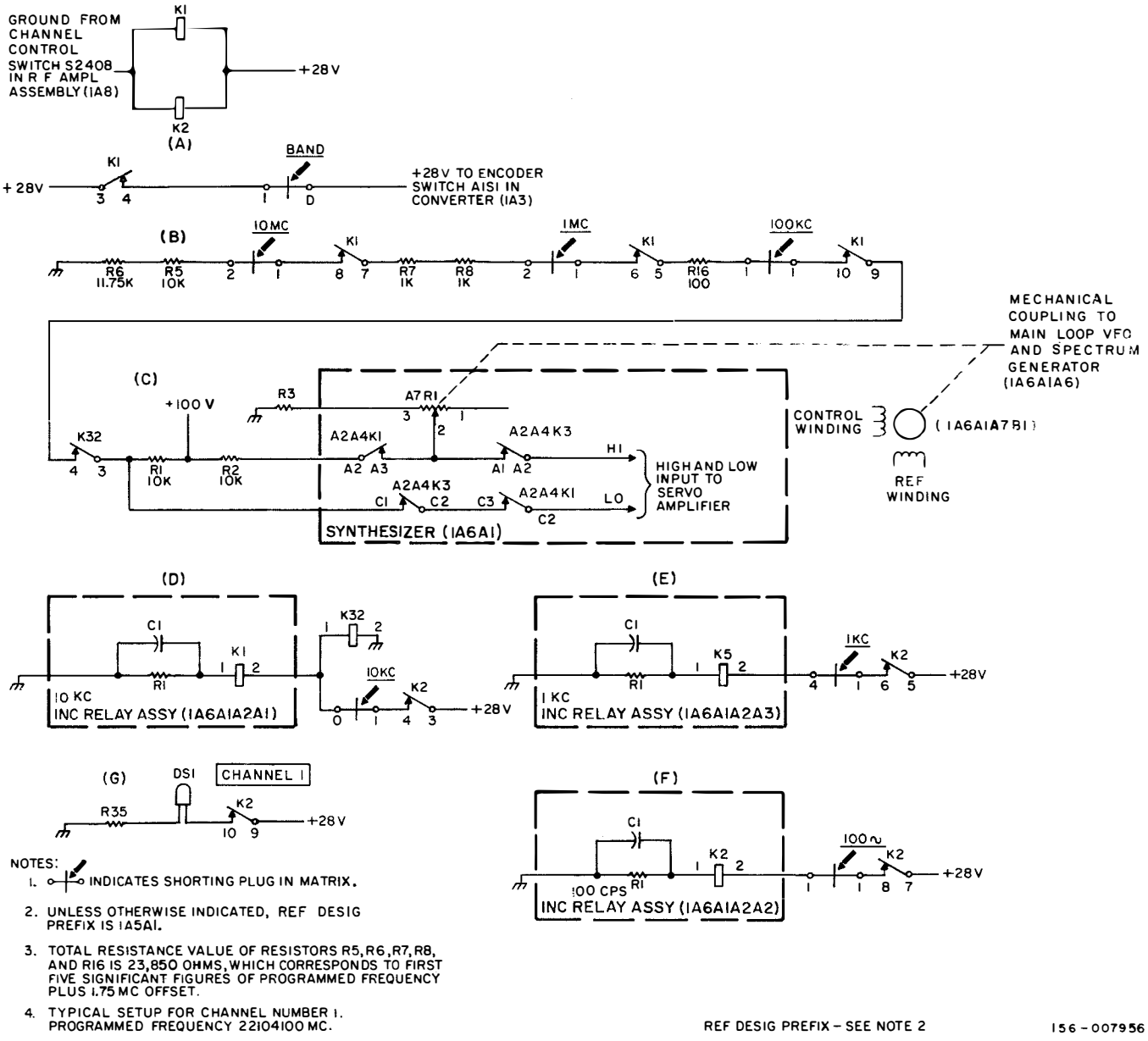


Figure 4-17. Synthesizer 1A6, Analog Memory Section, Channel 1 Operation, Simplified Schematic Diagram

contacts 7 and 8 of relay 1A5A1K2 through the 100-cycle (1 digit) shorting plug to incremental relay 1A6A1A2A2K2, to select the 100-cycle digit of the operating frequency. Relay 1A5A1K2 contacts 9 and 10 provides +28-VDC to channel 1 indicator lamp 1A5DS1 to indicate channel 1 is active. The 10-KC, 1-KC and 100-cycle incremental relay assemblies in the synthesizer insert the proper amount of inductance in the secondary loop circuits (10 KC, 1 KC, and 100 cycle) to obtain the proper secondary loop VFO operating frequencies. (Refer to paragraphs 4-3d, e, and f.)

(3) DIGITAL TIMING MEMORY SUBSECTION, CIRCUIT DESCRIPTION. — The digital timing memory (programmer) subsection (see figures 4-81 and 5-194) consists of trigger subassembly 1A6A1A3A1, timer subassembly 1A6A1A3A2, and coder subassembly 1A6A1A3A3. The programmer provides a three-slot time sequence which controls the sequence of operation for tuning the synthesizer and converter. Sequence 1 coarse tunes the synthesizer, sequence 2 tunes the converter and sequence 3 fine tunes the synthesizer. During sequence 3 a rest sequence is established which introduces a null detection circuit that compares the output of cathode follower 1A6A1A8V1 (synthesizer main loop error voltage) with a loop error bias level obtained from potentiometer 1A6A1A2A4R2. If the main error voltage increases beyond a predetermined level, null relay 1A6A1A2A4K4 will actuate and restart its sequence of operation. At the same time, a null pulse is applied to NOR gate 1A6A1A3A1A5 in the trigger subassembly which causes FAULT indicator lamp 1A6A1DS2 to begin flashing. This three-slot time sequence of operation, regardless of the channel selected, is the same for all channels.

(a) SEQUENCE 1 DESCRIPTION.- When the radio set is energized and a frequency channel is selected the autotune system in RF assembly 1A8 begins its sequence of operation (refer to paragraph 4-6b(11)(a) through 4-6b(11)(a)(3)). At the end of the first direction of rotation of the autotune system, reverse-interlock switch 1A8S253 sends a start pulse to Schmitt trigger A1A1 in the trigger subassembly. The output of the Schmitt trigger is applied to pin 1 of OR gate A1A6A and pin 9 of OR gate A1A6B. The output from pin 4 of OR gate A1A6A is a reset pulse which resets flip flops A3A1 and A3A2 in the coder subassembly, and flip flop A2A4 in the timer subassembly. The output from pin 7 of OR gate A1A6B is fed through delay multivibrators A2A1 and A2A3 (100 microseconds and 1 millisecond, respectively) to pin 8 of NOR gate A2A7. The delay multivibrators delay the pulse in order to allow sufficient time for flip flops A3A1 and A3A2 in the coder subassembly and flip flop A2A4 in the timer subassembly to reset. NOR gate A2A7 functions as an inverter to obtain a pulse of the correct polarity. The output from pin 7 of NOR gate A2A7 is an advance pulse which is applied to flip flops A3A1, A3A2, and A2A4 to change their state (sequence 1). When flip flops A3A1 and A3A2 in the coder subassembly change state, NAND gate A3A3A receives binary 1 (-12 volts) inputs which provides a binary 0 (0 volts) output that is applied to one input of NAND gate A3A5B. The output of NAND gate A3A5B is inverted by NAND gate A3A5A to produce a binary 0 output which completes the circuit of relay 1A6A1A2A4K5 and 1A6A1A2A4K3 in the synthesizer relay board. When the relays operate, the synthesizer begins to coarse tune during sequence 1.

(b) SEQUENCE 2 DESCRIPTION.- At the same time that the advance pulse advances flip flops A3A1 and A3A2, it also changes the state of flip flop A2A4 in the timer subassembly. The operation of this flip flop is delayed 5 seconds by delay circuit A2A5. The delayed output of flip flop A2A4 is applied to one input of NOR gate A2A6A. The NOR gate also receives binary 1 levels from flip flops A3A1 and A3A2 which open the gate to allow the 5-second delayed pulse to pass through. The output of NOR gate A2A6A is inverted by NOR gate A2A6B and applied to delay multivibrator A2A2 (100-microsecond delay). This delay multivibrator shapes the signal and the output is applied to the input of delay multivibrator A2A3. It then sends an advance pulse (through NOR gate A2A7) to flip flops A3A1, A3A2, and A2A4 to change their state. This time the binary output of A3A1 reverses (sequence 2) thus placing a binary 1 (-12 volts) on pin 8 of NAND gate A3A3B and a binary 0 (0 volts) on pin 1 of NAND gate A3A3A. Because NAND gate A3A3A has a binary 0 and binary 1 input it becomes inhibited and results in a binary 1 output. However NAND gate A3A3B has binary 1's at its input resulting in a binary 0 (0 volts) at its output. The binary 0 output completes the circuit to relays 1A6A1A2A4K1 and 1A6A1A2A4K2 in the synthesizer relay board. The binary 0 is also fed through NAND gates A3A5B and A3A5A to keep relays 1A6A1A2A4K3 and 1A6A1A2A4K5 actuated. When all relays are actuated, the converter begins to tune during sequence 2.

(c) SEQUENCE 3 DESCRIPTION.- The advance pulse which advanced the operation to sequence 2 also produced a delayed (5 seconds) output from flip flop A2A4 as during sequence 1. The delayed output of flip flop A2A4 is again allowed through NOR gates A2A6A and A2A6B to delay multivibrator A2A2. The output of delay multivibrator A2A2 is once again fed through delay multivibrator A2A3 and NOR gate A2A7 to advance flip flops A3A1, A3A2 and A2A4 to their next state (sequence 3). When flip flops A3A1 and A3A2 are in sequence 3 they provide binary 1's at the input of NAND gate A3A4B which results in a binary 0 output. NAND gates A3A3A and A3A3B

both receive inputs of binary 1's and binary 0's and result in an output of binary 1's which deactivate relays 1A6A1A2A4K1, 1A6A1A2A4K2, 1A6A1A2A4K3, and 1A6A1A2A4K5. When these relays deactivate, the synthesizer beings to fine tune. The rest pulse output of NAND gate A3A4B is applied to NOR gate A1A5B in the trigger subassembly. If the synthesizer main loop error bias voltage exceeds a predetermined level, null relay 1A6A1A2A4K4 actuates and applies a binary 0 (0 volt) at pin 9 of NOR gate A1A5B thus enabling the gate. When NOR gate A1A5B is enabled, its output enables NAND gate A3A6 in the timer subassembly, thus allowing the output of free running multivibrator A3A7 to appear at FAULT indicator lamp 1A6A1DS2, causing it to flash on and off. In the event of power failure, capacitor A1C2 in the trigger subassembly discharges through resistor A1R2. When power is restored capacitor A1C2 begins to recharge through resistor A1R2. The charging level of the integrator circuit (A1C2 and A1R2) is applied through NOR gate A1A5A to Schmitt trigger A1A2. The output of the Schmitt trigger is delayed 50 seconds by flip flop A1A3 and delay circuit A1A4 and applied to pins 2 and 8 of the OR gate A1A6. This input initiates the three slot tuning process as though a pulse were received from the autotune system in the RF amplifier assembly. However, the frequency, to which the synthesizer and converter tunes, is the same frequency to which it had been tuned when the power failed. START switch 1A6A1S4 will start the programmer sequence of operation when the transmitter is operated locally. This serves the same function as the pulse from reverse-interlock switch 1A8S253. For testing purposes, NORM-TEST switch 1A6A1A2A4S1 is placed in the TEST position and the START switch is operated to begin the sequence of operation.

(d) OVERALL TEST DATA. — Information which follows will be helpful in determining the performance of the memory control section. Refer to figure 4-81 for the circuit location and figures 5-87, 5-88 and 5-89 for physical location of test points. Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A for additional test data.

(4) SERVO AMPLIFIER, CIRCUIT DESCRIPTION. — The servo amplifier subsection consists of servo amplifier modulator and preamplifier assembly 1A6A1A9A1, servo amplifier driver and null detector assembly 1A6A1A9A2, and servo motors 1A6A1A7B1 and 1A3A1B3. Operation of the servo amplifier subsection is controlled by the analog memory subsection and the digital timing memory (programmer) subsection.

(a) When a new frequency channel is selected and the programmer begins sequence 1, the following occurs: an analog voltage corresponding to synthesizer output frequency (see figure 4-18), from the analog memory subsection, is applied to one input of servo amplifier differential chopper and preamplifier assembly A9A1. Another input to the servo amplifier differential chopper and preamplifier assembly is a voltage level obtained from servo motor driven potentiometer A7R1. The inputs to the servo amplifier differential chopper and preamplifier assembly are applied to differential amplifiers Q1 and Q2 (see figure 5-199). The differential amplifiers also receive a 115-VAC input which has been clipped by differential choppers VR1 and VR2. The output of the differential amplifiers is a square wave, whose phase relation to the differential chopper input is determined by the levels of the analog memory and the servo motor driven potentiometer. Diodes CR1, CR2, CR5 and CR6 are overload protection diodes to protect the transistors. The square wave output of differential amplifiers Q1 and Q2 is amplified by amplifier Q3, emitter follower Q4, and amplifier Q5. The output of Q5 is amplified and inverted by inverter Q6 and Q7 and applied to buffer amplifier A9A2Q2 in the servo amplifier driver and null detector assembly. Amplifier Q5 also applies an output to buffer amplifier A9A2Q1 in the servo amplifier driver and null detector assembly. The output of servo amplifier differential chopper and preamplifier assembly A9A1 is two square wave signals 180 degrees out of phase. Resistors R15 through R19 and capacitor C4 furnish an AC-DC feedback voltage which stabilizes the operation of amplifier Q3. Resistors R20 through R23 and diodes CR11 and CR12 provide a negative overload feedback voltage which is applied to the junction of overload protection diodes CR7 and CR8 and resistor R4. Buffer amplifiers Q1 and Q2 in servo amplifier driver and null detector assembly A9A2 (see figure 5-200) amplify the square wave input signals. The output of Q1 and Q2 is converted to a sawtooth voltage by delay (integrator) circuits R9 and C3, and R10 and C4, respectively. The sawtooth voltage is synchronized to a pulse derived from a 115-VAC sync voltage. The sync voltage is amplified by inverter amplifier Q6 and converted to trigger pulses by trigger Q7. The output of Q7 operates switch Q8 which provides pulses that prevent starting of the sawtooth signal until the sync signal is present. The sawtooth signal, which is synchronized to the output of switch Q8, triggers SCR trigger Q3 and Q4. The outputs of Q3 and Q4 are sharp pulses that trigger silicon-controlled rectifiers A2A4Q1 and A2A4Q2 (see figure 4-18). The silicon-controlled rectifiers are triggered to allow an unregulated 28 VDC to be applied to the control winding of servo motor A7B1. The phase relation of the trigger pulses compared to the 115-VAC applied to the reference winding of the servo motor determines the direction of rotation. Because the servo motor is mechanically coupled to potentiometer A7R1 and

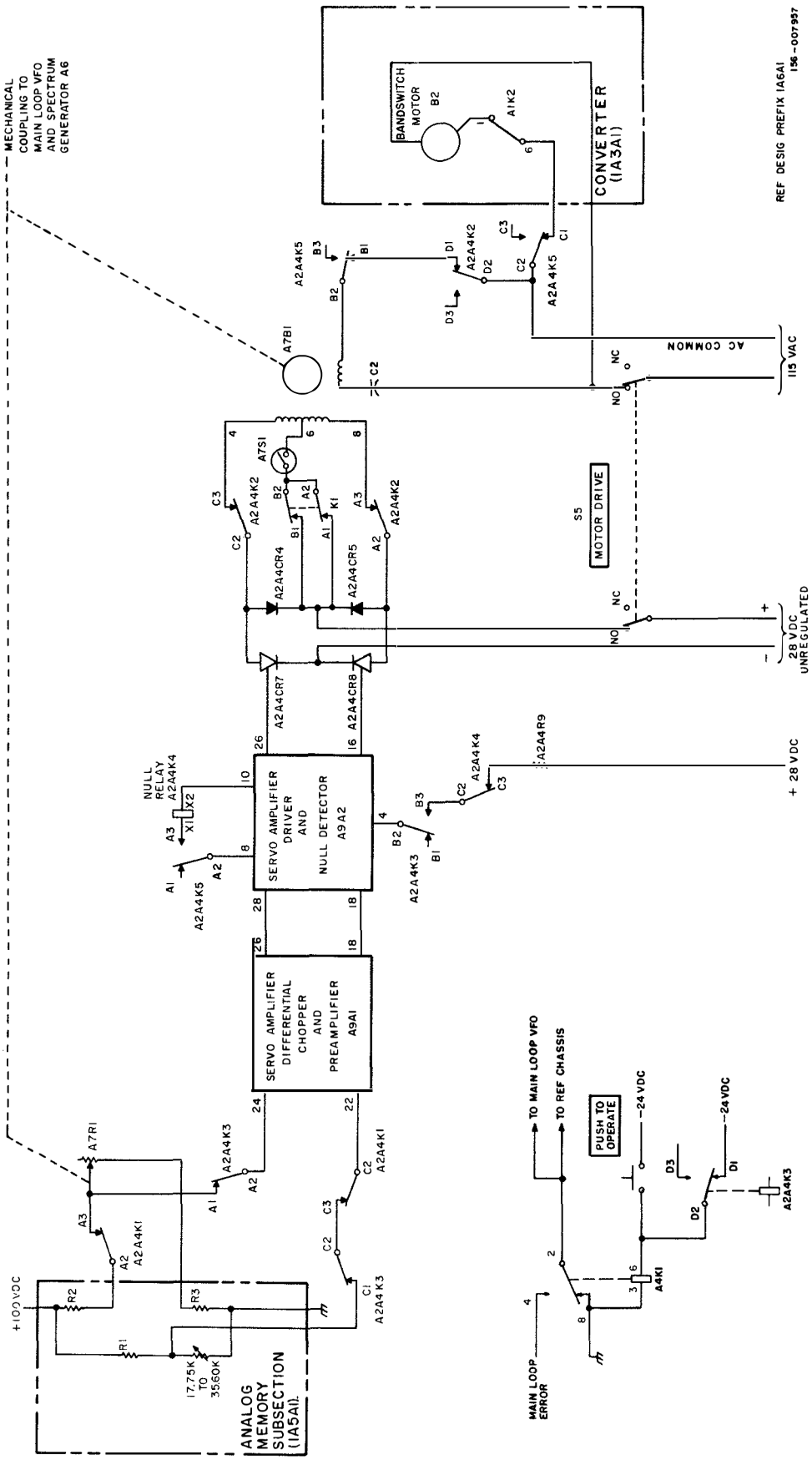


Figure 4-18. Synthesizer 1A6, Synthesizer Coarse Tune, Simplified Schematic Diagram

the VFO and spectrum generator gang (1A6A1A6), which tunes the main loop to the operating frequency, it will stop its rotation when the output level of the potentiometer is equal to the analog level from the analog memory subsection. When the servo motor stops rotation, the synthesizer is coarse tuned.

(b) During sequence 2 of operation (see figure 4-19), the output of servo driven potentiometer A7R1 is compared to the output voltage of a servo potentiometer in the converter unit. The unequal voltage at the input of servo amplifier differential chopper and preamplifier assembly 1A6A1A9A1 causes servo motor 1A3A1B1 in the converter to rotate. At the end of the second sequence, the synthesizer is coarse tuned and the exciter is tuned.

(c) During sequence 3 (see figure 4-20), a loop error bias voltage is compared to the synthesizer main loop error voltage. Any difference in voltage levels causes the servo motor in the synthesizer to rotate and fine tune the synthesizer. At the same time, deactivation of relay A2A4K5 places relay A2A4K4 in the null detection circuit (see figure 5-193). When the synthesizer loop error voltage exceeds a predetermined level which is sensed by diode CR1 or CR2, null detectors Q9 and Q5 actuate null relay A2A4K4 which causes FAULT indicator lamp 1A6A1DS2 to flash, indicating that the synthesizer output frequency is incorrect.

(d) OVERALL TEST DATA. — Information which follows will be helpful in determining the performance of the servo amplifiers. Refer to figures 5-199 and 5-200 for circuit location and figures 5-105 and 5-106 for physical location of test points.

4-4. AMPLIFIER, AUDIO FREQUENCY, AM-4246/FRT-24A(1A2), FUNCTIONAL DESCRIPTION.

a. OVERALL FUNCTIONAL DESCRIPTION (see figure 4-21). — The amplifier consists of an audio amplifier functional section and a phase detector functional section. The audio amplifier functional section determines the mode of emission, selects the sideband (either upper or lower), and provides an audio level to converter 1A3. The phase detector functional section contains a high stability 1-MC frequency standard which supplies converter 1A3 and synthesizer 1A6 with a 1-MC reference frequency. This functional section is also capable of comparing the internal frequency standard with an external 1-MC or 5-MC reference signal having a stability equal to or greater than the frequency standard. Phase or frequency error between the compared signals is indicated on a front-panel meter. The amplifier receives audio or keying inputs from keyer unit 6 and transmitter control units 2 or 3. A front-panel microphone input is also provided. Sideband selection is accomplished automatically by application of control signals from the dial control 1A1 or manually by the manipulation of front-panel selector switches. The amplifier can provide amplified outputs which are sideband selected and filtered to achieve an audio channel with a 300-cycle to 3400-cycle bandpass, or it can provide direct outputs without filtering or amplification.

b. OVERALL TEST DATA. — Information follows which will aid in determining the overall performance of the amplifier. Refer to figure 4-71 for the circuit location and figures 5-36 and 5-37 for the physical location of test points. The test equipment required is an electronic counter, a VTVM, and, an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(1) AC power input (1A2A1J1) 20 : 115 VAC. If not present, refer to paragraph 4-11.

(2) AC power input (1A2A1J2) 18 : 230 VAC. If not present, refer to figure 5-164.

(3) RF output (1A2A1J4) 16 : 1 MC at 1 VRMS min. to 1.5 VRMS max. into 50 ohms.

(4) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

c. AUDIO AMPLIFIER, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. — The audio amplifier functional section (see figure 4-22) consists of two sets of high-pass filters, low-pass filters, AGC and audio amplifiers, audio frequency attenuators, and audio voltmeters. One set is for the upper sideband audio channel and the other set is for the lower sideband audio channel. The audio amplifier functional section also contains a CW gating circuit whichreceives keying signals from remote transmitter control units 2 and 3 and provides a CW gate output to converter 1A3. The two sideband audio channels receive audio information from a line input from the remote transmitter control units or from a front-panel microphone. Since the upper and lower sideband audio channels are identical, only the upper sideband audio channel will be described (see figure 4-71). Audio information (speech or FSK) on a balanced 600-ohm phone-line is applied through balun transformer T1 to LINE LEVEL attenautor A11. The balun transformer converts the balanced input to a single-ended output and also reduces noise

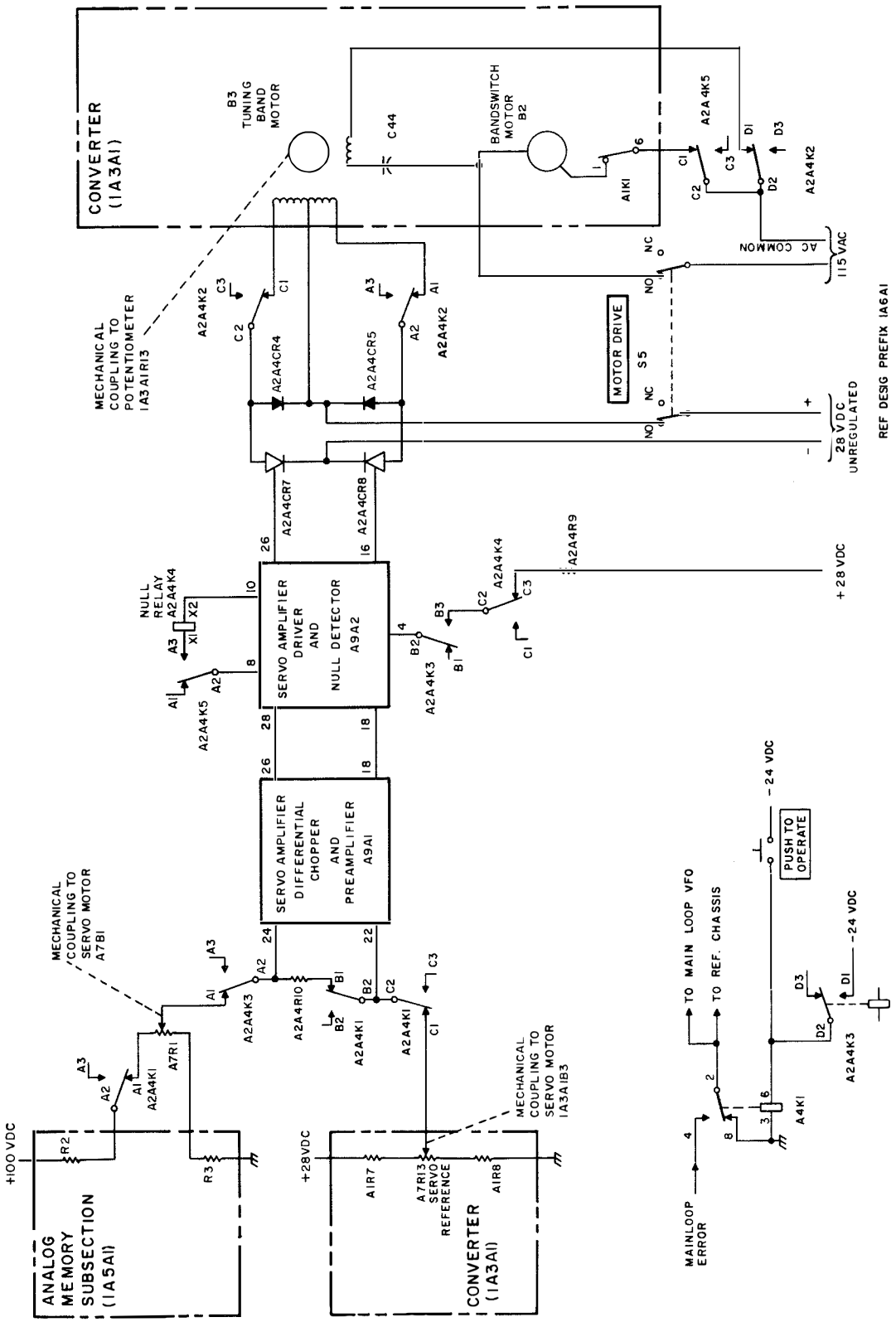


Figure 4-19. Synthesizer 1A6, Converter Bridge Tune, Simplified Schematic Diagram

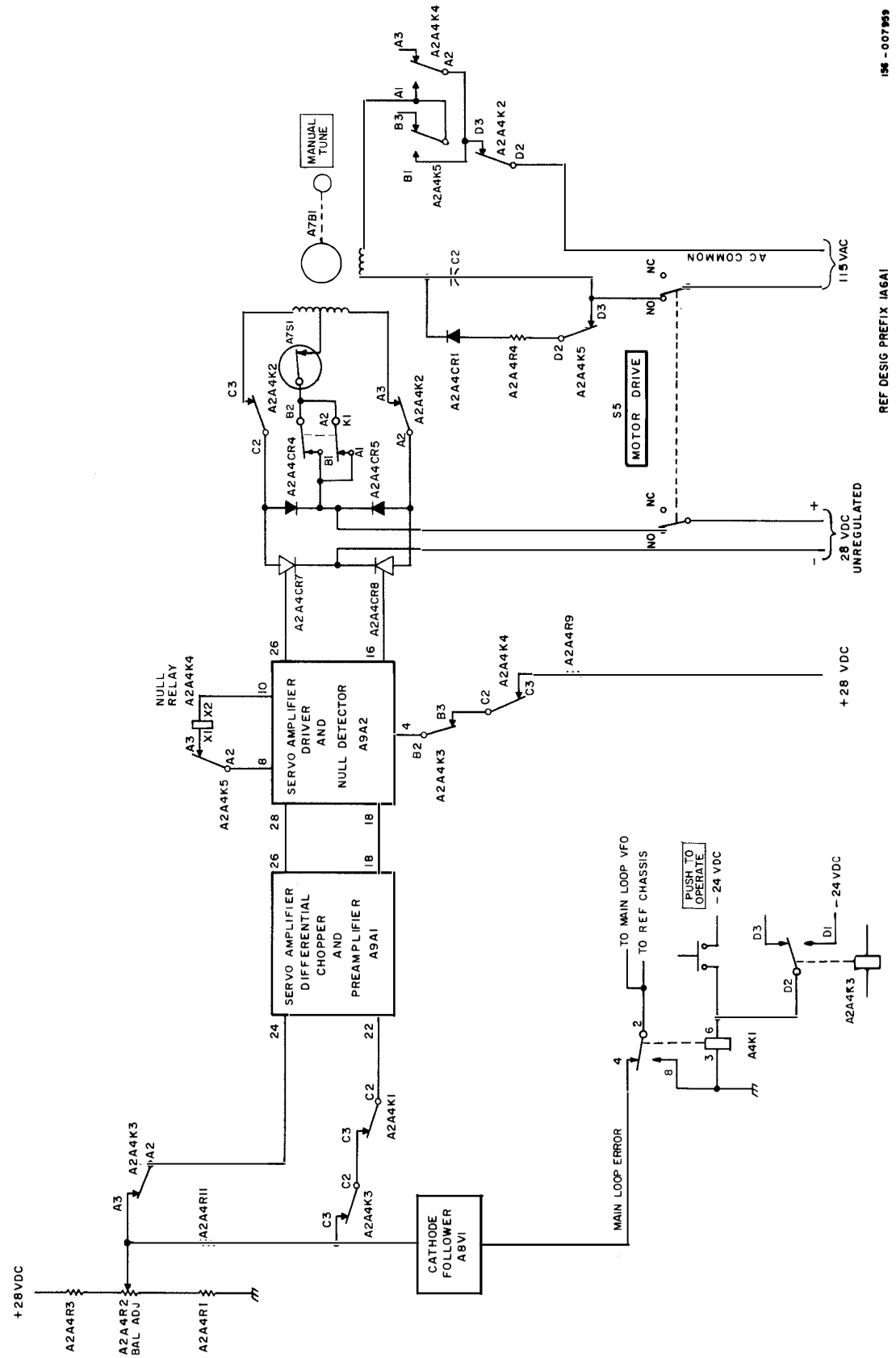


Figure 4-20. Synthesizer 1A6, Synthesizer Fine Tune, Simplified Schematic Diagram

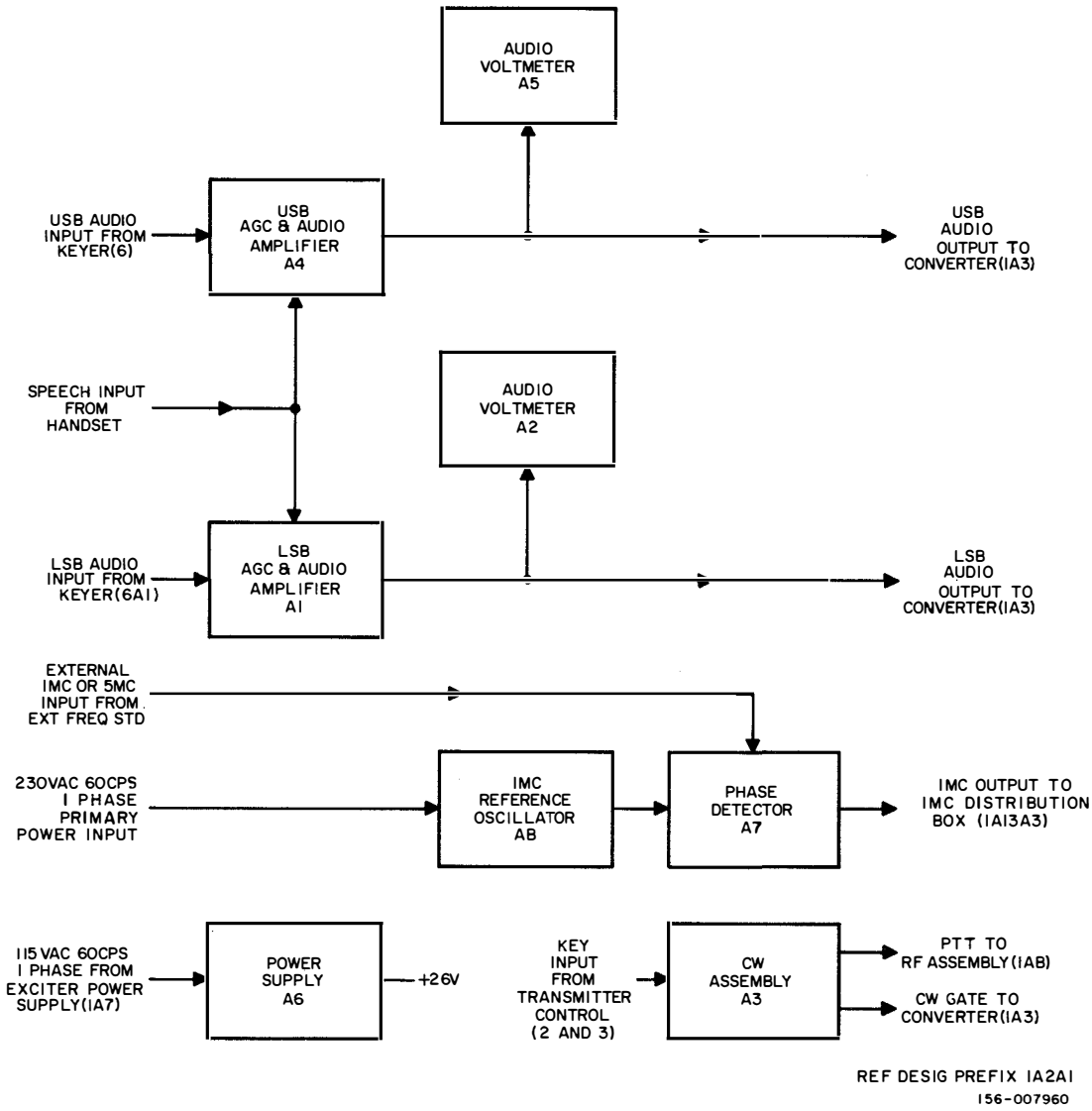


Figure 4-21. Amplifier 1A2, Overall Functional Block Diagram

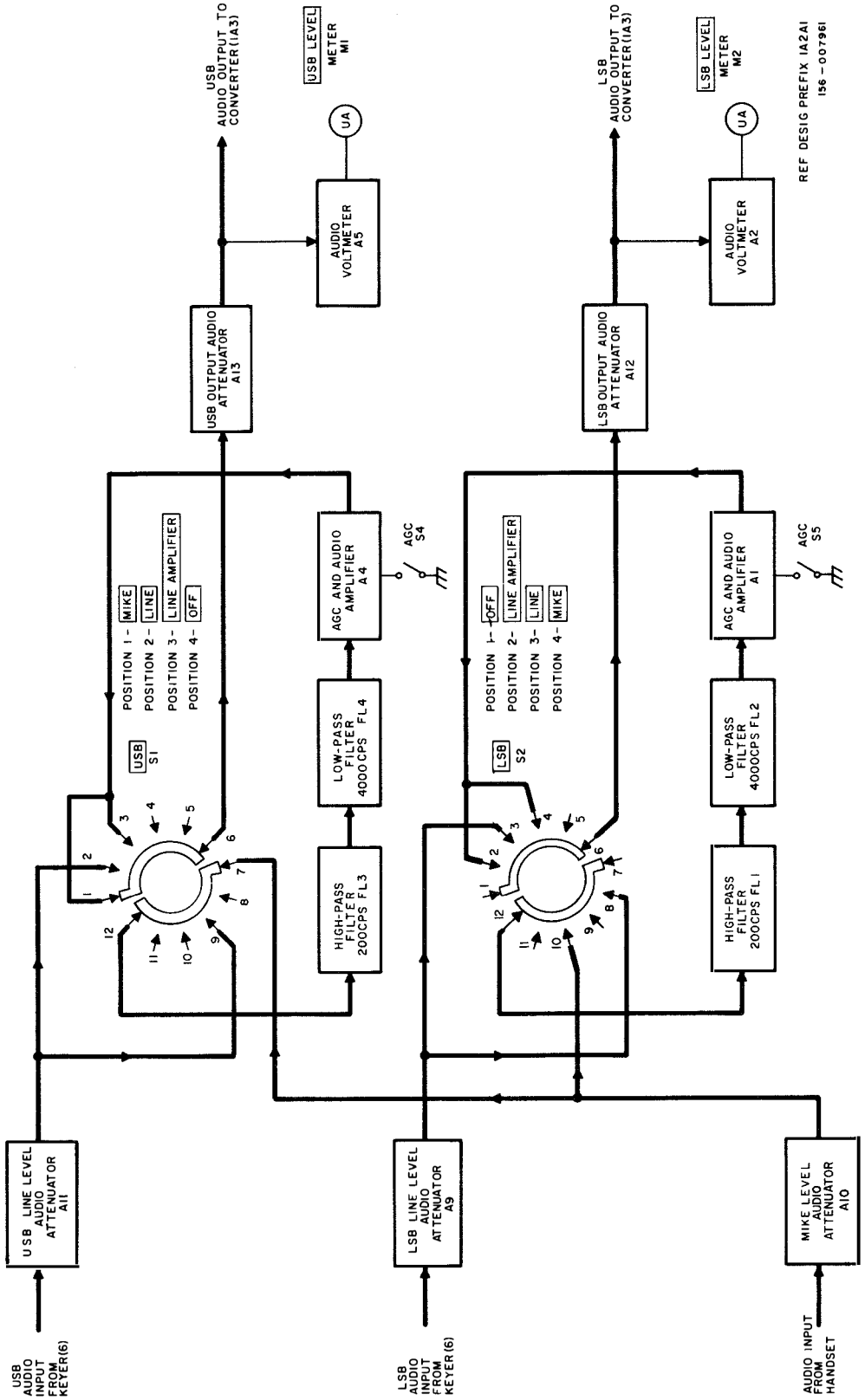


Figure 4-22. Amplifier 1A2, Audio Section Block Diagram

signals picked up by the phone line. The line level attenuator adjusts the level of the input signal to obtain the desired level for modulation in converter 1A3. When USB switch S1 is in the LINE position, the input signal is passed through the audio amplifier functional section unaltered, other than proper level adjustment. Audio voltmeter A5 monitors the output audio level and provides a signal level indication on USB LEVEL meter M1. When USB switch S1 is in the LINE AMPL position, the audio input signal is fed through high-pass filter FL3 and low-pass filter FL4 to AGC and audio amplifier A4. These filters provide a bandpass of 200 cycles to 4000 cycles. The audio signal is amplified by AGC and audio amplifier A4 (AGC action is selected by a front panel switch) and fed through USB switch S1 and audio attenuator A13 to converter 1A3. During operating modes A3b (two independent sidebands) and A3j (single sideband suppressed carrier, selectable upper and lower sideband), both the upper and lower sideband AGC and audio amplifiers are operative and the amplifier provides a two-channel output. However, operating in the A3a mode of emission, a ground signal completes the circuit to relay K2. Operation of K2 removes B+ from AGC and audio amplifier A1 and provides transmission on the upper sideband only. It also supplies operating voltage to relay K6 which applies a ground to the lower sideband channel. Operation of the relay also lights A3a indicator lamp DS2. When the radio set is in the A1 (continuous wave) operating mode of emission, a ground signal completes the circuit to relays K1 and K4. Operation of K1 applies B+ to CW gating circuit A3. It also lights A1 indicator lamp DS1. Keying information from transmitter control units 2 or 3 actuates relay K5 at the keying rate and causes ground pulses to be fed through closed contacts of K4 to the input of A3. The CW gating circuit energizes relay K3 which, in turn unbiases the driver in RF assembly 1A8. The keying circuit also provides a CW gating signal to the IF amplifier in converter 1A3. Approximately 3 seconds after completion of transmission, relay K3 de-energizes and biases the driver in RF assembly 1A8.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. - Information follows which will aid in determining the overall performance of the audio amplifier functional section. Refer to figure 4-71 for the circuit location and figures 5-36 and 5-37 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Set USB selector switch to each of its four positions and check USB LEVEL meter readings against typical readings given in table 3-13. (Audio must be applied to upper sideband input.)

(b) Set LSB selector switch to each of its four positions and check LSB LEVEL meter readings against typical readings given in table 3-13. (Audio must be applied to lower sideband input.)

(c) B+ (1A2A1J6-6). +26 VDC.

(d) Refer to paragraph 5-4 for general information and paragraph 5-4d for specific adjustment procedures of audio attenuator.

(3) AGC AND AUDIO AMPLIFIERS 1A2A1A1 and 1A2A1A4, CIRCUIT DESCRIPTION. AGC and audio amplifiers A1 and A4 are identical; therefore, only A1 will be described (see figure 4-71). When LSB selector switch S2 is in the LINE AMPL or MIKE position, AGC and audio amplifier A1 receives an audio signal with a bandpass of 300 to 3400 cycles from filter 1A2A1FL2. The input signal is amplified and applied to attenuator A12 for eventual application to converter 1A3. The signal is also rectified to produce an AGC bias level proportional to the input signal strength. The output signal is also applied to audio voltmeter A2 for monitoring on LSB LEVEL meter M2. The input signal is applied to the base of audio amplifier Q1 (see figure 4-23). To compensate for gain-versus-temperature variations of Q1, thermistor R25 is connected between the base and ground. Thermistor R25 is a temperature sensitive semiconductor with a high negative temperature coefficient of resistance. When the temperature of the thermistor increases, its resistance decreases and when its temperature decreases, its resistance increases. This characteristic of the thermistor maintains a constant gain-versus-temperature parameter of Q1. Capacitor C2 across the collector load resistor of Q1 is a high-frequency noise suppressor that shunts noise signals to ground. Capacitor C10 across the collector-base circuit of amplifier Q2 is also a noise suppressor. The output of Q1 is amplified by audio amplifiers Q2 through Q4 and applied to AGC amplifier Q5 and output emitter-follower Q6. AGC amplifier Q5 (see figure 4-24) provides voltage gain and isolates the audio amplifiers from the non-linear load characteristics of AGC rectifiers CR1 and CR2, connected as a voltage doubler. AGC rectifiers CR1 and CR2 detect changes in the average input signal strength and produce a proportional DC potential that biases the audio amplifiers to counteract any change. During zero-signal conditions, capacitor C22 charges to a reference level of +0.8 VDC established by resistors R13 and R22 and sensistor R23.

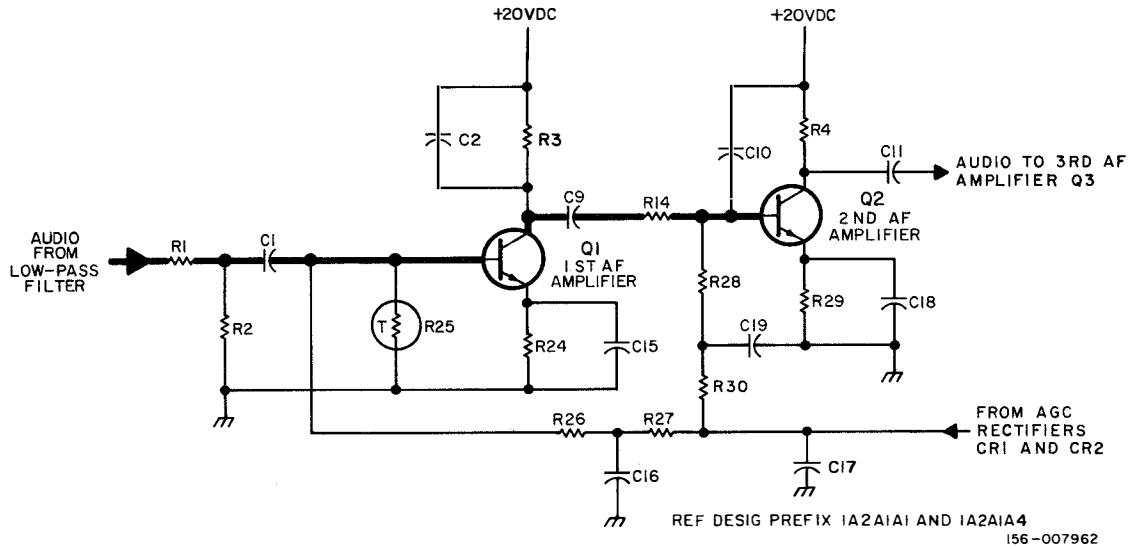


Figure 4-23. Amplifier 1A2, Audio Amplifier, Simplified Schematic Diagram

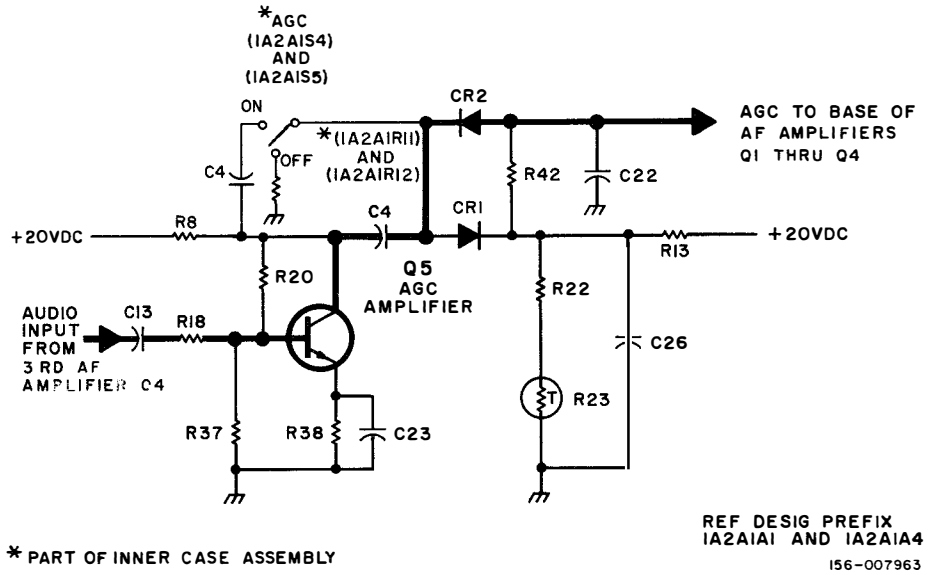


Figure 4-24. Amplifier 1A2, AGC Amplifier, Simplified Schematic Diagram

Sensistor R23 is a temperature-sensing and temperature-compensating silicon resistor that maintains the AGC line at a relatively constant reference level over the entire ambient temperature range of the AGC audio amplifiers. When the temperature of the sensistor increases, its resistance increases and when its temperature decreases, its resistance decreases. A positive going input signal to the AGC rectifier charges capacitor C4 to the level of the input. A negative going input signal charges capacitor C22 to the combined level of the input and the charge across capacitor C4. The larger the input signal to the AGC audio amplifier, the larger the AGC voltage and the lower the overall gain. Emitter-follower Q6 (see figure 5-110) provides the main output of the AGC audio amplifier. A sample of the output of the emitter-follower is amplified by sidetone amplifier Q7. Sidetone amplifier Q7 is a transformer-coupled, common-emitter amplifier that provides voltage and current gain and permits operation of a 600-ohm headset at a peak level of 8 milliwatts.

(4) AGC AND AUDIO AMPLIFIERS 1A2A1A1 AND 1A2A1A4, TEST DATA. - Information follows which will be helpful in determining the overall operation of the AGC and audio amplifiers A1 and A4. Refer to figure 4-71 for the circuit location and figures 5-37 and 5-38 for the physical location of test points. The test equipment required is a VTVM, and an audio oscillator (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Audio output with 11-MVRMS input and applicable LINE LEVEL control at maximum. (1A2A1A1-4 or 1A2A1A4-4) (R):and (U): 50 MVRMS. If correct, AGC and audio amplifier is operating properly.

(b) B+ (1A2A1A1-12 or 1A2A1-A4-12): +22 VDC.

(c) Refer to figure 5-170 for transistor voltage measurements.

(5) AUDIO VOLTMETER 1A2A1A2 AND 1A2A1A5, CIRCUIT DESCRIPTION. - Audio voltmeters A2 and A5 are identical; therefore, only A2 will be described (see figure 4-25). Audio voltmeter A2 consists of a class A amplifier and a bridge rectifier circuit. It receives an audio input signal from attenuator A12 and supplies a DC output level to LSB LEVEL meter M2. The input signal (0 to 0.10 VRMS) is applied to the base of common emitter amplifier Q1. The output of Q1 is rectified by bridge rectifier CR1 through CR4 to produce a DC level proportional to the input signal. The output of the bridge rectifier is applied to the meter. Full scale meter deflection is attained when the input level of the amplifier is 0.10 VRMS and mid scale (red line) deflection is attained when the input level is 50 MVRMS. Capacitor C4 and resistor R6 provide degenerative feedback for improved stability and reduced distortion.

(6) AUDIO VOLTMETER 1A2A1A2 AND 1A2A1A5, TEST DATA. - Information follows which will be helpful in determining the overall operation of the audio voltmeters A2 and A5. Refer to figure 4-71 for circuit location and figures 5-37 and 5-39 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) DC output with 50 MVRMS input (1A2A1A2-4-12 or 1A2A1A5-4-12) (Q):and (T): 0.06 VDC. If correct, audio voltmeter is operating properly.

(b) Audio input with applicable sideband selector switch in LINE position. (1A-2A1A2-16 or 1A2A1A5-16): 50 MVRMS with 300-MVRMS audio input.

(c) B+ (1A2A1A2-14 or 1A2A-1A5-14): +26 VDC.

(d) Refer to figure 5-171 for transistor voltage measurements.

(7) CW ASSEMBLY 1A2A1A3, CIRCUIT DESCRIPTION. - When the transmitter is set for CW operation, relay 1A2A1K1 energizes applying +26 VDC to the CW assembly (see figures 5-168 and 5-172). This causes transistor Q2 to conduct and Q1 to cut off. Conduction of transistor Q2 supplies a ground gate to converter 1A3 which enables the equipment for carrier on-off CW operation. When the key is closed, the positive potential on the base of Q1 is removed and the transistor conducts. Conduction of Q1 activates relay K3 which removes a grid blocking voltage to RF assembly 1A8. At the end of

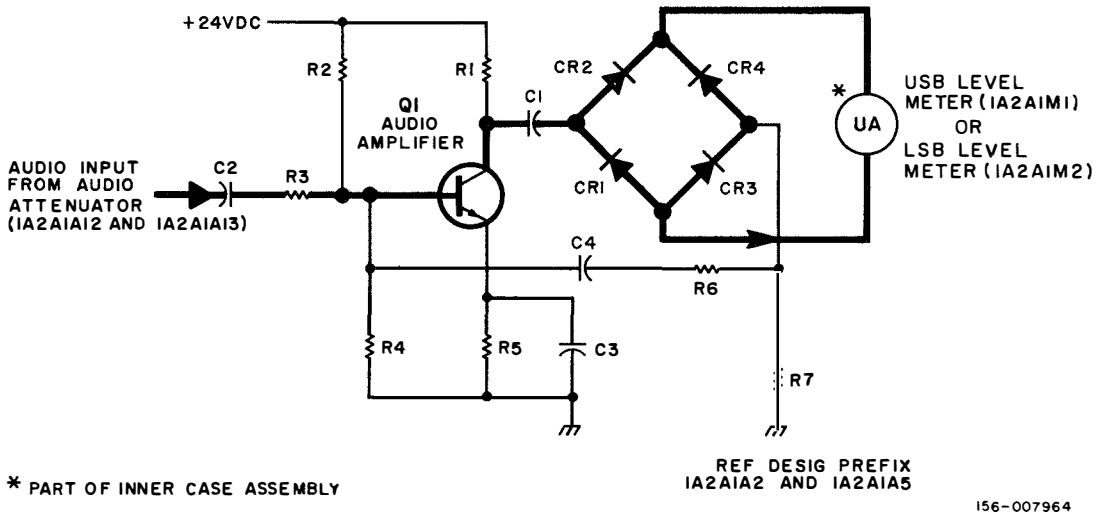


Figure 4-25. Amplifier 1A2, Audio Voltmeter, Simplified Schematic Diagram

keying (3 seconds), relay K3 deactivates and returns the grid blocking voltage to the RF assembly.

(8) CW ASSEMBLY 1A2A1A3, TEST DATA. - Information follows which will be helpful in determining the overall operation of the CW assembly A3. Refer to figure 4-71 for the circuit location and figure 5-40 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

Refer to figure 5-172 for transistor voltage measurements.

d. PHASE DETECTOR SECTION, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. - The phase detector functional section (see figure 4-26) consists of a 1-MC oscillator with a fine frequency adjustment circuit, a phase detector assembly, and a regulated power supply. It supplies a stable 1-MC reference signal to converter 1A3 and synthesizer 1A6. It also receives an external 1-MC or 5-MC reference signal of known high stability to determine the stability of the internally generated signal. If desired, the external signal can be supplied to the synthesizer instead of the internal signal. The internal 1-MC signal is generated by 1-MC oscillator and oven A8 (see figure 4-71). The 1-MC output of the oscillator is applied to phase detector driver A7V3 and amplifier A7V5. If REF SEL switch S3 is in the INT REF EXT PH DET or INT REF ONLY position, the internal 1-MC signal is applied to the synthesizer. In the INT REF EXT PH DET, EXT REF only, and EXT REF INT PH DET positions the external reference signal is amplified and applied to 1-MC oscillator A7A2. The output of A7A2 is a phase locked 1-MC signal. The 1-MC signal is applied to phase splitter A7V2 and amplifier A7V4. If REF SEL switch S3 is in the EXT REF ONLY or EXT REF INT PH DET position, the external 1-MC signal phase locked to the external reference is applied to the synthesizer. If REF SEL switch S3 is in the INT REF EXT PH DET position, the internal 1-MC signal output of phase detector driver A7V3 and the external 1-MC signal output of phase detector driver A7V2 are applied to

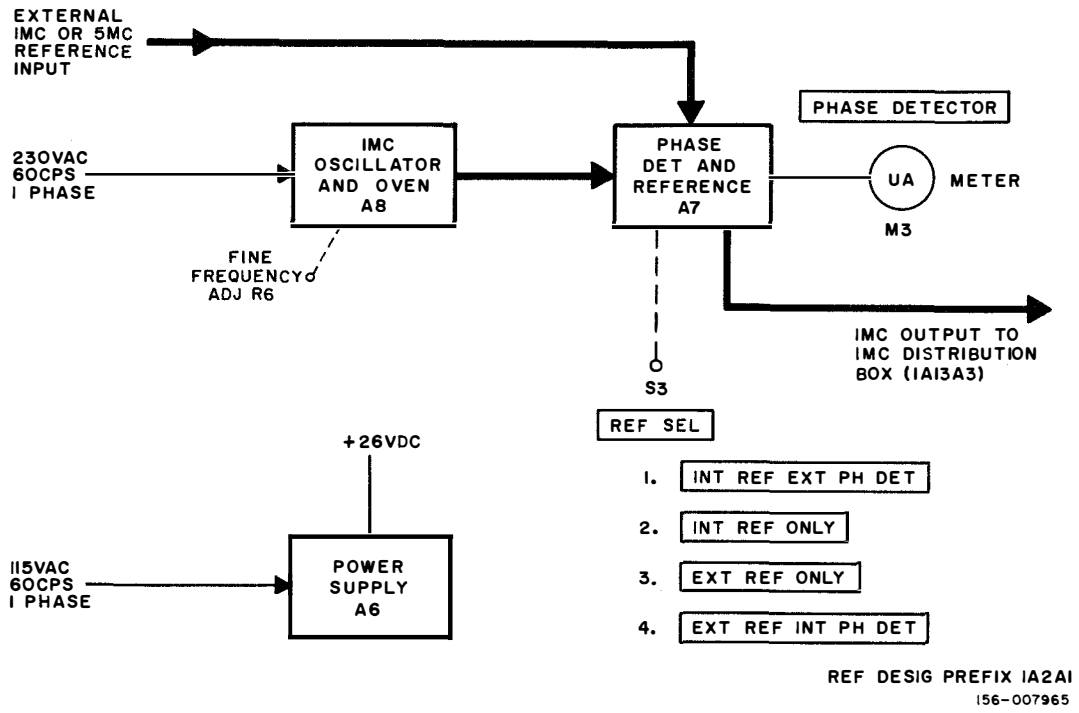


Figure 4-26. Amplifier 1A2, Phase Detector Section, Block Diagram

phase detector A7A3. The phase detector compares the frequency and phase of two signals. If a phase or frequency difference exists, a corresponding error voltage is produced and applied to PHASE MONITOR meter M3 for monitoring. Power supply and regulator A6 receives 115-VAC, 60-cycle primary AC power. The primary AC power is rectified and regulated to produce +26 VDC which is distributed to the audio amplifier.

(2) PHASE DETECTOR SECTION FUNCTIONAL SECTION, TEST DATA. - Information follows which will be helpful in determining the overall operation of the phase detector section. Refer to figure 4-71 for the circuit location and figures 5-36, 5-37, and 5-51 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output with REF SEL switch S3 in INT REF ONLY position (1A2A1-J4) (16) : 1-MC at 1.3 VRMS minimum.

(b) Power input (1A2A1J2) (18) : 230 VAC.

(c) Power input (1A2A1J1) (20) : 115 VAC.

(d) Check front panel PHASE DETECTOR meter readings for each position of REF SEL switch. Refer to table 3-13 for typical meter readings.

(e) Refer to paragraph 3-6b(2) for adjustment of 1A2A1R6.

(3) 1-MC OSCILLATOR AND CRYSTAL OVEN 1A2A1A8, CIRCUIT DESCRIPTION. The 1-MC oscillator (see figure 4-27) consists of a high-gain amplifier and an RF Wheatstone bridge in which resistor R1 is factory selected to give an oscillator output of 1.5 VRMS. The application of B+ and filament power produces noise transients which are fed back through transformer T2 to the bridge network. The bridge is initially unbalanced; the small plate signal is coupled through transformer T1 to the grid of V1 to initiate oscillations at a frequency determined by crystal A1Y1. As the oscillations build up, the current through RT1 increases, thereby raising the temperature and resistance of RT1 and balancing the bridge. When the bridge is balanced, there are two

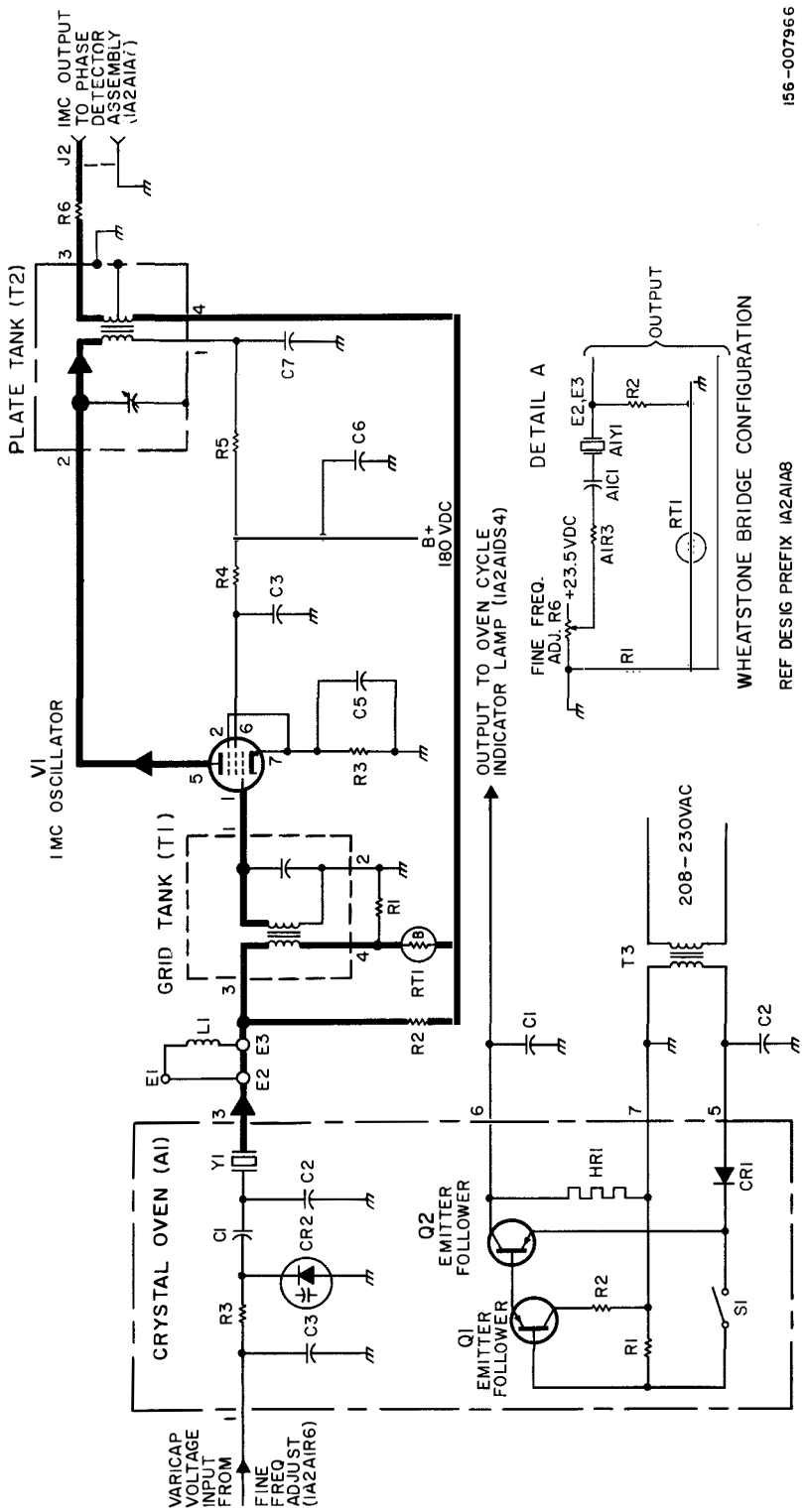


Figure 4-27. Amplifier 1A2, 1 MC Oscillator and Crystal Oven, Simplified Schematic Diagram

major circuit characteristics: The crystal arm consisting of A1Y1, A1C1, A1C2, and reactance control diode A1CR2 appears resistive in series resonance; the attenuation in the bridge equals the tube gain less circuit losses. If the tube gain decreases (due to a drop in B+ or filament voltage), feedback to the bridge is reduced. This results in a decreased current and resistance in RT1 which unbalances the bridge and causes the input drive to V1 to increase. The action of RT1 is similar to an automatic gain control (AGC) network and the output of the oscillator is kept constant. If the oscillator components external to the bridge network change value, the oscillator compensates for it by a shift in frequency; however, because of the bridge feedback, the change in frequency required for the compensation is a minimum. Reactance control diode A1CR2 in conjunction with FINE FREQ ADJ control 1A2A1R6 fine tunes the oscillator frequency. When the oscillator frequency can no longer be compensated for by adjusting FINE FREQ ADJ, a jumper is removed between E2 and E3 to regain control. The oven maintains the crystal at a constant temperature of 75°C, isolating it from ambient temperature variations. Transformer T3 is supplied 220 VAC from the primary power and is not controlled by the primary circuit breaker; T3 has its own fusing circuit. The AC input from T3 is rectified by diode A1CR1 and fed to switching transistors A1Q1 and A1Q2. The transistors are biased so that only 1 MA flows through A1Q1, while 250 MA flows through A1Q2 and through heater A1HR1. When 75°C is reached, mercury switch A1S1 closes and cuts off A1Q1 and A1Q2. The low current through A1Q1 results in a low current through the switch, thereby providing maximum reliability of switch operation. Oven indicator lamp 1A2A1DS4 in parallel with the heater, indicates when the oven is "on" or quiescent. The normal cycling time of the oven is approximately 8 to 10 seconds "on", and 15 to 20 seconds "off". Mercury switch A1S1 is similar to a thermometer and consists of a reservoir of mercury in a bulb and a fine capillary tube. Two fine wires are placed in the capillary tube, one at the 75°C position and the other always in contact with the mercury. When the mercury rises, it shorts the two wires and thereby closes the switch, in turn stopping the heating process.

(4) 1-MC OSCILLATOR AND CRYSTAL OVEN 1A2A1A8, TEST DATA. — Information follows which will be helpful in determining the overall operation of 1-MC oscillator and crystal oven assembly A8. Refer to figure 4-71 for the circuit location and figures 5-47 through 5-49 and 5-51 for the physical location of test points. The test equipment required is an electronic counter, a VTVM, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A2A1A8J2) (O): 1-MC at 1.5 VRMS nominal, with phase detector A7, connected. If correct, 1-MC oscillator is operating properly.

(b) Oven heater input voltage (1A2A1A8J1-7-8) (18): 208/230 VAC.

(c) Filament input voltage (1A2-A1A8J1-2): 6.3 VAC.

(d) Refer to figure 5-175 for voltage and resistance measurements.

(e) Refer to paragraphs 3-6b(2) and 5-4c for adjustment of 1A2A1R6 and 1A2A1-A8T2.

(5) PHASE DETECTOR AND REFERENCE 1A2A1A7, CIRCUIT DESCRIPTION. — Phase detector and reference assembly A7 (see figures 4-71 and 5-174) receives the 1-MC signal from an internal 1-MC oscillator and oven 1A2-A1A8 and an externally supplied 1-MC or 5-MC reference signal. The internal signal can be amplified and applied to the output, or the externally supplied signal can be amplified and applied to the output. The two signals can also be compared in a phase detector and any frequency and/or phase difference is indicated by PHASE DETECTOR meter 1A2A1M3. The 1-MC signal from 1-MC oscillator and oven 1A2A1A8 is applied to the grid of amplifier V5 and phase detector driver V3. When REF SEL switch 1A2A1S3 is in the INT REF EXT PH DET or INT REF ONLY position, amplifier V5 is operated when a ground is applied to its cathode. The 1-MC output of amplifier V5 is applied to distribution box located on the patch panel, which in turn supplies 1-MC to the synthesizer 1A6, converter 1A3 and 1-MC output jack. The primary winding of transformer T4 and capacitor C29 on the plate of V5 form a parallel resonant circuit (tank circuit) tuned to 1 MC. When REF SEL switch 1A2A1S3 is in the INT REF EXT PH DET or EXT REF INT PH DET position, B+ is applied to phase detector driver V3 and its output is applied to phase detector A3. The external 1-MC or 5-MC reference signal is coupled through a double tuned circuit consisting of T1, C1 and T2, C2 to the grid of amplifier V1. The plate circuit of V1 is double tuned by tank circuits L1, C8 and L2, C9 and R4. The output of V1 is applied to the base of emitter-follower A1Q1. If the input to amplifier V1 is 0.25 VRMS or greater, A1Q1 and squelch switch A1Q2 conduct and the output of A1Q1 is applied to 1-MC oscil-

lator A2Q1. The oscillator is tuned to "free-run" at a frequency of approximately 1 MC. The 1-MC or 5-MC input from emitter-follower A1Q1 synchronizes (phase locks) the oscillator; therefore, the output of A2Q1 is a 1-MC signal with a stability equal to that of the 1-MC or 5-MC external reference signal. Positive feedback for the oscillator is from collector to emitter and the base bias is set by resistors A2R1 and A2R2. Inductor A2L1 tunes the collector circuit of the oscillator. If the input to amplifier V1 is less that 0.25 VRMS, squelch switch A1Q2 cuts off. This results in an increased positive potential at the collector of A1Q2 which cuts off emitter-follower A1Q1 and 1-MC oscillator A2Q1. The output of the 1-MC oscillator is applied to phase splitter V2 and amplifier V4. When REF SEL switch A1S3 is in the EXT REF ONLY OR EXT REF INT PH DET position, a ground is applied to operate amplifier V4. The 1-MC output of amplifier V4 is applied to distribution box on patch panel and then to the synthesizer. The primary winding of transformer T3 and capacitor C19 on the plate of V4 forms a parallel resonant circuit tuned to 1-MC. When REF SEL switch 1A2A1S3 is in the INT REF EXT PH DET or EXT REF INT PH DET position, B+ is applied to phase detector driver V3 and its output is applied to phase detector A3. The phase detector is a quadrature detector which senses any frequency or phase difference between the internal and external signals. The output of the phase detector is applied to PHASE DETECTOR meter 1A2A1M3. If the two frequencies are the same and in phase, the output of the phase detector is zero. If the frequencies are the same but out of phase, the output of the phase detector is a DC signal with an amplitude and polarity proportional to the amount and direction of the phase difference. If both frequency and phase difference exists, the output of the phase detector is a clamped potential; the AC component is proportional to the amount and direction of the phase difference. The PHASE DETECTOR meter indicates the amount of frequency and phase difference by cycling of the meter pointer.

(6) PHASE DETECTOR AND REFERENCE 1A2A1A7, TEST DATA. — Information follows which will be helpful in determining the overall operation of phase detector and reference assembly A7. Refer to figure 4-71 for the circuit location and figures 5-42 through 5-46, 5-48, and 5-51 for the physical location of test points. The test equipment required is an electronic counter, a VTVM, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) RF output (1A2A1A7J4) (16): 1-MC at 1.5 VRMS nominal into normal circuit load. If correct, phase detector assembly is operating properly.

(b) External RF input (1A2A1A7J2) (19): 1 MC at 1 VRMS minimum or 5 MC at 1 VRMS minimum.

(c) Internal RF input (1A2A1A7J3) (O): 1 MC at 1.5 VRMS nominal. If frequency is unstable or incorrect, refer to paragraph 4-4d(3).

(d) Filament input voltage (1A2-A1A7J1-3): 6.3 VAC.

(e) B+ (1A2A1A7J1-1): 180 VDC.

(f) B+ with REF SEL switch 1A2-A1S3 in EXT REF ONLY position (1A2A1A7J1-4): 180 VDC.

(g) B+ with REF SEL switch 1A2-A1S3 in INT REF EXT PH DET and EXT REF INT PH DET position (1A2A1A7J1-5): 180 VDC.

(h) B+ (1A2A1A7J1-9): 26 VDC.

(i) RF output of amplifier V1 with REF SEL switch 1A2A1S3 in EXT REF ONLY position (1A2A1A7XA1-2) (N): 1 MC at 8 VRMS nominal. If correct, amplifier V1 is operating properly.

(j) RF output of squelch and emitter follower assembly A1 (1A2A1A7XA1-8) (M): 1-MC at 4.4 VRMS minimum. If correct, squelch and emitter follower A1 is operating properly.

(k) RF output of 1-MC oscillator assembly A2 (1A2A1A7XA2-8) (L): 1 MC at 0.9 VRMS nominal. If correct, 1-MC oscillator A2 is operating properly.

(l) Check front panel PHASE DETECTOR meter reading with REF SEL switch 1A2A1S3 in each of its four positions. Refer to table 3-13 for typical monitor meter readings.

(m) Refer to paragraph 5-4 for general information and to paragraph 5-4b for specific alignment procedures of 1A2A1A7T1 through 1A2A1A7T4, 1A2A1A7L1, 1A2A1A7L2, 1A2A1A7A2L1, 1A2A1A7A3R3, and 1A2A1A7R28.

(n) Critical adjustments.

(o) Refer to figure 5-174 for voltage and resistance measurements.

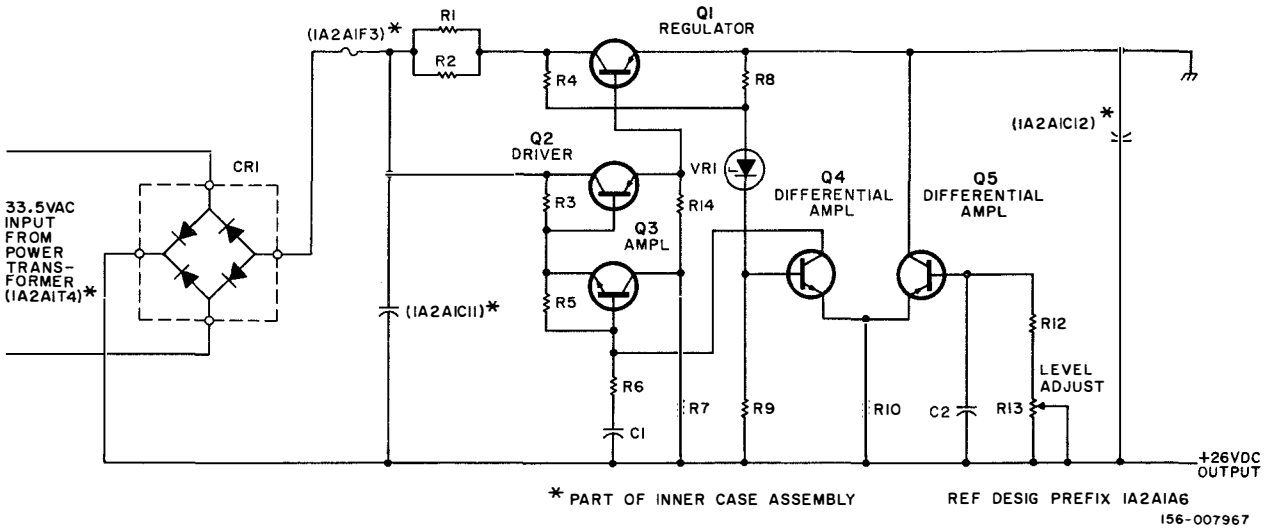


Figure 4-28. Amplifier 1A2, Power Supply and Regulator, Simplified Schematic Diagram

(7) POWER SUPPLY AND VOLTAGE REGULATOR 1A2A1A6, CIRCUIT DESCRIPTION.

The power supply and voltage regulator (see figure 4-28) receives 33.5 VAC, 50/60 cycles, from transformer 1A2A1T4 and supplies +26 VDC, regulated, to the audio amplifier unit. The AC input is rectified by full-wave bridge rectifier CR1 through CR4 and applied through fuse 1A2A1F3 and series regulator Q1 to filter capacitor A1C12. A portion of the output is compared by differential comparator Q4 and Q5 with a reference voltage developed by zener diode VR1. The resultant error voltage is amplified by amplifier Q3 and coupled through driver Q2 to the base of series regulator Q1, thus changing the bias on Q1. An increase in the output voltage increases the base voltage on Q1. The increased base voltage causes a decrease in the emitter current, thus reducing the output voltage. The output of the power supply and voltage regulator is +26 VDC ±0.3 VDC with a maximum ripple factor of 1 MVRMS. The maximum current capacity is 500 MA. Variable resistor R13 sets the output voltage to the required level.

(8) POWER SUPPLY AND VOLTAGE REGULATOR 1A2A1A6, TEST DATA. — Information follows which will be helpful in determining the overall operation of power supply and voltage regulator A6. Refer to figure 4-71 for the circuit location and figures 5-37, 5-41 and 5-51 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) DC output (1A2A1XA6-21) (P): +26 VDC.

(b) AC input to transformer 1A2-A1T4 (1A2A1T4 pins 1 and 4) (20): 115 VAC.

(c) AC input to voltage regulator assembly (1A2A1XA6-12-16): 33.5 VAC ±5%.

(d) Refer to figure 5-173 for transistor voltage measurements.

(e) Refer to paragraph 5-4 for general information and paragraph 5-4a for specific adjustment procedure of 1A2A1A6R13.

4-5. CONVERTER, AMPLITUDE SINGLE-SIDEBAND CV-1846/FRT-24A, (1A3) FUNCTIONAL DESCRIPTION.

a. OVERALL FUNCTIONAL DESCRIPTION (see figure 4-29). - The converter receives 17.75- to 35.60-MC, 100-KC, 1.75-MC, and frequency control signals from synthesizer 1A6. It also receives upper and/or lower sideband audio signals and a 1-MC signal from amplifier 1A2. The signals are processed to produce an output corresponding to the selected frequency and mode of emission. The output of the converter is applied to RF assembly 1A8 for final amplification and application to the antenna. The 1.75-MC signal is amplified by buffer amplifier A4A3 and applied to both ends of balanced modulator A3 (see figure 4-72). The upper and/or lower sideband audio signals modulate 1.75-MC signals to produce a modulated 1.75-MC subcarrier. The modulated subcarriers are filtered by A3FL1 and A3FL2 to remove the carriers and the resulting sidebands are combined to produce a composite 1.75-MC sideband IF signal which is applied through first and second double sideband amplifiers to relay K1 in IF assembly A4. When operating in band 3 or 4, relay A4K1 is deactivated and the signal is applied to linear amplifier A5. The 100-KC input signal is applied to a 300-KC generator A2 in IF assembly A4. When operating in band 1 or 2, the 300-KC input signal from the 300-KC generator is mixed with 1-MC to produce a 1300-KC signal. The 1300-KC signal is mixed with the 1.75-MC to produce a 450-KC composite sideband IF signal which is applied to relay K1 in the IF assembly A4. When operating in band 1 or 2, the relay is activated and the 450-KC IF signal is applied to the linear amplifier. The 17.75- to 35.60-MC input is applied to binary divider A2 and buffer and driver A6. The binary divider divides the signal by 8, 4, and 2 (first three bands) and applies the three outputs to buffer and driver A6. When operating in band 1 (2-4 MC), band 2 (4-8 MC), or band 3 (8-16 MC) as determined by frequency control data from the synthesizer, the buffer and driver select the correct binary divider output. When operating in band 4 (16-32 MC), the synthesizer input is fed directly to the buffer and division does not take place. The output of buffer and driver A6 is applied to linear amplifier A5. The frequency control data, from the synthesizer, is applied to encoder switch S1. Encoder switch S1 is a printed circuit assembly having four etched sliders and six wipers (see figure 5-177). Each slider has an open area which corresponds to an "in-band" condition. For example, when an operating frequency in the 16- to 32-MC band is selected, a momentary pulse is applied to the innermost slider of the switch. The momentary pulse activates relay K2 in frequency offset and bandswitch assembly A1. Relay A1K2 completes the circuit to one winding of motor B2 causing it to rotate. As soon as motor rotation is initiated, detent switch S4 engages, applying +28 VDC to the relay. This keeps the relay activated after the momentary pulse from the synthesizer is removed. Rotation of motor B2 sets switches S1, S2, S3, and S6 to the correct positions for the selected band. When the 16- to 32-MC wiper of encoder switch S1 reaches the open area on the slider, detent switch S4 opens removing +28 VDC from relay A1K2. The relay deactivates and opens the circuit to stop motor B2. The positions of switches S2, S3, and S6 now correspond to the 16- to 32-MC band. Contact 10 of switch S2 applies -12 VDC to enable the 16- to 32-MC band portion of buffer and driver A6. The output of the 16- to 32-MC band portion is applied to linear amplifier A5. Switch S3 selects the required value of resistance for balancing the analog bridge in conjunction with the synthesizer tuning. This procedure is described with the synthesizer automatic tuning portion in paragraph 4-3i. Switch S6 disables the 450-KC circuits and relay K1 in IF assembly A4. The IF assembly produces a 1750-KC or a 450-KC composite sideband IF signal which is applied to linear amplifier A5. The linear amplifier mixes the 1750 KC or 450-KC IF signal with the signal from buffer and driver A6 and produces a representative sideband signal in the selected band. The linear amplifier amplifies the sideband signal and applies it to the RF assembly 1A8. Tuning of the linear amplifier controls are accomplished by motor B1 which rotates in response to voltage from the synthesizer.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for test data. Also perform the applicable steps for the converter in Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

b. FREQUENCY OFFSET AND BAND SELECTOR 1A3A1A1, CIRCUIT DESCRIPTION. The frequency offset and band selector assembly (see figure 5-179) consists of two relays and eight precision bridge balancing resistors. The frequency offset and band selector assembly operates with encoder switch 1A3A1S1, motor 1A3A1B2, and bridge balancing resistor 1A3A1R13. When the converter is operated in the 16- to 32-MC band, a momentary pulse from synthesizer 1A6 is applied through encoder switch 1A3A1S1 to either relay K1 or K2 depending upon the encoder output. When the momentary pulse is applied to relay K1, the relay actuates and remains energized by the 28 VDC applied through holding contacts K2-2 and K2-5. When K2 is energized, servo motor 1A3A1B2 rotates and positions bridge balancing resistor 1A3A1R13. When servo

motor 1A3A1B2 is in the 16- to 32-MC band position, detent switch 1A3A1S4 opens and removes the holding voltage from relay K2, in turn opening the circuit to servo motor 1A3A1B2. Operation of relay K2 is identical to K1 and causes servo motor 1A3A1B2 to rotate in the opposite direction. Rotation of 1A3A1B2 also positions switch 1A3A1S3 to insert the proper amount of resistance in the resistance bridge circuit.

c. FREQUENCY OFFSET AND BAND SELECTOR 1A3A1A1, TEST DATA. - Information follows which will be helpful in determining the overall performance of the frequency offset and band selector circuit. Refer to figure 5-179 for circuit location and figure 5-56 for physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations.

Notes

1. Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

2. The following tests are performed with frequency offset and band switch assembly removed from converter.

(1) Measure resistance between pins on plug P1. Refer to figure 5-179 for resistance values.

(2) Connect ohmmeter between pins 7 and 18 of plug P1. Connect ground to pin 1 of P1. Apply +28 VDC to pin 2 of P1. Ohmmeter should indicate zero ohms. Apply +28 VDC to pin 15 and then remove +28 VDC from pin 2. Relay should remain actuated and ohmmeter should read zero ohms.

(3) Connect ohmmeter between pins 16 and 18 of plug P1. Connect ground to pin 1 of P1. Apply +28 VDC to pin 17 of P1. Ohmmeter should indicate zero ohms. Apply +28 VDC to pin 15 and then remove +28 VDC from pin 17. Relay should remain actuated and ohmmeter should read zero ohms.

(4) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

d. BINARY DIVIDER 1A3A1A2, CIRCUIT DESCRIPTION. - The binary divider assembly (see figure 5-180) consists of a squaring amplifier, amplifier, emitter follower, and three bistable multivibrators connected in cascade. The binary divider assembly receives a 17.75- to 35.60-MC input and divides this frequency range by 2, 4, and 8 when the front panel BAND switch is in positions 16-8, 8-4, and 4-2 respectively. When the BAND switch is in position 32-16, the binary divider does not operate. The 17.75- to 35.60-MC sine wave input is converted to square waves by squaring amplifier Q1. The output of Q1 is amplified by amplifier Q2 and applied through emitter-follower Q3 to the first bistable multivibrator consisting of Q4 and Q5. The divide-by-two output of Q4 and Q5 (9.750 to 17.750-MC) is fed to buffer and driver assembly A6 to cover the 8- to 16-MC band and to the second bistable multivibrator. The divide-by-four output (4.450- to 8.450-MC) of the second bistable multivibrator is fed to buffer and driver assembly A6 to cover the 4- to 8-MC band and to the third bistable multivibrator. The third bistable multivibrator provides a divide-by-eight output (2.450- to 4.450-MC) to cover the 2- to 4-MC band. Refer to Handbook of Electronic Circuits NAVSHIPS 900,000.102 for detailed description of bistable multivibrators.

e. BINARY DIVIDER 1A3A1A2, TEST DATA. - Information which follows will be helpful in determining the overall performance of binary divider A2. Refer to figure 4-72 for circuit location and figures 5-57, 5-67, and 5-69 for physical location of test points. The test equipment required is an electronic counter, a VTVM, an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

To change the synthesizer frequency manually, first set the desired frequency on the MANUAL SETTING digital switch. Remember that the actual output frequency of the synthesizer is 1.75 MC higher than the switch setting. Then set the SERVO MODE switch to MANUAL CHANNEL AUTO and throw the MOTOR DRIVE ON switch to ON. Press the START switch and after completion of tuning cycle throw MOTOR DRIVE ON switch off. To change incremental frequencies of 10 KC, 1 KC, and 100 cycles, it is only necessary to set the applicable digit on the MANUAL SETTING digital switch.

(1) RF input (1A3A1A2J2) (12) : 17.75- to 35.60-MC in 100-cycle steps at 600 MVRMS minimum from synthesizer 1A6. If frequency is unstable or incorrect, refer to paragraph 4-3h.

(2) RF output (1A3A1A2J1-3) (H) : 9.750 to 17.750 MC at 900 MVRMS typical with 19.5 to 35.5-MC input from synthesizer 1A6. If correct, binary divider is operating properly.

(3) RF output (1A3A1A2J1-5) (J) : 4.450 to 8.450 MC at 1.2 VRMS typical with 17.8 to 33.8-MC input from synthesizer 1A6. If correct binary divider is operating properly.

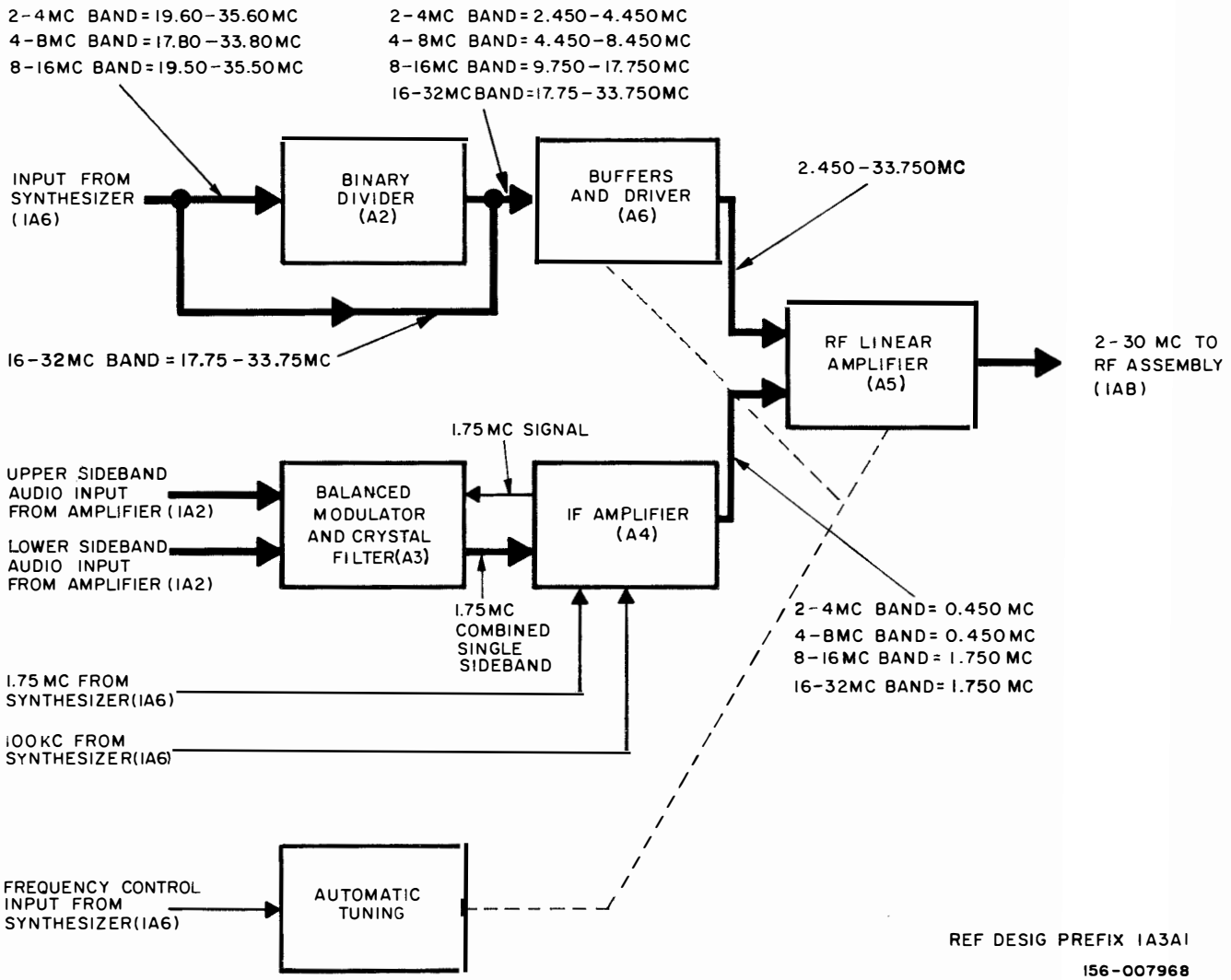


Figure 4-29. Converter 1A3, Overall Functional Block Diagram

(4) RF output (1A3A1A2J1-7) (I) : 2.450 to 4.450 MC at 1.2 VRMS typical with 19.6- to 35.6-MC input from synthesizer 1A6. If correct, binary divider is operating properly.

(5) Refer to figure 5-180 for transistor voltage measurements.

(6) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

f. BUFFER AND DRIVER 1A3A1A6, CIRCUIT DESCRIPTION. - The buffer and driver assembly (see figure 5-187) consists of four buffer amplifiers, a power amplifier, and two driver amplifiers. The assembly contains one buffer amplifier for each operating band. Only one buffer amplifier is energized (B+ voltage applied by switch 1A3A1S2) at a time, depending upon which band is in use. When the converter is operated in the 16- to 32-MC band, the 17.75- to 33.75-MC input from the synthesizer is amplified by buffer amplifier Q1, power amplifier Q2 and driver amplifiers Q6 and Q7 and is applied to emitter-follower Q8. The output of Q8 is applied to RF linear amplifier assembly 1A3A1A5. When the converter is operated in any of the remaining three bands, switch 1A3A1S2 applies B+ voltage to the applicable buffer amplifier. The output of the buffer amplifier is amplified by Q6 and Q7 and fed through emitter-follower Q8 to the RF linear amplifier assembly. Refer to Handbook of Electronic Circuits (NAVSHIPS 900,000.102) for description of buffer amplifiers and emitter followers.

g. BUFFER AND DRIVER 1A3A1A6, TEST DATA. - Information follows which will be helpful in determining the overall performance of buffer and driver A6. Refer to figure 4-72 for circuit location and figure 5-67 for physical location of test points. The test equipment required is an electronic counter, a VTVM, an RF VTVM with 50-ohm adapter (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

To change the synthesizer frequency manually, first set the desired frequency on the MANUAL SETTING digital switch. Remember that the actual output frequency of the synthesizer is 1.75 MC higher than the switch setting. Then set the SERVO MODE switch to MANUAL CHANNEL AUTO and throw the MOTOR DRIVE ON switch to ON. Press the START switch and after completion of tuning cycle throw MOTOR DRIVE ON switch off. To change incremental frequencies of 10 KC, 1 KC, and 100 cycles it is only necessary to set the applicable digit on the MANUAL SETTING digital switch.

(1) RF output in 16- to 32-MC band (1A3A1A6J2) (F) : 17.75-MC to 35.6-MC at 1.2 VRMS into 50-ohm load (typical). If correct, buffer and driver are operating properly.

(2) RF output in 8- to 16-MC band (1A3A1A6J2) (F) : 9.750 to 17.700 MC at 1.2 VRMS into 50-ohm load (typical). If frequency is incorrect, refer to paragraph 4-5d.

(3) RF output in 4- to 8-MC band (1A3A1A6J2) (F) : 4.450 to 8.450 MC at 1.08 VRMS into 50-ohm load (typical). If frequency is incorrect, refer to paragraph 4-5d.

(4) RF output in 2- to 4-MC band (1A3A1A6J2) (F) : 2.450 to 4.450 MC at 1.16 VRMS into 50-ohm load (typical). If frequency is incorrect, refer to paragraph 4-5d.

(5) Refer to figure 5-187 for transistor voltage measurements.

(6) Refer to Maintenance Standards Book for Radio Transmittng Set AN/FRT-24A.

h. BALANCED MODULATORS AND CRYSTAL FILTER 1A3A1A3, CIRCUIT DESCRIPTION. - The balanced modulator and crystal filter assembly (see figure 5-181) consists of two balanced modulators, two buffer amplifiers, two crystal filters, and one linear combiner. Subcarrier inputs of 1.75-MC from IF amplifier assembly 1A3A1A4 and audio inputs from amplifier 1A2 are combined in balanced modulators Z1 and Z2. The balanced modulators provide an upper and lower sideband output with a suppressed subcarrier that is amplified by buffer amplifiers V1 and V3. Buffer amplifiers V1 and V3 are conventional amplifier stages which isolate the crystal filters from the balanced modulators. The output of V1 is fed through crystal filter FL1 to remove the lower sideband frequencies. The output of V3 is fed through crystal filter FL2 to remove the upper sideband frequencies. The lower sideband from FL2 and upper sideband from FL1 are combined in linear combiner V2 to produce a combined single sideband output. Linear combiner V2 is a dual triode operated as a brodband IF amplifier with dual control grids and a common plate load. Mixing of the two sidebands is accomplished with a minimum of cross-modulation or frequency distortion. Current balancing resistor R6 is adjusted for equal voltage gain from either sideband input. The combined single sideband output of V2 is fed to the single sideband input of IF amplifier assembly 1A3A1A4. Refer to Handbook of Electronic Circuits (NAV-

SHIPS 900,000.102) for detailed description of buffer amplifiers and common plate load mixer circuits.

i. BALANCED MODULATOR AND CRYSTAL FILTER 1A3A1A3, TEST DATA. - Information follows which will be helpful in determining the overall performance of balanced modulator and crystal filter A3. Refer to figure 4-72 for circuit location and figures 5-58 and 5-59 for physical location of test points. The test equipment required is an electronic counter, a VTVM, an RF VTVM with 50-ohm adapter, and a radio test set (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(1) RF input (1A3A1A3J1 and 1A3A1A3J5): 1.75 MC at 530 MVRMS into 50-ohm load (typical) and 360 MVRMS unloaded. If frequency is unstable or incorrect, refer to paragraph 4-3c.

(2) Audio input (1A3A1A3J2 and 1A3A1A3J6); 50 MVRMS with a red line reading on applicable LEVEL meter of amplifier 1A2.

(3) Combined single sideband output (1A3A1A3J3): at 9-MV MVRMS into 50-ohm load (typical) on one sideband channel with 50-MVRMS audio input to amplifier. If correct, balanced modulator and crystal filter is operating properly.

(4) B+ (1A3A1A3J4-A-D): +180 VDC.

(5) Filament voltage (1A3A1A3J4-B-C): 6.3 VAC.

(6) Refer to figure 5-181 for voltage and resistance measurements.

(7) Refer to paragraph 5-5 for geneeral information and paragraph 5-5c for specific alignment procedure of 1A3A1A3R6.

j. IF AMPLIFIER 1A3A1A4, CIRCUIT DESCRIPTION. - The IF amplifier assembly (see figure 5-182) consists of 1750-KC buffer amplifier A3, carrier insertion circuits, 450-KC IF circuits, 300-KC generator A2, 1300-KC generator A1, and 450-KC sideband mixer, amplifier and filter circuits. The 1750-KC subcarrier circuits of the IF assembly include the 1750-KC buffer, carrier gate, sideband mixer, and 1750-KC sideband amplifier. At the 1750-KC and 450-KC subcarrier frequencies, these circuits produce a modulated 1750-KC subcarrier for application to RF linear amplifier assembly 1A3A1A5 and perform the carrier injection function. On the two high operating bands (8 to 30 MC), the 1750-KC sideband amplifier delivers the modulated 1750-KC subcarrier directly to the assembly output. On the two low frequency bands (2 to 8 MC), 1750-KC sideband amplifier V5 is disabled, and the sideband mixer output is converted to a modulated subcarrier frequency of 450 KC.

(1) 1750-KC BUFFERS A3. - Two identical transistorized buffer amplifiers in subassembly A3 isolate the 1750-KC reference frequency input from the 1750-KC circuits in the IF amplifier assembly (see figure 5-185). Amplifiers Q1 and Q2 are class A, common emitter amplifiers with tuned resonant collector loads. A sample of the 1750-KC reference frequency input is detected by diode CR1 to provide a DC signal for monitoring on the front-panel meter. A second 1750-KC reference frequency input sample is tapped from potentiometer R9 and applied to the carrier gate. Refer to Handbook of Electronic Circuits (NAVSHIPS 900,000.102) for description of class A, common-emitter amplifiers.

(2) CARRIER INSERTION. - The carrier insert gate, carrier mixer, and 1750-KC sideband amplifier control insertion of the carrier during transmission of CW, compatible AM or SSB reduced carrier. Carrier gate V3 is an interstage-tuned IF amplifier. Carrier insertion is controlled by contacts of carrier insert relay K2, which injects the 1750-KC subcarrier at the control grid of V3. A bias voltage of three different levels, determined by carrier insert assembly A8, varies the gain of the IF amplifier to determine the 1750-KC output amplitude. The control range extends in four steps; 0 DB, -10 DB, -20 DB, and suppressed carrier (-60 DB). Suppressed carrier is accomplished by removing the plate voltage and grounding the control grid. In the first 1750-KC double sideband amplifier V4, the sidebands are summed in a resistive mixer and combined with a controlled amount of carrier from the insert gate. Except for the dual control grids, which permit linear additive mixing for minimum intermodulation and frequency distortion, the carrier mixer is a conventional interstage-tuned IF amplifier as is the second 1750-KC sideband amplifier. Refer to Handbook of Electronic Circuits (NAVSHIPS 900,000.102) for description of amplifier circuits.

(3) 300-KC GENERATOR A2 AND 1300-KC GENERATORS A1. — In these assemblies the 100-KC reference frequency input from synthesizer 1A6 is multiplied by three and mixed with the 1-MC reference frequency input in a balanced mixer (see figures 5-183 and 5-184). The sum frequency (1300 KC) is filtered and fed to succeeding stages by a buffer amplifier. The X3 frequency multiplier and 300-KC buffer are basically conventional interstage-coupled IF amplifiers. The frequency multiplier is overdriven to produce odd-harmonic distortion. In the 1300-KC circuits, the 1-MC reference frequency input is coupled to transformer A1T2 through the impedance-matching and isolating network of transformer A1T1 and capacitors A1C1 and A1C2. The tuned circuit bypasses the 1-MC reference frequency to the modulator but prevents reverse feedback of the mixing process products. Mixing is accomplished by a balanced diode mixer in the secondary circuit of transformer A1T2. The 1-MC reference signal is applied out of phase to the two diodes while the 300-KC signal is applied in phase to both diodes. The resultant developed across potentiometer A1R2 contains the sum and difference frequencies produced by the mixing action. The 1-MC reference frequency can be suppressed by balancing A1R2. The 300-KC signal is greatly attenuated in succeeding tuned circuits. A bandpass filter consisting of two capacitively-coupled, parallel-resonant filters eliminates all the input signals except 1300 KC. The filtered output from the secondary of transformer A1T3 drives the 1300-KC buffer amplifier. Refer to Handbook of Electronic Circuits (NAVSHIPS 900,000.102) for description of transistor amplifier circuits.

(4) 450-KC SIDEBAND MIXER, AMPLIFIER AND FILTER. — The modulated 1750-KC subcarrier with controlled carrier is obtained from 1750-KC amplifier V4 and mixed with the 1300-KC signal in mixer V1. (See figure 5-182.) Mixer V1 is a dual triode with common plate and cathode loads. A nonlinear operating point produces intermodulation; the selective tuned circuits in the plate load of V1 and in subsequent amplifier V2 extract the modulated 450-KC subcarrier. A low-pass filter following V2 provides additional rejection of undesired frequency components. In the low-frequency operating range (2 to 8 MC), relay K1 is energized, and the modulated 450-KC subcarrier is applied to the output of the IF assembly. Also external band switch contacts enable the 450-KC amplifiers and disable the 1750-KC output amplifier by switching the 180-VDC B+ lines. Refer to Handbook of Electronic Circuits (NAVSHIPS 900,000.102) for description of common plate mixer circuits.

(5) CARRIER INSERTION AND SUBCARRIER FREQUENCY SELECTION. — Selection of CW, compatible AM and SSB suppressed carrier operation occurs through external circuitry. Energizing relay K2 applies the 1750-KC carrier to the carrier insert gate V3. Application of 180 VDC to the carrier insert gate V3 then enables the circuit. An external bias voltage applied to the control grid of this stage regulates the carrier gate voltage gain and determines the amount of carrier to be mixed with the sidebands in the carrier insert mixer. For selection of the 1750-KC or 450-KC modulated subcarrier, sections of an external bandswitch are used. On the low bands (2 to 8 MC) where the 450-KC modulated subcarrier is required, the 180-VDC plate supply is removed from 1750-KC sideband amplifier V5 and applied to the 450-KC sideband amplifier. Relay K1 is energized, and the 450-KC modulated subcarrier is connected to the output of the IF assembly. On high bands (8 to 30 MC) where the 1750-KC modulated subcarrier is required, the 450-KC sideband amplifier is disabled and the 1750-KC counterpart is enabled by the switched 180-VDC plate supply. Relay K1 is de-energized, delivering the 1750-KC modulated subcarrier to the output of the IF assembly.

k. IF AMPLIFIER 1A3A1A4, TEST DATA. — Information follows which will be helpful in determining the overall performance of IF amplifier A4. Refer to figure 4-72 for circuit locations and figures 5-60 through 5-64 for physical location of test points. The test equipment required is an electronic counter, a VTVM and an RF VTVM with 50-ohm adapter (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(1) IF output for 8- to 32-MC bands (1A3A1A4J3) (G): 1750 KC at 920 MVRMS with P18 connected, 145 MVRMS with P18 disconnected, and 45 MVRMS with 50-ohm load (VTVM adapter); with 50 MVRMS upper sideband audio input measured at 24-MC antenna frequency. If correct, IF amplifier is operating properly.

(2) IF output for 2- to 8-MC bands (1A3A1A4J3) (G): 450 KC at 240 MVRMS with P18 connected, 210 MVRMS with P18 disconnected, and 64 MVRMS with 50-ohm load (VTVM adapter); with 50 MVRMS upper sideband audio input measured at 4-MC antenna frequency. If correct, IF amplifier is operating properly.

(3) RF output of 1300-KC generator Bands A and B (1A3A1A4XA1J3) (DF): 1300 KC at 440 MVRMS with 1A3A1A4P2 connected, 460 MVRMS with 1A3A1A4P2 disconnected, and 180 MVRMS with 50-ohm load (VTVM adapter).

(4) RF output of 300-KC generator (1A3A1A4XA2J2) (DE) : 300 KC at 600 MVRMS with 1A3A1A4P6 connected, 1.4 VRMS with 1A3A1A4P6 disconnected, and 63 MVRMS with 50-ohm load (VTVM adapter).

(5) RF output of 1750-KC amplifier (1A3A1A4XA3J3) (DH) : 1750 KC at 23 MVRMS with 1A3A1A4P3 connected, 390 MVRMS with 1A3A1A4P3 disconnected, and 23.5 MVRMS with 50-ohm load (VTVM adapter).

(6) Refer to figures 5-182 through 5-185 for voltage and resistance measurements.

(7) Refer to paragraph 5-5 for general information and paragraphs 5-5a through 5-5d for specific alignment procedures of 1A3A1A4C28, 1A3A1A4C34, 1A3A1A4R21, 1A3A1A4C38, 1A3A1-A4C2, 1A3A1A4C3, 1A3A1A4R5, and 1A3A1A4C6.

l. RF LINEAR AMPLIFIER 1A3A1A5, FUNCTIONAL DESCRIPTION.

(1) OVERALL FUNCTIONAL DESCRIPTION. — The automatically tuned, RF linear amplifier assembly (see figure 4-72) heterodynes the modulated subcarrier from IF amplifier assembly A4 with the RF signal from buffer and driver assembly A6. It selects the difference frequency, and amplifies this difference signal to a 250-MW level. On the two lower bands (2 to 8 MC), the subcarrier is 450 KC above the linear amplifier output frequency. On the two higher bands (8 to 16 MC), the subcarrier is 1750 KC above the linear amplifier output frequency. The principal circuits are a diode mixer, three gain-controlled RF amplifiers, an output power amplifier, and diode detectors for metering samples of the external RF input and linear amplifier output. The subcarrier from the IF amplifier assembly is combined with the frequency from the buffer and driver assembly in the mixer. The mixer is a diode balanced modulator that receives the input signals and passes only the sum and difference frequencies. The difference frequency, corresponding to the final output frequency, is amplified by the three highly selective RF amplifiers and the output amplifier. The first amplifier gain is controlled by CHAN RF GAIN controls 1A3A1R1 through 1A3A1R10 or front-panel RF GAIN control 1A3A1R14. The second amplifier gain is controlled by an APC (average power control) voltage input and the third stage is controlled by a PPC (peak power control) voltage input.

(2) OVERALL TEST DATA. — Information follows which will be helpful in determining the overall performance of the RF linear amplifier A5 circuit. Refer to figure 4-72 for circuit location and figures 5-65 through 5-67 and 5-69 for physical location of test points. The test equipment required is an electronic counter, a VTVM, and an RF VTVM with 50-ohm adapter (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

To change the synthesizer frequency manually, first set the desired frequency on the MANUAL SETTING digital switch. Remember that the actual output frequency of the synthesizer is 1.75 MC higher than the switch setting. Then set the SERVO MODE switch to MANUAL CHANNEL AUTO and throw the MOTOR DRIVE ON switch to ON. Press the START switch and after completion of tuning cycle throw MOTOR DRIVE ON switch off. To change incremental frequencies of 10 KC, 1 KC, and 100 cycles, it is only necessary to set the applicable digit on the MANUAL SETTING digital switch.

(a) RF output (1A3A1A5E9) (11) : 2 to 30 MC at 2.2 VRMS minimum. If correct, RF linear amplifier assembly is operating properly.

(b) IF input, 2- to 8-MC bands (1A3A1A5J2) (G) : 450 KC at 240 MVRMS with P19 connected, 210 MVRMS with P19 disconnected, and 64 MVRMS with 50-ohm load (VTVM adapter); measured at 4 MC antenna frequency. If incorrect, refer to paragraph 4-5j.

(c) IF input, 8- to 32-MC bands (1A3A1A5J2) (G) : 1750 KC at 920 MVRMS with P19 connected, 145 MVRMS with P19 disconnected, and 45 MVRMS with 50-ohm load (VTVM adapter); measured at 24-MC antenna frequency. If incorrect, refer to paragraph 4-5j.

(d) RF input, 2- to 4-MC bands (1A3A1A5J1) (F) : 2.450 to 4.450 MC at 2.4 VRMS with P20 connected, 53 MVRMS with P20 disconnected, 1.15 VRMS with 50-ohm load (VTVM adapter). If incorrect, refer to paragraph 4-5d.

(e) RF input, 4- to 8-MC bands (1A3A1A5J1) (F) : 4.450 to 8.450 MC at 1.65 VRMS with P20 connected, 80 MVRMS with P20 disconnected, and 1.05 VRMS with 50-ohm load (VTVM adapter). If incorrect, refer to paragraph 4-5d.

(f) RF input, 8- to 16-MC bands (1A3A1A5J1) (F) : 9.750 to 17.750 MC at 3.3 VRMS with P20 connected, 120 MVRMS with P20 disconnected, and 1.2 VRMS with 50-ohm load (VTVM adapter). If incorrect, refer to paragraph 4-5d.

(g) RF input, 16- to 32-MC bands (1A3A1A5J1) (F) : 17.75 to 33.75 MC at 4.0 VRMS with P20 connected, 150 MVRMS with P20 disconnected, and 1.2 VRMS with 50-ohm load (VTVM adapter). If incorrect, refer to paragraph 4-5d.

(h) Refer to figure 5-186 for voltage and resistance measurements.

(i) Refer to paragraph 5-5 for general information, and 5-5f and 5-5i for specific alignment procedures.

(3) MIXER, CIRCUIT DESCRIPTION. The modulated subcarrier is heterodyned with the RF signal from buffer and driver 1A3A1A6 in a diode balanced modulator consisting of transformer T1, diodes CR2 and CR3, and capacitor C73 (see figure 5-186). Maximum rejection of the input frequencies in favor of the sum and difference products is obtained by adjustment of balancing potentiometer R28 and capacitor C73. A sample of the buffer input voltage is detected by diode CR4 for monitoring on the front-panel METER. The difference frequency from the balanced modulator is separated from the sum frequency by the subsequent highly selective amplifier stages. This difference frequency contains the same audio modulation as the subcarrier, but is translated to the desired final output frequency.

(4) MIXER, TEST DATA. — Information follows which will be helpful in determining the overall performance of the mixer circuit. Refer to figure 4-72 for circuit location and figure 5-65 for physical location of test points. The test equipment required is an electronic counter, a VTVM, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Output of mixer with converter set up for antenna frequency of 2 MC on band A (1A3A1A5XV1-2): 2 MC at 490 MVRMS.

(b) Output of mixer with converter set up for antenna frequency of 8 MC on band C (1A3A1A5XV1-2): 8 MC at 710 MVRMS.

(c) Check that front panel METER reads in the red area with METER SWITCH in SYNTH position.

(5) FIRST, SECOND, AND THIRD RF AMPLIFIERS, CIRCUIT DESCRIPTION. — The mixer output must be amplified with sufficient selectivity to extract the difference component of the modulation products, but with a bandpass wide enough to accommodate AM frequencies up to 4 KC on either side of the carrier. This is achieved in three cascaded, interstage-tuned, pentode RF linear amplifiers, V1, V2, and V3, with provisions for gain control, bandswitching, and fine tuning (see figure 5-186). Bandswitching is performed by sections of switch S1 and S2. A different interstage coupling transformer is selected for each band, the remaining three transformers are inactive in the circuit having their secondaries grounded. The transformer primaries are connected together for reduction of stray signal pickup. Fine tuning is performed by air-dielectric, variable tuning capacitors across the interstage transformer primaries. Amplifier V1 receives a gain control voltage from resistor R14 in the manual mode of operation and from resistors 1A3A1R1 through 1A3A1R10 in the preset mode of operation. APC controls the gain of the second linear RF amplifier and PPC controls the gain of the third linear RF amplifier.

(6) FIRST, SECOND, AND THIRD RF AMPLIFIERS, TEST DATA. — Information follows which will be helpful in determining the overall performance of the first, second, and third RF amplifiers. Refer to figure 4-72 for circuit location and figures 5-65 and 5-66 for physical location of test points. The test equipment required is an electronic counter, and an RF VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Refer to figure 5-180 for voltage and resistance measurements.

(b) Refer to paragraph 5-5 for general information and paragraph 5-5f for specific alignment procedures of 1A3A1A5T11 through 1A3A1A5T13 and 1A3A1A5C7 through 1A3A1A5C45.

(7) OUTPUT AMPLIFIER, CIRCUIT DESCRIPTION. — The output amplifier is a tuned RF amplifier similar to the preceding stages but employs an RF power pentode to produce a peak 250-milliwatt level and 50-ohm impedance at terminal E9. A sample of the RF output is detected by diode CR1 and made available for monitoring the RF output on the front-panel METER.

(8) OUTPUT AMPLIFIER, TEST DATA. — Information follows which will be helpful in determining the overall performance of the output amplifier circuit. Refer to figure 4-72 for circuit location and figure 5-65 for physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Check that front panel METER reads in the red.

(b) Refer to figure 5-186 for voltage and resistance measurements.

(c) Refer to paragraph 5-5 for general information and paragraph 5-5f for specific alignment procedures of 1A3A1A5T14 through 1A3A1A5T17 and 1A3A1A5C54 through 1A3A1A5C60.

m. CARRIER INSERT AND GAIN CONTROL 1A3A1A7 (see figure 5-177). — The carrier insert and gain control assembly consists of four carrier insert and gain control relays and three potentiometers.

(1) CW EMISSION. — When the converter is operated in the CW (A1) mode of emission, a ground signal actuates relay K2. Operation of K2 applies a carrier insert level to the control grid of 1750-KC carrier gate V3 in IF amplifier assembly 1A3A1A4. The amount of carrier is set by A1 carrier level adjustment R1. Relay K4 also actuates, providing plate and screen voltage to 1750-KC carrier gate 1A3A1A4V3.

(2) COMPATIBLE AM EMISSION. — When the converter is operated in the compatible AM mode of emission, a ground signal actuates relay K3. Operation of K3 applies a carrier insert level to the control grid of 1750-KC carrier gate 1A3A1A4V3. The amount of carrier is set by A3a carrier level adjustment R2. Relay K3 also applies an average power control (APC) level to 2nd RF amplifier V2 in RF linear amplifier assembly 1A3A1A5. This level is set by average power control adjustment R7. Relay K4 also actuates, applying plate and screen voltage to 1A3A1A4V3.

(3) SSB EMISSION. — When the converter is operated in the single sideband mode of emission, a ground from SSB switch 1A3A1S7 also selects the amount of carrier (0 DB, 10 DB and 20 DB) which applies a preset bias level controlled by RF GAIN control 1A3A1R14. When 1A3A1S7 is in the SUPPR CARRIER position K4 deenergizes. When K4 is actuated, it applies +26 VDC to carrier insert relay 1A3A1A4K2 and plate and screen voltage to 1750-KC carrier gate 1A3-A1A4V3. When RF GAIN control 1A3A1R14 is set to PRESET, relay K5 energizes and the gain of 1st RF amplifier V1 in RF linear amplifier assembly 1A3A1A5 is controlled by channel RF gain resistors 1A3A1R1 through 1A3A1R10. When K5 is energized, the gain of 1A3A1A5V1 is controlled by RF GAIN control 1A3A1R14.

n. CARRIER INSERT AND GAIN CONTROL 1A3A1A7, TEST DATA. — Information follows which will be helpful in determining the overall performance of carrier insert and gain control 1A3A1A7. Refer to figure 5-177 for circuit location and figure 5-55 for physical location of test points. Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A for additional test data.

4-6. RADIO TRANSMITTER T-973/FRT-24A, UNIT 1, FUNCTIONAL DESCRIPTION.

a. OVERALL FUNCTIONAL DESCRIPTION. — A simplified block diagram of Radio Transmitter T-973/FRT-24A is part of the overall block diagram of the Radio Transmitting Set, shown in figure 4-1. The transmitter consists of thirteen major items. One of these items is a cabinet (1A13) with accessories including blower assembly 1A13B641, which supplies air cooling to the high-power tubes in RF assembly 1A8. The cabinet houses RF assembly 1A8, dial control 1A1, power control 1A9, HV supply 1A10, LV supply 1A11, service supply 1A12, and patch panel 1A13A3. The cabinet also houses synthesizer 1A6, amplifier 1A2, converter 1A3, synthesizer power supply 1A4, and exciter power supply 1A7. These units are discussed separately and will be mentioned here to preserve continuity.

The RF assembly (see figure 5-207) is capable of generating up to 1 kilowatt of RF energy into a 52-ohm load. The frequency range of 2 to 30 MC is developed in synthesizer and converter units and applied to the RF assembly through the patch panel assembly. These frequencies, which are also known as channels, must not be confused with the term "band". The operating frequency range of the transmitter is divided into eight portions, or bands; for example, band 1 occupies the range of 2 to 3 MC, band 2 occupies the range of 3 to 4 MC, etc., as shown in paragraph 1-4b.

All tuning controls (including the 10-position channel switch and the eight-position band switches used in the RF stages of the transmitter) that are repositioned for a change in operating frequency are coupled to autotune motor B240 through mechanical positioning heads. The control head is capable of positioning the channel-switch shaft to 10 positions corresponding to 10 frequency channels, whereas six single-turn heads can position their respective eight-position switches or tuning capacitor controls to a position in one of the eight bands corresponding to the frequency channel selected. The autotune motor is actuated through a 10-position CHANNEL SELECTOR switch and a parallel-connected switching arrangement located on the control head. When a channel is selected either through the front-panel selector switch or at a remote point through the dial control, the autotune system automatically sets up the switches and tuning controls connected to the appropriate RF stages.

The voltage regulator employs two voltage reference tubes connected in series between the -150-volt and +600-volt power supplies; three

parallel-connected voltage-regulator tubes maintain a constant 300 volts for operation of the low-level RF stages.

The power control assembly (see figure 5-210) consists of control branches and primary circuits for applying 115 VAC or 230 VAC as required, to all circuits of the transmitter for operating the power, channel, and emission-selection systems. A local-remote switch in this unit sets up the transmitting set for operation locally or from one of the two remote stations. The assembly also contains a mode switch to select the type of emission (SSB-CW-AM); an electronic time-delay circuit (V501) which delays application of primary power to the LV and HV supplies during the 5-minute warm-up period; and a mechanical time delay of 1.5 seconds for momentary B+ delay, when switching from LV to HV.

The dial control assembly (see figure 5-167) contains relays actuated by pulses from Transmitter Control C-6466/FRT-24A. During remote operation of the transmitter these relays are capable of actuating the control circuits in the power control assembly to turn the transmitter on and off, to select the frequency channel by operating the autotune system, and to select the desired type of emission.

The LV supply (see figure 5-212) utilizes V301 and V302, connected as a fullwave rectifier, to deliver 620 VDC to the RF assembly. The HV supply (see figure 5-211) employs V401 and V402, connected as a full-wave rectifier, to deliver 3000 VDC to the plate circuits of the RF power amplifier. The service supply (see figure 5-213), consisting of an auto transformer, is connected to the primary power of the transmitter to supply power for Power Supply PP-4243/FRT-24A and Power Supply PP-4242/FRT-24A.

b. RF ASSEMBLY 1A8, FUNCTIONAL SECTION DESCRIPTION. — The RF assembly (see figures 4-83 and 5-207) consists of a tuned amplifier, RF driver, and final power amplifier. It also contains a voltage regulator, a power amplifier screen voltage regulator and an automatic tuning (autotune) system. The assembly receives the selected RF signal from converter 1A3. The RF signal is amplified and may be applied to the transmission line coupler (unit 7) for eventual application to the antenna or directly to a 50-ohm antenna. Tuning of the stages within the RF assembly is accomplished automatically by a single motor driving a control head and a series of single-turn heads. During remote automatic operation, the motor responds to digital information received from the transmitter control unit through dial control 1A1. During local automatic operation, the motor is controlled by CHANNEL SELECTOR SWITCH S243. The autotune system can be preset to operate on any of 10 frequency channels. When a new frequency channel is selected, autotune motor B240 rotates and positions the various controls in the RF assembly accordingly. At the same time, ground pulse information is sent to synthesizer 1A6 which, in turn, tunes the synthesizer circuits and converter 1A3 to the selected frequency. Automatic tuning of the synthesizer and converter is described in paragraph 4-3i. The RF signal input from the converter is applied to the cathode of amplifier V116. Tuning of V116 is accomplished by switch S109A and S109B and EXCITER TUNING control C114A and C114B. Switches S109, S103, S104, and S106 are mechanically ganged and together constitute the BAND SWITCH. During automatic operation, the BAND SWITCH is positioned by single-turn head O-288 and O-290 as described in paragraph 4-b(11)(a). The amplified output of exciter V116 is coupled through capacitor C247 to the grid of RF driver V114. The RF driver is a high level class AB amplifier which supplies sufficient signal amplification to drive power amplifier V115. Tuning of V114 is accomplished by switch S103 and DRIVER TUNING control C125. Voltage for amplifier V116 and RF driver V114 is supplied by voltage regulators V108 through V112. The output of the RF driver is coupled through capacitor C124 to the grid of power amplifier V115. The signal is amplified by V115 and coupled through a modified "Pi" network to the transmission line coupler or to a 50-ohm antenna. Tuning of the power amplifier is accomplished by BAND SWITCH portions of S104, LOADING COIL SWITCH S105, PA PLATE LOADING control C134, and PA LOADING control C135. During CW operation, a grid block voltage is applied to amplifier V116 approximately 0.3 second after completion of keying the transmitter. This cuts off V116 and disables the transmitter for on-off CW operation.

(1) AMPLIFIER 1A8V116, CIRCUIT DESCRIPTION. — The amplifier (see figure 4-30) receives the selected RF frequency in the 2- to 30-MC range from converter 1A3. The RF signal is applied to the cathode of amplifier V116. The RF signal is amplified and applied to RF driver V114. Tuning is accomplished by BAND SWITCH S109 and EXCITER TUNING capacitors C114A and C114B. When the operating frequency is changed during automatic operation, autotune motor B240 rotates. The BAND SWITCH S109 and EXCITER TUNING capacitors C114A and C114B are mechanically coupled to the motor through a series of single-turn heads. Rotation of the motor rotates the switch and capacitors, thus tuning the amplifier to the selected frequency. Degenerative feedback from power amplifier V115, is applied to the grid of the amplifier. Application of degenerative feedback improves the amplifier linearity and provides the required bandwidth during compatible AM and single sideband operation. The output of the amplifier is coupled through BAND SWITCH S109 and capacitor C247 to the grid of RF driver V114.

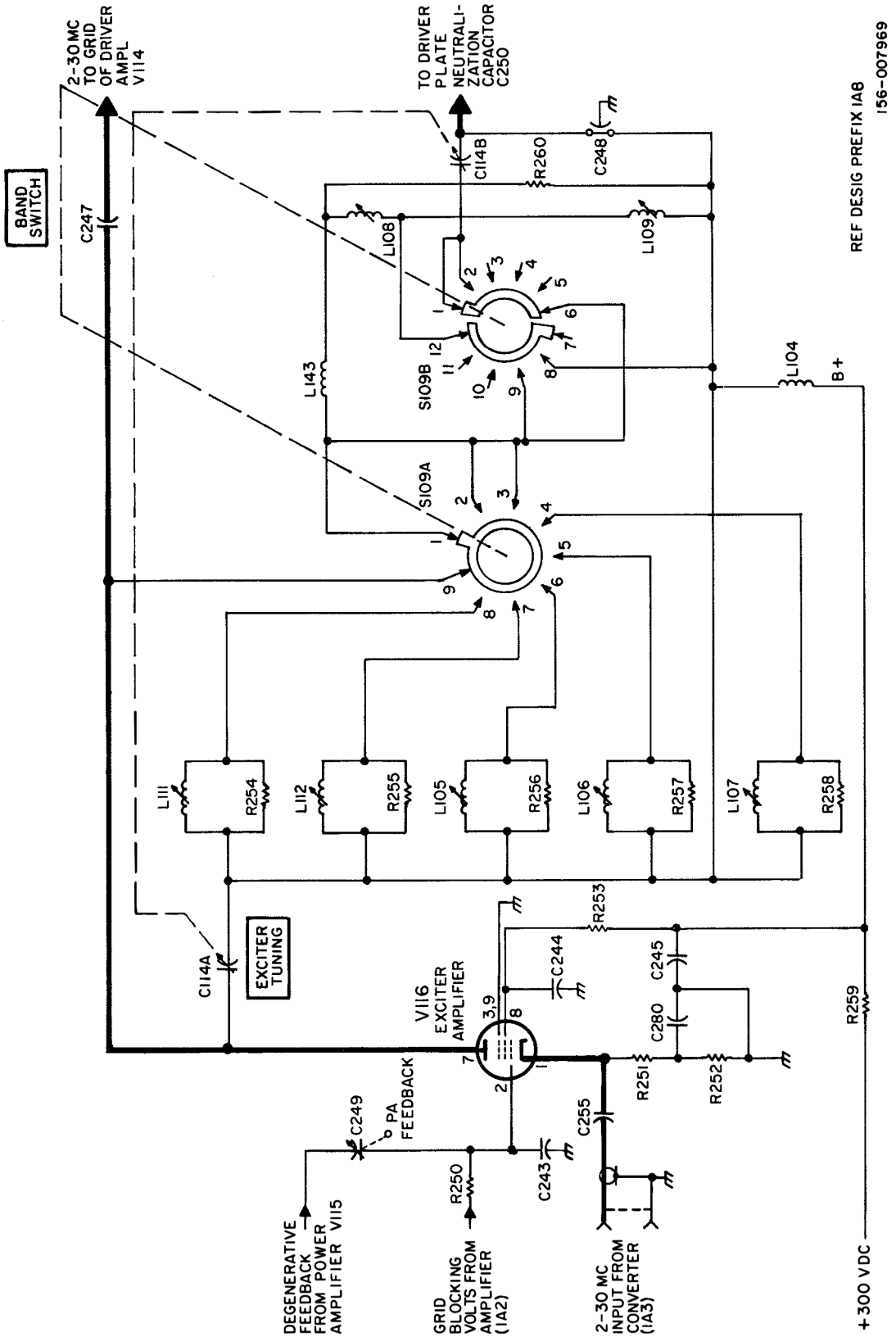


Figure 4-30. RF Assembly 1A8, Amplifier, Simplified Schematic Diagram

(2) AMPLIFIER 1A8V116, TEST DATA. — Information which will be helpful in determining the overall operation of the amplifier is listed below. Refer to figure 4-83 for circuit location and figures 5-127 and 5-128 for physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Check front panel MULTIMETER reading with multimeter switch 1A8S108 in 1st AMPL V X 1000 position. Refer to table 3-11 for typical meter readings.

(b) Refer to figure 5-207 for voltage and resistance measurements.

(c) Refer to paragraph 5-6 for general information and paragraph 5-6e for specific alignment procedures of 1A8L105, 1A8L106, 1A8L107, 1A8L108, 1A8L109, 1A8L111, 1A8L112, and 1A8C249.

(d) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

(3) RF DRIVER 1A8V114, CIRCUIT DESCRIPTION. — The RF driver (see figures 4-31 and 5-207) receives the RF output from amplifier V116 and provides sufficient excitation to drive power amplifier V115. RF driver V114 is a class AB amplifier. Fixed bias of -30 to -90 VDC is supplied by bias rectifier V113. The input frequency applied to the control grid of V114 through coupling capacitor C247 is controlled by switch S109A or S109B depending upon band of operation. The plate circuit is shunt-fed, the DC voltage being applied through RF choke L114, and the RF output through capacitor C124 to a tuned circuit consisting of variable capacitor C125 and a tapped inductor consisting of L115, L116, and L117. Wafer switch S103 introduces a different portion of this inductor to change the resonant frequency of the tank circuit to conform to each new band, and also shorts out the unused portion of the tank inductor to avoid detuning effects. For operation in the 2- to 3-MC band, the three coils are in series. On progressively higher-frequency bands, L117 and additional turns on L116 and L115 are shorted to produce the correct inductance for the operating frequency. The plate tank circuit is tuned to the exact frequency by variable air dielectric capacitor C125. The manual positioning or presetting of C125 is controlled from the front panel by the DRIVER PLATE TUNING control. During channel selection, the capacitor can be returned automatically to the preset position by single-turn head O-286 of the autotune system. S103 is part of the BAND SWITCH control, and is positioned together with S104, S106, and S109. RF driver V114 is biased for class AB operation with fixed bias which is applied to the grid. MULTIMETER M113 monitors the RF driver grid voltage when the multimeter switch is in the DR BIAS V X 200 position. The meter also monitors the RF driver grid current or plate current when the switch is in the DR GRID MA X 20 or DR PLATE MA X 100 positions, respectively. The plate voltage for the stage, +620 volts, is applied to the plate load impedance (L114) through meter M102 and an RF filter, consisting of L131, C145, C146, and C276 for bypassing the RF current away from the power supply. The screen grid is maintained at RF ground potential by capacitors C268 and C269 which acts as an interelectrode shield. Capacitor C250 is adjusted for proper neutralization of V114.

(4) RF DRIVER 1A8V114, TEST DATA. — Information which will be helpful in determining the overall operation of the RF driver is listed below. Refer to figure 4-83 for the circuit location and figures 5-127 and 5-128 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Check front panel MULTIMETER reading with multimeter switch 1A8S108 in DR GRID MA X 20, DR PLATE MA X 100, DR PLATE V X 100, and DR BIAS V X 200 positions. Refer to table 3-11 for typical meter readings.

(b) Refer to figure 5-207 for voltage and resistance measurements.

(c) Refer to paragraph 5-6 for general information and paragraph 5-6f for specific alignment procedures of 1A8C250.

(d) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

(5) POWER AMPLIFIER 1A8V115, CIRCUIT DESCRIPTION. — Power amplifier V115 (see figure 4-32) receives RF drive from RF driver V114 and provides final amplification for the RF signal. The power amplifier is capable of developing 1000-watt average power when operating type A1 mode of emission, 1000-watt peak envelope power (PEP) when operating in types A3b, A3j and F1 modes of emission, and 400-watt nominal carrier power when operating in type A3a mode of emission. The output of V115 is coupled through the directional coupler to the

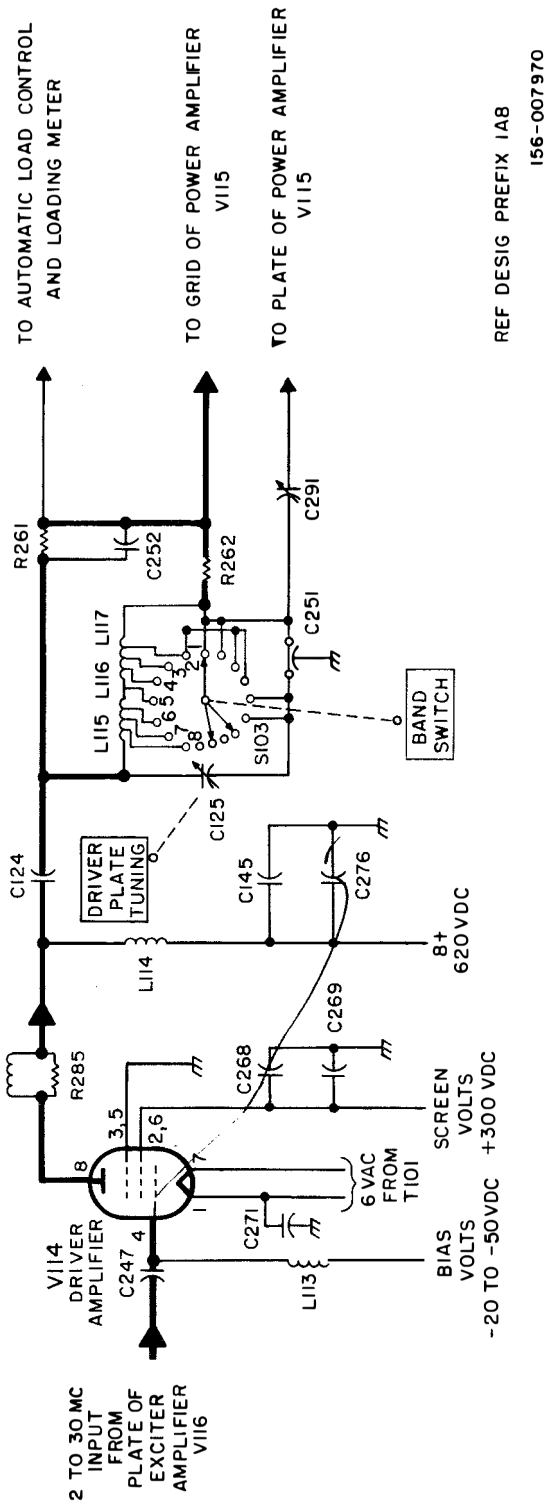


Figure 4-31. RF Assembly 1A8, RF Driver, Simplified Schematic Diagram

antenna or to the Transmission Line Coupler CU-390/FRT-24. Power amplifier V115 is biased for class AB operation by fixed bias supplied by bias rectifier V113 through the meter switching panel. When the multimeter switch is in the PA BIAS V X 200 position, MULTIMETER M113 monitors the power amplifier grid bias voltage. When the switch is in the PA GRID MA X 20 position, the meter monitors the power amplifier grid current. When the switch is in the PA FIL V X10 position, the meter monitors the power amplifier filament voltage.

The input frequency is applied through parasitic-suppressor R261 and C252 and coupling capacitor C124 to the control grid of V115. The output signal from the plate of V115 is applied to the plate tuned circuit through parasitic-suppressor circuit PC 102 and capacitor C132. The plate is shunt-fed, the DC voltage being applied through RF chokes L119 and L120. Switch S106 shorts out L120 in all bands above the third (6 MC), in order to maintain suitable RF choke characteristics over the entire frequency range. The power-amplifier tuned circuit is a pi-type, impedance-matching network which greatly attenuates harmonics and provides an excellent match between the high-impedance plate circuit and a low-impedance load. The Pi-network consists of vari-of coils L127 and L128 joined to a modified Pi-tapped inductor comprising coils L123 to L126, and sections of plate load variable capacitors C135 A/B and/or C136 A/B. S104 is an eight-position switch which introduces a different amount of inductance to change the resonant frequency of the pi network to conform with each new band. It also shorts out the unused portion of the inductance to avoid detuning effects. Another portion of this switch introduces one or more sections of C135 and/or C136 as shown in table 4-3. These capacitor sections are preset by the PA LOADING control to adjust the tank current, while C134, which resonates the plate circuit to the exact frequency is preset by the PA PLATE TUNING control. During channel selection these controls can be returned automatically to their preset positions by single-turn heads O-285 and O-289, of the autotune system.

The output of the network consists of coils L127 and L128 joined to a modified Pi-network which is mounted on a separate chassis and connected between L134 and L136 to supply additional harmonic-frequency suppression. These networks are used to match a 52-ohm load, and cancel the reactance of the load at the particular output frequency. Switch S105 adjusts the inductance of loading coils L127 and L128 for each frequency band. Normally, positions 1 through 8 of this switch correspond respectively with the eight bands previously selected by the BAND SWITCH. Since S105 is preset separately by the LOADING COIL SWITCH control (which can then be automatically returned to this position by single-turn head O-288 of the autotune system during channel selection), the switch can be adjusted independently to compensate for variations in load impedance. The inductance is changed in a conventional manner, turns of L127 and L128 being shorted together as the switch arm is advanced from position 00 to position 10. The modified Pi-network consists of coils L134, L135 and L136 as the arm of the Pi-network and capacitors C182 through C191 forming the remainder of the Pi-network. The output is taken from plug P102 and fed to jack J1 on the directional coupler shield. The directional coupler consists of identical forward and reflected power rectifier circuits.

TABLE 4-3. BANDSWITCHING FUNCTIONS OF S104 IN POWER AMPLIFIER PLATE TANK

SWITCH POSITION	BAND (MC)	FUNCTIONS OF SWITCH	
		TUNING COILS CONNECTED	TUNING CAPACITORS CONNECTED
1	2-3	L123, L124, L125 and L126	C135 and C136
2	3-4	L123, L124, L125, and part of L126	C135 and C136
3	4-6	L123, L124, L125, and part of L126	C135 and C136
4	6-8	L123, L124, and L125	C135 and C136
5	8-12	L123, L124, and part of L125	C136
6	12-16	L123, L124, and part of L125	C136
7	16-24	L123, and L124	C136B only
8	24-30	L123	C136B only

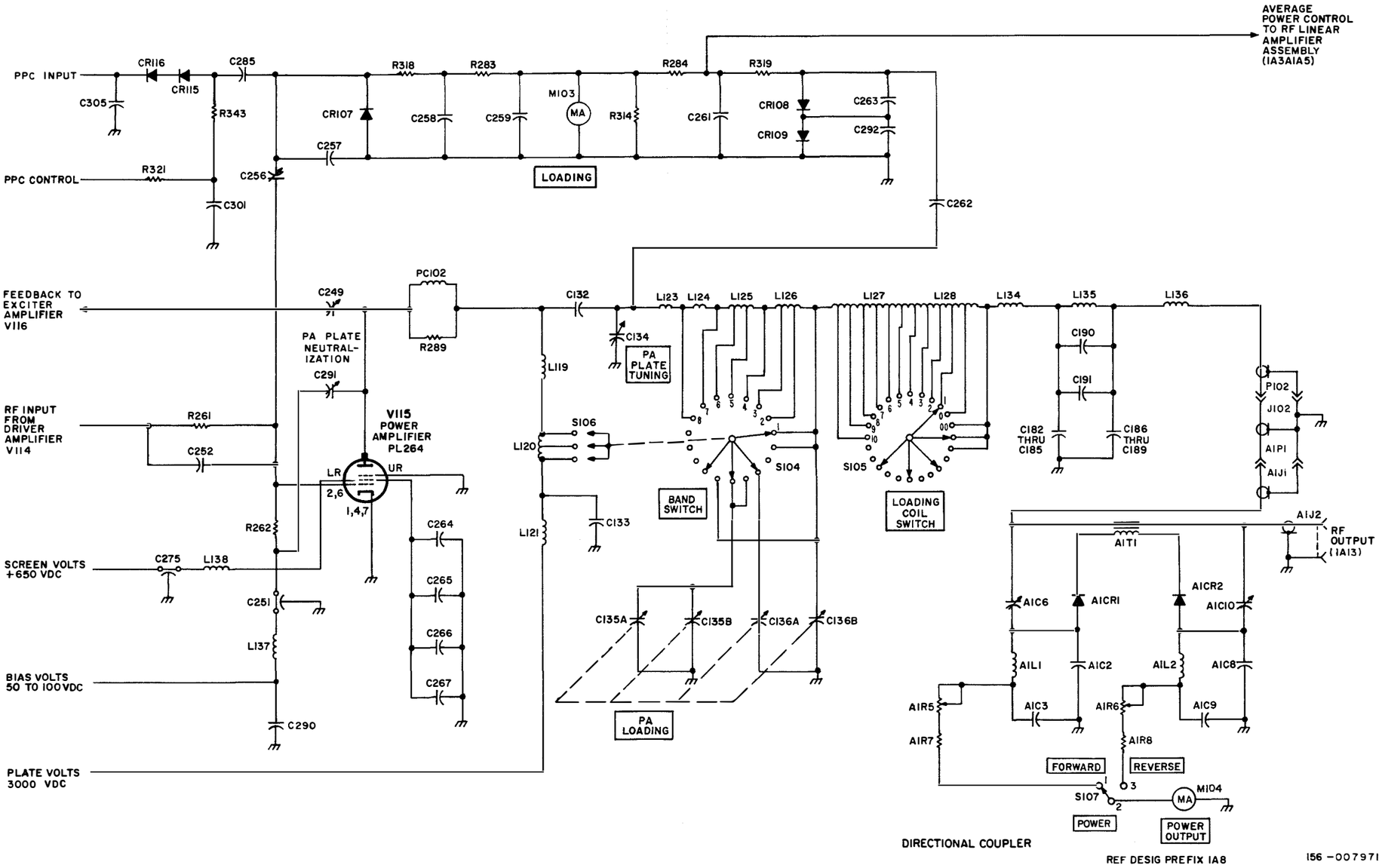


Figure 4-32. RF Assembly 1A8, Power Amplifier, Simplified Schematic Diagram

Both rectifier circuit inputs are connected to toroid transformer A1T1 and their outputs are connected to the POWER FORWARD-REVERSE switch. Jack A1J1 is connected to jack A1J2 on the directional coupler shield by a piece of No. 12 gauge wire. From A1J2 the output is coupled through 52-ohm coaxial cable to Transmission Line Coupler CU-390/FRT-24 or directly to a 50-ohm antenna. The No. 12 gauge wire traverses through the center of toroid transformer A1T1 and provides the necessary inductance so that toroid transformer A1T1 can sense the current across the output line. Capacitors A1C6 and A1 C10 are part of individual voltage divider circuits and are connected to the output line for voltage sensing. Potentiometers A1R5 and A1R6 are used to calibrate the POWER OUTPUT meter. The rectified outputs are switched to the POWER OUT PUT meter by the POWER FORWARD-REVERSE switch for monitoring and determining the SWR ratio.

The power amplifier is protected against overload by relay K102. When tube plate current exceeds a certain level, the relay is activated, thus disabling the amplifier. Resistor R150 sets the sensitivity of the relay and capacitor C138 prevents chatter. The PA CATHODE meter M105 monitors the power amplifier cathode current. The screen voltage (+630 volts) is supplied through LV-TUNE OPERATE switch S242A, and RF choke L138. When this switch is in the LV position for purposes of tuning and trouble-shooting, the screen voltage is disabled. In the TUNE position, contacts of this switch allow the high-voltage circuit to be energized while the screen grid voltage is dropped. This limits the plate current of V115 to a safe value in tuning procedure. In the OPERATE position, contacts of this switch energize the high-voltage circuit and the full screen voltage is applied.

(6) POWER AMPLIFIER 1A8V115, TEST DATA. — Information which will be helpful in determining the overall operation of the power amplifier is listed below. Refer to figure 4-83 for the circuit location and figures 5-124 and 5-125 for the physical location of test points. The test equipment required is a VTVM, (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Check front panel MULTIMETER reading with multimeter switch 1A8S108 in PA GRID MA X 20, PA SCREEN MA X 100, PA SCREEN V X 1000, PA BIAS V X 20, and PA FIL V X 10 positions. Refer to table 3-11 for typical meter readings.

(b) Refer to figure 5-207 for voltage and resistance measurements.

(c) Refer to paragraph 5-6 for general information and paragraph 5-6h for specific alignment procedure of 1A8C291.

(d) Critical adjustment.

(e) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

(7) VOLTAGE REGULATOR 1A8V108 THROUGH 1A8V112, CIRCUIT DESCRIPTION. — The voltage-regulator (see figure 4-33) consists of series regulators V110, V111, and V112, connected in parallel. They divide the +300-volt regulated current into three equal paths (to eliminate a bulky single tube), and a source of reference voltage made up of two cold-cathode type reference tubes (V108 and V109). This circuit supplies regualted +300 volts to the screen-grid and plate circuits of amplifier V116 and RF driver V114.

The +600 volts fed to the plates of the voltage regulator (V110, V111, and V112) is dropped to approximately 300 volts by load resistors R155 and R156 and the bucking voltage of the -150-volt supply. The sum of the voltage drops between the +600-volt input and the -150 volts from the bias supply produces a negative signal on the control grids. This signal will vary in accordance with power-input (+600 volts) fluctuations by a certain amount above or below the mean voltage of +300 volts established by reference tubes V108 and V109, which are connected in a voltage-divider circuit. The plate currents through the voltage-regulator tubes will change causing these tubes to act as automatic variable resistors to maintain a constant output of +300 volts. This control voltage at the junction of R124 and R154 becomes less negative as the +600-volt input rises, becuase the voltage drop across V108 and V109 remains constant. When the regulator grids become less negative, the plate current increases. The voltage drop across resistors R155 and R156 is therefore increased, so that the regulator reference voltage is reduced to the proper value. Consequently, if the regulator reference decreases, the control voltage to the grids of V110, V111, and V112 becomes more negative, the plate current decreases, and the plate voltage rises to its former value. Voltage-dropping resistor R123, connected in series with V108 and V109, drops the reference voltage slightly to impress the correct bias on the grids of the tubes. However, the voltage drop across this resistor does not change substantially with voltage variations, because V108 and V109 are connected in series with R124, a resistor of much higher value than R123; therefore voltage variations between the negative voltage source and the regulated 300-volt output will appear for the most part across R124 and consequently R154. The resistors in the control-grid and screen-grid circuits of V110, V111, and V112 prevent oscillations at audio fre-

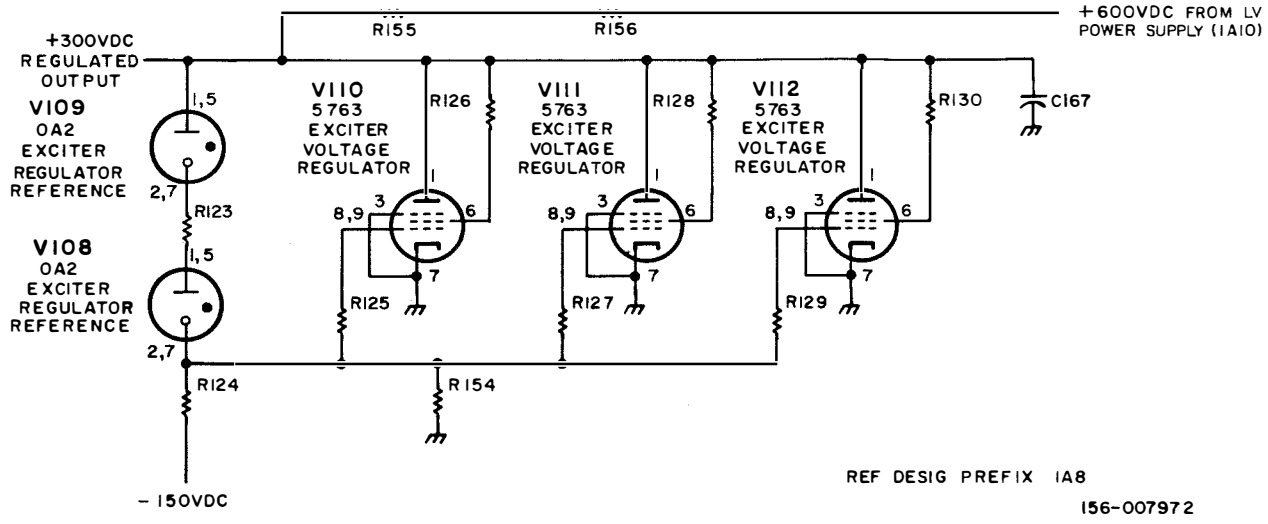


Figure 4-33. RF Assembly 1A8, Voltage Regulator, Simplified Schematic Diagram

quencies or higher. Capacitor C167 is a bypass capacitor for shunting audio and RF currents around the voltage regulator.

(8) VOLTAGE REGULATOR 1A8V108 THROUGH 1A8V112, TEST DATA. — Information which will be helpful in determining the operation of the voltage regulator is listed below. Refer to figure 4-83 for the circuit location and figures 5-127 and 5-128 for the physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Check front panel MULTIMETER reading with multimeter switch 1A8S108 in 1st AMPL V X 1000 position. Refer to table 3-11 for typical meter readings.

(b) Refer to figure 5-207 for voltage and resistance measurements.

(9) RF BIAS SUPPLY 1A8V113, CIRCUIT DESCRIPTION. — The RF bias supply (see figure 4-34), consisting of full-wave rectifier V113, receives 115-VAC and supplies -50-VDC bias voltage to RF driver V114 and -90-VDC to power amplifier V115. Refer to NAVSHIPS 900,000.102 for a description of a full-wave rectifier.

(10) RF BIAS SUPPLY 1A8V113, TEST DATA. — Information which will be helpful in determining the overall operation of the RF bias supply is listed below. Refer to figure 4-83 for the circuit location and figure 5-127 for the physical location of test points. The test equipment required is a VTVM, (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(a) Check front panel MULTIMETER reading with multimeter switch 1A8S108 in DR BIAS V X 200 and PA BIAS V X 200 positions. Refer to table 3-11 for typical meter readings.

(b) Refer to figure 5-207 for voltage and resistance measurements.

(11) AUTOTUNE SYSTEM 1A8, CIRCUIT DESCRIPTION. — The operating frequency within the 2- to 30-MC range for Radio Transmitter T-973/FRT-24A is determined by the position of the CHANNEL SELECTOR switch and the following controls: BAND SWITCH, EXCITER TUNING, DRIVER PLATE TUNING, P.A. PLATE TUNING, P.A. PLATE LOADING, LOADING COIL SWITCH. These tuning controls and switches can be automatically set to exact, predetermined positions by the autotune system. The autotune system can be controlled locally at the transmitter or from a remote station using Transmitter Control C-6466/FRT-24A. Refer to paragraph 4-6c(2) of this section for a circuit description

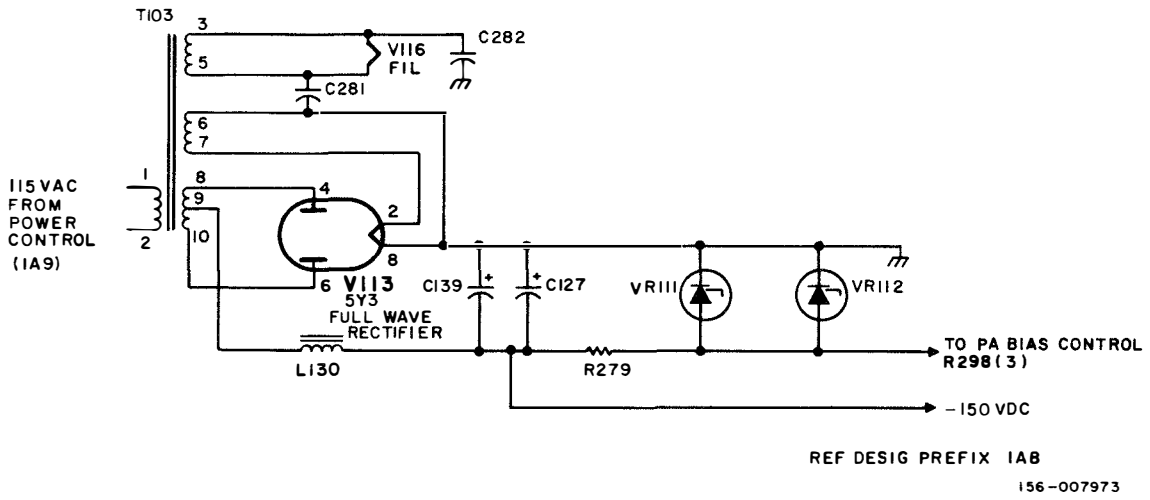


Figure 4-34. RF Assembly 1A8, RF Bias Supply, Simplified Schematic Diagram

of the autotune using a dial-type remote control system. The basic autotune system shown in figure 5-130 consists of six single-turn positioning heads, a 10-position control head, and a two-phase AC motor with associated chain drives and gearing to rotate the control and positioning heads. The electrical circuit for positioning the autotune-driven elements by controlling the operation of motor B240 consists of the control-head circuitry, CHANNEL SELECTOR switch S243, motor-starting relay K240, and motor-reversing relay K241. The six front-panel controls are each connected to a single-turn head.

(a) SINGLE-TURN HEADS. - Single-turn heads O-290 and O-288 position bandswitches S103, S104, S106, and S109 and the L-network shorting switch (S105), respectively; single-turn heads O-237, O-286, and O-289 position the tuning capacitors for the exciter, driver, and power-amplifier plate tanks, respectively; and single-turn head O-285 positions the pi-network loading capacitors. All single-turn heads are identical except for a slight modification of O-286 and O-287; these two rotate their associated shafts through 180 degrees instead of 330 degrees. The single-turn heads can be preset to operate the previously mentioned switches and capacitors for 10 different frequency settings. For manual tuning or presetting, the thumb screws on the control knobs are loosened. The autotune system must not be operated while the thumbscrews are loose or all the channel settings may be lost. All locking keys must be secured before operating the transmitter. In order to position the single-turn heads, autotune motor B240 drives them through chain belts and gears in the counter-clockwise direction preparatory to the final adjustment, which occurs when the motor reverses rotation. (The counterclockwise direction will be known as the first direction, and the clockwise direction, as the second direction, throughout the following discussion.) Figure 4-35 is a simplified diagram of a typical single-turn head; it is not an exact mechanical representation, but is adequate for purposes of explanation. Figure 5-31 is an exploded view of a single-turn head.

The portion of single-turn shaft 4 extending from the back of the single-turn head is coupled to the circuit element (such as wafer switch or variable capacitor) being controlled, while the portion of the shaft extending from the front of the unit is attached to a knob used for manual tuning and channel setting. Autotune motor B240 drives worm gear 1 in the first direction so that gear 2 rotates in the direction indicated by the solid arrow in figure 4-35. Gears 2 and 3 are fastened together, and rotation of gear 2 causes rotation of cam drum 7 through gears

3, 5, and 6 and ratchet drive 8. A clutch action exists between shaft 4 and gear 2 (and 3). Stop-ring drum 9 rotates in the first direction until rotation step 10 halts the shaft rotation, and the clutch slips keeping the stop-ring drum stationary. This action insures that the stop-ring drum always starts from the home-stop (0-degree) position in preparation for its clockwise or second direction of rotation. Cam drum 7 continues to rotate until the autotune motor reverses direction.

Cam drum 7 is composed of 10 slotted rings, the slots of which are evenly spaced around the drum so that each slot corresponds to a position of seeking switch S251 in the autotune control head circuits; ring 1 is synchronized with the first position of S251, etc. Pawl stack 11 is composed of 10 pawls, each of which has a heel and a toe. The pawl heels ride on their corresponding cam-drum rings, which keep the pawl toes in a back position, and do not allow them to fall into the slots on stop-ring drum 9. The pawl heels are tapered, so that when the cam drum rotates in the first direction, the heels fall part way into their respective slots, but ride out of the slots as the drum continues to rotate. In the first direction, if a pawl toe falls into its slot, on the stop-ring drum, the cam drum rotation will cause the pawl heel to ride out of the cam-drum slot, thus raising the heel and disengaging the toe from the stop-ring. At the beginning of the autotune cycle, one of the pawl toes is engaged in its respective stop ring, so that during the first direction of autotune operation, the stop ring becomes disengaged, or cleared in preparation for the second-direction cycle. The position of S251 in the autotune control circuit, when it causes autotune motor B240 to reverse direction, determines which cam-drum ring is positioned so that its slot is directly beneath its respective pawl heel.

Note

The rotation of the cam drum is identical with that of S251. The cam drum rotates continuously in the first direction only, in a manner similar to that of S251. When B240 reverses, to rotate in the second direction, the cam drum remains stationary, because ratchet drive 8 in this direction turns without coupling to the cam drum.

Shaft 4 can rotate in the second direction, until rotation stop 10 is engaged, which limits the rotation of shaft 4 and stop-ring drum 9 to 180 or 330 degrees (depending upon the type head being used). The position of rotation stop 10, as adjusted during manufacture, determines the number of degrees of shaft travel. This means that when the stop-ring drum is rotated, a portion of its circumference will pass the pawl toes. The stop rings are preadjusted so that during rotation all of the stop-ring slots pass beneath the toes. When a stop-ring slot moves under the pawl toe which has been released by its corresponding pawl heel, the toe will fall into the slot, and the stop-ring drum and shaft 4 will be held stationary. Because the shaft of the circuit element being controlled is mechanically linked to shaft 4, it will be positioned according to the stop-ring slot which has engaged its pawl toe. Autotune motor B240 will continue to rotate (in the second direction), but the clutch will slip, and shaft 4 will not be moved.

For the initial channel-frequency setting, a thumbscrew on the control knob is loosened about two turns, to allow a stop ring engaged to a pawl to slip on shaft 4. The other nine stop rings, not retained by their pawls, maintain their relative position to each other and the shaft, so that when the circuit-element knob is rotated (manually), these stop rings, the shaft, and the circuit element are rotated. The engaged stop ring is held stationary, and the setting at which the control knob is positioned becomes the new band setting for that stop ring. When the thumbscrew is tightened, all stop rings are fastened securely to each other and the shaft. Whenever this particular dial setting is again required, the CHANNEL SELECTOR switch is operated to the channel number corresponding to the ring on the cam drum. The autotune motor starts and brings the cam drum into the proper position, so that the pawl is over the corresponding slot in the cam drum. The remaining pawl heels contact the smooth portion of the cam drum. When the autotune control system causes the motor to reverse, the cam drum remains stationary, because of the action of ratchet 8, and the stop-ring drum rotates until the toe of the pawl falls into a corresponding slot in the stop-ring drum. When this occurs, the pawl grabs and holds shaft 4 stationary and thereby establishes a new capacitor bandswitch setting for the associated transmitter circuit. The slip clutch takes up the mechanical motion from the motor, permitting gears 3 and 4 to turn without changing the position of the shaft, until the motor is turned off by the autotune control circuit.

Note

If the thumbscrew on any control knob is not secured before autotune cycling, one of the pawl toes may fall into a stop ring as the pawl heel passes over its cam-drum slot. If that particular channel has been preset, the setting will be changed as the ring is rotated out of position.

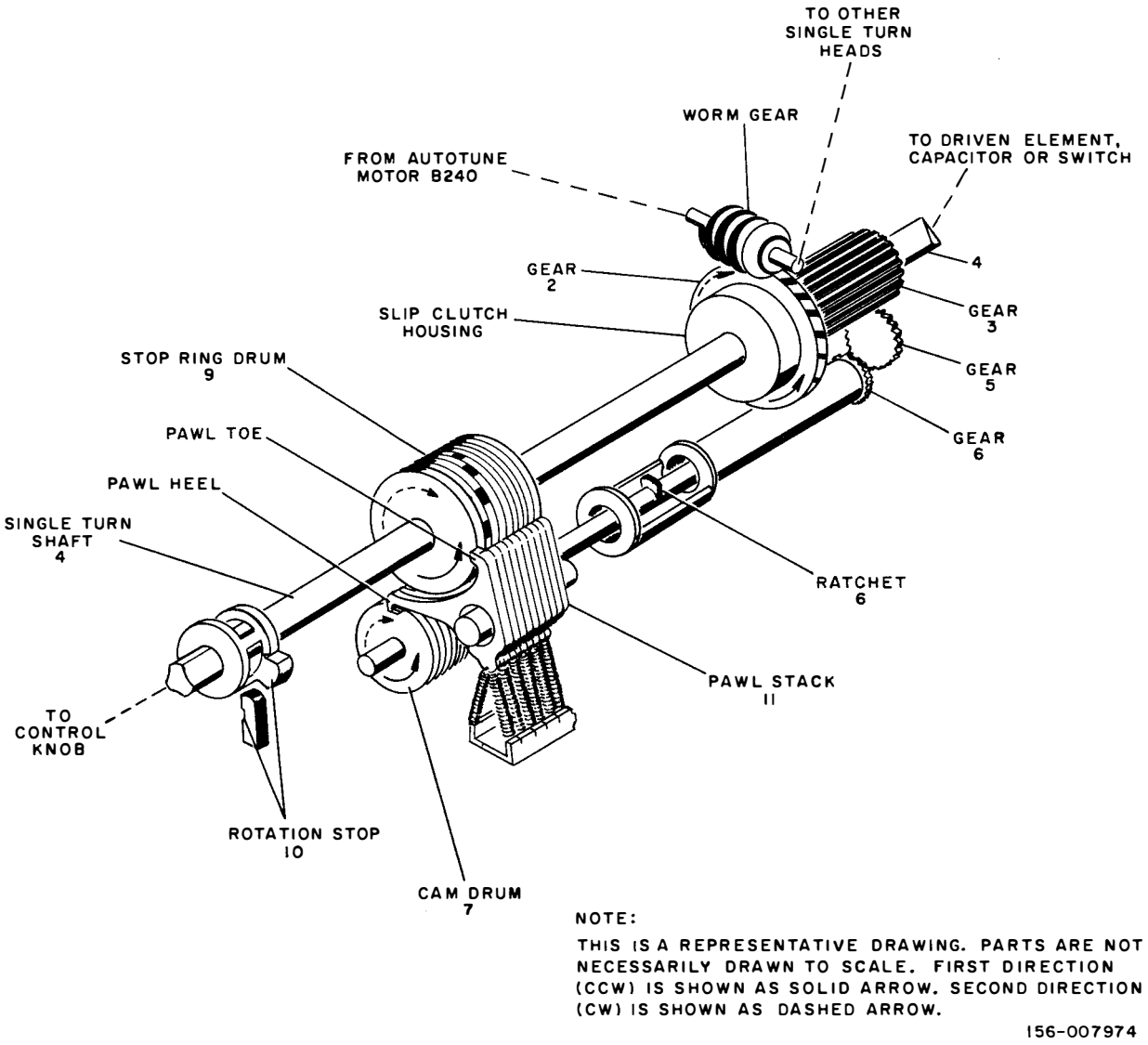


Figure 4-35. RF Assembly 1A8, Autotune System, Single-turn Head, Mechanical Diagram

(b) AUTOTUNE ELECTRICAL SYSTEM. - The autotune electrical system can be controlled locally or from a remote station, to properly position the control head and the six single-turn heads. These heads are initially adjusted to provide 10 frequency settings, each of which corresponds to one of the 10 positions on CHANNEL SELECTOR switch S243. The autotune electrical system performs a complete cycle of operation each time that the autotune cycle is initiated, regardless of the frequency channel selected. The following discussion covers only the local operation of the autotune system. For operation of the system from a remote station using a dial-type assembly in conjunction with the dial control located in the transmitter, refer to paragraph 4-6c(2) of this section. Although the control circuit for initiating autotune operation from a remote position is more complex, the autotune system proper functions in the same manner as in local operation. A schematic diagram of the autotune electrical system is shown in figure 4-36, and two block diagrams showing the entire autotune cycle for local operation are shown in figures 4-37 and 4-38. Control head O-284, together with its associated switches, is the heart of the autotune electrical system in that it controls the operation and direction of rotation of autotune motor B240 by energizing and deenergizing motor-starting relay K240 and motor-reversing relay K241 at the proper time and in the proper sequence. The electrical circuit of the control head is shown enclosed in dashed lines in figure 4-39. The sequence of operation of the electrical system is as follows:

(1) STARTING AUTOTUNE SYSTEM. When LOCAL-REMOTE switch S504 is placed in the LOCAL position, the autotune system is readied for operation by the completion of the circuit between ground and the rotor of CHANNEL SELECTOR switch S243; momentary-start contact (11) of this switch is connected to the winding of motor-starting relay K240. When S243 is turned to a new channel, the blades of the grounded rotor touch the momentary-start contact (in the new position, this contact lies between one of the slots), and K240 is energized. Contacts (2) of this relay close and supply a holding circuit to ground through the normally closed contacts (2) of motor-reversing relay K241. The normally-closed contacts (1) of K240 open the high-voltage disabling circuit (paragraph 4-6d (1)(c), of this section), so that transmitter operation is suspended during autotune cycling. The connection to the dial disabling circuit on contacts (2) is made only when the LOCAL-REMOTE switch is in the REMOTE position, so that channel selection by another remote station is suspended during autotune cycling. Contacts (3) close and connect the coil of K241 to reverse-interlock switch S253, in preparation for the motor-reversing operation (second direction). Contacts (4) close and complete the 115-VAC input to autotune motor B240. The motor then begins to run in a counterclockwise direction, driving the six single-turn heads and the control head.

(2) CONTROL-HEAD OPERATION. - A simplified diagram of the control head is shown in figure 4-39. Before the motor begins to run, actuator lever 1 is pressed against actuator 2, so that the contacting bar of limit switch S254 is touching contacts (B). As soon as the motor begins to run, as described in the previous paragraph, worm drive 3 and worm gear 4 move control-head shaft 5 and seeking switch S251 (auto-emission selector switch is used only in remote autotune operation with a dial-type unit; refer to paragraph 4-6c(2) of this section) through ratchet drive 6 for one complete revolution before the lost-motion coupler is engaged. This is done in order to insure that the locating drums and shafts of the single-turn heads are all in the home-stop (0-degree) position.

When lost-motion coupler 7 is engaged, worm gear 4 drives actuating lever 1 by means of slip clutch 8. As soon as the lever pressure is removed, the shorting bar S254 touches contacts (a) (because of a spring-return mechanism within the switch). Contacts (A) provide an alternate ground to the coil of K240, in readiness for the breaking of the holding circuit by the opening of contacts (2) of K240 at the time relay K240 is energized. The motor continues to drive in the first direction, moving the lever until it actuates switch S253. Contacts (A) of S253 are now connected together by the contacting bar inside the switch, readying the motor-reversing relay (K241); this relay will be energized as soon as seeking switch S251 and cam switch S252 are in the correct position. In the meantime, the friction clutch slips, keeping the lever against the spring-loaded mechanism of S253 , as well as rotating the shaft with its associated switches S250, S251, and S252. This rotation continues until the wiper contact of S251 reaches the grounded stationary contact (which corresponds to the new channel). This ground is carried through the closed contacts of S252, S253, and K240 to the other side of the coil relay K240, which then becomes energized.

Note

Cam switch S252 is synchronized with S251 so that its contacts close only in the exact center of each channel contact on S251. This ensures precision control of the channel drums in the single-turn heads, which in turn are synchronized with the rotation and position of seeking switch S251.

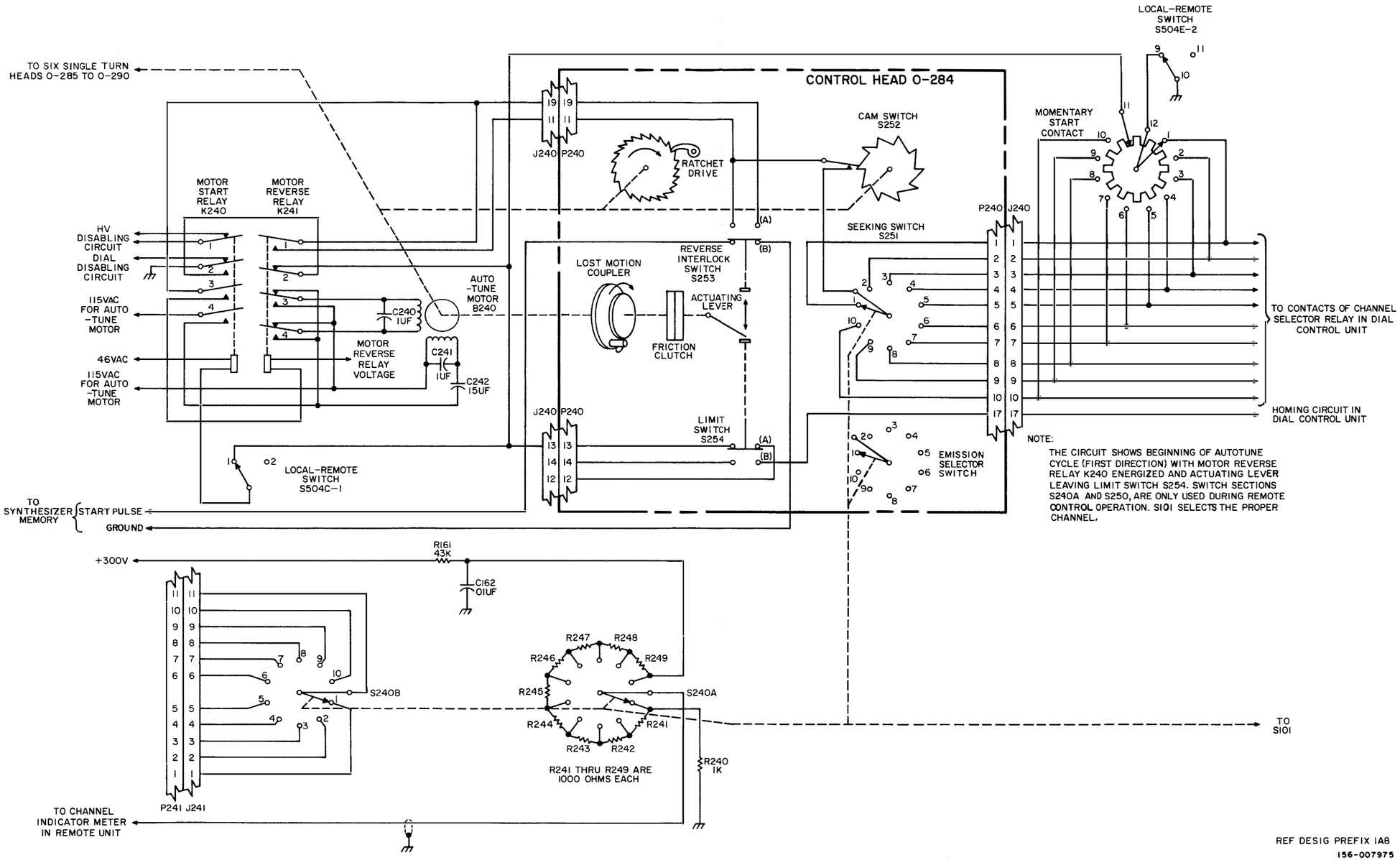


Figure 4-36. RF Assembly 1A8, Autotune System, Simplified Schematic Diagram

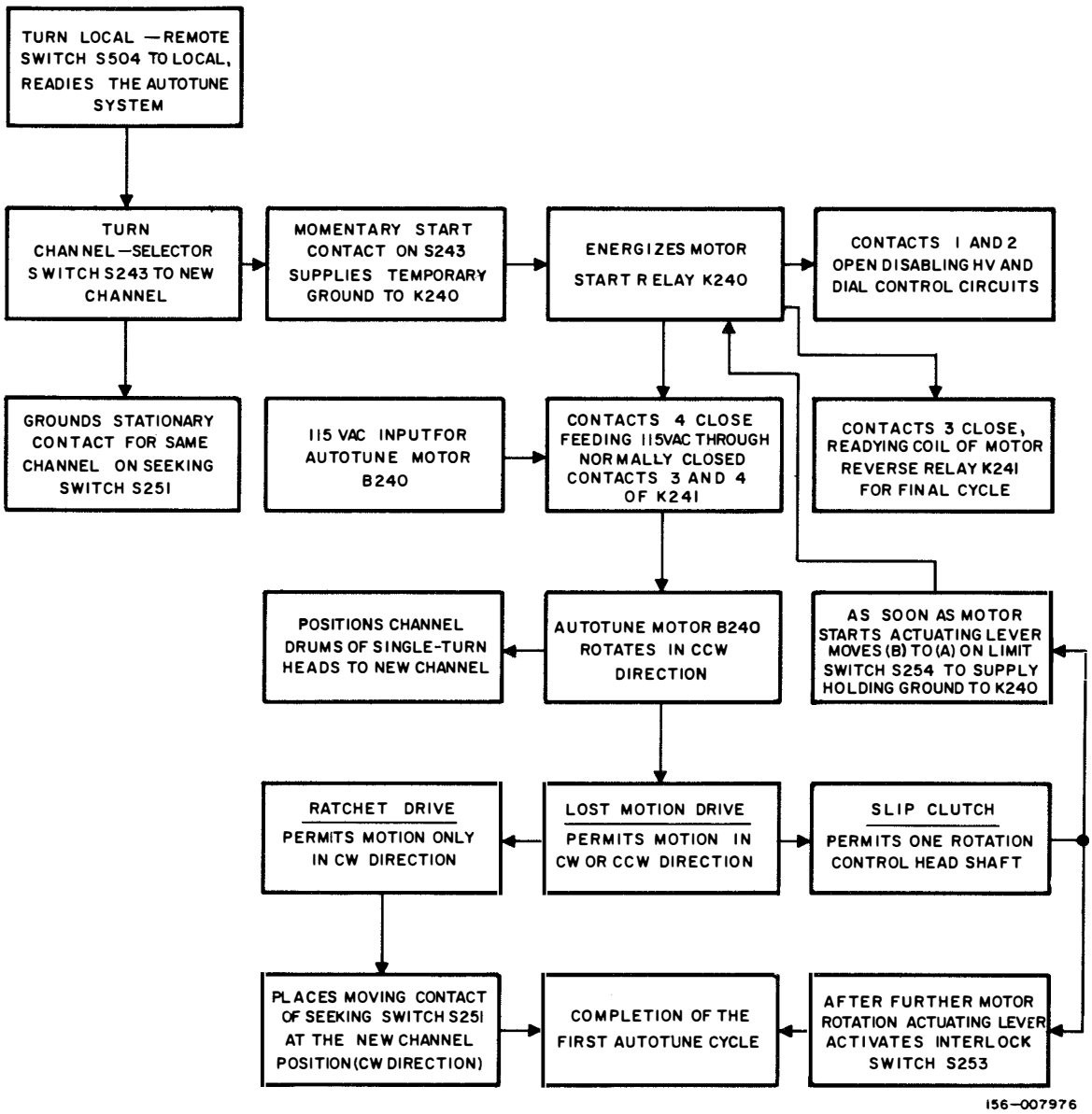


Figure 4-37. RF Assembly 1A8, Autotune System, Sequence of Operation for First Direction, Block Diagram

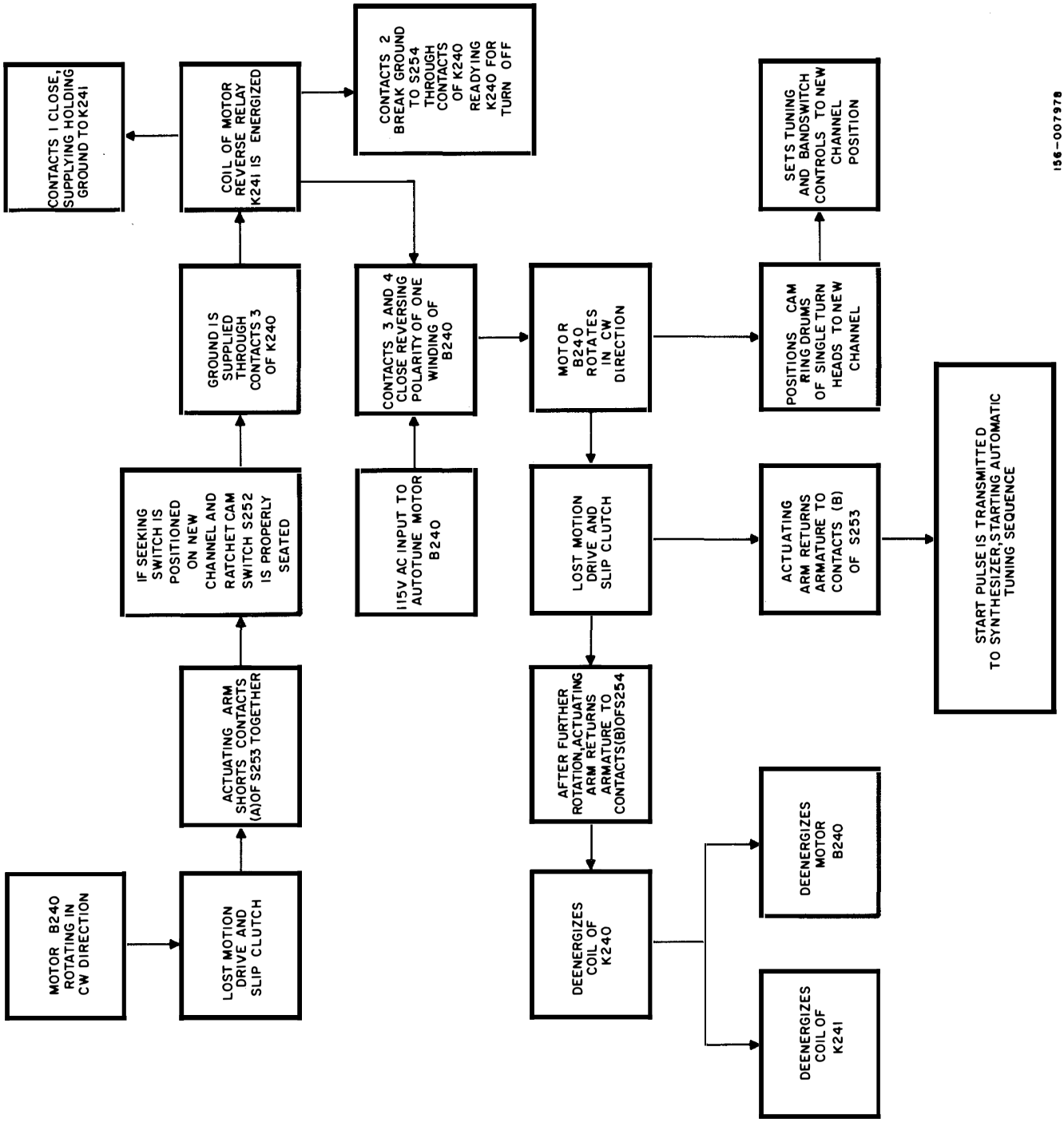


Figure 4-38. RF Assembly 1A8, Autotune System, Sequence of Operation for Second Direction, Block Diagram

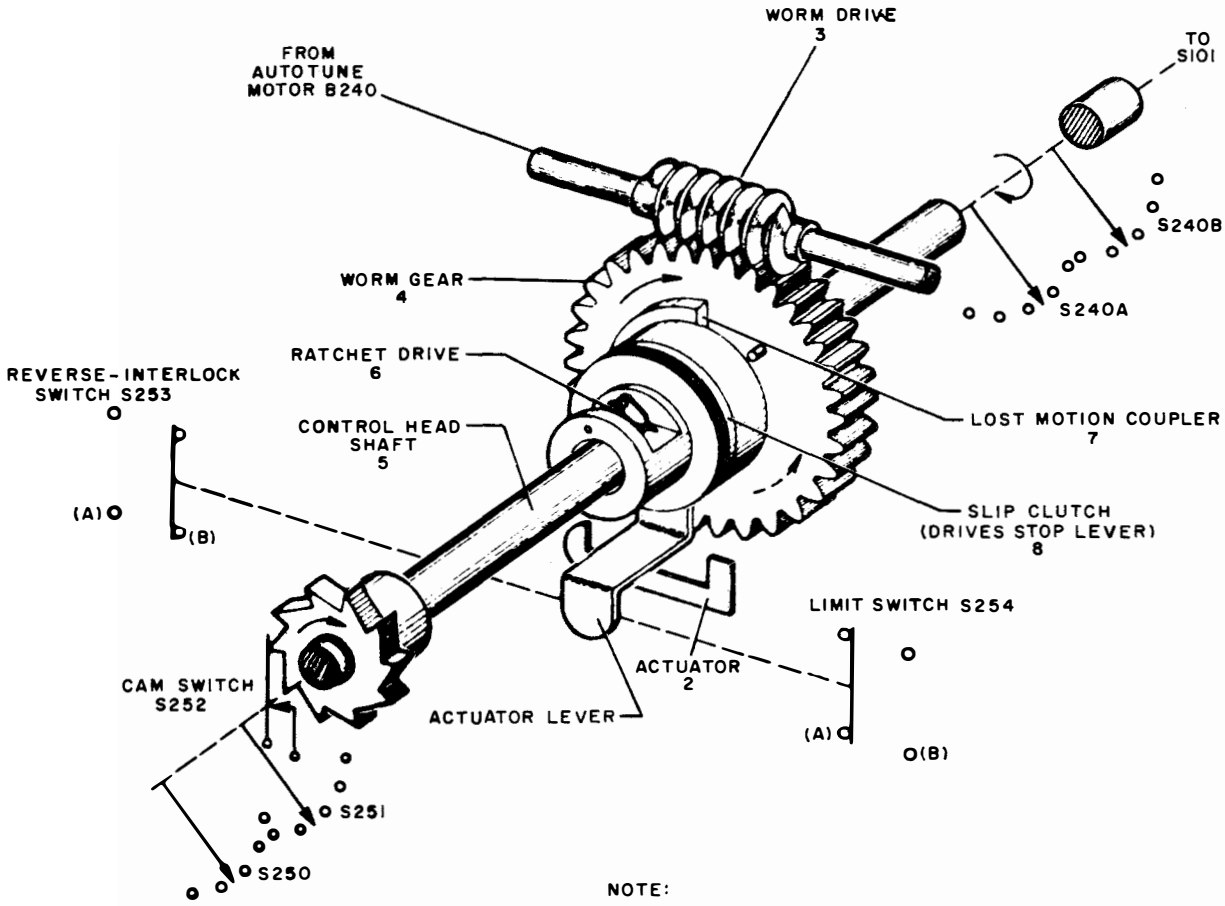


Figure 4-39. RF Assembly 1A8, Autotune System, Control Head, Mechanical Diagram

(3) COMPLETION OF AUTOTUNE CYCLE. - When motor-reversing relay K241 is energized, contacts (1) close, supplying an additional ground for holding purposes so that the relay will remain energized as soon as motor B240 reverses direction and opens S253. Contacts (3) and (4), in closing, reverse one phase of the 115-VAC input to the motor so that the motor will reverse its direction of rotation. Contacts (2) open, leaving limit switch S254, as the only remaining ground to motor-starting relay K240. Operation of S254 at the end of the autotune cycle will stop motor B240. When the motor rotates in a clockwise (second) direction, the worm drive begins to drive the worm gear in a counterclockwise direction. The ratchet drive prevents the control-head shaft from rotating in this direction, and the lost-motion coupler moves one complete turn before it begins to drive the lever back to its original position.

Note

Not only S251 but also switches S240 and S250 maintain the same position since they are all mounted in common on the control-head shaft. S240 and S250 are used only for control of the transmitter function with a dial-type unit, as discussed in paragraph 4-6b(11)(c) of this section.

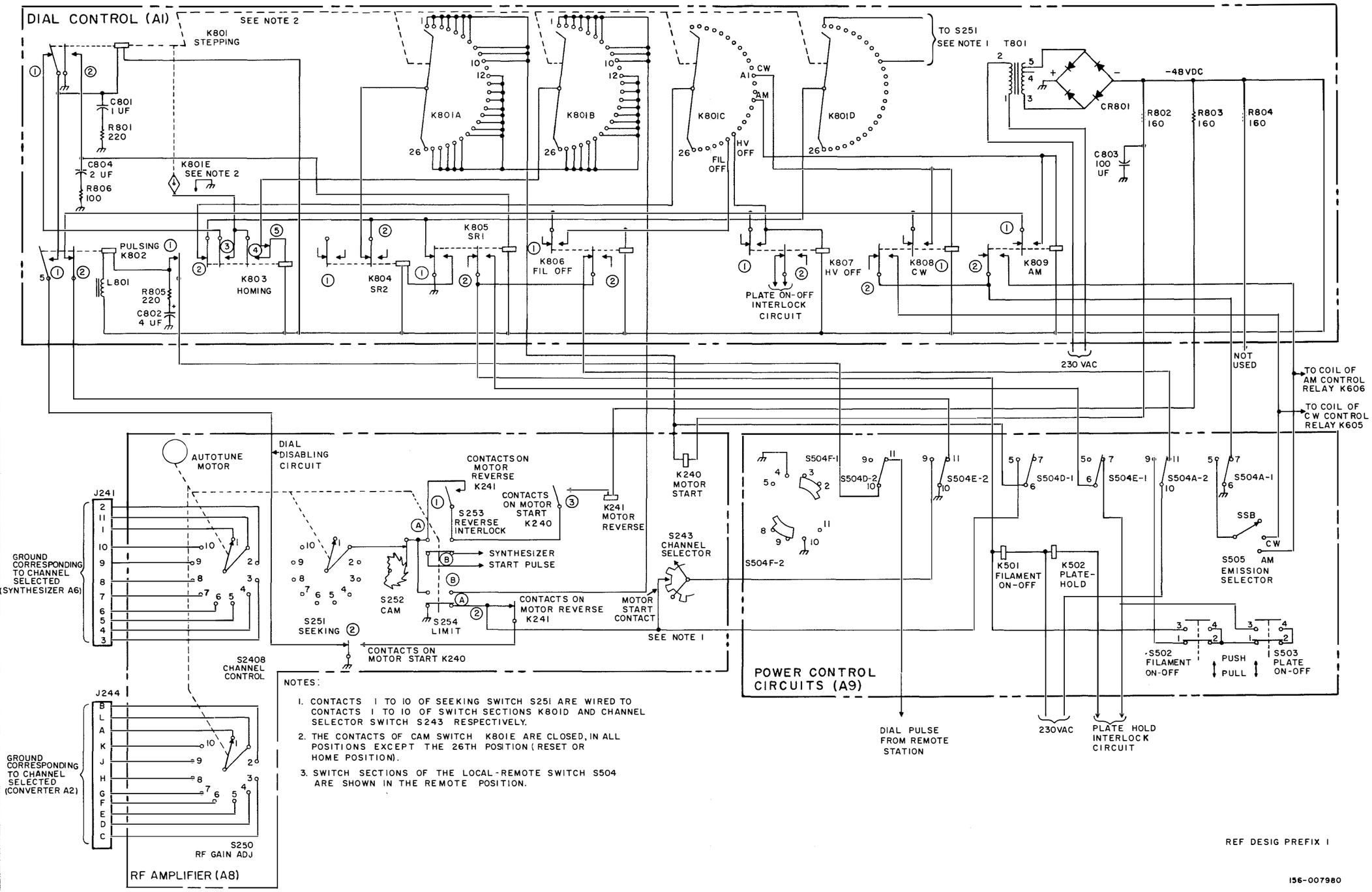
During this interval the locating drums of all the single-turn heads have sufficient time to start from their home or zero-degree position and rotate, if necessary, through their full range (180 or 330 degrees depending upon their design). Therefore, the circuit elements are properly positioned by the time the lost-motion coupler begins to drive the lever through the friction clutch. As soon as the lever position is changed, the contacting bar of S253 is returned to (B) starting the tuning sequence of synthesizer 1A6, keeping relay K240 energized by only the holding circuit of contacts (1). When the lever reaches limit switch S254, the contacting bar of this switch is forced over from contact (A) to (B). Relay K240 is deenergized, which in turn stops motor B240 and deenergizes relay K241. The high-voltage control circuit is complete, and the transmitter begins operation of the new channel that has been selected by the autotune system.

c. DIAL CONTROL 1A1, FUNCTIONAL SECTION DESCRIPTION. - The dial control (see figure 5-167) is used with Transmitter Control C-6466/FRT-24A for remote control operation of the transmitter. When the telephone dial is operated to turn the transmitter on or off, or to select a new frequency or a different type of emission, the proper number of ground pulses for the action desired are transmitted to the dial control, which by a sequence of events discussed below, operates the autotune system in the RF assembly, the synthesizer automatic tuning circuits, or the power control circuits to achieve the desired result. The dial control consists of a stepping-type relay, eight telephone-type relays, and a DC power supply for the relays. The LOCAL-REMOTE switch (S504) on power control 1A9 must be placed to the REMOTE position before the transmitter can be controlled from a remote station. In order to understand the operation of the dial control assembly for automatic channel selection, it is essential that the theory of operation of the autotune system, discussed in paragraph 4-6b(11), of this section be thoroughly understood. Figure 4-40 is a simplified schematic of the dial control and its associated circuits. Figures 4-41 and 4-42 are block diagrams showing the sequence of operation of the dial control during channel and power selection respectively.

(1) LOCAL-REMOTE SWITCHING. - The LOCAL-REMOTE switch (S504), located on power control 1A9 connects the dial control to the autotune and power control circuits when this switch is placed in the REMOTE position. Ground pulse information from a dial input to stepping relay K801 in conjunction with pulsing relay K802 effects the operation of relays K803 through K809 for the control of these circuits. In the LOCAL position of the switch, the same circuits are disconnected from the dial control, so that the same operation can be initiated by the transmitter front-panel controls. However, before the transmitter can be handled exclusively from a remote station, the required frequency channel should be preset and PRIMARY CIRCUIT BREAKER switch CB501 should be on. S504 is a six-deck, wafer-type switch on a common shaft. The decks are numbered alphabetically from S504A to S504F. S504A is nearest the driver or knob end, as shown in figure 4-43. All decks except S504F consist of three single-pole, double-throw switch sections, each of which is designated with the suffix 1, 2, or 3. Deck S504F consists of two double-pole, double-throw switch sections, each of which is designated with the suffix 1 or 2. Altogether, the LOCAL-REMOTE switch contains 17 switch sections; the function of each switch section for either one of its two positions is given below.

Note

For further explanation of the functions of S504 in the LOCAL position, refer to paragraphs 4-6b(11) and 4-6d of this section for local operation of the autotune system and power control circuit respectively.



NOTES:

1. CONTACTS 1 TO 10 OF SEEKING SWITCH S251 ARE WIRED TO CONTACTS 1 TO 10 OF SWITCH SECTIONS K801D AND CHANNEL SELECTOR SWITCH S243 RESPECTIVELY.
2. THE CONTACTS OF CAM SWITCH K801E ARE CLOSED, IN ALL POSITIONS EXCEPT THE 26TH POSITION (RESET OR HOME POSITION).
3. SWITCH SECTIONS OF THE LOCAL-REMOTE SWITCH S504 ARE SHOWN IN THE REMOTE POSITION.

Figure 4-40. Dial Control 1A1, Dial Control with Associated Circuits, Simplified Schematic Diagram

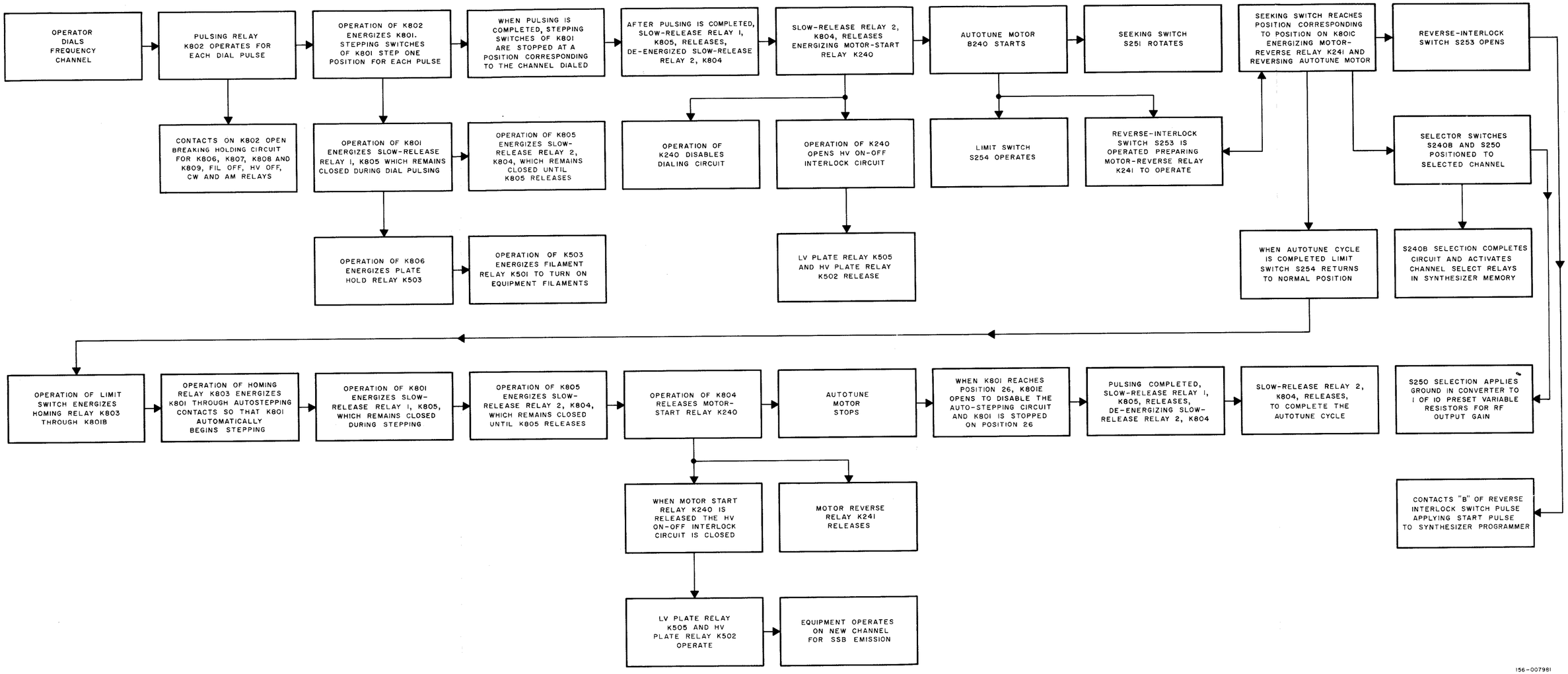


Figure 4-41. Dial Control 1A1, Sequence of Operation for Channel Selection, Block Diagram

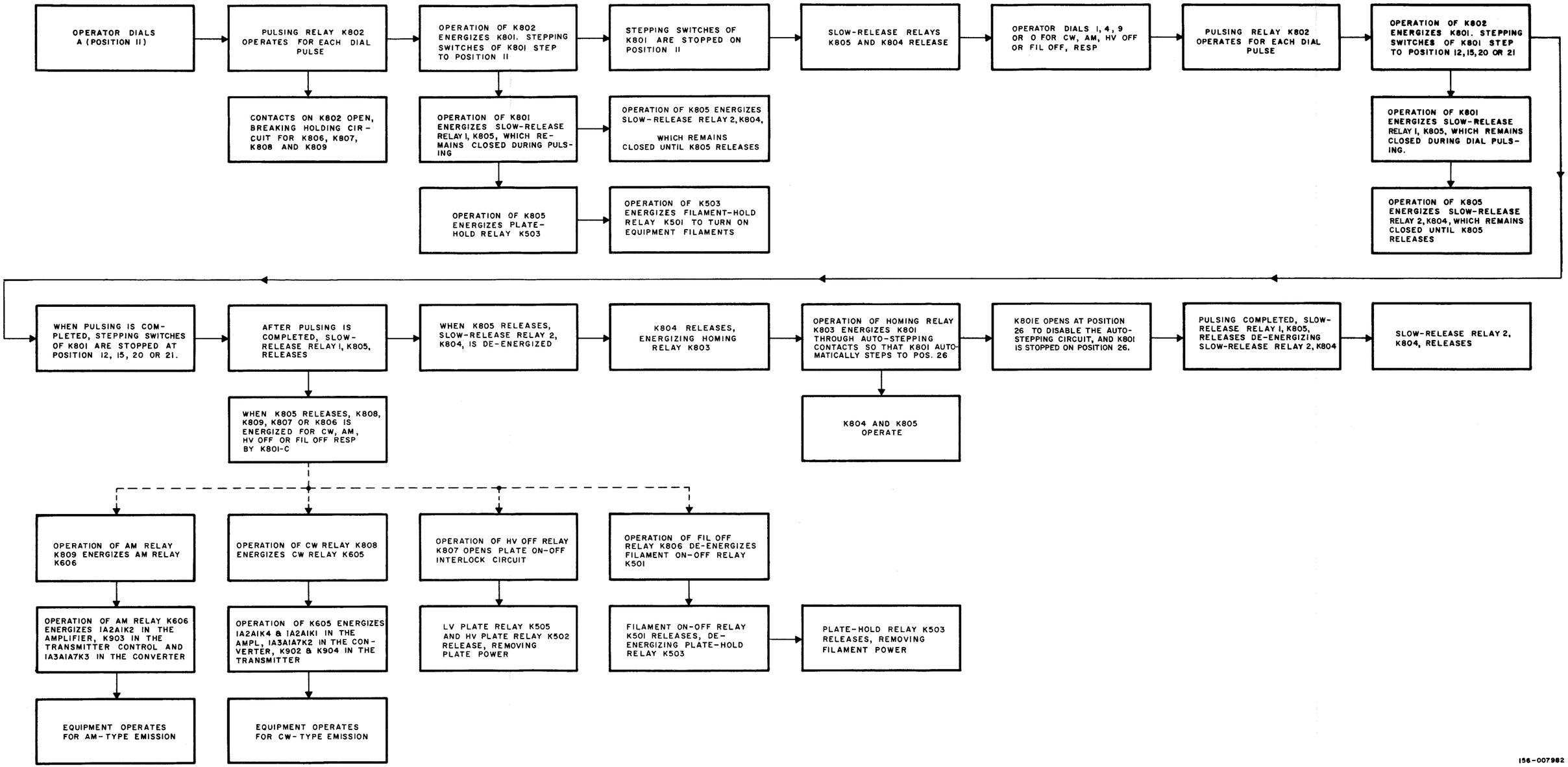


Figure 4-42. Dial Control 1A1, Sequence of Operation for Power or Emission Selection, Block Diagram

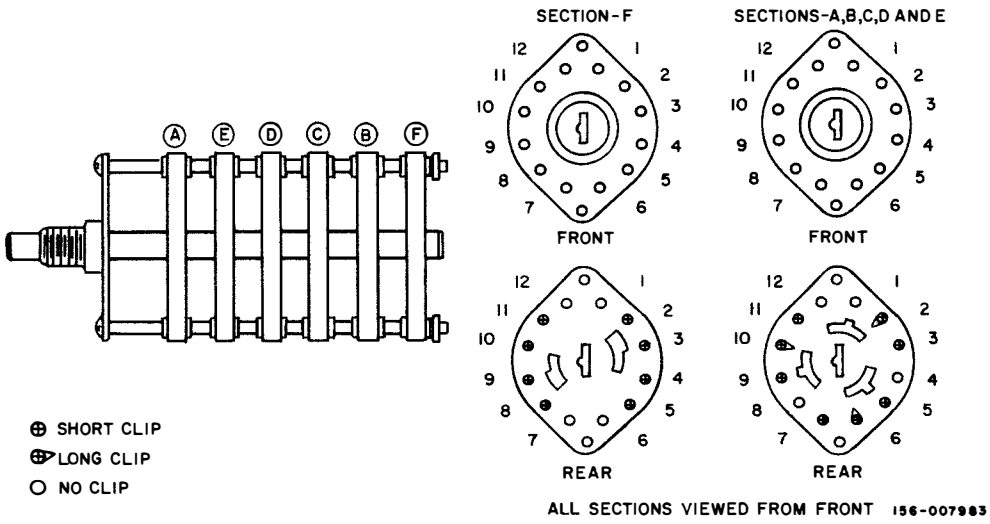


Figure 4-43. Power Control 1A9, Local-Remote Switch S504, Mechanical Diagram

S504A-1: In the LOCAL position, this section readies SSB-CW-AM switch S505 so it can be used to select different types of emission. In the REMOTE position, it breaks this circuit and introduces an alternate circuit in which CW and AM relays K808 and K809 of the dial control can select the different types of emission.

S504A-2: In the LOCAL position, this section permits FILAMENT switch S502 to energize the filament circuits. In the REMOTE position, it breaks this circuit and introduces an alternate circuit in which filament relay K806 of the dial control assembly can turn on the filament circuits.

S504E-1: In the LOCAL position, this section permits PLATE switch S503 to energize the plate circuits after a suitable time delay. In the REMOTE position, it breaks this circuit and introduces and alternate circuit in which plate delay relay K805 of the dial control assembly can turn on the low-voltage and high-voltage plate circuits after a suitable time delay.

S504E-2: In the LOCAL position, this section supplies ground to the rotor of CHANNEL SELECTOR switch S243 so that the autotune system can be cycled to a new frequency by changing the setting of this front-panel control. Also, in the LOCAL position, this switch section disables the functioning of the dial control assembly by opening the holding circuit to the relays of that unit. In the REMOTE position, it ungrounds the rotor so that the dial control assembly, when set into operation by a remote dial unit, can cycle the autotune system to a new frequency.

S504E-3: This switch section performs no function but is wired to receptacle J502 to be used as a spare.

S504D-1: In the LOCAL position, this section connects the coil of motor-starting relay K240 to the momentary start contact of S243 so that autotune motor B240 may be energized as soon as CHANNEL SELECTOR switch S243 is turned. In the REMOTE position, it disables this circuit so that only the dial control assembly can turn on the autotune system.

S504D-2: In the LOCAL position, this section disconnects the dial-pulse input from pulsing relay K802 of the dial control assembly. In the REMOTE position, this relay is reconnected to the dial input, in readiness for energization on the basis of ground-pulse information.

S504-3: This switch section performs no function but is wired to receptacle J502 to be used as a spare.

S504D-3, S504C-1, S504C-2, S504C-3: These switch sections do not perform any function in either the LOCAL or REMOTE positions.

(2) CHANNEL SELECTION. - Figure 4-41 is a block diagram of the sequence of action for obtaining a new channel by means of dial control 1A1 and associated circuits; figure 4-40 is the schematic diagram for the same circuits. For convenience, the channel-selection function of the dial control is divided into stepping, control-circuit-cycling, and homing sequences.

(a) STEPPING. - When the telephone dial on Transmitter Control C-6466/FRT-24A is operated to select a new channel, a number of ground pulses corresponding to the channel number dialed are produced by the rotation of the special switching contacts in the dial assembly. For example, 10 pulses are produced for channel 10. These pulses are fed through switch section S504D-2 to the coil of pulsing relay K802. Power for this relay and for all other relays in the dial control assembly is supplied through a bridge-type selenium-rectifier supply consisting of T801 and CR801. The positive side of this bridge circuit is grounded. A voltage of -48 VDC is therefore placed on the coil of K802 each time this relay receives a ground dial pulse, and in the example, the pulsing relay will operate its contacts for 10 distinct intervals. Contacts (1) of K802, in supplying 10 ground pulses to the coil of stepping relay K801, cause the armatures of K801A, K801B, K801C, and K801D to move to the tenth position. Contacts (2), in opening (one pulse is sufficient), break the holding circuit from ground through switch section S504E-2 to relays K806, K807, K808, and K809, which are the filament off, high-voltage off, CW and AM relays, respectively. By removing the holding circuits to these relays, these contacts stop the action of any relay which may have been energized previously; clearing this relay circuit is essential for setting up a transmitter function on the basis of new dial information. All transmitter functions are suspended except the filament circuits, which

remain or become energized. For more details on the operation of these relays in the power control circuits, refer to paragraph 4-6d(2) of this section.

(b) CONTROL CIRCUIT TURN ON. - As soon as K801 is energized (one pulse is sufficient), contacts (1), in closing, energize SR1 relay K805, which remains closed a fraction of a second after each pulse since it is of the slow-release type. Contacts (2) of K805, in closing, apply 115 VAC to plate-hold relay K503 and filament relay K501 through S504A-2, S504E-1, contacts (2) of K806, and the plate-hold interlock circuit. The radio set filament circuits are turned on. Contacts (1) of K805 energize autotune control relay (SR2), another slow-release type relay whose contacts remain open until a short time after K805 releases; this insures that the autotune motor, which is energized through K801A and motor-starting relay K240, does not start its rotation until the last ground pulse is fed to pulsing relay K802. Contacts (2) of K804 lift ground from the armatures of K801A, K801C, and K801D so that the autotune system will not cycle until the pulsing is completed. Switch section K801B is not affected at this time since it can energize homing relay K803 only after the autotune system has undergone a complete cycle (ready to return limit switch S254 to its original position, as discussed in paragraph 4-6b(11)(b)(3) of this section). As soon as K805 releases (assuming that channel 10 has been dialed, all armatures of the switch sections are now properly indexed at position 10), the armatures of K801C and K801D are returned to ground. In this position K801C does not have any effect, because its stationary contacts from positions 1 to 11 are unwired. However, stationary contacts 1 to 10 of K801D are wired in parallel with stationary contacts 1 to 10 of seeking switch S251 and CHANNEL SELECTOR switch S243. As soon as the armature of K801D is grounded, identically positioned contacts on S251 and S243 are placed at ground; this is equivalent to turning the CHANNEL SELECTOR switch to channel 10 when S504 is in the LOCAL position. As soon as relay K804 releases and grounds the armature of K801A, a ground is applied to the coil of motor-starting relay K240; this is equivalent to grounding the momentary-start contact while turning the rotor of the CHANNEL SELECTOR switch with S504 in the LOCAL position. The contacts of actuated relay K240 disable the control circuit to plate relays K502 and K505 so that plate voltage cannot be applied during autotune cycling, and disable the dial input circuits so that turning the telephone dial of any of the remote units has no effect during autotune cycling.

(c) HOMING. - When the autotune system cycles, it will set up the control head and the six single-turn heads on the new channel, as discussed in paragraph 4-6b(11)(b) of this section. When the autotune cycle has been completed, limit switch S254 is returned to its original position. Ordinarily, the autotune system is turned off at this point in LOCAL operation; however, in REMOTE operation, the system is still energized by the grounded contacts of K801A and K801D. When contacts (B) of S254 operate, they apply a ground through the first 10 stationary contacts and the armature of switch section K801B to closed contacts (5) of homing relay K803. Contacts (5) open, but ground is maintained to the coil by contacts (4) and K801E. Contacts (1) disable pulsing relay K802 so that there can be no new dial-pulse input during homing. Contacts (3) supply a ground through contacts (1) of K801, which begins automatically to step as a result of the make and break function of contacts (1) of K801. When the relay is energized, contacts (1) open, causing the relay to deenergize; contacts (1) then close, reenergizing the relay. Contacts (2) of K803 unground the armature of K801C so that during the homing process K806, K807, K808, and K809 cannot be energized as this armature is returned to its home on the 26th position. Contacts (2) of K801 supply a ground to slow-release relay K805, which in turn energizes K804. The contacts of K804, in opening, lift the ground from the armature of K801A, which in turn breaks the ground to relay K240. The contacts of K240 then deenergize the autotune electrical system, and apply 115 VAC to the control circuit to relays K502 and K505. High voltage is then applied to the transmitter circuits after a suitable time period has elapsed, allowing the transmitter to operate on the new channel setting. In the meantime, the armatures of K801 continue to step until they reach the 26th position, which is their normal position before receiving any new dial information from a remote station. Note that each armature has a wiper contact on either end so that a 26-position movement in effect returns the armature to its original place. At this time, cam switch K801E opens the ground to contacts (3) and (4) of homing relay K803 so that this relay and relay K801 are deenergized. Since contacts (2) of K801 are normally open, after a brief interval, relay K805 releases, in turn releasing K804.

(3) POWER OR EMISSION SELECTION. - At any time after the transmitter has been placed into normal operation, the dial control assembly is ready to receive pulse information not only for changing channels, as discussed previously, but also for selecting different types of emission or turning off the plate or filament voltages. When a new channel is dialed, the dial control relays will cycle and cause the transmitter to go into operation on the new frequency with SSB emission. If CW or compatible AM emission is desired, it is necessary to dial

A1 or A3, after channel selection has been made. Figure 4-42 is a block diagram of the sequence of actions that occur for power or emission selection.

(a) CONTROL-CIRCUIT RELAYS. - A detailed analysis of the power and emission control circuits is given in paragraph 4-6d of this section. A thorough understanding of these control circuits will clarify the relationship of the dial control function with transmitter operation. Three telephone-type relays are used in the dial control assembly to effect changes in the transmitter control circuits and subsequent operation. These relays are as follows:

K806, FIL OFF: The function of this relay is equivalent to that of FILAMENT switch S502, for which it is substituted during remote operation. Contacts (2) on this relay are connected in series with one side of the AC input through contacts of S504A-2 to the other side of filament relay K501. When K806 is energized, contacts (2) open and turn the transmitter filaments off; the plate voltage circuits are also disabled simultaneously.

K807, HV OFF: The function of this relay is equivalent to that of PLATE switch S503, for which it is substituted during remote operation. Contacts (2) on this relay are connected in series with the plate interlock circuit so that when K807 is energized, contacts (2) open, deenergizing plate relays K502 and K505, turning the plate voltage off.

K808, CW: The function of this relay, when energized, is equivalent to that of EMISSION SELECTOR switch S505 when the switch is set in the CW position during remote operation. When the relay is not energized the transmitter is set up for SSB operation. Contacts (2) on this relay connected in series with one side of the AC input through contacts of S504A-1 to the CW relay in the amplifier unit. When K808 is energized, contacts (2) close and actuate the CW relay so that the equipment is set up for CW operation.

K809, AM: The function of this relay, when energized, is equivalent to that of EMISSION SELECTOR switch S505 when the switch is set in the AM position during remote operation. When the relay is not energized, the transmitter is set up for SSB operation. Contacts (2) on this relay are connected in series with one side of the AC input through contacts of S504A-1 to the AM relay in the amplifier unit. When K809 is energized, contacts (2) close and actuate the AM relay so that the equipment is set up for AM operation.

(b) DIAL-CONTROL OPERATION. - The dial-control operation for power or emission selection is essentially the same as for channel selection except that the number of pulses required is greater. CW selection requires 12 pulses, AM selection requires 14 pulses, high-voltage off selection requires 20 pulses, and filament off selection requires 21 pulses to drive the armature of K801 to an equivalent position for accomplishing the required action. Dialing the letter A (11 pulses), steps K801 to position 11. Since contacts (11) on the stepping switches are blank, the armatures stop and do not function to operate the autotune system. Now, dialing the number 1, 3, 9, or 0 (1, 3, 9, or 10 pulses) steps K801 so that the ungrounded armature of K801C stops at the CW, AM, high-voltage off, or filament off position, in preparation for energizing K809, K808, K807, or K806. When the pulsing stops, SR1 relay K805 is deenergized and releases SR2 relay K804. Contacts (1) of K805 apply a ground to the arm of K801C to energize the selected relay. The contacts of K804 apply a ground to homing relay K803 through the closed circuit of K801A and K801B. K801 steps to position 26 and stops. Each relay, K806, K807, K808, and K809, is interlocked by self-holding contacts (1) so that once a relay has been energized by the stepping action of K801C, it will remain energized through the ground holding circuit consisting of its own contacts and closed contacts (2) of pulsing relay K802. The holding circuit to the relay will release only when K802 is again energized by the dial-pulse input. In the event the transmitter has been set up for CW operation by dialing A1, it can be returned to AM or SSB operation by dialing the correct sequence. Dialing the number A operates pulsing relay K802 so that contacts (1) on this relay break the holding circuit to the coil of K808. Contacts (2) of K808 then set up the transmitter for AM or SSB operation. The armatures of K801 are stopped on position 11; dialing the number 3 steps the armatures to position 14, a position which permits K803 to home K801 to position 26.

d. POWER CONTROL 1A9, FUNCTIONAL SECTION DESCRIPTION. - The power control (see figure 5-210), supplies primary power for application to the plate, filament, control, and blower circuits of Radio Set AN/FRT-24A. On the front panel are mounted 5 controls, 2 panel lights, 16 fuses, and 16 blown-fuse indicator lights. PRIMARY CIRCUIT BREAKER CB501 is the main power (230 VAC) input switch, and FILAMENT control S502 and PLATE control S503 are used to turn power on or off in the filament and plate circuits. When these spring-loaded momentary-contact switches are pulled toward the operator, the control circuit sequence will begin. FILAMENT lamp I501 will light immediately, and after a 4- to 5-minute delay, PLATE lamp I502 will go on, indicating that plate voltage is being applied.

Note

The following discussion is concerned only with application of power. The complete function of LOCAL-REMOTE switch S504 is discussed in greater detail in conjunction with the dial control (paragraph 4-6c of this section). The complete function of EMISSION-SELECTOR (SSB, CW, AM) switch S505 is discussed where applicable in the paragraphs dealing with the dial control assembly.

Circuit breaker CB501 is a magnetic type switch providing overload protection for the primary input circuits; when this switch is opened as a result of an overload, it can be reset (after a 5-second delay) by manual operation of the toggle. The three control-circuit branches, the independent bias, filament, and plate power circuits as well as the blower, autotune, and DC relay supply circuits are individually protected by cartridge fuses (mainly of the slow-blow type). Table 3-17 gives the fuse symbol, the circuit it protects, and the rating of the fuse. As an aid in trouble shooting, whenever a fuse opens because of an overload in a particular circuit, a neon -type lamp connected across the fuse will light, indicating a blown fuse. Whenever the lamps are used in circuits having voltages higher than their maximum rated voltage, a voltage-dropping resistor is used in series with the lamp to limit current (when a fuse opens) through the lamp to a safe value.

Beneath the front panel is an access door which covers five relays, four connectors time-delay tube V501, and adjustment control R523. On the bottom of the component are mounted two autotransformers, T501 and T502, for supply stepped-down AC voltages; these autotransformers are energized by the FILAMENT control. Figure 5-210 is a schematic diagram of the power control assembly. Figure 4-45 clarifies the relationship between the power control assembly and its associated circuits. Figure 4-44 is a block diagram showing the sequence of actions of the power control assembly for local operation.

(1) LOCAL OPERATION. - When PRIMARY CIRCUIT BREAKER CB501 is turned ON, 230-volt, single-phase, 50/60-CPS power is applied directly to the primary of DC relay supply transformer T801 in dial control 1A1, and to service supply autotransformer T701, which supplies 230 VAC to synthesizer power supply 1A4 and exciter power supply 1A7.

(a) FILAMENT-POWER APPLICATION. - Pulling the FILAMENT knob forward causes contacts (3 and 4) of S502 to momentarily complete the 230-volt circuit to filament relay K501 through its normally closed contacts (1) and (2) and switch section S504A-2. The controls of this relay perform the following functions:

Closed contacts (3 and 4 return the coil to closed contacts (1 and 2) of S502 so that when momentary switch S502 returns to its normal position, relay K501 will remain energized through this holding circuit.

Closed contacts (5 and 6) and (7 and 8) apply 230 VAC to terminals 1 and 7 of autotransformers T501 and T502, to blower B641, and to the primary windings of T102, T301, and T402 which are the power-amplifier, low-voltage-rectifier, and high-voltage-rectifier respectively. Upon application of voltage of these components, PRIMARY VOLTAGE meter M671, an AC type voltmeter, will indicate the amplitude of the primary voltage, and FILAMENT HOURS meter M663, a synchronous self-starting electric clock, will begin to operate the direct-reading type dial. Autotune transformer T502 (between terminals 1 and 6) applies 220 VAC to the primary winding of T101, the exciter filament transformer, and 115 VAC (between terminals 1 and 2) to the primary winding of T103, the RF bias transformer. Autotransformer T501 applies 115 VAC (between terminals 1 and 2) to energize FILAMENT indicator lamp I501. These terminals also supply 115 VAC for operation of autotune motor B240.

(b) TIME-DELAY CIRCUIT. - Terminals 6 and 7 of T501 supply 10 VAC to the cathode-heater circuit of time-delay tube V501. The plate circuit is returned to one side of the primary voltage, and the cathode circuit is returned to the other side through load resistors R522, R523, and R519 and contacts 7 and 8 of K501. Rectification of the AC voltage to be developed at the cathodes, and capacitor C501 is charged through resistor R520. The rising positive potential at C501 is fed through R521 to the control grids of V501, causing the plate current of this tube to increase. After approximately 4 to 5 minutes, the plate current becomes great enough to cause time-delay relay K504 to operate. Bringing up the tube to its required plate emission is delayed not only by the long-time-constant circuit consisting of C501 and R520, but also by the slow heating of the tube cathodes due to the fact that the heaters are operated at approximately 3 volts below their normal rating. Cathode bypass capacitor C502 filters the cathode voltage to prevent K504 from chattering with plate-current pulsations. The plate current will stabilize when the grid potential reaches the same potential as the cathode (zero bias). During the time that C501 is charging, the grid bias as measured with respect to the cathode becomes increasingly less negative. Potentiometer R523 is used in adjusting the time-delay circuit so that K504 will actuate after a 30-second

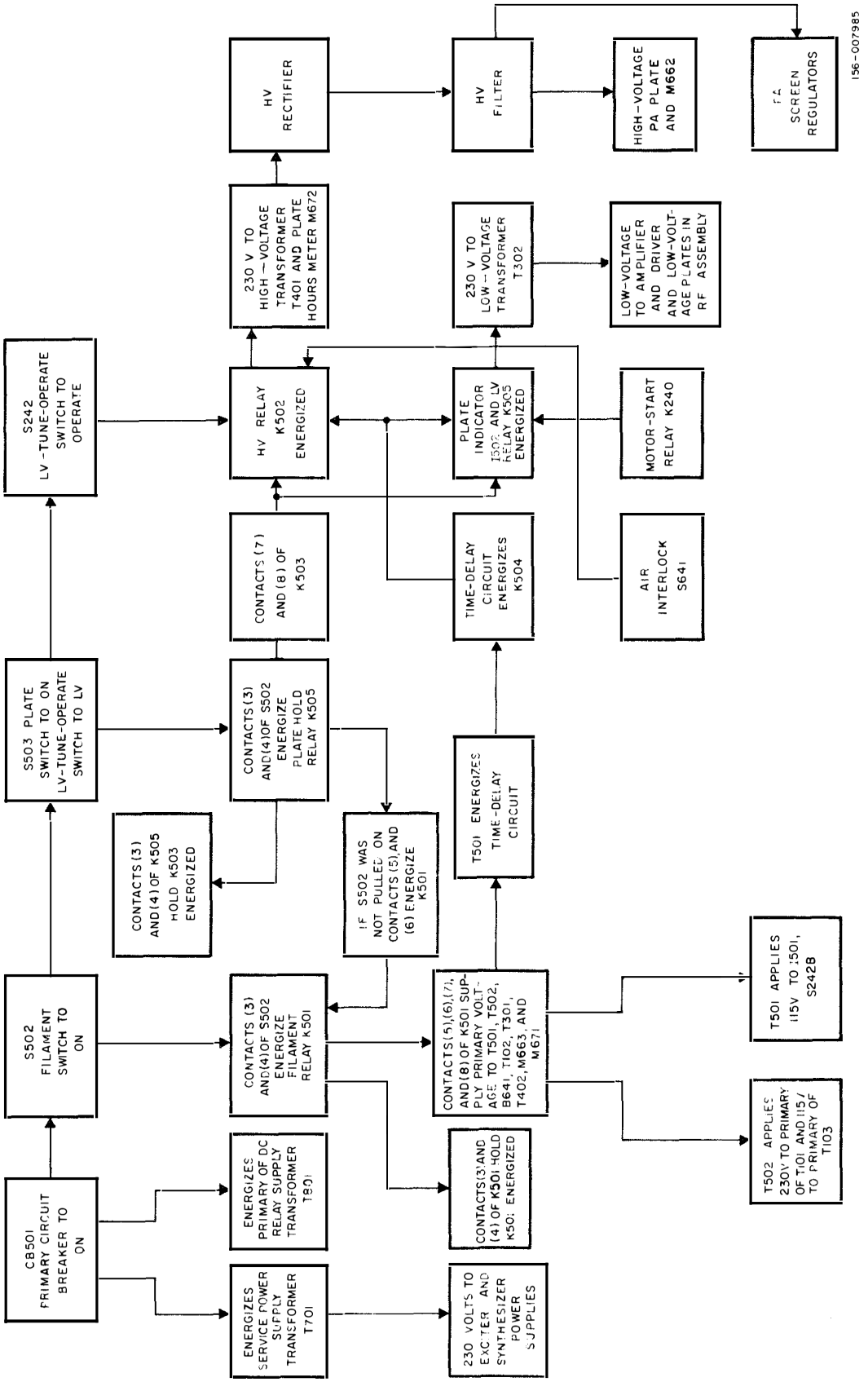


Figure 4-44. Power Control 1A9, Sequence for Local Operation, Block Diagram

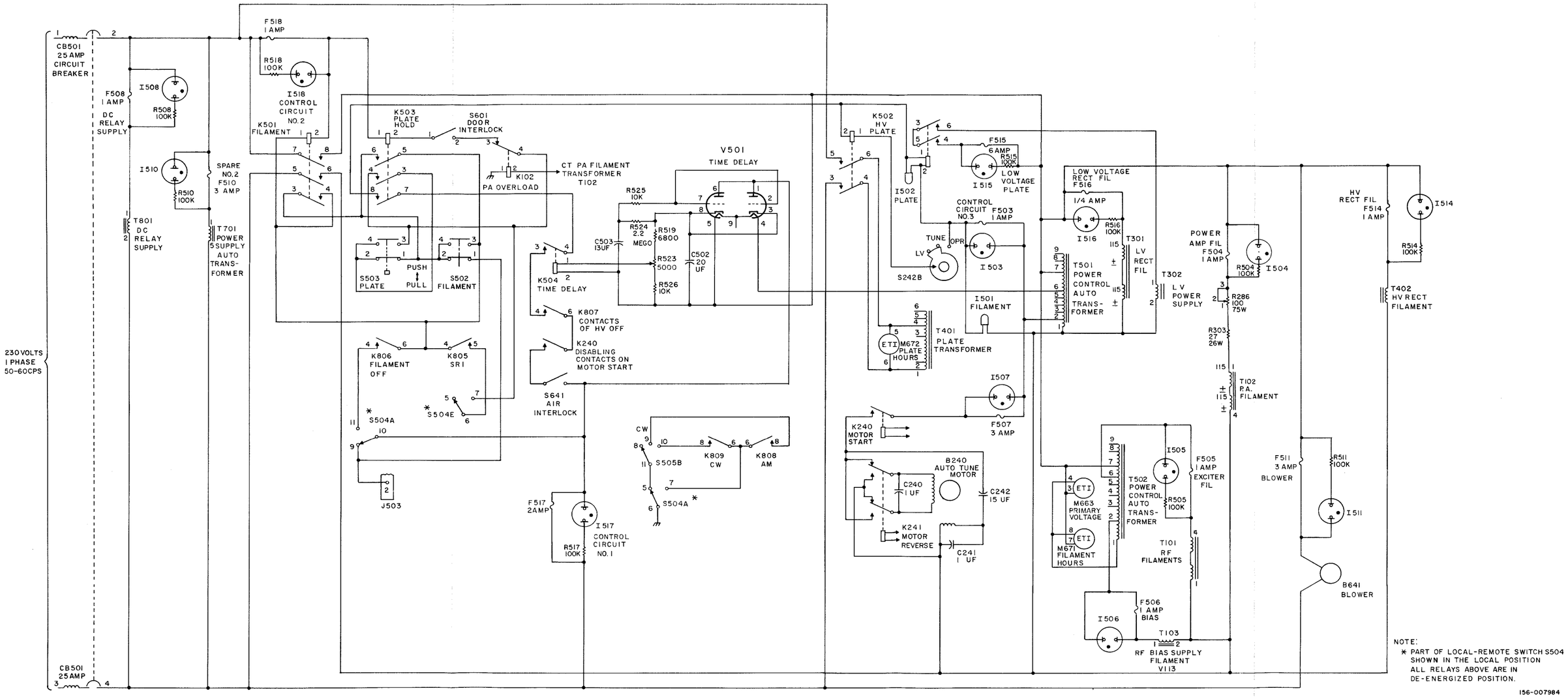


Figure 4-45. Power Control 1A9, Power Control with Associated Circuits, Simplified Schematic Diagram

delay. Changing this adjustment establishes a different current requirement for V501 at which sufficient voltage will be built up to energize the relay. If the primary input voltage should be momentarily removed, capacitors C501 and C502 will discharge through the coil of K504, and keep the contacts closed. However, when the contacts release, the relay will be reenergized quickly if, during the interval of voltage removal, the cathodes of V501 have not completely cooled.

(c) PLATE-POWER APPLICATION. - Plate hold relay K503 may be energized by switch S503, either before or after the time-delay circuit has operated. Pulling the PLATE knob forward causes contacts (3) and (4) of S503 to momentarily complete the 230-volt circuit through the closed contacts of S502, S504A-2, and the plate-hold interlock circuit consisting of normally closed contacts of P.A. overload relay K102 and door interlock S651 (when the cubicle doors are shut). S621 HV shorting switch although not electrically connected to interlock circuit, acts in conjunction with door interlock as a safety measure. The contacts of plate-hold relay K503 perform the following functions:

Contacts (3) and (4) return the coil to closed contacts (1) and (2) of S502 and S503, so that when momentary switch S503 returns to its normal position, relay K503 will remain energized through this holding circuit.

Closed contacts (5) and (6) energize filament relay K501 in the event FILAMENT switch S502 has not been operated previously; these contacts are provided so that K501 and K503 may be energized simultaneously in the event the PLATE control alone is actuated to the ON position. On the other hand, pressing this control breaks only the plate hold circuit to K503, whereas, if the FILAMENT control is pressed while K503 is energized not only is the filament circuit to K501 broken but also the plate hold circuit to K503. Since plate hold relay K503 receives its energizing voltage through the normally closed contacts of S502, operating the FILAMENT control to off, disables power applied to most of the transmitter except for the synthesizer and exciter which remain energized.

Closed contacts (7) and (8) ready the plate interlock circuit to complete the 115-volt, AC circuit to the low-voltage and high-voltage plate relays (K505 and K502). The plate interlock circuit consists of the following relays whose pertaining contacts must be closed before K505 and K502 can operate: Time-delay relay K504 which actuates after 4 minutes, high-voltage off relay K807 (normally-closed), in the dial control assembly, motor-starting relay K240 (contacts normally closed after the autotune system has cycled), air interlock S641 (contacts normally closed if blower B641 is operating normally). When the plate interlock circuit is completed, low-voltage plate relay K505 and PLATE indicator lamp I502 are energized. The closed contacts of K505 apply 230 VAC to the primary winding of T302, the low-voltage rectifier plate transformer. If the LV-TUNE-OPERATE switch (S242) is in the TUNE-OPERATE positions, high-voltage plate relay K502 is energized. The closed contacts of K502 apply 230 VAC to the primary winding of high-voltage rectifier plate transformer T401 and PLATE HOURS meter M672 (identical in operation to M671).

(2) REMOTE OPERATION. - When PRIMARY CIRCUIT BREAKER CB501 is turned on and LOCAL-REMOTE switch S504 is at the REMOTE position, the radio set is readied for power application by operation from a remote station. As previously discussed in paragraph 4-6c of this section, dial control 1A1 permits operation of power control 1A9 by means of a telephone dial. Switch sections S504A-2 and S504E-1 provide an alternate circuit for the energization of filament relay K501 and plate hold relay K503 by dial control relays K806 and K807 respectively. In remote operation, relays K806 and K807 perform the same functions as the FILAMENT and PLATE controls do in local operation. Switches S502 and S503, which are operated by the FILAMENT and PLATE controls respectively, are taken out of the circuit by the action of the LOCAL-REMOTE switch; all other circuits except the emission-selection circuit are the same as during local operation of the power control assembly. Switch section S504A-1, in the REMOTE position, replaces SSB-CW-AM switch S505 with an alternate circuit using CW relay K808 and AM relay K809 of dial control 1A1.

e. LV SUPPLY 1A11, FUNCTIONAL DESCRIPTION.

(1) OVERALL FUNCTIONAL DESCRIPTION. - The LV supply (see figure 4-46) uses two rectifiers, type JAN 3B28 (V301 and V302), connected as a full-wave rectifier plate transformer T302. The filaments of V301 and V302 receive power from rectifier filament transformer T301. The JAN 3B28 is a xenon-filled tube which operates satisfactorily over a wide ambient-temperature range. The rectified voltage is fed to a single-section choke-input filter consisting of choke L301 and capacitor C301. This type of filter gives better voltage regulation and protects the rectifiers by preventing current surges, such as those that occur when power is first applied. The 620-VDC output is taken from a voltage divider and bleeder consisting of R301 through R309 (a series-parallel combination equivalent to a 100,000-ohm, 18-watt resistor) and R310. The 620-volt output supplies all the plate and screen circuits in the RF assembly except the plate and screen grid of power amplifier V115.

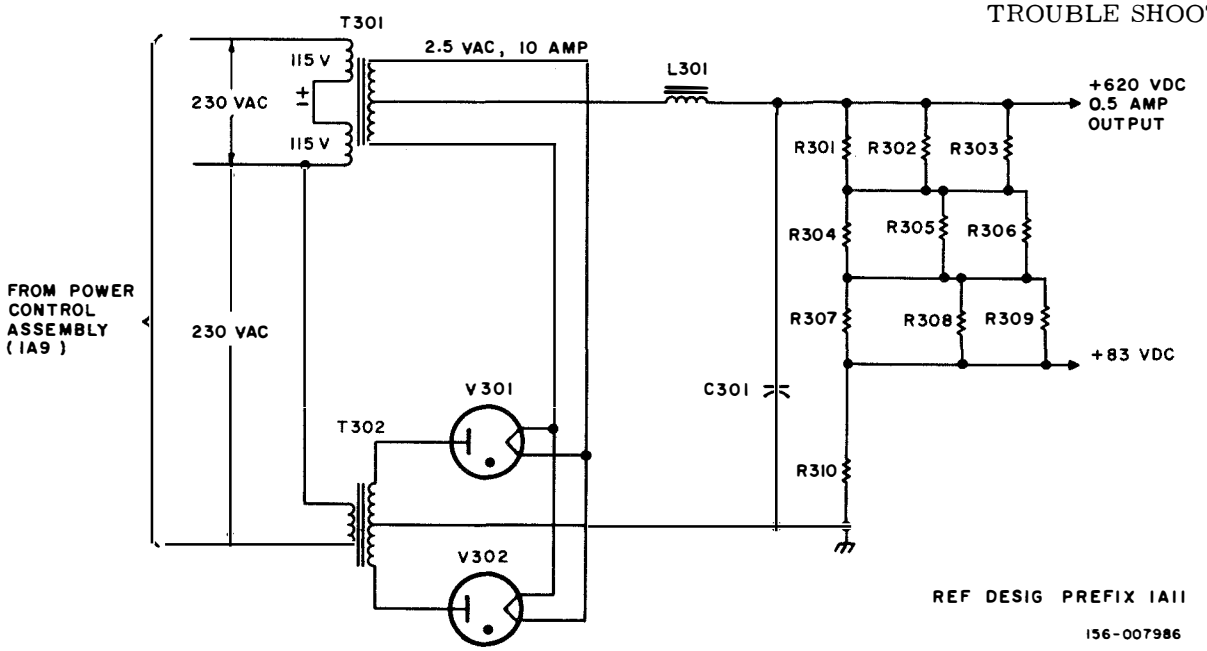


Figure 4-46. LV Supply 1A11, Simplified Schematic Diagram

(2) OVERALL TEST DATA. - Information which will aid in determining the performance of the LV supply is listed below. Refer to figure 4-84 for the circuit location of test points and figure 5-138 for the physical location of test points. The test equipment required is a VOM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

WARNING

Dangerously high voltage exists. Use extreme care when measuring.

(a) Output (TB301-6) (7): 620 VDC.

(b) Output (TB301-5) (8): 83 VDC.

(c) Input (TB301, across terminals 2 and 3): 230 VAC.

(d) Input (TB301, across terminals 1 and 2): 115 VAC.

(e) Refer to figure 5-212 for voltage and resistance measurements.

(f) Refer to Maintenance Standard Book for Radio Transmitting Set AN/FRT-24A.

f. HV SUPPLY 1A10, FUNCTIONAL DESCRIPTION.

(1) OVERALL FUNCTIONAL DESCRIPTION. The HV supply (see figure 4-47) consists of a rectifier assembly, a filter assembly, and rectifier plate transformer T401. The power supply uses two rectifiers, type JAN 4B32 (V401 and V402), connected as a full-wave rectifier to T401. The filaments receive power from rectifier filament transformer T402. The JAN 4B32 is a xenon-filled tube which operates satisfactorily over a wide ambient-temperature range. The rectified voltage is fed to a double-section choke-input filter consisting of chokes L401 and L402 and capacitors C402 and C403. This type of filter gives better voltage regulation and protects the rectifiers by preventing current surges, such as those that occur when power is first applied. For better regulation, a series-resonant filter consisting of L401 and C401 maintains a high input to the rectifiers so that the power-supply (3000-VDC output voltage does not rise excessively when the load is removed. Capacitor C404 is connected across C401 to lower the resonant frequency of the filter for 50-CPS operation. The output voltage is applied to the plate and screen circuits of power amplifier V115 of RF assembly 1A8.

(2) OVERALL TEST DATA. - Information which will aid in determining the performance of the HV supply is listed below. Refer to figure 4-84 for the circuit location of test points and figures 5-135 through 5-137 and 5-140 for the physical location of test points. The test equipment required is a VOM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

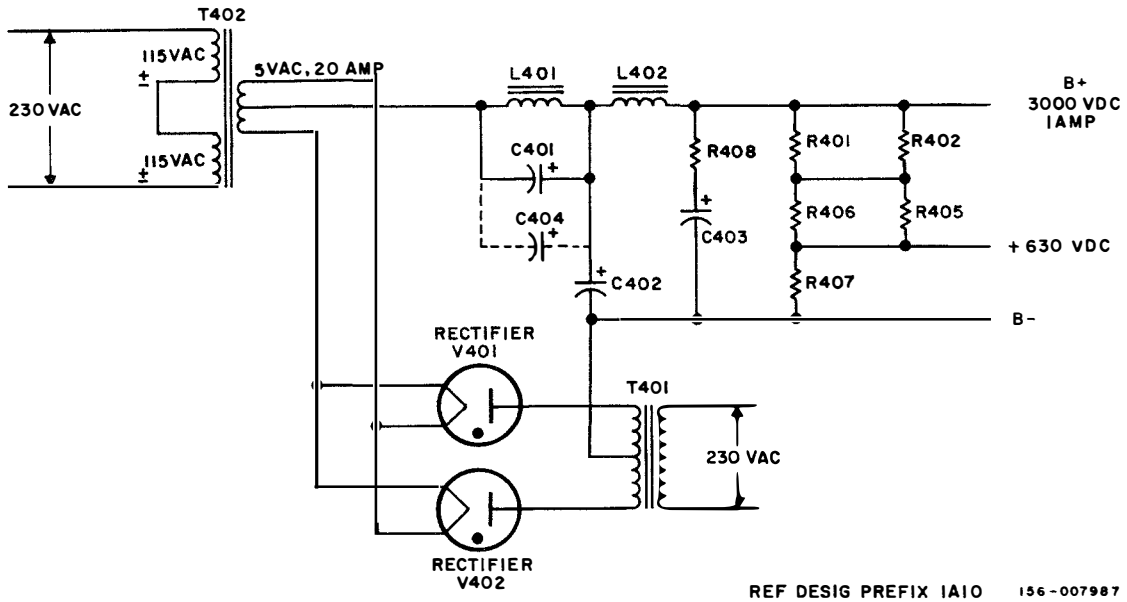


Figure 4-47. HV Supply 1A10, Simplified Schematic Diagram

WARNING

Dangerously high voltage exists in the equipment. Use extreme care when performing measurements.

(a) Output (observe PLATE VOLTAGE meter) (5) : 3 KV.

(b) Output (observe MULTIMETER) (6): 630V

(c) Input (TB401, across terminals 1 and 2): 230 VAC.

(d) Input (T401, across terminals 1 and 4): 230 VAC.

(e) Refer to figure 5-211 for voltage and resistance measurements.

(f) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

g. SERVICE SUPPLY 1A12, FUNCTIONAL DESCRIPTION.

(1) OVERALL FUNCTIONAL DESCRIPTION. - The service supply (see figure 5-213) receives 208-VAC primary AC power from power control 1A9 and distributors it to synthesizer power supply 1A4 and exciter power supply 1A7. The 208-VAC input is applied to terminal 5 of autotransformer T701. Terminals 1 and 7 of the autotransformer supply 230 VAC to exciter power supply 1A7 and synthesizer power supply 1A4. Terminals 1 and 2 of the autotransformer are connected to jack J703 which can be used as a spare 115-VAC power source.

(2) OVERALL TEST DATA. - Information which will be helpful in determining the overall performance of the service supply is listed below. Refer to figure 4-84 for circuit location and figure 5-139 for physical location of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

WARNING

High voltages exist in this equipment. Use extreme caution when performing measurments.

(a) Output (J701 B & C) (9) : 230 VAC.

(b) Output (J704 B & C) (10) : 230 VAC.

(c) Output (J702 A & B): 115 VAC.

(d) Input (T701-5): 208 VAC.

(e) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

4-7. TRANSMISSION LINE COUPLER CU-390/FRT-24, UNIT 7, FUNCTIONAL DESCRIPTION.

a. OVERALL FUNCTIONAL DESCRIPTION (see figure 4-48). - The transmission line coupler matches the unbalanced, 52-ohm coaxial cable attached to the output of Radio Transmitter T-973/FRT-24A to a two-wire, 300-600-ohm balanced transmission line. For convenience, shielding, appearance, and safety to personnel, coaxial cable is used to transmit RF power within the transmitter shelter, whereas for outdoor transmission 600-ohm, two-wire lines are required to match the high-impedance inputs of broad-band type antenna systems. The coupler first transforms the unbalanced 52-ohm output to a balanced 52-ohm output, and then steps up the impedance to approximately 600 ohms by means of artificial transmission lines and other circuit refinements.

b. OVERALL FUNCTIONAL SECTION, TEST DATA. - Information which will aid in determining the overall performance of the transmission line coupler is listed below. Refer to figure 5-223 for the circuit location and figure 5-161 for the physical location of test points.

Using a 2-30 MC signal generator and an SWR meter, with a 600 ohm, 1-watt non-inductive load, the SWR of the transmission line coupler at various frequencies between 2 and 30 MC should be no greater than 2:1. Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

c. CIRCUIT DESCRIPTION (see figure 4-48). - The transmission line coupler is a device that provides both balancing and impedance transformation. It matches the unbalanced 52 - ohm output from the pi-L coupler of the transmitter to a balanced 600-ohm, two-wire line feeding the antenna system. Figure 4-49, A through C, illustrates the basic theory from which this coupler was derived.

Figure 4-49A shows an ideal long transmission line whose input impedance (Z_{in} is equal to the terminating or output impedance (Z_o) and also shows an ideal matching transformer with a balanced input and a balanced output and an impedance-matching ratio of 1:1. If long equally terminated transmission lines are connected in

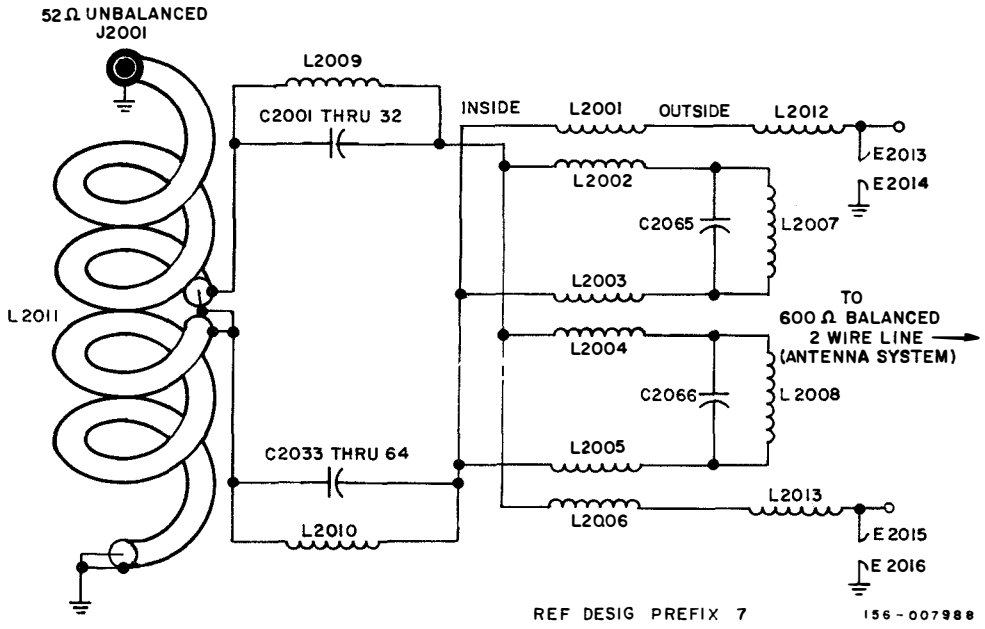


Figure 4-48. Transmission Line Coupler 7, Simplified Schematic Diagram

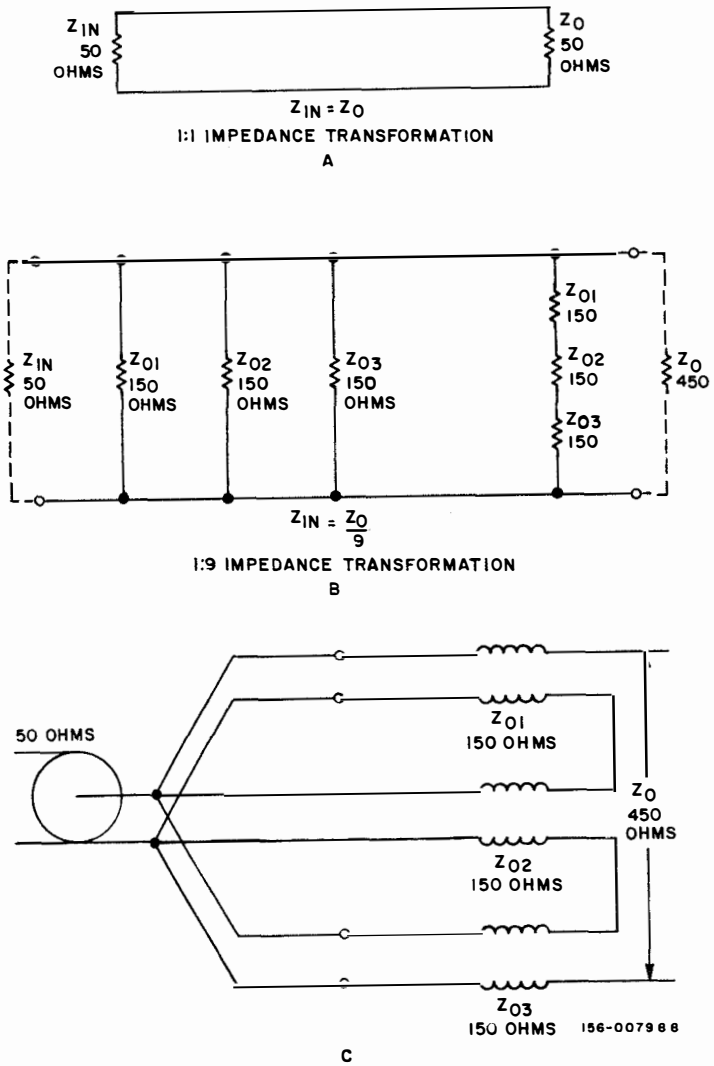


Figure 4-49. Transmission Line Coupler 7, Derivation Diagrams

parallel at one end and in series at the other end, the output impedance (Z_o), as shown in figure 4-49 B, the result is the same as putting lumped resistances in series at the Z_o end and in parallel at the Z_{in} end. The impedance transformation at the input end (looking from the coupler to the transmitter) is step down, and at the output (looking from the coupler to the actual antenna transmission line) step up; in either case, it varies as the square of the number of transmission lines used regardless of whether the circuit constants are lumped or distributed. Since three separate transmission lines are used, the output impedance (Z_o) will appear as nine times Z_{in}, or 450 ohms for balanced impedance transformation.

Figure 4-49C shows the equivalent circuit for the conditions represented in figure 4-49B except that an unbalanced input is fed through the coupler to a balanced output; the circuit also uses artificial transmission lines having lumped constants instead of long terminated lines. If a 600-ohm load is connected across the 450-ohm output of this device, a standing-wave ratio (SWR) of $1.33{:}1 = \frac{(600:1)}{450}$ will exist, assuming a balanced input and output condition. In practice this is very difficult to achieve with antennas and transmission lines particularily when they have to work over a wide frequency range such as 2 to 30 MC. Any unbalance in the transmission line would cause a high standing-wave ratio with subsequent distortion of the radiation pattern.

Lumped transmission lines L2001 and L2002, L2003 and L2004, and L2005 and L2006 are arranged so that their windings offer opposition to the flow of unbalanced currents (always in the same direction) and no opposition to the flow of balanced currents (always in opposite directions). Balance is obtained by the use of a coil balun, L2011, to couple the matching unit to the unbalanced 52-ohm transmitter output jack (P2001). This balun consists of a coaxial line wound as an inductance and connected as shown in the schematic in figure 4-48. As connected, the center conductor of the grounded half of this coil is not used and the circuit operates as if it were comprised of two tank circuits balanced to ground. The unbalanced 52-ohm output, taken from Radio Transmitter T-973/FRT-24A through an RG-17A/U coaxial cable and connector J107, is introduced to a 52-ohm balanced circuit, L2011, which converts this output to a balanced 52-ohm input. This input impedance is then stepped up in impedance by a device similar to the type discussed above. L2011 is made up of two sections of coiled RF coaxial cable, which together with their distributed capacitances, act as two parallel resonant circuits equivalent to a center-tapped input over the entire operating range to maintain line balance. L2011 covers a 4:1 range in frequency; the use of capacitors C2001 through C2064 (64 capacitors in all) and coils L2009 and L2010 extend the low-frequency range and the overall coverage to 15:1. An improvement in the standing-wave ratio is obtained by the use of tuned circuit C2065 and L2007, in series with the sections of an artificial transmission line consisting of spiral windings L2002 and L2003; and by the use of tuned circuit L2006 and L2008 in series with the other sections of artificial transmission line consisting of spiral winings L2004 and L2005. Two loading coils (L2012 and L2013) are used to extend the frequency range of the coupler to 31.25 MC at the high-frequency end of the range, to prevent an otherwise rapidly rising SWR at 30 MC. These series loading coils, together with the feed-through "bowl" capacitance of 3.6 microfarads to ground (existing at E2003 and E2004, and E2005 and E2006, respectively), also form a small L-type network that matches the 450-ohm theoretical output impedance of the coupler to a 600-ohm load. A horn gap, E2013 and E2014, connected to one side of the balanced line, and E2015 and E2016 connected to the other, protect the equipment from damage due to extremely high voltage surges such as occur during lightning storms.

d. TEST DATA. - Information which will aid in determining the performance of the transmission line coupler is listed below. Refer to figure 5-223 for the circuit location of test points and to figure 5-161 for the physical location of test points.

Using a 2-30 MC signal generator and an SWR meter, with a 600-ohm, 1-watt noninductive load, the SWR of the transmission line coupler at various frequencies between 2 and 30 MC should be no greater than 2:1.

4-8. TRANSMITTER CONTROL C-6466/FRT-24A, UNITS 2 AND 3, FUNCTIONAL DESCRIPTION.

a. OVERALL FUNCTIONAL DESCRIPTION (see figure 4-85). - An audio signal can be applied by either an external amplifier or microphone to input transformer T901. The input signal is amplified by transformer-coupled stages V901 and V903, the input audio and output audio amplifiers, respectively, both of which are operated Class A push-pull. The advantages of using transformers T901, T902, and T903 are ease in matching balanced input and output lines, in driving the push-pull amplifiers, and in obtaining a pass band (100 to 5000 CPS) for voice frequencies with optimum gain. An audio-level meter (M902) can be switched to measure the audio level at the output of V901 or the audio level at the output of

transformer T903. The amplified signal taken from T903 is applied to Audio Frequency Amplifier AM-4246/FRT-24A through a switch circuit in Frequency Shift Keyer KY-557/URT.

A bridge-type compressor circuit reduces the gain of the amplifier whenever the audio level exceeds a preset value. This circuit includes compressor rectifier V904, compressor tube V902, interstage transformer T902, and an audio bridge. Whenever the audio signal from V903 exceeds the preset value of cut-off bias applied to V904, V904 conducts, and the resulting rectified voltage is applied to the input of V902. Tube V902 then conducts and brings the audio bridge more nearly into balance, so that the audio signal voltage appearing across the primary winding of T902 is reduced, thereby lowering the overall gain of the amplifier as long as a signal exceeding the preset value is maintained.

Telephone dial S903 of the transmitter control applies ground pulses to dial control 1A1, which in turn selects the required transmitter function. The number of pulses transmitted corresponds to the number dialed. By dialing certain positions, an established group of pulses will actuate the dial control to set the transmitter to a different frequency channel or type of emission, or to turn off its plate or filament circuits. The new frequency channel to which the transmitter has been set is indicated on CHANNEL meter M901, since a voltage proportional to the channel selected is fed to this meter from the autotone system through 1A8S240 channel indicating switch.

Power for all the circuits of the transmitter control is supplied by rectifier V906. Power for the operation of a microphone, push-to-talk relay K905 and for keying is obtained from taps on bleeder resistors connected across the output of V906. During phone operation, pressing the push-to-talk switch on the microphone energizes K905, which in turn applies a 20/60 MA loop current through its contacts to energize a relay in amplifier 1A2 which removes the grid blocking voltage from the transmitter and makes it operational. During CW operation, a telegraph key is shunted across the normally open contacts of K905, so that depressing the key applies the same 20/60 MA loop current to amplifier 1A2, which then turns on the RF carrier for on-off type keying.

b. OVERALL FUNCTIONAL TEST DATA. Information which will aid in determining the overall performance of the transmitter control unit is listed below. Refer to figure 4-85 for the circuit location of test points and to figures 5-147 through 5-149 for the physical location of test points.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(1) Set up transmitter control unit as follows:

(a) Set ON-OFF switch to ON; the "power" lamp lights.

(b) Set INPUT-OUTPUT switch to OUTPUT.

(c) Insert microphone in MICROPHONE jack.

(2) Talk into microphone and observe the OUTPUT LEVEL meter; the meter will indicate.

(3) Set INPUT-OUTPUT switch to INPUT.

(4) Talk into microphone and observe the OUTPUT LEVEL meter; the meter will indicate.

(5) Dial "5" on the EMISSION AND CHANNEL SELECTOR dial; CHANNEL meter indicates "5" and A7, SSB lamp lights.

(6) Dial "A3" on the EMISSION AND CHANNEL SELECTOR dial; the A3, AM lamp lights.

(7) Dial "A1" on the EMISSION AND CHANNEL SELECTOR dial; the A1, CARRIER, CW lamp lights.

(8) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

c. INPUT AUDIO AMPLIFIER, CIRCUIT DESCRIPTION (see figure 4-50). - Input audio amplifier V901 is a class A push-pull voltage amplifier using cathode bias. Two inputs are provided for this stage; a jack for a carbon microphone and terminals for a 600-ohm balanced input. The MICROPHONE jack (J904) is supplied with power from taps on the power-supply bleeder system (R933 through R937), and is coupled through capacitor C901 to a portion of the primary winding of input transformer T901. The complete primary winding of the transformer, representing a balanced 600-ohm input, is connected to terminals 11 and 12 of terminal board TB901, which is located on the rear of the chassis. A dual AUDIO GAIN control (R901A and R901B) is incorporated into the grid circuit of the input audio amplifier so that the input level to the amplifier may be adjusted. The plate circuits of

V901 are connected in a balanced push-pull arrangement, by plate load resistors R903 and R904, and are connected directly to an audio bridge circuit contained in compressor stage V902.

d. INPUT AUDIO AMPLIFIER, TEST DATA. - Information which will aid in determining the performance of the input audio amplifier circuit is as follows. Refer to figure 4-85 for the circuit location of test points and figures 5-148 and 5-149 for the physical location of test points. Perform voltage and resistance measurements as indicated on figure 5-214.

e. OUTPUT AUDIO AMPLIFIER, CIRCUIT DESCRIPTION (see figure 4-51). - Output audio amplifier V903 is a class - A push-pull voltage amplifier using cathode bias. The input signal for this stage is coupled from the output of the compressor stage by transformer T902. The primary winding of output transformer T903 comprises the plate load for the output audio amplifier. A balanced 600-ohm output to the amplifier 1A2 is furnished by the secondary winding of T903, which is connected to terminals 4 and 5 of terminal board TB901, located on the rear of the chassis.

f. OUTPUT AUDIO AMPLIFIER, TEST DATA. - Information which will aid in determining the performance of the output audio amplifier circuit is as follows. Refer to figure 4-85 for the circuit location of test points and to figures 5-147 through 5-149 for the physical location of test points. Measure the resistances and voltages indicated on figure 5-214.

g. COMPRESSOR RECTIFIER, CIRCUIT DESCRIPTION (see figure 4-52). - Compressor rectifier stage V904 is connected as a full-wave, biased rectifier. The value of positive bias applied to the cathodes of V904 is determined by the setting of COMPRESSOR SET asjustment R927. Since the plates and grids of this rectifier are fed a signal from the plates of the output audio amplifier, the rectifier will conduct whenever the audio output signal exceeds the bias level and the positive bias across resistor R922 will increase. The additional positive bias thus developed is used to control the action in compressor stage V902.

h. COMPRESSOR RECTIFIER, TEST DATA. - Refer to figure 4-85 for the circuit location of test points and to figures 5-148 and 5-149 for the physical location of test points. Measure the resistances and voltages indicated on figure 5-214.

i. COMPRESSOR AND AUDIO BRIDGE, CIRCUIT DESCRIPTION (see figure 4-53). - The compressor stage controls the action in two separate audio bridge circuits. Since the two bridge circuits are identical, only one will be described. Input audio amplifier V901 acts as the voltage source for the bridge, while compressor V902 comprises one arm of the bridge. The additional positive bias developed by compressor rectifier V904 is applied between grid and cathode of V902. Below the threshold of compression (before the compressor rectifier conducts), the plate-to-cathode resistance of V902 is greater than 27,000 ohms; therefore, the bridge circuit (R905, R906, R907, and V902) is unbalanced, and a large percentage of the audio-signal output voltage of V901 appears across one-half of the primary winding of transformer T902. However, when the audio level exceeds the threshold of compression, the compressor rectifier conducts and applies a greater positive bias to the grid of V902, which in turn conducts by a greater amount. As the conduction of V902 increases, its plate-to-cathode resistance decreases by a proportional amount (approaches 27,000 ohms), and the bridge is brought more nearly into balance. As the bridge is brought into balance, the audio-signal voltage across the primary winding of T902 is reduced. This proportionally reduces the output of amplifier (V903) to maintain a nearly constant output level.

j. COMPRESSOR AND AUDIO BRIDGE, TEST DATA. - Refer to figure 4-85 for the circuit location of test points and figures 5-148 and 5-149 for the physical location of test points. Perform voltage and resistance measurements indicated on figure 5-214.

k. AUDIO METERING CIRCUIT, CIRCUIT DESCRIPTION (see figure 4-54). - The AUDIO LEVEL meter (M902) is a rectifier-type VU meter. The meter may be connected into either the input or output circuit of the amplifier by placing INPUT-OUTPUT switch S902 in the appropriate position. With the switch in the OUTPUT position, the meter is connected into the secondary-winding circuit of transformer T903. With the switch in the INPUT position, the meter is connected into the cathode circuit of push-pull cathode follower V905, which is direct-coupled to the plates of input audio amplifier V901.

l. AUDIO METERMING CIRCUIT, TEST DATA. - Information which will aid in determining the performance of the audio metering circuit is listed below. Refer to figure 4-85 for the circuit location of test points and figures 5-148 and 5-149 for the physical location of test points.

(1) Set OFF-ON switch to OFF.

(2) Set INPUT-OUTPUT switch to OUTPUT.

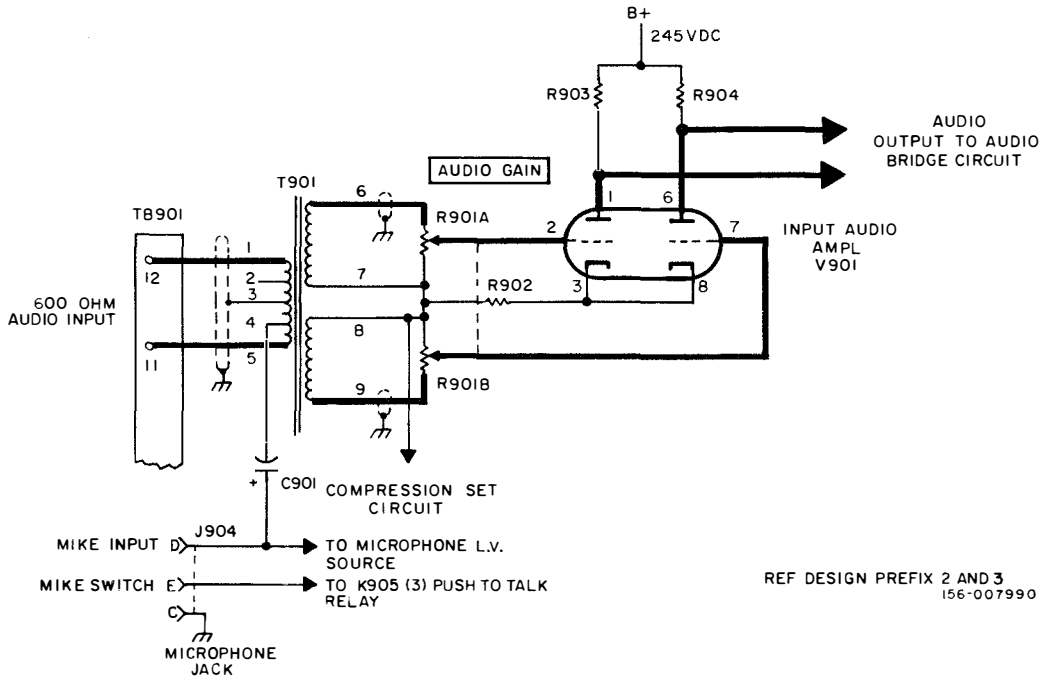


Figure 4-50. Transmitter Control 2 and 3, Input Audio Amplifier, Simplified Schematic Diagram

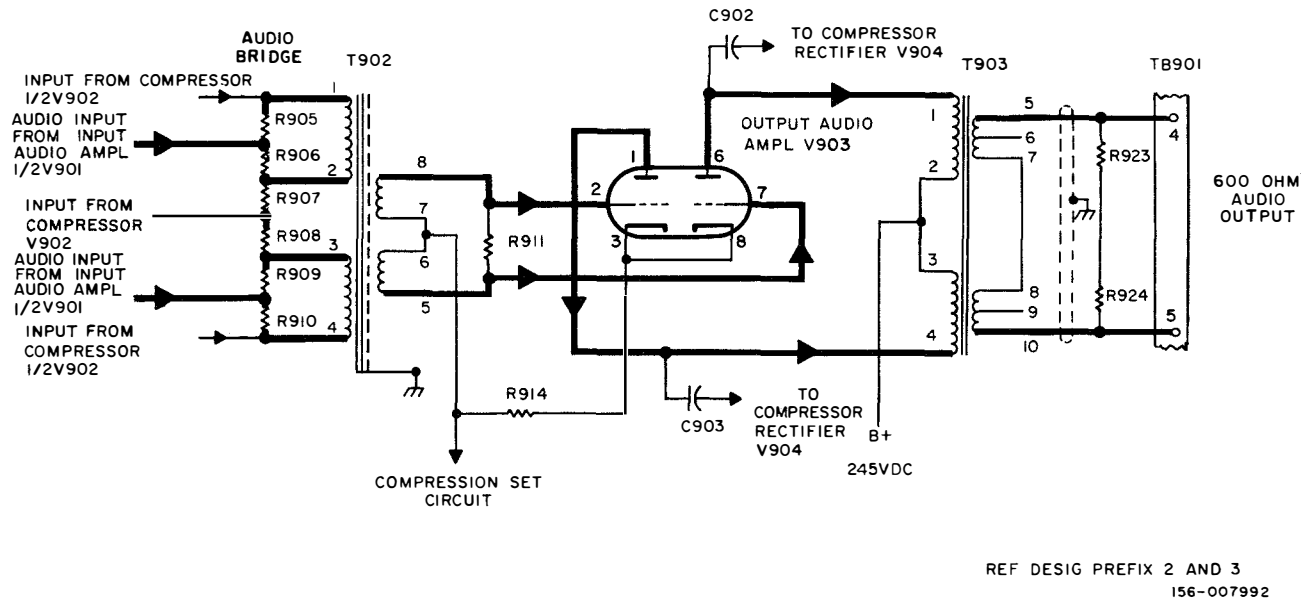


Figure 4-51. Transmitter Control 2 and 3, Output Audio Amplifier, Simplified Schematic Diagram

(3) Measure the resistances indicated on figure 5-214.

(4) Set OFF-ON switch to ON.

(5) Observe AUDIO LEVEL meter; meter will indicate.

(6) Set INPUT-OUTPUT switch to INPUT and observe AUDIO LEVEL meter; meter will indicate.

m. POWER SUPPLY, CIRCUIT DESCRIPTION (see figure 4-55). - The power supply utilizes a full-wave rectifier circuit with a choke-input filter (V906 and associated circuitry), to furnish power for the various circuits contained in the transmitter control. A bleeder network composed of resistors R929 through R932 and R933 through R937, is connected across the output of the power supply to provide the proper operating voltages. An indicator light (I901), located on the top of the inner chassis, is connected in parallel with the primary circuit fuse and will light whenever this fuse blows.

n. POWER SUPPLY, TEST DATA. - Information which will aid in determining the performance of the power supply circuit is as follows. Refer to figure 4-85 for the circuit location of test points and figures 5-148 and 5-149 for the physical location of test points. Perform the voltage and resistance measurements indicated on figure 5-214.

o. KEYING AND PUSH-TO-TALK CIRCUITS, CIRCUIT DESCRIPTION (see figure 4-56). Voltages for keying and push-to-talk operations are furnished from taps on the bleeder system of the self-contained power supply. Closing the key delivers 20/60 MA loop current to the keying line from a tap on the power-supply bleeder system. With the equipment set up for CW operation, this keying voltage operates the CW assembly in amplifier 1A2. The keying line also operates the push-to-talk circuits in the transmitter when the equipment is set up for AM or SSB operation. Closing the push-to-talk switch on the micorophone, operates relay K905 from voltage taps on the power-supply bleeder network. Contacts on relay K905 apply 20/60 MA loop current to the keying line, which operates the push-to-talk relay in the transmitter.

p. KEYING AND PUSH-TO-TALK CIRCUITS, TEST DATA. - Information which will aid in determining the performance of the keying and push-to-talk circuits is listed below. Refer to figure 4-85 for the circuit location of test points and figures 5-148 and 5-149 for the physical location of test points.

(1) Press the push-to-talk switch, speak into the handset and listen for the operation of relay K905.

(2) Dial a random number on the EMISSION AND CHANNEL SELECTOR dial; the CHANNEL meter indicates the number dialed and the A7 SSB lamp lights.

(3) Dial "A1" on the EMISSION AND CHANNEL SELECTOR dial; the A1 CARRIER CW lamp lights.

(4) Dial "A3" on the EMISSION AND CHANNEL SELECTOR dial; the A3 AM lamp lights.

q. TELEPHONE DIAL AND CHANNEL-INDICATOR CIRCUITS, CIRCUIT DESCRIPTION (see 4-57). - Telephone dial switch S903 is similar to the conventional type used in ordinary commercial telephone dials, except that 11 dial positions instead of 10 are required to set up all the functions of equipment. The dial circuit is normally open and is pulsed to ground, the number of pulses corresponding to the number dialed. Dialing A, for example, produces 11 pulses. Dialing a number 1 to 10 sets up the autotune system and consequently the transmitter and synthesizer circuits on the corresponding channel, and also turns on the filament and plate voltages if transmitter was in standby operation. The autotune system operates switch 1A8 S240A and position its arm on one of the taps of the voltage divider consisting of 1A8R240 through 1A8R249, which is connected to the +300-volt output of the exciter voltage regulator through 1A8R161. These taps correspond to the 10-channel positions of the dial, so that a different voltage for each channel is applied to CHANNEL IND. meter M901, to make the meter indicate the number of the channel selected.

Dialing A1 or A3 selects CW or phone transmission, respectively, as described in paragraph 4-6c 1 (a). Dialing any channel automatically places equipment in the A7 (SSB) mode of emission. Dialing A9 turns off the high voltage, and dialing A0 turns off the high voltage and the filament voltage of the RF 1A8 assembly.

r. TELEPHONE DIAL AND CHANNEL INDICATOR CIRCUITS, TEST DATA. - Information which will aid in determining the performance of the telephone-dial and channel-indicator circuits is listed below. Refer to figure 4-85 for the circuit location of test points and figures 5-148 and 5-149 for the physical location of test points.

(1) Set OFF-ON switch to ON.

(2) Dial a random number on EMISSION AND CHANNEL SELECTOR dial; number dialed is indicated on CHANNEL meter.

(3) Repeat step (2) above several times, each time using a different number.

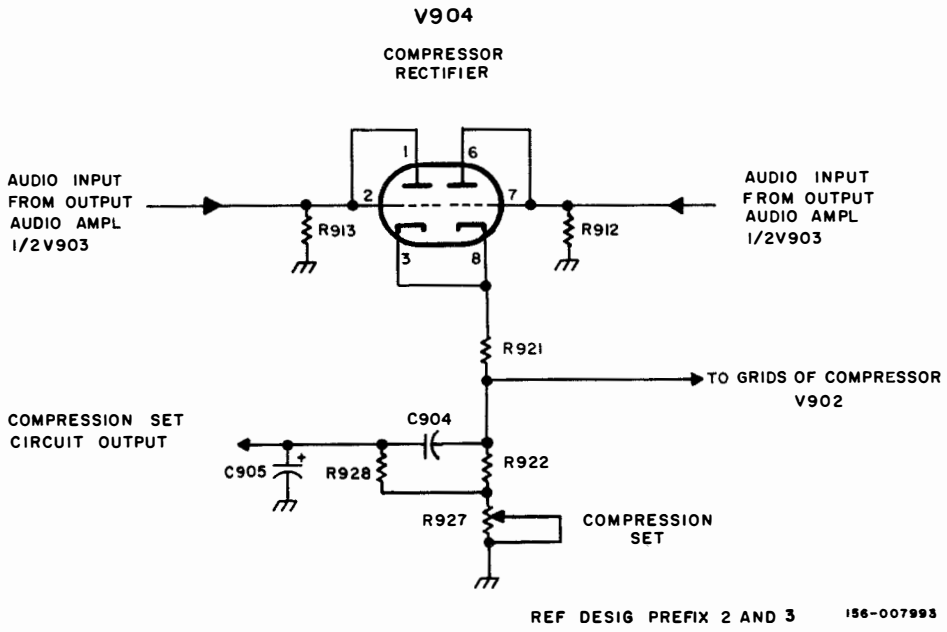


Figure 4-52. Transmitter Control 2 and 3, Compressor Rectifier, Simplified Schematic Diagram

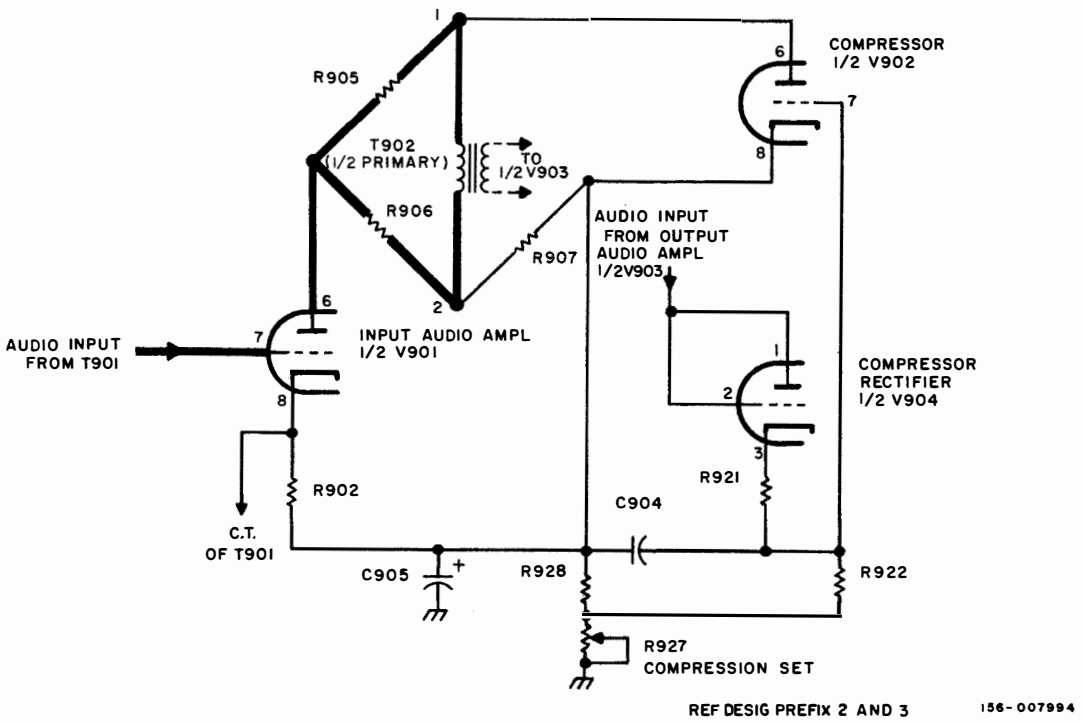


Figure 4-53. Transmitter Control 2 and 3, Compressor and Audio Bridge Circuit, Simplified Schematic Diagram

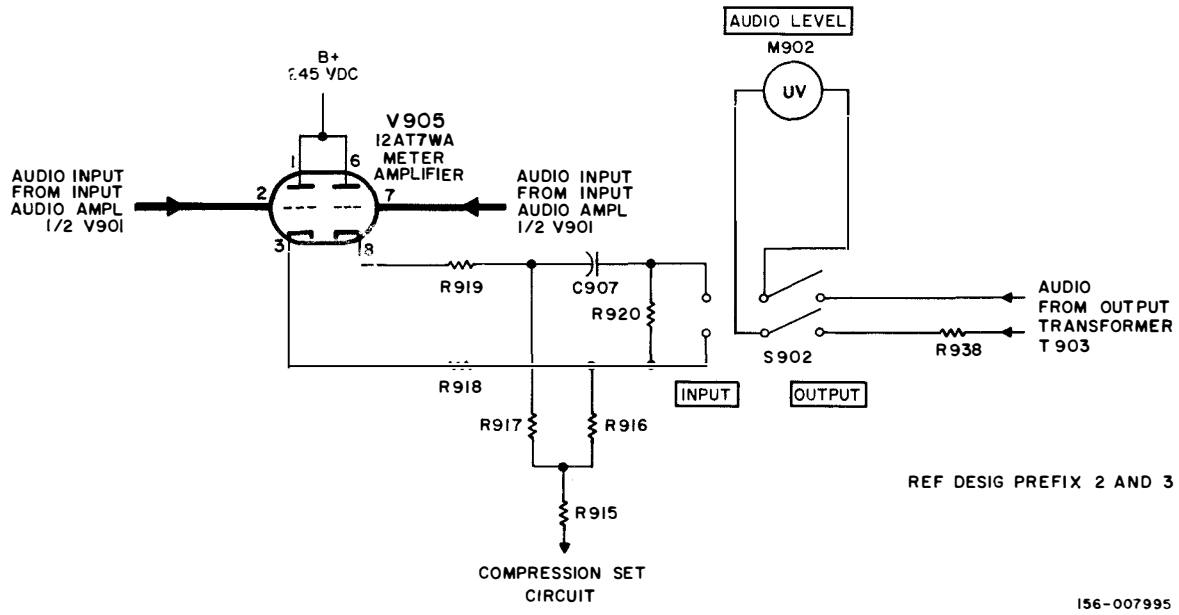


Figure 4-54. Transmitter Control 2 and 3, Audio Metering, Simplified Schematic Diagram

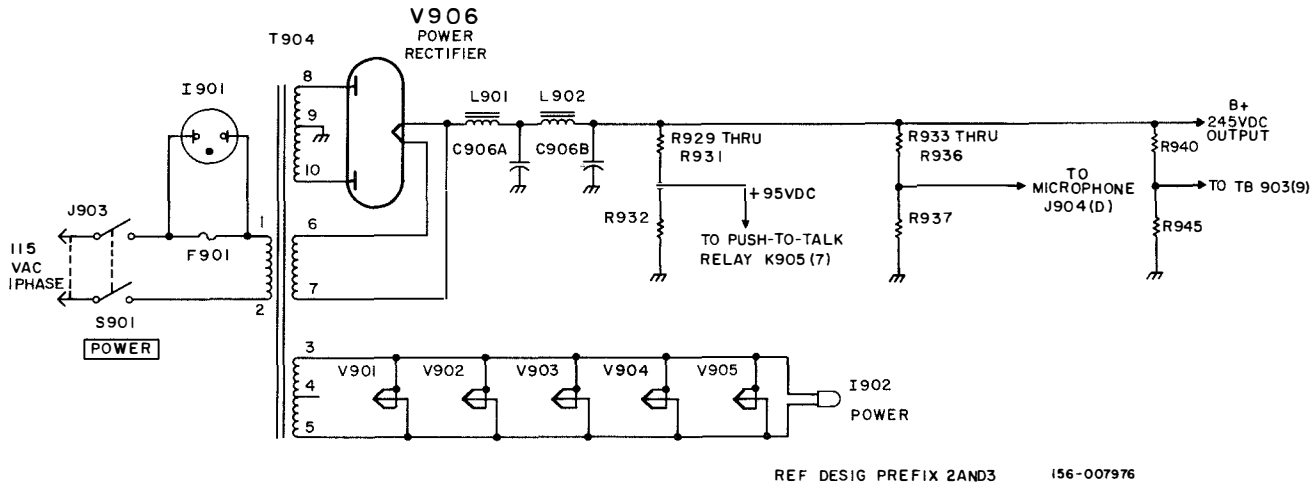


Figure 4-55. Transmitter Control 2 and 3, Power Supply, Simplified Schematic Diagram

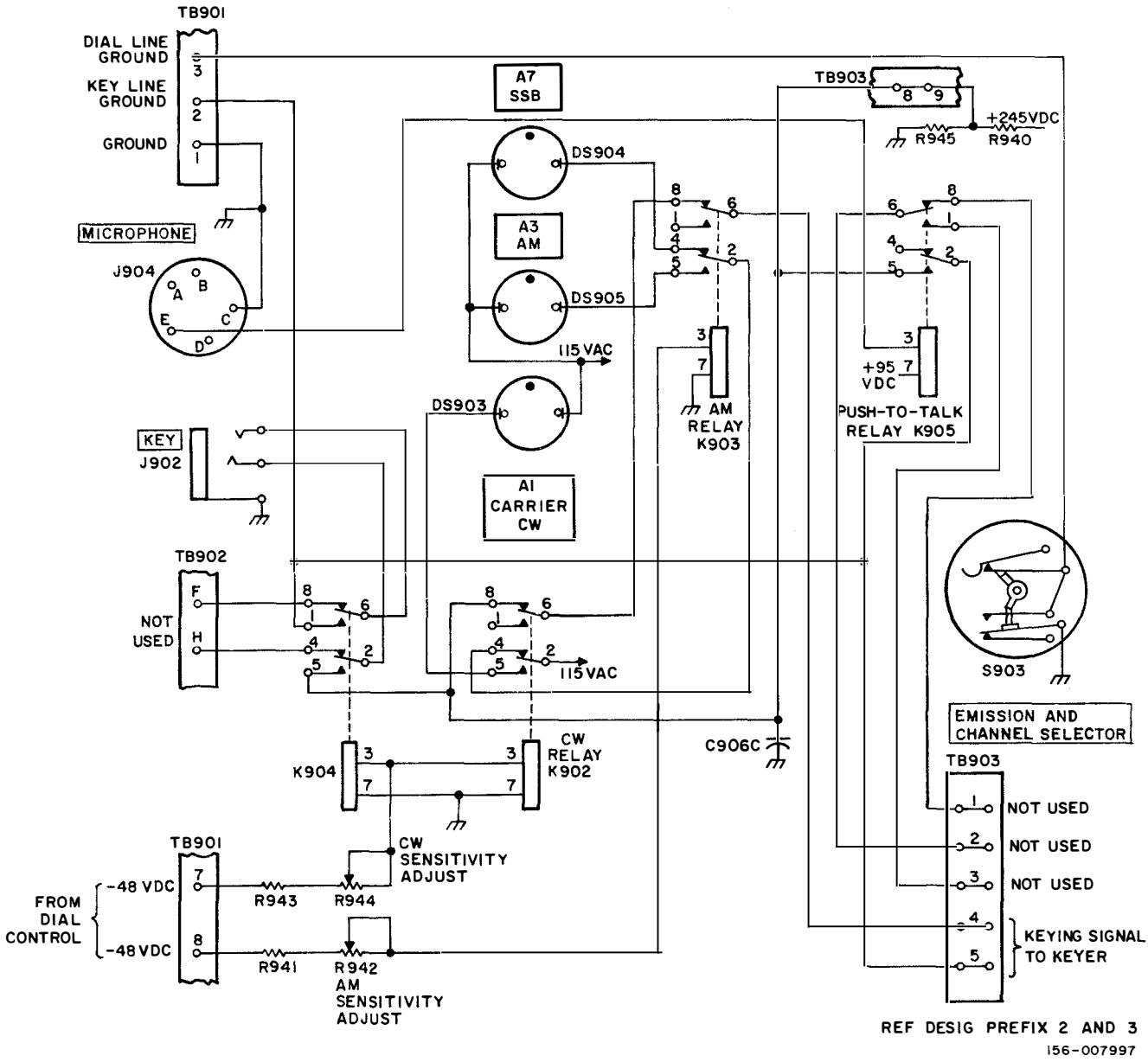


Figure 4-56. Transmitter Control 2 and 3, Keying and Push-to-Talk Circuits, Simplified Schematic Diagram

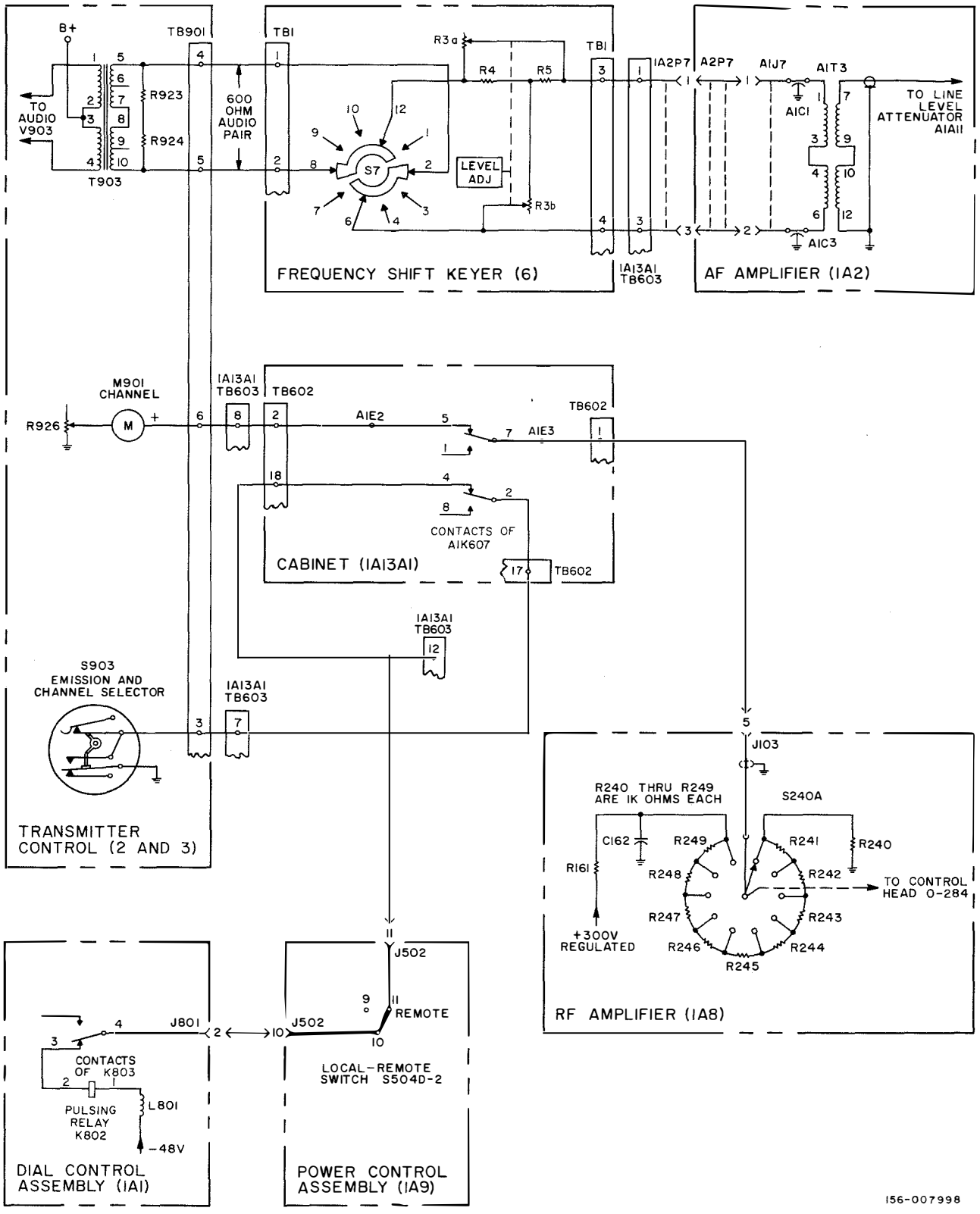


Figure 4-57. Telephone Dial and Channel Indicator Circuits, Simplified Schematic Diagram

4-9. KEYER, FREQUENCY SHIFT KY-557/URT, UNIT 6, FUNCTIONAL DESCRIPTION.

a. OVERALL FUNCTIONAL DESCRIPTION (see figure 4-58). - The keyer consists of a keying functional section, 1-KC oscillator functional section, an output functional section, and a power supply functional section. The keyer receives a 20/60 MA key loop from TTY equipment, audio from transmitter control units 2 and 3, and upper and lower sideband audio from external phone lines. The keyer also accepts key closures from a telegraph key. Depending upon the input signal and the mode of operation, the keyer furnishes the following outputs: Upper and/or lower sideband audio from the transmitter control units; upper and/or lower sideband audio from external phone line; frequency shift keyed 2000 cycles (425 cycles above and below 2000 cycles; 2425 cycles/1575 cycles) from the 20/60 MA TTY key loop; frequency shift keyed 2550 cycles (425 cycles above and below 2550 cycles; 2975 cycles/2125 cycles) from the 20/60 MA TTY key loop; interrupted 1-KC from closures of the telegraph key or from the 20/60 MA TTY key loop.

The keying functional section consists of mark and space oscillators, triggering and gating circuits, and a divider circuit. When the keyer is in the FSK mode of operation, the 20/60 MA key loop input is translated into a frequency shift keyed output having a center frequency of 2000 cycles or 2550 cycles. Actually, the center frequency of the FSK signal does not exist, it is really the average of the mark and space frequencies. When the keyer is in the 2000-cycle FSK mode, the output (when keyed by the 20/60 MA TTY key loop) is either 2425 cycles or 1575 cycles, which is actually an 850-cycle shift and not a 425-cycle deviation from 2000 cycles. When the keyer is in the 2550-cycle FSK mode, the output is 2975 cycles and 2125 cycles. The output of the keying functional section is applied to the output functional section.

The 1-KC oscillator functional section consists of a 1-KC oscillator and a gating circuit. When the keyer is in the 1,000-cycle FSK mode of operation, the 20/60 MA TTY key loop input is translated into an interrupted 1000-cycle output. The 1-KC oscillator functional section also provides on-off keying in accirdance with closures of the telegraph key. The output of the 1-KC oscillator functional section is applied to the output functional section.

The output functional section consists of tone suppression, gating, and monitoring cir-

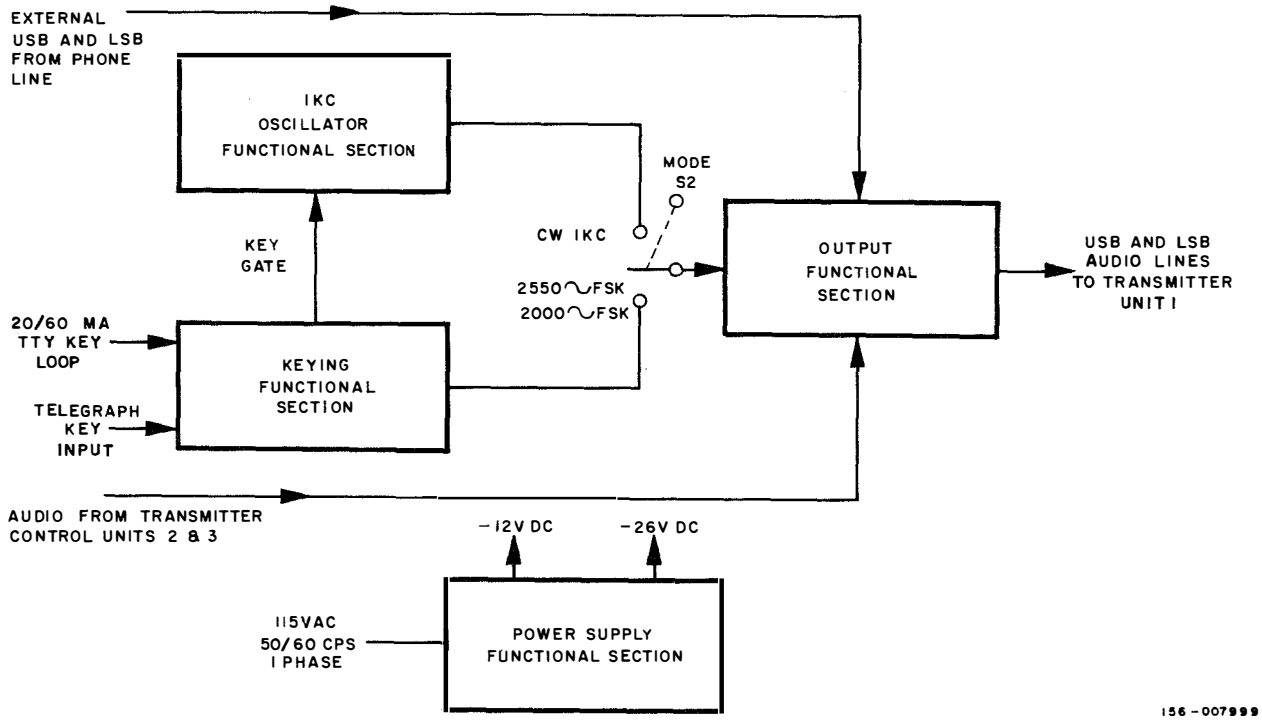


Figure 4-58. Keyer 6, Overall Functional Block Diagram

cuits. This functional section receives 2000-cycle FSK or 2550-cycle FSK from the keying functional section, or an interrupted 1000-cycle signal from the 1-KC oscillator functional section. It also receives audio signals from transmitter control units 2 and 3, and upper and lower sideband audio from external phone lines. All signals leaving the keyer can be monitored visually using front panel meters which indicate signal level, or aurally by connecting a headset to a set of output monitoring jacks on the front panel. The output of the output functional section (keyer output) is applied to amplifier 1A2 in Radio Transmitter T-973/FRT-24A.

The power supply functional section furnishes DC operating and control voltages to the assemblies in the keyer.

b. OVERALL TEST DATA. - Information follows which will aid in determining the overall performance of the keyer. Refer to figure 4-86 for the circuit location and figure 5-160 for the physical location of test points.

(1) Set up the teletypewriter as follows:

(a) Turn "DC power" switch to "off" position.

(b) Turn "line selector" switch to "20" position.

(c) Turn "motor switch" to "off" position.

(d) Place "send-lock" switch in "send" position.

(2) Set up the keyer as follows:

(a) Turn TEST switch to LINE.

(b) Turn FUNCTION LSB switch to OFF.

(c) Turn FUNCTION USB switch to FSK, CW.

(d) Set TONE SUPPR switch to OFF.

(e) Turn DELAY control to its extreme counterclockwise position.

(f) Adjust USB LEVEL ADJUST control so that pointer of meter directly above control is in center of red portion of meter dial.

(g) Turn MODE switch to OFF.

(h) Connect oscilloscope across pins 3 and 4 of terminal board TB1 on rear panel of keyer.

(i) Connect an ammeter between telepewriter and pin 8 or 9 of TB2 on rear panel of keyer.

(j) Set KEYLINE INVERTER switch on rear panel of frequency shift keyer to NORM, with respect to TTY.

(3) Turn "DC power" switch on teletypewriter to "on"; ammeter should indicate approximately 30 MA.

(4) Turn MODE switch to 2550~ FSK position and depress random keys on teletypewriter; "mark" and "space" frequencies should be observed on the oscilloscope.

(5) Set TONE SUPPR switch in ON position, turn DELAY control to its extreme clockwise position and depress LTRS key on teletypewriter; a signal appears instantaneously on oscilloscope or head phone connected to USB monitor and ceases after 10 seconds.

(6) Set TONE SUPPR switch to OFF position and depress random keys on teletypewriter; a signal should be heard.

(7) Repeat step (6) above with MODE switch turned to 1 KC, CW position.

c. KEYING FUNCTIONAL SECTION, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. - The keying functional section (see figures 4-59 and 4-86) is composed of key gate and 1-KC oscillator, A2, crystal oscillator, A3, crystal oscillator, A4, trigger and binary gate, A5, and divider, A6. Because the operation of the keyer is the same for 2000-cycle FSK, as it is for 2550-cycle FSK, only the 2000-cycle FSK operation will be described. With MODE switch, S2, in 2000~ FSK position, operating voltage (-12 VDC) is applied to crystal oscillator, A4. The crystal oscillator assembly contains two crystal oscillators (12.6 KC and 19.4 KC) which begin oscillating with the application of the -12 VDC from MODE switch, S2. The 12.6-KC and 19.4 KC outputs of crystal oscillator A4 are applied through MODE switch, S2, to trigger and binary gate, A5. Crystal oscillator, A3, also contains two crystal oscillator circuits (17.0 KC and 23.8 KC). The 23.8-KC crystal oscillator circuit of A3 obtains its operating voltage directly from the keyer power supply and remains continuously energized. The 23.8-KC output of A3 is applied to key gate and 1-KC oscillator, A2. The 20/60 MA TTY key

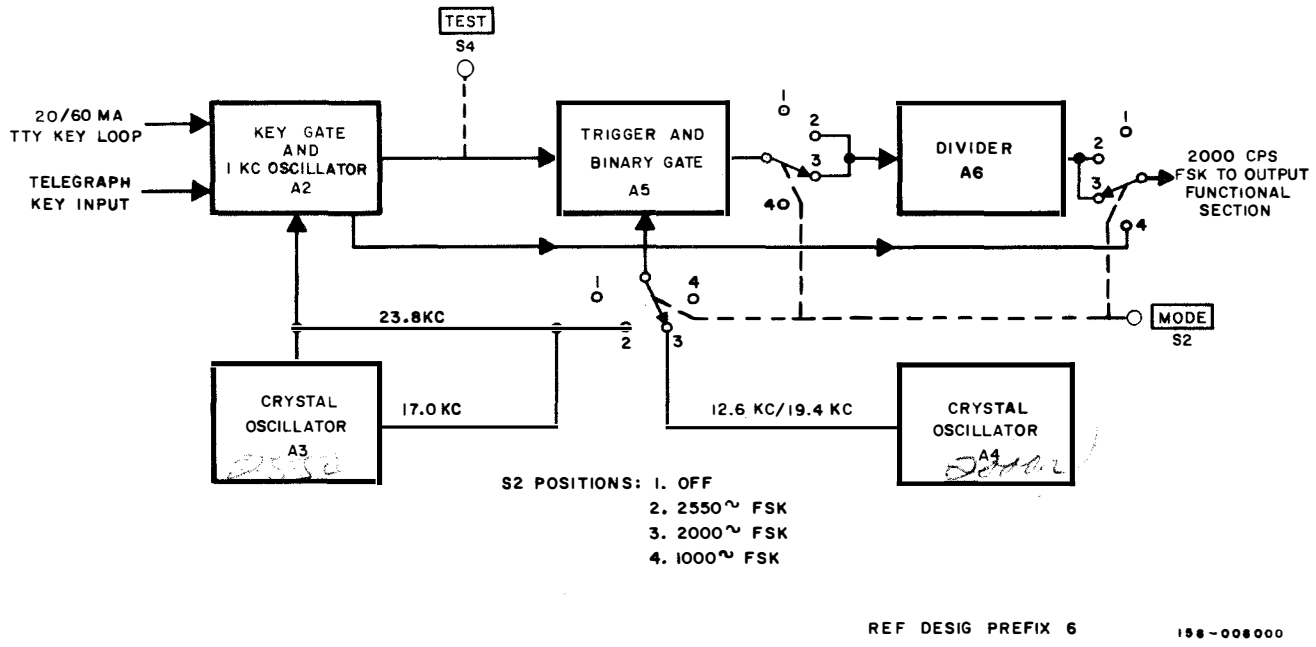


Figure 4-59. Keyer 6, Keying Section, Block Diagram

loop is also applied to key gate and 1-KC oscillator, A2, which keys the 23.8 KC. The keyed output is applied through TEST switch, S4, to trigger and binary gate, A5, which in turn gates the 12.6-KC and 19.4-KC input from crystal oscillator, A3. The gating circuit in A5 gates the 12.6-KC and 19.4-KC signals in accordance with the mark and space inputs from the 20/60 MA TTY key loop. The gated (FSK) output of trigger and binary gate, A5, is applied through MODE switch, S2, to divider, A6. Divider, A6, divides the FSK signal (12.6 KC and 19.4 KC) by eight to produce the 2000-cycle FSK output (1575 cycles and 2425 cycles; 850-cycle shift). The output of divider, A6, is applied to the output functional section. DELAY control, R2, provides from 0 to 10 seconds delay before termination of the keyer output, after completion of the teletype message.

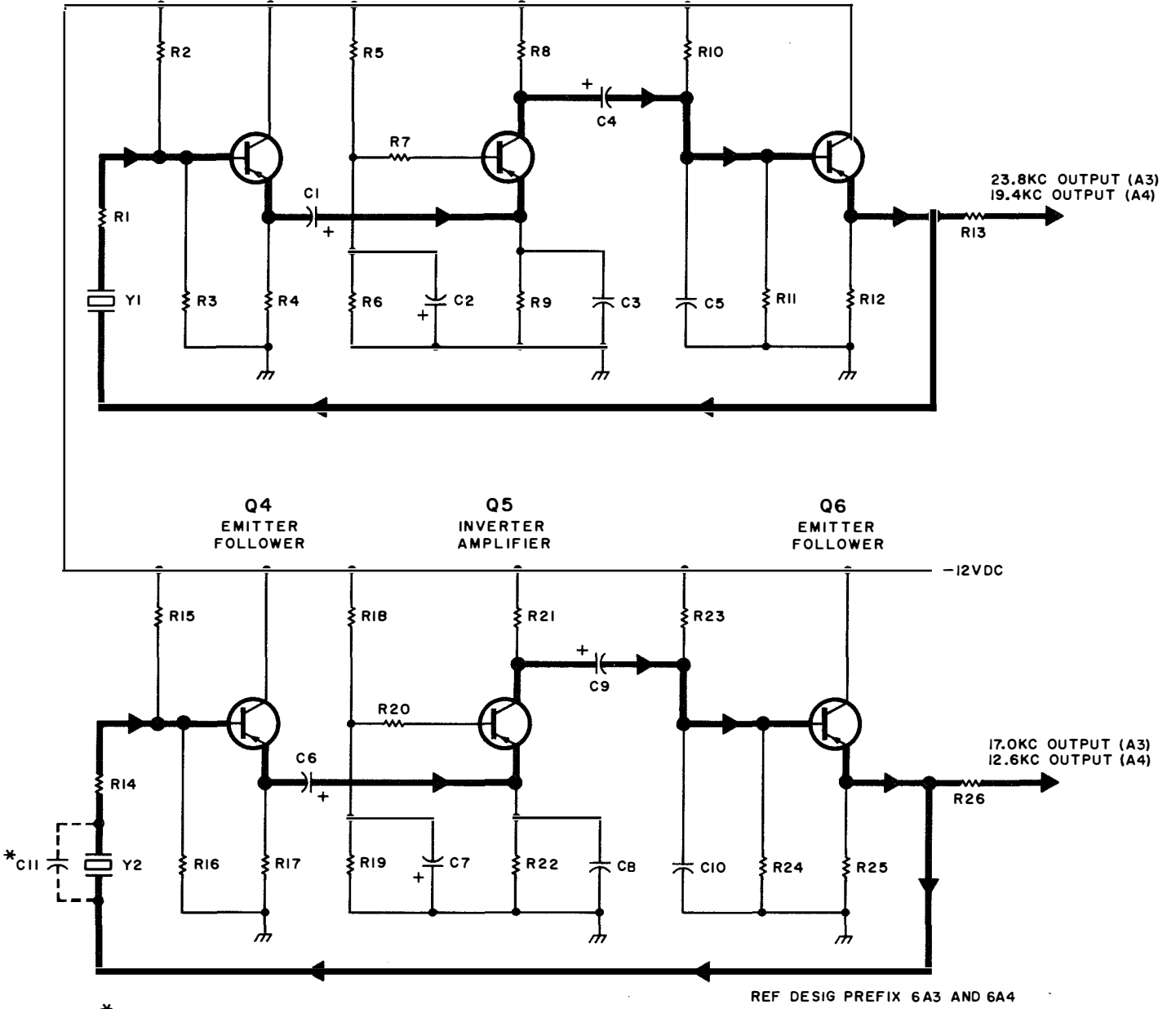
(2) OVERALL FUNCTIONAL SECTION TEST DATA. - Information follows which will aid in determining the overall performance of the keying functional section. Refer to figure 4-86 for the circuit location and figures 5-154 through 5-159 for the physical location of test points.

(a) Set up keyer as indicated in the note referenced in test points (BT) , (BU) , (BW) , (BX) , (CB) through (CE) and 58 of figure 4-86 and perform measurements.

(b) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

(3) CRYSTAL OSCILLATORS, A3 and A4, CIRCUIT DESCRIPTION. (See figure 4-60). - The crystal oscillators generate frequencies of 12.6 KC, 17 KC, 19.4 KC, and 23.8 KC. They consist of four separate oscillators, one for each of four different frequencies, but all of which have the same basic circuit configuration. Because of circuit similarity, only one, the 23.8-KC oscillator will be described and the same description will apply, with the exception of the crystal used and applicable component reference designation changes, to the other three oscillators.

The crystal oscillator is of the series resonant type, using a crystal as the series resonant feedback element, and consists of emitter followers Q1 and Q3, amplifier Q2, and crystal Y1. When power is applied, current flows through emitter follower Q1 and is coupled by capacitor C1 to the emitter of amplifier Q2. The phase of the collector current of inverter amplifier Q2 is the same as the emitter current. The output of



ASSEMBLY	Y1	Y2	CENTER FREQ
A3	23.8KC	17.0KC	2550∿
A4	19.4KC	12.6KC	2000∿

156-008001

Figure 4-60. Keyer 6, Crystal Oscillator, Simplified Schematic Diagram

inverter amplifier Q2 is coupled to the base of emitter follower Q3, whose output is coupled to applicable components of the keyer. A portion of the output of emitter follower Q3 is applied to one face of crystal Y1, which causes a mechanical displacement of the crystal, causing it to oscillate at a frequency of 23.8 KC. The other face of the crystal is connected to the base of emitter follower Q1, causing its output to oscillate at a 23.8-KC frequency, and is passed through the circuit as described previously.

(4) CRYSTAL OSCILLATORS, A3 AND A4, CIRCUIT TEST DATA. - Information follows which will aid in determining the performance of crystal oscillators, A3 and A4. Refer to figure 4-86 for the circuit location and figures 5-152 and 5-155 for the physical location of test points.

(a) Set up keyer as indicated in the note referenced in test points (CB) through (CE) of figure 4-86 and perform measurements.

(b) Refer to figure 5-218 for transistor element voltage measurements.

(c) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

(5) KEY GATE, A2, CIRCUIT DESCRIPTION. (See figure 4-61). - The key gate, which is part of key gate and 1-KC oscillator, A2, receives messages from a 20/60 MA TTY key loop and 23.8 KC from crystal oscillator, A3. It also receives key closures from a telegraph key for "on-off" keying. The two outputs of the key gate are signals which vary from 0 to -5 volts. One output is applied to output and suppression gate, A7, and the other output is applied through TEST switch, S4, to trigger and binary gate, A5. The key gate consists of two key gate amplifiers; a key gate, a recitifier circuit, a delay circuit, and two emitter followers. The 23.8-KC input from crystal oscillator, A3, is applied to the base of key gate amplifier Q1. Base bias is set by a voltage divier (resistors R2 and R3) between -12 VDC and ground. The collector load for Q1 is the primary of transformer T1. The secondary of T1 together with diodes CR1, CR2, and CR3 and the primary of transformer T2 form a gating circuit. The gating circuit enables or inhibits the 23.8 KC applied to key gate amplifier Q2. When the 20/60 MA TTY is generating a "space" signal, current in the key loop ceases and inhibits the gate. With the gate inhibited, the 23.8-KC output of Q1 no longer is allowed to pass through the gate and thus is removed from the base of Q2. When the TTY is generating a message, the gating circuit is enabled and inhibited in accordance with

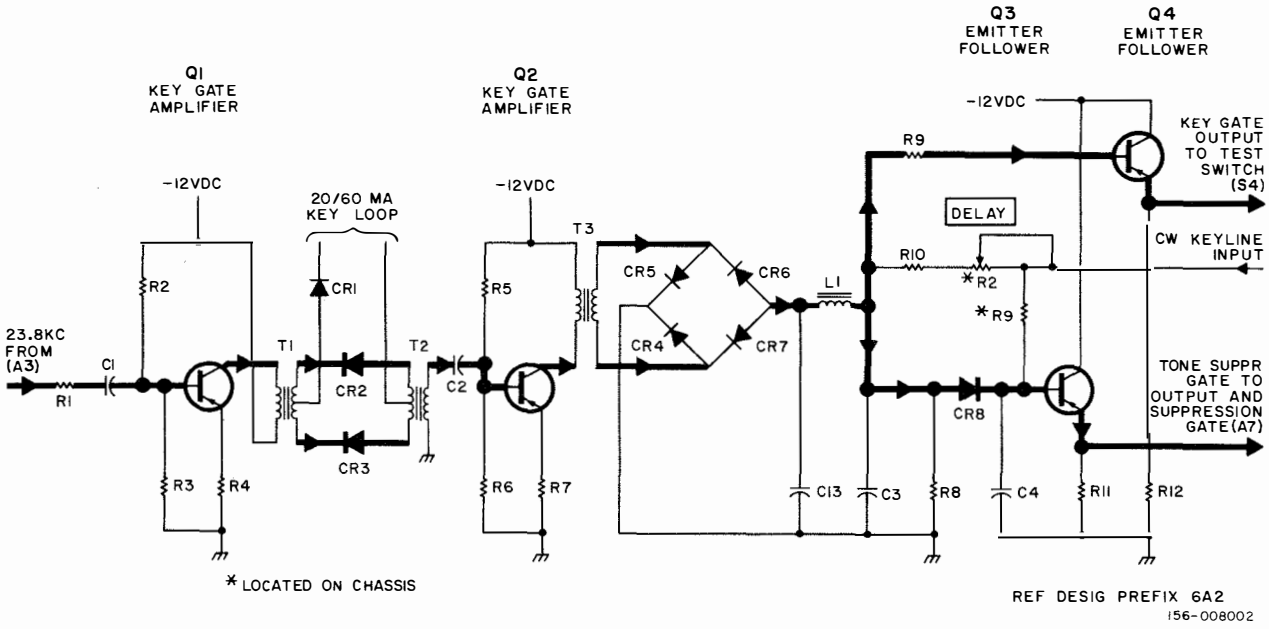


Figure 4-61. Keyer 6, Gate, Simplified Schematic Diagram

the "mark" and "space" input signal, which in turn starts and stops the 23.8 KC applied to key gate amplifier Q2. Base bias for Q2 is set by voltage divider resistors R5 and R6. The collector load for Q2 is the primary of transformer T3. The secondary of T3 is applied to two legs of bridge rectifier CR4 through CR7. The bridge rectifier converts the gated 23.8-KC input to a DC output. The output of the bridge rectifier is filtered by a single section capactive input filter consisting of capacitors C13 and C3, choke L1, and resistor R8. The output of the filter is a -5-VDC potential that is applied to the base of emitter follower Q4 and the anode of diode CR8. The output of emitter follower Q4 is applied through TEST switch, S4, to trigger and binary gate, A5. When the gating circuit is inhibited and there is no output from the bridge rectifier and filter circuit, diode CR8 conducts. Conduction of CR8 puts a positive potential on the base of emitter follower Q3 cutting Q3 off. A delay circuit consisting of resistors, R9 and R10, DELAY potentiometer, R2, and capacitor C4 provides from 0 to 10-second delay before emitter follower Q3 is allowed to conduct. When the TTY is generating "mark" the gating circuit is enabled, the 23.8-KC is rectified by the bridge rectifier, filtered, and applied to emitter follower Q3. The output of Q3 (-5 VDC) is applied to trigger and binary gate, A5. The output of the filter circuit also reverse biases diode CR8 which cuts it off and applies a negative potential on the base of emitter follower Q3. This negative potential causes Q3 to conduct and provide a -5-VDC "mark" output to output and suppression gate 6A1A7. Refer to Handbook of Electronic Circuits (NAVSHIPS 900,000.102) for description of semiconductor amplifier and emitter follower circuits. When the keyer is in "on-off" keying operation, using a telegraph key, the key closures apply -5.2 VDC to the base circuits of emitter followers Q3 and Q4 turning them "on". When the telegraph key is open, emitter followers Q3 and Q4 are turned "off".

(6) KEY GATE, A2, CIRCUIT TEST DATA. - Information follows which will aid in determining the performance of the key gate. Refer to figure 4-86 for the circuit location and figures 5-152 and 5-154 for the physical location of test points.

(a) Set up keyer as indicated in the note referenced in test points (BU), (BX), (BY) and (CK) of figure 4-86 and perform measurements.

(b) Refer to figure 5-217 for transistor element voltage measurements.

(c) Refer to Maintenance Standards Bock for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

(7) TRIGGER AND BINARY GATE, A5, CIRCUIT DESCRIPTION. (See figure 4-62). - The trigger and binary gate receives "mark" and "space" signals (-5 VDC to 0 VDC) from key gate and 1-KC oscillator, A2, and "mark" and "space" frequencies (19.4 KC and 12.6 KC/23.8 KC and 17.0 KC) from crystal oscillators, A3 and A4. The outputs of the trigger and binary gate are Schmitt trigger pulses which are applied to divider, A6, and to key gate and 1-KC oscillator, A2. The trigger and binary gate consists of two Schmitt triggers, an inverter amplifier, and an audio gate. When MODE switch, S2, is in the 2000~ FSK position, 19.4 KC and 12.6 KC are are applied to audio gate CR3 and CR4. With a "mark" input to the Schmitt trigger, Q1 conducts and Q2 cuts off. When Q2 is at cutoff, -7 VDC appears at its collector and is applied through SENSE INVERTER switch, S3 (NORM position), to the anode of audio gate diode CR4. The -7 VDC is also applied to the base of inverter amplifier Q3. The inverted output (-0.8 VDC) of Q3 is applied through SENSE INVERTER switch, S3, to the anode of audio gate CR3. With -7 VDC applied to the anode of diode CR4, the diode becomes reverse biased and inhibits the gate. With the gate inhibited the 12.6 KC is not allowd through, however, the -0.8 VDC applied to the anode of CR3 enables this gate and allows the 19.4 KC to pass to the base of Q4. Transistors Q4 and Q5 form a Schmitt trigger which provides square wave outputs having a pulse repetition rate of 19.4 KC that is applied to divider, A6. With a "space" input to Schmitt trigger Q1 and Q2, Q1 cuts off and Q2 conducts. When Q2 is conducting, -0.3 VDC appears at its collector and enables audio gate CR4. The inverted output of Q3 (-7 VDC) inhibits audio gate CR3. With CR4 enabled, it allows the 12.6 KC to pass to the base of Q4. The output of the Schmitt trigger (Q4 and Q5) is now 12.6 KC. With SENSE INVERTER switch, S3, in INV position, the "mark" and "space" output frequencies of the trigger and binary gate are reversed. Operation of the trigger and binary gate is the same for "mark" and "space" frequencies of 23.8 KC and 17.0 KC.

(8) TRIGGER AND BINARY GATE, A5, CIRCUIT TEST DATA. - Information follows which will aid in determining the overall performance of trigger and binary gate, A5. Refer to figure 4-86 for the circuit location and figure 5-152 and 5-156 for the physical location of test points.

(a) Set up keyer as indicated in the note referenced in test points (BX), (CI), (CH), and (BW) of figure 4-86 and perform measurements.

(b) Refer to figure 5-219 for transistor element voltage measurements.

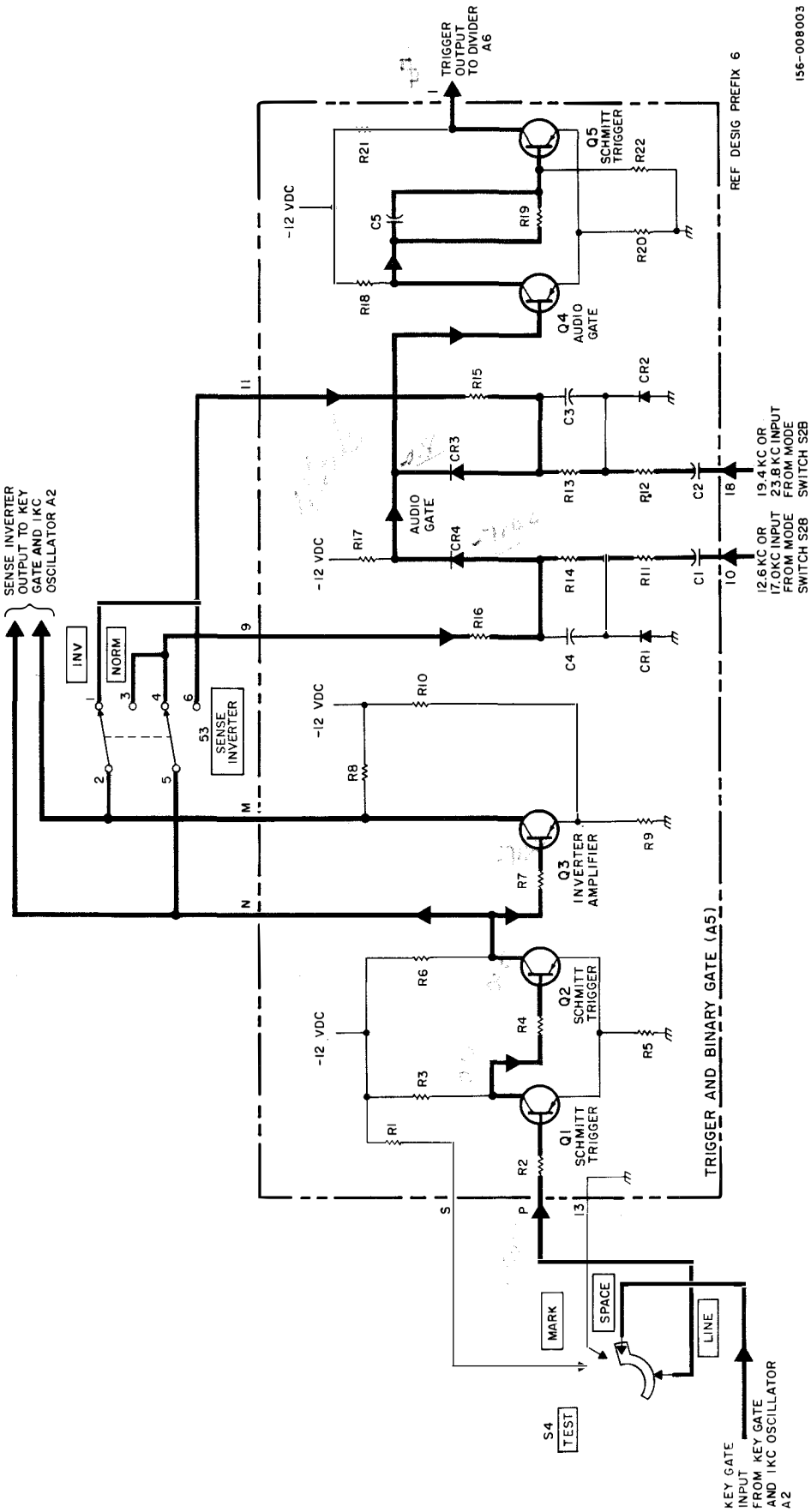


Figure 4-62. Keyer 6, Trigger and Binary Gate, Simplified Schematic Diagram

(c) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

(9) DIVIDER, A6, CIRCUIT DESCRIPTION. (See figure 4-63). - The divider receives frequency shift keyed trigger pulses from trigger and binary gate, A5. When MODE switch, S2, is in the 2550~ FSK position, the FSK trigger pulses are 23.8-KC and 17.0-KC. When the switch is in the 2000~ position, the FSK trigger pulses are 19.4 KC and 12.6 KC. The output of the divider at one-eighth the input frequency (2425 CPS/1575 CPS and 2975 CPS/2125 CPS) is applied through low-pass filter, Z1, to output and suppression gate, A7. The divider consists of three bistable multivibrators connected in cascade and a push-pull amplifier. The input trigger pulses are applied to multivibrator Q1 and Q2 and divided by two. The output of Q2 is applied to multivibrator Q3 and Q4. The divide-by-four output of Q4 is applied to multivibrator Q5 and Q6. The divide-by-eight output of Q5 is applied to push-pull amplifier Q7 and the divide-by eight output of Q6 is applied to push-pull amplifier Q8. The push-pull output developed across output level potentiometer R29 is applied through low-pass filter, Z1, to output and suppression gate, A7. Refer to Handbook of Electronic Circuits NAVSHIPS 900,000.102 for description of multivibrators and push-pull amplifiers.

(10) DIVIDER, A6, CIRCUIT TEST DATA. - Information follows which will aid in determining the overall performance of divider, A6. Refer to figure 4-86 for the circuit location and to figure 5-152 and 5-157 for the physical location of test points.

(a) Set up keyer as indicated in the note referenced in test points (BW) and (BT) of figure 4-86 and perform measurements.

(b) Refer to figure 5-220 for transistor element voltage measurements.

(c) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

d. 1-KC OSCILLATOR FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. - The 1-KC oscillator functional section (see figures 4-64 and 4-86) receives "mark" and "space" gating signal from trigger and binary gate, A5. When the keyer is in the 1,000-cycle FSK mode of operation, the 20/60 MA TTY key loop input is translated into an interrupted 1,000-cycle output. The 1-KC oscillator functional section also provides on-off keying in accordance with closures of the telegraph key. The interrupted output of the 1-KC oscillator functional section is applied to the output functional section.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. - Information follows which will aid in determing the overall performance of the 1-KC oscillator functional section. Refer to figure 4-86 for the circuit location and figures 5-152 and 5-154 for the physical location of test points.

(a) Set up keyer as indicated in the note referenced in test points (CI), (CH), (BV), (CG), and (CF) of figure 4-86 and perform measurements.

(b) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

(3) 1-KC OSCILLATOR, A2, CIRCUIT DESCRIPTION. - (See figure 4-65).- The 1-KC oscillator receives gating signals from trigger and binary gate, A5, and generates continuous wave signals which are routed to the output functional section. It consists of Colpitts oscillator Q5, a gate composed of diodes CR9 and CR10, emitter follower Q6, and amplifier Q7. For a description of the oscillator, refer to Handbook of Electronic Circuits NAVSHIPS 900,000.102. The oscillator output is coupled through capacitor C8, potentiometer R17 and resistor R18 to the anode of diode CR9. The cathodes of diodes CR9 and CR10 are held at a constant potential of 2.1 VDC by voltage divider resistors R19 and R20. When a "mark" signal is received by the trigger and binary gate, potentials of -0.3-VDC and -8-VDC are applied to the anodes of diodes CR9 and CR10, respectively. Application of these potentials forward biases CR9 and reverse biases CR10. Since CR9 is now forward biased (enabled), the 1-KC oscillator output is allowed through to the base of emitter follower Q6. The output of Q6 is applied to the base of amplifier Q7. The output of Q7 is applied through MODE switch, S2, and low pass filter, Z1, to output and suppression gate, A7. When a "space" signal is received by the trigger and binary gate, a -7-VDC potential is applied to the anode of diode CR9 and a -0.8-VDC potential is applied to the anode of diode CR10, thus CR9 is reverse biased and CR10 is forward biased, the 1-KC oscillator output is prevented from passing through the gate, and there is no 1-KC oscillator output.

(4) 1-KC OSCILLATOR, CIRCUIT TEST DATA. - Information follows which will aid in determining the overall performance of the 1-KC oscillator portion of key gate and 1-KC oscil-

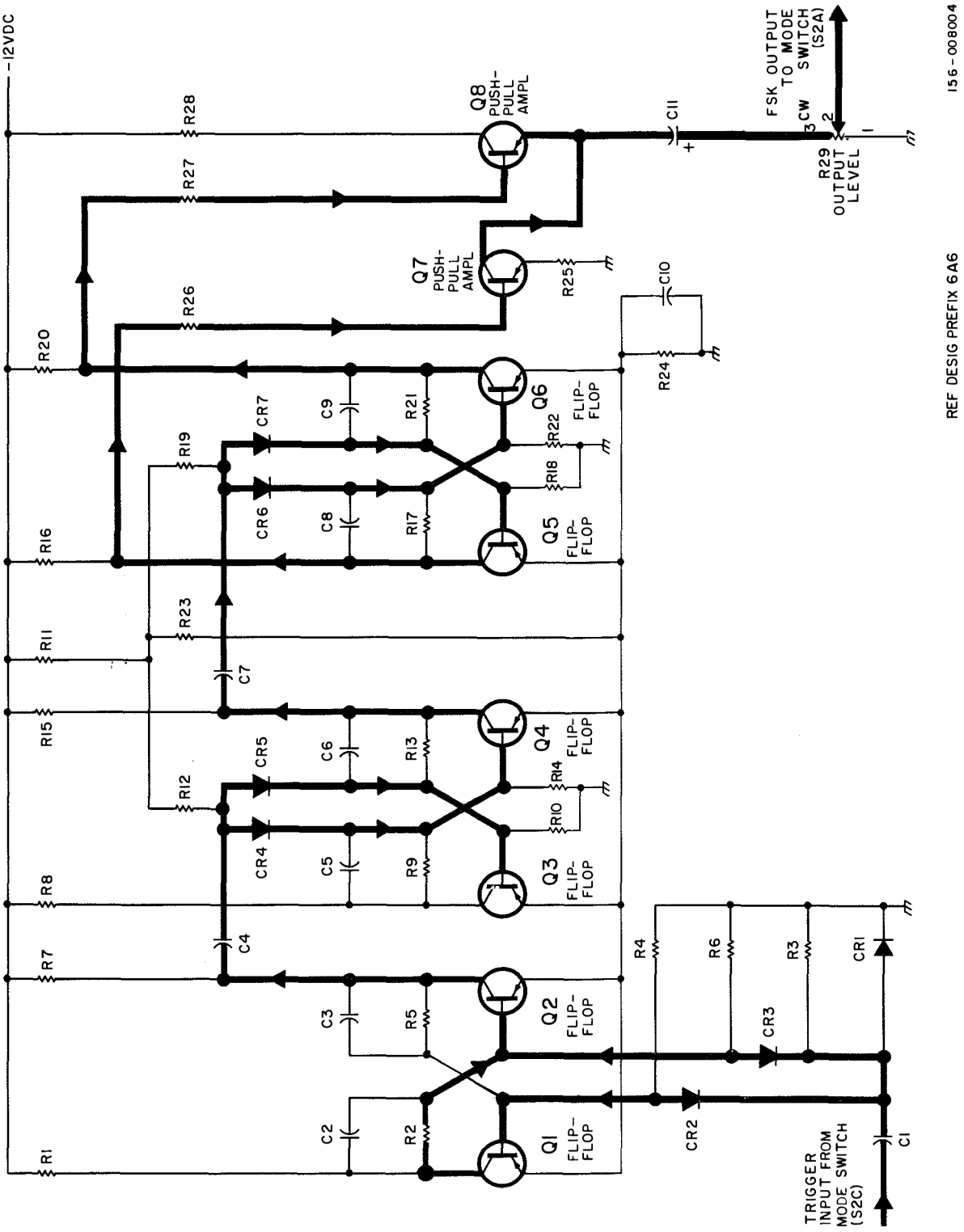


Figure 4-63. Keyer 6, Divider, Simplified Schematic Diagram

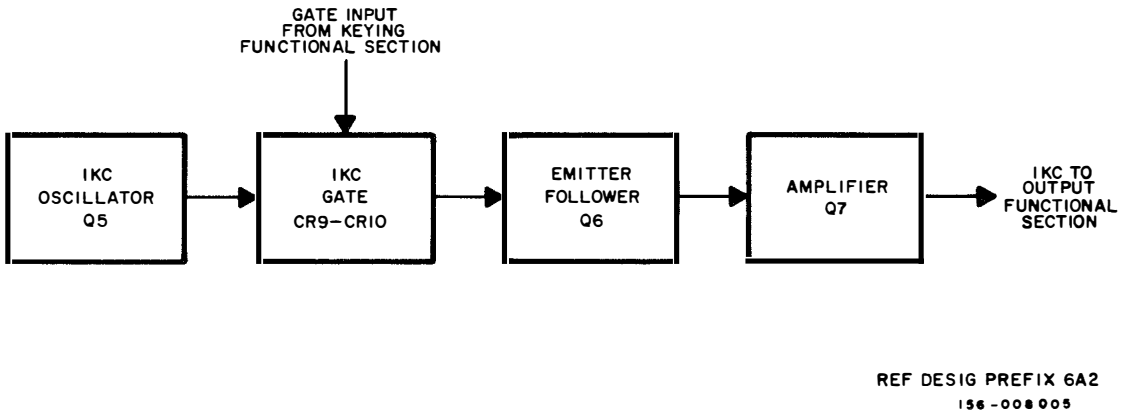


Figure 4-64. Keyer 6, 1-KC Oscillator Section, Block Diagram

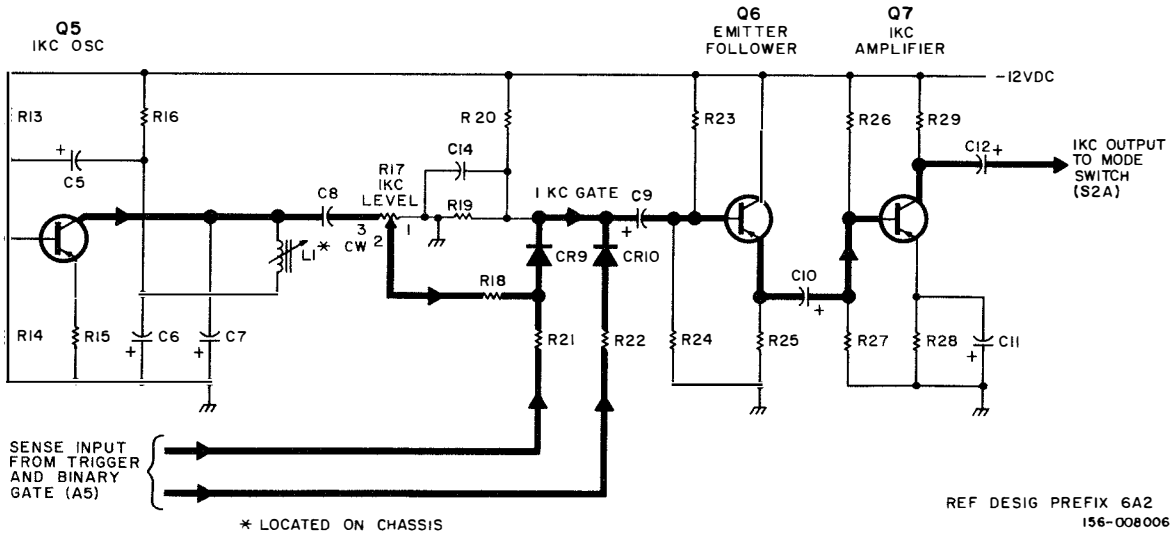


Figure 4-65. Keyer 6, 1-KC Oscillator Simplified Schematic Diagram

lator, A2. Refer to figure 4-86 for the circuit location and figure 5-151 for the physical location of test ponts.

(a) Set up keyer as indicated in the note reference in test points (CF), (CG), and (BV) of figure 4-86 and perform measurements.

(b) Refer to figure 5-217 for transistor element voltage measurements.

(c) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

(d) Critical adjustment: A1L1.

e. OUTPUT FUNCTIONAL SECTION, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL SECTION DESCRIPTION. - The output functional section (see figures 4-66 and 4-86) is composed of output and suppression gate, A7, and audio metering assembly, A8. The output functional section receives FSK signals (2000 CPS and 2550 CPS) from the keying functional section, 1-KC on-off keying from the 1-KC oscillator functional section, audio from transmitter control units 2 and 3, and external upper and lower sideband audio from phone lines. The output functional section monitors all signals leaving the keyer. The signals can either be monitored visually using front panel meters or aurally using headsets connected to the front panel monitor jacks. The output of the output functional section, either 2000-cycle FSK, 2550-cycle FSK, on-off keying (1-KC), phone line audio, or audio from the transmitter control units. is fed to amplifier 1A2 in the transmitter.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. - Information follows which will aid in determining the overall performance of the output functional section. Refer to figure 4-86 for the circuit location and to figures 5-152, 5-158, and 5-159 for the physical location of test points.

(a) Set up keyer as indicated in the note referenced in test points (59), (60), (CJ), and (BR) of figure 4-86 and perform measurements.

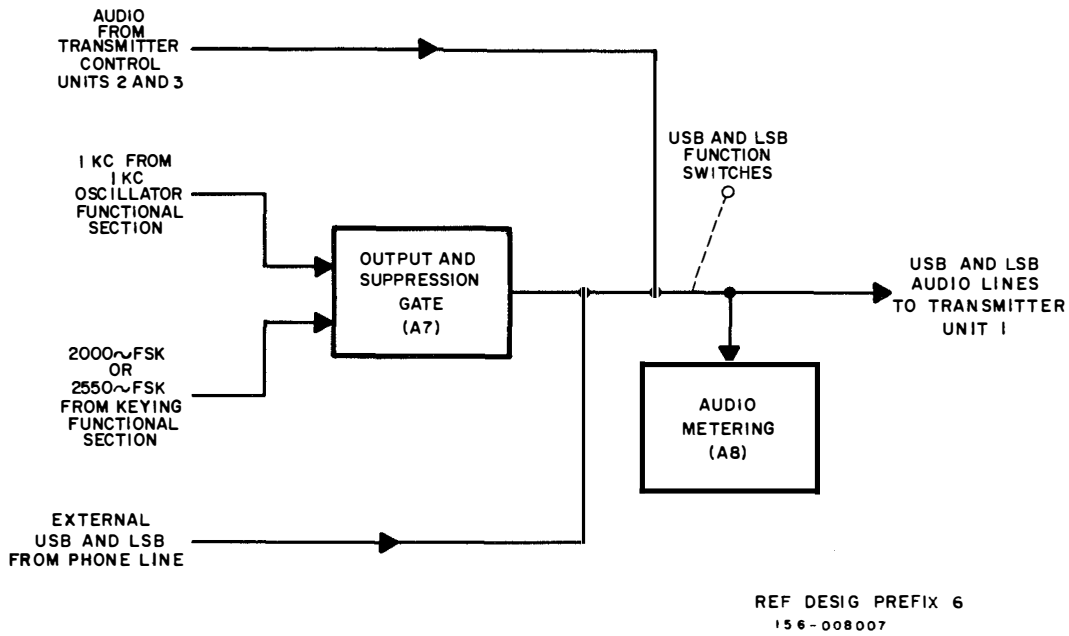


Figure 4-66. Keyer 6, Output Section, Block Diagram

(b) Refer to Maintenance Standards Book for Radio Transmittng Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

(3) OUTPUT AND SUPPRESSION GATE, A7, CIRCUIT DESCRIPTION. (See figure 4-67). - The output and suppression gate receives FSK signals from the frequency shift keying functional section and 1-KC continuous wave signals from the 1-KC oscillator functional section and routes them to the transmitter control units. It consists of emitter follower Q1, TONE SUPPRESSION switch 6A1S6, transistors Q2 and Q3 which comprise a Schmitt trigger, emitter follower gate Q4, tone amplifier Q5, relay driver Q6, and push-to-talk relay 6A1K1. A conditioning pulse from the key gate is applied to the base of emitter follower Q1 and passed to the base of Q2. Transistor Q2 is effectively out of the circuit when TONE SUPPRESSION switch S6 is turned to OFF, since the output of Q1 is sent to ground. When TONE SUPPRESSION switch S6 is set to ON, the output of Q1 is applied to the base of transistor Q2 to turn it on. Simultaneously transistor Q3 which was formerly conducting is now turned off and its negative going output is applied to the base of gate Q4 and relay driver Q6. The output of gate Q4 is applied to the emitter of tone amplifier Q5 to turn it on and allow it to pass the output of the low pass filter, which may be either a frequency shifted or CW signal to transformer T1. The output of the secondary of transformer T1 is one of the output circuits of the output and suppression gate and its signal is routed to the audio metering circuit. The output of relay driver Q6 operates a push-to-talk relay.

(4) AUDIO OUTPUT AND SUPPRESSION GATE, CIRCUIT TEST DATA. - Information follows which will aid in determining the overall performance of the output and suppression gate, A7. Refer to figure 4-86 for circuit location and figure 5-158 for the physical location of test points.

(a) Set up keyer as indicated in the note referenced in test points (BQ), (BR), (BS), (BU), and (CJ) of figure 4-86 and perform measurements.

(b) Refer to figure 5-221 for transistor element voltage measurements.

(c) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

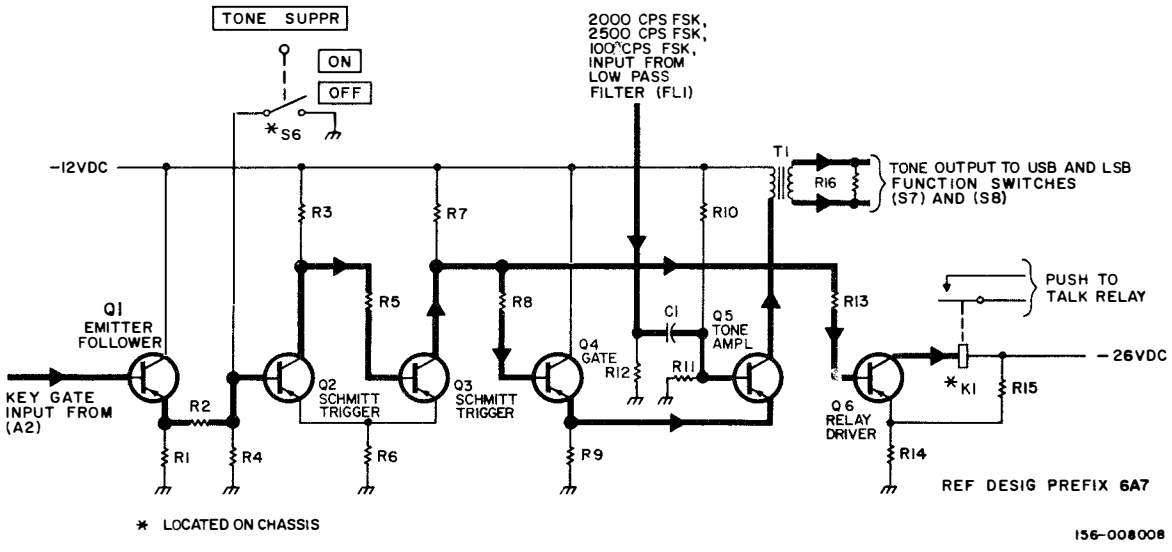


Figure 4-67. Keyer 6, Output and Suppression Gate, Simplified Schematic Diagram

(5) AUDIO METERING, A8, CIRCUIT DESCRIPTION. (See figures 4-68 and 4-86). The audio metering circuit monitors the upper and lower sidebands from transmitter control units 2 and 3 external audio, and the output of output and suppression gate, A7. It consists of bridge rectifier CR1 through CR4, and bridge rectifier CR5 through CR8. Since the configurations of the upper sideband and the lower sideband metering circuits are identical except that they have different reference designations and that one is for upper and the other for lower sidebands, only the upper sideband will be described. When USB FUNCTION switch, S7, is turned to OFF. There are no inputs to the audio metering circuit and USB LEVEL meter, M1, indicates no input. When USB FUNCTION switch, S7, is turned to C-6466, the output of Transmitter Control C-6466/FRT-24A is applied through USB FUNCTION switch, S7, across the attenuator pad composed of R3, R4, and R5 to bridge rectifier CR1 through CR4. This causes a signal to appear at USB MONITOR jack, J1, whose level is indicated on USB LEVEL meter, M1. Portions of the output are also routed to amplifier 1A2 in the transmitter.

(6) AUDIO METERING, CIRCUIT TEST DATA. - Information follows which will aid in determining the overall performance of the audio metering circuit, A8. Refer to figure 4-86 for the circuit location and figures 5-157, 5-158, 5-159 and 5-160 for the physical location of test points.

(a) Set up keyer as indicated in the note referenced in test points 59 and 60 of figure 4-86 and perform measurements.

(b) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

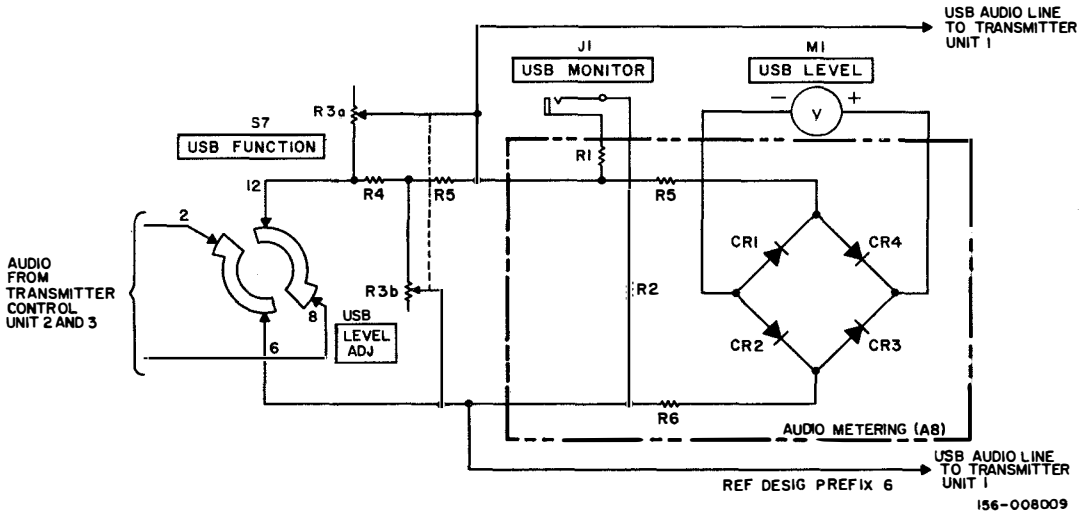


Figure 4-68. Keyer 6, Audio Metering Circuit, Simplified Schematic Diagram

f. POWER SUPPLY FUNCTIONAL SECTION, FUNCTIONAL SECTION DESCRIPTION.

(1) OVERALL FUNCTIONAL, SECTION DESCRIPTION. - The power supply functional section (see figure 4-69) converts the 115-VAC input to a -12-VDC and -26-VDC output which is applied to the operating circuits in the keyer. It consists of power transformer, T1, and power supply A1.

(2) OVERALL FUNCTIONAL SECTION TEST DATA. - Information follows which will aid in determining the overall performance of the power supply functional section. Refer to figure 4-86 for the circuit location and to figure 5-152 for the physical location of test points.

(a) Measure voltage at testpoints (BO) and (BP) of figure 4-86.

(b) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A (NAVSHIPS 0967 009 2060).

(3) POWER SUPPLY, A8, CIRCUIT DESCRIPTION. (See figure 4-70). - The power supply consists of bridge rectifier CR1 through CR4, filter capacitor C1, resistor R1, and zener diode VR1. It receives 20 VAC from power transformer, T1, and converts it to -26 VDC. The -26 VDC is dropped through resistor R1 and zener diode VR1 to -12 VDC. Refer to Handbook of Electronic Circuits NAVSHIPS 900,000.102 for description of power supplies and regulator circuits.

4-10. POWER SUPPLY PP-4242/FRT-24A,(1A4), FUNCTIONAL DESCRIPTION.

a. OVERALL FUNCTIONAL DESCRIPTION. - Power Supply PP-4242/FRT-24 (synthesizer power supply, see figures 4-73 and 5-188), receives 230-VAC, 60-CPS, primary power from the service supply 1A12 and supplies all the synthesizer (1A6) filament and DC voltage requirements. The 230-VAC primary voltage is coupled through ON-OFF switch S1 to the primary winding of power transformer T1. The 230-VAC is also applied to power supply subassembly A2. The secondary of transformer T1 consists of five step-down windings. Secondary winding consisting of pins 5 and 6 steps down the primary AC voltage to 33 VAC which is applied to full wave bridge rectifier CR1 through CR4. Refer to Handbook of Electronic Circuits (NAVSHIPS 900,000.102) for detailed description of a full wave bridge rectifier. The output of bridge rectifier CR1 through CR4, +28 VDC, unregulated, is coupled through fuse F4 to the synthesizer. Blown fuse indicator lamp DS4 lights when fuse F4 blows. Secondary winding consisting of pins 7 and 8 steps down the primary AC voltage to 34 VAC which is applied to full wave bridge rectifier CR5 through CR8. The output of bridge rectifier CR5 through CR8, at +28 VDC, is filtered by capacitor C1 and coupled through fuse F6 to the synthesizer. Blown fuse indicator lamp DS6 lights when fuse F6 flows. A portion of the output, developed across voltage divider A3R4, A3R8, and A3R9, is compared by comparator A3Q2 with a reference established by zener diodes A3VR3 and A3VR4. The resultant error is amplified by driver A3Q1 and applied to regulator Q1 and Q2 changing the bias on Q1. An increase in the output voltage increases the base bias of regulator Q1, thereby decreasing the output voltage. A decrease in the output voltage decreases the base bias of Q1, thereby increasing the output voltage. Secondary winding consisting of pins 9 and 10 steps down the primary AC voltage to 28 VAC which is applied to full wave bridge rectifier CR9 through CR12. The output of bridge rectifier CR9 through CR12, at -36 VDC, is filtered by capacitor C3, coupled through fuse F5, dropped to -12 VDC (by resistor R1 and zener diode A3VR5) and applied to the synthesizer. Blown fuse indicator lamp DS5 lights when fuse F6 blows. A portion of the output developed across voltage divider A3R17, A3R20, and A3R21, is compared by comparator A3Q3 with a reference established by zener diode A3VR6 in the same manner described above. Secondary winding consisting of pins 13 and 15 steps down the primary AC voltage to 13 VAC which is applied to full wave bridge rectifier CR13 through CR16. The output of bridge rectifier CR13 through CR16, at -14 VDC is filtered by capacitor C4 coupled through fuse F8 and dropped to -6.3 VDC by regulator Q5 and applied to the synthesizer filament circuits. A portion of the output, developed across voltage divider A3R26, A3R30, and A3R31, is compared by comparator A3Q5 with a reference established by zener diode A3VR7. The resultant error is amplified by driver A3Q6 and applied to regulators Q6 and Q5 as described above.

b. OVERALL TEST DATA. - Information which will be helpful in determining the overall performance of the power supply circuit is described below. Refer to figure 4-73 for circuit location and to figure 5-70 for physical loction of test points. The test equipment required is a VTVM (refer to Section 1 for type designations).

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

(1) +28-VDC unregulated output (+28 V UNREG test points and GROUND) (40) : +28 VDC.

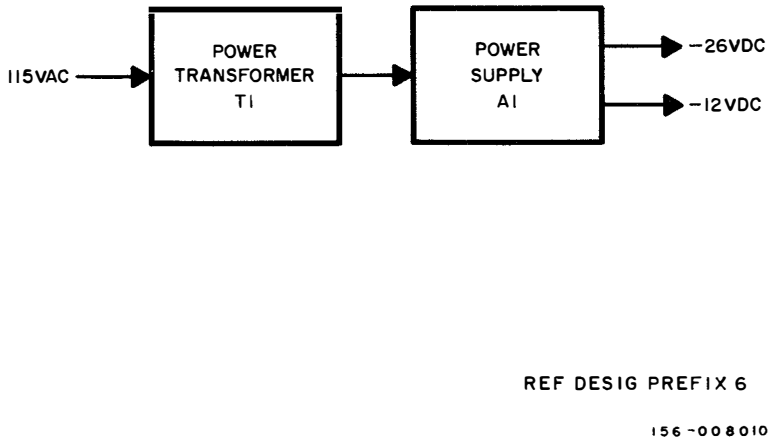


Figure 4-69. Keyer 6, Power Supply Section, Block Diagram

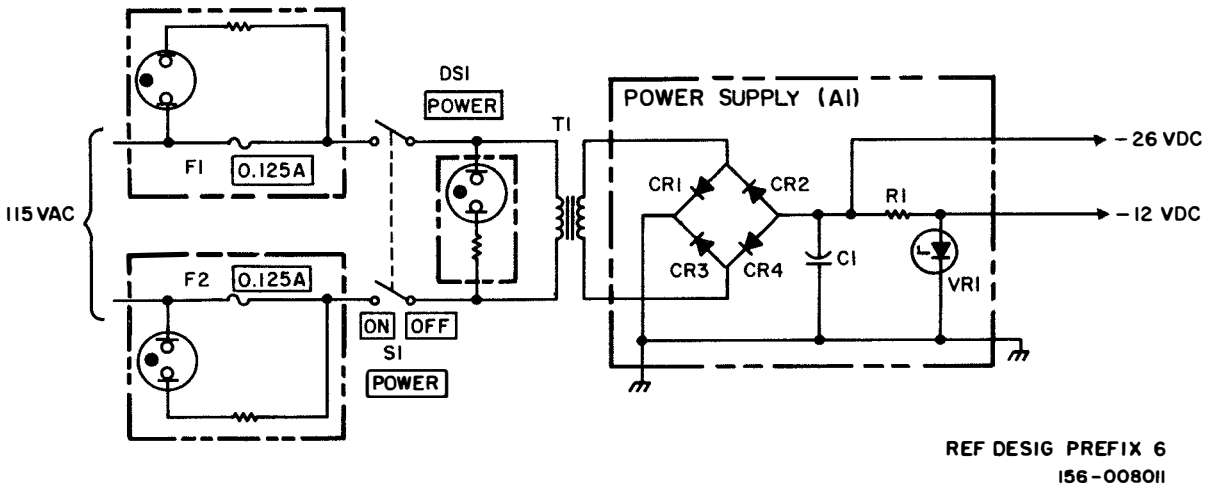


Figure 4-70. Keyer 6, Power Supply, Simplified Schematic Diagram

(2) +28 VDC regulated output (+28V REG test point and GROUND) (41) : +28 VDC.

(3) +12 VDC regulated output (+12V REG test point and GROUND (42) : +12 VDC.

(4) -24 VDC regulated output (-24V REG test point and GROUND) (43) : -24 VDC.

(5) -12 VDC regulated output (-12V REG test point and GROUND) (44) : -12 VDC.

(6) 115 VAC output (115 VAC SEC test points) (63) : 115 VAC.

(7) 6.3 VDC output (6.3 VDC FIL test points) (45) : 6.3 VDC.

(8) Refer to paragraph 5-2 for adjustment procedures.

(9) Refer to figure 5-188 for transistor voltage measurements.

(10) Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

c. POWER SUPPLY SUBASSEMBLY A2, CIRCUIT DESCRIPTION. - The power supply subassembly (see figure 5-189) receives 230 VAC from the power supply assembly and supplies +185 VDC, regulated to synthesizer 1A6. The 230-VAC input is rectified by full wave bridge rectifier CR1 through CR4 and applied to filter capacitor C1 and C2. The output of the filter is applied through series regulators Q1 and Q2 and amplifier Q3 to terminal 1 and 11 of TB2. A portion of the output is compared by differential comparator Q7 and Q8 with a reference voltage developed by zener diode VR2. The resultant error is applied to emitter-followers Q5 and Q6, varying current gain, and coupled through driver Q4 to amplifier Q3 changing its bias. An increase in the output voltage causes an increase in the base current of Q3, which decreases the output voltage. Transistors Q1 and Q2 are normally saturated, and because of their resistance, have no effect on the regulating circuit. Zener diode VR1 sets the bias at the base of Q2. An increase in conduction through resistor R4 increases the negative voltage at the emitters of Q1 and Q2, which pulls Q1 and Q2 out of saturation and allows them to absorb any additional voltage which Q3 does not regulate. If either capacitor C1 or C2 is shorted, the fuse blows, and diode CR9 protects regulator transistor Q1, Q2 and Q3 from the discharge of capacitor C4. If capacitor C4 shorts, the fuse blows and diode CR11 protects Q8 from the discharge of capacitor C7. A saturating bias supply protects the series regulators Q1 and Q2 from any excessive voltages, which may occur if the output of the power supply is shorted and there is no feedback to the driver Q4. Loss of feedback to the driver Q4 would cause the entire output of the power supply to appear across Q1, Q2 and Q3. By maintaining a minimum forward bias on driver Q4, regulators Q1, Q2, and amplifier Q3 never become completely nonconductive. Fuse F7 and blown fuse indicator lamp DS7 are connected to terminal 8 and 18 of the power supply. When F7 blows DS7 lights.

d. POWER SUPPLY SUBASSEMBLY, TEST DATA. - Information which will be helpful in determining the overall performance of the power supply subassembly circuit is listed below. Refer to figure 4-73 for circuit location and figures 5-70 and 5-72 through 5-75 for the physical location of test points.

(1) +180 VDC regulated output (+180 REG test point and GROUND) (62) : +180 VDC.

(2) Refer to paragraph 5-2 for adjustment procedure.

(3) Refer to figure 5-189 for transistor voltage measurements.

4-11. POWER SUPPLY PP-4243/FRT-24A,(1A7), FUNCTIONAL DESCRIPTION.

a. OVERALL FUNCTIONAL DESCRIPTION. - Power Supply PP-4243/FRT-24A (exciter power supply, see figures 4-82 and 5-206) receives 230 VAC, 60 CPS from service supply 1A2 and furnishes all of the converter (1A3) and amplifier (1A2) voltage requirements. The 230-VAC input is applied to the primary windings of power transformers T1001 and T1002. The output of T1001 is rectified by full wave rectifier V1001 and V1002. The output of the rectifier is filtered by choke input filter consisting of inductor L1001 and capacitors C1001, C1002, C1008, and C1010. The 270-VDC output of the filter is dropped to 185-VDC by resistor R1016 and is applied to the amplifier (1A2). Refer to Handbook of Electronic Circuits (NAVSHIPS 900,000.102) for a description of the full wave rectifier and choke input filter circuits. The output from the high voltage secondary windings (pins 9 and 10, and 11) of transformer T1002 is rectified by full wave rectifier V1004. The output of the rectifier is filtered by choke input filter consisting of inductors L1002 and L1003, and capacitors C1003, C1004, and C1009. The 240-VDC output of the filter is dropped to +185-VDC by resistor R1014 and applied to the converter (1A3). The output from the high voltage secondary winding (pins 9 and 11) of transformer T1002 is also rectified by half wave rectifier CR1005 and CR1006. The output of the rectifier is filtered by resistor input filter

consisting of resistors R1012 and R1013, and capacitors C1005, C1006, and C1007. The -30-VDC output of the filter is applied to the converter (1A2). The outputs from the 6.3-VAC secondary windings of transformer T1002 (pins 12 and 13, and pins 14 and 15) and of transformer T1001 (pins 12 and 13) are connected in series and applied to full wave bridge rectifier A1CR1001 through A1CR1004. The output of the bridge rectifier is filtered by capacitor input filter consisting of capacitors A1C1011 and C1012, and resistor A1R1009. The output of the filter is dropped to -10 VDC by resistor R1015 and applied to the converter (1A3). Refer to Handbook of Electronic Circuits (NAVSHIPS 900,000.102) for a description of half-wave rectifier and full-wave bridge rectifier circuits. Application of primary 115-VAC power to the amplifier (1A2) and converter (1A3) is controlled by switch S1002A and S1002B respectively. The 185-VDC and -30-VDC outputs of the power supply and the 240-VDC and 270-VDC outputs of the two choke input filters are monitored on meter M1001 in conjunction with switch S1003.

b. OVERALL TEST DATA. - Information which will be helpful in determining the overall performance of the Power Supply PP-4243/FRT-24A circuit is as follows. Refer to figure 4-82 for circuit location and figures 5-119 through 5-122 for physical location of test points. Perform voltage measurements as indicated in table 3-15. Refer to Maintenance Standards Book for Radio Transmitting Set AN/FRT-24A.

Note

Refer to the servicing block diagram of this functional section at the end of Section 4 for additional test data.

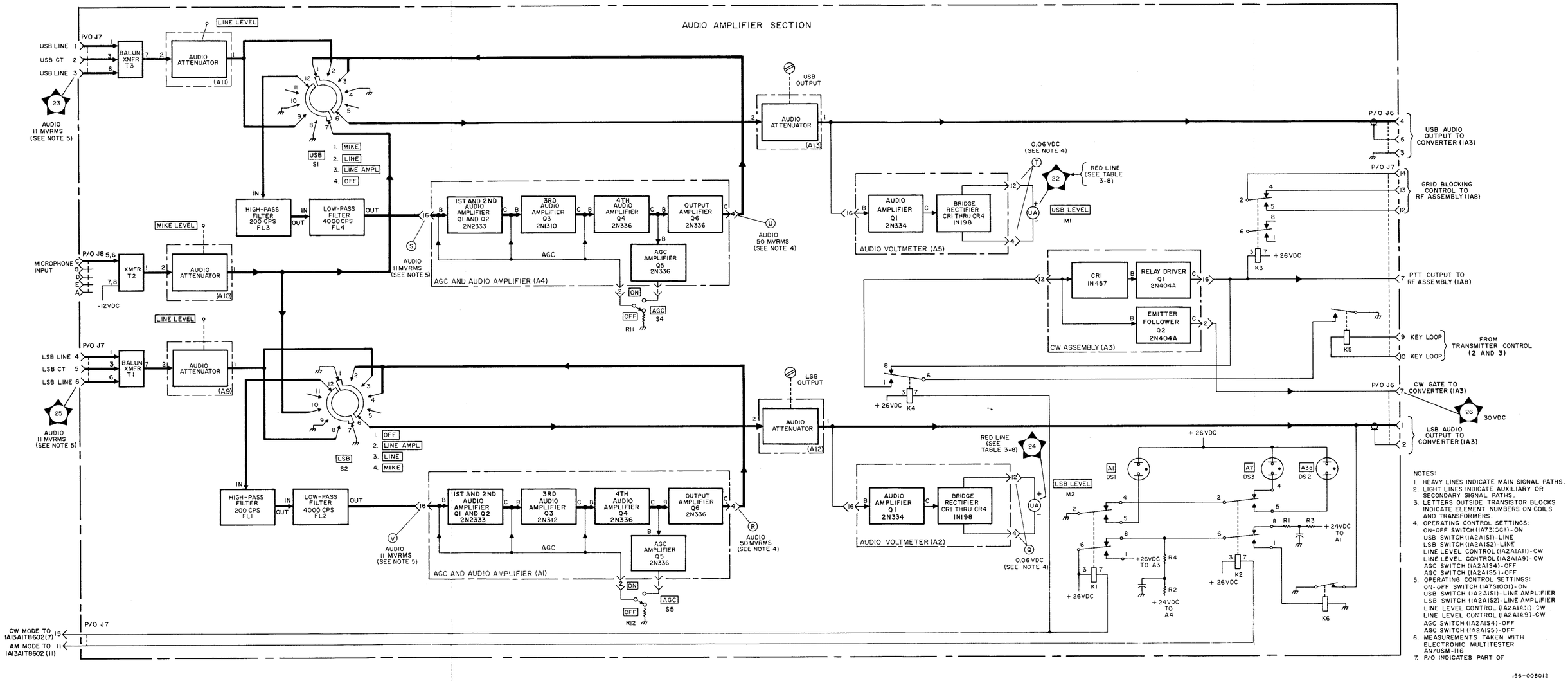


Figure 4-71. Amplifier 1A2, Servicing Block Diagram (Sheet 1 of 2)

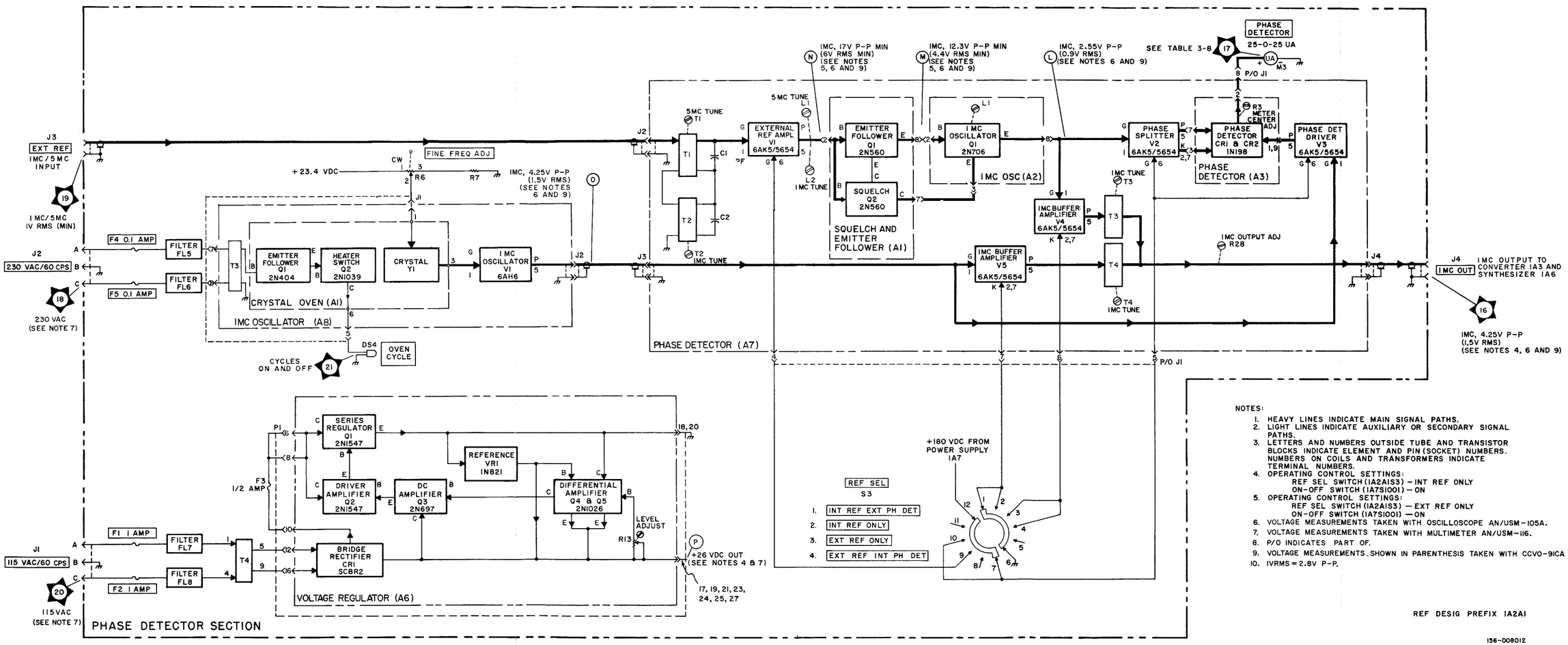
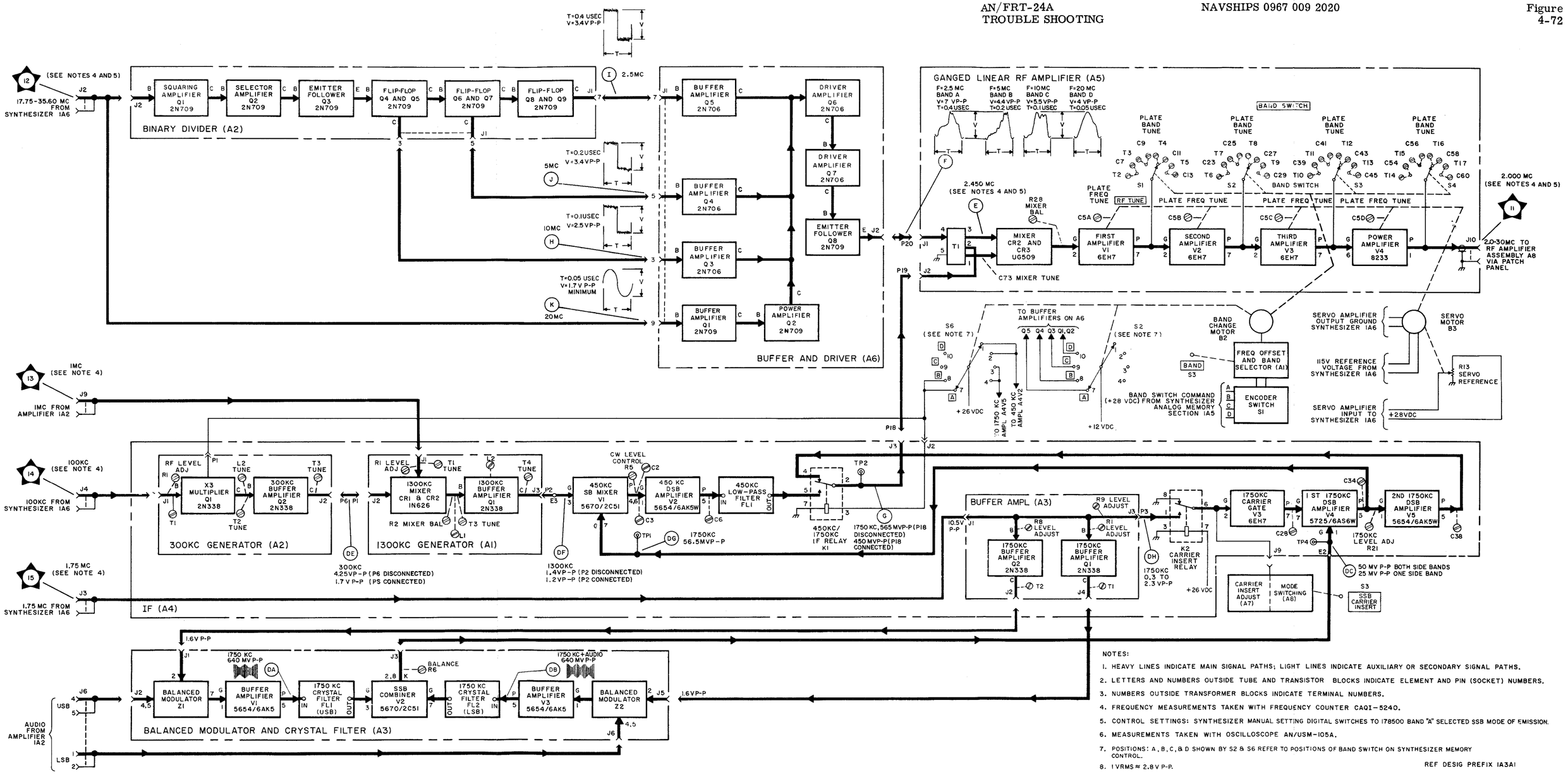


Figure 4-71. Amplifier 1A2, Servicing Block Diagram (Sheet 2 of 2)



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS AND NUMBERS OUTSIDE TUBE AND TRANSISTOR BLOCKS INDICATE ELEMENT AND PIN (SOCKET) NUMBERS.
3. NUMBERS OUTSIDE TRANSFORMER BLOCKS INDICATE TERMINAL NUMBERS.
4. FREQUENCY MEASUREMENTS TAKEN WITH FREQUENCY COUNTER CAQI-5240.
5. CONTROL SETTINGS: SYNTHESIZER MANUAL SETTING DIGITAL SWITCHES TO 178500 BAND "A" SELECTED SSB MODE OF EMISSION.
6. MEASUREMENTS TAKEN WITH OSCILLOSCOPE AN/USM-105A.
7. POSITIONS: A, B, C, & D SHOWN BY S2 & S6 REFER TO POSITIONS OF BAND SWITCH ON SYNTHESIZER MEMORY CONTROL.
8. 1 VRMS ≈ 2.8 V P-P.

REF DESIG PREFIX 1A3A1

156-008013

Figure 4-72. Converter 1A3, Servicing Block Diagram

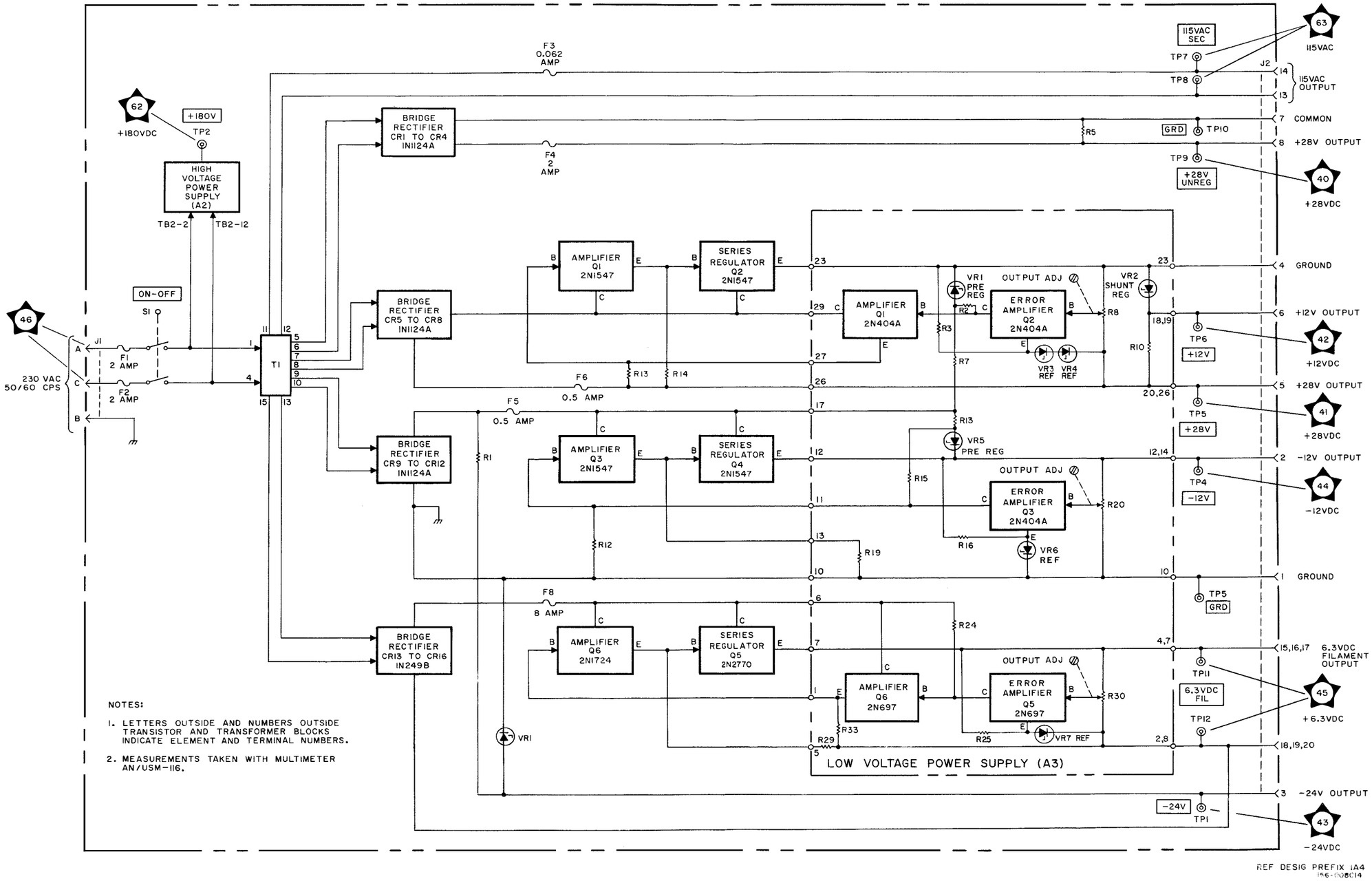


Figure 4-73. Synthesizer Power Supply 1A4, Servicing Block Diagram

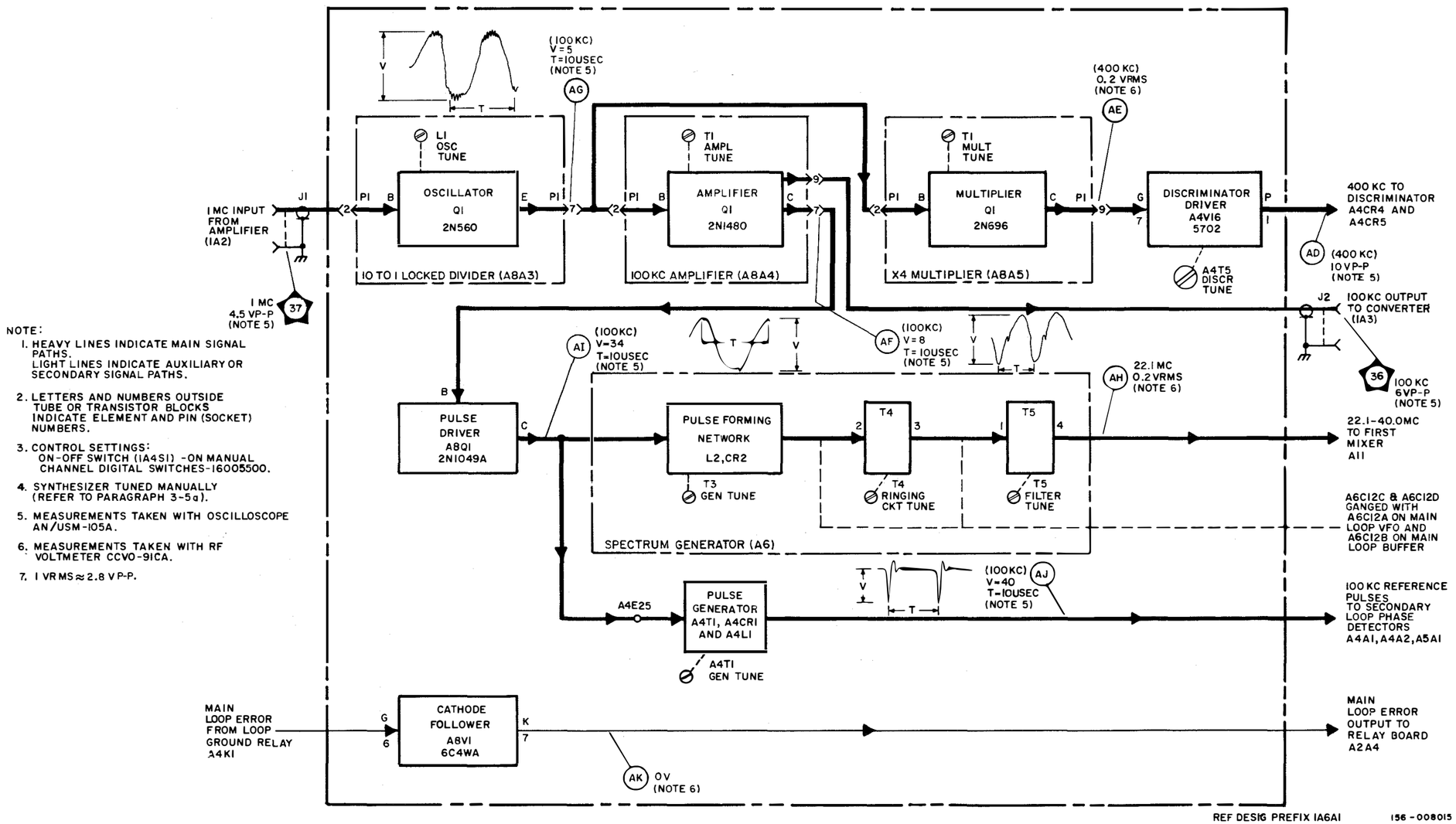


Figure 4-74. Synthesizer 1A6, Reference Circuits, Servicing Block Diagram

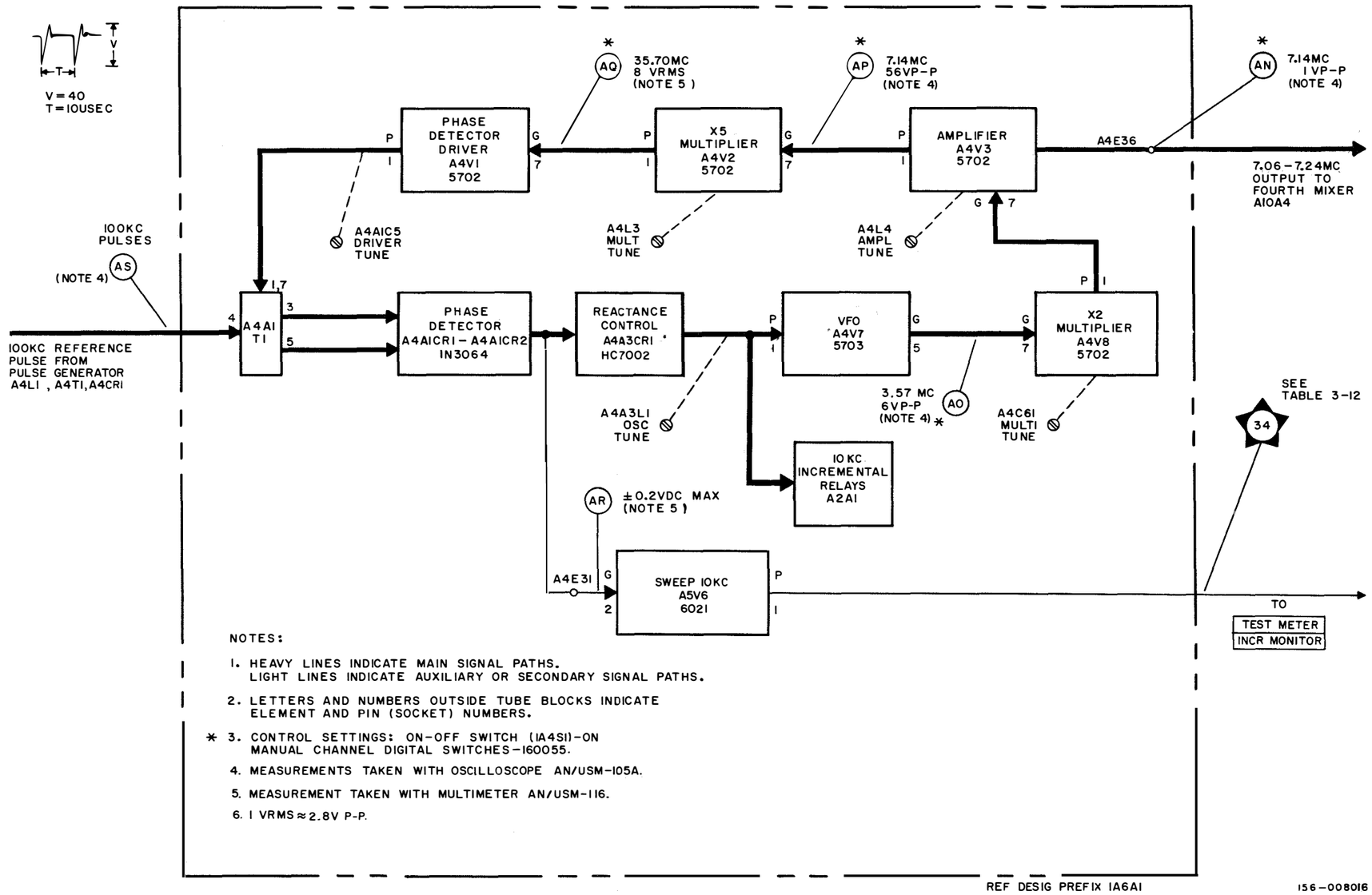
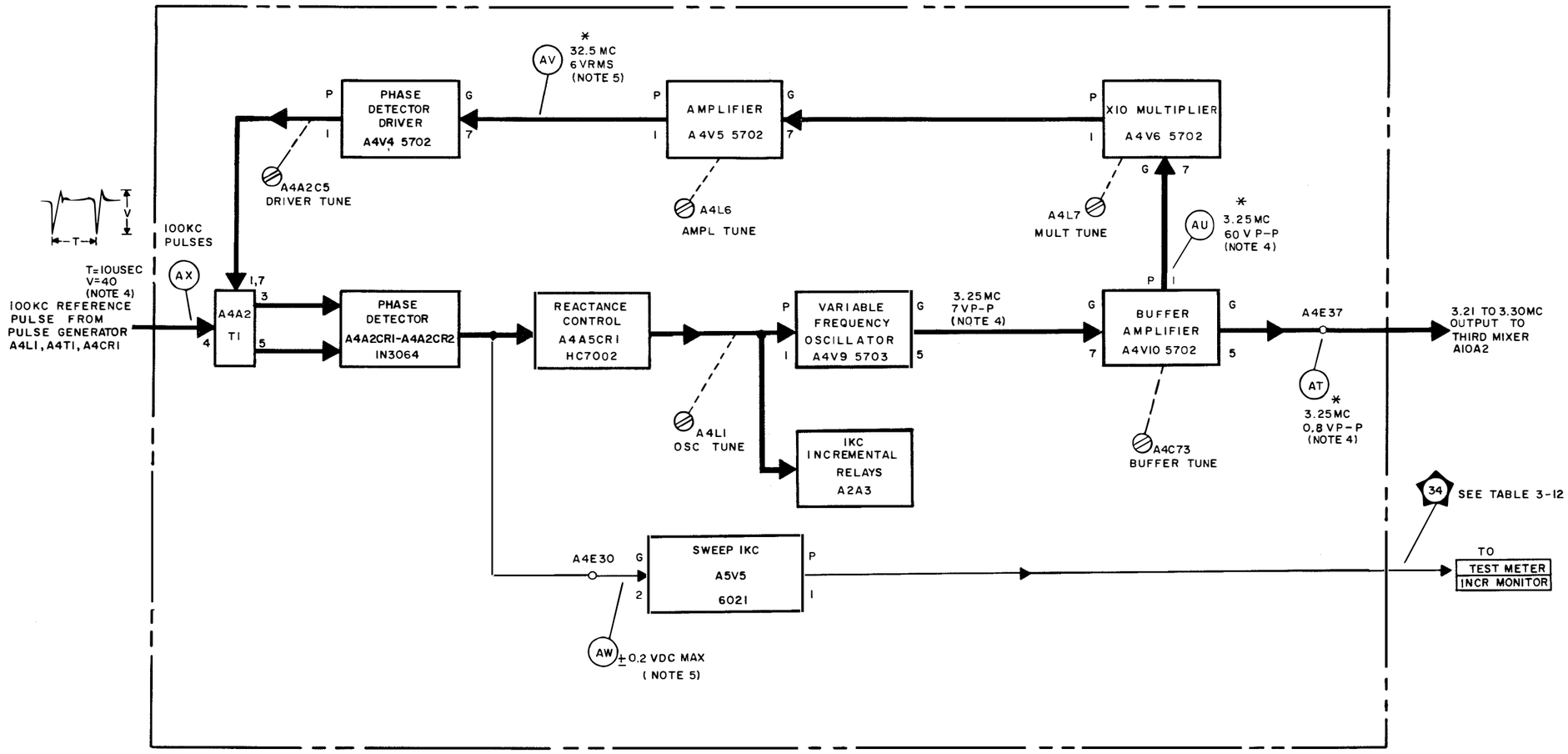


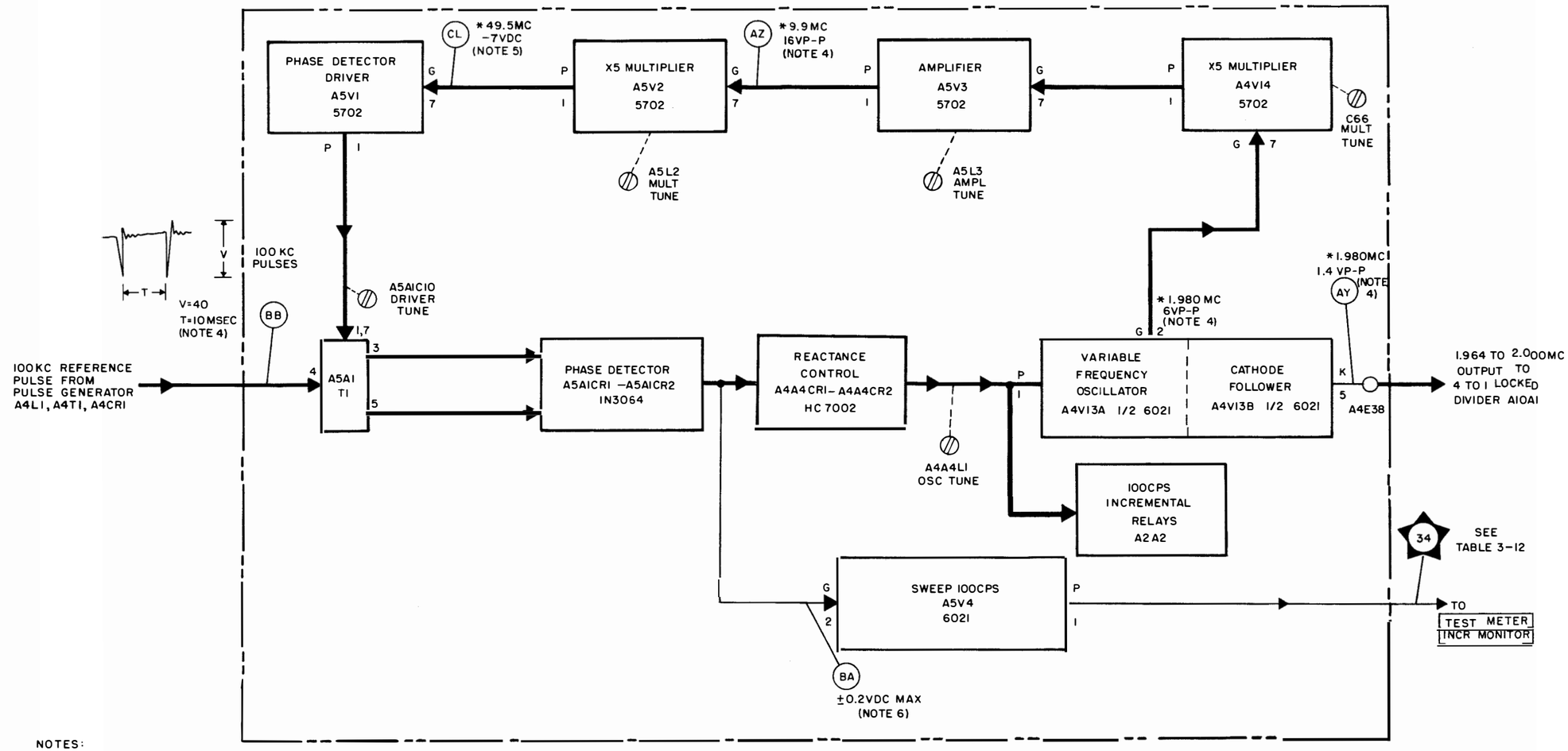
Figure 4-75. Synthesizer 1A6, 10-KC Loop Circuits, Servicing Block Diagram



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATH; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS AND NUMBERS OUTSIDE TUBE BLOCKS INDICATE ELEMENTS AND PIN (SOCKET) NUMBERS.
3. * CONTROL SETTINGS:
   ON-OFF SWITCH (1A4S1) ON.
   MANUAL CHANNEL DIGITAL SWITCHES 160055.
4. MEASUREMENTS TAKEN WITH OSCILLOSCOPE AN/USM-105A.
5. MEASUREMENTS TAKEN WITH MULTIMETER AN/USM-116.
6. 1 VRMS ≈ 2.8VP-P.

Figure 4-76. Synthesizer 1A6, 1-KC Loop Circuits, Servicing Block Diagram

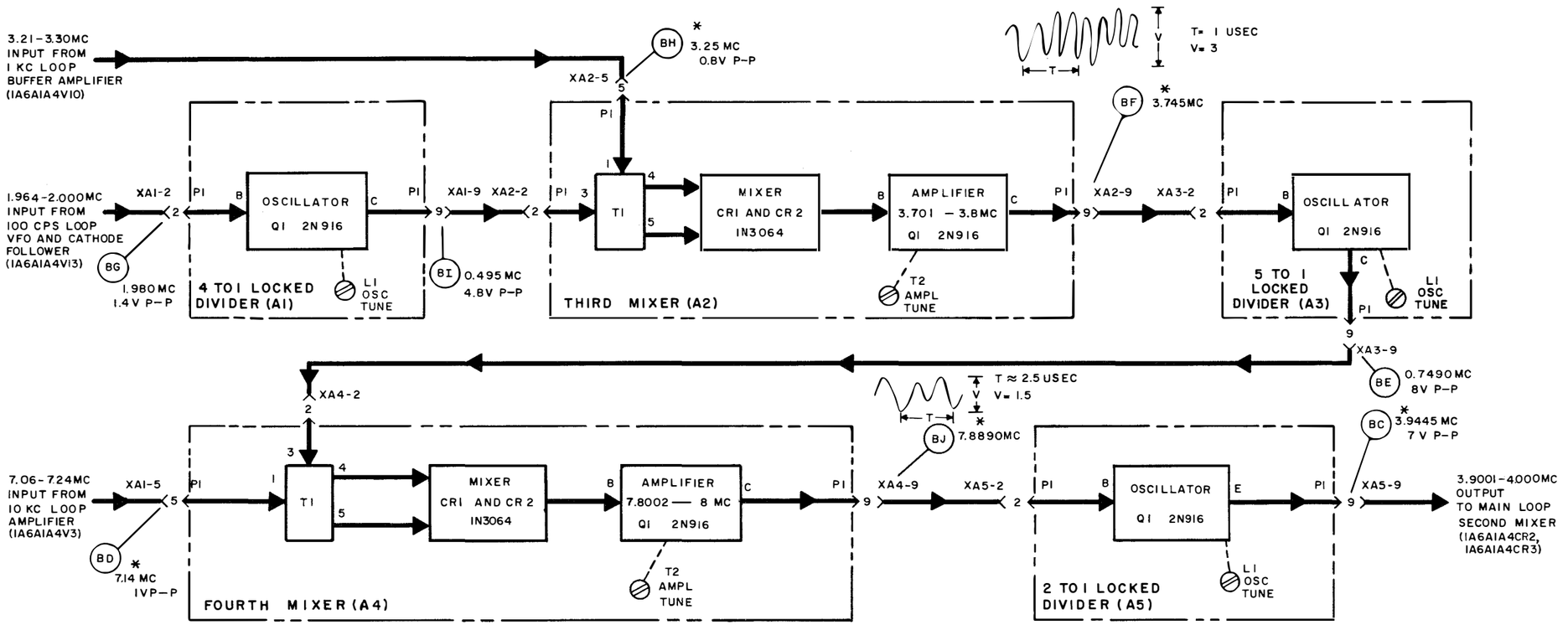


NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS, LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS AND NUMBERS OUTSIDE TUBE BLOCKS INDICATE ELEMENT AND PIN (SOCKET) NUMBERS.
*3. CONTROL SETTINGS:
   ON-OFF SWITCH (1A4S1)-ON
   MANUAL CHANNEL DIGITAL SWITCHES-160055.
4. MEASUREMENTS TAKEN WITH OSCILLOSCOPE AN/USM-105A.
5. MEASUREMENT TAKEN WITH MULTIMETER AN/USM-116 AND 1 MEGO DECOUPLING RESISTOR.
6. 1 VRMS ≈ 2.8 VP-P.

156-008018

Figure 4-77. Synthesizer 1A6, 100-Cycle Loop Circuits, Servicing Block Diagram



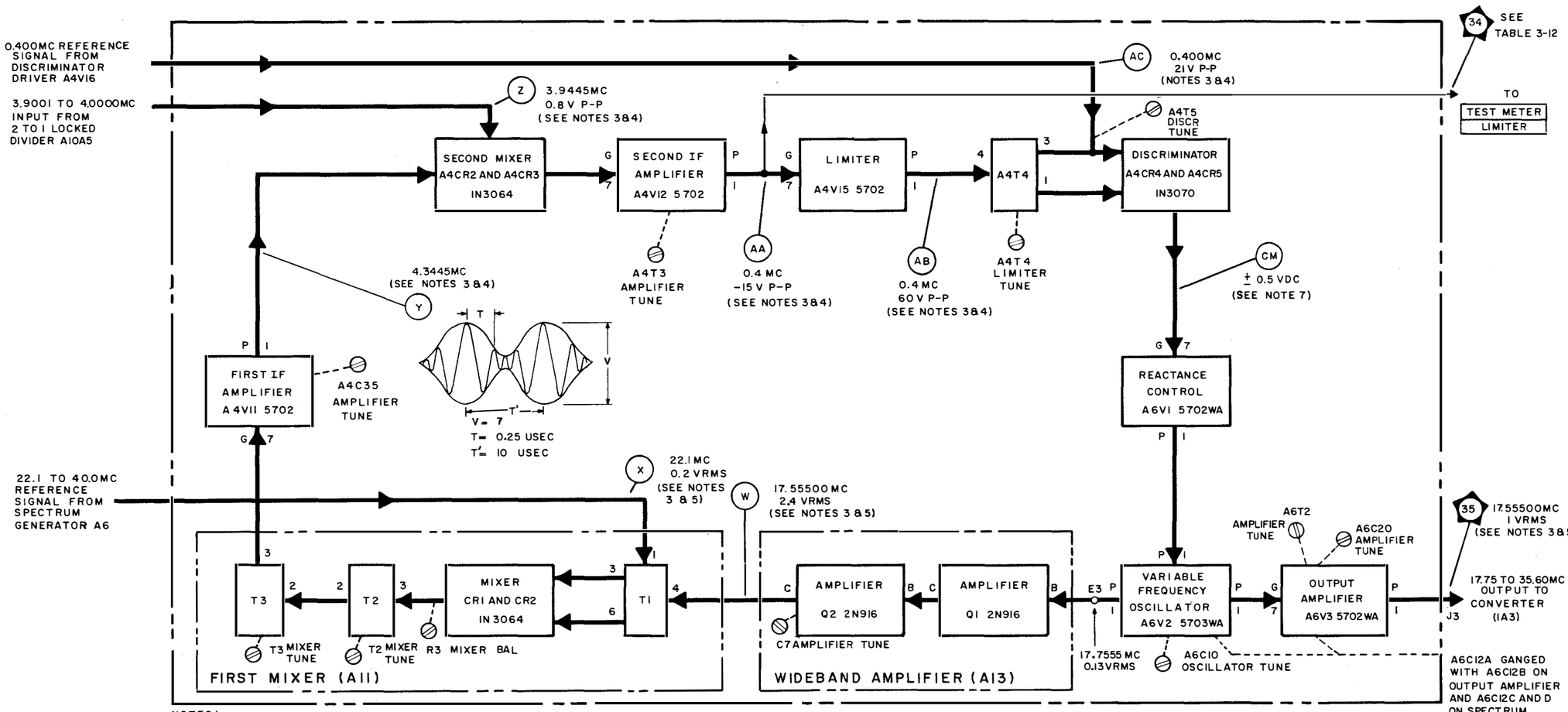
NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR BLOCKS INDICATE ELEMENTS.
3. * CONTROL SETTINGS:
   ON-OFF SWITCH (1A4S1) ON.
   MANUAL CHANNEL DIGITAL SWITCHES 160055.
4. MEASUREMENTS TAKEN WITH OSCILLOSCOPE AN/USM-105A.
5. 1 VRMS ≈ 2.8V P-P.

REF DESIG PREFIX 1A6A1A10

156-008019

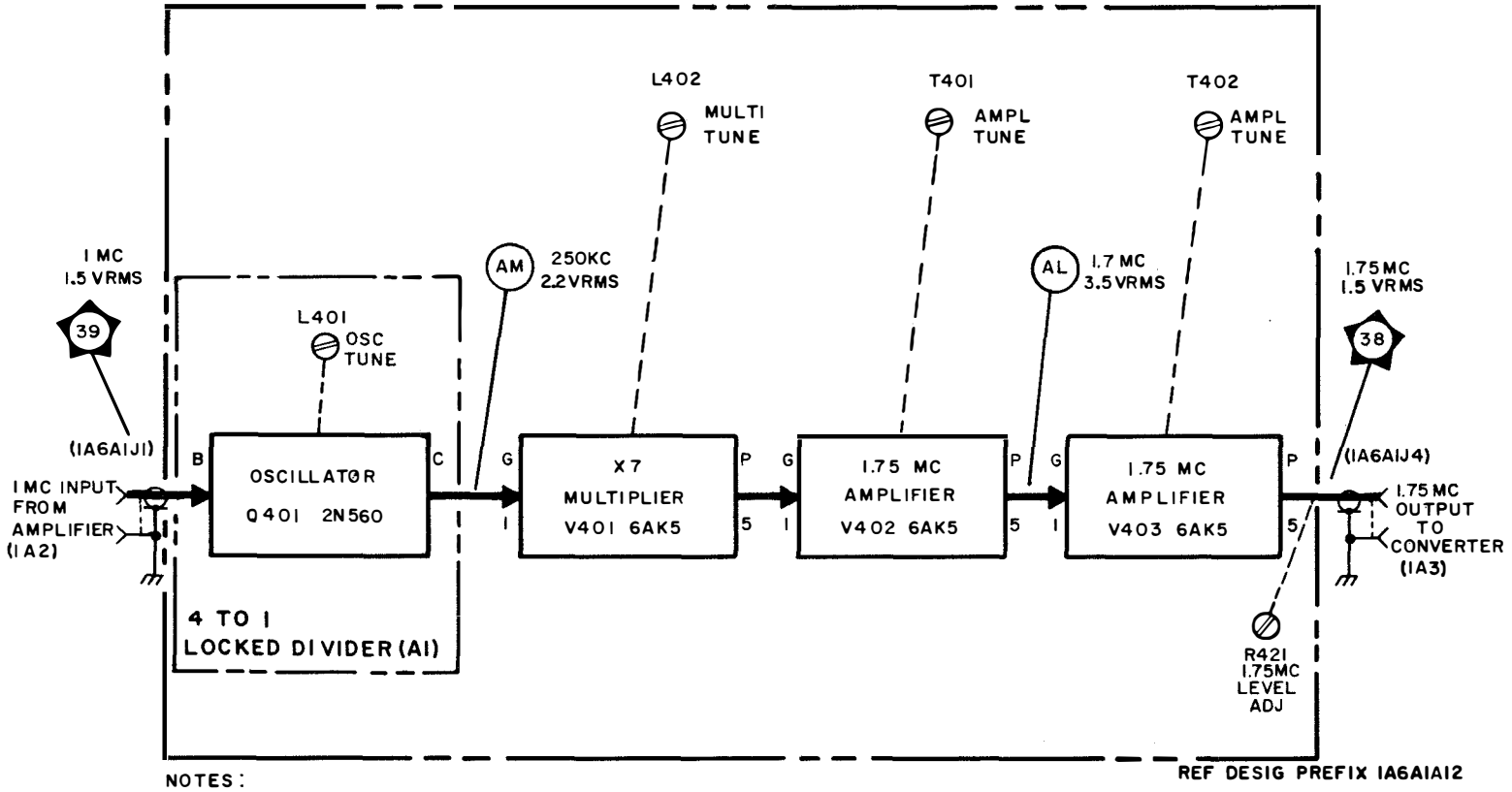
Figure 4-78. Synthesizer 1A6, Incremental Divider Circuits, Servicing Block Diagram



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS, LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS AND NUMBERS OUTSIDE TUBE BLOCKS INDICATE ELEMENT AND PIN (SOCKET) NUMBERS.
3. CONTROL SETTINGS:
   ON-OFF SWITCH (1A4S1) ON.
   MANUAL CHANNEL DIGITAL SWITCHES 200055.
   SWITCH MOTOR TO ON AND MOMENTARILY DEPRESS START BUTTON.
   AFTER TUNING CYCLE IS COMPLETED VOLTAGES MAY BE TAKEN.
4. MEASUREMENTS TAKEN WITH OSCILLOSCOPE AN/USM-105A.
5. MEASUREMENT TAKEN WITH RF VOLTMETER CCVO-91CA.
6. MEASUREMENT TAKEN WITH MULTIMETER AN/USM-116.
7. IVRMS≈2.8 VP-P

Figure 4-79. Synthesizer 1A6, Main Loop Circuits, Servicing Block Diagram

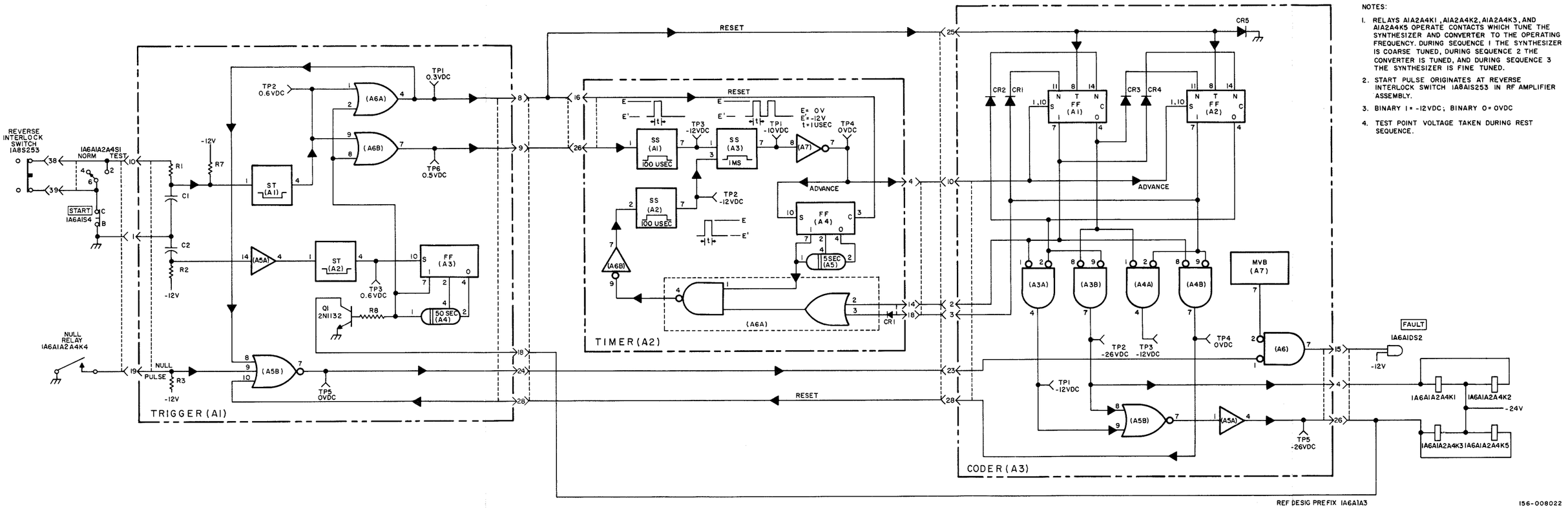


NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LETTERS OUTSIDE TRANSISTOR BLOCKS INDICATE ELEMENTS
2. CONTROL SETTING ON-OFF SWITCH (1A4S1)
3. MEASUREMENTS TAKEN WITH VOLTMETER AN/USM-116.
4. 1 VRMS ≈ 2.8 VP-P.

156-008021

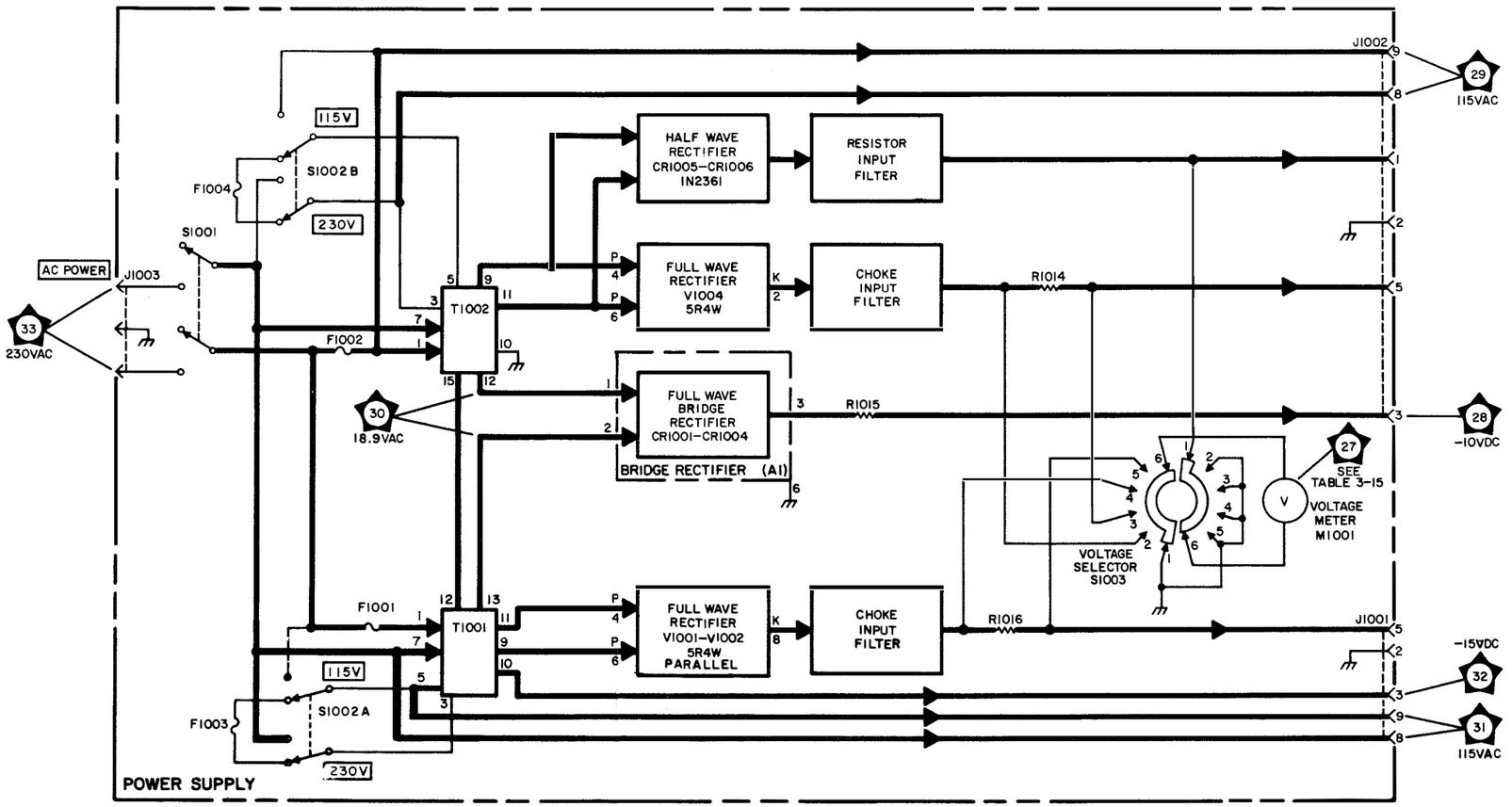
Figure 4-80. Synthesizer 1A6, 1.75 MC Assembly, Servicing Block Diagram



NOTES:

1. RELAYS A1A2A4K1, A1A2A4K2, A1A2A4K3, AND A1A2A4K5 OPERATE CONTACTS WHICH TUNE THE SYNTHESIZER AND CONVERTER TO THE OPERATING FREQUENCY. DURING SEQUENCE 1 THE SYNTHESIZER IS COARSE TUNED, DURING SEQUENCE 2 THE CONVERTER IS TUNED, AND DURING SEQUENCE 3 THE SYNTHESIZER IS FINE TUNED.
2. START PULSE ORIGINATES AT REVERSE INTERLOCK SWITCH 1A8A1S253 IN RF AMPLIFIER ASSEMBLY.
3. BINARY 1 = -12VDC; BINARY 0 = 0VDC
4. TEST POINT VOLTAGE TAKEN DURING REST SEQUENCE.

Figure 4-81. Synthesizer 1A6, Digital Timing Memory (Programmer), Logic Diagram



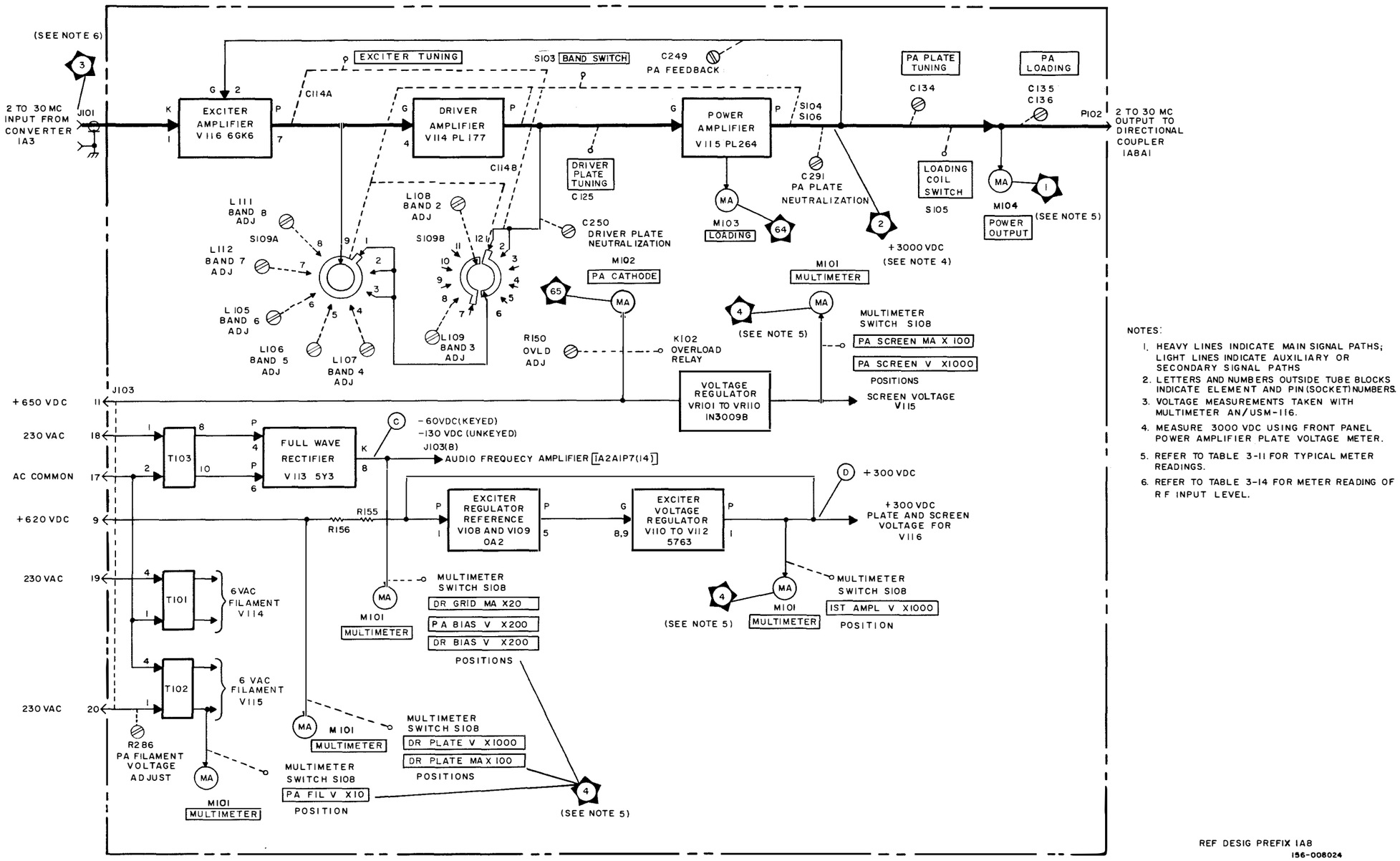
NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS AND NUMBERS OUTSIDE TUBE BLOCKS INDICATE ELEMENT AND PIN (SOCKET) NUMBERS. NUMBERS OUTSIDE TRANSFORMER BLOCKS INDICATE TERMINAL NUMBERS.
3. MEASUREMENTS TAKEN WITH ELECTRONIC MULTIMETER AN/USM-11C.

REF DESIG PREFIX 1A7

156-008023

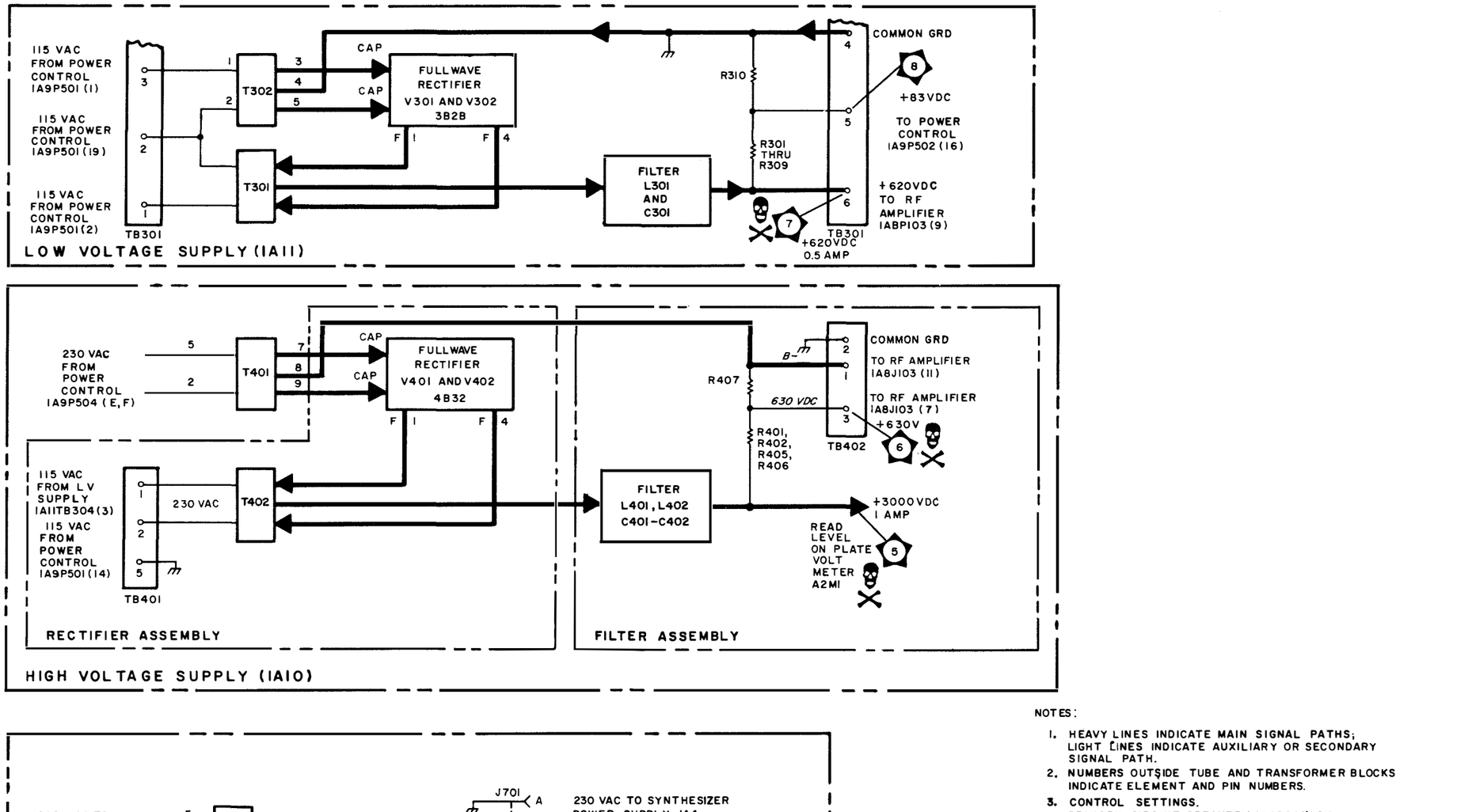
Figure 4-82. Exciter Power Supply 1A7, Servicing Block Diagram



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS
2. LETTERS AND NUMBERS OUTSIDE TUBE BLOCKS INDICATE ELEMENT AND PIN (SOCKET) NUMBERS.
3. VOLTAGE MEASUREMENTS TAKEN WITH MULTIMETER AN/USM-116.
4. MEASURE 3000 VDC USING FRONT PANEL POWER AMPLIFIER PLATE VOLTAGE METER.
5. REFER TO TABLE 3-11 FOR TYPICAL METER READINGS.
6. REFER TO TABLE 3-14 FOR METER READING OF R F INPUT LEVEL.

Figure 4-83. RF Assembly 1A8, Servicing Block Diagram



NOTES:

1. HEAVY LINES INDICATE MAIN SIGNAL PATHS; LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATH.
2. NUMBERS OUTSIDE TUBE AND TRANSFORMER BLOCKS INDICATE ELEMENT AND PIN NUMBERS.
3. CONTROL SETTINGS.
   PRIMARY CIRCUIT BREAKER (1A9CB501) ON
   PLATE SWITCH (1A9S503) ON
   FILAMENT SWITCH (1A9S502) ON
4. MEASUREMENTS TAKEN WITH MULTIMETER AN/PSM-4
5. SIGNIFIES DANGEROUSLY HIGH VOLTAGES EXIST KEEP CLEAR! USE EXTREME CARE WHEN MEASURING.

156-008025

Figure 4-84. Power Supplies 1A10, 1A11, and 1A12, Servicing Block Diagram

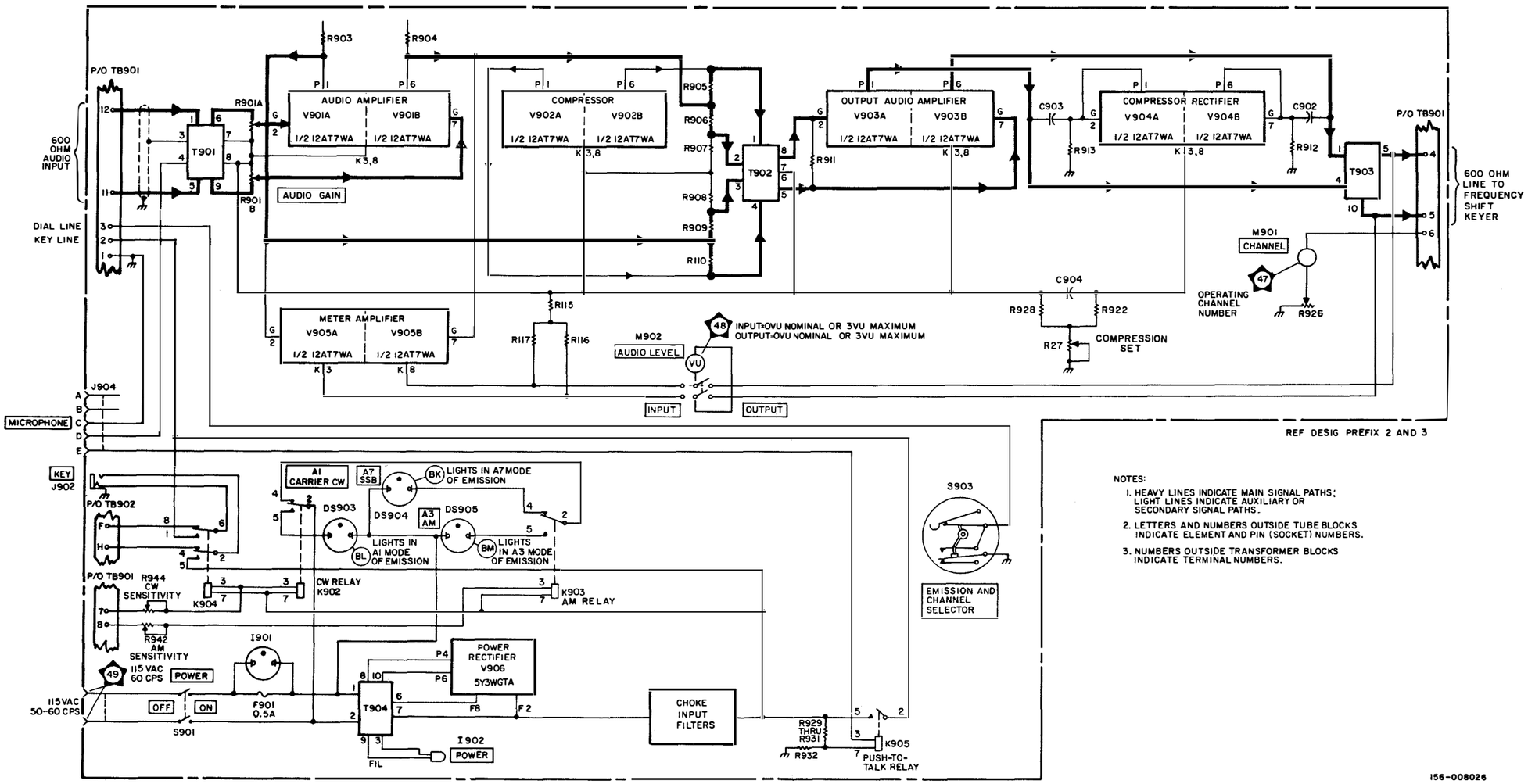
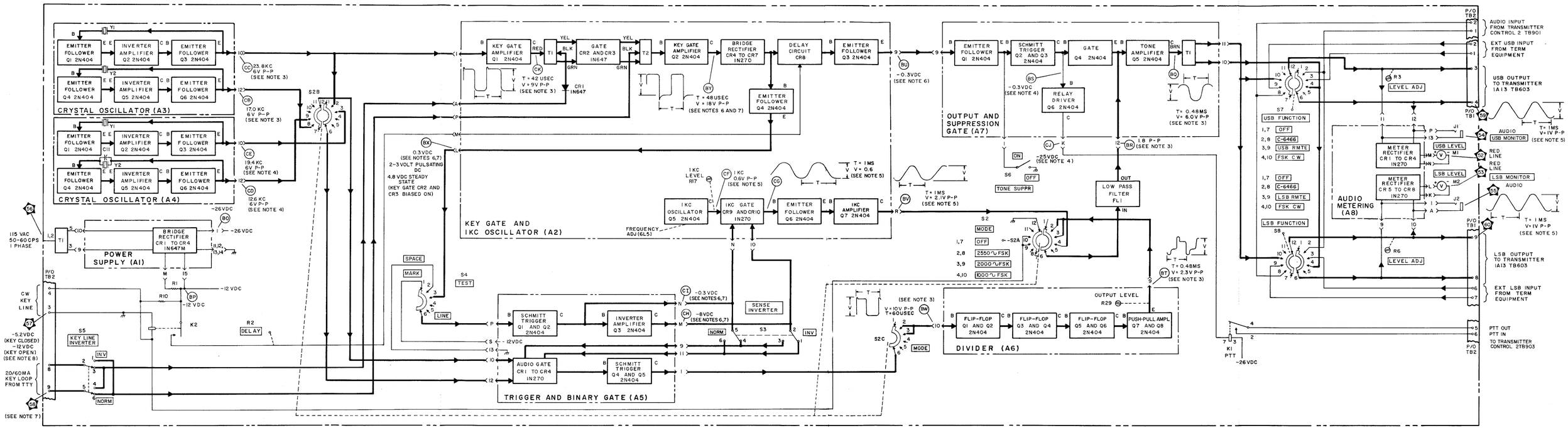


Figure 4-85. Transmitter Control 2 and 3, Servicing Block Diagram



NOTES:
1. HEAVY LINES INDICATE MAIN SIGNAL PATHS, LIGHT LINES INDICATE AUXILIARY OR SECONDARY SIGNAL PATHS.
2. LETTERS OUTSIDE TRANSISTOR BLOCKS INDICATE ELEMENTS NUMBERS ON COILS AND TRANSFORMERS INDICATE TERMINAL NUMBERS.
3. OPERATING CONTROL SETTINGS:
   MODE SWITCH (S2)-2550 ∿ FSK
   USB FUNCTION SWITCH (S7) FSK CW
   LSB FUNCTION SWITCH (S8) FSK CW
   USB LEVEL ADJ (R3) RED LINE ON M1
   LSB LEVEL ADJ (R6) RED LINE ON M2
   TONE SUPPR SWITCH (S6) ON
   TEST SWITCH (S4)-MARK
   DELAY CONTROL (R2) FULLY COUNTERCLOCKWISE.
4. OPERATING CONTROL SETTINGS:
   MODE SWITCH (S2) 2000 ∿ FSK
   USB FUNCTION SWITCH (S7) FSK CW
   LSB FUNCTION SWITCH (S8) FSK CW
   USB LEVEL ADJ (R3) RED LINE ON M1
   LSB LEVEL ADJ (R6) RED LINE ON M2
   TONE SUPPR SWITCH (S6) ON
   TEST SWITCH (S4) MARK
   DELAY CONTROL (R2) FULLY COUNTERCLOCKWISE
5. OPERATING CONTROL SETTINGS:
   MODE SWITCH (S2) 1000 ∿ CW
   USB FUNCTION SWITCH (S7) FSK CW
   LSB FUNCTION SWITCH (S8) FSK CW
   USB LEVEL ADJ (R3) RED LINE ON M1
   LSB LEVEL ADJ (R6) RED LINE ON M2
   TONE SUPPR SWITCH (S6) ON
   TEST SWITCH (S4) LINE
   DELAY CONTROL (R2) FULLY COUNTERCLOCKWISE
6. OPERATING CONTROL SETTINGS:
   MODE SWITCH (S2) 2000 ∿ FSK
   USB FUNCTION SWITCH (S7) FSK CW
   LSB FUNCTION SWITCH (S8) FSK CW
   USB LEVEL ADJ (R3) RED LINE ON M1
   LSB LEVEL ADJ (R6) RED LINE ON M2
   TONE SUPPR SWITCH (S6) ON
   TEST SWITCH (S4) LINE
   DELAY CONTROL (R2) FULLY COUNTERCLOCKWISE
7. TYPE LETTER "R" ON TELETYPEWRITER
8. OPERATE TELEGRAPH KEY.
9. OPERATE PUSH-TO-TALK SWITCH ON HANDSET.
10. EXPLANATION OF SYMBOLS PLACED AT WAVEFORMS
    V = PEAK VOLTAGE
    T = DURATION OF THE PORTION OF THE WAVEFORMS INDICATED.
11. WAVEFORMS RECORDED USING OSCILLOSCOPE AN/USM-105A.
12. P/O INDICATES PART OF.

Figure 4-86. Keyer 6, Servicing Block Diagram