KAM-143B/TSEC REGISTER Nº 1998

REPAIR AND MAINTENANCE INSTRUCTIONS FOR TSEC/KW-7 (FOUO)

Volume I—Description, Installation and Theory of Operation

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DEPARTMENT OF DEFENSE
NATIONAL SECURITY AGENCY
WASHINGTON 25, D. C.

April 1963

ORIGINAL

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Volume I—Description, Installation and Theory of Operation

LETTER OF PROMULGATION

1. This is a CONFIDENTIAL registered publication and will be handled, stored, and accounted for and destroyed in accordance with current regulations of the appropriate Department, Agency, or other controlling authority pertaining to registered cryptomaterial. Formal authorization for access to CONFIDENTIAL cryptomaterial is required for personnel to have access to this publication.

2. This publication will become effective upon receipt. Authorization for the eventual disposal of this publication will be issued at an appropriate time by the Director, National Security Agency.

3. Amendments to this publication will be promulgated by means of printed or electrically transmitted amendments. Individuals entering such amendments shall so indicate on the "Record of Amendments" page included herein as page 5.

4. This publication is distributed to authorized holders of TSEC/KW-7.

5. THIS PUBLICATION CONTAINS INFORMATION AFFECTING THE NATIONAL DEFENSE OF THE UNITED STATES WITHIN THE MEANING OF THE ESPIONAGE LAWS, TITLE 18, U.S.C., SECTIONS 793, 794, AND 798. ITS TRANSMISSION OR THE REVELATION OF ITS CONTENTS IN ANY MANNER TO AN UNAUTHORIZED PERSON IS PROHIBITED BY LAW.

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7. This publication may not be carried in aircraft for use therein.

Gordon A. Blake
GORDON A. BLAKE
Lieutenant General, USAF
Director

LIST OF EFFECTIVE PAGES

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GENERAL INFORMATION ON RECENT EQUIPMENT CHANGES

Several recent changes were made to the TSEC/KW-7 that were not incorporated into the original printing of the repair and maintenance instructions for the TSEC/KW-7. These changes are listed here for information purposes. They will be incorporated into the appropriate volume of the repair and maintenance instructions in the first amendment thereto.

1. A special medium-speed flip-flop has been substituted for medium speed flip-flop 1A7MD21.
2. The Loop-Inhibit/Allow switch has been removed and a red strap wire has been added between XA11-D and XA11-N. This will only affect the KW-7 during Two-Wire Loop Adapter (KWL-4) operation. This strap will have to be removed to permit the KWL-4 to be used.
3. Some wiring has been changed in the Loop Output Circuit located on Relay Assembly A18. Also a 1 millihenry choke has been added.
4. The output of the Time Standard (E-AJY) has been changed from a 7 volt peak-to-peak square wave to a 2 volt rms sine wave.

RECORD OF AMENDMENTS

Identification of Amendment and Reg. No. (if any)	Date Entered	By Whom Entered (Signature; Rank or Rate; Name of Command)

RECORD OF PAGE CHECKS

Date Checked	By Whom Checked (Signature; Rank or Rate; Name of Command)	Date Checked	By Whom Checked (Signature; Rank or Rate; Name of Command)
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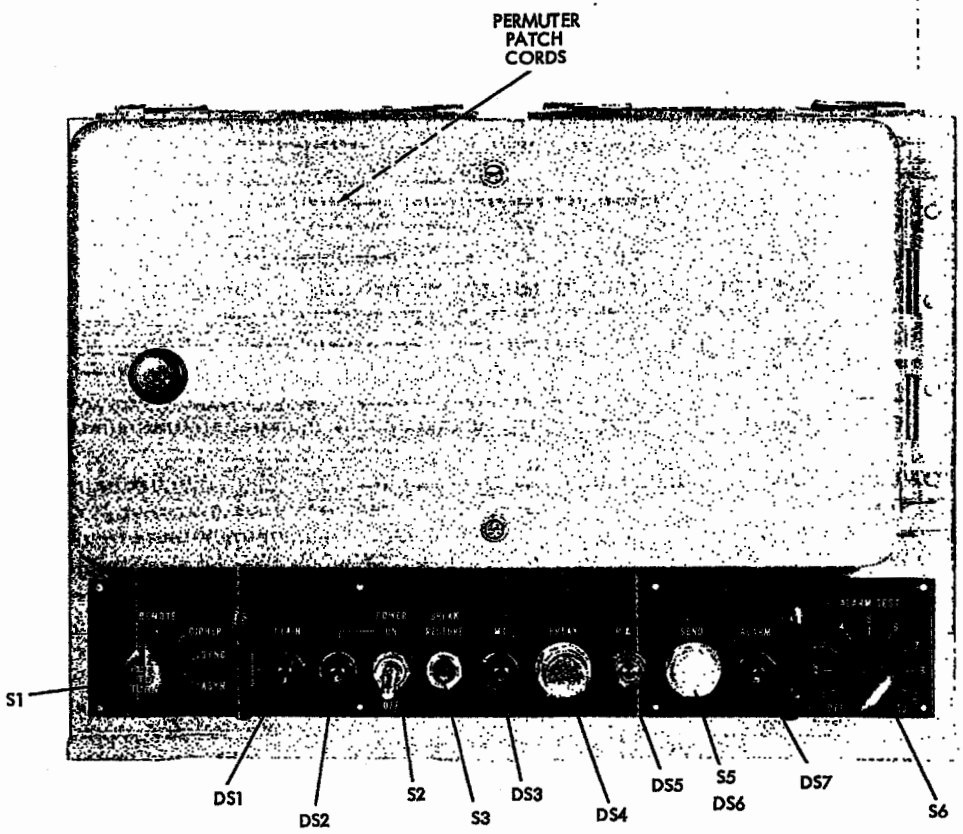


Figure 1-1.—KW-7 Main Assembly.

CHAPTER 1

INTRODUCTION AND CLASSIFICATIONS

1000—INTRODUCTION

1001. Contents.—This book is Volume I of three volumes containing repair and maintenance information for the TSEC/KW-7 Electronic Tactical Teletypewriter Security Equipment (fig. 1-1). It also contains information about the following special-purpose ancillary units designed to operate with the TSEC/KW-7: Remote Control Unit, Functional Remote Control Unit, and the Two-Wire Loop Adapter (fig. 1-2).

Short Title	*Long Title*
KAM-143B/TSEC	Repair and Maintenance Instructions for TSEC/KW-7 (FOUO)—(Volume I—Description, Installation, and Theory of Operation).
KAM-144B/TSEC	Repair and Maintenance Instructions for TSEC/KW-7 (FOUO)—(Volume II—Preventive Maintenance, Troubleshooting, and Diagrams).
KAM-145A/TSEC	Repair and Maintenance Instructions for TSEC/KW-7 (FOUO)—(Volume III—Illustrated Parts Lists).

Personnel maintaining the TSEC/KW-7 will need these three publications. A fourth publication, KAM-146A/TSEC, "Limited Repair and Maintenance Instructions for TSEC/KW-7", is a special-purpose document designed for personnel who will be authorized to perform limited maintenance.

1002. Operating Instructions.—Operating instructions for the TSEC/KW-7 are contained in the effective edition of KAO-83/TSEC. Maintenance personnel should familiarize themselves with this publication.

1003. Qualifications for Maintenance Personnel.—No persons will attempt to perform repair and maintenance work on the TSEC/KW-7 unless they have successfully completed an approved course of instruction in the maintenance of the equipment.

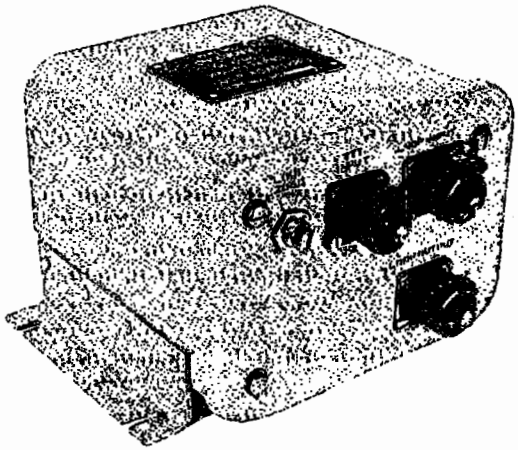
1004. Modification of Equipment.—No modification will be made to the TSEC/KW-7 without prior authorization by the Director, National Security Agency. Correspondence pertaining to modification of the TSEC/KW-7 should be forwarded through proper Service or Agency channels to Assistant Director, NSA, for Communications Security, National Security Agency, 3801 Nebraska Ave., N.W., Washington 25, D.C., ATTN: S2. The modification instructions (KABs) which have been issued by the National Security Agency for the TSEC/KW-7 are listed on the last page of chapter 2.

1005. Terminology.—At various places in this manual, the equipment is referred to either as the TSEC/KW-7 or simply as the KW-7. Some of the short title nomenclature has been dropped for the sake of brevity. It should be understood that all such references mean the production TSEC/KW-7 equipment.

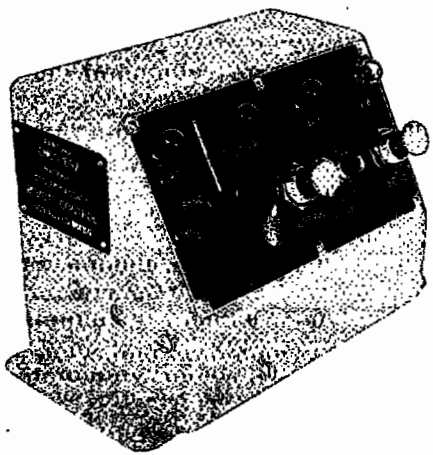
1006. Comments and Recommendations.—Comments and recommendations regarding the KW-7 equipment or the contents of this book are invited. Such comments and recommendations

should be forwarded through normal Service or Agency channels to the Assistant Director NSA, for Communications Security, National Security Agency, 3801 Nebraska Ave., N.W., Washington 25, D.C., ATTN: S2.

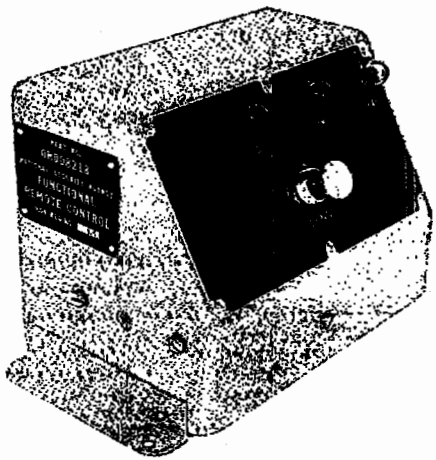
For Army Accounts: Comments regarding this manual or the equipment will be forwarded through channels to the Commanding Officer, U.S. Army Signal Communications Security Agency, Arlington Hall Station, Arlington 12, Virginia, ATTN: SIGCR-4.



Two-Wire Loop Adapter



Remote Control Unit



Functional Remote Control Unit

Figure 1-2.—Remote Control Unit, Loop Adapter Unit, and Functional Remote Control Unit.

1100—SECURITY CLASSIFICATIONS

1101. Classification of KAM-143B/TSEC.—This book is a registered publication and is classified ~~CONFIDENTIAL—CRYPTO.~~ Formal authorization for access to CONFIDENTIAL cryptomaterial is required for personnel to have access to this publication.

1102. Classification of KW-7.—The KW-7 is classified CONFIDENTIAL—CRYPTO.

a. Formal authorization for access to CONFIDENTIAL cryptomaterial is required for:
(1) Internal viewing.
(2) External viewing with permuter cover removed.
(3) Access to maintenance and operating instructions.

b. The KW-7 may be viewed externally by uncleared personnel provided that:
(1) They are escorted by properly cleared personnel.
(2) The equipment is closed and the permuter cover is attached.
(3) Attention is not directed to the equipment or its function.

Note: Photographs of the KW-7 with the permuter cover in place should be marked "FOR OFFICIAL USE ONLY". All other information concerning crypto-equipments and cryptosystems are government information, "FOR OFFICIAL USE ONLY", and shall not be revealed to any greater extent than operationally necessary. Equipments and systems should not be publicly exhibited or discussed, nor should information be released to the press or other news media.

1103. Classification of Components.—The KW-7 consists of the following components which are classified as shown:

Trigraph Designator	Classification
E-AJJ	CONFIDENTIAL—CRYPTO
E-AJK	CONFIDENTIAL—CRYPTO
E-AJL	CONFIDENTIAL—CRYPTO
E-AJM	CONFIDENTIAL—CRYPTO
E-AJN	UNCLASSIFIED
E-AJO	CONFIDENTIAL—CRYPTO
E-AJP	UNCLASSIFIED
E-AJQ	UNCLASSIFIED
E-AJR	UNCLASSIFIED
E-AJS	UNCLASSIFIED
E-AJT	UNCLASSIFIED
E-AJU	UNCLASSIFIED
E-AJV	CONFIDENTIAL—CRYPTO
E-AJW	UNCLASSIFIED
E-AJX	UNCLASSIFIED
E-AJY	UNCLASSIFIED
E-AJZ	UNCLASSIFIED

1104. Safeguarding the Equipment.—The KW-7 and its associated equipment will be handled and accounted for in accordance with the regulations of each Service or Federal Agency governing the handling of registered cryptomaterial. Specific requirements for the safeguarding of cryptomaterial are contained in the effective editions of KAG-1/TSEC, KAG-8/TSEC, and KAG-9/TSEC.

CHAPTER 2

DESCRIPTION OF EQUIPMENT

2000—FUNCTIONAL DESCRIPTION

2001. General.—The KW-7 (fig. 1-1) is a portable ~~cryptographic device~~ CRYPTO-EQUIPMENT capable of operation either synchronously for on-line tactical point-to-point or netted teletypewriter communications or asynchronously for communicating directly with teletypewriter equipment. The form of communication between stations is manually selected to be either plain text or cipher text. With plain operation selected, information is transmitted and received in plaintext form. In cipher operation, however, the KW-7 enciphers plaintext characters received from a teletypewriter keyboard or transmitter-distributor by combining them with the key stream output of its key generator. The resulting cipher text output is in 7.0 or 7.42 baud teletypewriter form. It is then transmitted over wire lines or by a radio link to other cryptographically compatible KW-7 equipped stations in the communications system without revealing the message contents to other than the intended parties. A receiving KW-7 receives the input teletypewriter signal, converts it to data for internal processing and by a decryption process cancels the key signal added at the transmitting site. The resultant plain text is copied on a teletypewriter page printer. Major sections of the KW-7 are the input section, extensor and control section, key generator section, alarm section, output section, and timing generator section. Ancillary equipment provided for special-purpose use of the KW-7 include a remote control unit, a functional remote control unit, and a two-wire loop adapter unit, (fig. 1-2).

2002. Equipment Required.—A secure communications system requires at least two KW-7's—one at each end of the transmission link. Each KW-7 is capable of transmitting or receiving information, but not simultaneously. Placing two KW-7's at each station permits full-duplex operation; that is, the simultaneous transmission and reception of information.

2003. KW-7 Function.—Figure 2-1 illustrates a simplified block diagram of two KW-7's in operation. The functional description of the equipment is as follows:

a. Input Section.

(1) The loop input section is the portion of the KW-7 that accepts input signals in either the 7.0 or the 7.42 baudot code at nominal speeds of 60, 67, and 100 words per minute (45, 50, and 75 baud modulation rates respectively) from standard teletypewriter devices and converts these binary signals into levels that can be processed by the system.

(2) The line input section accepts 7.0 baudot code from the line at 60, 67, or 100 words per minute and converts these binary signals into levels that can be processed by the system.

b. Extensor and Control Section.—The extensor and control section retimes the asynchronous signal inputs from the teletypewriter devices to the synchronous KW-7 timing. This retiming is necessary so that the KW-7 start pulse and the input information pulse transitions will occur exactly in step with the timing pulses which are generated within the KW-7 control sections.

c. Key Generating Section.—The key generating section is responsible for the security of the system. The key signal generated by this section is a two-level signal containing many transitions from one level to another. The distribution of high and low levels in the key signal is of a random nature. The key signal generated by one KW-7 is duplicated by

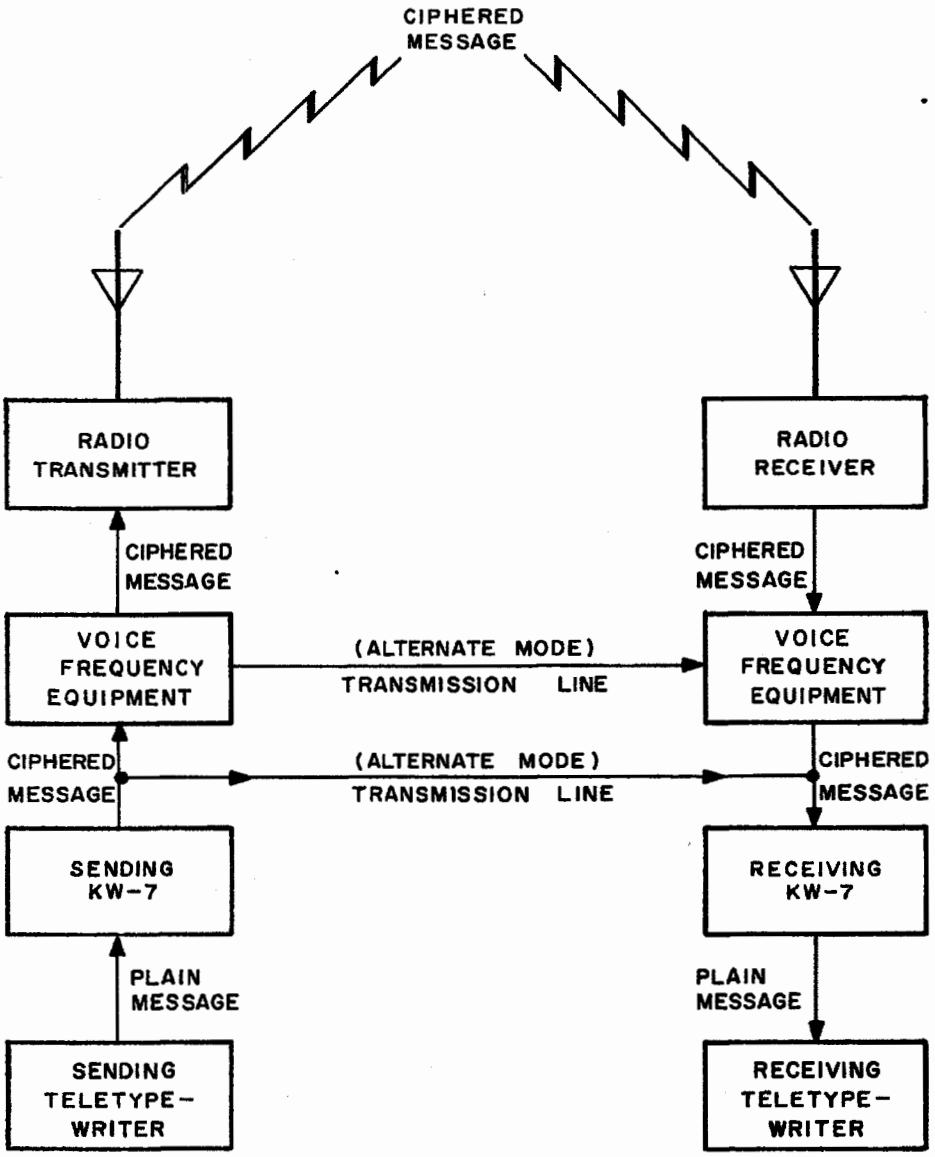


Figure 2-1.—Half-Duplex Operation.

another KW-7 when the two equipments are interconnected through some form of communications link and have their permuter patch cords wired in identical configurations in agreement with a key list.

d. Alarm Section.—The alarm section is that portion of the KW-7 which monitors various portions of the key generator. In the event of a malfunction within the key generator, transmission is stopped and the operator is notified by both an audible alarm and an indicator lamp that such a condition exists.

e. Output Section.—The output section is that portion of the KW-7 which converts the data information to binary information signals for transmission to a receiving KW-7 and to the transmitting KW-7's page printer.

f. Timing Generator Section.—The timing generator section provides a crystal-controlled time reference to the other sections for synchronizing their operations.

g. Remote Control Unit.—The KW-7 is provided with a remote control unit which allows the KW-7 to be operated at a position up to a maximum of 500 feet away. The remote control unit contains a complete set of parallel controls, indicators, and signal input/outputs necessary for remote operation of the KW-7.

h. Functional Remote Control Unit.—The functional remote control unit provides the KW-7 with a limited set of parallel controls and indicators by which it may be operated at a location up to 500 feet away. When the Functional Remote Control Unit is used, the KW-7 can be operated in cipher mode only.

i. Two-Wire Loop Adapter Unit.—The two-wire loop adapter unit is supplied with the KW-7 when it is necessary to convert a four-wire loop input/output circuit to a two-wire loop input/output circuit. This unit is used in a limited number of special applications.

2004. Key Formation.—The KW-7 uses permuter patch cords to determine which outputs of the key generator will be used for combining to form key. The arrangement of the patch cords controls the overall pattern of the key signal. In regular operational use, patch cords are normally changed daily. The use of a different key signal each day increases the security of the system.

2005. Types of Operation.—The KW-7 may be used in either of two operations: half-duplex or full-duplex. The following subparagraphs describe each operation and some possible combinations which may be used.

a. Half-Duplex Operation (fig. 2-1).—When the KW-7 is connected for half-duplex operation either station can transmit or receive information, but not both simultaneously. Two typical types of operation using the half-duplex system are two-station and multi-station. The two-station operation provides communication between two stations; the multi-station operation permits communication throughout a net (more than two stations).

b. Full-Duplex Operation (fig. 2-2).—When the KW-7 is operating in the full-duplex operation, two units are located at each station to permit simultaneous transmission and reception.

2006. Modes of Operation.—The KW-7 can be operated in one of two modes: plain or cipher. The following subparagraphs describe the operation of the KW-7 in each mode.

a. Plain Mode of Operation.—In the plain mode of operation, the KW-7 may operate either plain synchronous or plain asynchronous.

(1) *Plain synchronous operation.*

(a) *Transmit operation.*—During plain synchronous operation, the KW-7 accepts either 7.0 or 7.42 baudot code loop inputs (real-time) from a teletypewriter key-

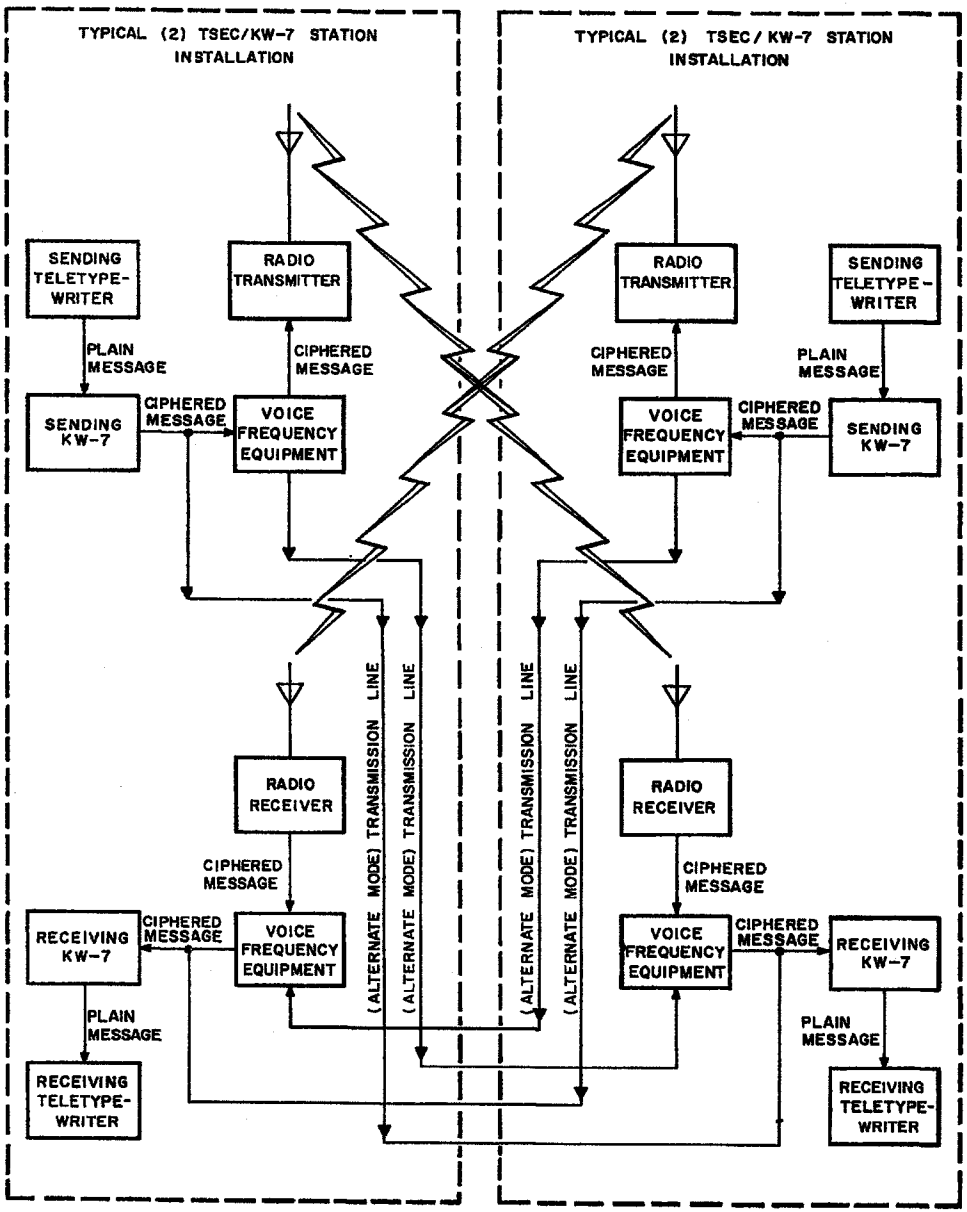


Figure 2-2.—Full-Duplex Operation.

board or a transmitter-distributor. The 7.0 or 7.42 code is retimed (real-time converted to system-time) with the internal KW-7 timing and the resulting 7.0 code is fed to the line output circuit for transmission to another KW-7 and to the loop output circuit. The information from the loop output circuit is printed out on the transmitting KW-7's page printer (home copy).

(b) *Receive operation.*—The receiving KW-7 accepts the 7.0 baudot code transmitted by the transmitting KW-7 at its line input circuit. This 7.0 code is examined within the KW-7 and then fed to the loop output circuit where it is printed out on the receiving KW-7's page printer.

(2) *Plain asynchronous operation.*

(a) *Transmit operation.*—Transmit operation of the KW-7 in the plain asynchronous mode is the same as that discussed for plain synchronous operation.

(b) *Receive operation.*—The receiving KW-7 line input circuit accepts 7.42 teletypewriter signals directly from teletypewriter equipment and routes the information to the receiving page printer.

b. Cipher Mode of Operation.

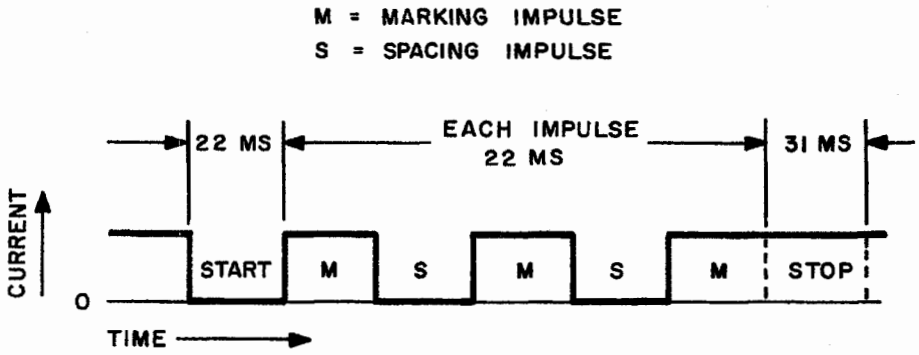
(1) *Transmit operation.*—During cipher operation the KW-7 accepts either 7.0 or 7.42 baudot code loop inputs from a teletypewriter keyboard or transmitter-distributor. The data inputs are retimed within the extensor and control section to form a 7.0 code that is combined with the key generator signal to produce the cipher text. This cipher text is converted to teletypewriter signals by the output circuit for transmission to other KW-7 equipped stations. The loop input signals, in addition to being supplied to the extensor and control section, are fed directly to the loop circuit where they are printed out on the page printer as plain text (home copy).

(2) *Receive operation.*—A receiving KW-7 accepts 7.0 baudot code data at its line input circuit. This data, the cipher text sent from the transmitting station, is examined by the extensor and control section to ascertain that a message is being received and, if so, processed through the key generator section where the information is decrypted by canceling the key signal added at the transmitting KW-7. The resultant plain text is supplied to the loop output circuit where it is printed out on the receiving page printer.

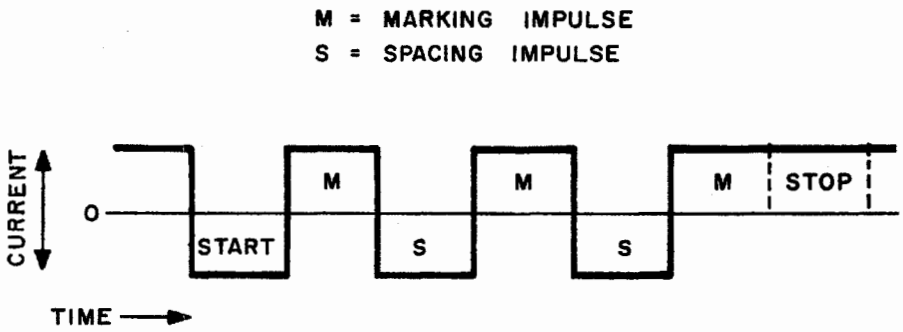
2007. Types of Transmission.—The KW-7 equipment has provisions for two types of transmission: dc land-line teletypewriter transmission or radio transmission. The following subparagraphs briefly describe each type of transmission.

a. DC Land-Line Transmission.—In direct-current land-line teletypewriter transmission, the output of the sending unit is routed through a transmission line directly to the receiving unit. The KW-7 can operate on either neutral or polar type of line operation. In neutral operation, current flows in one direction only. Marking impulses are current impulses, and spacing impulses are non-current impulses. In polar operation, current flows in both directions. Marking impulses are current impulses in one direction; spacing impulses are current impulses in the opposite direction.

Note: Figure 2-3 illustrates nominal signals for both neutral and polar operation. It should be understood that start (space) signal (mark and space) and stop (mark) durations for each type will vary in proportion to the teletypewriter speed; i.e., the baud period for 60 words-per-minute operation is greater than that for 100 words-per-minute operation. Table 2-1 defines the individual length for the various bauds at teletypewriter speeds with 7.42 baudot code.



A. NEUTRAL SIGNAL FOR LETTER Y AT 60 WPM



B. POLAR SIGNAL FOR LETTER Y AT 60 WPM

Figure 2-8.—Teletypewriter Character Formation, Neutral and Polar Signals.

TABLE 2-1

TELETYPEWRITER BAUD SPACING

Speed (WPM)	Start and Baud (milliseconds)	Stop (milliseconds)
60	22.2	31.5
67	20.0	28.4
100	13.3	18.9

b. Radio Communications Transmission.—The output from the KW-7 can be used to modulate a tone keyer, such as the TH-5, making the KW-7 compatible with standard radio communications facilities.

2100—PHYSICAL DESCRIPTION

2101. Weight and Dimensions.

a. Packed.—When fully packed for shipment or storage, the KW–7 carrying cases have the following weights and dimensions:

(1) The KW–7 equipment carrying case is 21¼ inches high, 20¼ inches wide, 22 inches deep, and weighs approximately 125 pounds.

(2) The Remote Control Unit carrying case is 15¾ inches high, 26½ inches deep, and weighs approximately 6 pounds.

(3) The Spare Parts carrying case is 12⅜ inches high, 24½ inches wide, 15¾ inches deep, and weighs approximately 75 pounds.

b. Unpacked.

(1) The KW–7 is 11$\frac{9}{32}$ inches high, 15$\frac{21}{64}$ inches wide, 14$\frac{13}{16}$ inches deep and weighs 74.0 pounds.

(2) The Remote Control Unit is 5¼ inches high, 6$\frac{1}{16}$ inches wide, 4⅜ inches deep and weighs approximately three pounds.

(3) The Two-Wire Loop Adapter Unit is 4 inches high, 5¼ inches wide, 5⅛ inches deep and weighs approximately two pounds.

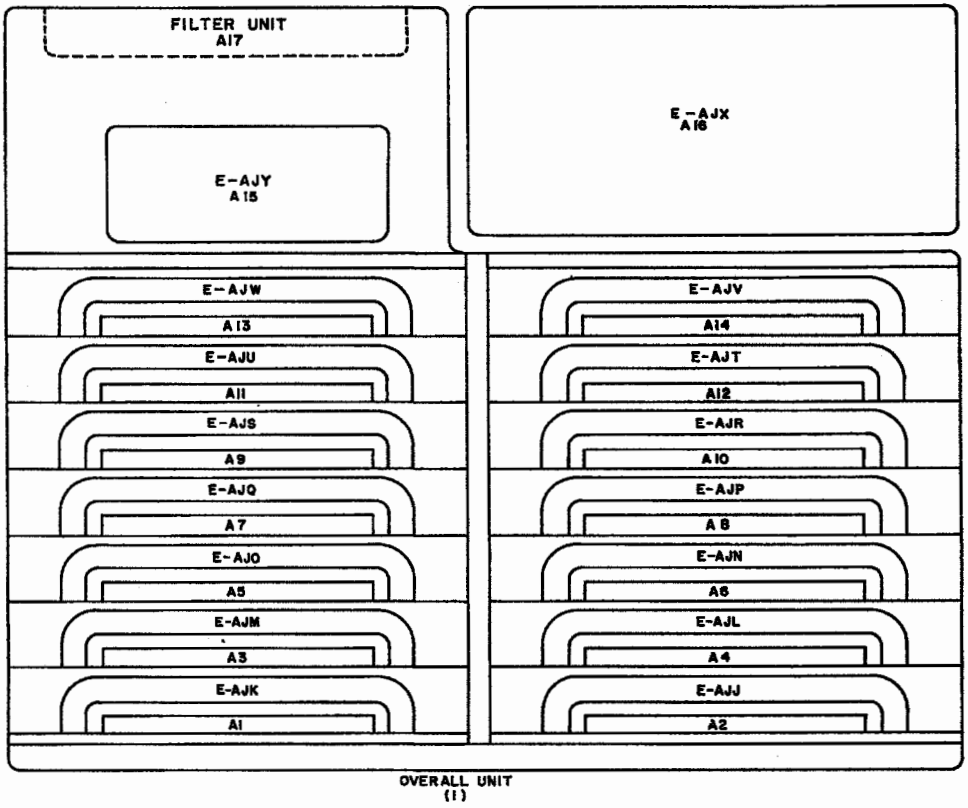
(4) The Functional Remote Control Unit is 4¼ inches high, 8½ inches wide, 5⅛ inches deep and weighs approximately two pounds.

2102. Storage Requirements.—Security regulations govern the location of cryptographic devices. Storage of the KW–7 and associated ancillary units should be handled in accordance with existing MIL specifications on electronic equipment as well as specific instructions for classified equipment.

2103. Major Assemblies (fig. 2–4 and 2–4A).—The KW–7 equipment consists of four major assemblies: the KW–7, the Remote Control Unit, the Functional Remote Control Unit, and the Two-Wire Loop Adapter Unit. The KW–7 contains the circuitry required to perform the cryptographic function. The Remote Control Unit is utilized when remote operation of the system is required, the Two-Wire Loop Adapter Unit is utilized when the equipment is to be used with a two-wire high-level loop circuit and the Functional Remote Control Unit is utilized when the equipment is to be operated, in the cipher mode only, at a remote location Table 2–2 lists the four major assemblies.

2104. Subassemblies.—The only major assembly which contains subassemblies is the KW–7 (fig. 2–4). Table 2–3 defines these individual subassemblies.

a. Subassemblies A1 through A14.—Subassemblies A1 through A14 are printed-circuit cards which are mounted within the KW–7 "wire-nest". Each card consists of a double-sided etched board mounted on a rectangular frame. One side of the card (fig. 2–5) has encapsulated circuits (modules) mounted on it. Each module has both its individual part number and a triangular symbol embossed on the top. The latter allows the technican to determine in which direction the module must be placed when it becomes necessary to install one. The etch board also has a triangular symbol for proper module orientation. The square solder pod immediately to the right of this symbol is pin number 1. Subsequent module pins are numbered clockwise. (Refer to Section 4200 of Chapter 4 for illustrations which show the pin orientation.) The last two digits of the part number are located underneath each module, etched into the printed-circuit board. This allows the technician to verify the type of module to be replaced. The other side of the card (fig. 2–6) has, in addition to etch, the reference designator of each module found on that board. In this man-



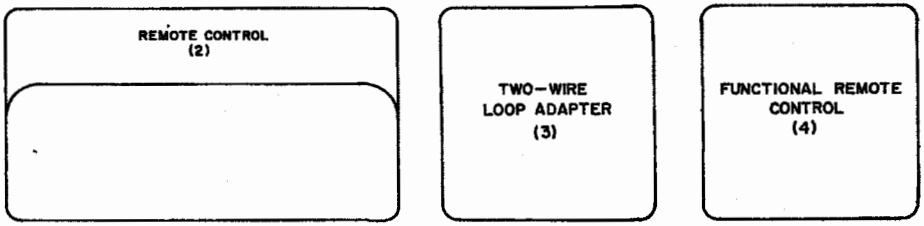


Figure 2-4.—Unit Assemblies.

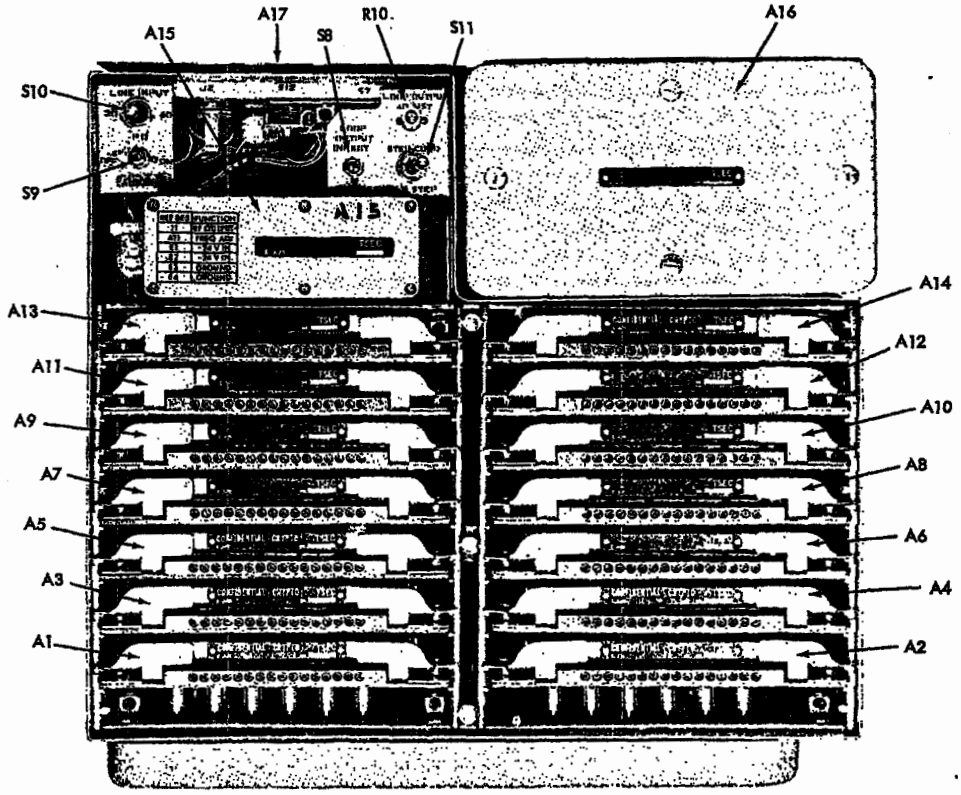


Figure 2-4A.—KW-7, Top View (Cover Removed).

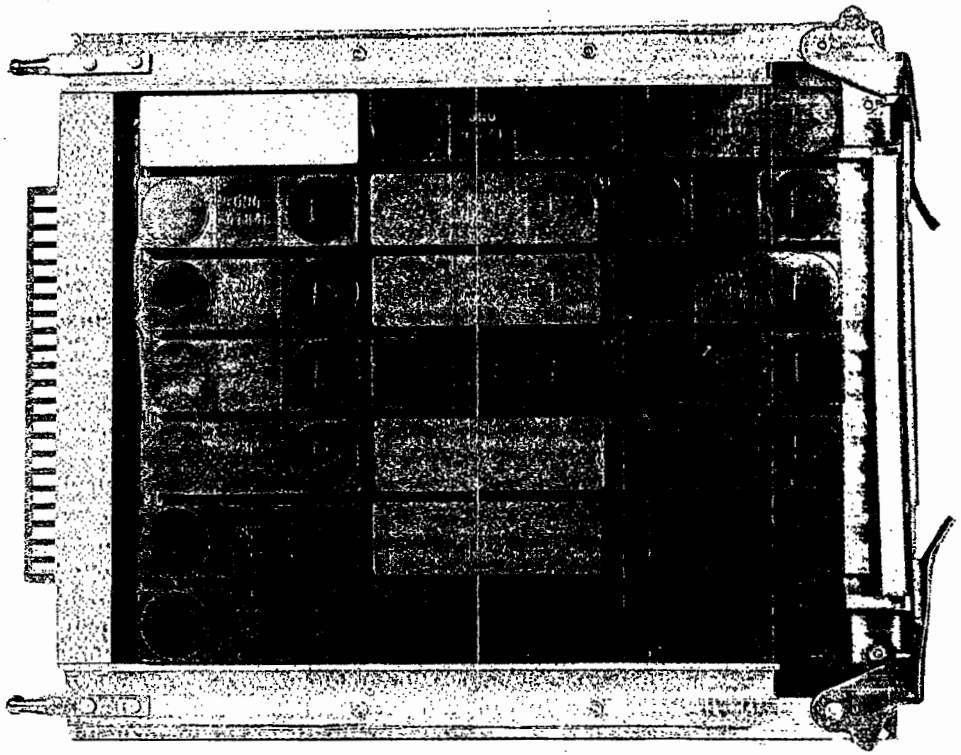


Figure 2-5.—Typical Card Assembly (Module Side).

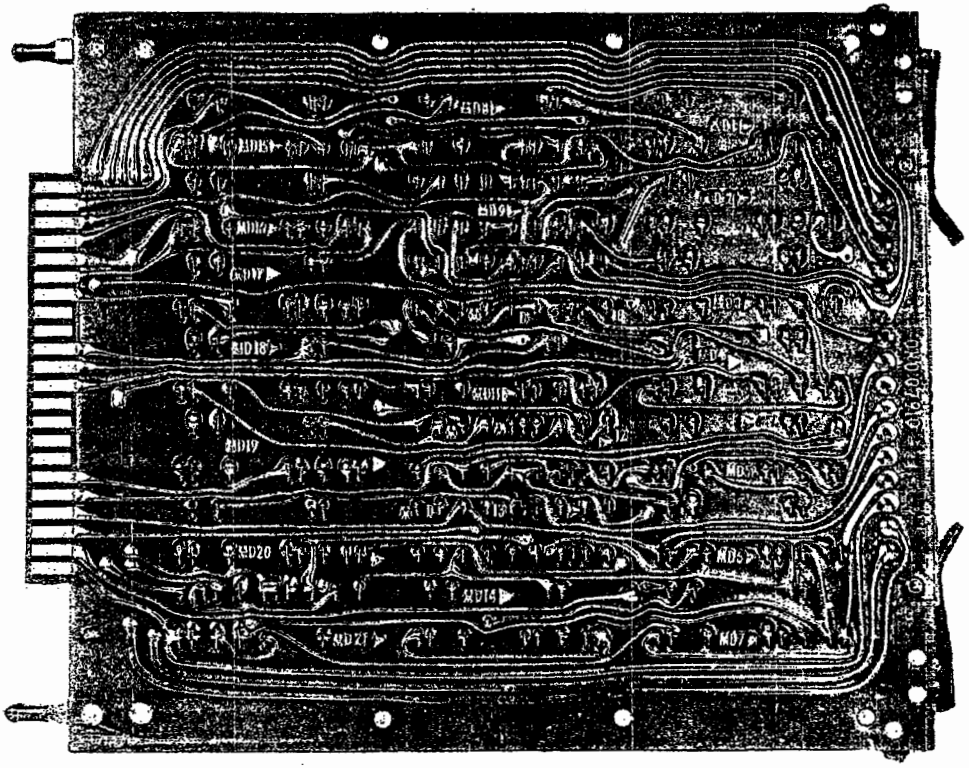


Figure 2-6.—Typical Card Assembly (Etch Side).

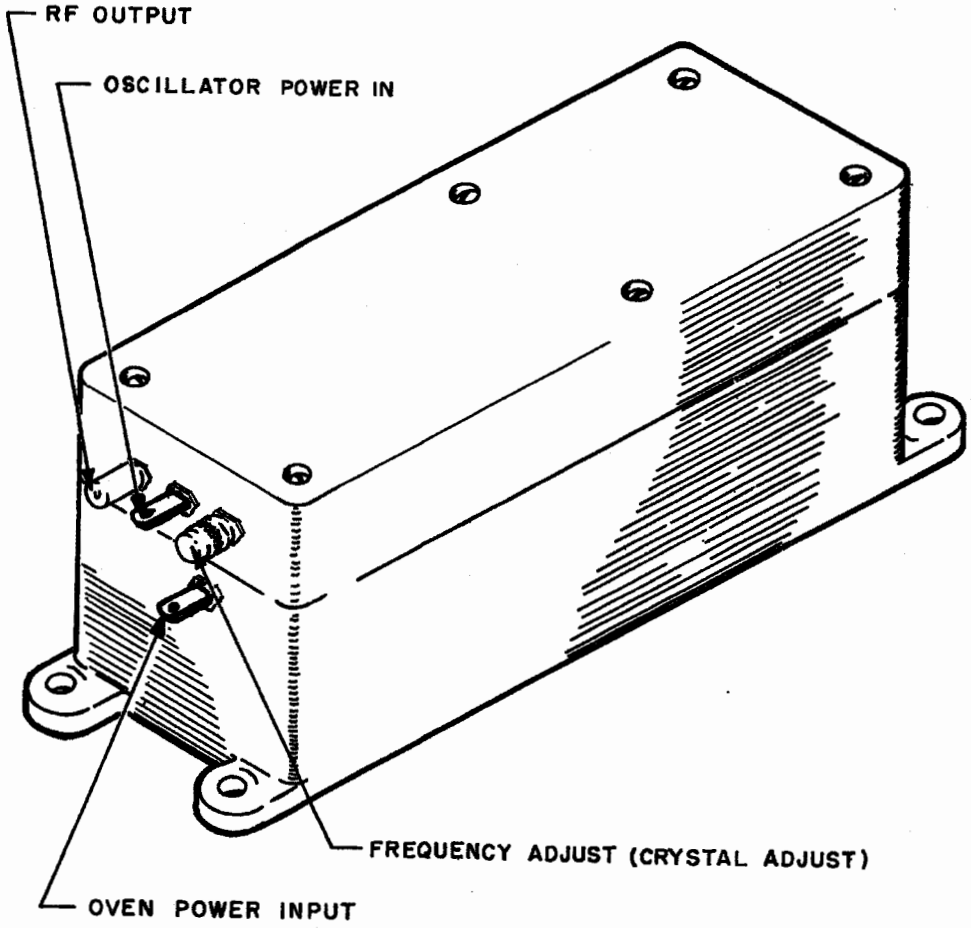


Figure 2-7.—Time Standard (A15), Typical Configuration.

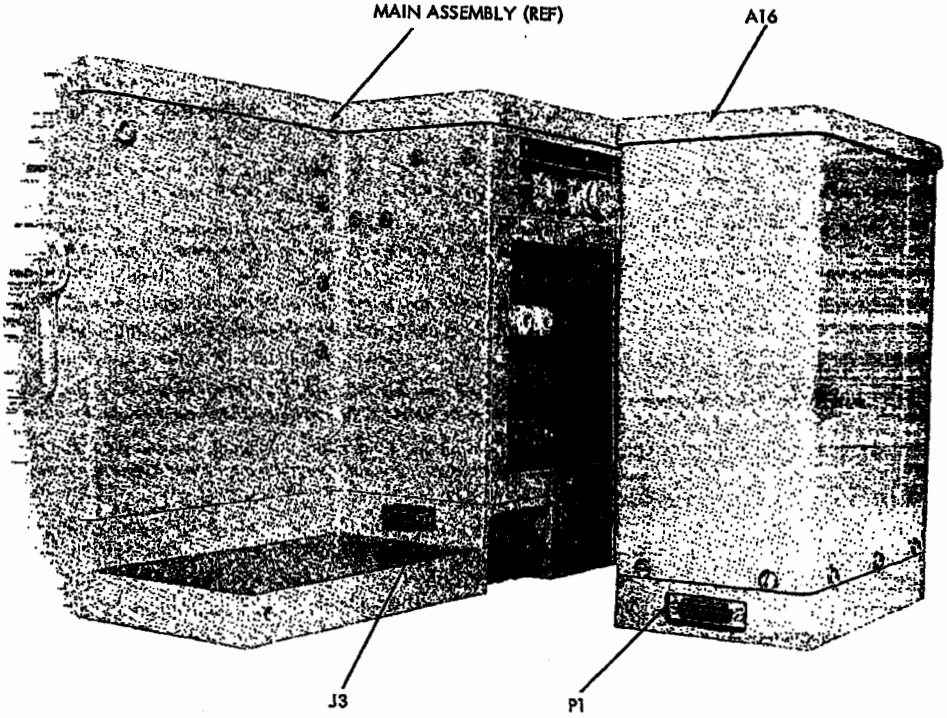


Figure 2-8.—Power Supply (A16).

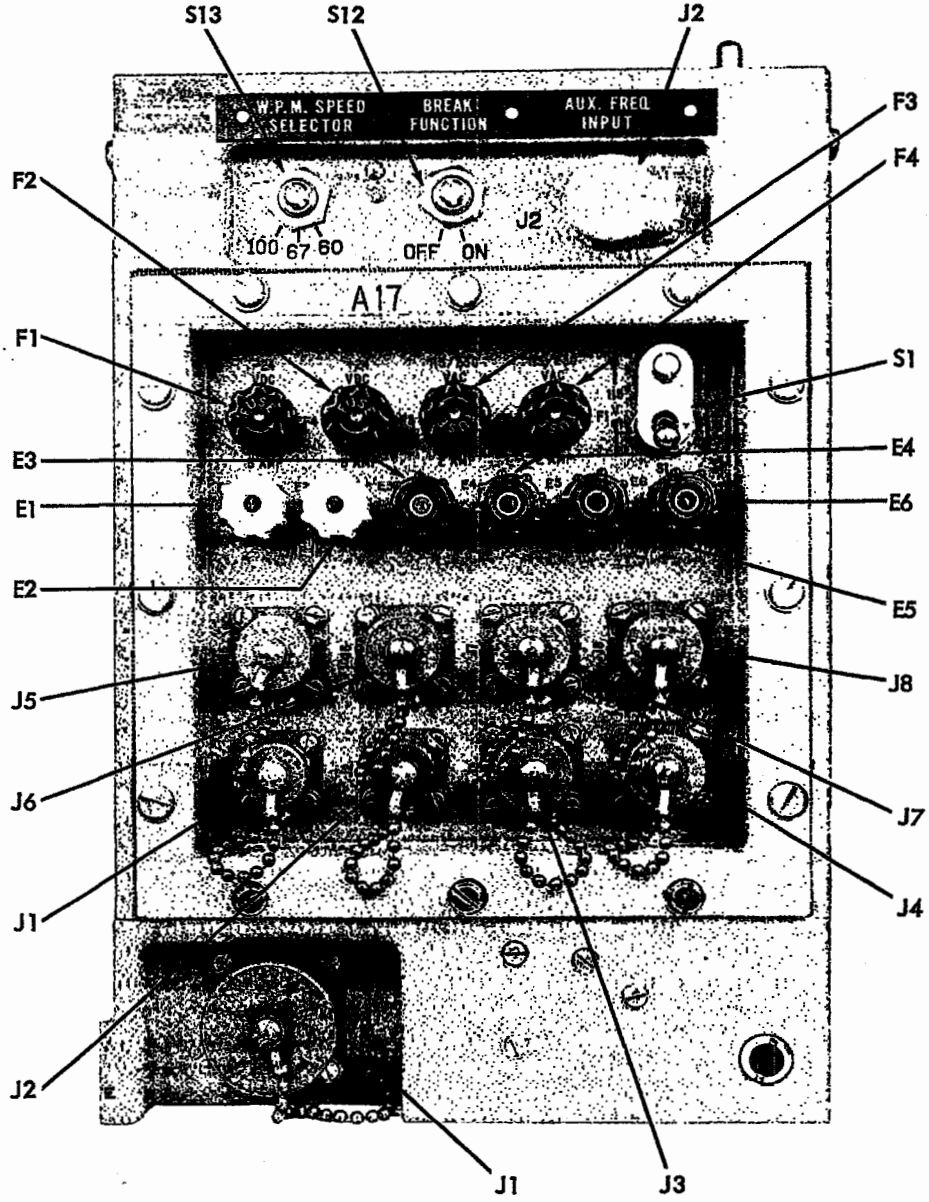


Figure 2-9.—Filter Unit (A17).

ner it is possible to not only know the part number of the module but which module is to be placed where. The rectangular card frame has a test point block mounted on it. The test points provide the technician with readily accessible points for troubleshooting the equipment.

b. *Subassembly A15.*—Subassembly A15 is the time standard used to provide the basic timing pulses for the KW–7. Figure 2–7 illustrates a typical configuration for the subassembly.

c. *Subassembly A16.*—Subassembly A16 is the power supply used to provide the KW–7 with the necessary operating voltages. The power supply (fig. 2–8) is enclosed within a rectangular aluminum housing which may be removed for troubleshooting purposes. The top portion of the power supply is also removable and is used to enclose the power supply test panel. This test panel provides test points and potentiometer adjustments which enable the technician to adjust the power supply voltages.

d. *Subassembly A17.*—Subassembly A17, the filter unit (fig. 2–9), is located at the rear of the KW–7 and contains all of the external input/output connection provisions except the remote connector. These inputs and outputs are all filtered within the filter unit.

e. *Subassembly A18.*—Subassembly A18, the relay assembly, is installed in the bottom of the KW–7 Main Assembly (see fig. 2–15) and contains associated components (relays, transistors, etc.) which contribute to the operation of the KW–7 equipment.

TABLE 2–2

LIST OF MAJOR ASSEMBLIES

Name of Major Assembly	Physical Configuration (Figure Number)
KW–7 Main Assembly	1–1
Remote Control Unit Assembly	1–1
Two-Wire Loop Adapter Unit Assembly	1–1
Functional Remote Control Unit Assembly	1–1

TABLE 2–3

LIST OF MAIN ASSEMBLY MAJOR SUBASSEMBLIES

Trigraph Designator	Reference Designation	Name of Subassembly	Location of Subassembly (Figure Number)
E–AJK	A1	Shift Register No. 1	2–4
E–AJJ	A2	Shift Register No. 2	2–4
E–AJM	A3	Key Generator No. 1	2–4
E–AJL	A4	Key Generator No. 2	2–4
E–AJO	A5	Alarms	2–4
E–AJN	A6	Master Control	2–4
E–AJQ	A7	Clock	2–4
E–AJP	A8	Input Counter	2–4
E–AJS	A9	Registers	2–4
E–AJR	A10	Output Counter	2–4

TABLE 2-3 (Continued)

Trigraph Designator	Reference Designation	Name of Subassembly	Location of Subassembly (Figure Number)
E-AJU	A11	Input Circuit	2-4
E-AJT	A12	Indicator Counter	2-4
E-AJW	A13	Output Circuit	2-4
E-AJV	A14	Noise Generator	2-4
E-AJY	A15	Time Standard	2-4
E-AJX	A16	Power Supply	2-4
None	A17	Filter Unit	2-4, 2-9
None	A18	Relay Assembly	2-15

2105. General Construction.—The major portion of the KW-7 equipment is housed in the Main Assembly and consists of the power supply, time standard, filter unit, and fourteen printed circuit card subassemblies. The remaining units of the KW-7, the Remote Control Unit, the Two-Wire Loop Adapter Unit and the Functional Remote Control Unit contain those components necessary to adapt the system to remote operation and operation with a two-wire high current level loop circuit.

a. *KW-7 Main Assembly.*—The KW-7 Main Assembly is fabricated of a sheet aluminum enclosure riveted to a cast aluminum base. Overall dimensions of the cabinet are $10^{5}\%_{4}$ inches high, 13% inches wide, and $12\%_{6}$ inches deep. All major components, signal connections, card wiring cables, indicator lights and controls are mounted on the Main Assembly casting.

b. *Remote Control Unit.*—The Remote Control Unit is made of welded aluminum construction. It is finished in corrosion resistant enamel. The components necessary to allow the KW-7 to be operated remotely are mounted within the assembly.

c. *Two-Wire Loop Adapter Unit.*—The Two-Wire Loop Adapter Unit is made of welded aluminum construction. It is finished in corrosion resistant enamel. Cable connections are provided on the exterior of the unit.

d. *Functional Remote Control Unit.*—The Functional Remote Control Unit is of welded aluminum construction and finished in corrosion resistant enamel. The indicators and controls required to effect remote control of the KW-7 in the cipher mode are mounted on the assembly.

2106. Reference Designation System.—Each unit, assembly, subassembly, or detail part in the KW-7 equipment has a letter-numbered code designation that associates symbols on a drawing with the location of components in a parts list or in the equipment. The discussion of the reference designation system is divided into three parts: Unit designation, subassembly designation, and detail part.

a. *Unit Designation.*—The KW-7 system consists of four units. Unit 1 refers to the KW-7 Main Unit, Unit 2 refers to the Remote Control Unit, Unit 3 refers to the Two-Wire Loop Adapter Unit, and Unit 4 refers to the Functional Remote Control Unit.

Reference Designation	*Definition*
1	KW-7 Main Unit
2	Remote Control Unit
3	Two-Wire Loop Adapter Unit
4	Functional Remote Control Unit

b. Subassembly Designation.—The main assembly is divided into subassemblies. These subassembly reference designation numbers are preceded by the letter A and are added to the unit number for a particular assembly. For example, 1A1 is the reference designator for assembly 1 in the KW-7. In this case, 1A1 refers to the first card of the KW-7. 1A2 refers to the second card of the KW-7.

c. Detail Part Designation.—Detail parts contained on a subassembly are identified by adding a part designation letter and number to the subassembly reference designator. For example, Module MD1 of the first card (1A1) is reference designated as 1A1MD1. Following are examples which illustrate reference designators for detail parts:

Reference Designation	*Definition*
1C2	Second capacitor of the KW-7
1A6MD11	Eleventh module of sixth subassembly of the KW-7
3CR4	Fourth diode of the Two-Wire Loop Adapter
2J1	First jack of the Remote Control Unit

2107. Provision for Electrical Connections.—The KW-7 contains provisions for making electrical connections to various pieces of ancillary equipment. Table 2-4 defines those connectors located on the KW-7, the Remote Control Unit, Two-Wire Loop Adapter Unit and the Functional Remote Control Unit.

TABLE 2-4

KW-7 CONNECTORS

Unit Ref. Desig.	Fig. No.	Type	Panel Marking	Function
KW-7 Filter 1A17	2-10	Quick-disconnect	J1, AC POWER	Provides 115V/230V power input to the equipment.
1A17	2-10	Quick-disconnect	J2, 24VDC	Provides DC power input to the equipment.
1A17	2-10	Quick-disconnect	J3, LOOP IN-1 J4, LOOP IN-2 CP2	Allows two loop-in signals to be fed to the equipment. (If only one input is to be used it will be necessary to place the jumper plug, supplied with the equipment, in the CP2 connector.)
1A17	2-10	Quick-disconnect	J5, TD STEP	Provides a means of stepping a transmitter-distributor by employing the internal KW-7 timing.
1A17	2-10	Quick-disconnect	J6, PTS	Provides for the connection of a device that prevents inadvertent transmission of plain text information.
1A17	2-10	Quick-disconnect	J7, LOOP OUT-1 J8, LOOP OUT-2 CP1	Allows two loop-out signals to be transmitted from the equipment. (If only one output is being used it will be necessary to place the jumper plug, supplied with the equipment, in the CP1 connector.)
1A17	2-10	Twist-top terminals	E1, LINE IN E2, LINE IN	Provides a means of accepting either two-wire or four-wire line-in signals. (If two-wire line-in is being used it will be necessary to place a jumper wire between E2 and E4, LINE OUT.)

TABLE 2-4 (Continued)

Unit Ref. Desig.	Fig. No.	Type	Panel Marking	Function
1A17	2-10	Twist-top terminals	E3, GRD	Allows the KW-7 to be grounded to to the TTY.
1A17	2-10	Twist-top terminals	E4, E5 and E6, LINE OUT	Provides a means of transmitting two-wire or four-wire neutral or polar signals. (If neutral is used, terminal E6 is not connected.)
KW-7				
1	2-10	Phone Jack	J2, AUX. FREQ. INPUT	Allows an external 100KC timing signal to be used in place of the internally generated 1MC timing signal.
1	2-10	Quick-disconnect	J1, REMOTE	Allows the KW-7 to be controlled by either the remote control unit or the functional remote control unit. Also provides signal path.
Remote Control Unit				
2	2-11	Quick-disconnect	J1, REMOTE BOX	Performs the same function as the REMOTE connector located on KW-7.
2	2-11	Quick-disconnect	J2, PTS	Performs the same function as the PTS connector located on KW-7.
2	2-11	Quick-disconnect	J3, LOOP IN-1 J4, LOOP IN-2 CP1	Performs the same function as the LOOP IN-1 and LOOP IN-2 connectors located on the KW-7. (If only one input is used it is necessary to install the jumper plug, supplied with the equipment, in the CP1 connector.)
2	2-11	Quick-disconnect	J5, LOOP OUT-1 J6, LOOP OUT-2	Performs the same function as the LOOP OUT-1 and LOOP OUT-2 connectors located on the KW-7. (If only one output is used it is necessary to install the jumper plug, supplied with the equipment, in the CP2 connector.)
2	2-11	Quick-disconnect	J7, TD Step	Performs the same function as the TD STEP connector on KW-7.
Two-Wire Loop Adapter Unit				
3	2-12	Quick-disconnect	J2, TTY INPUT	Provides connection of the two-wire high-level loop input-output teletypewriter circuit.
3	2-12	Quick-disconnect	J1, LOOP INPUT	Allows the converted low-level loop input signal to be fed into the KW-7 loop input.
3	2-12	Quick-disconnect	J3, LOOP OUTPUT	Allows the plaintext loop output signal from the KW-7 to be converted by the two-wire Loop Adapter Unit and fed to the Loop TTY.

TABLE 2-4 (Continued)

Unit Ref. Desig.	Fig. No.	Type	Panel Marking	Function
Functional Remote Control Unit				
4	2-13	Quick-disconnect	J1, REMOTE BOX	Performs the same function as the REMOTE connector located on the KW-7.
4	2-13	Quick-disconnect	J2, TD STEP	Performs the same function as the TD STEP connector located on the KW-7.

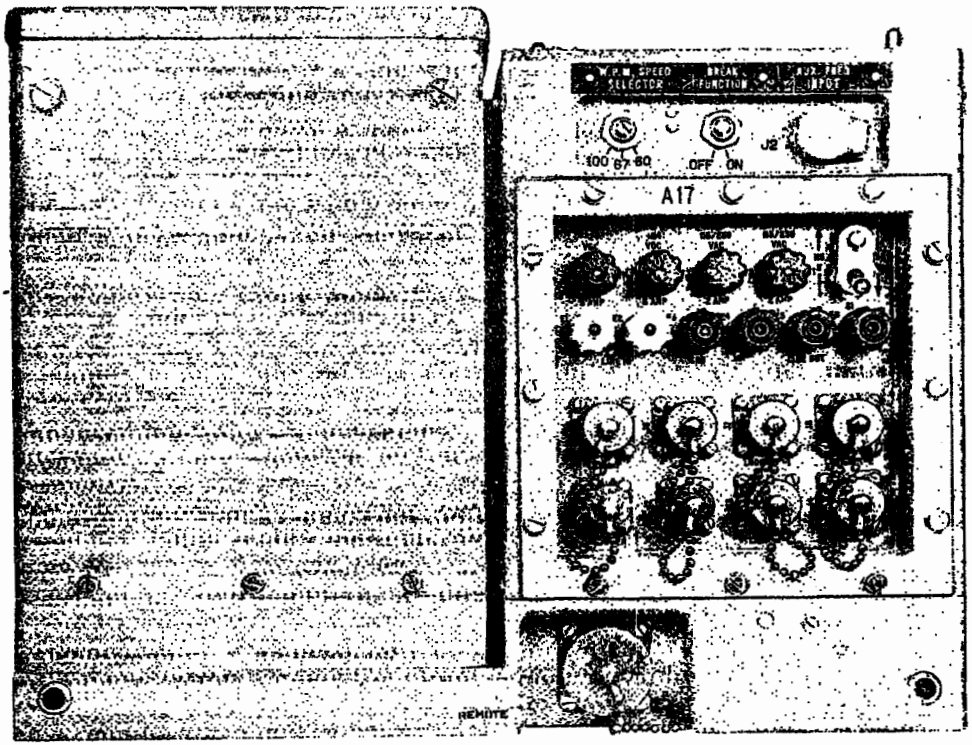


Figure 2-10.—Rear View of KW-7.

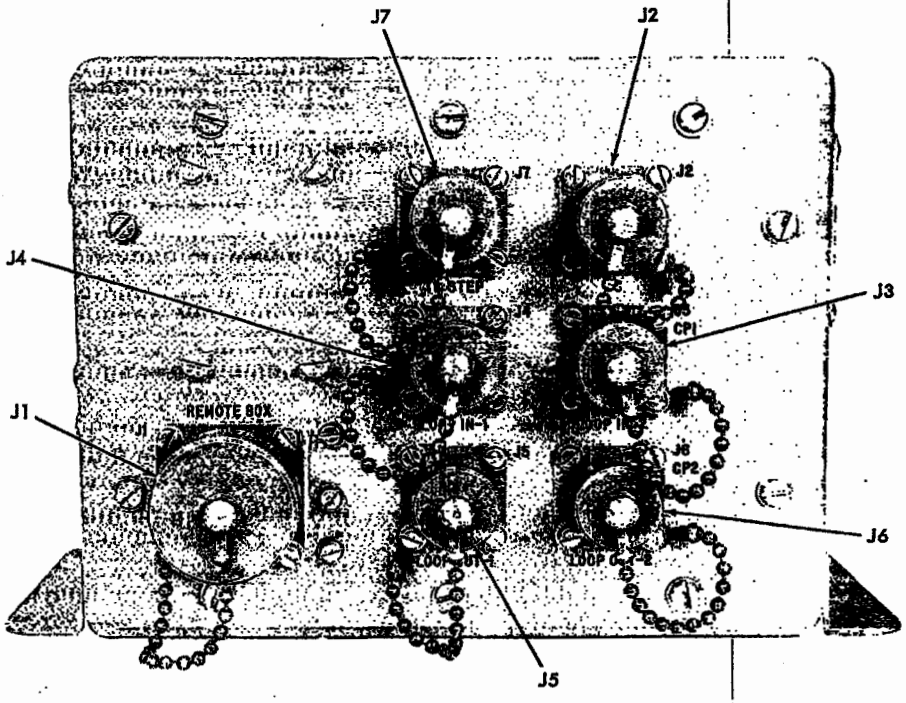


Figure 2-11.—Rear View of Remote Control Unit.

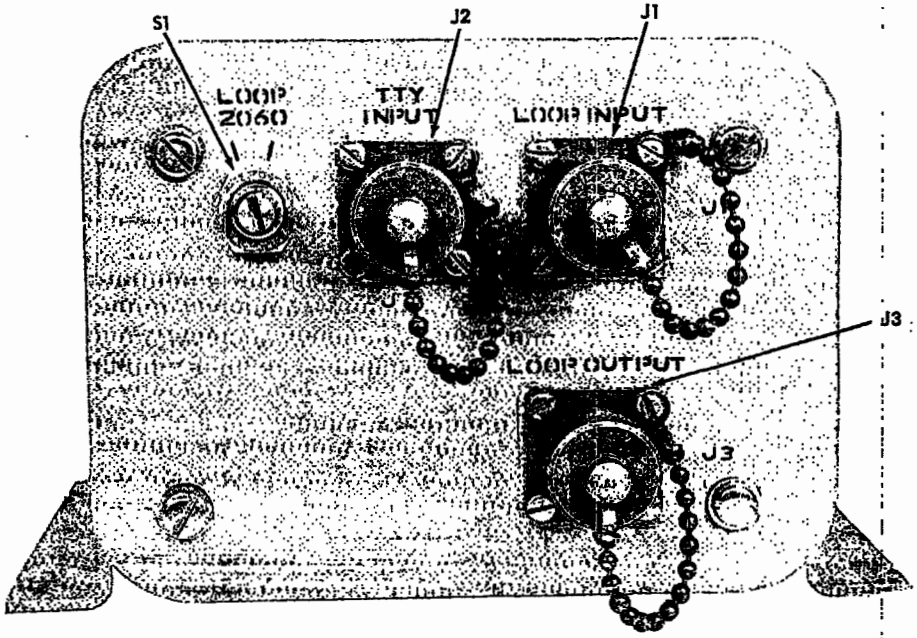


Figure 2-12.—Front View of Loop Adapter Unit.

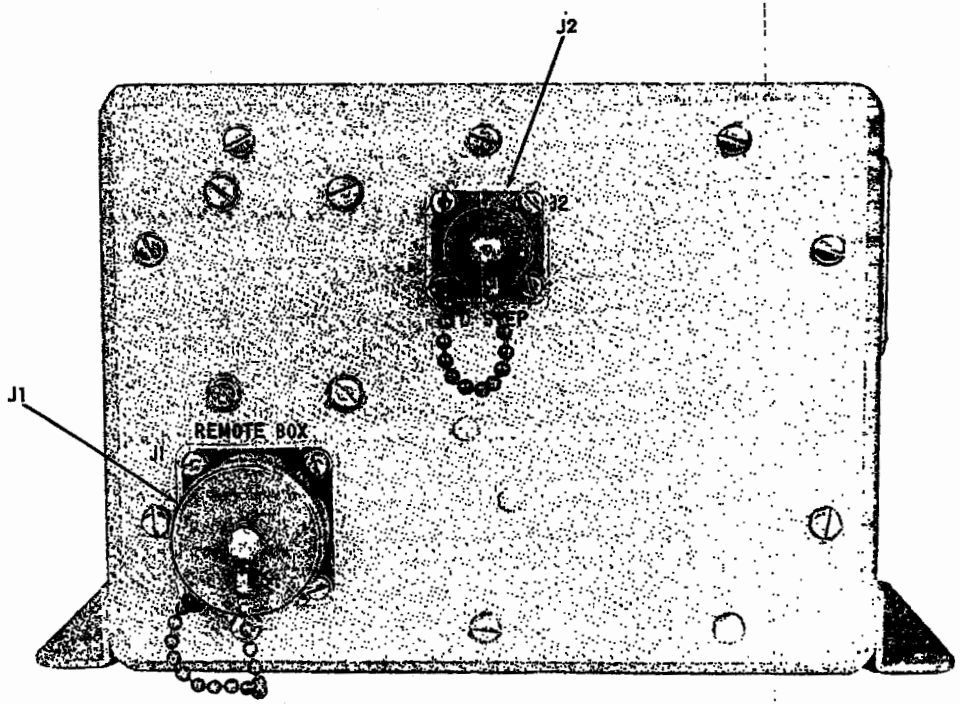


Figure 2-13.—Rear View of Functional Remote Control Unit.

2108. Operating Controls and Indicators.—Tables 2-5 and 2-6 define those operating controls and indicators located on the KW-7, Remote Control Unit, Two-Wire Loop Adapter Unit and Functional Remote Control Unit.

TABLE 2-5

OPERATING CONTROLS AND INDICATORS

Unit	Ref. Desig.	Fig. No.	Type	Panel Marking	Function
KW-7					
1	DS1	2-14	Indicator Lamp	PLAIN	Indicates when the KW-7 is being used in either the Plain Synchronous (SYNC) or Plain Asynchronous (ASYNC) modes of Operation.
1	DS2	2-14	Indicator Lamp	POWER ON	Indicates when primary power has been applied to the KW-7.
1	DS3	2-14	Indicator Lamp	MI	Allows the KW-7 operator to visually determine that a failure has occurred in the randomizer.
1	S4/DS4	2-14	Pushbutton Switch/Indicator Lamp	BREAK	Allows the KW-7 operator to break the line. The indicator lamp is provided to inform the equipment operator of this break condition.
1	DS5	2-14	Indicator Lamp	P&I	Indicates that the KW-7 has initiated the phasing and indicator phase of operation.
1	S5/DS6	2-14	Pushbutton Switch/Indicator Lamp	SEND	Allows the KW-7 operator to initiate the phasing and indicator phase of operation. The indicator lamp is a visual aid to provide a means of monitoring the activation of the send circuits.
1	DS7	2-14	Indicator Lamp	ALARM	Indicates that a failure exists in the key generator.
1	S1	2-14	Rotary Switch	REMOTE-CIPHER-SYNC-ASYNC	Allows the KW-7 to be placed in one of three operating modes: Remote, Cipher or Plain. (The operator has two choices of Plain operation: Synchronous or Asynchronous.)
1	S2	2-14	Toggle Switch	POWER ON-OFF	Allows 115V AC, 230V AC or 24V DC power to be applied to the KW-7.
1	S3	2-14	Pushbutton Switch	BREAK RESTORE	Allows the KW-7 operator to to remove the break condition. (Returns the line out circuitry to the line.)
1	S6	2-14	Rotary Switch	ALARM TEST	Allows the KW-7 operator to simulate failures within the alarm portions of the equipment so as to check the alarm portions for proper operation.

TABLE 2-5 (Continued)

Unit	Ref. Desig.	Fig. No.	Type	Panel Marking	Function
1	S12	2-10	Rotary Switch	BREAK FUNCTION	Allows the KW-7 operator to disable the break function when the equipment is being used with radio equipment.
1	S13	2-10	Rotary Switch	W.P.M. SPEED SELECTOR	Allows the KW-7 operator to match the KW-7 operating speed to that of the teletypewriter equipment.
1	LS1	2-15	Buzzer	None	Allows the KW-7 operator to monitor the alarm circuits and the break circuits. The alarm will sound if an alarm circuit fails, if a break occurs in the line or if operating in plain mode.
KW-7 Filter 1A17	S1	2-10	Toggle Switch	115V/230V	Provides a means of switching the internal power supply to accept either 115V AC or 230V AC.
Remote Control Unit 2	DS1	2-16	Indicator Lamp	PLAIN	Performs the same function as does the PLAIN indicator lamp located on the KW-7.
2	DS2	2-16	Indicator Lamp	CIPHER	Allows the KW-7 operator to verify that Cipher operation is in effect when selected.
2	DS3	2-16	Indicator Lamp	ALARM	Performs the same function as the ALARM lamp located on the KW-7.
2	DS4	2-16	Indicator Lamp	P&I	Performs the same function as the P&I indicator lamp located on the KW-7.
2	S1	2-16	Rotary Switch	SYNC-ASYNC-CIPHER	Performs the same function as does the switch used on the KW-7.
2	S2/DS5	2-16	Pushbutton Switch/Indicator Lamp	BREAK	Performs the same function as does the BREAK switch located on the KW-7.
2	LS1		Buzzer	None	Performs the same function as the buzzer located on the KW-7.
2	S3	2-16	Pushbutton Switch	BREAK RESTORE	Performs the same function as the BREAK RESTORE switch located on the KW-7.
2	S4/DS6	2-16	Pushbutton Switch/Indicator Lamp	SEND	Performs the same functions as the SEND switch located on the KW-7.

TABLE 2-5 (Continued)

Unit	Ref. Desig.	Fig. No.	Type	Panel Marking	Function
3	S1	2-12	Rotary Switch	LOOP 20-60	Allows the KW-7 operator to select the proper operating current.
4	S1/DS4	2-17	Pushbutton Indicator Lamp	SEND	Performs the same function as the SEND switch located on the KW-7.
4	DS1	2-17	Indicator Lamp	P&I	Performs the same function as the P&I indicator lamp located on the KW-7.
4	DS2	2-17	Indicator Lamp	ALARM	Performs the same function as the ALARM indicator lamp located on the KW-7.
4	DS3	2-17	Indicator Lamp	READY	Indicates that the control unit is operational.
4	LS1	2-17	Buzzer	None	Performs the same function as the Buzzer located on the KW-7.

TABLE 2-6

INTERNAL OPERATING CONTROLS

Unit	Ref. Desig.	Fig. No.	Type	Panel Marking	Function
1	R10	2-4	Potentiometer	LOOP OUTPUT ADJUST	Allows the KW-7 operator to properly adjust the loop-out current.
1	S8	2-4	Toggle Switch	LOOP OUTPUT INHIBIT/ ALLOW	Allows the KW-7 operator to disable the loop-out circuit and switch it to the Two-Wire Loop Adapter Assembly.
1	S9	2-4	Toggle Switch	ALARM ON-OFF	Allows maintenance personnel to disable the audible alarm buzzer when troubleshooting in PLAIN text.
1	S10	2-4	Toggle Switch	LINE INPUT 20-PO-60	Allows the KW-7 operator to select one of three line modes of operation: 20 ma or 60 ma neutral or polar.
1	S11	2-4	Toggle Switch	TD STEP STEP-CONT	Allows the KW-7 operator to program the transmitter-distributor circuits for either continuous or stepping operation.
Card E-AJV					
1A14	S1	2-5	Toggle Switch	20-60	Allows the KW-7 operator to select the proper Loop output current.

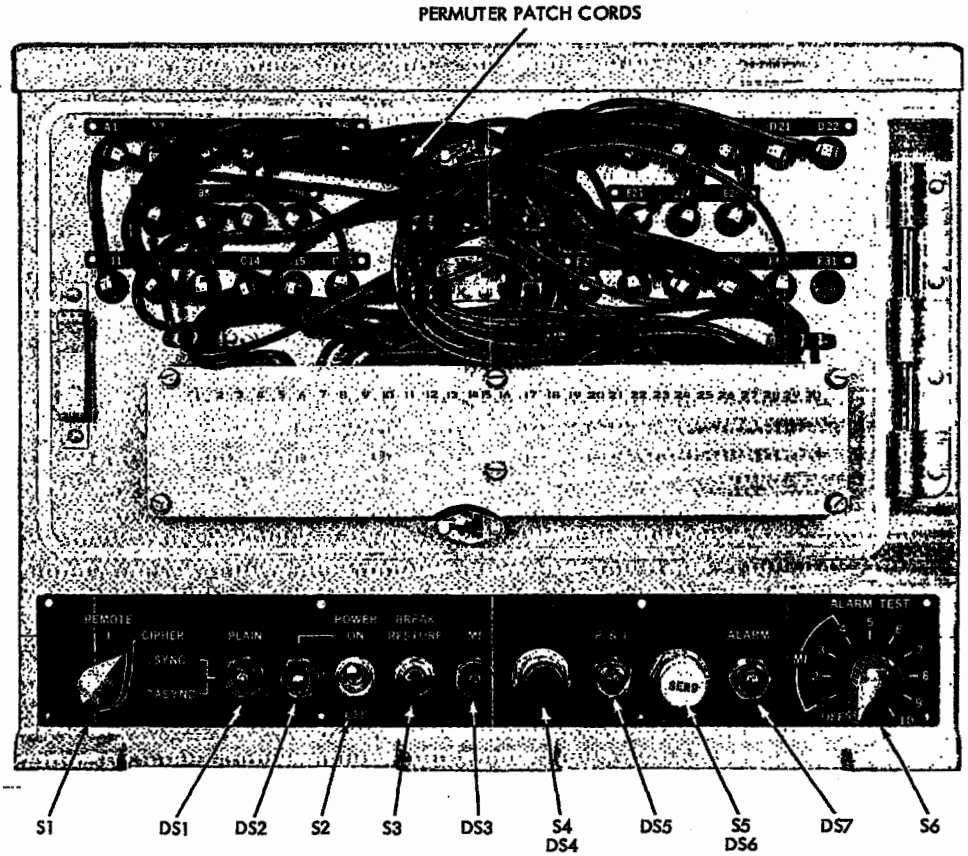


Figure 2-14.—Front View of KW-7 (Patch Cord Cover Removed).

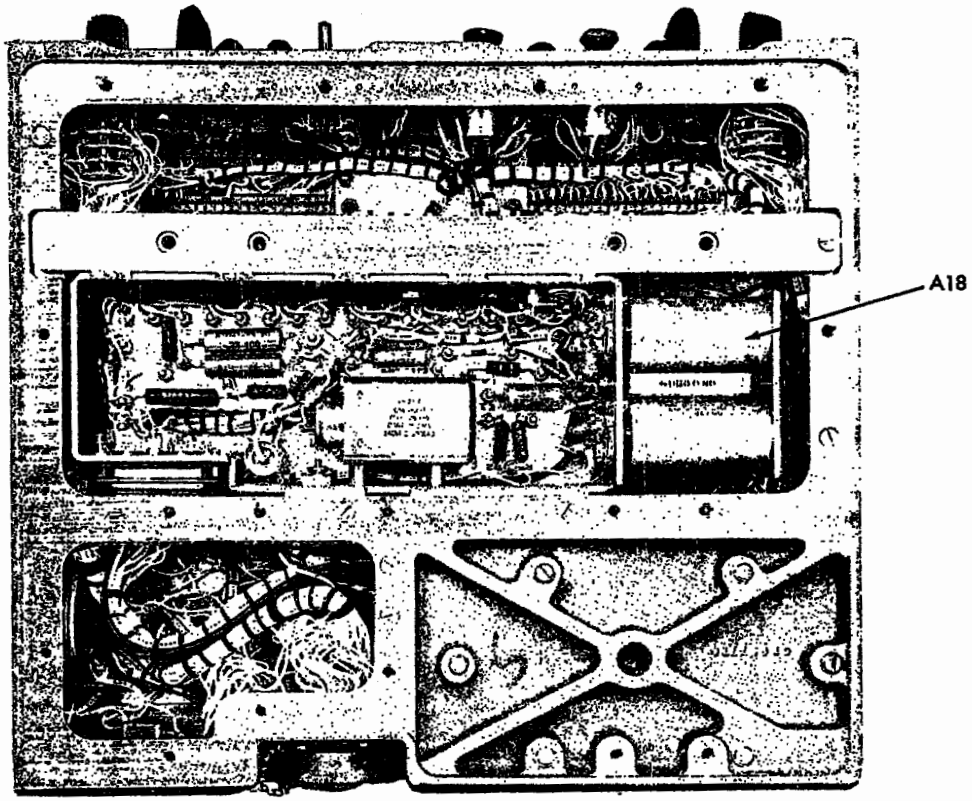


Figure 2-15.—Bottom View of KW-7 (Cover Removed).

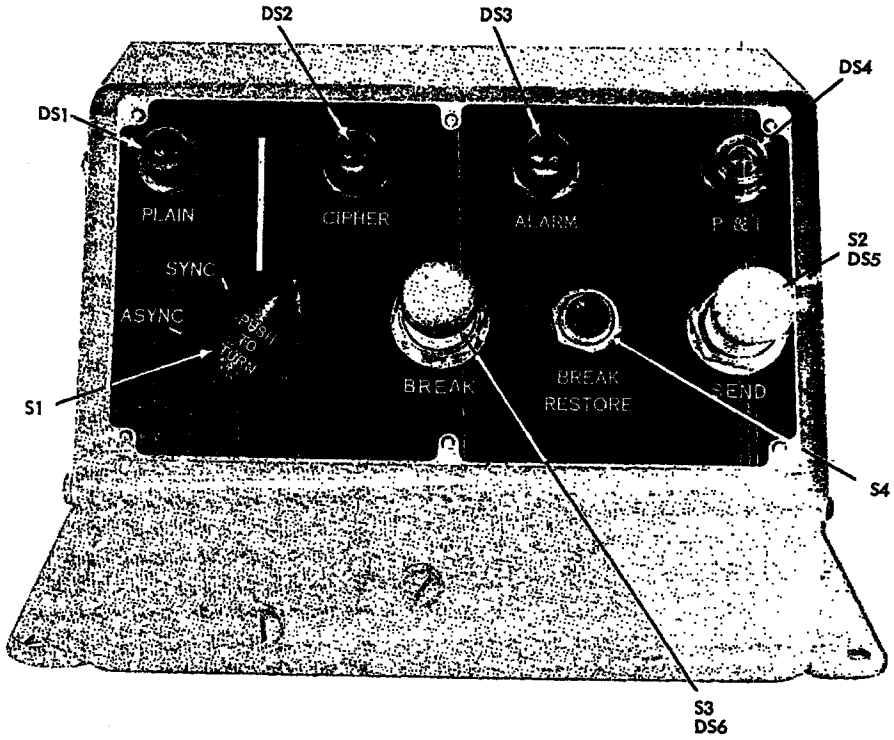


Figure 2-16.—Front View of Remote Control Unit.

2200—ELECTRICAL CHARACTERISTICS

2201. Electrical Power Requirements.—The KW-7 operates with either of three voltages as shown in table 2-7. Table 2-7 also gives the tolerance of operation.

TABLE 2-7

ELECTRICAL POWER TOLERANCES

Voltages	Frequency	Tolerance
115 VAC		+10 percent, −15 percent (97.75 to 126.5 volts AC)
	50-400 cps	±10 percent
230 VAC		+10 percent, −15 percent (195.50 to 253.0 volts AC)
	50-400 cps	±10 percent
24 VDC		21 to 31 volts DC

2202. Power Consumption.—When the KW-7 is first turned on, it momentarily places a peak starting load of 300 watts on the power line. Following this initial surge, the equipment consumes approximately 80 watts of power.

2203. Input Signal Requirements.

a. Information Signal.—The KW-7 is designed to operate with any standard teletypewriter device that provides or accepts information signals in the 7.0 or 7.42 baudot code at nominal speeds of 60, 67 or 100 words per minute. In normal operation, the 7.42 code is generated by teletypewriter devices (teletypewriter keyboard or free-running transmitter-distributor) and the 7.0 code is generated by another KW-7 or a stepped transmitter-distributor. Table 2-8 defines the various inputs to the KW-7.

b. Timing.—The only timing information contained in the input signals is the occurrence of the stop-start transitions. The baudot code units contain data only.

TABLE 2-8

KW-7 INPUT SIGNALS

Input To	Type of Input	
	Mark	Space
Loop-In-Circuit	Approximately 80 microamperes	No current
Line-In-Circuit (Neutral Operation)	20 or 60 milliamperes	No current
Line-In-Circuit (Polar Operation)	+20 or +30 milliamperes	−20 or −30 milliamperes

2204. Output Signal Requirements.—The KW-7 is capable of generating 20 or 60 milliampere signals for neutral operation and +20 or +30 and −20 or −30 milliampere signals for polar operation. Table 2-9 describes the various outputs from the KW-7.

TABLE 2-9

KW-7 OUTPUT SIGNALS

Output To	Type of Output from KW-7	
	Mark	Space
Teletypewriter page printer	20 or 60 milliamperes	No current
Another KW-7 or teletypewriter (Neutral)	20 or 60 milliamperes	No current
Another KW-7 or teletypewriter (Polar)	+20 or +30 milliamperes	−20 or −30 milliamperes

2300—MODIFICATION INSTRUCTIONS ISSUED BY NSA FOR TSEC/KW-7

2301. Introduction.—Table 2-10 below is provided to inform maintenance personnel of KW-7 modification instructions that have been issued by the National Security Agency. If the table is blank, it means that no equipment modifications have been promulgated thus far. As future modifications (if any) are issued, information regarding them will be inserted in the Table by means of Amendments to this manual.

TABLE 2-10

LIST OF MODIFICATIONS TO THE KW-7

Short Title (KAB)	Long Title	Publication Date	Equipments Affected

CHAPTER 3

EMPLOYMENT

3000—UNPACKING AND INSPECTION

3001. Unpacking.—Prior to unpacking the KW-7 equipment from the carrying cases, consideration should be given to the work area location of the equipment, accessibility of equipment for maintenance, convenience of operating personnel, illumination, and the normal flow of traffic in the designated area.

a. Packaging Data.—The following subparagraphs describe the physical characteristics and the contents thereof for each of the three carrying cases.

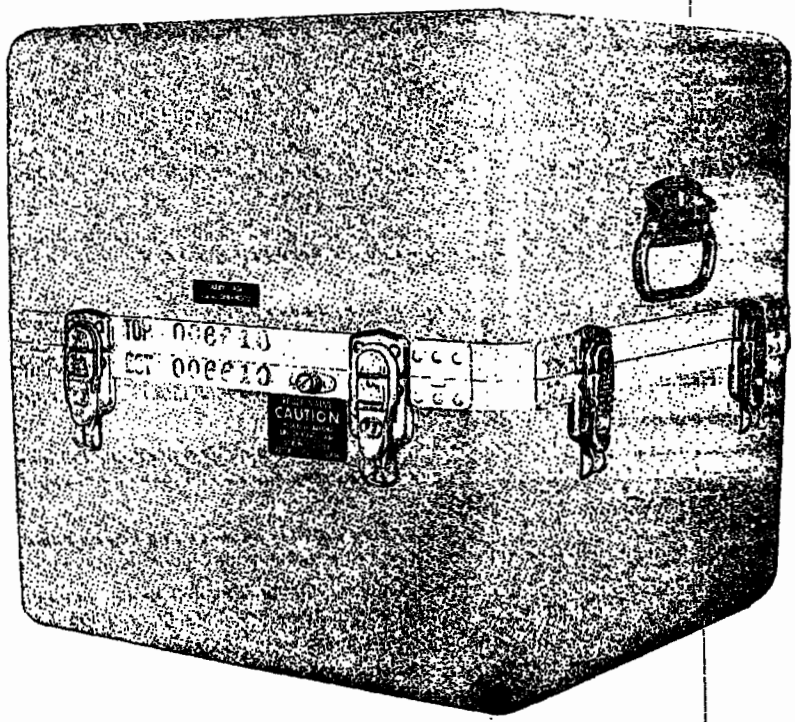


Figure 3-1.—Carrying Case.

(1) *KW-7 equipment carrying case (fig. 3-1).*—The KW-7 equipment carrying case is of fiberglass construction with dimensions, volume and net weight as presented in Table 3-1. Contents of the case are as follows:

(a) One KW-7 Main Assembly

(b) One Key Generator (KG) test adapter card

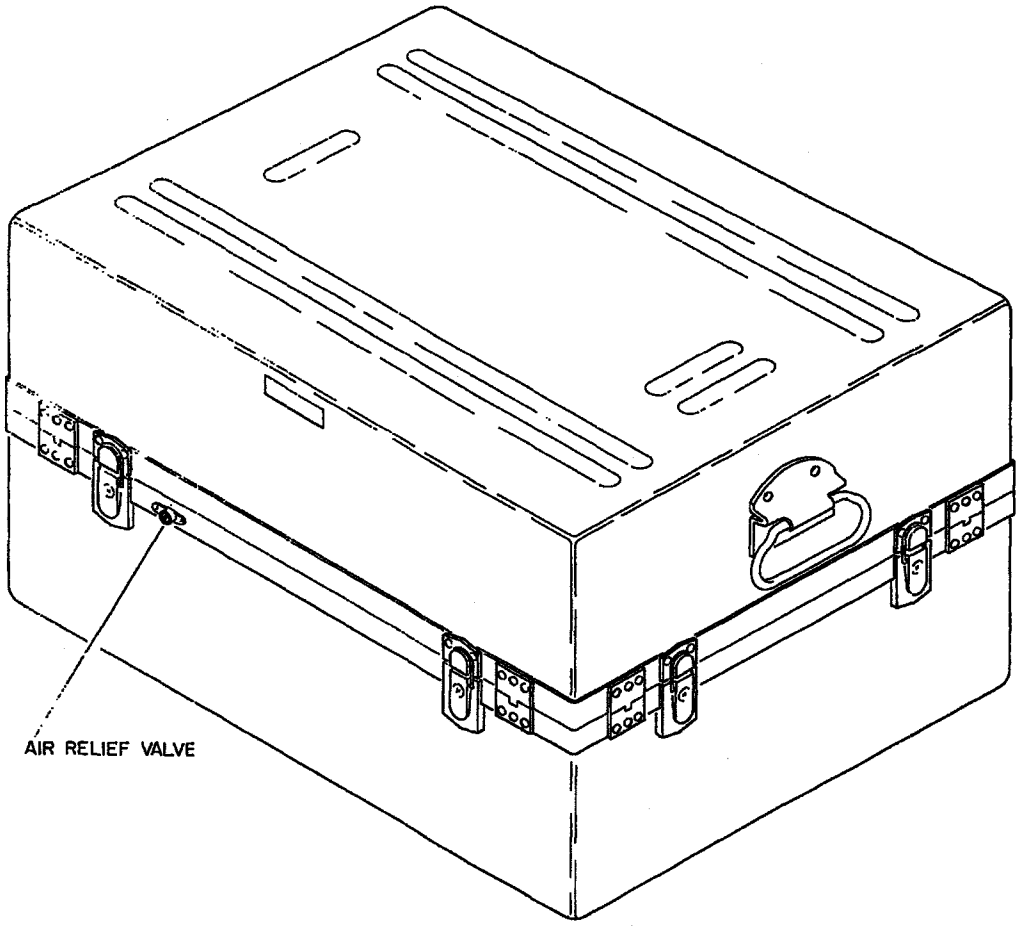


Figure 3-1A.—Carrying Case, Remote Control Unit.

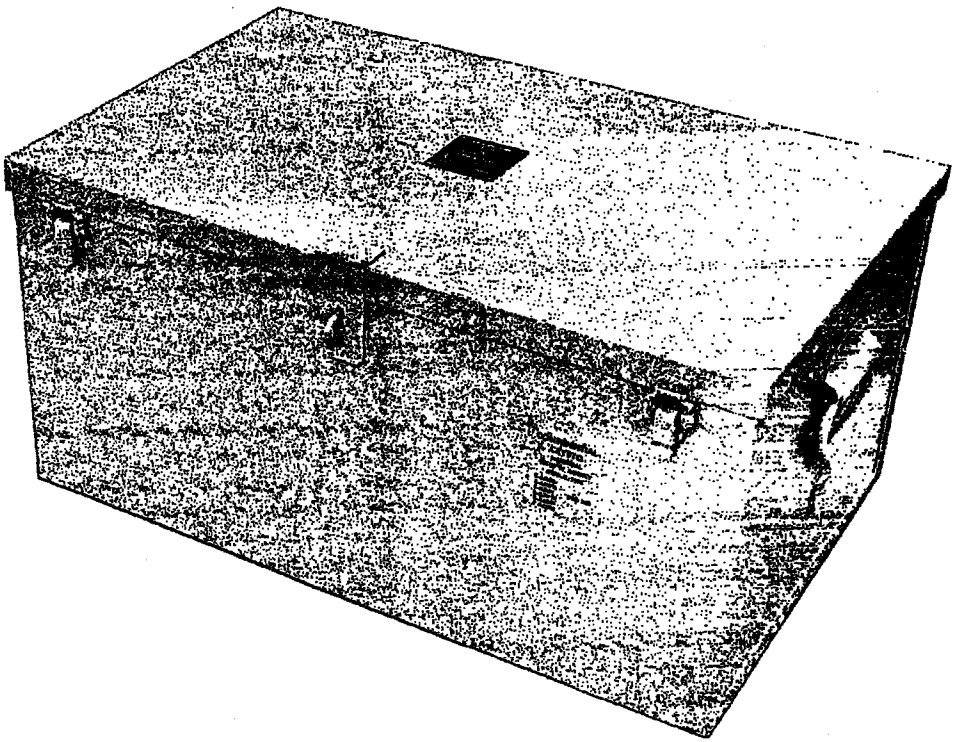


Figure 3-1B.—Carrying Case, KWQ-8 Spare Parts.

(c) One test extender card
(d) One 115-volt AC power cable assembly (W2)
(e) One 230-volt AC power cable assembly (W1)
(f) Two loop-input cable assemblies (W6)
(g) Two loop-output cable assemblies (W7)
(h) One transmitter-distributor cable assembly (W5)
(i) One jumper plug (CP) for use with Loop-In connector
(j) One jumper plug (CP) for use with Loop-Out connector
(k) One PTS connector for PTS cable assembly (fabrication by user)
(l) One DC connector for DC power cable assembly (fabrication by user)

TABLE 3-1

KW-7 EQUIPMENT CARRYING CASE

Height (in.)	Width (in.)	Depth (in.)	Volume (cu. ft.)	Weight (lb.)
21¼	20¼	22	5.5	Approx. 45

(2) *Remote unit carrying case (fig. 3-1A).*—The Remote Control Unit carrying case is of aluminum construction with dimensions, volume and net weight as presented in Table 3-1A. Contents of the case are as follows:
(a) One Remote Control Unit
(b) One Remote Control Cable Assembly (W4)
(c) One transmitter-distributor cable assembly (W5)
(d) Two loop-input cable assemblies (W6)
(e) Two loop-output cable assemblies (W7)

TABLE 3-1A

REMOTE CONTROL UNIT CARRYING CASE

Height (in.)	Width (in.)	Depth (in.)	Volume (cu. ft.)	Weight (lb.)
15¾	26½	20½	3.6	Approx. 40

(3) *KWQ-8/TSEC spare parts carrying case (fig. 3-1B).*—The KWQ-8/TSEC spare parts carrying case is of steel construction with dimensions, volume and net weight as presented in Table 3-1B. Contents of the case are as follows:
(a) One each of subassemblies A1 through A17
(b) An assortment of replaceable parts

TABLE 3-1B

KWQ-8/TSEC SPARE PARTS CARRYING CASE

Height (in.)	Width (in.)	Depth (in.)	Volume (cu. ft.)	Weight (lb.)
12¾	24½	15¾	2.5	Approx. 38

b. Unpacking Procedures.—The following subparagraphs describe the procedures to be performed when unpacking the carrying cases.

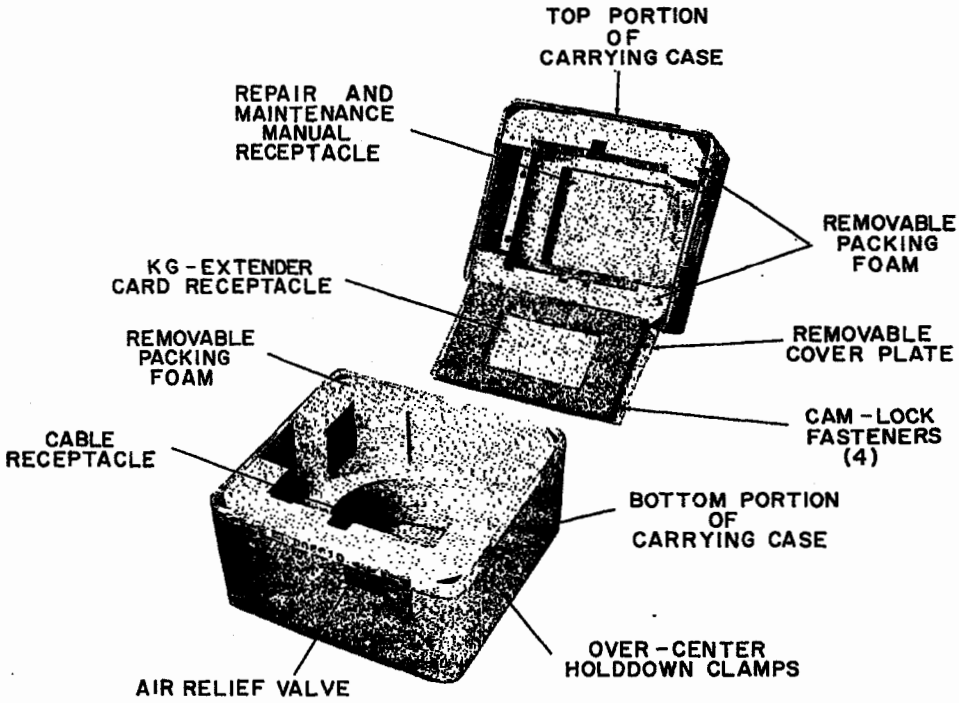


Figure 3-2.—Diasssembly of KW-7 Carrying Case.

(1) *KW-7 equipment carrying case (fig. 3-2).*

(a) Place the carrying case on a suitable work surface.

(b) Using a screw driver, rotate the air relief valve to its extreme counterclockwise position.

WARNING: THE CARRYING CASE IS SHIPPED IN AN AIRTIGHT CONDITION AND REQUIRES PRESSURE EQUALIZATION PRIOR TO BEING OPENED. PERSONNEL MAY BE SERIOUSLY INJURED IF THE AIR RELIEF VALVE IS NOT FIRST OPENED.

(c) Unlock the eight over-center hold-down clamps and remove top portion of the case.

(d) Remove the KW-7 from the bottom portion of the case, and then remove the foil wrapping from the unit.

(e) Remove the cable assemblies found in the cutout located in the bottom portion of the case.

(f) To obtain access to the KG Test Adapter and Extender cards, unlock the four cam-lock fasteners which secure the metal cover plate to the top portion of the case.

(2) *Remote control unit carrying case.*

(a) Place the carrying case on a suitable working surface.

(b) Using a screw driver, rotate the air relief valve, located on the front of the case, to its extreme counterclockwise position.

WARNING: THE CARRYING CASE IS SHIPPED IN AN AIRTIGHT CONDITION AND REQUIRES PRESSURE EQUALIZATION PRIOR TO BEING OPENED. PERSONNEL MAY BE SERIOUSLY INJURED IF THE AIR RELIEF VALVE IS NOT FIRST OPENED.

(c) Unlock the eight over-center hold-down clamps and remove the top portion of the case.

(d) Unfasten the retaining straps and remove the Remote Control Unit and cable assemblies.

3002. Inspection Procedure and Damage Report.—Carefully inspect the equipment to see if it was damaged in shipment. If damage is apparent, it shall be reported in accordance with those instructions issued by the Department or Agency having custody of the equipment.

Note: Navy holders shall report cases of damage in accordance with regulations prescribed by the Bureau of Ships.

3100—INSTALLATION

3101. Special Tools and Test Equipment Required.—The KW-7 requires no special tools to perform installation or maintenance. Table 3-2 defines the test equipment needed to perform both installation and maintenance.

TABLE 3-2

TEST EQUIPMENT REQUIRED FOR INSTALLATION AND/OR MAINTENANCE

Test Equipment	Required For	Supplied
KG Test Adapter Card	Maintenance	With KW-7
Extender Card	Maintenance	With KW-7
Multimeter, Triplett 630 or equivalent	Installation and Maintenance	By User
Oscilloscope, Tektronix 535 or equivalent	Installation and Maintenance	By User
Electronic Counter, Hewlett-Packard 525D or equivalent	Installation and Maintenance	By User
Power Supply Extender Cable (W20)	Maintenance	With spare parts kit

3102. Locating the KW-7.

a. Security Restrictions.—The KW-7 equipment must be installed in an area which has been approved for the installation of equipments having the classification of "CONFIDENTIAL—CRYPTO". Uncleared personnel shall not have free access to the equipment.

b. Environmental Conditions.—Table 3-3 defines the environmental conditions under which the KW-7 will satisfactorily operate.

TABLE 3-3

KW-7 EQUIPMENT ENVIRONMENTAL CONDITIONS

Environmental Condition	Minimum Value	Maximum Value
Altitude	Sea level	50,000 feet
Humidity	zero percent	95 percent
Ambient Temperature	−40°C (−40°F)	50°C (122°F)

3103. Preparation for Installation.—Prior to performing any installation procedures, it may be desirable to make the following checks.

a. Continuity Tests.—Using a multimeter, check for continuity in the interconnecting cables.

b. Fuse Check.—Remove the four fuses, located on the rear of the KW-7 and check the value of each. Check each fuse for signs of damage, replace those which appear to be damaged. Table 3-4 defines the individual fuse ratings.

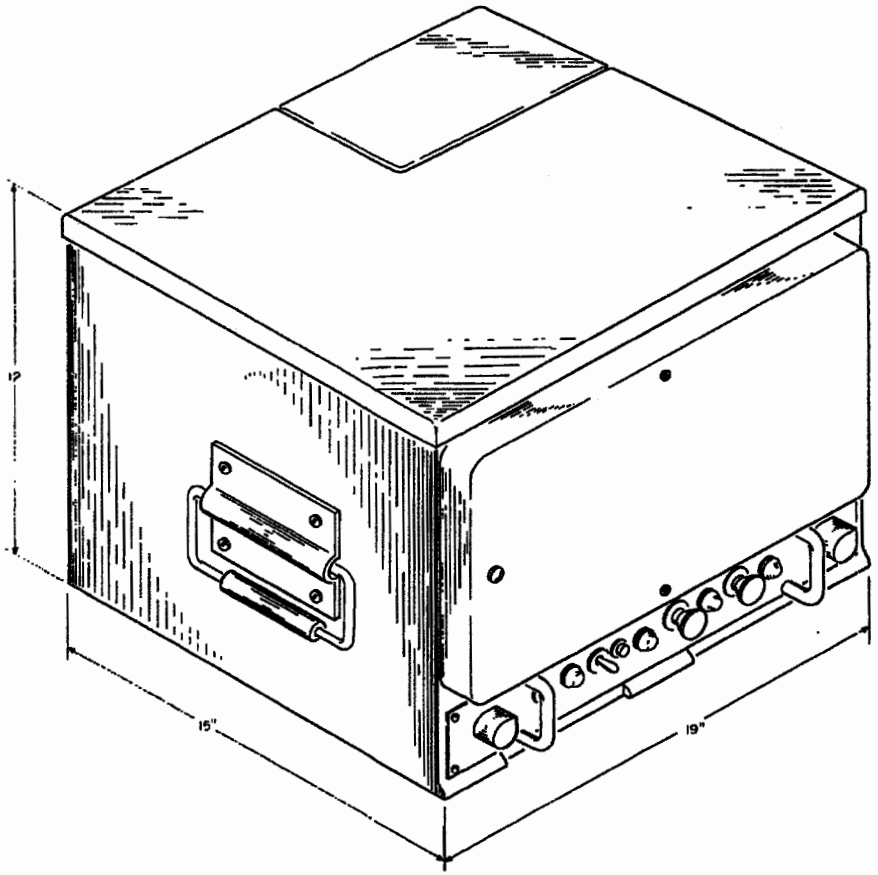


Figure 3-3.—Space Requirements for Bench Mounting.

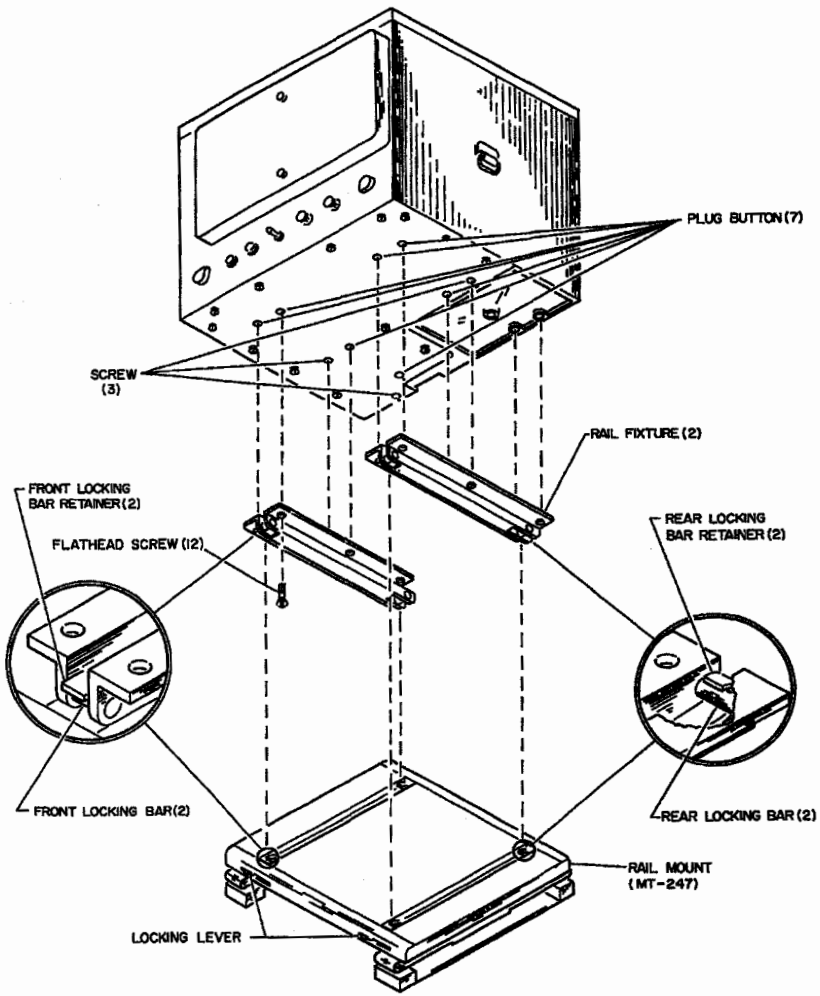


Figure 3-4.—Rail Mount Installation.

TABLE 3-4

FUSE RATINGS

Panel Marking	Rating (amp)
−24 VDC	5
+24 VDC	5
115/230 VAC	2
115/230 VAC	2

3104. Installation Procedures.—The KW-7 is designed for several types of installations; bench mount, rail mount, vibration mount, fixed slide mount, fixed rack mount and pivotal slide mount. The pivotal slide mount allows the KW-7 to be pivoted 90 degrees up or 45 degrees down when the slide is fully extended, thus providing ease of maintenance. The following procedures describe the steps required for each installation.

a. *Bench Mount* (*fig. 3-3*).—The only requirement to bench mount the KW-7 is the assurance of adequate space for maintenance and operation.

b. *Rail Mount* (*MT-297 Vehicular Mount*) (*fig. 3-4*).—The KW-7 equipment is adaptable for rail mounting in aircraft and small vehicles. The following steps describe the procedure to rail mount the KW-7 equipment:

(1) Remove the indicate 3 mating hole screws and seven plug buttons and store them in a suitable receptacle to prevent loss.

(2) Align the two rail fixtures so that the front locking bars face the front of the KW-7 equipment.

(3) Install and tighten 12 flathead screws to secure the rail fixtures to the bottom plate of the KW-7.

(4) With the two locking levers fully seated in the left-hand position, place the KW-7 on the mount so that the rail fixtures are positioned in the retainer recesses.

(5) Pull the two locking levers 90 degrees to the right. This locks the KW-7 to the rail mount.

Note: To remove the KW-7 equipment from the rail mount, reverse the installation procedure.

c. *Vibration Mount* (*fig. 3-5*).—The KW-7 is adaptable for vibration mounting in aircraft, ships, and large vehicles. The following steps describe the procedure to perform vibration mounting:

(1) Rotate the three hold-down clamp butterfly nuts counterclockwise until the three hold-down clamp bars can be rotated 90 degrees to the left.

(2) Slide the KW-7 equipment onto the vibration mount until the two mating holes located on the lower rear of the KW-7 are seated against the two guide pins located in the rear of the vibration mount.

(3) Rotate the three hold-down clamp bars 90 degrees to the right and tighten the three butterfly nuts until the three hold-down clamps are seated firmly against the three protrusions on the front of the KW-7 equipment chassis.

Note: To remove the KW-7 from the vibration mount, reverse the installation procedure.

d. *Fixed Slide Mount* (*fig. 3-6*).—The KW-7 equipment is adaptable for slide mounting on standard 19-inch racks in fixed installations or in large mobile installations. The following steps describe the procedure to perform slide mounting:

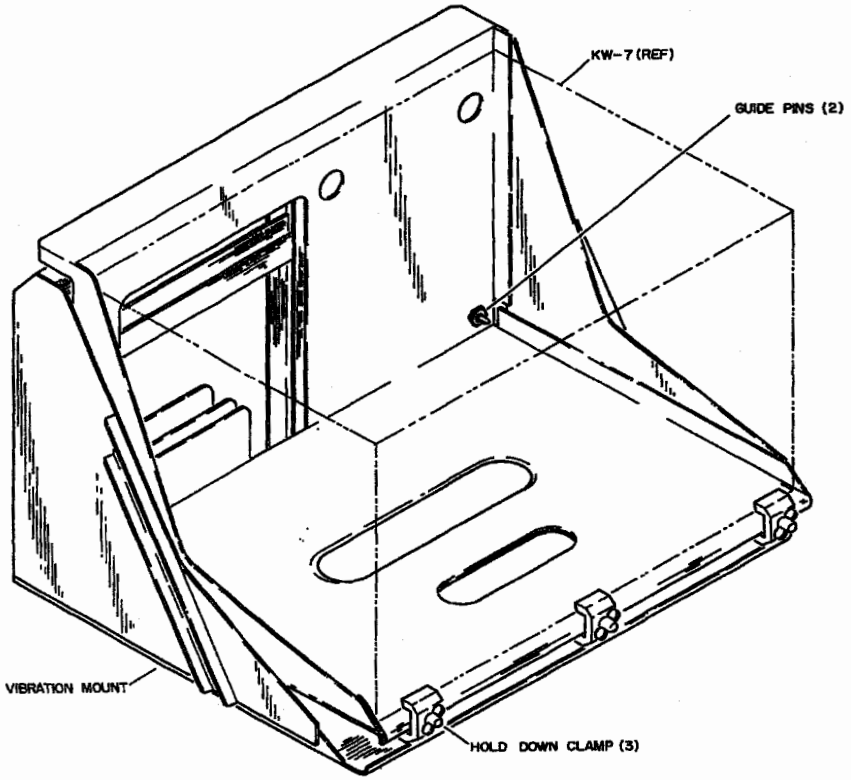


Figure 3-5.—Vibration Mount Installation.

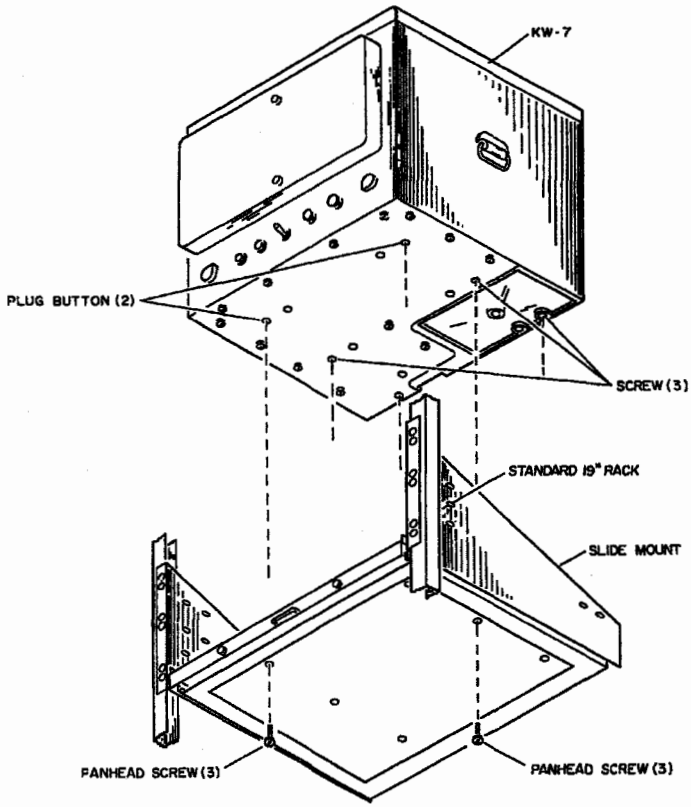


Figure 3-6.—Fixed Slide Mount Installation.

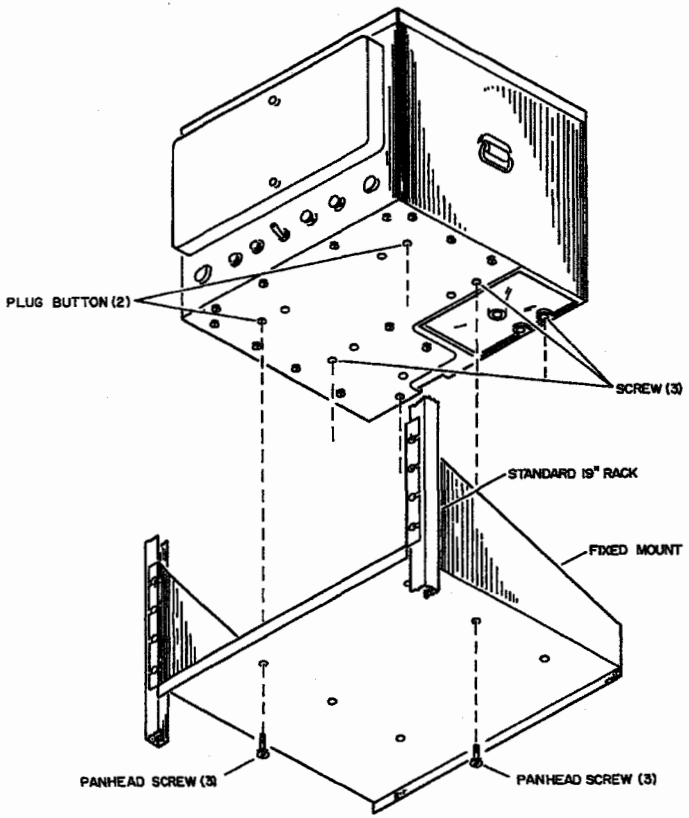


Figure 3-7.—Fixed Mount Installation.

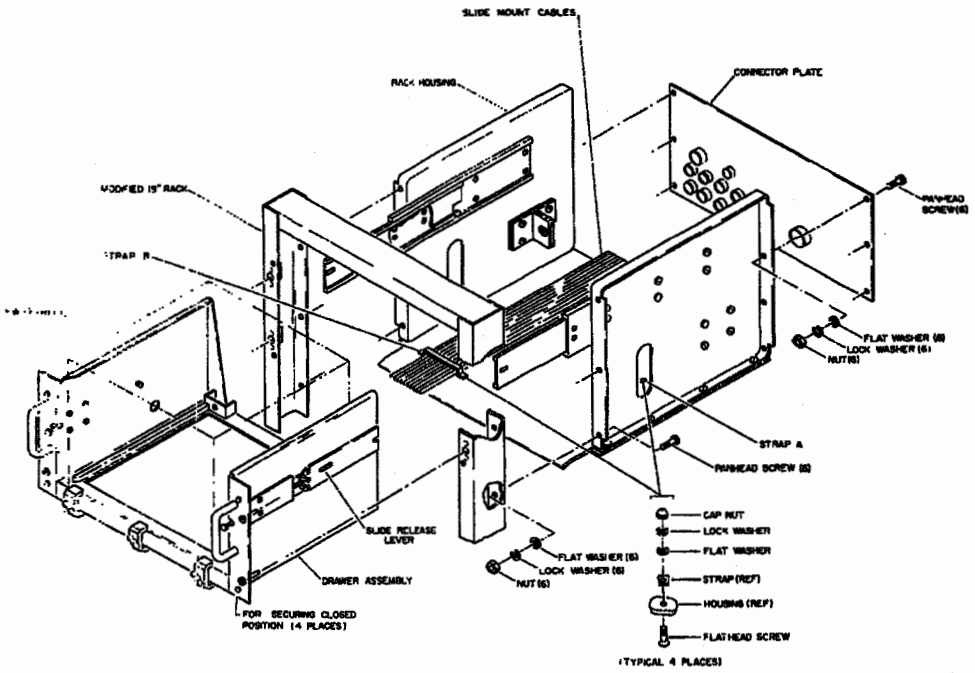
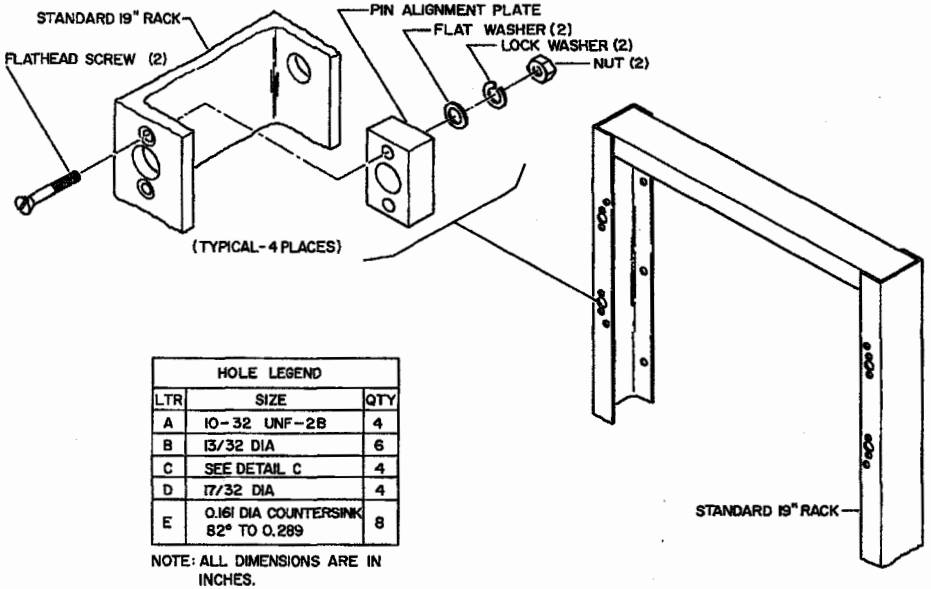


Figure 3-8.—Pivotal Slide Mount, Rack Type Mounting.



HOLE LEGEND		
LTR	SIZE	QTY
A	10-32 UNF-2B	4
B	13/32 DIA	6
C	SEE DETAIL C	4
D	17/32 DIA	4
E	0.161 DIA COUNTERSINK 82° TO 0.289	8

NOTE: ALL DIMENSIONS ARE IN INCHES.

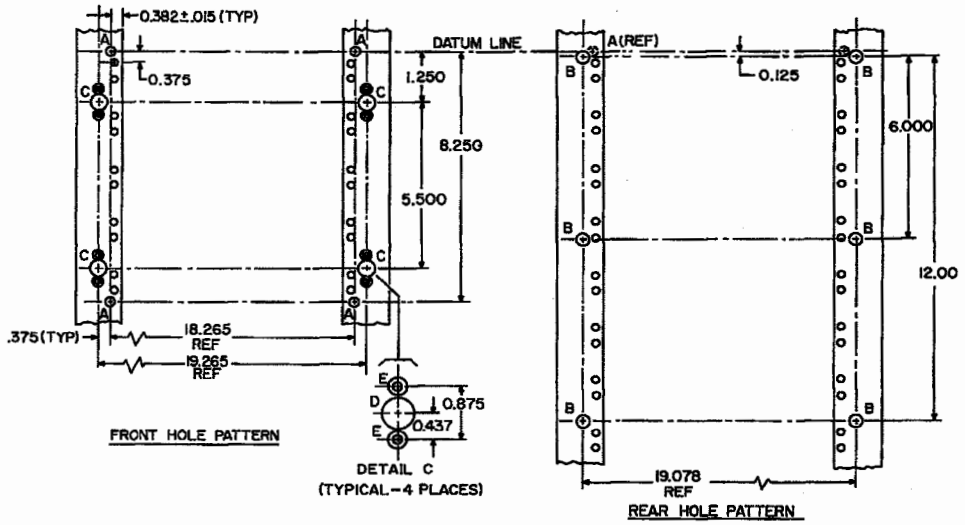


Figure 3-9.—Modification of Standard 19-Inch Rack.

(1) Remove the indicated 3 mating hole screws and 2 plug buttons from the bottom plate of the KW-7 and store them in a suitable receptacle to prevent loss.

(2) Extend the sliding plate to its full length and lower the KW-7 onto the mounting plate taking care to align the screw holes in the mount with the KW-7 mounting plate holes.

(3) Insert and tighten the 6 panhead screws provided with the slide mount and determine that the KW-7 equipment is securely fastened to the sliding plate.

(4) Return the slide to its normal position.

Note: To remove the KW-7 from the slide mount, reverse the installation procedure.

e. *Fixed Mount (fig. 3-7)*.—The KW-7 is adaptable for fixed mounting on standard 19-inch racks in fixed installations or in large mobile installations. The following steps describe the procedure to perform fixed rack mounting.

(1) Remove the indicated 3 mating hole screws and 2 plug buttons from the bottom plate of the KW-7 and store them in a suitable receptacle to prevent loss.

(2) Fasten the fixed mount in a standard 19-inch rack and place the KW-7 on the fixed mount. Carefully align the screw holes in the bottom of the fixed mount with the KW-7 bottom plate mating holes.

(3) Insert and tighten the 6 panhead screws provided with the fixed mount and determine that the KW-7 is securely fastened to the fixed rack mount.

Note: To remove the KW-7 from the fixed mount, reverse the installation procedure.

f. *Pivotal Slide Mount, Rack Type Mounting (fig. 3-8)*.—Installation of the KW-7 on the rack type mounting of the pivotal slide mount is accomplished in three phases: modification of a standard 19-inch rack to accommodate the mount, assembly and installation of the mount and, finally, installation of the KW-7 on the mount.

(1) *Rack modification (fig. 3-9)*.—The standard 19-inch rack is modified in the following manner:

(a) Drill and tap four holes (hole legend A) in the front side of the rack's channels. Observe spacing shown in the "front hole pattern".

(b) Drill holes per detail C hole pattern (hole legend D and E) at four places in the front side of the rack's channels. Observe spacing shown in the "front hole pattern" and detail C.

(c) Drill six holes (hole legend B) in the rear side of the rack's channels. Observe spacing shown in the "rear hole pattern".

(d) Install the four pin alignment plates inside the channels at the C locations and secure each to the front side of the rack with two flathead screws, flat washers, lock washers and nuts.

(2) *Mount assembly and installation*.—The mount consists of three assemblies: the housing, the connector plate and the drawer. The assembly of the housing and installation of the three assemblies is as follows:

(a) *Housing assembly (fig. 3-10)*.

1. Secure the bottom plate to the right-hand side and the left-hand side at eight places with a flathead screw, flat washer, lock washer, and nut.

2. Position one support bracket and shim on each housing side, and secure them at four places each with a panhead screw, flat washer, lock washer and nut.

(b) *Housing installation (fig. 3-8)*.

1. Position the housing on the rear side of the rack.

2. Align the holes in the front of the housing's sides with the six B holes (see fig. 3-9) and secure the housing at six places with a hex-head screw, flat washer, lock washer and nut.

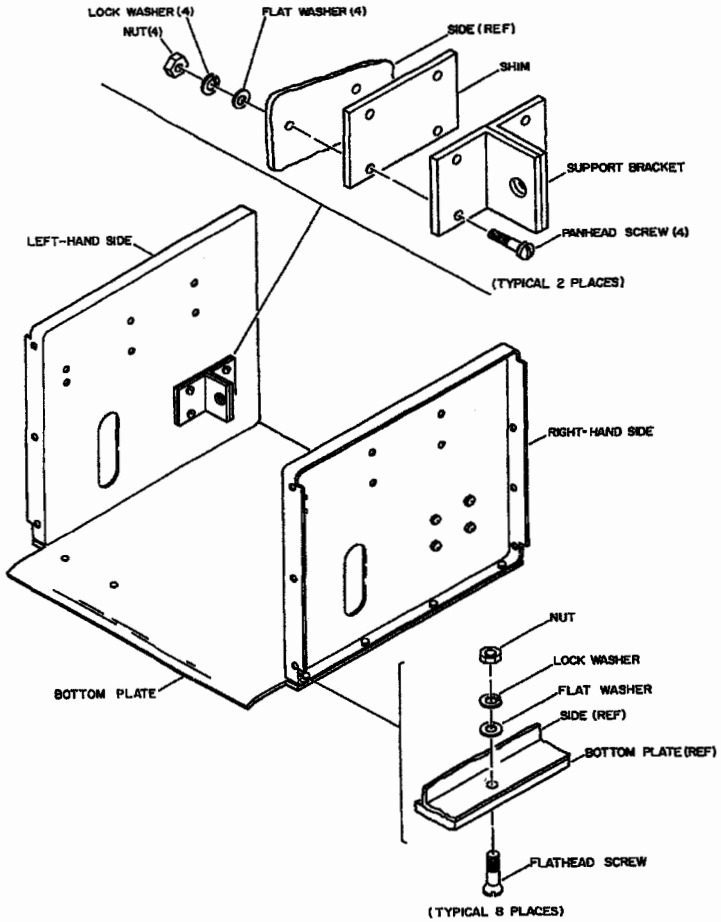


Figure 3-10.—Housing Assembly, Rack Installation.

(c) *Connector plate installation (fig. 3-8).*—Position the connector plate on the rear of the housing and secure it with six panhead screws, flat washers, lock washers and nuts.

(d) *Drawer installation (fig. 3-8).*

1. Trip the release lever on both slides and remove the slide assemblies from the drawer.
2. Fully extend the slides and align the mounting holes in each with the six corresponding holes in each housing side.
3. Secure each slide to the housing at six places with a flathead screw, flat washer, lock washer and nut.
4. Insert the drawer in the slides; check that the release levers are in the locked position.

(e) *Cable installation (figs. 3-8 and 3-11).*—Twelve special purpose cables are included for the purpose of allowing the KW-7, after the mounting, to be fully extended and pivoted without exerting stress on the system interconnecting cables.

1. Install the slide mount cables as follows:

Cable	Cable Connector	To Connector Plate Connector
W17	W17P2/5J7	J7
W16	W16P2/5J8	J8
W15	W15P2/5J9	J9
W14	W14P2/5J10	J10
W13	W13P2/5J3	J3
W12	W12P2/5J4	J4
W11	W11P2/5J5	J5
W10	W10P2/5J6	J6
W9	W9P1/5J1	J1
W8	W8P1/5J2	J2
W18	W18P1/5J11	J11
W19	W19/5E1	E1

2. Place cable W18 under retaining strap A, and secure the strap with a flathead screw, flat washer, lock washer and cap nut at two places.

3. Place all remaining cables under retaining strap B, and secure the strap with a flathead screw, flat washer, lock washer and cap nut at two places.

(3) *KW-7 Installation on mount (fig. 3-8).*

(a) Turn the three thumb-screws to the extreme counterclockwise position. Turn the clamps to the side.

(b) Slide the KW-7 between the rail guides until the guide pins located at the rear of the unit are fully seated in the receptacles provided at the rear of the unit.

(c) Position the three clamps upright and secure them in place by turning the three thumb-screws clockwise until tight.

(d) Pull the slide mount forward and install the mount cables as follows:

Cable	Cable Connector	To KW-7 Connector
W17 (Loop In 1)	W17P1/1A17J4	1A17J4
W16 (Loop In 2)	W16P1/1A17J3	1A17J3
W15 (DC Power)	W15P1/1A17J2	1A17J2
W14 (AC Power)	W14P1/1A17J1	1A17J1
W13 (Loop Out 2)	W13P1/1A17J8	1A17J8
W12 (Loop Out 1)	W12P1/1A17J7	1A17J7
W11 (PTS)	W11P1/1A17J6	1A17J6

Cable	Cable Connector	To KW-7 Connector
W10 (TD Step)	W10P1/1A17J5	1A17J5
W9 (Line Out)		1A17E4, 1A17E5, 1A17E6
W8 (Line In)		1A17E1, 1A17E2
W18 (Remote)	W18P1/1J1	1J1
W19 (Ground)	W19/1A17E3	1A17E3

(e) Pull forward on the knurled knobs and pivot the drawer up and down. Return the drawer to the horizontal position and run the slide forward and back; there should be no binding.

(f) Secure the slide in the closed position by means of the four retaining screws located on the front of the drawer.

(g) Connect the system interconnecting cables to the slide mount to set up the desired form of operation. (In the event that only one loop-input and/or one loop-output circuit is connected, install the jumper plugs, supplied with the KW-7 equipment, in the unused slide mount loop circuit connectors.)

g. Pivotal Slide Mount, Shelf Type Mounting (fig. 3-11).—Installation of the KW-7 on the shelf type mounting of the pivotal slide is accomplished by assembling the mount and then securing the unit to the mount.

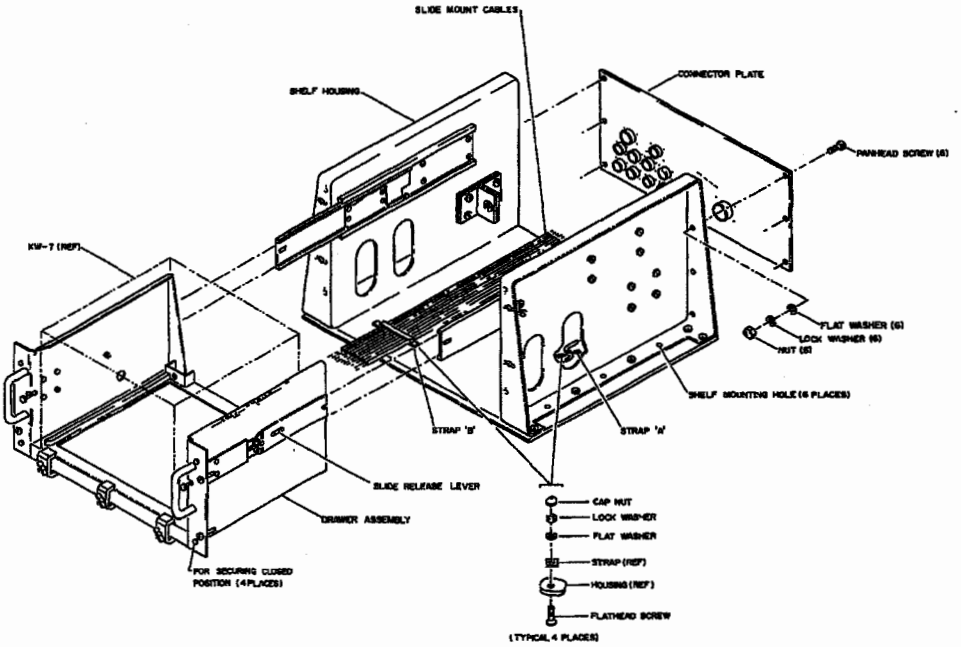


Figure 3-11.—Pivotal Slide Mount, Shelf Type Mounting.

(1) *Mount assembly.*—The mount consists of three assemblies: the housing, the connector plate and the drawer. The assembly of the housing and the installation of the three assemblies to form the mount is as follows:

(a) *Housing assembly (fig. 3-12).*

1. Secure the bottom plate to the right-hand side and the left-hand side at 12 places with a flathead screw, flat washer, lock washer and nut.
2. Position one support bracket and shim on each housing side, and secure them at four places each with a panhead screw, flat washer, lock washer and nut.
3. Secure each of the four pin alignment plates to the housing at the indicated points with two flathead screws, flat washers, lockwashers and nuts.

(b) *Housing installation.*—Secure the housing to the applicable mounting surface by means of attaching parts inserted through the six available holes in the bottom plate of the housing.

(c) *Connector plate installation (fig. 3-11).*—Position the connector plate on the rear of the housing and secure it with six panhead screws, flat washers, lock washers and nuts.

(d) *Drawer installation (fig. 3-11).*

1. Trip the release lever on both slides and remove the slide assemblies from the drawer.
2. Fully extend the slides and align the mounting holes in each with the six corresponding holes in each housing side.
3. Secure each slide to the housing at six places with a flathead screw, flat washer, lock washer and nut.
4. Insert the drawer's slides into the slide members secured to the housing; check that the release levers are in the locked position.

(e) *Cable installation.*—Installation procedures for the slide mount cables are the same as for rack type mounting (refer to paragraph 3104*f*(2)(e)).

(2) *KW-7 Installation on mount (fig. 3-11).*—The procedures for installing the KW-7 on the shelf type mounting are the same as for the rack type mounting (refer to paragraph 3104*f*(3)).

3105. System Interconnecting Wiring Procedures.—The necessary information for connecting the KW-7 in several types of operation is provided in the following tables. Table 3-5 lists the cables in general terms and table 3-6 lists the cabling connections required for a particular installation. The cables are identified by band markers connected adjacent to the plugs. The first part of the identification is the cable designator; the second part after the slash is the connector to which it can be mated. For instance, cable W1 is for the 230 VAC power input. One end of the cable is designated W1P1/1A17J1. This connects to 1A17J1 in the KW-7 filter unit. The other end is labled W1P2/230VAC. This connects to the 230VAC power source. Sometimes a cable can be connected to more than one equipment, (i.e. on the KW-7 or the Remote Control Unit). In this case, the band marker will list both connectors to which this cable may be connected. The type of operation used will determine the equipment to which this cable is connected. Table 3-6 pertains to system connections for using the KW-7 in plain synchronous and cipher modes only. For plain asynchronous mode operation, substitute a teletypewriter for a KW-7 as shown in figure 3-19. Note this configuration is applicable to two-wire neutral operation only. The other types of operation may be likewise converted to plain asynchronous mode use by replacing a KW-7 with a teletypewriter. In such instances, the KW-7 line-out circuit must terminate at the page-printer terminals, while the KW-7 line-in circuit must terminate at the keyboard terminals. Connections for the additional circuit utilized in four-wire systems are to be made in the standard manner for the teletypewriter equipment in use.

Note: In all cable connections, insure a good ground connection between the units by securing the ground lead on each cable connector to an adjacent screw on the teletypewriter equipment.

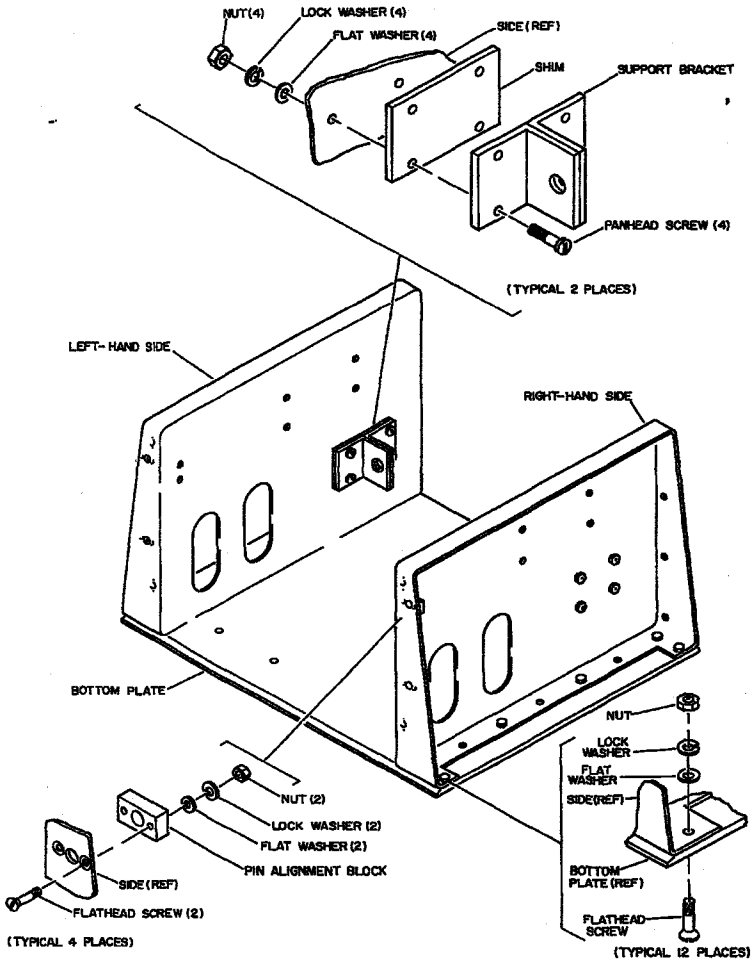


Figure 3-12.—Housing Assembly, Shelf Installation.

TABLE 3-5

KW-7 CABLE REQUIREMENTS

Cable Name	Reference Designator	Connector Identification	To
230 VAC	W1	W1P1/1A17J1	KW-7
		W1P2/230 VAC	Primary 230 VAC Power Source
115 VAC	W2	W2P1/1A17J1	KW-7
		W2P2/115 VAC	Primary 115 VAC Power Source
Two-Wire Loop Adapter (Loop-Out Operation)	W3	W3P1/1A17J7	KW-7
		W3P2/3J3	Two-Wire Loop Adapter
Two-Wire Loop Adapter (Loop-In Operation)	W3	W3P1/3J1	Two-Wire Loop Adapter
		W3P2/1A17J3	KW-7
Remote	W4	W4P1/1J1	KW-7
		W4P2/2J1	Remote Control Unit
		W4P2/4J1	Functional Remote Control Unit
TD Step	W5	W5P1/1A17J5	KW-7
		W5P1/2J7	Remote Control Unit
		W5P1/4J2	Functional Remote Control Unit
		TTY TD Step	Step Transmitter Distributor
Loop Input (One Loop-In Operation)	W6	W6P1/1A17J3	KW-7
		W6P1/2J3	Remote Control Unit
		TTY Output	Teletypewriter Keyboard
Loop Input (Two Loop-In Operation)	W6	W6P1/1A17J4	KW-7
		W6P1/2J4	Remote Control Unit
		TTY Output	Teletypewriter Keyboard
Loop Output (One Loop-Out Operation)	W7	W7P1/1A17J7	KW-7
		W7P1/2J5	Remote Control Unit
		TTY Input	Teletypewriter Page Printer
Loop Output (Two Loop-Out Operation)	W7	W7P1/1A17J8	KW-7
		W7P1/2J6	Remote Control Unit
		TTY Input	Teletypewriter Page Printer
Pivotal Slide Mount Cables: Line In	W8	W8P1/5J2	Slide Mount
			KW-7

TABLE 3-5 (Continued)

Cable Name	Reference Designator	Connector Identification	To
Line Out	W9	W9P1/5J1	Slide Mount KW-7
TD Step	W10	W10P2/5J6 W10P1/1A17J5	Slide Mount KW-7
PTS (optional)	W11	W11P2/5J5 W11P1/1A17J6	Slide Mount KW-7
Loop Out - 1	W12	W12P2/5J4 W12P1/1A17J7	Slide Mount KW-7
Loop Out - 2	W13	W13P2/5J3 W13P1/1A17J8	Slide Mount KW-7
AC Power	W14	W14P2/5J10 W14P1/1A17J1	Slide Mount KW-7
DC Power	W15	W15P2/5J9 W15P1/1A17J2	Slide Mount KW-7
Loop In - 1	W16	W16P2/5J8 W16P1/1A17J3	Slide Mount KW-7
Loop In - 2	W17	W17P2/5J7 W17P1/1A17J4	Slide Mount KW-7
Remote	W18	W18P2/5J11 W18P1/1J1	Slide Mount KW-7
Ground	W19	W19/5E1 W19/1A17E3	Slide Mount KW-7
DC Power			Connector furnished; cable to be fabricated by user.

TABLE 3-6

KW-7 CABLE AND WIRING CONNECTIONS

Type of Connection	Cable	Wire	Connector	To	Fig. No.	Comments
Primary Power Sources						
115 VAC	W2		W2P1/1A17J1	KW-7, Connector A17J1	3-13 thru 3-19	None
			W2P2/115VAC	Primary Power Source	3-13 thru 3-19	None

TABLE 3-6 (Continued)

Type of Connection	Cable	Wire	Connector	To	Fig. No.	Comments
230 VAC	W1		W1P1/1A17J1	KW-7, Connector A17J1	3-13 thru 3-19	None
			W1P2/230VAC	Primary Power Source	3-13 thru 3-19	None
24V DC				KW-7, Connector A17J2 (positive lead to pin A, negative lead to pin C and ground lead to pin B; cable to be fabricated by user)	3-13 thru 3-19	None
Loop Modes of Operation						
Loop Input	W6		W6P1/1A17J3	KW-7, Connector A17J3	3-13 thru 3-19	If only one Loop-In connector is used it will be necessary to insert the jumper plug in Loop-In Connector A17J4.
			TTY OUTPUT	Teletypewriter keyboard	3-13 thru 3-19	None
Loop Output	W7		W7P1/1A17J7	KW-7, Connector A17J7	3-13 thru 3-19	If only one Loop-Out connector is used it will be necessary to insert the jumper plug in Loop-Out connector A17J8.
			TTY INPUT	Teletypewriter Page Printer	3-13 thru 3-19	None
TD Step	W5		W5P1/1A17J5	KW-7, Connector A17J5		Stepping clutch magnet coil.
			TTY TD STEP	Transmitter Distributor		None
Remote Control	W4		W4P1/1J1	KW-7, Connector J1	3-14	None
			W4P2/2J1	Remote Control Unit, Connector J1	3-14	None
Remote Control Unit Loop Input	W6		W6P1/2J4	Remote Control Unit, Connector J4	3-14	If only one Loop-In connector is used it will be necessary to insert the jumper plug in Loop-In connector J3.
			TTY OUTPUT	Teletypewriter keyboard	3-14	None

TABLE 3-6 (Continued)

Type of Connection	Cable	Wire	Connector	To	Fig. No.	Comments
Remote Control Unit Loop Output	W7		W7P1/2J5	Remote Control Unit, Connector J5	3-14	If only one Loop-Out connector is used it will be necessary to insert the jumper plug in Loop Out connector J6.
			TTY INPUT	Telstypewriter Page Printer	3-14	None
Remote Control Unit TD	W6		W6P1/2J3	Remote Control Unit, Connector J8.	3-14	None
			TTY OUTPUT	Transmitter-Distributor	3-14	None
Two-Wire Loop Adapter Unit Loop Output	W3		W3P1/1A17J7	KW-7, Connector A17J7	3-18	The jumper plug must be inserted in Loop Out connector A17J8.
			W3P2/3J3	Two-Wire Loop Adapter Connector J8	3-18	None
Two-Wire Loop Adapter Unit Loop Input	W3		W3P1/3J1	Two-Wire Loop Adapter Connector J8	3-18	None
			W3P2/1A17J3	KW-7, Connector A17J3	3-18	The jumper plug must be inserted in Loop Out connector A17J4.
Two-Wire Loop Adapter Unit, Two-Wire Loop		X	Two-Wire Loop Adapter Unit Connector J2, pin C	One side of 7K potentiometer 2.	3-18	None
		X	Telstypewriter keyboard	The other side of the 6K potentiometer, through a 1K5W resistor	3-18	None
		X	Two-Wire Loop Adapter Unit, Connector J2, pin B	Negative side of the DC voltage Source	3-18	None
		X	Page Printer Input	Positive side of DC voltage source	3-18	None
Functional Remote Control Unit	W4		W4P1/1J1	KW-7, Connector J1	3-18	None
			W4P2/4J1	Functional Remote Control Unit, Connector J1	3-18	None

TABLE 3-6 (Continued)

Type of Connection	Cable	Wire	Connector	To	Fig. No.	Comments
	W5		W5P1/4J2	Functional Remote Control Unit, Connector J2	3-18	None
			TTY TD STEP	Step Transmitter Distributor	3-18	None
Line Modes of Operation						
Two-Wire Neutral		X	A17E5, located on Station A	A17E1, located on Station B	3-13	None
		X	A17A1, located on Station A	Positive terminal of 120 VDC line battery	3-13	None
		X	A17E5, located on Station B	Through 7K potentiometer to negative terminal of 120 VDC line battery.	3-13	None
		X	A17E2 to A17E4, located on both KW-7's		3-13	This jumper wire is only used for Two-Wire Neutral Operation.
		X	A17E3, located on both KW-7's.	Earth Ground	3-13	None
Two-Wire Polar		X	A17E2, located on Station A.	Common point of DC voltage source 1 and 2, which is connected to earth ground.	3-15	None
		X	A17E1, located on Station A.	One side of a 7K, 25 watt potentiometer 1.	3-15	None
		X	A17E4, located on Station A.	Positive side of DC voltage source 1.	3-15	None
		X	A17E5 located, on Station A.	One side of 7K, 25 watt potentiometer 2.	3-15	None
		X	A17E6, located on Station A.	Negative side of DC voltage source 2.	3-15	None
		X	A17E3, located on both KW-7's.	Earth Ground	3-15	None
		X	A17E2, located on Station B.	Common point of DC voltage source 3 and 4, which is connected to earth ground.	3-15	None

TABLE 3-6 (Continued)

Type of Connection	Cable	Wire	Connector	To	Fig. No.	Comments
		X	A17E4, located on Station B.	Positive side of DC voltage source 3.	3-15	None
		X	A17E5, located on Station B.	Other side of 7K, 25 watt potentiometer 1.	3-15	None
		X	A17E6, located on Station B.	Negative side of DC voltage source 4.	3-15	None
		X	A17E1, located on the receiving KW-7.	Other side of 7K, 25 watt potentiometer 2.	3-15	None
Four-Wire Neutral		X	A17E1, located on Station A.	Positive side of DC voltage source 2.	3-16	None
		X	A17E2, located on Station A.	A17E4, located on Station B.	3-16	None
		X	A17E3, located on Station A.	Earth Ground.	3-16	None
		X	A17E5, located on Station A.	Negative side of DC voltage source 1.	3-16	
		X	A17E4, located on Station A.	E2, located on Station B.	3-16	None
		X	A17E1, located on Station B.	Through 7K, 25 watt potentiometer 1 to positive side of DC voltage source 1.	3-16	None
		X	A17E3, located on Station B.	Earth Ground.	3-16	None
		X	A17E5, located on Station B.	Through 7K, 25 watt potentiometer 2 to negative side of the DC voltage source 2.	3-16	None
Four-Wire Polar		X	A17E1, located on Station A.	One side of 7K, 25 watt potentiometer 1.	3-17	None
		X	A17E2, located on Station A.	Common point for DC voltage source 3 and 4, which is connected to earth ground.	3-17	None
		X	A17E3, located on Station A.	Common point for DC voltage source 1 and 2, which is connected to earth ground.	3-17	None
		X	A17E4, located on Station A.	Positive side of DC voltage source 2.	3-17	None

TABLE 3-6 (Continued)

Type of Connection	Cable	Wire	Connector	To	Fig. No.	Comments
		X	A17E5, located on Station A.	One side of 7K, 25 watt potentiometer 2.	3-17	None
		X	A17E6, located on Station A.	Negative side of DC voltage source 1.	3-17	None
		X	A17E1, located on Station B.	The other side of potentiometer 2.	3-17	None
		X	A17E2, located on Station B.	Common point of DC voltage source 1 and 2.	3-17	None
		X	A17E3, located on Station B.	Common point of DC voltage source 3 and 4.	3-17	None
		X	A17E4 located on Station B	Positive side of DC voltage source 4.	3-17	None
		X	A17E5 located on Station B	The other side of potentiometer 1.	3-17	None
		X	A17E6 located on Station B.	Negative side of DC voltage source 3.	3-17	None
Aux. Timing Source						
AUX. 100KC INPUT			KW-7 Aux. 100KC input connector 1J2(TIP).	Positive side of 100KC signal source.		
			KW-7 Aux. 100KC input connector 1J2 (Ring)	Negative side of 100KC signal source.		

3106. Teletypewriter Connections.—Table 3-7 lists several types of teletypewriter equipments that may be used with the KW-7. Sometimes connections are given for Loop-In 1 and 2 and also Loop-Out 1 and 2. If only one Loop-In or one Loop-Out is desired, use the jumper plug in the unused KW-7 Loop circuit jack. The technical manuals are also listed for several teletypewriter equipments. Special information such as bypassing filters in the Loop-In circuit etc. is included in the "Type Teletypewriter" column of Table 3-7.

TABLE 3-7

TELETYPEWRITER LOOP CONNECTIONS

Type Teletypewriter	Loop In No. 1		Loop In No. 2		Loop Out No. 1		Loop Out No. 2	
	Pin A	Pin B	Pin A	Pin B	Pin A	Pin B	Pin A	Pin B
AN/FGC-25, 25X, 26, 57 (TM11-2246) (To 31W4-2FGC25-1) (Bypass Filters Z2 and Z3)	Term "A" Line No. 1	Term "B" Line No. 1	Jumper Plug		Term "A" Line No. 2	Term "B" Line No. 2	Jumper Plug	
AN/GGC-3, TT-76 (Bypass Filters Z3 and Z4)	TB2 Term 1	TB2 Term 2	TB2 Term 6	TB2 Term 7	TB2 Term 4	TB2 Term 5	Jumper Plug	
AN/GG-C, TT-76-A (Bypass Filters FL1 and FL2)	TB1 Term 1	TB1 Term 2	TB1 Term 6	TB1 Term 7	TB1 Term 4	TB1 Term 5	Jumper Plug	
AN/FGC-20, 20X, 21, UGC-4, TT98, 99, 100, 100B (TM11-2230) (Bypass Filter Z2)	Term and Sw. Box 2	Term and Sw. Box 5	Jumper Plug Turn R10 Completely CCW and DC Switch S11 to OFF.		Term and Sw. Box 3	Term and Sw. Box 4	Jumper Plug	
Model 15 (Bypass Filter 92222 and condensor 93883)	Term 32	Term 34	Jumper Plug		Term 41	Term 42	Jumper Plug	
Model 14 Reperforator					Term 31	Term 32	Jumper Plug	
AN/TGC-5, 54 (TM11-2249-25) (Bypass Filters FL1 and FL5)	Term "A" Line 3	Term "B" Line 3	Term "A" Line 1	Term "B" Line 1	Term "A" Line 4	Term "B" Line 4	Term "A" Line 2	Term "B" Line 2
TT-47A, 48A, 69A, 70A (Model 28) (NAVSHIPS 91713) (On TB751, hook green wire from pin 9 to pin 6. Remove jumper between pins 6 and 7. Connect jumper between pins 8 and 9)	TB 751 Term 7	TB 751 Term 8	Jumper Plug		TB 751 Term 5	TB 751 Term 10	Jumper Plug	
AN/UGC5, 6 (Remove jumper between C8 and C9. Move slate wire from C7 to C9)	Term C5	Term C15	Jumper Plug		Term C7	Term C8	Jumper Plug	
AN/TGC-3 (TM11-680) (To 16-1-117) (Remove Filter "BB")	TBA Term 11	TBA Term 12	Jumper Plug		TBA	TBA	Jumper Plug	

TABLE 3-7 (Continued)

Type Teletypewriter	Loop In No. 1		Loop In No. 2		Loop Out No. 1		Loop Out No. 2	
	Pin A	Pin B	Pin A	Pin B	Pin A	Pin B	Pin A	Pin B
TT-4, (TM11-2234) (To 16-35TT-4-5) (Connect shorting bar from terminal 5 to terminal 6. Remove shorting bar between terminals 2 and 3. Set Switch S4 to "DC Line.")	Term 1	Term 2	Jumper Plug		Term 3	Term 4	Jumper Plug	
TT-26C and 27A (TM11-680) (To 16-1-117)	Term 7	Term 8	Term 3	Term 4	Term 1	Term 2	Jumper Plug	
Model 19 (Strap Term 1 and 6. Also remove internal battery from Model 19.)	Term 3 E603	Term 4 E603	Jumper Plug		Term 2 E603	Term 5 E603	Jumper Plug	
TT-5/FG (TM11-2215) (To 16-35775-61)	Term 32	Term 34	Jumper Plug		Term 41	Term 42	Jumper Plug	
TT-7/FG (TM11-2216)	Term 2 "C" Block	Term 5 "C" Block	Term 5 "D" Block	Term 6 "D" Block	Term 3 "C" Block	Term 4 "C" Block	Jumper Plug	

3200—ADJUSTMENT, TESTING AND OPERATION

3201. Adjustments.

a. Introduction.—Before any adjustments are made or the power is turned on, the permuter cords must be set up. To achieve cryptographic synchronization, both KW-7 permuter patch cord arrangements must be set the same. Arrange them as shown in table 3-8. Also the switches should be set as shown in table 3-9.

WARNING: THE PATCH CORDS MUST NEVER BE SET AS SHOWN IN TABLE 3-8 WHEN THE KW-7 IS CONNECTED TO THE LINE.

TABLE 3-8

PATCH CORD TEST ARRANGEMENT

From Combiner Board Jack	To Register Card Terminal	From Combiner Board Jack	To Register Card Terminal
1	A1	16	C16
2	A2	17	D17
3	A3	18	D18
4	A4	19	D19
5	A5	20	D20
6	A6	21	D21
7	B7	22	D22
8	B8	23	E23
9	B9	24	E24
10	B10	25	E25
11	C11	26	F26
12	C12	27	F27
13	C13	28	F28
14	C14	29	F29
15	C15	30	F30

TABLE 3-9

PRELIMINARY SWITCH SETTINGS

Switch	Fig. No.	Position
ALARM	2-4A	ON
LINE INPUT	2-4A	20 or 60 milliamperes (to be determined by the line)
Loop Mode (Located on Card E-AJV)	2-4A	Forward (60 milliamperes) or rear (20 milliamperes) (depends on loop-out circuit)
TD-STEP	2-4A	STEP OR CONT (depends on TD)
LOOP INHIBIT/ALLOW	2-4A	ALLOW
WPM SPEED SELECTOR	2-10	60, 67, or 100 (determined by teletypewriter speed)
BREAK FUNCTION	2-10	ON
115V/230V*	2-10	115V or 230V (depends on AC source)
PCR	2-14	PLAIN-SYNC
ALARM TEST	2-14	OFF
POWER	2-14	ON.

* If 24 VDC is used, this switch is not connected in the circuit.

b. Preliminary Adjustments.

(1) *Power supply.*—Remove the power supply top cover and, using a multimeter, measure the voltages indicated in table 3-10 and make any adjustments necessary to bring the voltages to the proper level.

WARNING: EXERCISE CARE WHEN MAKING THE MEASUREMENTS AND ADJUSTMENTS. HIGH VOLTAGES ARE PRESENT IN THE EQUIPMENT.

TABLE 3-10

POWER SUPPLY OUTPUT VOLTAGE MEASUREMENTS/ADJUSTMENTS

Voltage	From Test Point	To Test Point	Voltage Adjustment	Adjust For
+6V	J3	J2 (GND)	+6V ADJ	+6V ±3%
−6V	J4	J2 (GND)	−6V ADJ	−6V ±3%
−18V	J5	J2 (GND)	−18V ADJ	−18V ±2%
−24V	J6	J2 (GND)	−24V ADJ	−24V ±3%
−53V	J1	J2 (GND)	−53V ADJ	−53V ±5%

(2) *Loop-Out current.*

(a) Using the multimeter as an ammeter, place it in series between the spade lug on the end of one of the loop output leads from J7 and its corresponding terminal on the teletypewriter, leaving the other loop output lead connected to the teletypewriter.

(b) Adjust teletypewriter loop-out current control (if one is used) to the maximum current position.

(c) Adjust the LOOP OUTPUT ADJUST potenitometer (located at the top of the KW-7) until a reading of either 20 or 60 milliamperes, as determined by the teletypewriter in use, is observed on the multimeter.

(3) *Line In.*

(a) Using the multimeter as an ammeter, place the meter in series with terminal E1 (line-in) and the line battery.

(b) Adjust the 7K, 25 watt potentiometer, included in the line circuit, until the ammeter indicates a reading of either 20 or 60 milliamperes, as determined by the line.

Note: If polar operation is employed, both sides of the line will have to be adjusted until the meter indicates a reading of +20 or +30 milliamperes on the mark side and −20 or −30 milliamperes on the space side. The reading will depend on the line current used.

3202. Testing.—Prior to placing the KW-7 equipment in normal traffic operation, it will be necessary to determine that the functional units within the equipment are operating properly. This may be accomplished by performing various tests on the equipment in an off-line condition. The tests which are required to determine the operational status of the equipment are divided into two categories: back-to-back local and back-to-back remote operation. Both back-to-back tests simulate actual on-line conditions. In the event that local requirements dictate the use of the Functional Remote Control Unit and/or the Loop Adapter Unit, the back-to-back testing should include steps to verify the operational status of the equipment. All personnel operating

the KW-7 equipment, either on-line or in a test phase, should familiarize themselves with and be guided by the affective edition of KAO-83/TSEC, the equipment operating manual.

WARNING: THE TOP COVER, BOTTOM COVER, AND PERMUTER PATCHCORD COVER MUST BE SECURELY FASTENED ON THE KW-7 WHEN IT IS BEING USED TO TRANSMIT OR RECEIVE CLASSIFIED TRAFFIC

a. *Local Back-to-Back Operational Test.*—The following paragraphs describe those tests required to determine the operational capability of the KW-7 when operated locally.

(1) Perform the wiring connections indicated in figure 3-13.

(2) Open the front cover on both equipments and check to be sure the permuting patch cords are connected as shown in table 3-8.

(3) Set the switches as shown in table 3-9. Note several options are given in the "position" column. The particular setting will depend on local operating conditions.

(4) Perform the steps indicated in table 3-11 and determine that the indicated response is normal. In the event that any action does not result in the normal response, it will be necessary to refer to Chapter 3 of KAM-144B/TSEC.

TABLE 3-11

LOCAL OPERATIONAL TEST

Action		Normal Response	
Station A Operator	**Station B Operator**	**Station A**	**Station B**
1. Depress the SEND pushbutton for five seconds.	None.	SEND and P&I indicator lamps come on. After completion of phasing and indicator cycle, P&I lamp goes out.	P&I indicator lamp comes on. After completion of phasing and indicator cycle, P&I lamp goes out.
2. Transmit a test message via the transmitter-distributor or keyboard.	None.	Page printer prints message.	Page printer prints message.
3. None.	Depress the BREAK pushbutton for five seconds.	BREAK indicator lamp and audible alarm come on and transmission stops.	BREAK indicator lamp and audible alarm come on.
4. None.	Depress the BREAK RESTORE pushbutton.	None.	BREAK indicator lamp and audible alarm go out.
5. None.	Depress the SEND pushbutton for five seconds.	P&I indicator lamp comes on and the BREAK indicator lamp and indicator lamp go out. After phasing and indicator cycle has been completed, P&I lamp goes out.	P&I indicator lamp comes on. After phasing and indicator cycle has been completed, P&I lamp goes out.
6. None.	Transmit a test message via the transmitter-distributor or keyboard.	Page printer prints message.	Page printer prints message.
7. Depress the BREAK pushbutton for five seconds.	None.	BREAK indicator lamp and audible alarm come on.	BREAK indicator lamp and audible alarm come on and transmission stops.

TABLE 3-11 (Continued)

Action		Normal Response	
Station A Operator	Station B Operator	Station A	Station B
8. Depress the BREAK RESTORE pushbutton.	None.	BREAK indicator lamp goes out and audible alarm goes off.	None.
9. Depress the SEND pushbutton for five seconds.	None.	P&I indicator lamp comes on. After phasing and indicator cycle has been completed, P&I lamp goes out.	P&I indicator lamp comes on and the BREAK indicator lamp and audible alarm go off. After phasing and indicator cycle has been completed, P&I lamp goes out.
10. Place PCR switch in CIPHER position.	Same as for Station A.	None.	None.
11. Rotate ALARM TEST switch through all test positions, pausing at each for five seconds.	Same as for Station A.	Observe occurrence of indications listed in Table 3-14 for each position.	Same as for Station A.
12. Repeat actions 1 through 9.	Same as for Station A.	Same.	Same.

b. Remote Back-to-Back Operational Test.—The only significant difference between this test and the preceding local test is that now a Remote Control Unit is attached to the KW-7. This permits remote control of the KW-7 up to a distance of 500 feet.

(1) Perform the wiring connections indicated in figure 3-14.

(2) Open the front cover on both equipments and check to be sure the permuting patch cords are connected as shown in table 3-8. Note several options are given in the "position" column. The particular setting used will be determined by the local operating conditions.

(3) Set the switches as shown in table 3-12.

TABLE 3-12

REMOTE OPERATION, SWITCH SETTINGS

Switch	Fig. No.	Position
ALARM	2-4	ON
LINE INPUT	2-4	20 or 60 milliamperes (to be determined by the line).
Loop Mode (Card E-AJV)	2-4	Forward (60 milliamperes), or rear (20 milliamperes) (depends on loop-out circuit).
TD-STEP	2-4	STEP or CONT (depends on TD).
LOOP INHIBIT/ALLOW	2-4	ALLOW
WPM SPEED SELECTOR	2-10	60, 67, or 100 (determined by teletypewriter speed).
BREAK FUNCTION	2-10	ON

TABLE 3-12 (Continued)

Switch	Fig. No.	Position
115/230*	2-10	115V or 230V (depends on AC source).
PCR (STATION B)	2-14	REMOTE
PCR (STATION A)	2-14	CIPHER
ALARM TEST	2-14	OFF
POWER	2-14	ON
PC (Remote Control Unit)	2-16	CIPHER

*If 24 VDC is used, this switch is not connected in the circuit.

(4) Perform the steps indicated in table 3-9 and determine that the indicated response is normal. In the event that any section does not result in the normal response, it will be necessary to refer to chapter 3 of KAM-144B/TSEC.

TABLE 3-13

REMOTE OPERATIONAL TEST

Action		Normal Response	
Station A Operator	Station B Operator	Station A Operator	Station B Operator
1. None.	Depress Remote Control Unit B SEND pushbutton for five seconds.	Station A P&I indicator lamp comes on. After completion of phasing and indicator cycle, Station A P&I indicator lamp will go off.	Remote Control Unit B and KW-7 Station B SEND and P&I indicator lamps come on. After completion of the phasing and indicator cycle, Remote Control Unit B and KW-7 Station B P&I indicator lamps will go off.
2. None.	Transmit a test message from the transmitter-distributor or keyboard.	Page Printer prints message.	Page Printer prints message.
3. Depress BREAK pushbutton for 5 seconds.	None.	Station A BREAK indicator and audible alarms come on.	Remote Control Unit B and KW-7 Station B BREAK indicator lamps and audible alarm come on and message transmission stops.
4. Depress BREAK RESTORE pushbutton.	None.	Station A BREAK indicator lamp and audible alarm goes off.	None.
5. Depress SEND pushbutton switch for 5 seconds.	None.	Station A SEND and P&I indicator lamps come on. After completion of phasing and indicator cycle, the P&I indicator lamps go out.	Remote Control Unit B and KW-7 Station B P&I indicator lamps come on, the BREAK indicator lamps and the audible alarms go off. After phasing and indicator cycle has been completed, P&I lamps go out.

TABLE 3-13 (Continued)

Action		Normal Response	
Station A Operator	Station B Operator	Station A Operator	Station B Operator
6. Transmit a test message from the transmitter-distributor or keyboard.	None.	Page Printer prints message.	Page Printer prints message.
7. None.	Depress Remote Control Unit B BREAK pushbutton for five seconds.	Station A BREAK indicator lamp and audible alarm come on. Also transmission stops.	Remote Control Unit B and KW-7 Station B BREAK indicator lamps and audible alarms come on.
8. None.	Depress Remote Control Unit B BREAK RESTORE pushbutton.	None.	Remote Control Unit B and KW-7 Station B BREAK indicator lamps and audible alarms come on.
9. None.	Depress Remote Control Unit B SEND pushbutton for five seconds.	Station A P&I lamp comes on and the BREAK indicator lamp and audible alarm go off. After phasing and indicator cycle has been completed P&I lamp goes off.	Remote Control Unit B and KW-7 Station B SEND and P&I indicator lamps come on. After phasing and indicator cycle has been completed, P&I lamp goes out.
10. None.	Transmit a test message from the transmitter-distributor or keyboard.	Page Printer prints the message.	Page Printer prints the message.
11. Transmit a test message from the transmitter-distributor or keyboard.	None.	Page Printer prints the message.	Page Printer prints the message.

3203. Operation.—As previously stated, the KW-7 provides for the transmision or reception of intelligence in the form of either plain text or cipher text. The following subparagraphs describe the procedures for placing the KW-7 equipment in either operational condition. Although these procedures are related directly to a two-station half-duplex operation, they may also be applied to a full-duplex or multistation operation. If a malfunction occurs during any of the procedures, reference should be made to Chapter 3 of KAM-144B/TSEC for trouble-shooting information.

a. *Establishing Plain Text Communications.*—The following procedures pertain to the operation of the KW-7 for the transmission or reception of plain text communications.

(1) Perform the required wiring and cabling connections to affect the desired system operation (refer to figs. 3-13 through 3-18).

(2) Set the switches as shown in table 3-9.

(3) The transmitting station operator should depress the SEND pushbutton and hold it depressed for approximately five seconds.

(4) The P&I indicator lamp located at both stations should become illuminated as soon as the transmitting station operator depresses the SEND pushbutton.

(5) After release of the SEND pushbutton, the P&I lamp, located at both stations, should become deactivated as soon as the phasing and indicator cycle has been properly completed in both units.

(6) The transmitting station operator should now transmit a test message to determine the reception capability of the receiving station.

(7) The receiving station operator should observe the test message and determine that it is not garbled. If the test message is garbled for any period of time, interrupt transmission by depressing the BREAK push-button/indicator until the BREAK lamp is illuminated. Paragraph *c* (which follows) describes the steps required to employ the break feature of the equipment.

Note: In the event that the KW-7 is being operated with a radio communications link, the BREAK FUNCTION switch should be placed in the OFF position. If the test message is garbled, the receiving station operator will have to advise the transmitting station operator by an alternate mode of communication.

b. Establishing Cipher Text Communications.—The following procedures pertain to the operation of the KW-7 for the transmission or reception of cipher text communications.

(1) Perform the required wiring and cabling connections to affect the desired system operation (refer to figs. 3-13 through 3-18).

(2) Unlock the KW-7's front cover and set the permuter patch cords in an operational setup based on a key list. Relock the cover.

WARNING: THE PATCH CORDS MUST NEVER BE SET AS SHOWN IN TABLE 3-8 WHEN THE KW-7 IS CONNECTED TO THE LINE.

(3) Set the switches as shown in table 3-9 with the exception that the PCR switch is to be placed in the CIPHER position.

(4) Rotate the ALARM TEST switch through all of its positions, pausing for approximately five seconds at each position, and observe the occurrence of the associated indications defined in table 3-14.

(5) Perform steps 3 through 7 of paragraph *a* above.

TABLE 3-14

ALARM TEST SWITCH, TEST POSITION INDICATIONS

Position	ALARM Lamp	MI Lamp	Audible Alarm	Send and P&I Lamps
OFF	Off	Off	Off	Off
1	On	On	Audible	Off
2	On	On	Audible	Off
3	On	On	Audible	Off
4	On	On	Audible	Off
5	On	On	Audible	Off
6	On	Off	Audible	On
7	On	Off	Audible	Off
8	On	Off	Audible	Off
9	On	Off	Audible	Off
10	Off	Off	Audible	Off
11	Off	Off	Off	Off

c. Break Procedure, Two-Station Half-Duplex Operation.—The break procedure is employed when a receiving station observes extended garble being printed out on the page printer. The following paragraphs describe the steps to be performed for operation with 2-wire or 4-wire lines and with radio equipment.

(1) *Wire line operation.*—During 2-wire or 4-wire operation the station will have the BREAK FUNCTION switch placed in the ON position. If, during the course of a message reception, extended garble appears on the page printer, the following steps should be performed:

(a) The station observing the garble should immediately depress the BREAK pushbutton/indicator until the indicator becomes illuminated.

(b) The transmitting station should halt transmission as soon as its BREAK pushbutton/indicator becomes illuminated and then attempt a new start. In the event that the new start again results in a break operation, the transmitting station should halt communications and refer to Chapter 3 KAM-144B/TSEC.

(2) *Radio equipment operation.*—During operation with radio equipment, the station must have the BREAK FUNCTION switch in the OFF position. This prevents the generation of break indications due to radio fadeout. If, during the course of a message reception, extended garble appears on the page printer the following steps should be performed:

(a) The station which observes the garbled message should notify the transmitting station by an alternate mode of communication.

(b) Upon notification of a break condition, the transmitting station should halt transmission immediately and attempt a new start. In the event that the garble continues, the transmitting station should halt operation and refer to Chapter 3 of KAM-144B/TSEC.

3204. Operational Errors.—When the KW-7 fails to perform properly, the trouble may be either an operational or functional error. Operational errors are those caused by human error in operating the equipment. In contrast, functional errors are those caused by malfunctions within the equipment itself. Operational errors are most likely to occur when a piece of equipment is first installed. If the trouble is experienced within a newly installed KW-7, check out the operating procedure to eliminate it as a possible cause of the difficulty before going on to troubleshooting techniques, outlined in KAM-144B/TSEC. Table 3-15 describes those operational errors which might affect proper operation of the equipment.

TABLE 3-15

OPERATIONAL ERRORS

Symptom	Possible Operational Error	Remedy
KW-7 inoperative; all indicator lamps out.	Primary power connections to unit improperly made.	Check all power connections.
BREAK indicator lamp continually on (BREAK FUNCTION switch ON).	Line circuit connections improperly made.	Check all line connections.
Cannot transmit.	Loop circuit connections improperly made.	Check all loop connections.
Garbled reception.	Improper switch settings. Broken or improperly seated permuter patch cord.	Check all switch settings for proper setting. Check all patch cords.
Page printer runs open.	Jumper plugs improperly seated or missing.	Check jumper plugs.
Constant alarm (Cipher operation).	Permuter patch cords improperly wired.	Check for proper patch cord wiring.

3300—VIOLATIONS OF CRYPTOSECURITY

3301. General.

a. The equipment malfunctions and failures and other insecurities listed below are of concern to both operators and maintenance personnel. Where the operator has not been trained in the electronic theory of the equipment, maintenance personnel shall be responsible for preparing the necessary reports of equipment malfunction or failure.

b. Reports concerning equipment malfunctions or failures cannot be evaluated unless they contain detailed information. Paragraph 3304 provides guidance regarding the contents of such reports.

c. The information in a report concerning equipment malfunctions or failures shall be classified SECRET—CRYPTO. The complete report shall be classified in accordance with the instructions contained in the effective edition of KAG–1.

3302. Reports of Physical Insecurities.—The reporting procedures for physical insecurities vary depending upon the circumstances. The insecurities listed in *a* below must be reported immediately by message, assigned at least a PRIORITY precedence in accordance with the procedures for message reports contained in Section 5200 of the effective edition of KAG–1. The insecurities listed in *b* below must be reported in accordance with the procedures for letter reports contained in that section of KAG–1 referenced above.

a. Message Reports.

(1) Physical loss of keying material (superseded, current or future).

(2) Any instance of unauthorized viewing of keying material or the KW–7 plugboard when keyed according to an operational key list.

Note: It is possible to obtain the plugging arrangements through examination of the key operating and combining circuits of an operating KW–7. One way to accomplish this is through use of a probe and ohmmeter. If there is reason to believe this has occurred, it should be reported as an instance of unauthorized viewing of keying material.

b. Letter Reports.

(1) Physical loss of crypto-equipments, maintenance manuals and operating instructions.

(2) Any instance of the KW–7 being left unattended under circumstances that might allow unauthorized persons access to the classified portions of the equipment. (Provided that *a* (2) above could not have occurred.)

(3) Any instance of an unauthorized person having an opportunity to view, photograph or copy the classified elements, maintenance manuals or operating instructions.

3303. Reports of Equipment Malfunctions and Failures and Other Reportable Insecurities.

a. Equipment malfunctions and failures will be reported in accordance with the procedures for message reports contained in Section 5200 of the effective edition of KAG–1.

b. The following equipment malfunctions and failures will be reported in accordance with paragraph *a* above if they occur during periods of alarm failure.

(1) Intermittent or constant failure of any stage of the Fibonacci chain.

(2) A constant output (00000 or 11111) of the special points circuits.

(3) A constant output (00000 or 11111) of the accumulator.

(4) A constant output (00000 or 11111) of the feedback re-entry adders.

(5) A constant output (00000 or 11111) of the final Modulo 2 adder circuits.

c. Any occurrence of inadvertent plain text transmission of special intelligence information resulting from equipment malfunction or failure, will be reported in accordance with paragraph *a* above.

d. The reportable insecurities listed below will be reported in accordance with the procedures for letter reports contained in Section 5200 of the effective edition of KAG–1.

(1) Malfunction or failure of noise source or amplifier filters.

(2) Oscillation in noise source or amplifier filter circuits.

(3) Any transmission with improper plugging (i.e., improper plugging or plugs not inserted at all).

(4) Modification or removal of components of the key generating, key combining, randomizer or alarm circuits without prior approval of the Director, National Security Agency.

(5) Any use of the same plugboard setting for a period exceeding 26 hours.

(6) Manipulation of the equipment by unqualified personnel not under the supervision of a qualified operator.

(7) Disablement of the plaintext audible alarm except for maintenance purposes.

(8) Transmission in the clear of information concerning equipment failure or malfunction or operator error which might have produced faulty key. (Revealed condition messages are excluded from this restriction.)

(9) A transmission in which any serious operating error occurs which appears to weaken the security of the system. (Revealed condition messages are excluded from this restriction.)

(10) Operation of the equipment when the following precautions are not observed:

(a) All covers must be on the equipment and secured.

(b) All shield grounds must have continuity through their respective connectors.

(c) All filters must be in proper operating condition.

3304. Report Information.—When an equipment malfunction, failure or other reportable insecurity occurs, the following information should be included in the report of the occurrence:

a. Time transmission occurred and length of faulty transmission.

b. Description of how the failure was detected.

c. Indication of the degree of failure.

(1) Constant, intermittent, or occasional periods of complete failure.

(2) Intermittent rapid cutting in and out.

(3) Other unreliable operation.

d. Description of output of the faulty circuit.

e. Effect of the failure on other circuits.

f. Identification or description of any components that were at fault.

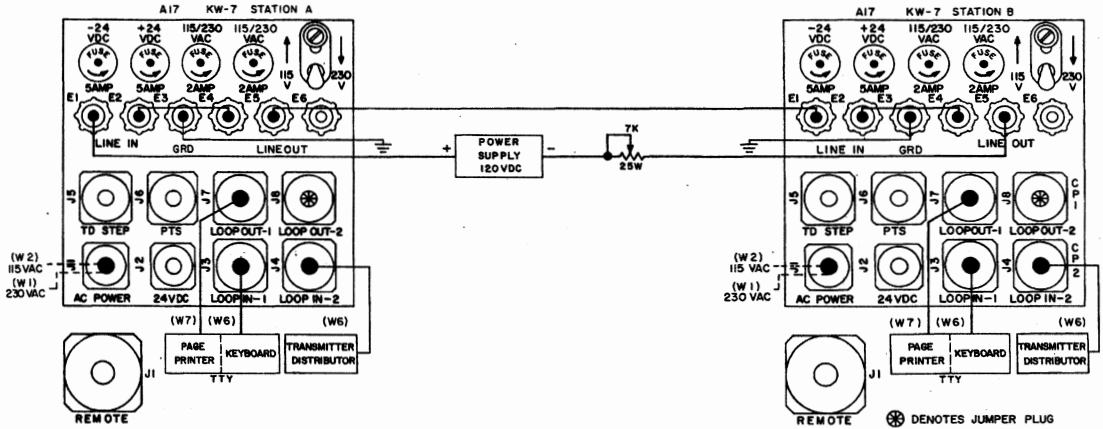


Figure 3-13.—Connections for Two-Wire Neutral Operation.

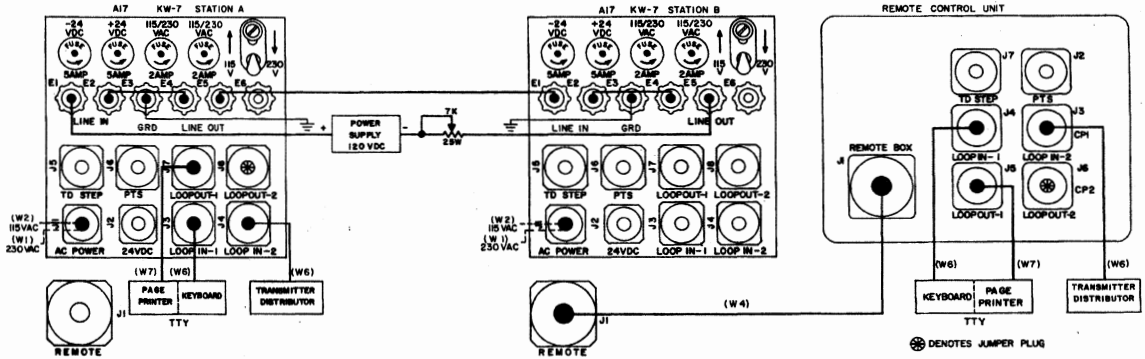


Figure 3-14.—Connections for Two-Wire Neutral Operation, Remote Control.

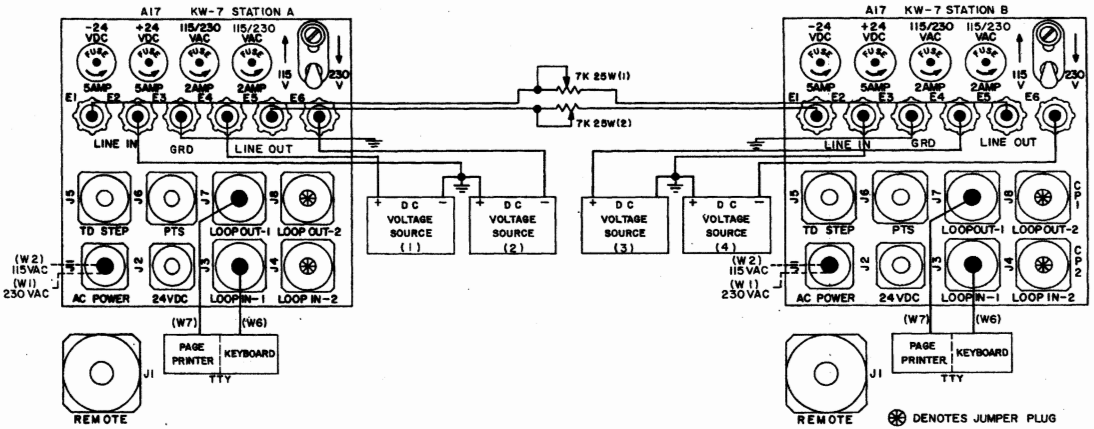


Figure 3-15.—Connections for Two-Wire Polar Operation.

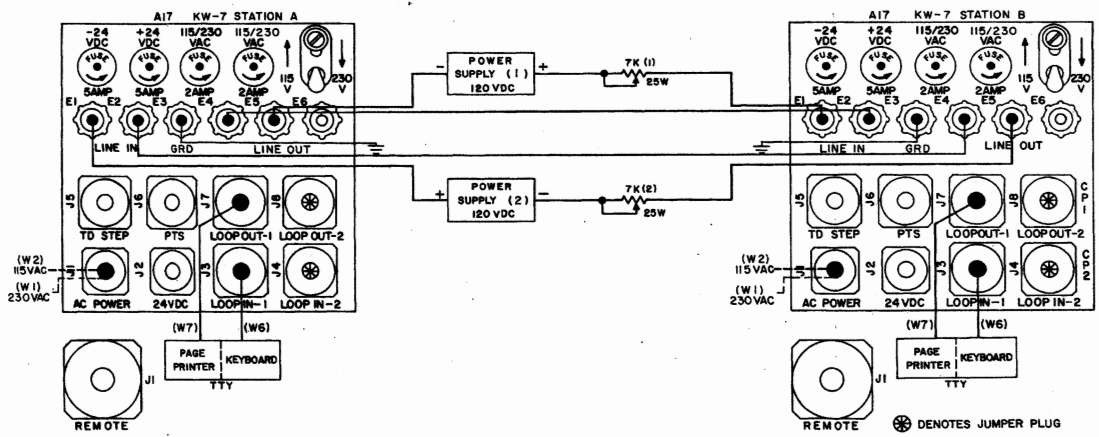


Figure 3-16.—Connections for Four-Wire Neutral Operation.

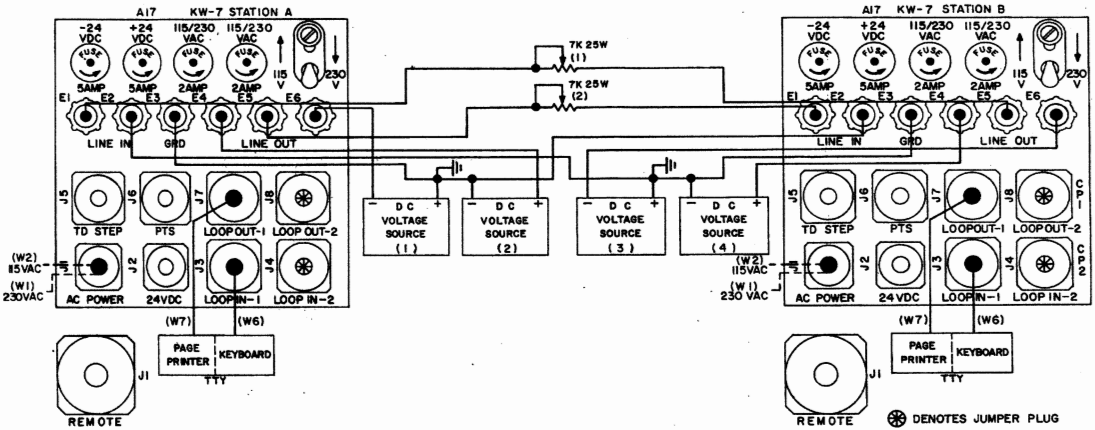


Figure 3-17.—Connections for Four-Wire Polar Operation.

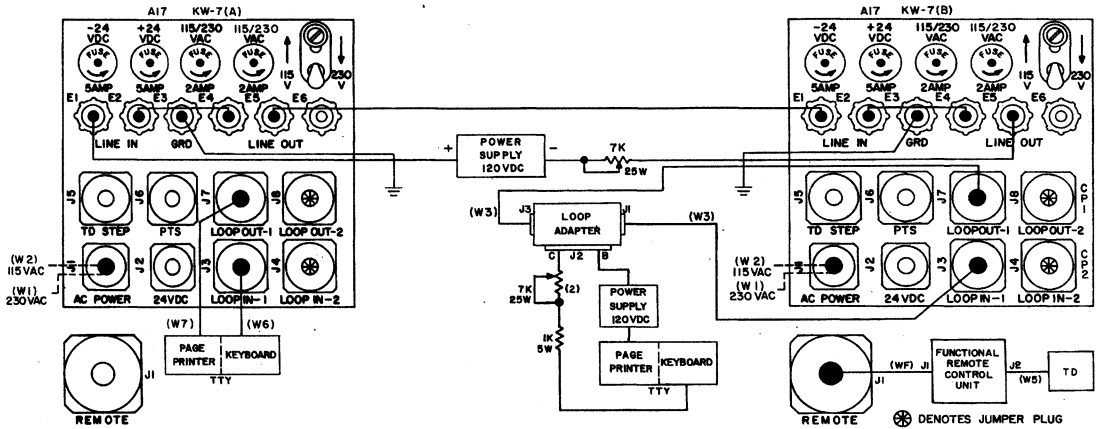


Figure 3-18.—Connections for Loop Adapter/Functional Remote Control Operation.

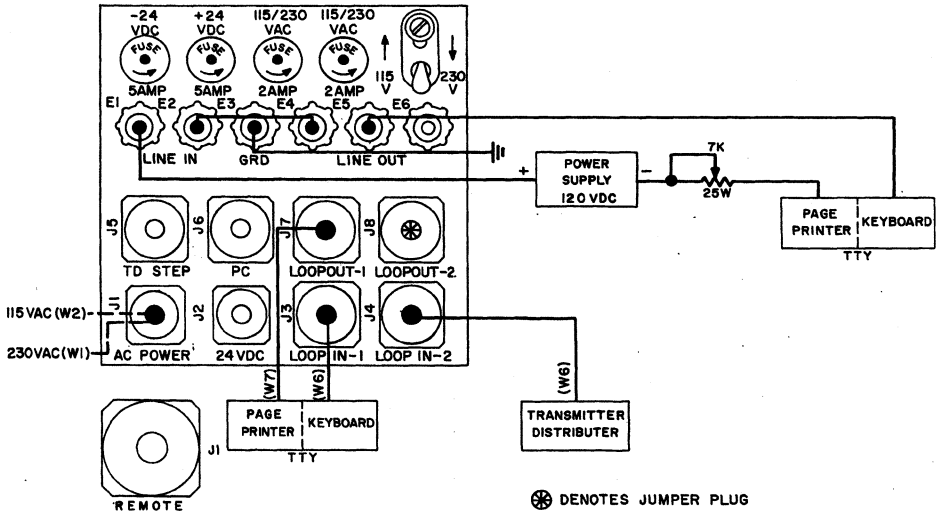


Figure 3-19.—Connections for Plain Asynchronous Two-Wire Neutral Operation.

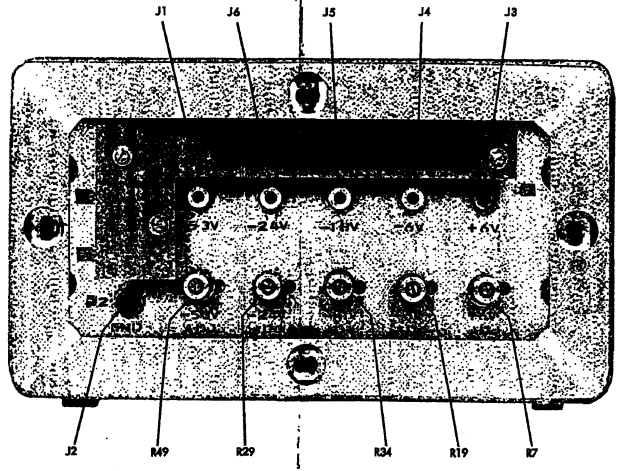


Figure 2-20.—Power Supply, Top View (Cover Removed).

CHAPTER 4

THEORY OF OPERATION

4000—OVERALL DESCRIPTION

4001. General.—Use of the KW-7 equipment by a communications system permits the open transmission of classified information without fear of revealing the contents to other than the intended parties. Each KW-7 functions as a transceiver in that it can either transmit or receive data, but not simultaneously. Operating as a transmitter, the KW-7 accepts input signals from a teletypewriter keyboard or transmitter-distributor and transforms this plain text information into a form called cipher. When this cipher is transmitted it is intelligible only to other KW-7's in the system. As a receiver, the KW-7 accepts cipher signals and, by a process known as decryption, recovers the data content of the message that was originally concealed by the transmitting KW-7. The KW-7 is also capable of transmitting and receiving plaintext information. Certain special terms are used in the ensuing discussion of this equipment. These terms are explained when they first appear in the text.

a. Form of Information Transmitted.—To understand the form of information transmitted between a pair of KW-7's consider first the transmission of information by means of a simple neutral teletypewriter system. Information in such a system is transmitted by opening and closing the circuit at the transmitting end. At the receiving end, the open or closed condition of the circuit is indicated by the presence or absence of current through a load in the circuit. Basically, then, there are only two states in which the circuit can exist; current is either flowing or not flowing through the circuit at a given instant or, similarly, a voltage is either developed or not developed across the load. Because the simple method of transmitting information just described involves only two states, the system can be described as a binary system. The two states of a binary system are usually distinguished by designating one of the states as the ONE state and the other as the ZERO state. Information is conveyed in such a system by the sequence in which these ONE's and ZERO's occur. Returning again to the simple teletypewriter system, the closed circuit (current flow) can be designated arbitrarily as the ONE state and the open circuit (no current flow) can be designated as the ZERO state.

b. Neutral Teletypewriter Transmission Information.—Actual neutral teletypewriter data signals consist of an electrical five unit code of current and no-current intervals. Inpulses which energize the teletypewriter selector magnets are known as marking impulses and those which do not are known as spacing impulses (see fig. 2-3 in chapter 2). This five unit code is composed of five selecting intervals which may be either marking (current flow) or spacing (no current flow) according to the code sequence of the character to be transmitted. Each group of five data selecting intervals is preceded by a start interval (no current flow) and is followed by a stop inpulse (current flow). To further relate this five unit code to the binary system it is possible to call each of the five selecting intervals a baud (the smallest bit of information contained in any teletypewriter character). Thus the letter A is represented by a start interval followed by five bauds (two marks and three spaces) and ending with a stop impulse. Binarily this is represented by 0110001. Therefore, by the introduction of unit time intervals, the teletypewriter code can be resolved into serial binary form in which information is conveyed solely by a sequence of binary bits.

4002. Encryption and Decryption.—The plaintext information on which the KW-7 operates to produce cipher is in serial binary form when it is submitted for encryption; i.e., the information is represented as a sequence of ONE bits and ZERO bits, each occupying a unit time interval. The encrypting process (the process which converts plaintext to cipher) performed by the KW-7 modifies the sequence of ONE's and ZERO's in a way that conceals the information represented by this sequence. Conversely, in performing the complementary process of decryption (converting the cipher back into plaintext), the receiving KW-7 recovers the original sequence of ONE's and ZERO's of the text from the cipher. The actual encrypting process involves the addition of a random sequence of ONE's and ZERO's (called key) to the text in order to produce cipher. The decrypting process involves the addition of the identical random sequence of ONE's and ZERO's to the cipher to recover the plaintext. This method of encryption and decryption generally is known as an additive key method.

a. Additive Key Method.—The transmitting KW-7 converts plaintext messages into cipher text messages by an additive key method. The plaintext is added to the key, one baud at a time by an addition process called MOD2 addition. MOD2 addition is merely binary addition neglecting the ONE carries. Table 4-1 shows the comparison between binary addition and MOD2 addition.

TABLE 4-1

COMPARISON BETWEEN MOD 2 ADDITION AND BINARY ADDITION

	MOD2 Sum	Binary Sum
0 plus 0 =	0	0
0 plus 1 =	1	1
1 plus 1 =	0	0 with a 1 carry

(1) For example the letter A in plaintext is represented in teletypewriter code by the binary number 11000. This binary number is preceded by a ZERO start baud, and followed by a ONE stop baud. Therefore, the complete plaintext representation for the letter A is 0110001. When plaintext is MOD2 added to key, the start and stop bauds remain in plaintext to permit receiver synchronism, but the middle five information bauds are encrypted (added to key bauds). The key is added to the letter A (text) one baud at a time to produce cipher. The following example illustrates MOD2 addition of key to the letter A.

	Key	10101
(Plus)	Text (A)	11000
(Equals)	Cipher (A)	01101

The resulting MOD2 sum, called cipher, bears little resemblance to the original representation of the letter A. Thus, the cipher conceals the plaintext for secure transmission by the KW-7.

(2) The receiving KW-7 receives the letter A in cipher form, and converts the cipher to plaintext again, by MOD2 adding an identical segment of key to the cipher, as shown in the following example.

	Cipher (A)	01101
(Plus)	Key	10101
(Equals)	Text (A)	11000

Thus the decryption of the letter A in cipher form recovers the original plaintext form of 11000. The key actually will be a constantly changing sequence of ONE's and ZERO's, but will have a random sequence in the transmitting KW-7, which is synchronized to an identical random sequence in the receiving KW-7. Each character of a teletypewriter message can be placed in cipher form for secure transmission by the additive key method just described.

b. Key Generator Setup.—The initial setup of the key generators used in the KW-7 cryptographic system determine the particular key cycle produced. If this initial setup were built into the key generator with a fixed format, the same key cycle would always be produced, thus weaking the security of the system by allowing interceptors to accumulate information on the key cycle, and, eventually allowing them to duplicate the key cycle. This risk is avoided by provision of a variable initial key generator setup. The format of the key initial setup can be manually changed periodically in both the transmitter and receiver, thus, effecting an overall change in the key cycle. Because of the need for synchronism between the key generators in both the transmitter and receiver, both key generators always have the same starting point in the key cycle with the initiation of a send operation. However, the starting point is continually changing to provide increased transmission security. A sequence of automatic modification operations are performed by the key generator logic, thereby increasing the cycle length of the key stream pattern. The key stream is composed of a random sequence of binary ONE's and ZERO's. The manual capability of changing the key cycle on a planned schedule further increases the security of crypto transmission, over and above that provided by the automatically generated portion of the key stream.

4003. Operational Phases.—The following discussion presents a simplified description of the operation of the KW-7 both as a transmitter and receiver (figs. 4-1 through 4-6). This discussion defines what occurs during the cipher, plain synchronous, and plain asynchronous operations.

a. Cipher Operation.

(1) *Send phasing (fig. 4-1).*—When the transmitting KW-7 operator depresses the SEND pushbutton/indicator switch, the KW-7 automatically generates MOD-8 letters characters (phasing characters) and transmits them to the receiving KW-7.

(2) *Send indicator (fig. 4-1).*—After the transmitting KW-7 operator releases the SEND pushbutton/indicator switch, the KW-7 continues to generate and transmit MOD-8 letters characters until a blank character is generated by the randomizer. The KW-7 recognizes the first blank character generated by the randomizer as the first random message indicator character and transmits it and the subsequent sequence of letters and blank characters in MOD-7. The KW-7 continues to transmit this series of letters and blank characters until twelve blank characters, including the initial blank character, and then twelve letters characters have been transmitted.

(3) *Send normal (fig. 4-1).*—During the send normal phase, the transmitting KW-7 adds the output from its key generator (key) to the plain text output (synchronous 7.0 baud data) from the extensor and control and produces cipher (MOD-2 sum of synchronous 7.0 baud data plus key) which is fed to the line output circuit for transmission to the receiving KW-7.

(4) *Receive phasing (fig. 4-2).*—At all times, except when actively transmitting, the KW-7 is searching for and will recognize MOD-8 letters characters. After four consecutive mark-space transitions have occurred, at the proper eight count time, the receiving KW-7 recognizes that a genuine phasing start has taken place, locks in its counters and searches for the first blank character of the indicator phase.

(5) *Receive indicator (fig. 4-2).*—The receiving KW-7 recognizes the first MOD-7 blank character received as the beginning of the receive indicator phase. The receiving KW-7 votes on this blank character by counting four out of the six spacing bits (five information bits and one start bit as spaces). The receiving KW-7 then counts 12 blank characters

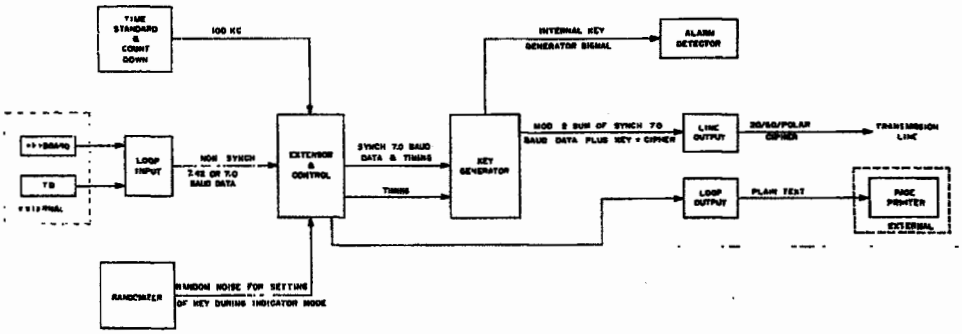


Figure 4–1.—Send Cipher Operation, Block Diagram.

(including the initial blank character) and then 12 letters characters, at which time the receiving KW–7 recognizes that the indicator phase has been completed and will automatically go into the receive normal phase.

(6) *Receive normal (fig. 4–2).*—During the receive normal phase, the receiving KW–7 adds the output of its key generator (key) to the output from the extensor and control (7.0 baud cipher) and produces plaintext (7.0 baud cipher plus key) which is fed to the receiving KW–7's loop output for printout on its external page printer.

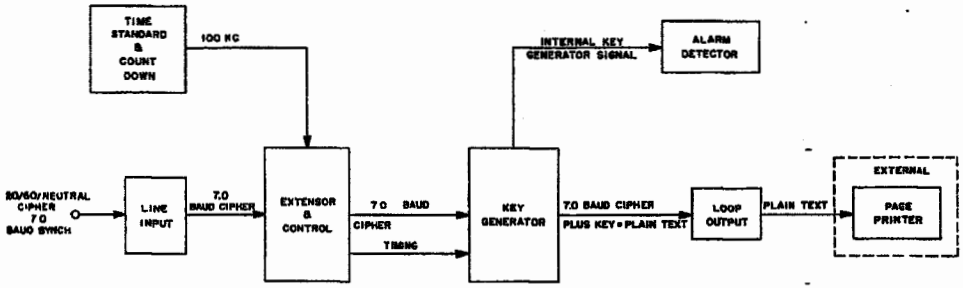


Figure 4–2.—Receive Cipher Operation, Block Diagram.

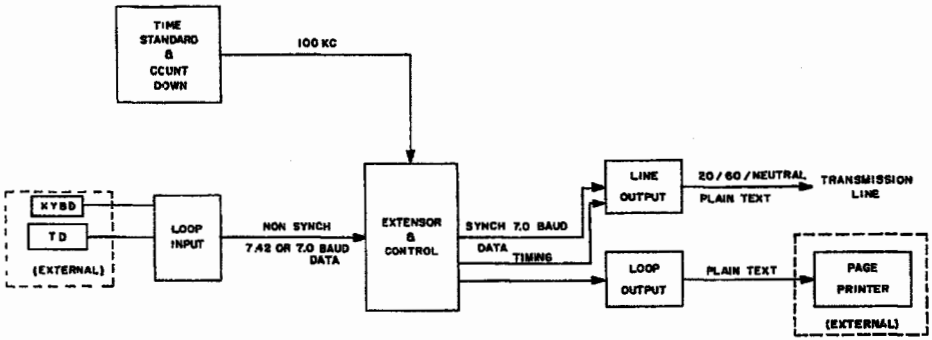


Figure 4–3.—Send Plain Synchronous Operation, Block Diagram.

b. Plain Synchronous Operation.

(1) *Send phasing (fig. 4-3).*—When the transmitting KW-7 operator depresses the SEND pushbutton/indicator switch, the KW-7 automatically generates and transmits MOD-8 letters characters. The KW-7 continues to transmit these MOD-8 letters characters, after the SEND pushbutton/indicator switch has been released, until such time that a blank character is generated by the randomizer. The KW-7 recognizes the first blank character as the end of phasing and by-passes the indicator period to go directly into normal.

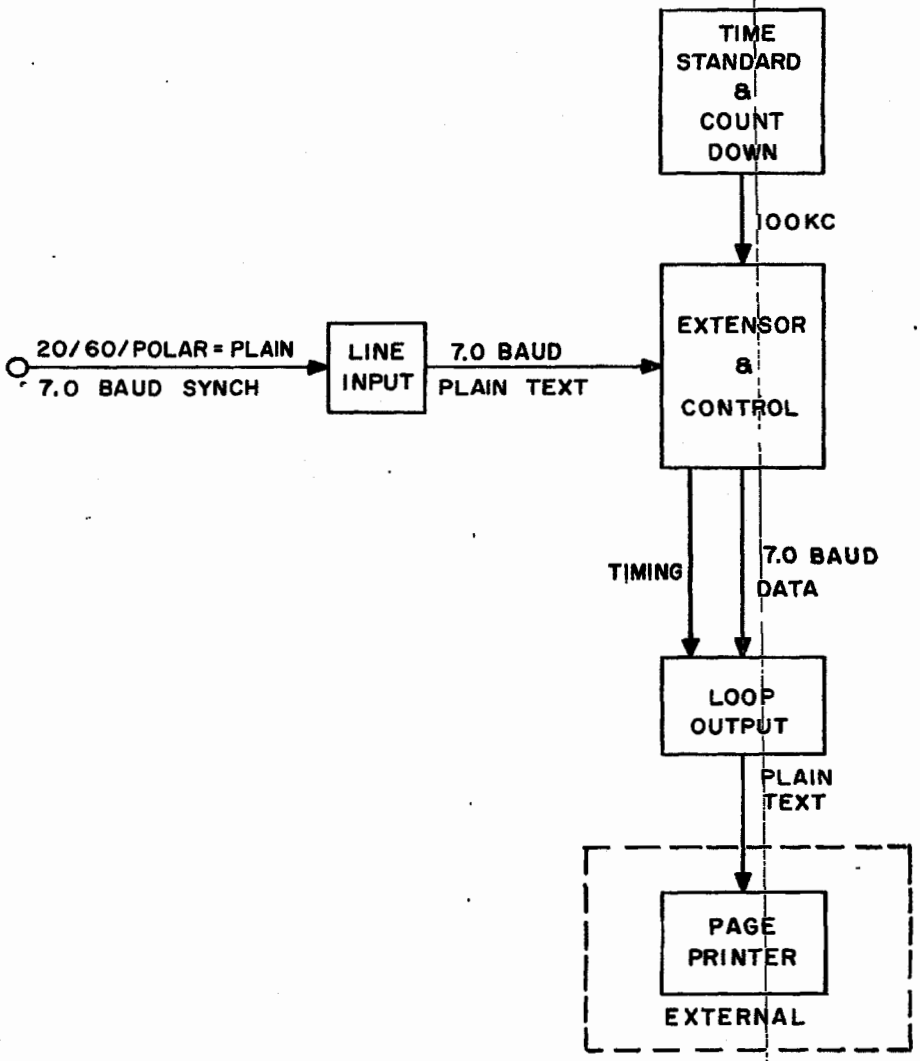


Figure 4-4.—Receive Plain Synchronous Operation, Block Diagram.

(2) *Send normal (fig. 4-3).*—During the normal phase, the KW-7 accepts plain text inputs from a teletypewriter keyboard or transmitter-distributor, transmits the start-stop 7.0 7.42 baud data to the loop output circuit for page printer printout, and also converts this input into synchronous 7.0 baud data plus timing. This information is then fed to the line output circuit for transmission to another KW-7.

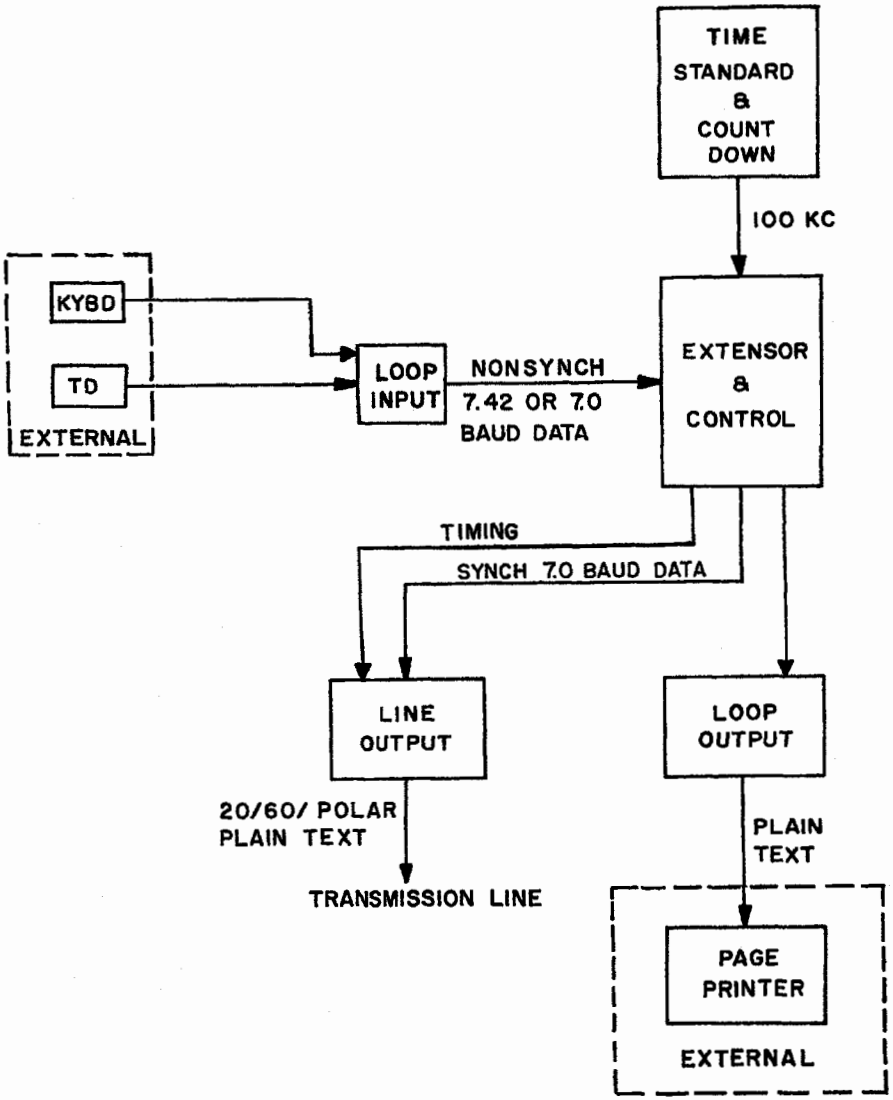


Figure 4-5.—Send Plain Asynchronous Operation, Block Diagram.

(3) *Receive phasing (fig. 4–4).*—During receive phasing the KW–7 searches for and recognizes MOD–8 letters characters until such time that a 7.0 unit blank character is received. At this time, the KW–7 recognizes that the phasing phase is over and by-passes the indicator phase to go directly into the normal phase.

(4) *Receive normal (fig. 4–4).*—The KW–7 accepts the plain text information and directs it through the extensor and then through the loop output circuit, to the receiving KW–7's page printer.

c. *Plain Asynchronous Operation.*

(1) *Send normal (fig. 4–5).*—Send normal operation for plain asynchronous operation is the same as that discussed for plain synchronous operation.

(2) *Receive normal (fig. 4–6).*—During receive normal phase, the KW–7 accepts asynchronous teletypewriter inputs at its line input circuit, and feeds it to its loop output circuit for printout on the external page printer without going through the extensor.

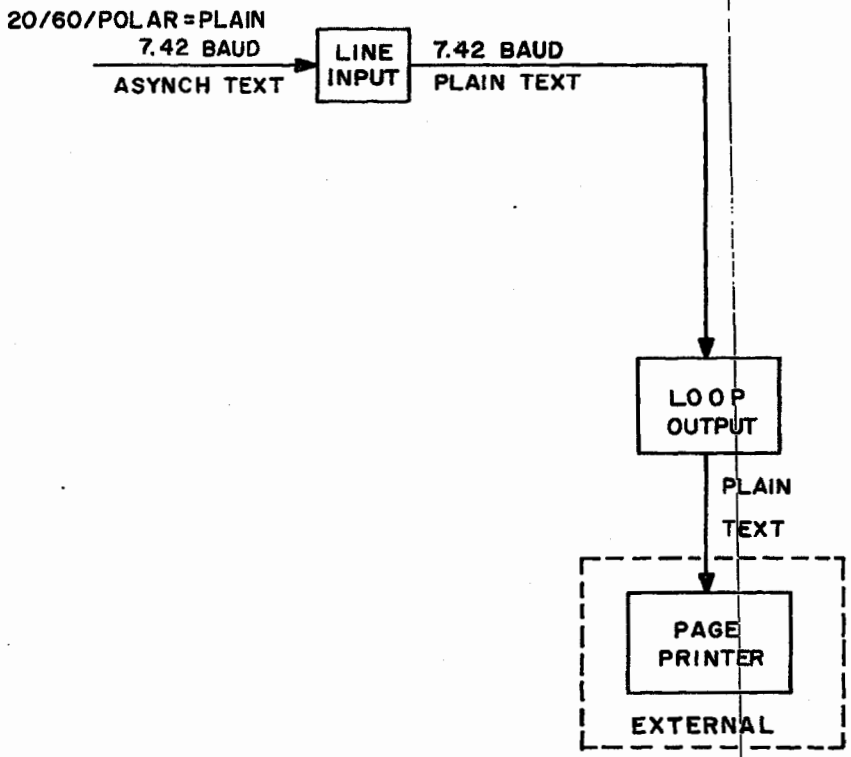


Figure 4–6.—Receive Plain Asynchronous Operation, Block Diagram.

4100—DETAILED THEORY, TRANSISTORS

4101. Semiconductor Material, Properties, and Atomic Structure.

a. Introduction.—Much of the advancement in the field of digital computers is directly attributable to the parallel development of semiconductor devices. The two most widely used devices are the transistor and the diode. The employment of these two devices has made it possible to develop extremely fast computers which consume less power and are more reliable than the earlier vacuum tubes. With the increased utilization of semiconductors, the understanding of their operation is essential for electronic technicians.

b. Properties.—A semiconductor possesses electrical properties which classify it as neither a good insulator nor a good conductor. The resistivity of the material is dependent upon the availability of current carriers which, in turn, is controlled by the arrangement of the atoms within the material. The two elements which are most widely employed in the manufacture of transistors and diodes are silicon and germanium. Either germanium or silicon in their pure forms are insulators, but when a small amount of an impurity (0.05 ppm) is added, the material becomes a semiconductor.

c. Atomic Structure.—The atom is the smallest particle of an element which still retains the properties of the element. The atom is composed of protons (positively charged particles) and neutrons (neutral particles) which form the central portion of nucleus, and electrons (negatively charged particles) which rotate in orbits around the nucleus. The atom may be pictured as a sun with planets revolving about it. The number of rotating electrons (which equals the number of protons in the nucleus) is known as the atomic number of the element. Electrons are separated in groups called shells, at certain distances from the nucleus. To present a picture of sizes involved in the atom, if the nucleus were considered to be the size of a baseball, the nearest electron shell would be one and one-half miles away! The lightest element, hydrogen, has only one shell containing one electron, whereas germanium has four shells with 2, 8, 18 and 4 electrons respectively. The electrons in the outer-most shell, called valence electrons, may never number more than eight. It is these outer electrons, and the processes involved with them, that bond atoms together. The atomic structure of germanium is shown in figure 4–7. The atoms of silicon and germanium in the natural solid

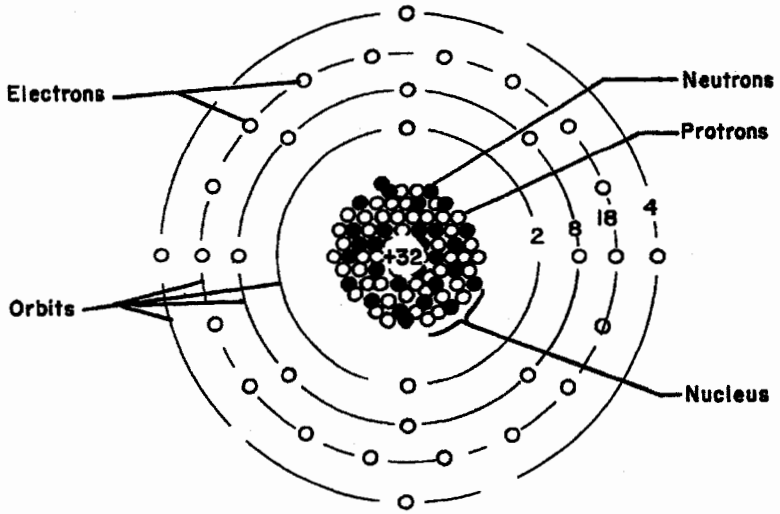


Figure 4–7.—The Atomic Structure of Germanium.

state are held together by a covalent bond. This covalent bond is formed by the interaction of the valence electrons of one atom with the valence electrons of other atoms. Since both silicon and germanium have only four valence electrons, and since the outer shell can accommodate eight, there are four empty spaces which electrons from another atom or atoms may occupy. Each of the four valence electrons interlinks with an electron orbit of an adjacent atom to form a solid covalent bond so that every atom appears to have a complete outer shell. This formation of many bonds into a regular pattern is known as a crystal lattice.

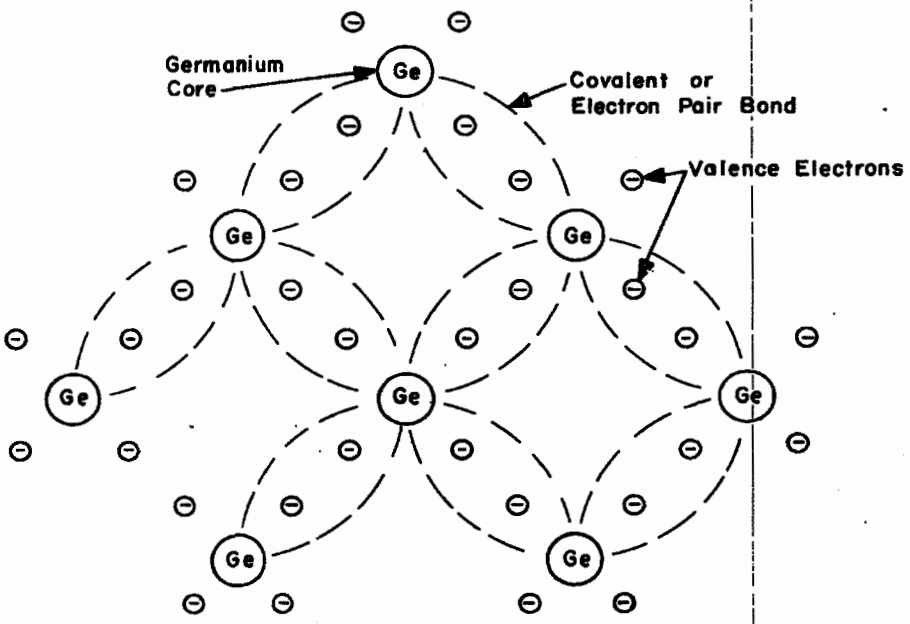


Figure 4-8.—Symbolic Structure of Pure Germanium.

d. Conduction.

(1) *Impurities.*—It is possible for atoms of substances other than germanium to combine with the lattice structure of germanium. Two types of impurities are added to germanium to produce the desired electrical properties: one type, known as donors, has five valence electrons; the second type, called acceptors, has only three valence electrons.

(2) *Donor theory.*—Since the donor material (usually arsenic) has five valence electrons, when it combines with germanium (four valence electrons) there is one excess electron existing in the lattice. The newly-formed material, characterized by the spare electron, in known as N-type germanium (N standing for negative since there is the excess of electrons which have a negative charge) and is classified as a donor (fig. 4-9). The free electron is very loosely held in the lattice structure and therefore is relatively free to be moved by an electromagnetic field (in fact, room temperature supplies more than enough energy to release this electron from its bond to the arsenic atom). The conductivity of the crystal will depend upon the number of free electrons which can be caused to move through the lattice structure by a battery connected across the crystal. When this excess electron leaves the donor atom, the result is the production of a positive ion.

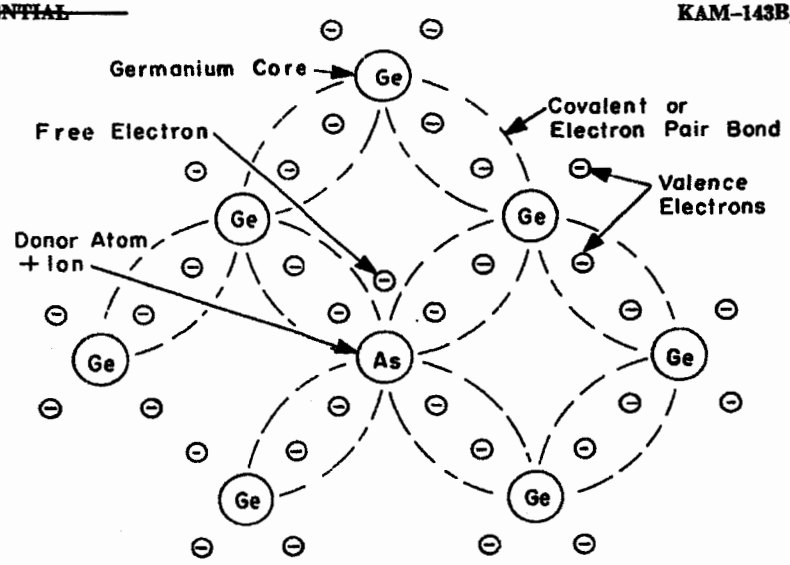


Figure 4–9.—Symbolic Structure of N-Type Germanium.

(3) *Acceptor theory.*—The element indium is often employed as the added impurity to produce acceptor material. Indium has only three valence electrons so that when it combines in the germanium lattice, there is the absence of one electron. The acceptor material is known as P-type germanium (P standing for positive since an electron is absent and the resulting charge is positive). The indium atom "borrows" an electron from a neighboring germanium atom thus breaking an existing covalent bond. The bond that had an electron taken from it now acquires a "hole" (fig. 4–10). The visualization of the absence

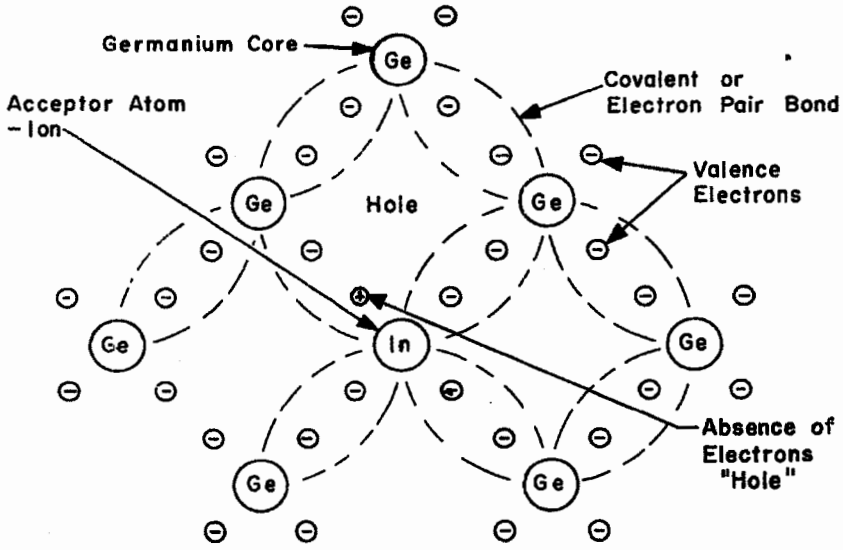


Figure 4–10.—Symbolic Structure of P-Type Germanium.

of an electron as a hole is an important concept in explaining the physics of a semiconductor. A brief paragraph describing holes and their significance will be presented. A hole is actually a movable energy state that acts as a positive electric charge. The relative motion of the hole is dependent upon the movement of electrons within the lattice structure; as voids are filled by loose electrons the hole appears to move about. Hole motion is restricted to movements from one atom to another while an electron may move about freely. The concept of holes is limited to semiconductor devices, and the holes may only move within a semiconductor, not in the electrical circuit. Holes, when attracted by the negative terminal of a voltage source, will diffuse through the semiconductor.

(4) *Conclusion.*—Thus it has been shown that two types of current carriers may be inserted into a semiconducting device: the negatively charged electron and the positively charged hole. Both carriers contribute to the conductivity of the material. Electrons are ordinarily identified with donor or N-type materials, holes with acceptor or P-type.

4102. The Semiconductor Junction.

a. Introduction.—When a section of N germanium is joined with a section of P germanium, the result is a PN junction. This device is known as a diode and functions primarily as a voltage rectifier. When this junction is made, a small potential difference is established. It would be expected that the excess electrons would migrate across the junction from the N material to fill the holes which exist in the P material. In actuality, a repulsive force is established which accounts for the potential difference. This repulsion is due to the fact that the negatively charged *atoms* of the P material repel the *electrons* in the N material. This repulsive force is known as the potential hill or barrier and can only be overcome by an external voltage (fig. 4–11).

b. Forward and Reverse Bias.

(1) *Forward bias.*—Forward bias in a semiconductor device may be accomplished by simply connecting the negative pole of a battery to the N-type material and the positive pole to the P-type. This arrangement attracts the electrons in the N-type material and the

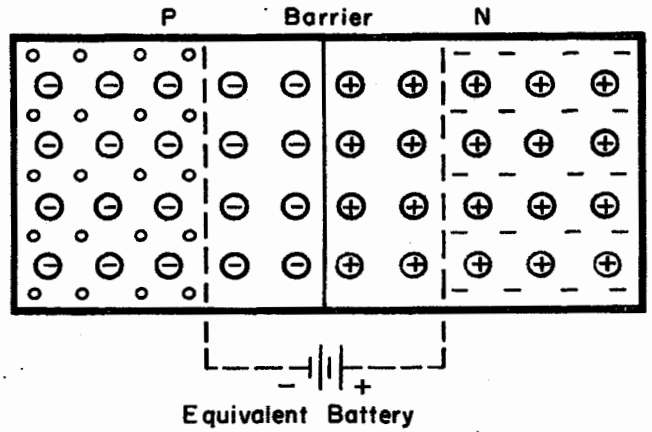


Figure 4–11.—PN Junction, No Bias.

holes in the P-type material towards the junction of the two materials. The potential barrier is then broken down and a large current is established at the junction due to the electron-hole exchange (fig. 4–12).

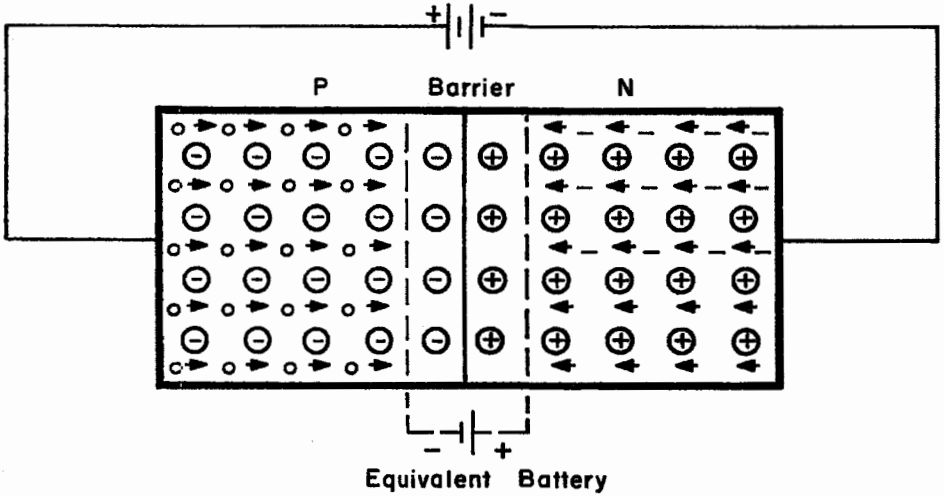


Figure 4–12.—PN Junction, Forward Bias.

(2) *Reverse bias.*—If the battery connections are reversed (i.e., negative pole to the P-type material and positive pole to the N-type) both the holes and electrons are forced away from the junction and the potential barrier is increased. Relatively little current will flow in this state (fig. 4–13).

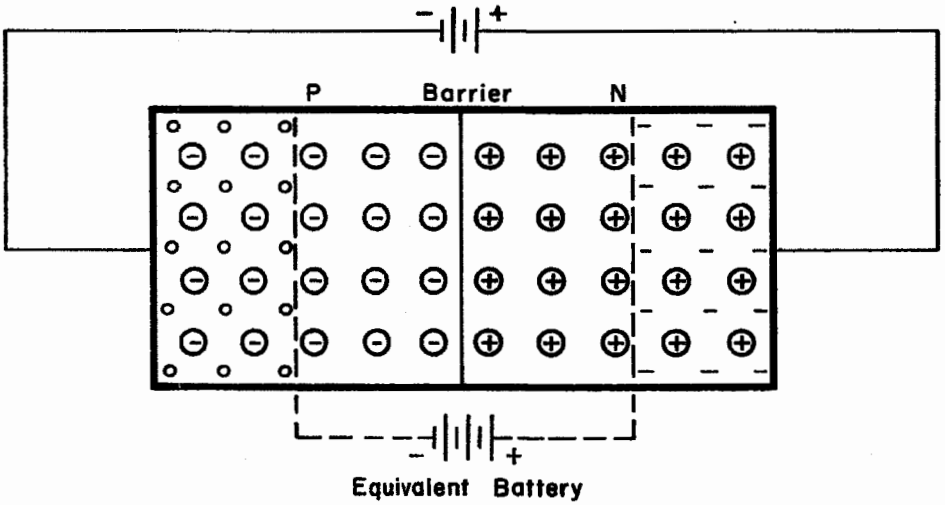


Figure 4–13.—PN Junction, Reverse Bias.

(3) *Conclusion.*—It can now be seen that a low resistance is associated with forward bias whereas reverse biasing increases the potential barrier and develops a high resistance. It is this unidirectional voltage characteristic that has made the diode so useful in rectification and in RF and IF detection.

c. *Diode Action.*

(1) *Reverse current flow and diode breakdown.*—When the diode is biased in the reverse direction, a small current flow is detectable. This current is caused by minority carriers which are a few electrons existing in the P material and a few holes present in the N material. Minority carrier current, called leakage or cut-off current, is entirely dependent upon the ambient temperature. However, if an excessive reverse voltage is applied, the diode will conduct as well in the reverse direction as it normally does in the forward direction. This is a result of the breaking of many covalent bonds throughout the lattice. Enough voltage will cause complete breakdown of all covalent bonds and *crystal breakdown* occurs (extremely large reverse current).

(2) *The diode operation.*—Figure 4–14 presents a typical curve of voltage versus current across the PN junction of a diode. Note that under a forward bias the current is carried by the majority carriers and flows in a positive direction. Under reverse bias, as previously stated, the current flows in a negative direction and is generated by minority carriers. The point of crystal breakdown is shown as a sharp "knee" in the curve. The voltage at which breakdown occurs is known as the Zener voltage. Note that for a wide span of currents the voltage remains practically constant (Zener effect). The heat generated by crystal breakdown will render the ordinary diode useless; however, special diodes have been designed which utilize these characteristics while resisting the damaging effects of heavy reverse conduction. These are known as Zener diodes, and are principally used as voltage regulators in power supplies.

4103. The Transistor.

a. *Introduction.*—The word transistor derives its meaning from the two words which describe its electrical action: TRANSfer resISTOR. The junction transistor is merely an extension of the diode combining two PN junctions in a single device. In operation, one of the junctions is biased in the forward direction, the other in the reverse direction. For amplification, a signal is inserted in the forward bias direction and extracted in the reverse bias direction. The transistor transfers the signal from the low resistance circuit to the high resistance circuit.

b. *Transistor Classification by Construction.*

(1) *The PNP transistor.*—The PNP transistor is formed by inserting a narrow strip of N-type germanium between two wider pieces of P-type germanium (fig. 4–15). The three regions, known as the emitter, base, and collector (P-N-P), are fitted with metal contacts in order that they may be connected to an external circuit. The junction between the emitter and the base is called the emitter junction, and the junction between the base and collector is known as the collector junction. Repulsion of electrons by negative ions occurs at each junction, as was described for the diode, hence, in the quiescent state, a depletion region is present at the emitter and collector junctions. The collector resistance is higher than the emitter resistance and usually is larger in area to accept most of the current carriers (holes). When the transistor is biased as shown in figure 4–16, holes diffuse through the base and combine with electrons that enter the collector from the negative terminal of the collector battery. The transistor is an extremely efficient device: 92 to 99 per cent of the emitter current reaches the collector.

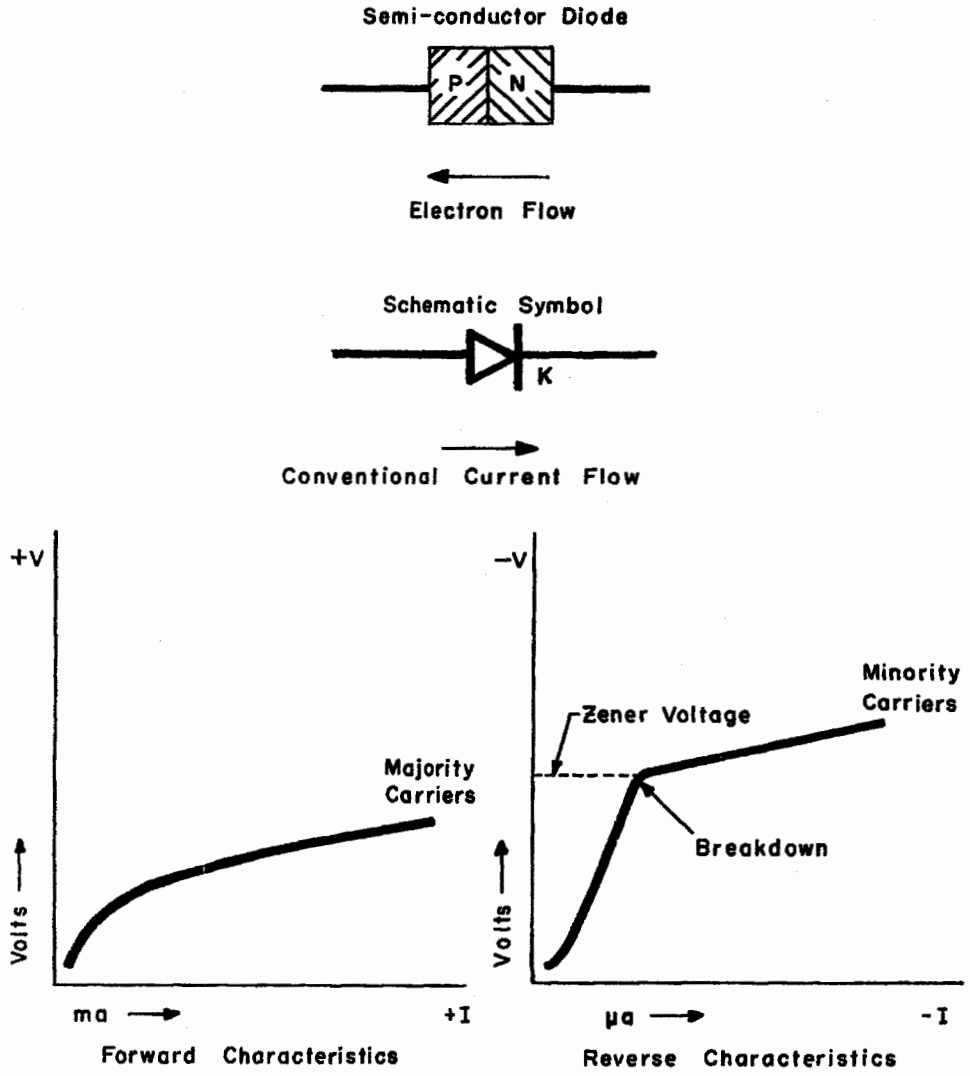


Figure 4-14.—Typical Diode Characteristics.

(2) *The NPN transistor.*—The NPN transistor is similar in operation and construction to the PNP except that a thin strip of P-type material is placed between two pieces of N-type material and the current carriers are electrons instead of holes. Figure 4-17 presents the biasing arrangement for the NPN transistor. Note that the battery polarities are reversed from those of the PNP, but this arrangement still provides a forward bias at the emitter and a reverse bias at the collector.

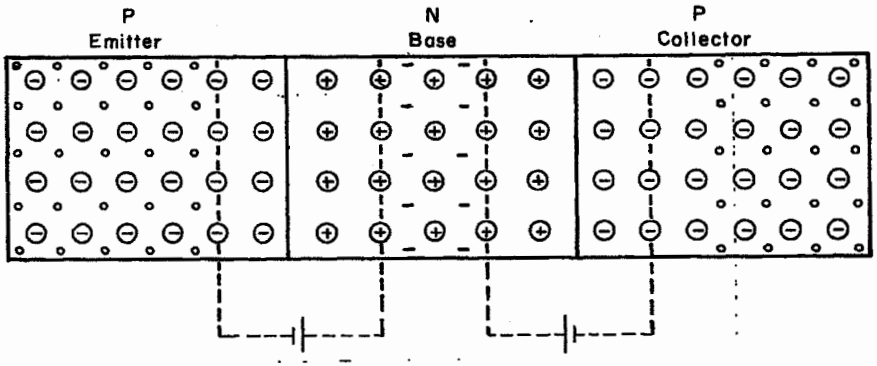


Figure 4-15.—PNP Transistor, No Bias.

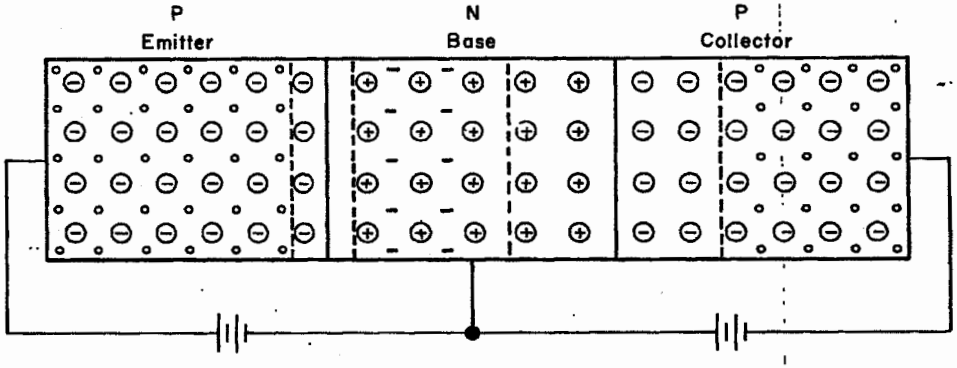


Figure 4-16.—PNP Transistor, Properly Biased.

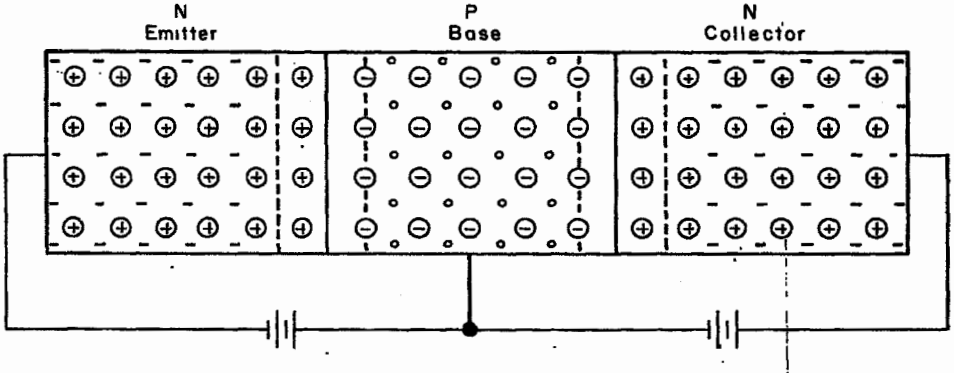


Figure 4-17.—NPN Transistor, Properly Biased.

(3) *Vacuum tube analogy.*—The three sections of the transistor, the emitter, the base, and the collector, can be related to corresponding components of the triode vacuum tube. The emitter is analogous to the cathode, the base is analogous to the grid and the collector is analogous to the plate. The vacuum tube is controlled by voltage, whereas the transistor is controlled by current. Also, in the vacuum tube, the current flows through a vacuum while in a transistor the current flows through a solid. The magnitude of the emitter to collector current is controlled by varying the forward bias voltage. This action is similar to the vacuum tube in that the plate current of the tube is dependent upon the grid to cathode voltage. The vacuum tube employs a heater to cause electrons to leave the cathode by thermionic emission, whereas the transistor needs no such device. The electron flow in the vacuum tube is always from negative (cathode) to positive (plate), but the collector of the transistor may be either positive or negative with respect to the emitter depending upon whether electrons or holes are the current carriers. In most vacuum tubes there is no appreciable current between the cathode and the grid, whereas there is an emitter-base current present in the transistor.

4104. The Transistor as an Amplifier.

a. Introduction.—The transistor is capable of amplifying an electrical signal because of its electrical characteristics. Figures 4–18 and 4–19 show the normal circuit symbols for the

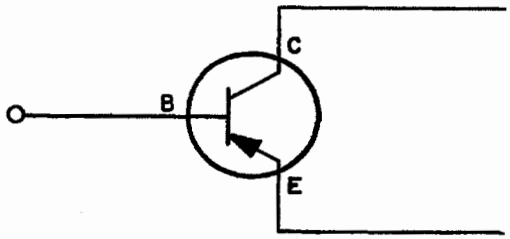


Figure 4–18.—Circuit Symbol for PNP Transistor.

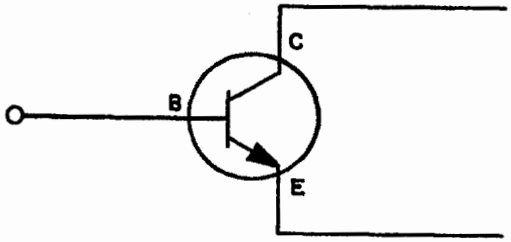


Figure 4–19.—Circuit Symbol for NPN Transistor.

PNP and NPN transistors. Note that the direction of the arrow on the emitter is towards the center of the transistor for the PNP transistor and away from the center for the NPN. The *electron* current in the emitter always flows against this arrow. Three rules will aid in understanding the physical behavior of the transistor as a circuit element; 1) the first letter in the designation of the type of transistor indicates the polarity of emitter voltage with respect to the base; 2) the second letter represents the polarity of the collector voltage with respect to the base; and 3) the first and second letters represent the polarity of the emitter with respect to the collector. There are three basic types of transistor amplifier circuits. These configurations will be discussed in the following sections.

b. Amplifier Types.

(1) *The common base amplifier.*—The common base configuration derives its name from the fact that the base of the transistor is connected to the input and output circuits as pictured in figure 4-20. The input signal is impressed between the emitter and the base,

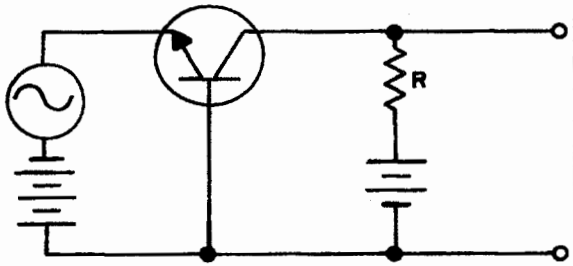


Figure 4-20.—Common-Base Amplifier (NPN).

and the output is taken from between the collector and the base. When a positive signal is impressed, the emitter forward bias voltage is decreased as well as the emitter current. Thus, the collector current is decreased and the voltage drop across resistor R is also decreased. Since the potential difference across the resistor has decreased, the *output* voltage increases. If a negative signal is used as the input, the output voltage *decreases* for the same reason. The output voltage in this type of amplifier is always in phase with the input signal. This configuration is similar to the grounded grid vacuum tube amplifier.

(2) *The common collector amplifier.*—The common collector amplifier is also known as an emitter follower and is similar to the vacuum tube cathode follower. In this configuration, the collector is common to the input and the output (fig. 4-21). The output

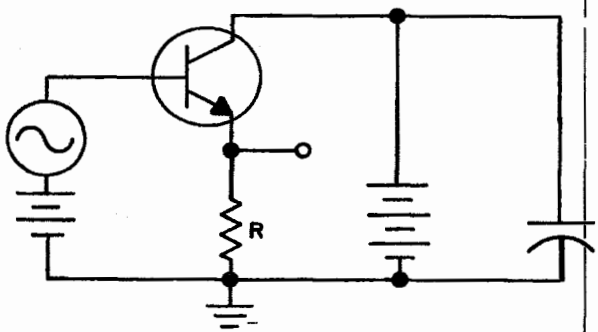


Figure 4-21.—Common-Collector Amplifier (NPN).

is taken from between the emitter and collector terminals and the input is impressed between the base and collector. The proper biases on the collector and emitter are maintained. During positive voltage input signal, the voltage across R increases and the output voltage decreases; the opposite is true for negative input. The output signal is in phase with the input signal.

(3) *The common emitter amplifier.*—With this configuration, the emitter is common to the input and output (fig. 4-22). A positive input signal causes a decrease in the output voltage and a negative input causes an increase in output voltage. The output signal is out of phase with the input. This circuit is similar to a grounded cathode vacuum tube circuit.

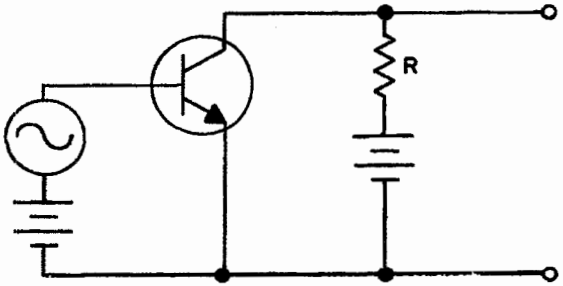


Figure 4-22.—Common-Emitter Amplifier (NPN).

(4) *Conclusion.*—In a discussion of this type, the actual mathematics and physics of the operation of transistors have been omitted. The descriptions provided will enable the student to acquire a general understanding of solid-state phenomena. Further analyses may be found in other publications and the reader is encouraged to delve as deeply into the subject as time and effort permit. The following paragraph (The Transistor as a Switch) will also be presented in a simplified form.

4105. The Transistor as a Switch.

a. *Introduction.*—The word "switch" is simply a term which has come into common usage; the correct term in this case is multivibrator. Other modifications of the multivibrator which have been given common names are "flip-flop", "binary", and "toggle". The entire field of multivibrators encompasses a broad area in the application of both vacuum tubes and transistors. This chapter will discuss only those types of transistor multivibrators most frequently encountered in the KW-7. Physically, the multivibrator is a regenerative-type amplifier employing two separate stages. The electrical operation of this device is characterized by the fact that conduction in one of the stages causes a voltage cutoff in the other stage. Essentially, this is accomplished by high positive voltage feedback. These states of operation are spoken of as end-states. The multivibrator circuit may be either in the stable or quasi-stable condition. If a circuit is in the stable condition, it will remain in one of the two end-states indefinitely unless externally excited. A circuit in the quasi-stable remains in one end-state for a definite time period, determined by the values of the circuit elements. It then returns to the other end-state. Multivibrators are classified as either astable (no stable states), monostable (one stable state, one quasi-stable state), or bistable (two stable states).

b. *The Astable Multivibrator.*—The astable multivibrator is depicted in figure 4-23. This type of multivibrator, also called the free-running multivibrator, has no stable states. It oscillates between two quasi-stable states. The output waveform from this device is usually rectangular, thus it is commonly employed as a pulse generator for testing digital circuitry.

Conduction in one transistor causes cutoff in the other, and the oscillations are repetitive as long as power is constantly applied; an on-off action of the transistors is thus achieved. Pulse width and repetition time are functions of the R-C time constants. If sufficient collector voltage is not supplied, or if the device is designed for too high a frequency, a truly rectangular waveform will not be achieved.

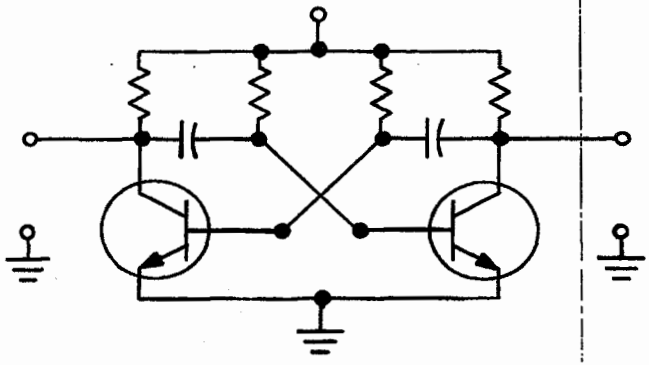


Figure 4-23.—Astable Multivibrator.

c. *The Monostable Multivibrator.*—The circuit arrangement for the monostable multivibrator, also called the one-shot multivibrator, is shown in figure 4-24. The monostable multivibrator has one stable state and one quasi-stable state, but it does not oscillate like the astable type. The circuit remains in the stable state (one transistor on and the other off) until it is triggered by an external pulse. It remains in this new quasi-stable state for a period determined by the value of the coupling capacitor and associated resistance. It then returns to its original condition. Each applied trigger produces one rectangular pulse, hence the name of one-shot multivibrator. Digital computers employ the monostable multivibrator as a gating device, as a time delay device, and as a pulse width varier. Either a positive or a negative pulse may be applied to the device.

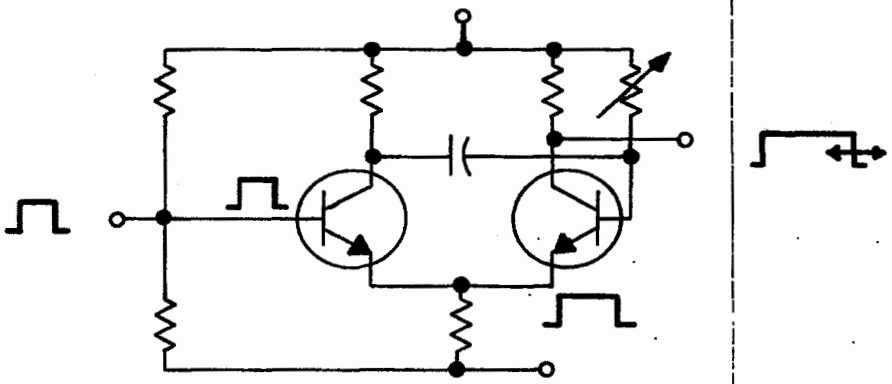


Figure 4-24.—Monostable Multivibrator.

d. *The Bistable Multivibrator.*—The basic circuit from which all types of bistable multivibrators are developed is shown in figure 4-25 and is known as the Eccles-Jordan trigger circuit. The bistable multivibrator is commonly referred to as a "flip-flop". The flip-flop derives

its name from the actual operation of the bistable multivibrator which has two stable states. The device can rest in either of these two states until an external trigger is applied. Unlike the monostable multivibrator, the bistable multivibrator must be retriggered to return it to its original state. The most common use of the bistable multivibrator is for "storing" either the ONEs or ZEROs of the binary numbering system used in digital computers. Various arrangements of flip-flops may be constructed to perform arithmetic operations such as addition, subtraction, multiplication, and division. The bistable multivibrator may also be employed to generate rectangular pulses, but two trigger pulses are required to form the wave. The logical flip-flop, most commonly used in digital computer circuits, is similar to the basic Eccles-Jordan trigger circuit with the following modifications: 1) logical switching circuits are placed at the input and output, 2) provisions for resetting the flip-flop are provided, 3) circuitry is added to render the flip-flop useful in systems employing square waves, and 4) output circuits are added to provide a means of monitoring the state of the flip-flop.

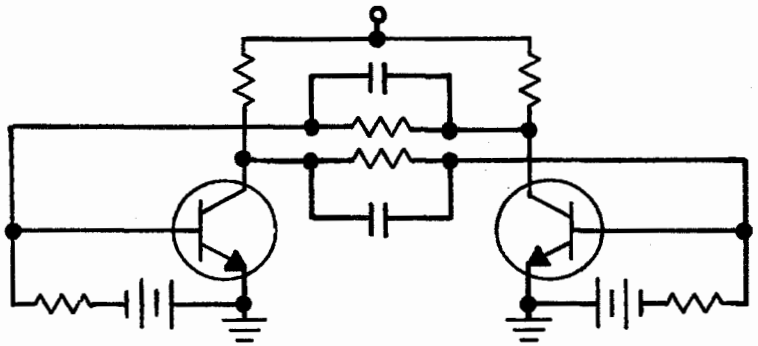


Figure 4-25.—Bistable Multivibrator.

e. Conclusion.—In multivibrator application, the input of one amplifying stage is directly connected to the output of the second stage. Employing the three types of multivibrators and the various configurations within each classification, many useful devices may be constructed. It is these various devices that have lent to the rapid development of digital techniques.

4106. The Schmitt Trigger.

a. Introduction.—The Schmitt trigger differs from the ordinary bistable multivibrator in that one of the coupling networks has been replaced by a common-emitter resistor. The Schmitt trigger is in reality an emitter coupled bistable multivibrator (fig. 4-26). In the operation of all types of electrical equipment, electrical noise is always present in varying degrees of magnitude. Noise waveforms not only enter between signal pulses but they may very well affect the signal pulse itself. Since digital computers are made to respond to specific types of waveforms, it often becomes necessary to reshape these waves. This function is performed by the Schmitt trigger which converts any input signal to a rectangular wave of fixed amplitude.

b. Operation.—The end state of a Schmitt trigger is determined by the amplitude of the input signal relative to a fixed preset level. This level is established by the base to emitter bias. Figure 4-26 illustrates a typical Schmitt trigger, with a signal applied to the input terminals which is more positive than the preset level, the output transistor saturates. This provides

a maximum positive voltage at the output terminals. When the input returns to a level below the reference point, the circuit changes state and the output transistor goes to cut off. The output voltage is then at the maximum negative value. Typical input and output waveshapes for a Schmitt trigger are shown in figure 4-27.

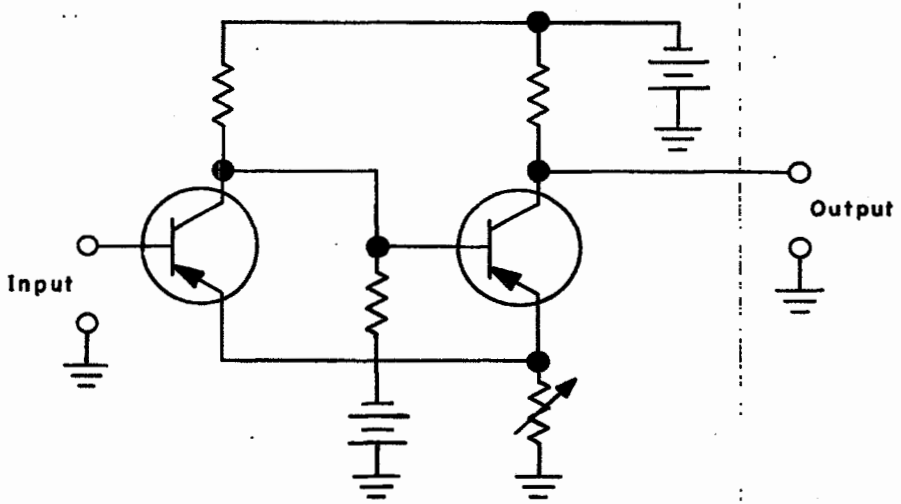


Figure 4-26.—Typical Schmitt Trigger.

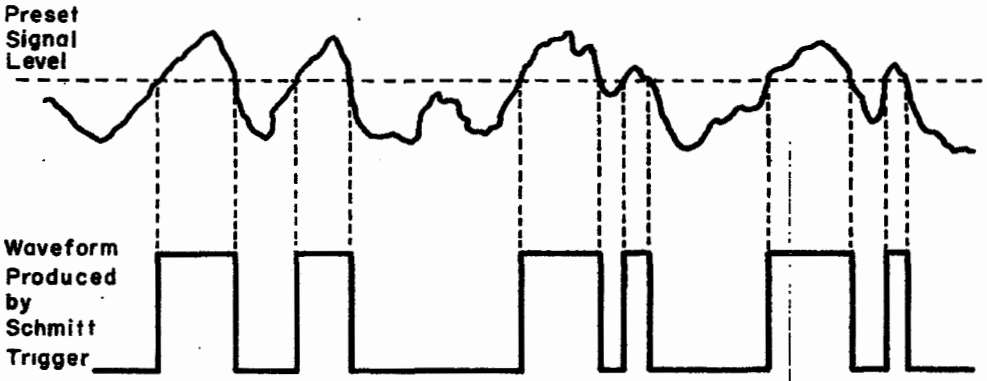


Figure 4-27.—Waveform Discrimination and Signal Detection (Schmitt Trigger).

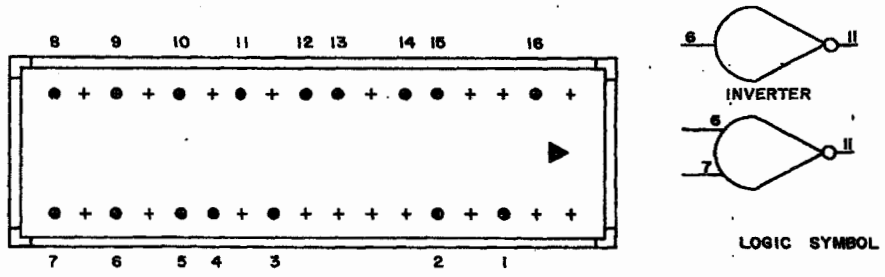
4200—DETAILED THEORY, BASIC KW-7 CIRCUITS

4201. General.—Logical operation of the KW-7 is accomplished by the arrangement of basic circuits in many functional configurations. These basic circuits are packaged in modules which serve as the building blocks of the KW-7 system. The modules, or logic elements, contain one or more circuits, the operation of which may be modified by external connections. A prerequisite for an understanding of the KW-7 is a thorough knowledge of the operation of the various logic elements. The discussions that follow are supported by schematic diagrams of the logic elements. Included in each diagram is the appropriate logic symbol and, where applicable, a truth table which defines the input/output relationship. Those modules which were designed for specific application are not covered here. These units are described within the coverage for the specific circuit where they are used.

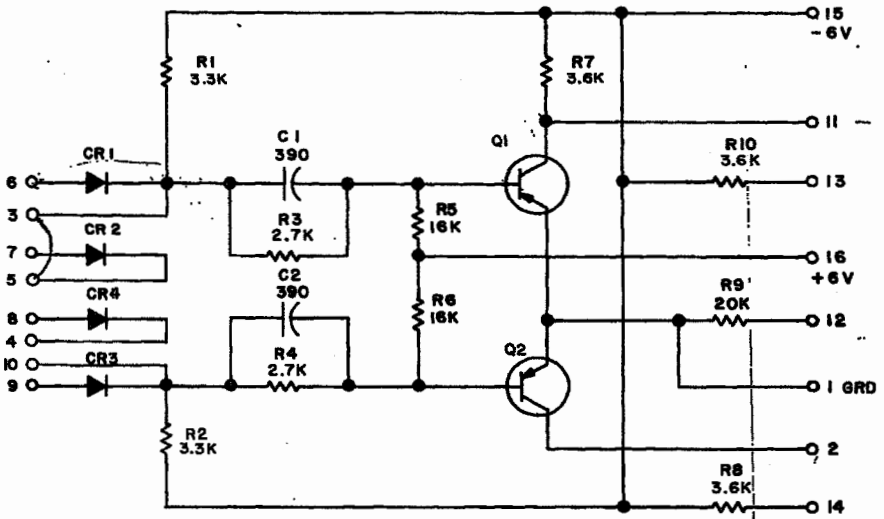
4202. NOR Gate (fig. 4-28).—Two logic elements contain the circuits which perform the logical NOR function. One of these elements (fig. 4-28) may be connected to provide two independent two-input NOR gates. The other element (fig. 4-29) may be connected to provide two independent three-input NOR gates. The logical NOR function may be represented by the boolean expression $X = \overline{A + B}$, where X = output and A and B are the input signals. This expression is read "not A or B". The combination of "not" and "or" provides a ONE output when both inputs are ZERO. With any other input conditions the ouput is a ZERO. In this example a two-input gate has been used. The principle is the same, however, regardless of the number of inputs—the output is a ONE only when all inputs are ZERO. The truth table for a two-input NOR gate is shown in figure 4-28.

a. *Two-Input NOR Gate.*—The element illustrated in figure 4-28 contains circuits which may be connected to form two individual NOR gates. A single independent NOR gate may be formed when input signals are applied to terminals 6 and 7 and terminals 3 and 5 are connected. The output of the gate is available at terminal 11. The NOR gate consists of two-basic parts: a diode OR and an inverter. The OR gate is formed by diodes CR1 and CR2 and resistor R1. The inversion is performed by transistor Q1 and associated components. The input at terminals 6 and 7 are either logical ZERO's or ONE's (in the KW-7 the logical ZERO has been defined as a −6-volt signal, the logical ONE as a 0-volt signal). Because of the negative bias applied to their cathodes through R7, CR1 and CR2 conduct when a logical ONE (0-volts) is applied to their respective input terminals. With either or both diodes conducting a positive voltage is fed through the coupling network composed of capacitor C1 and resistor R3 to the base of Q1. This cuts the transistor off and the full supply voltage appears at the collector. This voltage, −6V, represents a logical ZERO and is the output of the NOR gate. In the case where a logical ZERO is applied to both input terminals, neither diode conducts and the condition of the inverter is determined by the base-to-emitter bias. The base of Q1 is tied to the junction of resistors R3 and R5 which with R1 form a series voltage divider connected between the +6 and −6V DC supplies. This forward biases Q1 and saturates it. Since the emitter connection is returned to ground, the transistor conducts. This results in a large voltage drop across the load resistor and a collector voltage which approximates zero volts—a logical ONE. With a single input the circuit operates as a simple inverter, producing a ONE output with a ZERO input and a ZERO output with a ONE input. Additional diodes may be added to the input circuit, permitting each transistor to handle up to five inputs. To reduce the level of the logical ZERO from −6 to approximately −5.1 volts, terminal 12 is shorted to terminal 11. This connects resistor R9 across Q1.

b. *Three-Input NOR Gate.*—Figure 4-29 illustrates the schematic of the module which may be connected to form two three-input NOR gates. In addition to the schematic, figure 4-29 also illustrates the logic symbol and the truth table for the three input NOR gate. For transistor Q2 to operate as an individual NOR gate it is necessary to jumper pins 12 and 13 together. Transistor Q1 operates as a NOR gate without further connections. If both



NOTE: UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS ARE 1/4 W ±5%
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS
ALL TRANSISTORS ARE 2N404
ALL DIODES ARE IN695
ON007836
COLOR: DARK YELLOW



2 INPUT NOR GATE TRUTH TABLE

INPUT	A	0	0	1	1
	B	0	1	0	1
OUTPUT	$X=\overline{A+B}$	1	0	0	0

INVERTER TRUTH TABLE

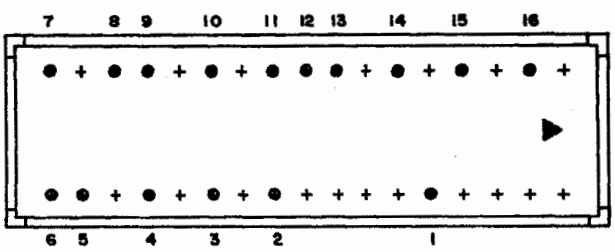
INPUT	A	0	1
OUTPUT	$X=\overline{A}$	1	0

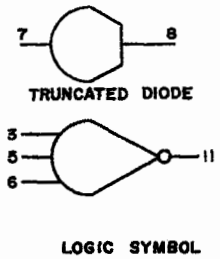
Figure 4-28.—Two-Input NOR Gate/Inverter Module, Schematic Diagram.

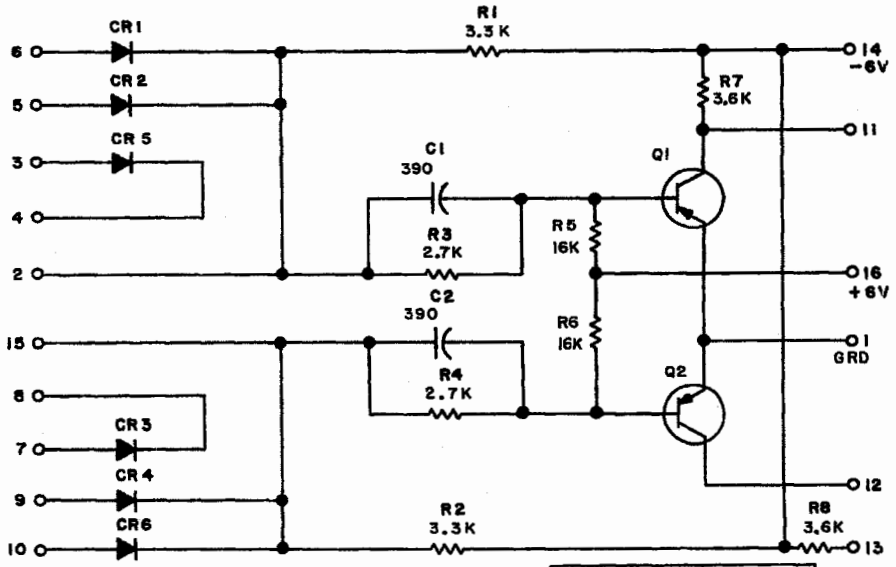
transistors are to be used as NOR gates with a common output, pin 12 should be jumped to pin 11 and resistor R7 would then be used as the common collector load resistor. For transistor Q1 to operate as a three input NOR gate, it is necessary to jumper pins 2 and 4 together. The theory of operation for the three input NOR gate is the same as that for the two input NOR gate.

4203. Truncated Diode.—To give versatility to the use of the Two-Input and Three-Input NOR gates, two diodes in each module are not internally connected to the input circuit. These

diodes (CR2 and CR4 of the Two Input NOR gate and CR3 and CR5 of the Three Input NOR gate) may be used to supplement the input of either of the two types of NOR gates. This permits a maximum of five inputs. A truncated diode is drawn on the logic diagrams only when the diode contained in one module is used to supplement the input of a Two Input or Three Input NOR gate contained in another module. Figure 4-29 illustrates the logic symbol for the truncated diode.







NOTE: UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS ARE 1/4W ± 5%
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS
ALL TRANSISTORS ARE 2N404
ALL DIODES ARE IN695
ON003837
COLOR: LIGHT YELLOW

INPUT	A	00001111
	B	00110011
	C	01010101
OUTPUT	$X=\overline{A+B+C}$	10000000

TRUTH TABLE

Figure 4-29.—Three-Input NOR Gate/Truncated Diode Module, Schematic Diagram.

4204. Inverter.—Figure 4–28 illustrates the schematic for the two-input NOR gate. When either portion of this gate (transistor Q1 and Q2) is utilized with a single input (either pin 6 or pin 9) the NOR gate acts as an inverter. The inverter inverts the logical value of a single input signal. In addition to the schematic, figure 4–28 also illustrates the logic symbol and the truth table for the inverter. The theory of operation for the inverter follows that discussed for the two-input NOR gate and need not be repeated.

4205. Low Speed Flip-Flop (fig. 4–30).—The low speed flip-flop circuit is a conventional Eccles-Jordan bistable multivibrator. This circuit differs from the bistable multivibrator primarily in the base emitter arrangement. In the stable state, one transistor is conducting (ON) while the other is cut off (OFF). The states of the transistors are switched with the application of a properly applied trigger pulse. In addition to the schematic, figure 4–30 also illustrates the logic symbol for the low speed flip-flop.

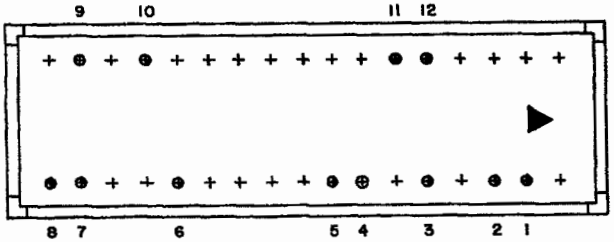
a. *Circuit Operation.*—The application of a negative trigger pulse to the base of the cutoff transistor or a positive pulse to the base of the conducting transistor will switch the conducting state of the circuit. Figure 4–30 shows two separate inputs: pins 1 and 2 and 7 and 8. It should be mentioned that pins 1 and 2 feed an AND gate (capacitor C3, resistor R7, and diode CR1) and pins 7 and 8 also feed an AND gate (capacitor C4, resistor R8, and diode CR2). The operation of the AND gate is described in a later subparagraph and need not be explained here. It will suffice to mention that the output from this gate is a +6 volt pulse when a logical ONE is applied to the resistor and a positive going pulse is applied to the capacitor. In addition to these two AND gates, provision is made for the external addition of extra AND gates. Pins 4 and 9 serve this purpose.

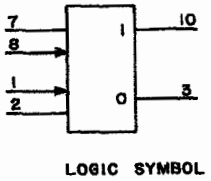
b. *Trigger Pulse Application.*—Assume that transistor Q1 is conducting and transistor Q2 is cut off. A positive input from pins 1 and 2 causes transistor Q1 to cut off. The drop in collector current in transistor Q1 causes the collector voltage to decrease. This change in voltage is coupled to the base of transistor Q2 and increases its forward bias; conduction in transistor Q2 begins to increase. The collector current increases, and the collector voltage changes from a negative value to a more positive value. This change in voltage is coupled to the base of transistor Q1, making the base more positive and further decreasing the conduction of the transistor. The regenerative feedback continues until transistor Q1 is in a cutoff condition and transistor Q2 is conducting at saturation. The time constants of capacitor C1 and resistor R2, and capacitor C2 and resistor R3 essentially determine the fall time (from conduction to cutoff) of both transistors. It may be noted that during the rapid transition period, both transistors conduct. In one transistor the conduction is increasing and in the other the conduction is decreasing. The output taken between collector and ground is a unit step voltage when one trigger is applied. To arrange the circuit as a complementing flip-flop the following terminals are connected together: 2 to 10, 7 to 3, and 1 to 8. When these connections are made an enabling signal need not be applied to the input gate and the flip-flop changes state with a trigger at either input terminal.

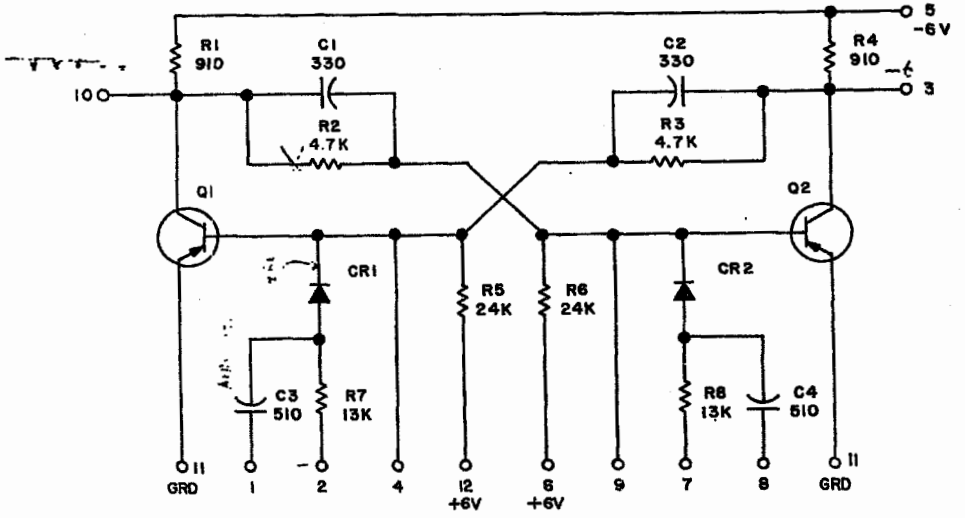
4206. Medium Speed Flip-Flop (fig. 4–31).—The medium speed flip-flop is a conventional bistable multivibrator. The theory of operation is essentially the same as that of the low speed flip-flop, which is described in the previous paragraph. Circuit differences which are in the input circuit will be discussed here. This module is used only in the divide-by-20 counter. For this reason the circuit is arranged as a complementing flip-flop. The binary input to the flip-flop is applied to terminal 5. Steering diodes CR1 and CR5 insure that the positive input pulse is applied to the base of the conducting transistor. In some cases a delete pulse is fed back to the flip-flop. This signal is applied to terminal 7 and results in a logical ZERO at output terminal 3.

a. *External Connections.*—The following terminals are connected: 9 to 10, 3 to 6, and 2 to 4. When the circuit application requires a delete input, terminal 8 is grounded and a feedback pulse is applied to terminal 7.

b. Circuit Operation.—As previously stated, the medium speed flip-flop is arranged as a complementing flip-flop. This stage changes state every time one input pulse is applied to terminal 5. Diode steering gates associated with each transistor insure that the input is applied to the base of the conducting transistor. The steering gate for transistor Q1 is formed by diodes CR1 and CR2, and for Q2 by diodes CR4 and CR5. Assuming that Q1 is conducting and Q2 is cut off, CR1 is biased on by the collector voltage of Q1, while CR5 is biased off by the collector voltage of Q2. With CR5 biased off, no current flows through reistor R4 and a −6 volt potential is applied to the anode of CR4. This bias prevents CR4 from conducting when an input pulse is applied through terminal 5 to capacitor C5. However, with CR1 biased on, there is a large voltage drop across R1 and the potential at the anode







NOTE, UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS ARE 1/4W, ±5%
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS
ALL TRANSISTORS ARE 2N404
ALL DIODES ARE IN695
ON007841
COLOR. MEDIUM MAROON

Figure 4-30.—Low-Speed Flip-Flop Module, Schematic Diagram.

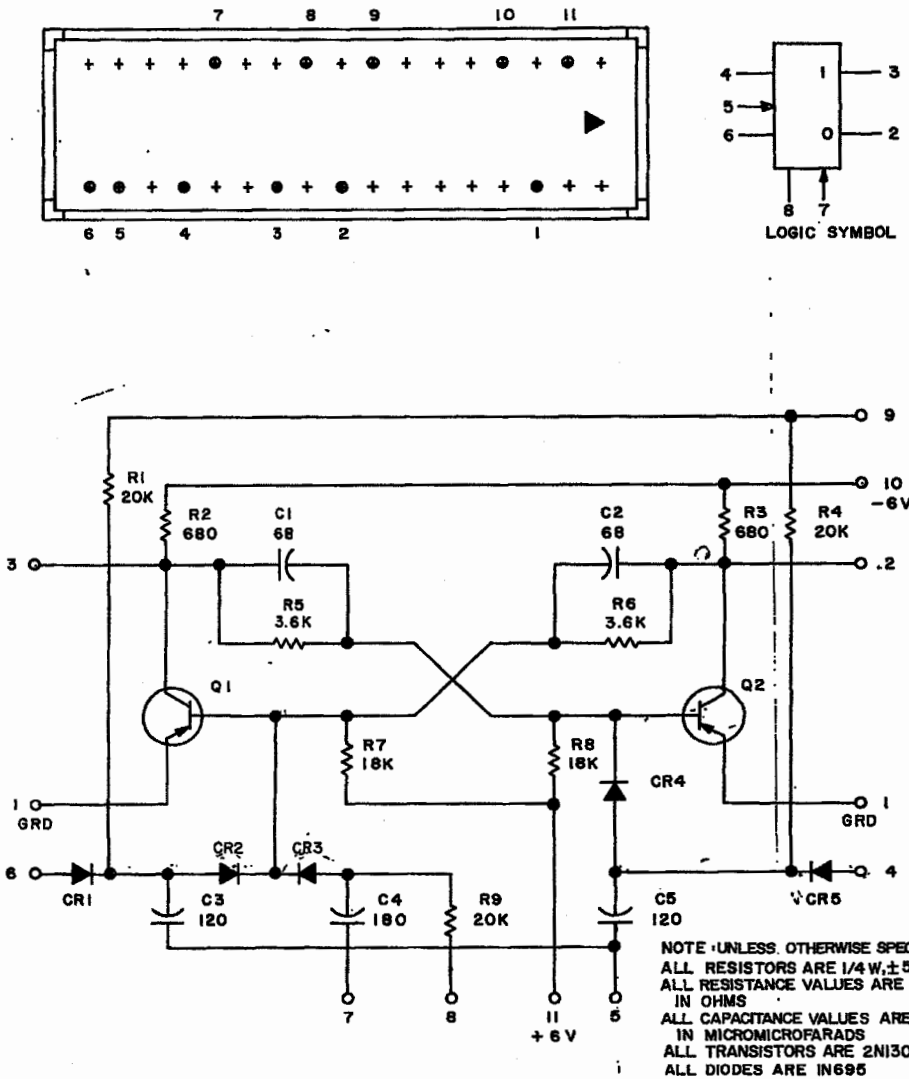
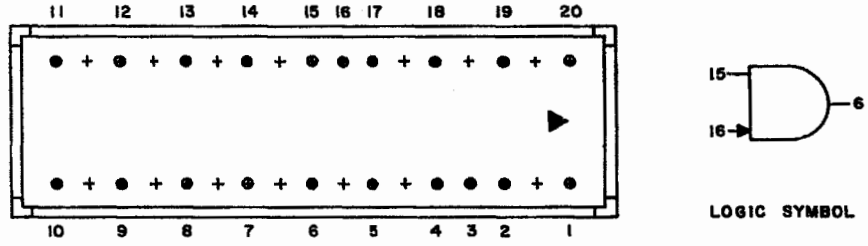


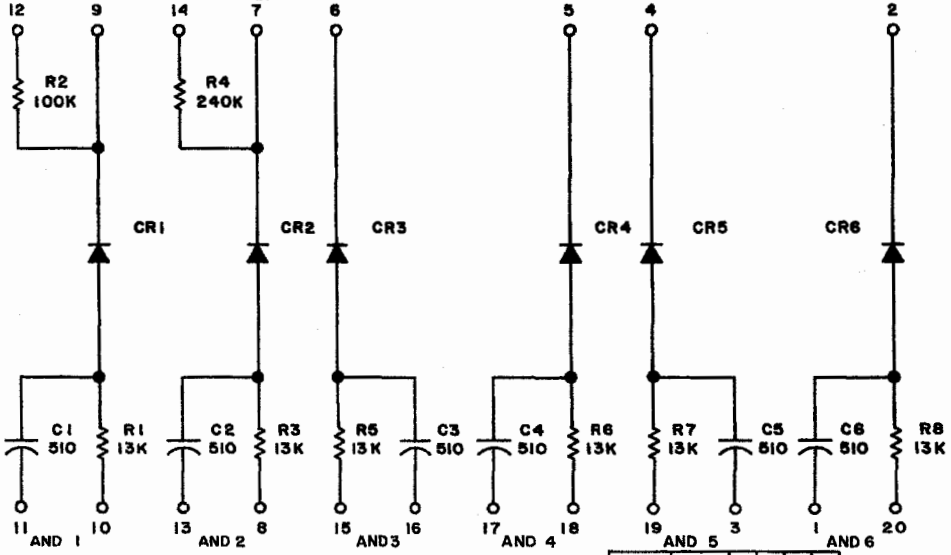
Figure 4-31.—Medium-Speed Flip-Flop Module, Schematic Diagram.

of CR2 is such that the diode is forward biased. In this condition the positive input pulse is coupled through C3 and CR2 to the base of Q1. Circuit operation is the same when Q1 is cut off and Q2 is conducting. In this case, CR4 is forward biased and CR2 is reverse biased. When the feedback gate is used, terminal 9 is grounded; this permanently enables an AND gate consisting of diode CR3, resistor R9, and capacitor C4. The feedback pulse occurs when the output of the flip-flop would normally be a logical ONE. This pulse, applied to the base of Q1, cuts off the transistor and returns the output (taken from the collector of Q1) to a logical ZERO.



LOGIC SYMBOL

NOTE ; UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS ARE 1/4W, ±5%
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS
ALL DIODES ARE IN695.
OR 007842
COLOR: GREY



TRUTH TABLE

INPUT	A	1	1	0	0
	B	1	0	1	0
OUTPUT	X=A·B	1	0	0	0

M

Figure 4-32.—AND Gate Module Schematic Diagram.

4207. AND Gate.—Figure 4-32 illustrates the module which contains the various external AND gate combinations utilized by all low speed flip-flops and one-shot multivibrators. The function of the AND gate is to provide triggering when an enabling level and a trigger pulse are simultaneously applied to the input terminals. In addition to the schematic, figure 4-32 also illustrates the logic symbol and the truth table for the AND gate.

Note: The term AND is derived from the logical operation of the circuit; if A "and" B are "one's" then the output is a "one". It should be noted that the ONE output of the AND gate is a +6 volt pulse. This applies only to the AND gate.

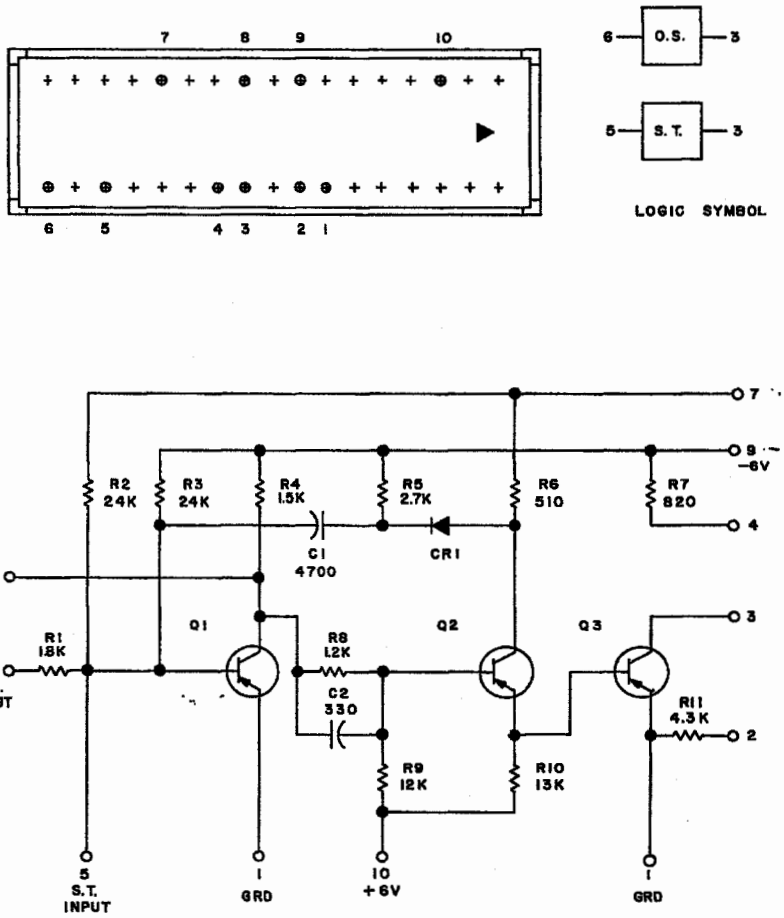
a. *AND Gate Combinations.*—The AND gate module contains six individual AND gates. All low speed flip-flops have provision for addition of four external AND gates to each side of the flip-flop. The low speed flip-flop also contains two internal AND gates which are identical with AND gates 3 through 6 (fig. 4-32). To add an input to each side of a flip-flop any pair of AND gates 3 through 6 are connected to the flip-flop input. When three inputs are required to any one side of a flip-flop, AND gate 2 is used with one of AND gate 3 through 6. Resistor R4 (240K), returned to +6 volts, compensates for the loading effects of the three AND gates on the flip-flop. When four inputs are required to any one side of the flip-flop, AND gate 1 is used with two other AND gates selected from gates 3 through 6. Resistor R2 (100K), returned to +6 volts, compensates for the loading effects on the flip-flop. By adding AND gate 2 to this combination, the input gates are increased to the maximum of five.

b. *Circuit Operation.*—The output of the AND gate is a +6 volt pulse only when both inputs are logical ONEs, providing that the level input (shown by the straight line input) to the resistor arrives before the pulse signal input (shown by the arrow input) to the capacitor. A positive-going transition at the capacitor input always causes the capacitor-resistor network to create a positive-going pulse with a 6-volt step. If the enabling ONE (0 volts) is present at the resistor input prior to the pulse input to the capacitor and the capacitor has charged sufficiently, this 6-volt step passes through the diode and appears at the AND gate's output as +6 volts. If the resistor input remains at the ZERO level, (−6 volts) however, the 6-volt step results in a 0-volt level being applied to the diode. Under this condition, the diode can not conduct and therefore the AND gate has no output. From this discussion, it is apparent that the 6-volt step is always referenced to whatever voltage is present at the resistor input.

4208. One Shot Multivibrator.—Figure 4-33 illustrates the schematic of the module which may be connected as either a one-shot multivibrator or a Schmitt trigger. The following discussion describes the operation of the module when it is arranged as a one-shot multivibrator. This circuit produces an output pulse of a predetermined duration each time an input trigger is applied. Included in the module is an output amplifier. The logic symbol for the one-shot multivibrator is included in figure 4-33.

a. *Circuit Operation.*—The application of a positive trigger pulse to the base of the conducting transistor will switch the transistor from its stable state to its quasi-stable state. Figure 4-33 illustrates one input and two outputs (pins 8 and 3). The one-shot multivibrator produces a logical one (0 volts) at pin 3 whenever the circuit is triggered by a positive pulse. When no positive input is applied to the circuit the output at pin 3 is a logical ZERO (−6 volts). In order for this circuit to operate as a one-shot, pins 3 and 4 and pins 7 and 9 must be jumpered together.

b. *Trigger Pulse Application.*—With pins 7 and 9 tied together, a negative voltage is applied to the base of transistor Q1 causing it to conduct. This causes a positive voltage to appear at the base of Q2, which presents a positive voltage to the base of Q3, the output stage. The positive voltage at the base of Q3 (reverse bias) cuts this stage off and therefore causes the output to assume a logical ZERO (−6 volts) state. Thus, the quiescent output level of the one-shot multivibrator is a logical ZERO. To trigger the one-shot multivibrator a



NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/4W, ±5%
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROFARADS
ALL TRANSISTORS ARE 2N404
ALL DIODES ARE IN695.
FOR ONE SHOT OPERATION, CONNECT PIN 7 TO PIN 9
FOR SCHMITT TRIGGER OPERATION, CONNECT PIN 7 TO PIN 3
IN ALL OPERATIONS, EXCEPT WHEN DRIVING A SET DRIVER
CONNECT PIN 3 TO PIN 4
ON007843
COLOR: BLACK

Figure 4-33.—One Shot/Schmitt Trigger Module, Schematic Diagram.

positive going pulse is applied to pin 6 from an AND gate (see 4207 above). This positive going transient cuts stage Q1 off causing Q1 collector voltage to go negative. The negative going collector voltage at Q1 is coupled to the base of Q2 causing the Q2 collector current to increase. The increase collector current has a dual effect and the resultant negative-going swing at the emitter is coupled to the base of output stage Q3. This drives Q3 to saturation, producing a logical ONE at the output. At the same time the positive-going collector voltage forward biases CR1 and charges C1 such that stage Q1 is cut off. Q1 will be held off (causing the output to remain at a logical ONE) by this positive feedback network long after the input transient which caused this condition has disappeared. C1 then discharges towards −6 volts but becomes clamped at ground (34 microseconds) by the base emitter junction of Q1. At this time the one-shot multivibrator resumes its quiescent state causing the output to return to a logical ZERO (−6 volts).

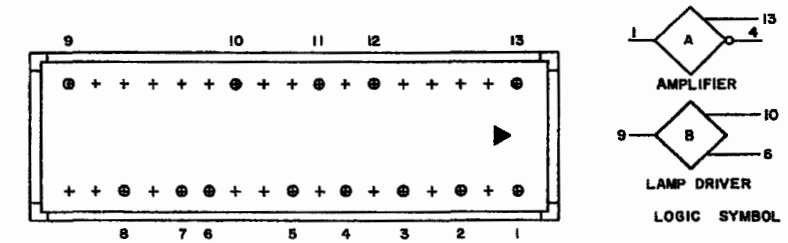
4209. Schmitt Trigger.—The discussion that follows is concerned with operation of module described above when it is connected as a Schmitt trigger. The Schmitt trigger is essentially a conventional Eccles-Jordan bistable multivibrator with one of the regenerative coupling networks replaced by a 24K resistor (R2). This particular arrangement provides additional regenerative feedback to obtain a faster switching time. In addition to the schematic of the Schmitt trigger, figure 4–33 also illustrates the logic symbol for the Schmitt trigger. Schmitt trigger operates in one of two stable states. When the circuit is triggered by a positive external signal it is switched from one stable state to the other. It will remain in this state until the external input signal drops below the triggering level. At this time the circuit will revert to its original state.

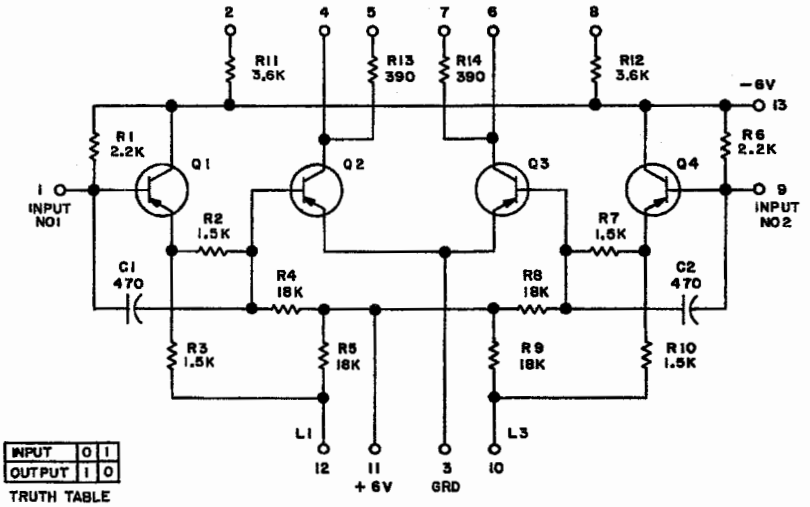
a. *Circuit Operation.*—The application of a positive voltage to the base of the conducting transistor will switch the conducting state of the circuit. Figure 4–33 illustrates one input (pin 5) and one output (pin 3). The Schmitt trigger produces a logical ONE output (0 volts) at pin 3 whenever the input at pin 5 is a logical ONE. When the input to pin 5 is a logical ZERO (−6 volts), the output at pin 3 will be a logical ZERO. In order for the Schmitt trigger to operate, pins 3, 4, and 7 must be jumpered together.

b. *Trigger Pulse Application.*The operation of the Schmitt trigger in the quiescent state is identical to that of the one-shot multivibrator and need not be repeated. When pulsed, however, operation is quite different. The purpose of the Schmitt trigger is to "square" the input pulse. That is, decrease the rise and fall times of the applied pulse. When the leading edge of a pulse is applied to the input (pin 5) it resembles a ramp function (long rise time). Q1 will be gradually reverse biased. The effects of this reverse bias are amplified by Q2 and Q3 and then fed back to the input of Q1 through R2, further reverse biasing Q1. This effect avalanches with the result that the ramp function is converted into a step with a fast rise time. The opposite effect takes place when the input pulse starts to fall towards a logical ZERO (−6 volts). The output of the Schmitt trigger then is a replica of the input pulse except that it is "squared" and amplified.

4210. Amplifier.—Figure 4–34 illustrates the module which contains two independent circuits, each of which may be connected as either a power amplifier or a lamp driver. In addition to the schematic, figure 4–34 also illustrates the logic symbol for the amplifier. The discussion that follows describes operation of an amplifier. For purposes of clarity only one of the two amplifier circuits will be discussed. For transistors Q1 and Q2 to operate as an amplifier, it is necessary to jumper pin 2 to pin 4. (If the other half of the circuit were used, pins 6 and 8 would be jumpered together.) The output of the circuit is taken from pin 4 (pin 6, if the other half of the circuit is used).

a. *Circuit Operation.*—The amplifier consists of an emitter follower (Q1) and a common emitter amplifier (Q2). The emitter follower is used in the circuit as an impedance matching device for the input and output signal (high input impedance and low output impedance).



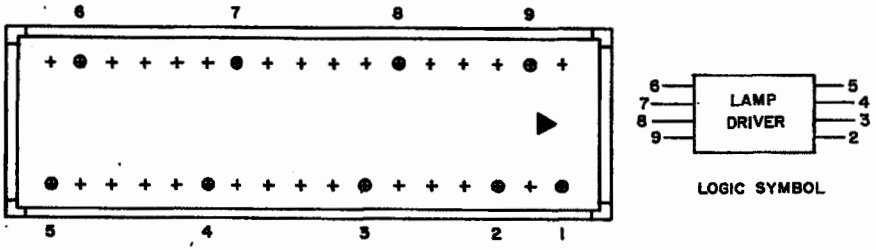


NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/4W, ±5%
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS
ALL TRANSISTORS ARE 2N404
PINS 10 AND 12 USED ONLY TO DRIVE REMOTE CONTROL UNIT LAMP DRIVER.
FOR AMPLIFIER APPLICATION: JUMPER PIN 2 TO PIN 4 (A) AND/OR PIN 6 TO PIN 8 (B).
FOR LAMP DRIVER APPLICATION: GROUND PINS 5 (A) AND/OR 7 (B).
ON007838
COLOR: MEDIUM ORANGE

Figure 4-34.—Power Amplifier/Lamp Driver Module, Schematic Diagram.

b. Input Signal Application.—A logical ONE (0 volts) applied to the base of transistor Q1 is impressed on the base of Q2 through emitter resistor R2. This positive-going voltage causes transistor Q2 to become cut off and causes the collector voltage to decrease to a negative value. This negative output is taken from pin 4 and is used throughout the KW–7 circuits.

4211. Lamp Driver.—When properly connected, the module described in the previous paragraph (fig. 4–34) may be used to form two independent lamp drivers. For purposes of clarity only one lamp driver circuit will be discussed. The lamp driver physical configuration is identical with that for the amplifier circuit discussed in the preceding paragraph. For transistors Q1 and Q2 to operate as a lamp driver, it will be necessary to jumper pin 5 to pin 3. (If the other half of the circuit were being used, pin 7 would be jumpered to pin 3.) The two outputs from this circuit are taken from pin 6 (pin 4 from the other half of the circuit), and pin 10 (pin 12 from the other half of the circuit). Pin 12 and pin 10 respectively supply voltage to the remote box lamp driver. The only difference between the lamp driver and the amplifier is that one side of



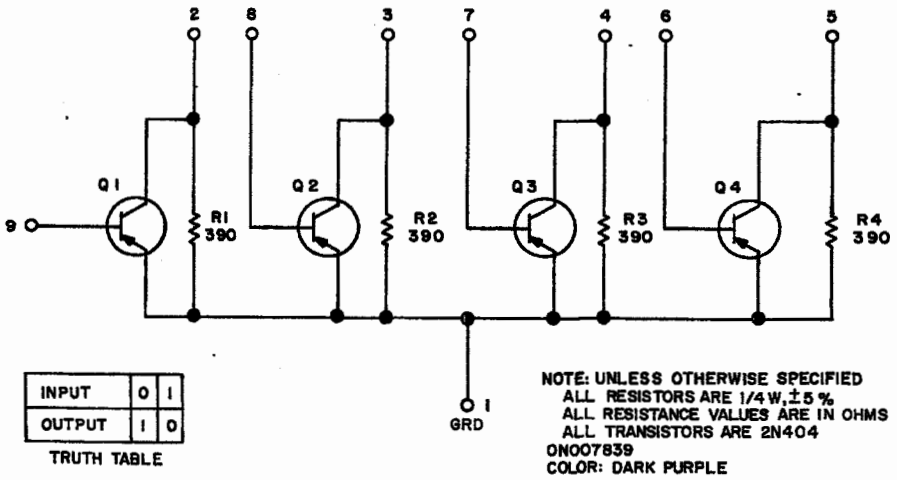
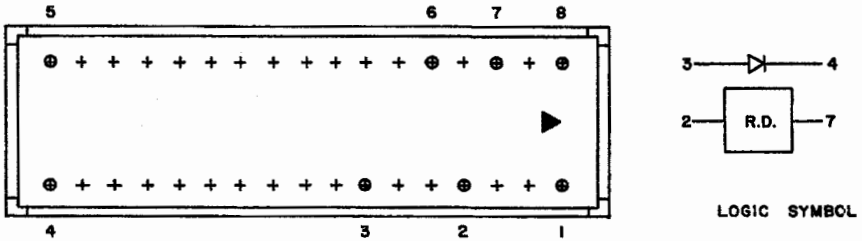


Figure 4–35.—Remote Control Unit Lamp Driver Module, Schematic Diagram.

an indicator lamp is tied to pin 4 and the other side of the indicator lamp to a −6 volts. A logical ZERO input (−6 volts) to the lamp driver will apply a logical ONE (0 volts) at pin 4 and cause the indicator lamp to light.

4212. Remote Control Unit Lamp Driver.—Figure 4–35 illustrates a string of four lamps drivers. These lamp drivers operate on separate inputs and each output (pins 2, 3, 4, and 5) is tied to one side of an indicator lamp; the other side of the indicator lamp is tied to −6 volts. The application of a logical ZERO input (−6 volts) to any of the input pins (pins 9, 8, 7, or 6) will cause the indicator lamp to light. The remote control unit lamp driver must be used in conjunction with the lamp driver (fig. 4–36) with one of the input pins (pins 6, 7, 8 or 9) being connected to pin 10 or 12 of the lamp driver.



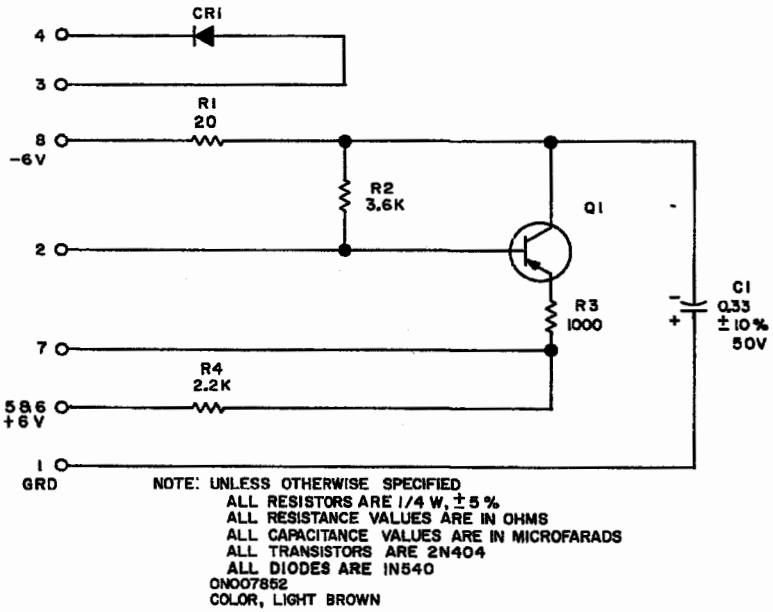
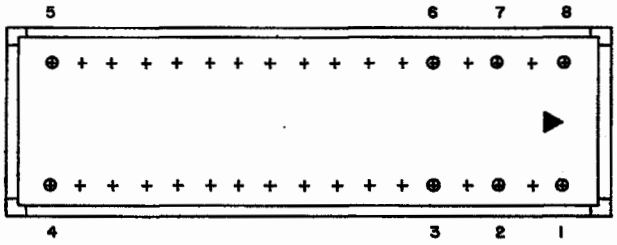
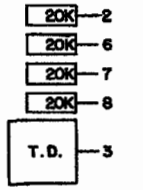


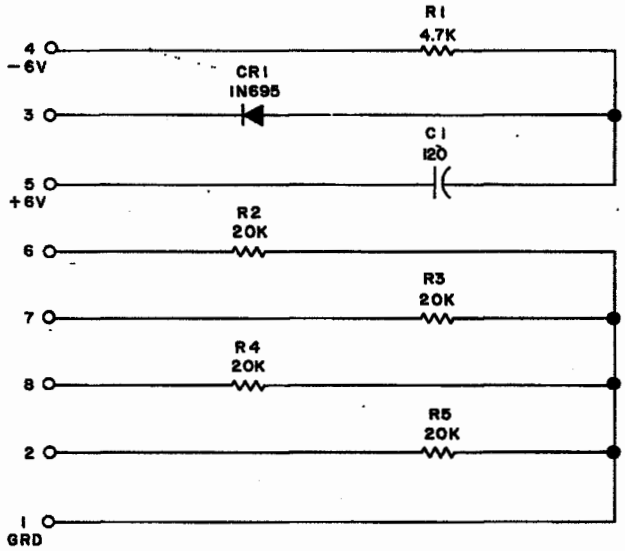
Figure 4–36.—Relay Driver Module, Schematic Diagram.

4213. Relay Driver.—The module illustrated in figure 4-36 is a simple emitter follower which is used to provide driving current for a relay circuit. The output signal, developed across resistor R4, is taken from terminal 7. A decoupling network consisting of resistor R1 and capacitor C1 prevents the feedback of transients to the output terminals of the −6 VDC supply. Also included in the module is a diode, CR1, which may be connected across a relay coil to provide transient suppression.



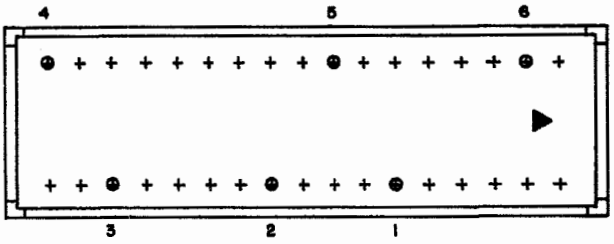


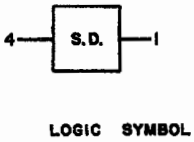
LOGIC SYMBOL

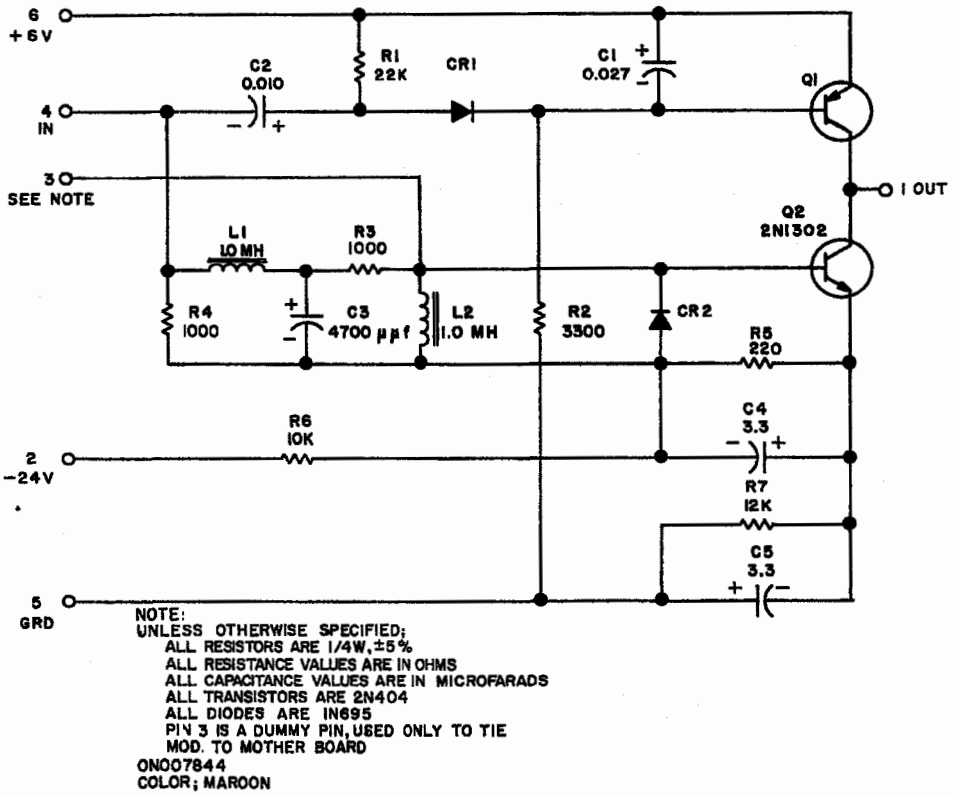


NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/4W, ±5%
ALL CAPACITANCE VALUES ARE IN MICROFARADS
ONO07850
COLOR, LIGHT PURPLE

Figure 4-37.—Time Delay Module, Schematic Diagram.







NOTE:
UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS ARE 1/4W, ±5%
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROFARADS
ALL TRANSISTORS ARE 2N404
ALL DIODES ARE IN695
PIN 3 IS A DUMMY PIN, USED ONLY TO TIE
MOD. TO MOTHER BOARD
ON007844
COLOR; MAROON

Figure 4-38.—Set Driver Module, Schematic Diagram.

4214. Time Delay (fig. 4-37).—A time delay circuit is used to provide a short time delay between the application of power and the initial setting of the logic circuits of the KW-7. This circuit is formed by resistor R1, capacitor C1, and diode CR1. When power is applied to the unit a −6 volt potential appears at terminal 4 and a +6 volt potential at terminal 5. At this time the output of the module, at terminal 3 is a +6 volt signal. As the capacitor changes the voltage changes in a negative direction. The circuit values are such that this change is relatively linear and the output is a negative-going ramp signal. This signal is applied to the input of a Schmitt trigger. After a period of 200 milliseconds the signal reaches the triggering level of the Schmitt trigger and the initial set signal is generated. Included in the module are four 20K ohm resistors which may be used to attenuate the output of a NOR gate. Such attenuation is required when the NOR output is used as the transient input for an AND gate which has been enabled by the output of a flip-flop.

4215. Set Driver (fig. 4-38).—The schematic of a set driver is illustrated in figure 4-38. The module provides a ZERO volt negative pulse which is used to set a large number of flip-flops. The input to the module, applied to terminal 4, is a 6-volt positive rectangular pulse with a duration of approximately 34 microseconds. The module contains two transistor circuits. One of these, Q1, is a PNP transistor which is normally conducting. The other, Q2, is an NPN transistor which is normally cut off. The input pulse is applied through capacitor C2 and diode CR1 to the base of Q1, cutting the transistor off. (Q2 is held in this state by the charge on C1.) This causes the output voltage at terminal 1 to drop from +6 volts to 0 volts. The input pulse is also applied to a time delay network consisting of L1 and L2, R3 and R4, and C3. This network provides a brief time delay before the pulse is applied to the base of Q2. The application of the positive input pulse causes Q2 to conduct, lowering the output voltage to approximately −10 volts. Q2 conducts for the duration of the input pulse. When this pulse is terminated transistor Q2 returns to cutoff. The output now rises to 0 VDC and remains at this value until C1 has discharged sufficiently for Q1 to begin conducting. When Q1 conducts the output voltage returns to its quiescent value of approximately 46 VDC.

4216. Digital to Analog Module 1 Through 3.—These modules are described in paragraph 4404*l* and *m*.

4217. Loop Input.—This module is described in paragraph 4402*c*.

4218. Special One-Shot.—This module is described in paragraph 4402*e*(3).

4219. Noise Generator, Gate and Amplifier.—These modules are described in paragraph 4402*e*.

4300—FUNCTIONAL OPERATION

4301. General.—The following discussion describes, at a block diagram level, the functional operation of the KW-7. This functional description is divided into two parts: Extensor and Control, and Key Generator. In this manner it is possible to observe the functional operation of the KW-7 logically. Signals enter the Extensor and Control and are coupled to the Key Generator.

a. *Block Diagram Symbols.*—Before any discussion of the block diagrams can be attempted, it is necessary to explain some of the symbols and abbreviations used on the individual diagrams. Each functional section, contained within both the Extensor and Control and the Key Generator, is identified by individual titles. Within each functional section are several blocks which define those circuits composing the functional section. In this manner it is possible to relate the entire functional section to individual circuit operation. Inputs and outputs are given short titles wherever possible. All outputs which are used by a functional section not on the block diagram being discussed, are referenced to the applicable diagram (e.g., if an output, located on fig. 4-39 goes to a functional section on fig. 4-40 then the output is so designated).

b. *Block Diagrams Abbreviations.*—In addition to the drawing conventions just described, some discussion of signal names and abbreviations is necessary before the individual block diagrams can be properly used. Most signal names are simply abbreviations of the name of the circuit or functional unit in which the signal originates. Thus, the output bit rate characters, generated by the output bit rate and character counter, are identified as OBR (Output Bit Rate). In the case where a circuit generates two opposite outputs (one high and the other low), the outputs are designated X and $\overline{X}$ (not X). The Not sign ($\overline{X}$) is assigned to the signal line that is set low (a ZERO) when the equipment is operating properly. The X designation applied to the other line indicates that the signal on that line is set high (a ONE). Although these level designations are arbitrary, they are useful in indicating the starting condition of each signal.

(1) In the case of a functional unit containing several identical circuits with outputs taken from one or more of these circuits, the circuits themselves are numbered sequentially and the signals from these circuits carry the same number. For example, Output Bit Rate and Character Counter contains eight identical circuits (flip-flops) which are numbered sequentially from 0 to 7. An output signal is taken from each circuit, specifically from the circuit output side that is presently being employed by the system. These signals are therefore identified as OC (output counter) 0 through 7 (OC0 through OC7).

(2) Whenever an output, generated by a functional section, is fed to another functional section located on the same figure, it will not necessarily be referenced. In the cases where the output and input are located in close proximity it was possible to draw connecting lines, in the cases where this was not possible, it is left to the ability of the reader to locate the proper input in relation to an output from another functional section.

4302. Theory of Operation, Functional Units.—The following paragraphs describe the operation of the individual functional units which comprise the KW-7.

4303. Extensor and Control.—The extensor and control processes and retimes the input information before it is applied to the key generator. Figure 4-39 illustrates the extensor and control as broken down into the following functional blocks.

Time Standard	Receive Phasing
Clock Pulse Generating	Indicator Control

Input Counter	Indicator
Output Counter	Normal Generating
Data Input	Send Phasing
Phase Correction	Break Generating
Data Extensing	Audible Alarm
Output Control	S.T. Power Set, Power Set, and Set Generating
Send Normal	Randomizer and Alarm
Receive Normal	

In this section, the blocks are discussed only in terms of their purpose and major input-output signals, in a later section, the operation of each block is discussed in detail.

a. *Time Standard Circuit.*—The time standard furnishes a stable 1 MC signal which is the source for the timing signals required in the KW-7.

b. *Clock Pulse Generating Circuit.*—The clock pulse generating circuit reduces the frequency of the 1 MC time standard to a frequency which is compatible with teletypewriter operation The clock output is manually set to one of three frequencies by the WPM (words per minute) selector switch.

c. *Input Counter Circuit.*—The input counter counts down the clock frequency in order to generate the input bit rate (IBR) and the input character rate (IC7) timing pulses. These pulses are used primarily to sample (examine) the incoming information at specified times.

d. *Output Counter Circuit.*—The output counter counts down the clock frequency in order to generate the following timing pulses: OBR (output bit rate) CTRP (output character rate), P, Pd, $\overline{\text{START}}$, OBR·BIT 1, START, and STOP. P is a 34 microsecond pulse which is derived from CTRP and thus occurs at the output character rate. Pd is identical to P, but delayed 34 microseconds. $\overline{\text{START}}$ and OBR, in conjunction with OBR·BIT 1, are used to compare locally-generated timing with the timing of the incoming data so that the local KW-7, if in receive mode, can be synchronized to the sending KW-7. START and STOP are used during send operation to ensure that the key generator will not encipher the start and stop baud of each character.

e. *Data Input Circuit.*—The data input circuit accepts data from a local loop teletypewriter (send mode) or from the line (receive mode) and gates it to the phase correction and data extensing circuits. ABIN will consist of locally-generated loop information during send, and line information during receive.

f. *Phase Correction Circuit.*—The phase correction circuit is used during receive to compare the locally generated timing with the timing of the input data. If the two are out of phase, the phase correction circuit shifts the local clock frequency until the local timing matches the input data timing.

g. *Data Extensing Circuit.*—The data extensing circuit momentarily stores input data ABIN until the key generator portion of the KW-7 is ready to accept it. The data extensing circuit consists of three shift registers, SRA, SRB, and SRX. Operation of these shift registers during send differs from the operation during receive, as described in the following paragraphs.

(1) *Send operation.*—During send operation, the data extensing circuit converts 7.42 baud real-time asynchronous ABIN loop data (from the local TTY) into 7.0 baud network-time synchronous E data. The synchronous E data is then fed to the key generator where it is combined with key to form cipher.

(a) Data extensing is accomplished as follows. The first ABIN character is stored in SRA, sequentially, one bit at a time, with a total time of 7.42 bauds required to complete storage. At Pd time this character is transferred to SRX and then

immediately shifted out of SRX at the OBR rate. Since there is no fixed time relationship between the loading of SRA and the occurrence of Pd, Pd can occur immediately after SRA is loaded, or it can occur up to a full character time later.

(b) Similarly, the second ABIN character is stored in SRB, transferred to SRX at Pd time, and immediately shifted out of SRX at OBR rate.

(c) The third ABIN character goes into SRA, from SRA into SRX, and from SRX to the key generator. The fourth character goes into SRB, and so on. Thus all odd-numbered characters go to SRA, and all even-numbered characters into SRB.

(d) It should be noted that the SRX read-out rate (7.0 bauds per character) is greater than the data read-in rate (7.42 bauds per character). If input data is arriving continuously with no time lapse between characters, the SRA-to-SRX or SRB-to-SRX transfer time will advance 0.42 baud per character, so that after a certain time the transfer will be attempted before SRA or SRB is fully loaded. The send normal circuit detects when this condition is about to occur, by examining the AO and BO control signals which are used to determine whether data is available in SRA or SRB for transfer to SRX. The AO and BO signals combine in a MOD 2 adder to generate to an SNA signal. The SNA signal generates CSM signal to inhibit the transfer until the character is fully loaded into SRA or SRB. The SNA signal also inhibits the auto key generator in the Key Generator circuit via the output control so that pure key is not transmitted in the absence of data; during this interval the KW-7 transmits a speed differential lockup (all mark signal). Normal operation resumes as soon as the character has been fully loaded into SRA or SRB.

(e) During send, the input counter is synchronized once per character by the stop-start transition of the character to the loop input data from the local teletypewriter. The output of the counter, IBR and IC7 pulses are used to sample the input data. In the absence of local copy, the input counter changes from MOD 6 to MOD 8 to permit detection of phasing characters coming from another KW-7.

(2) *Receive Operation.*—Receive (Cipher or Plain Synchronous) operation differs from send operation in two respects.

(a) First, retiming of the input is not necessary. This is because the input data is now occurring at 7.0 bauds per character, since it is coming from another KW-7 instead of a local loop teletypewriter. Second, SRA is used only to check the validity of the incoming data, (validity is defined as at least one ZERO information bit per character). The contents of SRA are examined at P time, and reset to ZERO 34 microseconds later at Pd time. The data itself is routed continuously through SRB to SRX.

(b) In receive plain asynchronous operation, a distant teletypewriter sends 7.42 baud asynchronous data to the line input of the KW-7 (data input). The input counter counts in MOD 6 and is reset by a MISS pulse each character time. The 7.42 baud asynchronous data bypasses the extensor via the gated loop in circuit (data input). From there the 7.42 data is routed through the loop output circuit to the local page printer. The input counter, which has been synchronized by the input data is used to sample the data as it passes through the output register.

h. Output Control Circuit.—The output control circuit monitors the shift and transfer controls of the SRA and SRB registers during send operation. If information is not available, the output control generates an M signal which disables the auto key generator and line output circuits, preventing the transmission of pure key in the absence of text. In receive operation, the output control develops a LOCO (loop output control) signal which controls the flow of information to the local page printer. The LOCO pulse is one baud time in duration, and permits the receivers local page printer to start in letter shift. The second LOCO

pulse (and all others following) is produced indirectly as a result of the M signal and is one character time in duration.

i. Send Normal Circuit.—The send normal circuit examines LOOP INPUT data in order to determine the counting mode of the input counter, and also controls the transfer of loop information into the data extensing circuit. During phasing, the input counter is operating in MOD 8, that is, it divides the input bit rate (IBR) by 8. This is necessary because the phasing characters contain 8 bits in order to be distinguishable from information characters which contain 7 bits (start bit, 5 information bits, and stop bit). During indicator and normal, the send normal circuit forces the input counter to operate MOD 6, only if active data transmission exists, or in plain asynchronous mode. The information characters at these times consist of 7 bits. Operation of the send normal circuit is such that when the KW-7 is not actively sending, it is examining its own line input for the presence of MOD 8 phasing characters, which are an indication that another KW-7 has initiated phasing and intends to begin transmitting. In addition, the send normal circuit generates a SHIFT A GATE which tells the receive normal circuit when to shift SRA. When SRA is loaded with one character, a SHIFT A signal is generated, to transfer the contents of SRA to SRX. SRX is shifted out at an OBR rate. At the same time a SHIFT B gate enables shifting of the next character into SRB at an IBR rate. When SRX has been shifted out, a TRANSFER B signal enables the contents of SRB to transfer to SRX for output shifting.

j. Receive Normal Circuit.—The receive normal circuit generates TRANSFER B and SHIFT A commands for the data entensing circuit. TRANSFER B occurs at Pd rate during receive and is generated when the KW-7 enters the normal phase of receive operation. In receive, SHIFT A occurs only when ABIN is ZERO, that is, only ZEROS are shifted into SRA; the SHIFT A repetition rate at this time is OBR. In send, SHIFT A occurs at the IBR rate upon command of the SHIFT A GATE from send normal.

k. Receive Phasing Circuit.—During receive phasing, the input character counter is operating MOD 8 in order to generate an IC7 signal with a period equal in length to an 8 bit character. These MOD 8 IC7 signals are used by the receive normal logic to sample the incoming 8 bit LINE IN phasing characters. After four consecutive 8 bit LINE IN phasing characters have been detected and counted, the receive normal circuit generates a pulse which tells the indicator control circuit that phasing has been successfully completed.

l. Indicator Control Circuit.—The indicator control circuit detects when receive phasing has been successfully completed, and generates a LOCK IN GATE (LIG) which initiates the indicator phase of receive operation. The LOCK IN GATE triggers the send phasing circuit and resets the break generating circuit (if necessary). The LOCK IN GATE also generates a SET pulse, which resets the KW-7 circuits.

m. Indicator Circuit.—The indicator circuit is used during indicator phase of operation to establish a random starting point for the Fibonacci register of the key generator. During the indicator phase of operation, a random sequence of blank and letter characters are being shifted out of the SRX shift register. The duration of the indicator phase is determined by the time required for the occurrence of 12 blank characters followed by 12 letter characters; normally this period will vary from about 7 seconds to 15 seconds. The blank and letter character detecting circuits examine the contents of stage SRX5 of shift register SRX once during each character period. During send indicator operation, stage SRA2 in the SRA register monitors the random signal generator (M2B). Stage SRA2 is set to ZERO as soon as a ONE is sensed in the M2B random bit stream. SRA2 then enables a $\overline{\text{CLX}}$ signal to force a blank character (all ZEROES) into the SRX register. Stage SRX5 of the SRX register then enables the blank character detect circuit which steps the indicator counter by one count for every blank character detected. After counting 12 ZEROES (re-

presenting 12 separate blank characters), the indicator counter disables the blanks detector, and enables the letters detector. The letters detector now examines SRX5 and inserts one count for each letter character. The SRX register, under control of OBR is loaded with all ONES (letters character) when SRA2 does not sense a ZERO. When 12 letters have been counted, the indicator counter generates a signal which tells the normal generator that the indicator phase of operation is completed. During normal phase of operation, the indicator counter is used as a BREAK recognition circuit. However, if a line break occurs, the BREAK detector sees a low line condition (space) at the line input. The indicator counter begins counting blanks and, if the break condition has not been relieved by the time the counter reaches 12, it generates an INDC signal which triggers the break generator, stopping the KW-7. During receive indicator operation, the SRA register shifts ZEROS as the random message indicator characters are received on the line input circuit. As soon as a ZERO is shifted into stage SRA2 the blank character detect circuit is enabled in the same manner just described for send indicator. (The process of sampling SRA2 for presence of a ZERO during receive indicator operation is called voting.) Thus, the main difference between send indicator and receive indicator operation lies in the source of random message information and in the method of entering ZEROS into SRA2.

n. Normal Generating Circuit.—The normal generating circuit generates the NORMAL signal which establishes the conditions required to carry out the normal phase of operation.

o. Send Phasing Circuit.—The send phasing circuit generates the SEND signals which establish the conditions required for send operation. Eight bit phasing information is transmitted by the KW-7 as long as the SEND switch is kept depressed. When the SEND switch is released, the KW-7 goes into indicator phase. If another KW-7 initiates phasing while the local KW-7 is in the send mode, a LOCK IN GATE will reset the send phasing circuit, taking the local unit out of send and placing it in receive.

p. Break Generating Circuit.—The break generating circuit gives the receiving operator a visible and audible indication of a line break, and allows him to signal the sending operator in case of malfunction. The break generating circuit consists of the break generator and the break switches. The application of the ST POWER SET signal resets the break generator, allowing the KW-7 to go through phasing and indictor and begin normal operation. If text is being satisfactorily received, the indicator counter is continually being reset and is unable to generate the INDC signal. If a break occurs, the indicator counter counts until 12 successive break characters (all spaces) have been received, and then generates an INDC signal which triggers the break generator. The break generator disables the receiving KW-7 and energizes the BREAK indictor lamp and audible alarm. Three manually operated switches are provided in the break generating circuit. These are the BREAK switch, the BREAK RESTORE switch and the BREAK FUNCTION switch. The BREAK switch allows the receiving KW-7 operator to generate a BRK and a $\overline{\text{BRK}}$ signal when he observes garbled text or when he wishes to assume command of the network. The BRK signal disables the line output, causing the local KW-7 to generate a break signal which stops the sending KW-7 and triggers a break indication in all other receiving units in the network. The $\overline{\text{BRK}}$ signal resets the local indicator counter. In order to relieve the break condition in his own unit the operator must activate the BREAK RESTORE switch. The BREAK RESTORE switch allows the KW-7 operator to end the break condition so that transmission of messages can resume (assume, of course, that the transmission line has not actually been broken). Pressing the BREAK RESTORE switch relieves the local break conditions. The BREAK FUNCTION switch disables the break indication circuits when radio transmission is used. This is necessary to eliminate the breaks which may otherwise result from signal fadeout.

q. Audible Alarm Circuit.—The audible alarm informs the operator when a alarm condition has occured within the KW-7. The alarm will sound when the BREAK, BUZ 1 or PLAIN

signals enable the alarm. The BREAK signal will be an enable signal when the line is open. The BUZ 1 signal will be an enable signal when an alarm condition causes the line output control relay to become deenergized. The PLAIN signal will be an enable signal during the plain mode of operation, so that an audible warning is always sounded (when the alarm switch is in the ON position) when in the PLAIN MODE.

r. *S.T. Power Set, Power Set, and Set Generating Circuit.*—The S.T. power set, power set, and set generating circuit produces various set signals which are used to establish prerequisite conditions throughout the system. These signals are triggered in any one of seven ways as follows:

(1) Approximately 200 milliseconds after closure of the POWER switch
(2) When the PCR switch is switched from cipher to plain
(3) When the PCR switch is switched from plain to cipher
(4) When a break condition is detected by the break generating circuit
(5) During testing when the ALARM TEST switch is set to any position except OFF
(6) During receive when the KW-7 completes phasing as indicated by a LOCK IN GATE
(7) When entering the send mode of operation

s. *Randomizer and Alarm Circuit.*—The primary function of the randomizer is to produce, during the indicator mode, the M2B signal. This signal is a fully random stream of ONES and ZEROS which is applied to stage 2 of SRA in the extensor and control. The random triggering of SRA has the end result of assuring that the key generation starts at a random point in the Fibonacci cycle. An alarm circuit provides a warning if the randomizer is not functioning properly.

4304. Key Generator.—The function of the Key Generator is to encipher messages during Send Cipher operation and decipher messages during Receive Cipher operation. Figure 4-40 illustrates the functional block diagram of the Key Generator circuits.

a. *Primary Key Generating Circuit.*—The primary key generating circuit produces the five primary key timing signals. The primary key generating circuit consists of the Fibonacci shift register, the permuter patchboard, and combiners $\overline{p}$ through $\overline{t}$. The Fibonacci shift register is a conventional 39 stage shift register. When triggered by F DRIVE pulses, a pattern of ONEs and ZEROs are shifted through the register. The permuter connects the outputs of 30 of the first 31 of these stages to combiners $\overline{p}$ through $\overline{t}$ via permuter patch cords. The permuter is a pluggable device, which provides a method of selecting which stages of the Fibonacci shift register are to be connected to a particular combiner. In each combiner the outputs selected from up to six stages are combined to produce one of the five key timing signals ($\overline{p}$, $\overline{q}$, $\overline{r}$, $\overline{s}$, and $\overline{t}$). The $\overline{s}$ combiner also has provisions for a PLAIN signal input which stops the shifting action of the Fibonacci shift register when the KW-7 is operating in the plain mode. The outputs from combiners $\overline{s}$ and $\overline{t}$ are applied to the drive pulse generating and pulse deletion circuit. The outputs from combiners $\overline{p}$ through $\overline{r}$ are applied to the secondary key generating circuit.

b. *Drive Pulse Generating and Pulse Deletion Circuits.*—The drive pulse generating and pulse deletion circuits produce the drive pulses used to trigger the Fibonacci shift register and provides a method of stopping the Fibonacci cycle for one step by deleting a drive pulse when certain conditions exist in the key generator.

(1) *Drive pulse generating circuit.*—The drive pulse generating circuit produces the KG DRIVE pulses at the OBR rate if the KW-7 is in either the indicator or normal phase of operation and is not in the plain mode. It consists of the drive pulse generator and the drive pulse gate. The $\overline{I\&N}$ signal applied to the drive pulse generator is an enable signal during all operations except the phasing mode. During the indicator and normal phases of operation (cipher operation) the drive pulse generator produces KG

DRIVE pulses each time th OBR output is an enable pulse. The KG DRIVE pulses are gated through the drive pulse gate causing the F DRIVE pulses to trigger the Fibonacci shift register.

(2) *Pulse deletion circuit.*—The pulse deletion circuit stops the Fibonacci cycle for one step by occasionally deleting an F DRIVE pulse. The circuit is so arranged that two successive pulses can not be deleted. The pulse deletion circuit consists of the 1 to 0 detector and the $\overline{s}\cdot\overline{t}$ adder. During normal cipher operation the sum of the $\overline{s}\cdot\overline{t}$ adder allows the 1 to 0 detector to send an enabling SPECIAL POINT U signal to the drive pulse gate. This, in conjunction with the KG DRIVE pulses from the drive pulse generator, allows the F DRIVE pulses to be fed to the Fibonacci shift register. The only time the F DRIVE pulses are inhibited is when the sum of the $\overline{s}\cdot\overline{t}$ adder goes from a logical ONE to a logical ZERO. This inhibits the drive pulse gate and deletes only the subsequent F DRIVE pulse from the Fibonacci shift register. Also, the application of the PLAIN signal places an inhibit on the input of the $\overline{s}$ combiner and prevents the F DRIVE pulses from shifting the Fibonacci shift register.

c. *Secondary Key Generating Circuit.*—The secondary key generating circuit combines the outputs from the primary key generating circuit to produce two secondary key timing pulses: X and W. The secondary key generating circuit consists of a $\overline{q}\cdot\overline{r}$ adder and accumulator, a Y delay, a P delay, a Y·P adder and a Y·S adder.

(1) *$\overline{q}\cdot\overline{r}$ adder.*—The $\overline{q}\cdot\overline{r}$ adder is a re-entry adder which adds the outputs of the $\overline{q}$ and $\overline{r}$ combiners to produce the $\overline{T}$ signal. The output of the adder is a ZERO when the $\overline{q}\cdot\overline{r}$ signals are of opposite polarity.

(2) *Accumulator.*—The accumulator is a gated flip-flop which will change its state each time it is pulsed by a KG DRIVE pulse but only if $\overline{T}$ is a ZERO.

(3) *Y delay.*—The Y delay generates the same output as the accumulator, but is delayed one baud in time (YN–1).

(4) *P delay.*—The P delay delays the $\overline{p}$ output from the primary key generating circuit for one baud time. Operation of the P delay is essentially the same as the Y delay. It's output is a PN signal.

(5) *Y·P adder.*—The Y·P adder is an adder which adds the YN–1 and outputs of the PN signals to produce the first secondary key signal X.

(6) *Y·S adder.*—The Y·S adder is an adder which adds the YN–1 and S signals to produce the second secondary key signal W.

d. *Auto Key Circuit.*—The auto key circuit increases the key depth by generating a modified key signal which is a function both of the previously transmitted cipher signal (Z1) and the secondary key signal X. This modified key signal is called the auto key signal or the $\overline{V}$ signal. The auto key circuit consists of the E gate, the Z1 gate, the X·Z adder, the auto key register, the auto key drive inhibiter, the auto key drive generator and the $\overline{V}$ combiner.

(1) *E and Z1 gates.*—The E and the Z1 gates control the flow of information into the X·Z adder. In the receive normal mode, both the NORMAL 3 and the SEND 2 signals are enabled which causes the Z1 gate to become disabled (inhibited) and the E gate to become enabled. The input to the X·Z adder is then the $\overline{E}$ signal. During send normal operation, the $\overline{E}$ gate is disabled by the SEND 2 signal, which is an inhibit level at this time, causing the Z1 gate to be enabled. The input to the X·Z adder is now $\overline{Z1}$ signal.

(2) *X·Z adder.*—The X·Z adder generates an L signal by performing a MOD 2 addition on the X key stream and the output of either the E or Z1 gate. This L signal is applied to the auto key register.

(3) *Auto key register.*—The auto key register is a conventional five stage shift register. When the register is triggered by the A KEY DRIVE pulses the L signal is shifted

through the register. Each output from the shift register (Q) forms one input to the $\overline{V}$ combiner.

(4) *Auto key drive inhibitor.*—The auto key drive inhibitor inhibits the auto key drive generator at all times except during the time of the five information bits of each character. The $\overline{\text{M GATED}}$ signal is enabled whenever a character is being received or transmitted. The START signal is an enable signal except during the start bit of each character. The STOP signal is an enable signal except during the stop bit of each character. Therefore, the only time the output from the auto key drive inhibitor enables the auto key drive generator is when the five information bits of a character are being transmitted or received.

(5) *Auto key drive generator.*—The auto key drive generator generates the A KEY DRIVE pulses which drive the auto key register. These pulses, having the same repetition rate as the KG DRIVE pulses, occur only when the input is enabled by the output from the auto key drive inhibitor.

(6) *$\overline{V}$ combiner.*—The $\overline{V}$ combiner, combines the X signal, from the secondary key generating logic, with the Q outputs of the auto key register, producing a signal called $\overline{V}$.

e. Final Key Generating and Key Adding Circuit.—The final key generating and key adding logic performs two functions: it generates the final key signal (K), and it adds this signal to plain text to produce cipher, or to cipher to produce plain text. The final key generating and key adding circuit consists of the final key generator (W·V adder), key adder and the start-stop gate.

(1) *Final key generator.*—The final key generator is the W·V adder which performs a MOD 2 addition of the secondary key signal (W) from the secondary key circuit, and the $\overline{V}$ auto key stream from the auto key logic. This adder produces the final key signal (K) which is applied to the key adder; two additional outputs, $\overline{W}$ and V, are applied to the alarm logic.

(2) *Key adder.*—The key adder performs a MOD 2 addition of the final key signal (K) and the E output from the data extensing circuit. It should be remembered that E will be plain text during send operation, and cipher during receive operation. Therefore, during send, the MOD 2 addition of E and K gives cipher, while during receive the same process gives plain text. The output from the key adder, Z1 is applied to the start-stop gate, to the alarm key adder, and to the Z1 gate.

(3) *Start-stop gate.*—The start-stop gate assures that the start and stop bauds of a character will be transmitted in plain text during both plain and cipher operations. This is required because the start and stop bauds are required to synchronize the receiving KW-7. The start-stop gate is inhibited during the reception of the START and STOP inputs; at all other times the Z1 signal is inverted and passed through the gate to the line Z2 gate and to the loop gate, except during the start and stop bauds of a character. The Z2 signal will be plain text if the KW-7 is receiving and cipher if transmitting. The Z3 signal is fed to the Z2 gate and to the feedback Z gate.

f. Loop Output Circuit.—The loop output gates the plain message (whether in Plain or Cipher mode) to the loop output circuit during both send and receive operations. Major circuits in the logic are the loop Z2 gate, the gated loop in gate, the bit rate gate, and the loop output register.

(1) *Loop Z2 gate.*—The loop Z2 gate produces the $\overline{Z2}$ signal during the receive normal operation, but only if the text is valid (the validity is determined by the presence of the LOCO signal). The enable signals for the loop Z2 gate are the SEND 1, $\overline{\text{NORMAL 3}}$, LOCO ($\overline{\text{M Gated}}$), and Z2.

(2) *Gated loop-in gate.*—The gated loop-in gate passes the GATED LOOP signal during send operation and receive plain asynchronous. The gated loop-in gate is inhibited when an ALARM signal is generated.

(3) *Bit rate gate.*—The bit rate gate allows the loop output register to be triggered by IBR signals during send operation, or by OBR1 pulses during receive operation. In the send operation, $\overline{\text{SEND 1}}$ is an enable while SEND 1 is an inhibit. Under these conditions, the outputs invert the IBR pulses. In the receive operation the $\overline{\text{SEND 1}}$ is an inhibit input signal, while SEND 1 is an enable input. The bit rate OBR1 is now inverted at the output. The output from the bit rate gate is the LOOP OUT DRIVE pulse.

(4) *Loop output register.*—The loop output registers supplies the LOOP OUT information to the loop output circuit. The state of this register is controlled by LOOP OUT signal supplied by the gated loop in gate. The LOOP OUT DRIVE pulse enables the loop out register. This pulse occurs one-half baud after the start of each baud period. This insures that the loop out signal is not fed to the output circuit when it is changing state.

g. Line Output Circuit.—The line output circuit gates the transmitted message to the line output circuit. This circuit consists of the line E gate, line Z2 gate, the line output register and the output control relay gate.

(1) *Line E gate.*—The line E gate supplies phasing and indicator information (E) to the line output register during the phasing and indicator or message information during the normal ($S \cdot \overline{N}$) phase of the send operation.

(2) *Line Z2 gate.*—The line Z2 gate passes data ($\overline{Z2}$) during the send normal operation, but only if the message is valid ($\overline{M}$); that is, a transmission is being made. The enable signals for the line Z2 gate are the Z2, $\overline{\text{SEND 3}}$, $\overline{\text{NORMAL 3}}$, and $\overline{M}$.

(3) *Line output register and control.*—The line output register acts as a buffer between the key generator logic and the line. This register supplies LINE-OUT information at a DBR2 rate. The line output register control provides a means of inhibiting the output of the line-output circuit. If a break condition occurs the BRK signal will inhibit the line output register gating and prevent line-out information from being sent out on the line.

(4) *Output control relay gate.*—The output control relay gate controls a relay in the line output register control to prevent inadvertant transmission of plain text while operating in the cipher mode. The ALARM signal and the $\overline{\text{SEND}}$ signal causes the relay to prevent transmission during receive operation or when there is an equipment malfunction causing an alarm. The PLAIN signal enables the relay throughout the plain mode of operation.

h. The Fibonacci Feedback Circuit.—The Fibonacci feedback circuit is used to extend the Fibonacci cycle. The Fibonacci feedback circuit consists of the feedback Z1 gate, the 35 gate and the Fibonacci feedback adder.

(1) *Feedback 35 and Z gate.*—The 35 and Z gates, control the $\overline{35}$ or $\overline{Z3}$ input to the Fibonacci feedback adder. During phasing and indicator, the NORMAL 2 signal is enabled while the $\overline{\text{NORMAL 3}}$ is inhibited. The output of the feedback Z gate is a $\overline{Z3}$ signal, which is fed to the Fibonacci feedback adder. During normal operation the $\overline{\text{NORMAL 2}}$ signal is inhibited and the NORMAL 3 is enabled. The output of the 35 feedback gate is $\overline{35}$, which is fed to the Fibonacci feedback adder.

(2) *Fibonacci feedback adder.*—The Fibonacci feedback adder generates the A signal which is the result of a MOD 2 addition of the 39th Fibonacci stage output, and either the $\overline{35}$ or $\overline{Z3}$ signal. During phasing and indicator operation, the A signal is the MOD 2 sum of the 39 and the $\overline{Z3}$ signals, while during normal operation the A signal is the MOD 2 sum of the 39 and the $\overline{35}$ signals. In either case, the A signal determines the pattern of ONE's and ZERO's which will be shifted through the Fibonacci shift register.

i. Fibonacci, I&N and Loop Activity Alarm Circuit.—The Fibonacci, I&N and Loop Activity alarm circuit generates an alarm indication if any of the following conditions occur: 1)

The W stream does not undergo at least one ZERO to ONE signal transition during a given eight character period, 2) The 39 stream does not undergo a transition from ZERO to ONE or from ONE to ZERO during a given eight character period, 3) The Fibonacci begins generating an alternating output (101010), 4) The I&N flip-flop is not set to ONE during the normal mode of operation, or 5) Loop information is generated during the phasing or indicator phase of send operation.

(1) *Fibonacci alarm.*—The Fibonacci alarm consists of the Fibonacci alarm generator (P stream monitor), the W stream monitor circuit and the Fibonacci alternation detector.

(a) *Fibonacci alarm generator.*—The Fibonacci alarm generator will generate a Fibonacci alarm signal if there is no activity in the Fibonacci shift register for an 8-character period.

(b) *The W stream monitor circuit.*—The W stream monitor circuit consists of the CTRP gate, the ÷ 8 counter and the W stream monitor. The I&N signal enables the CTRP gate during indicator and normal phases of operation. The PLAIN signal is an enable if the KW-7 is in the cipher mode. Therefore, the CTRP gate produces an output ($\overline{\text{CTRP}}$) signal at the CTRP rate. This signal is fed to the ÷ 8 counter where its repetition rate is divided by eight to give the ASP (alarm sampling pulse signal). The ASP and the W signals are fed to the W stream monitor. If the W stream is being generated properly, a ZERO to ONE transition will occur at least once between every two ASP pulses. If the W stream is not being generated properly the W ALARM signal will be generated and will trigger the alarm generator.

(c) *Fibonacci alternation detector.*—The Fibonacci alternation detector causes an alarm indication if the Fibonacci shift register produces an alternating pattern (constant A signal) for an eight character period. If the Fibonacci is operating properly, some activity will occur in the A signal before the generation of the ASP signal so that the A signal, in conjunction with the KG signal, enables the Fibonacci alternation detector. If, however, no A signal activity occurs between two ASP signals the second ASP signal will trigger the Fibonacci alternation detector and cause an alarm indication to be generated.

(2) *I&N alarm detector.*—The I&N alarm detector provides an alarm indicator if the I&N flip-flop is not properly set during normal operation. There are two inputs to the detector: $\overline{\text{NORMAL 2}}$ and I&N. During the normal mode of operation, $\overline{\text{NORMAL 2}}$ enables the detector. If the I&N flip-flop is operating properly I&N inhibits the detector and no output is produced. However, if a malfunction occurs, I&N is an enable signal and the detector produces a signal which triggers the alarm generator.

(3) *Loop activity detector.*—The loop activity detector causes an alarm indication to be generated if loop information is generated during phasing or indicator. The NORMAL 2 signal is an enable signal during phasing and indicator, the $\overline{\text{LINE-IN}}$ signal is an enable if there is no line information and the ABIN Signal is an enable if either line or loop information is available. Therefore, if the KW-7 is in phasing or indicator, if line information is absent, and if loop information is present, all three inputs will be enabled, causing an alarm indicator to be generated.

j. Fibonacci Feedback Alarm Circuit.—The Fibonacci feedback alarm circuit checks the operation of the Fibonacci feedback circuit by adding A and the quantities that form A in a MOD 2 adder-comparator circuit in such a way that an alarm will be triggered if either the feedback or checking circuit malfunction. The Fibonacci feedback alarm circuit consists of the Z2 gate, the 35 gate, the 39-A adder and the Fibonacci feedback comparator.

(1) *Z2 gate and 35 gate.*—The Z2 gate and the 35 gate have a common output ($\overline{\text{Z2}}$ or $\overline{35}$). At any given time, either the Z2 gate or the 35 gate will be enabled. The Z2 gate is enabled by a NORMAL 2 signal during indicator. The 35 gate is enabled by a $\overline{\text{NORMAL 2}}$ signal during normal operation.

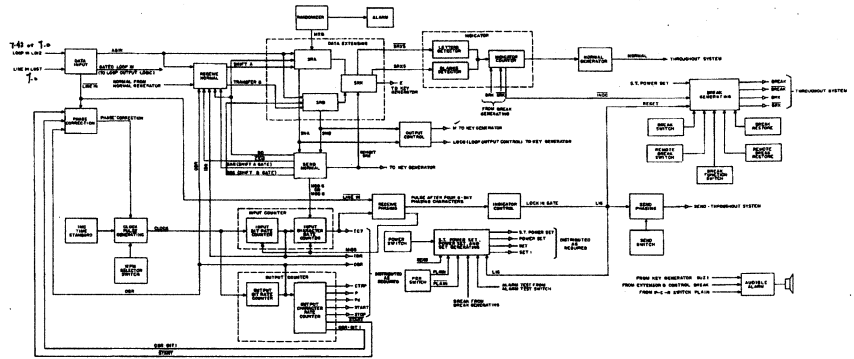


Figure 4-20.—Extensor and Control, Overall Block Diagram.

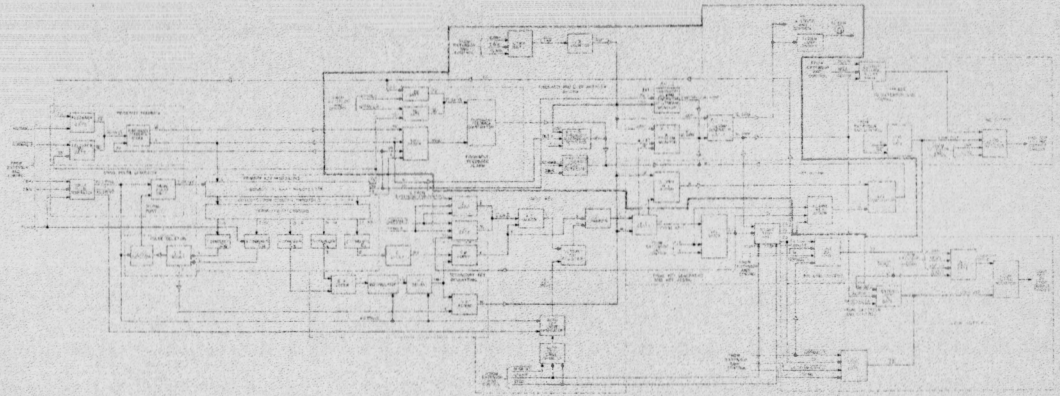


Figure 4-40. Key Generator, Overall Block Diagram.

(2) *39·A adder.*—The 39·A adder performs a MOD 2 addition of the 39 signal from the Fibonacci, and the A signal which is fed back to the first state of the Fibonacci shift register. The output from the 39·A adder (39+A) is fed directly to the Fibonacci feedback comparator.

(3) *Fibonacci feedback comparator.*—The Fibonacci feedback comparator performs re-entry addition of the 39·A signal and the $\overline{Z2}$ or $\overline{35}$ signal. As long as the Fibonacci feedback is being generated properly, the output of the feedback comparator is inhibited. However, if a malfunction occurs in the generation of the Fibonacci feedback, the Fibonacci feedback comparator will be enabled, causing the FIBONACCI FEEDBACK ALARM signal to be generated.

k. Key Alarm Circuit.—The key alarm circuit checks the formation of the key signal. The circuit consists of the alarm W·V adder, the alarm key adder, and the key comparator. To fully understand the operation of the key alarm circuit it should be noted that the final key was obtained by MOD 2 adding the W and V streams from the secondary key generator.

(1) *Alarm W·V and alarm key adders.*—The alarm key adder performs a MOD 2 addition of cipher (Z1) and plain text (E) to produce the K signal, while the alarm W·V adder performs a MOD 2 addition of V and W to produce K. The outputs of these two adders must always be equal if the KW-7 is operating properly. If outputs are not equal an alarm indication is generated.

(2) *Key comparator.*—The key comparator performs a MOD 2 addition of the output from the alarm key adder and the alarm W·V adder. As long as these two signals (K) are identical, signifying correct circuit operation, the output of the key comparator (KEY ALARM) will be a ZERO. If a malfunction occurs, the signals will no longer be identical, and the comparator will generate an alarm indication.

4305. Remote Control Unit Operation (fig. 4-41).—The KW-7 is equipped with a remote control unit which may be employed to fully operate the KW-7 from a remote location. The Remote Control Unit provides a parallel set of signal inputs and outputs and control and indicator functions. An input from a teletypewriter keyboard or TD to the remote control unit is transmitted to the KW-7 via a remote cable. The length of this cable may be a maximum of 500 feet. The loop-output information is transmitted from the KW-7 loop-out circuit through the remote cable to the remote control unit where it is in turn routed to a page printer. The internal operation of the KW-7 is identical to that previously described and need not be discussed further.

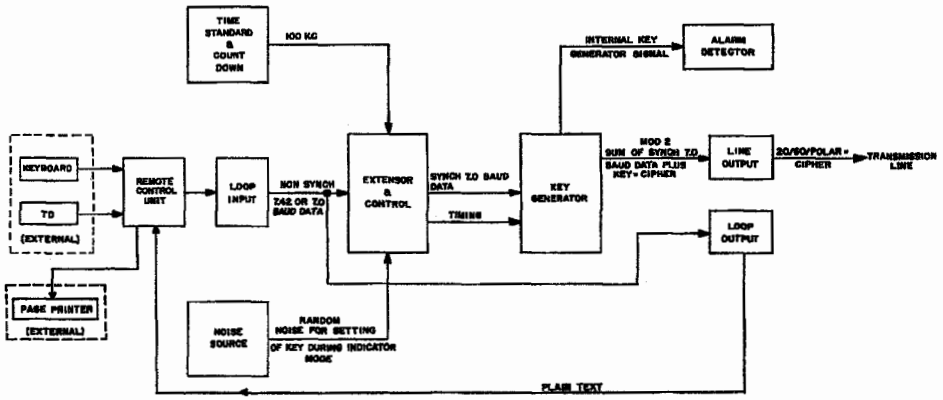


Figure 4-41.—Remote Control Unit Operation, Block Diagram.

4306. Two-Wire Loop Adapter Unit Operation (figs. 4-42 and 4-43).—For special field applications it is necessary that the KW-7 low current level four-wire Loop-Input/Output system be converted to a high current level two-wire system. It is also necessary that the high-level (20/60 milliampere) teletypewriter signals be converted to low-level signals for use with the KW-7 Loop-Input circuit. This is accomplished by the two-wire loop adapter unit. When the two-wire loop adapter unit is employed it is necessary to place the LOOP ALLOW/ LOOP INHIBIT switch, located in the top of the KW-7, in the INHIBIT position. The teletypewriters have the keyboard and page printer in series so that when a message is sent on the keyboard it is automatically printed out on page printer without the necessity for "home"

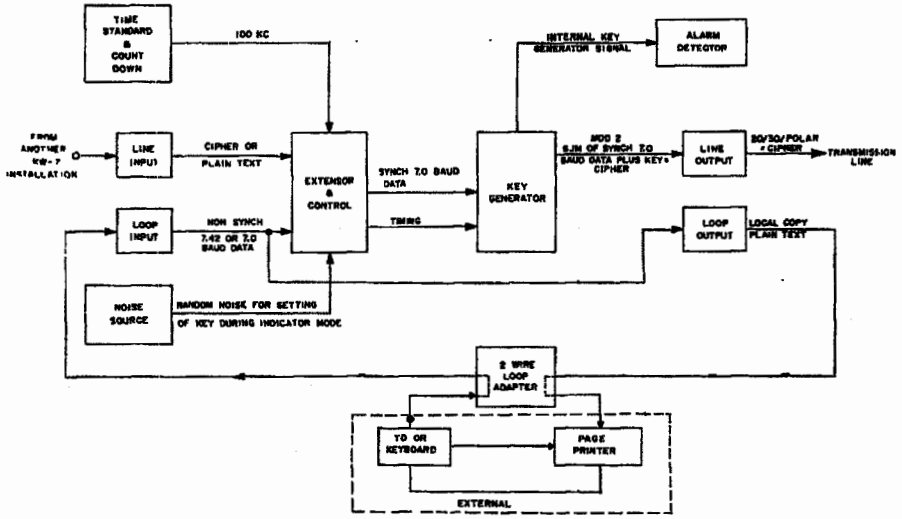


Figure 4-42.—Two-Wire Loop Adapter Unit Operation, Functional Block Diagram.

copy (Loop output) from the KW-7. The LOOP INHIBIT switch prevents the KW-7 loop-output circuit from interferring with the series keyboard page printer printout during transmit operation. Effectively then, a message is transmitted to the KW-7 loop-input circuit and at the same time printed on the local page printer. It is inhibited on the loop-output circuit, and also transmitted to another KW-7 through the line-output circuit. When receiving, the message is received at the KW-7 line-input circuit and routed through the Loop-Output circuit and the two-wire loop adapter unit to the page printer.

4307. Functional Remote Control Unit Operation.—When the two-wire loop adapter is employed with the KW-7, remote control of the KW-7 can be accomplished by using a functional remote control unit. The functional remote control unit can control KW-7 operations up to a maximum of 500 feet. The KW-7 is automatically forced into cipher mode when the functional remote control unit is connected. The functional remote control unit does not have the complete array of controls and indicators provided on both the KW-7 and the remote control unit. It contains a SEND switch to initiate phasing and indicator modes of operation, and both SEND and P&I lights to indicate SEND and PHASING and INDICATOR modes, respectively. An AUDIBLE ALARM and ALARM light are provided to indicate failure in the KW-7 due to either a simulated or an actual alarm condition. A TD stepping relay in the functional remote control unit will allow control signals from the KW-7 to step a remote

transmitter-distributor. A READY light is provided to indicate that the functional remote control unit is active. The functional remote control unit provides only control functions; no data signals are routed through the unit. Thus if SEND is initiated from the functional remote control unit, the KW-7 begins the transmission preparation and sends back control signals through the functional remote control unit to step the transmitter-distributor. The TD in turn transmits the plain text message directly to the KW-7 through the two-wire loop adapter unit.

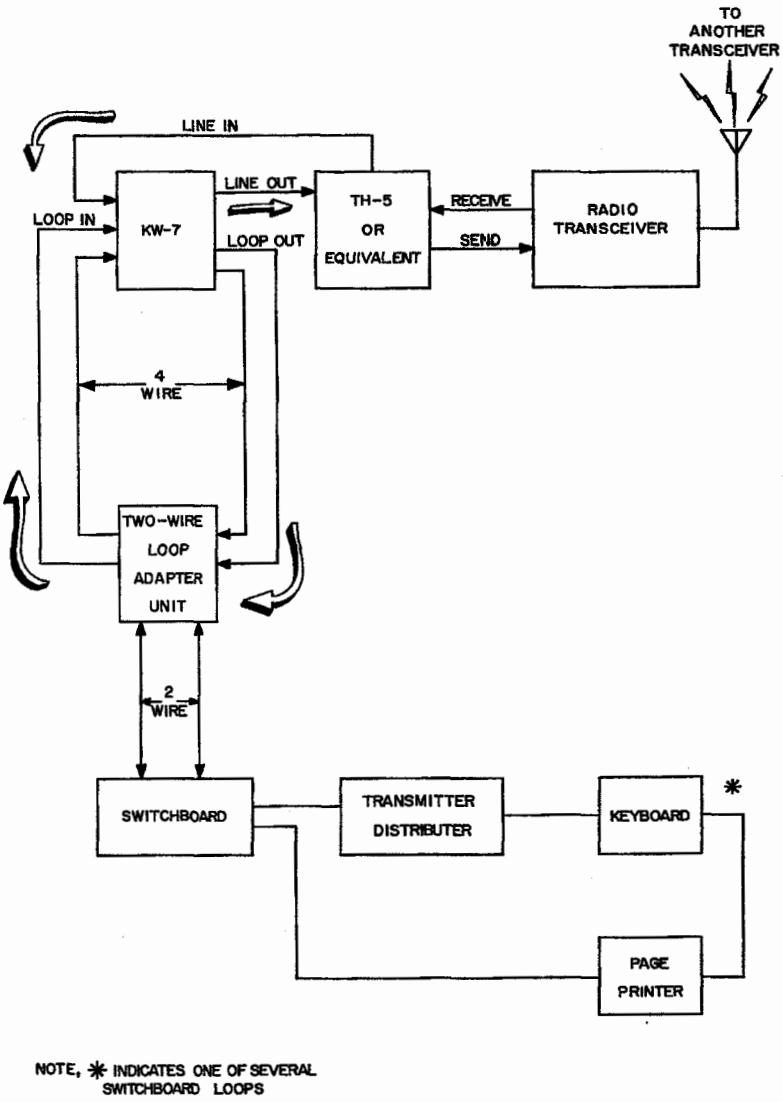


Figure 4-43.—Two-Wire Loop Adapter Unit, Typical Operation.

4400—DETAILED THEORY, FUNCTIONAL UNITS

4401. General.—In this section, the various functional units in the KW-7 are analyzed by means of logic diagrams. Idealized waveforms are included on several diagrams and some are included in the text to aid in understanding the circuit operation. As a further aid, several functional units are incorporated into a single diagram so that their inter-relationship may be more readily seen. In such cases, the functional units are separated by heavy broken lines. Each logic diagram includes information required for understanding the flow of signals. The overall logic diagrams for the extensor and control circuits (E and C) and the key generator circuits (KG) are in KAM-144B. Table 4-2 lists the names and abbreviations of signals used in the KW-7.

a. Logic Element Identification.—Each logic element is identified by a letter-digit designation (i.e. A11, 15). A11, 15 means that the subassembly in which the logic element may be found is A11 and that the module number is (MD) 15. This system makes it possible to determine, at a glance, the exact physcial location of the card and the module number on any logic diagram.

b. Input/Output Pin Numbering.—To clarify the relationship between the physical location of the individual logic elements and the schematics of these elements, the input and output leads have all been identified by the module pin numbers. In this manner it is possible to relate the input to a logic element with the physical input found on the subassembly board.

c. Test Point Identification.—Numerous test points are found throughout the logic diagrams. The test point designations identify the subassembly on which the test points are located and also identify the specific name of that test point. An example of test point identification follows: TPA1-11 indicates that test point 11 located on subassembly A1 is to be used. This eliminates the need for specifically coding test points to determine the exact location of logic element inputs or outputs.

TABLE 4-2

KW-7 CARD SIGNAL NAMES

Card	Signal	Connector Pin	Signal Description
E-AJK(A1)	Set	8	System initial set pulse
	F Drive Pulse	C	Fibonacci shift register drive pulse
	A	2	Fibonacci feedback signal
	$\overline{A}$	1	Fibonacci feedback signal
	$\overline{r1}$	x	$\overline{r}$ code combiner input
	$\overline{r2}$	19	$\overline{r}$ code combiner input
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GND	10	Ground
	16	F	Fibonacci shift register, output stage No. 16
	$\overline{16}$	E	Fibonacci shift register, output stage No. 16
	$\overline{r4}$	y	$\overline{r}$ code combiner input
	$\overline{r3}$	21	$\overline{r}$ code combiner input
	$\overline{r}$	22	$\overline{r}$ code combiner output
	$\overline{s}$	Z	$\overline{s}$ code combiner output
	$\overline{t}$	P	$\overline{t}$ code combiner output
E-AJJ(A2)	SET	8	System initial set pulse
	F Drive Pulse	9	Fibonacci shift register drive pulse
	$\overline{16}$	4	Fibonacci shift register, output stage No. 16
	16	1	Fibonacci shift register, output stage No. 16
	$\overline{r4}$	2	$\overline{r}$ code combiner input
	$\overline{r3}$	D	$\overline{r}$ code combiner input

TABLE 4-2 (Continued)

Card	Signal	Connector Pin	Signal Description
E-AJJ(A2) (Continued)	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	$\overline{32}$	x	Fibonacci shift register, output stage No. 32
	32	21	Fibonacci shift register, output stage No. 32
	$\overline{r2}$	3	$\overline{r}$ code combiner input
	r1	5	$\overline{r}$ code combiner input
	$\overline{p}$	R	$\overline{p}$ code combiner output
	$\overline{q}$	E	$\overline{q}$ code combiner output
	$\overline{r}$	B	$\overline{r}$ code combiner output
E-AJM(A3)	YN-1	5	An intermediate code form
	$\overline{p}$	M	$\overline{p}$ code combiner output
	SET	N	System initial set pulse
	KG	1	Timing signal for key generator activity
	$\overline{KG}$	2	Timing signal for key generator activity
	START	3	Time interval decoded from output counter
	STOP	4	Time interval decoded from output counter
	$\overline{M}$	B	Gating level that indicates data activity
	$\overline{PC0}$	W	Phasing counter, stage 0 output
	BG·$\overline{NO}$	V	BG and $\overline{\text{Normal}}$
	$\overline{PC1}$	X	Phasing counter, stage 1 output
	S·$\overline{N}$	Y	Send and $\overline{\text{Normal}}$
	WPM100	C	100 words per minute
	WPM67	K	67 words per minute
	$\overline{NORMAL\ 3}$	J	
	SEND 2	U	
	$\overline{s}$	P	$\overline{s}$ code combiner inverted output
	$\overline{YN-1}$	A	An intermediate code form
	E	T	Extensor (SRX) output
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	$\overline{E}$	E	$\overline{\text{Extensor (SRX) output}}$
	Z1	D	Output data form prior to start and stop bauds addition
	W	R	An intermediate code form
	V	S	Output of auto key generator
	$\overline{W}$	22	An intermediate code form
E-AJL(A4)	Z1	12	Output data form prior to start and stop bauds addition
	32	1	Fibonacci shift register, stage No. 32 output
	F Drive Pulse	3	Fibonacci shift register drive pulse
	32	2	Fibonacci shift register, stage No. 32 output
	SET	L	System initial set pulse
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	NORMAL 2	18	
	Z3	15	Output data form after start and stop bauds addition
	AT3A	4	Alarm test switch output
	$\overline{s}$	D	$\overline{s}$ code combiner output
	$\overline{t}$	K	$\overline{t}$ code combiner output
	I&N	S	Indicator or Normal
	OBR	T	Output bit rate
	PLAIN	A	
	$\overline{q}$	13	$\overline{q}$ code combiner output

TABLE 4-2 (Continued)

Card	Signal	Connector Pin	Signal Description
E-AJL(A4) (Continued)	$\overline{F}$	V	$\overline{F}$ code combiner output
	A	Y	Fibonacci feedback signal
	AT3A	N	Alarm test switch output
	Z1A	11	Output data form prior to addition of start and stop bauds
	35	J	Fibonacci shift register, stage No. 32 output
	$\overline{39}$	Z	Fibonacci shift register, stage No. 39 output
	39	22	Fibonacci shift register, stage No. 39 output
	YN-1	5	An intermediate code form
	$\overline{YN-1}$	C	An intermediate code form
	$\overline{NORMAL\ 3}$	19	
	A	21	Fibonacci feedback signal
	KG	R	Timing signal for key generator activity
	SP	F	Special point, F drive pulse deletion level
	$\overline{8}$	8	$\overline{8}$ code combiner inverted output
	$\overline{A}$	W	Fibonacci feedback signal
	AT4B	M	Alarm test switch output
E-AJO(A5)	$\overline{OBR1}$	M	Output bit rate
	$\overline{W}$	C	An intermediate code form
	$\overline{AT2A}$	B	Alarm test switch output
	ASP	1	Alarm sampling pulse
	I&N	4	Indicator and Normal
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	SET	L	System initial set pulse
	AT3A	K	Alarm test switch output
	GEO	T	Gated extensor output, crypto sync line
	NORMAL 1	U	
	KG	11	Timing signal for key generator activity
	Z2	9	An intermediate code form
	NORMAL 2	8	
	$\overline{NORMAL\ 2}$	H	
	35	J	Fibonacci shift register, stage No. 35 output
	39	D	Fibonacci shift register, stage No. 39 output
	$\overline{A}$	E	Fibonacci feedback signal
	$\overline{39}$	13	Fibonacci shift register, stage No. 39 output
	AT5	P	Alarm test switch output
	A	14	Fibonacci feedback signal
	AT6	R	Alarm test switch output
	GZO	F	Gated Z stream output, data line
	V	V	Output of auto key generator
	W	15	An intermediate code form
	$\overline{SEND\ 1}$	S	
	PLAIN	12	
	$\overline{E}$	21	Extensor (SRX) output
	Z1A	19	Output data form prior to addition of start and stop bauds
	E	20	Extensor (SRX) output
	Z1A	22	Output data form prior to addition of start and stop bauds
	AT8	18	Alarm test switch output
	AT7	X	Alarm test switch output
	$\overline{AT1A}$	2	Alarm test switch output
	AT10A	Z	Alarm test switch output
	ALARM 1	A	Condition indicative of a compromising failure which will disable transmitter
	ALLR	6	Alarm lamp remote

TABLE 4-2 (Continued)

Card	Signal	Connector Pin	Signal Description
E-AJO(A5) (Continued)	ALL	5	Alarm lamp
	TEX	16	Text
	$\overline{\text{TEX 1}}$	Y	$\overline{\text{Text}}$
	BUZ 1	W	Audible alarm actuator
E-AJN(A6)	$\overline{\text{INDC}}$	D	$\overline{\text{Indicator counter}}$
	SE 1	15	Send switch output
	SE2	X	Send switch output
	OC6	21	Output counter, stage 6
	$\overline{\text{CTRP}}$	W	$\overline{\text{P counter}}$
	−24V	14	Power supply voltage
	+6V	7	Power supply voltage
	P	13	Output counter character rate timing pulse
	INDC	1	Indicator counter
	−6V	17	Power supply voltage
	GRD	10	Ground
	SNB	J	Timing pulse (receive mode) for M flip-flop
	SNA	9	Something not available (data presence level)
	PLAIN	20	
	AT4A	11	Alarm test switch output
	OC0	M	Output counter, stage 0
	$\overline{\text{CLX}}$	B	$\overline{\text{Clear X register}}$
	$\overline{\text{SP}}$	3	$\overline{\text{Special point, F drive pulse deletion level}}$
	KG	4	Timing signal for key generator activity
	LIG	L	Lock in gate
	ALARM SET	Y	Level from alarm test switch which generates set pulses
	NORMAL 1	F	
	$\overline{\text{BREAK}}$	E	
	BRLR	S	Break lamp remote
	BRL	N	Break lamp
	SEND	16	
	BREAK	19	
	$\overline{\text{I\&N}}$	8	$\overline{\text{Indicator or Normal}}$
	I&N	H	Indicator or Normal
	NORMAL 2	A	
	NORMAL 3	6	
	$\overline{\text{NORMAL 2}}$	5	
	SEND 2	U	
	SEND 1	P	
	BG	18	Gating level for CLX
	$\overline{\text{SEND}}$	R	
	SET	K	System initial set pulse
	SET 1	12	Input to SET driver
	POWER SET	C	A special purpose set pulse
	SEND 1	V	
E-AJQ(A7)	$\overline{\text{LINE IN}}$	E	$\overline{\text{Gated line output}}$
	$\overline{\text{OBR-BIT 1}}$	A	$\overline{\text{Output bit rate and bit 1}}$
	OBR1	D	Output bit rate
	SEND 1	5	
	$\overline{\text{I\&N}}$	C	$\overline{\text{Indicator or Normal}}$
	$\overline{\text{START}}$	6	
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	TMSTD	Y	Time standard
	100KC B	8	100KC (internal or external) timing pulse to timing counter

TABLE 4-2 (Continued)

Card	Signal	Connector Pin	Signal Description
E-AJQ(A7) (Continued)	SET	Z	System initial set pulse
	WPM67	W	67 words per minute
	WPM100	X	100 words per minute
	SG	F	Slow gate
	100KC A	K	Internally generated 100KC signal
	CLOCK	V	Corrected system timing pulses
E-AJP(A8)	CLOCK	2	Corrected system timing pulse
	−24V	14	Power supply voltage
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	TRB	3	Transfer pulse, B register
	TRA	4	Transfer pulse, A register
	POWER SET	20	A special purpose set pulse
	$\overline{FL}$	21	$\overline{\text{Input character (fixed length) gating level}}$
	$\overline{EG}$	D	$\overline{\text{Gating level for CLX}}$
	$\overline{SEND\ 3}$	6	
	NORMAL 3	C	
	LIIST	F	Line in schmitt trigger
	MOD 6	Y	Input counter counting mode (6 bauds per cycle)
	$\overline{LOIG}$	K	$\overline{\text{Loop in gate}}$
	$\overline{NSC}$	22	$\overline{\text{Non-synchronous continuous}}$
	SEND 1	16	
	PA	Z	Plain asynchronous
	CLX	19	Clear X register
	IBR	V	Input bit rate
	LIG	18	Lock in gate
	$\overline{PCI}$	9	$\overline{\text{Phasing counter, stage 1}}$
	$\overline{PCO}$	5	$\overline{\text{Phasing counter, stage 0}}$
	$\overline{T8}$	1	A pulse used to measure MOD 8 phasing characters
	IC7	A	Input counter, stage 7
	$\overline{IBR1}$	W	$\overline{\text{Input bit rate}}$
E-AJS(A9)	S·$\overline{N}$	A	Send and $\overline{\text{Normal}}$
	Pd	3	P pulse delayed
	$\overline{SEND\ 2}$	H	
	SET	1	System initial set pulse
	SHIFT-A	R	SRA register shift pulse
	ABIN	4	Input of A and B registers
	$\overline{ABIN}$	5	$\overline{\text{Input of A and B registers}}$
	$\overline{CTRP}$	21	$\overline{\text{P counter}}$
	M 2 B	B	Randomizer output to SRA 2
	$\overline{CLX}$	19	$\overline{\text{Clear X register}}$
	TRA	P	Transfer pulse, A register
	INDC	22	Indicator counter
	NORMAL 2	X	
	$\overline{INDC}$	Y	$\overline{\text{Indicator counter}}$
	OBR1	12	Output bit rate
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	TRB	20	Transfer pulse, B register
	SHIFT B	6	SRB register shift pulse
	SRA2	11	Shift register A, stage 2
	SRA5	V	Shift register A, stage 5
	$\overline{SRA5}$	18	$\overline{\text{Shift register A, stage 5}}$

TABLE 4-2 (Continued)

Card	Signal	Connector Pin	Signal Description
E-AJS(A9) (Continued)	$\overline{E}$	2	Extensor (SRX) output
	E	S	Extensor (SRX) output
	ZOD	W	ZERO/ONE indicator message detector
E-AJR(A10)	SET	1	System initial set pulse
	CLOCK	2	Corrected system timing pulse
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	I&N	E	Indicator or Normal
	PILD	A	Phasing or Indicator lamp driver
	NORMAL 1	H	
	SRA 2	B	Shift register A, stage 2
	$\overline{BG}$	C	Gating level for CLX
	$\overline{BREAK}$	F	Recognized break condition
	SET 1	8	Input to SET driver
	$\overline{BRK}$	11	$\overline{BREAK}$
	LIOD	M	Line out digital
	LIIST	14	Line in schmitt trigger
	$\overline{NORMAL\ 2}$	N	
	BRK	K	Signal initiating transmisson break
	BRLO	R	Break receive lockout
	OC6	Z	Output counter, stage 6 output
	OC0	3	Output counter, stage 0 output
	OBR	22	Output bit rate
	CTRP	20	P counter
	$\overline{CTRP}$	Y	$\overline{P\ counter}$
	$\overline{OC6}$	21	$\overline{Output\ counter,\ stage\ 6\ output}$
	$\overline{OBR\ 1}$	12	$\overline{Output\ bit\ rate}$
	$\overline{CTRP\ 1}$	19	$\overline{P\ counter,\ stage\ 1\ output}$
	STOP	X	
	$\overline{OBR \cdot BIT\ 1}$	J	$\overline{Output\ bit\ rate\ and\ bit\ 1}$
	START	T	
	$\overline{START}$	V	
	$\overline{P}$	9	$\overline{Output\ counter\ character\ rate\ timing\ pulse}$
	P	W	Output counter character rate timing pulse
	ICR	D	Indicator counter reset
	Pd	S	P pulse delayed
	OBR 1	4	Output bit rate
	CLX	P	Clear X register
	$\overline{CLX}$	18	$\overline{Clear\ X\ register}$
	OBR 2	V	Output bit rate
	BTC	13	Break receive level to break (indicator) character counter
E-AJU(A11)	NORMAL 3	15	
	ABIN	M	Input of A and B registers
	IBR	14	Input bit rate
	SET	F	System initial set pulse
	$\overline{T8}$	B	$\overline{A\ pulse\ used\ to\ measure\ MOD\ 8\ phasing\ characters}$
	IC7	H	Input counter, stage 7 output
	P	E	Output counter character rate timing pulse
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	$\overline{SEND\ 1}$	3	
	LIS	N	Loop inhibit switch
	$\overline{PA}$	L	$\overline{Plain\ asynchronous}$

TABLE 4-2 (Continued)

Card	Signal	Connector Pin	Signal Description
E-AJU(A11) (Continued)	LIIR	4	Line in relay
	M	K	Gating level that indicates data activity
	OBR1	18	Output bit rate
	NORMAL3	2	
	Z2	1	Data output in final form (start-stop bauds superimposed)
	LOCO	A	Loop output control
	PC0	U	Phasing counter, stage 0 output
	LO12	6	Loop in
	PTS	S	Plain text safety
	PC1	T	Phasing counter, stage 1 output
	ALARM 1	P	
	SEND 1	Y	
	SAG	20	Shift A gate
	IBRI	X	Input bit rate
	SBG	21	Shift B gate
	OBRI	19	Output bit rate
	SEND	22	
	FL	C	Input character (fixed length) gating level
	DS	16	Down shift
	NSC	9	Non-synchronous continuous
	MOD 6	J	Input counter counting mode (6 bauds per cycle)
	LOIG	D	Loop in gate
	LOOD	V	Loop out digital
	LIIST	5	Line in schmitt trigger
	SEND 2	R	
	FL	8	Input character (fixed length) gating level
	SEL	11	Send lamp
	SELR	13	Send lamp remote
	SHIFT-A	Z	Register A shift pulse
	SHIFT-B	W	Register B shift pulse
E-AJT(A12)	ICR	N	Indicator counter reset
	Pd	F	P pulse delayed
	BTC	22	Break receive level to break (indicator) character counter
	ZOD	1	ZERO/ONE indicator message detector
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	BRK	4	Break
	GRD	10	Ground
	DS	5	Down shift
	SEND 3	A	
	SET	M	System initial set pulse
	IC7	C	Input counter, stage 7 output
	SEND	Y	
	SRA5	W	Shift register A, stage 5 output
	TEX	J	Text
	OBR2	3	Output bit rate
	TEX-1	8	Text
	SRA5	12	Shift register A, stage 5 output
	FL	2	Input character (fixed length) gating level
	SEND 2	T	
	NORMAL 2	S	
	SET 1	B	Input to SET driver
	P	19	Output counter character rate timing pulse
	INDC	20	Indicator counter
	INDC	21	Indicator counter

TABLE 4-2 (Continued)

Card	Signal	Connector Pin	Signal Description
E-AJT(A12) (Continued)	M	Z	Gating level that indicates data activity
	Pd	H	P pulse delayed
	LIOD	K	Line out digital
	LOCO	6	Loop out control
	SNA	18	Something not available (data presence level)
	TRA	P	Transfer pulse, A register
	SAG	E	Shift A gate
	SNB	V	Timing pulse (receive mode) for M flip-flop
	SBG	D	Shift B gate
	M	X	Gating level that indicates data activity
	TRB	U	Transfer pulse, B register
E-AJW(A13)	SOS	2	Special one shot (randomizer) output
	AT1B	P	Alarm test switch output
	RNA1	R	Randomizer (stage 1)
	CTRP	1	P counter
	I&N	5	Indicator or Normal
	PLAIN	4	
	+6V	7	Power supply voltage
	-6V	17	Power supply voltage
	GRD	10	Ground
	ABIN	19	Input of A and B registers
	RNA2	S	Randomizer (stage 2)
	AT2B	T	Alarm test switch output
	SET	22	System initial set pulse
	OBR2	Z	Output bit rate
	M2A	V	Randomizer output to alarm
	M2B	21	Randomizer output to SRA2
	PLAIN-1	X	
	BREAK	3	
	BUZ1	6	Audible alarm actuator
	CLOCK	B	Corrected system timing pulses
	OC6	H	Output counter, stage 6
	ALARM 1	9	Condition indicative of a comprising failure which will disable transmitter
	CTRP2	11	P counter
	M	D	Gating level that indicates data activity
	NORMAL 3	12	
	Z1A	16	Output data form prior to addition of start-stop bauds
	START	18	
	STOP	14	
	NORMAL	13	
	E	N	Extensor (SRX) output
	SEND2	Y	
	MIL	L	MI lamp
	ASP	20	Alarm sampling pulse
	ACT	W	Activity (PTS function)
	AUDO1	K	Audible alarm
	REDR	A	Relay driver
	GZO	15	Gated Z stream output, data line
	Z3	M	An intermediate code form
	Z2	J	An intermediate code form
	S·N	E	Send and Normal
	GEO	F	Gated extensor output, crypto sync line
	AT4B	C	Alarm test switch output
	Z1A	U	Output data form prior to addition of start-stop bauds
	SEND3	8	

TABLE 4-2 (Continued)

Card	Signal	Connector Pin	Signal Description
E-AJV(A14)	LIIR	3	Line in relay
	ALARM SET	U	Level from alarm test switch which generates set pulses
	AUDO1	A	Audible alarm
	REDR	D	Relay driver
	LOA1	19	Loop output analog 1
	−40VR	16	Zener controlled 40 volt reference for loop out circuits
	−18V	22	Power supply voltage
	−53V	12	Power supply voltage
	$\overline{OBRI}$	P	Output bit rate
	+6V	7	Power supply voltage
	−6V	17	Power supply voltage
	GRD	10	Ground
	$\overline{S \cdot N}$	21	Send and Normal
	AT4A	M	Alarm test switch output
	LIOD	5	Line out digital
	LOOD	C	Loop out digital
	LOA2	2	Loop out analog 2
	LOOA	B	Loop out analog
	LIOR	4	Line out relay
	LIOA	6	Line out analog
	AUDO2	1	Audible alarm
	NCL	E	Negative coil (TD step relay)
	TDS1	K	Transmitter-Distributor step pulse 1
	PCL	F	Positive coil (TD step relay)
	LOOP	V	Loop out positive
	LOA3	20	Loop out analog 3
	ZR	15	Zener reference
	LOON2	T	Loop out negative 2
	SOS	11	Special one shot (randomizer) output
	RNA1	R	Randomizer (stage 1)
	M2B	H	Randomizer output to SRA2
	M2A	N	Randomizer output to alarm logic
	RNA2	S	Randomizer (stage 2)

4402. Detailed Theory.—The remaining portion of this section is devoted to a detailed analysis of the individual functional units contained within the KW-7. The previous section described the functional operation of the KW-7 at the detailed block diagram level. The purpose of this section is to further expand this description to encompass the logic operation of the same functional units. These units will be broken down into separate logic diagrams and will be discussed on a logic level. Each input and output will be traced throughout the entire system to enable the technician to follow signal flow. Where necessary waveforms will be incorporated into the logic diagrams to bring out a specific point. The logic will be explained in the same order as the explanation of the functional units.

a. *Timing.*—The following paragraphs describe the timing used by the KW-7. Accurate timing is necessary to enable the receiving KW-7 to synchronize itself with the transmitting KW-7. To achieve this timing, various circuits contained within the Extensor and Control portion of the system are employed. These circuits are the time standard, the divider circuit, the input bit and character counter, and the output bit and character counter. The following paragraphs describe the function of each of these circuits and define its relation to the timing of the system. Also figures 4-84 through 4-86 illustrate timing during phasing and synchronization and extensor and control operation during Receive Plain and Send Cipher.

(1) *Time standard.*—The time standard employed by the KW-7 is an adjustable, crystal-controlled, one megacycle oscillator. The time standard provides a stable time reference to allow operation over long intervals of time without the requirement that synchronization be transmitted.

(2) *Divider circuit.*—The divider circuit counts down the 1 mc signal to a frequency suitable for use within the remaining portions of the timing circuitry. The output from this circuit is also fed to the phase correction logic circuit for further use within the timing circuits.

(3) *Phase correction circuit.*—The phase correction circuit automatically adjusts the receiver timing if frequency drift occurs between the transmitting and receiving KW-7. This adjustment is accomplished by monitoring the stop-start transition of incoming data (line input) and correcting the local timing to synchronize it with the incoming signal.

(4) *Clock pulse generating circuit.*—The clock pulse generating circuit controls the repetition rate of the system clock pulses. The clock pulse repetition rate depends upon the setting of the speed selector switch which synchronizes the KW-7 with the teletypewriter equipment being employed.

b. Timing Diagrams (fig. 4-44).—To fully understand the function of timing, it will first be necessary to relate the various timing functions to an illustration depicting the sequential occurrence of these pulses. Prior to discussing the timing pulses it should be mentioned that the phase correction circuit appear on the timing diagram. Although the phase correction circuit is an inherent part of the timing it does not play an active part in the actual generation of timing pulses. Each pulse generated by the timing circuit is identified on the illustration. In addition to pulse identification, the test point or module pin number at which these pulses may be observed, is also identified on the illustration.

(1) *Time standard and divider circuit pulses.*—The 1 mc output from the time standard is fed to a five stage counter (divide by 20) located within subassembly A7. The five stages of the divider circuit count the fundamental 1 mc frequency down to 50 kc for further use throughout the KW-7. The 50 kc output is fed to the phase correction circuit and to the clock pulse generating circuit.

Note: Figure 4-44 (sheet 1) illustrates two 50 kc pulse trains one beneath the other. In order to illustrate the timing sequence it was necessary to reduce the expanded 50 kc pulse train to allow sufficient room to implement the remaining timing pulses. This practice was also used to divide the IBR (input bit rate) and OBR (output bit rate) pulses.

(2) *Clock pulse generating circuit pulses.*—Subassembly A7 also contains the circuit required to generate one of three fundamental clock frequencies. The selection of the proper clock frequency depends on the setting of the speed selector switch which matches the clock frequency to the speed of the teletypewriter. Figure 4-44 illustrates the individual frequencies generated by each stage of the counter for all three teletypewriter speeds. The output from the clock pulse generating circuit (1125 cps, 1250 cps, or 1875 cps) is fed to both the input bit rate and character counter and the output bit rate and character counter for further processing.

(3) *Input bit rate and character pulses.*—The input bit rate and character counter consists of eight stages divided into two separate functions. The first five stages combine to generate the input bit rate pulse (IBR). Feedback control in the five stage IBR counter forces a counting cycle of 25 instead of a count of 32. The last three combine to generate the input character pulse (IC7). During the normal phase of the send mode, if the KW-7 is not actively transmitting data, the input character counter generates character pulses which consists of eight bits (MOD 8). The eight bit character pulses are used by the receive phasing circuit to detect that another KW-7 has initiated

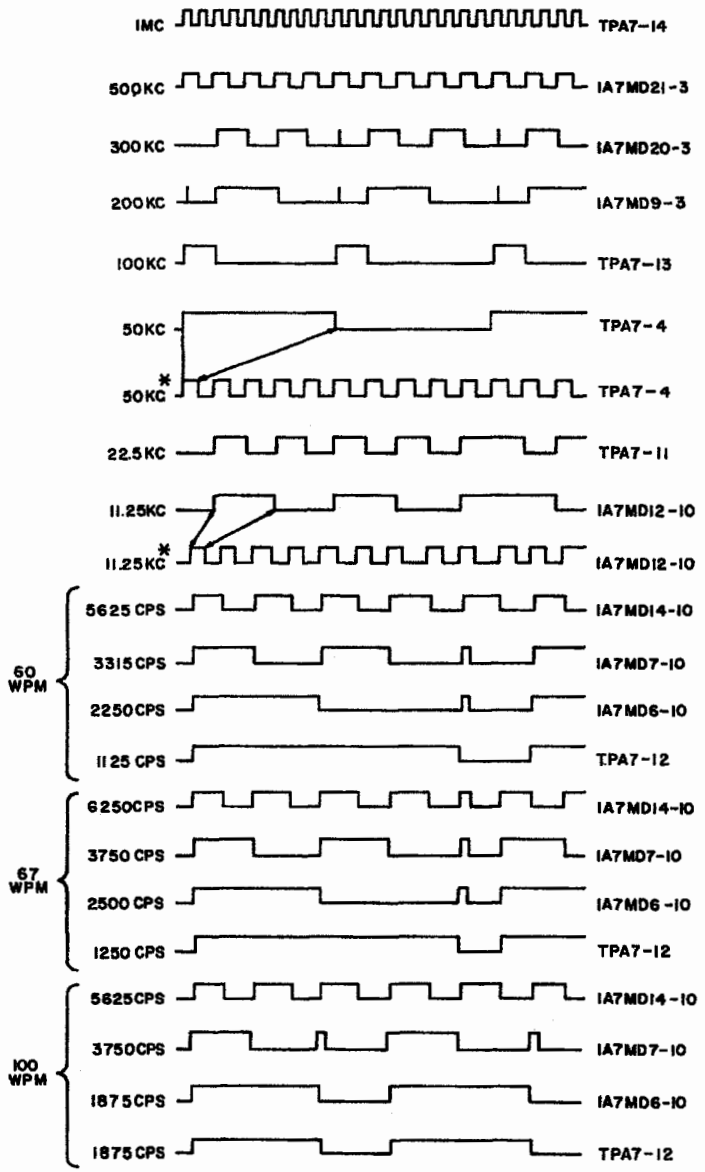


Figure 4-44.—Timing Diagrams (Sheet 1).

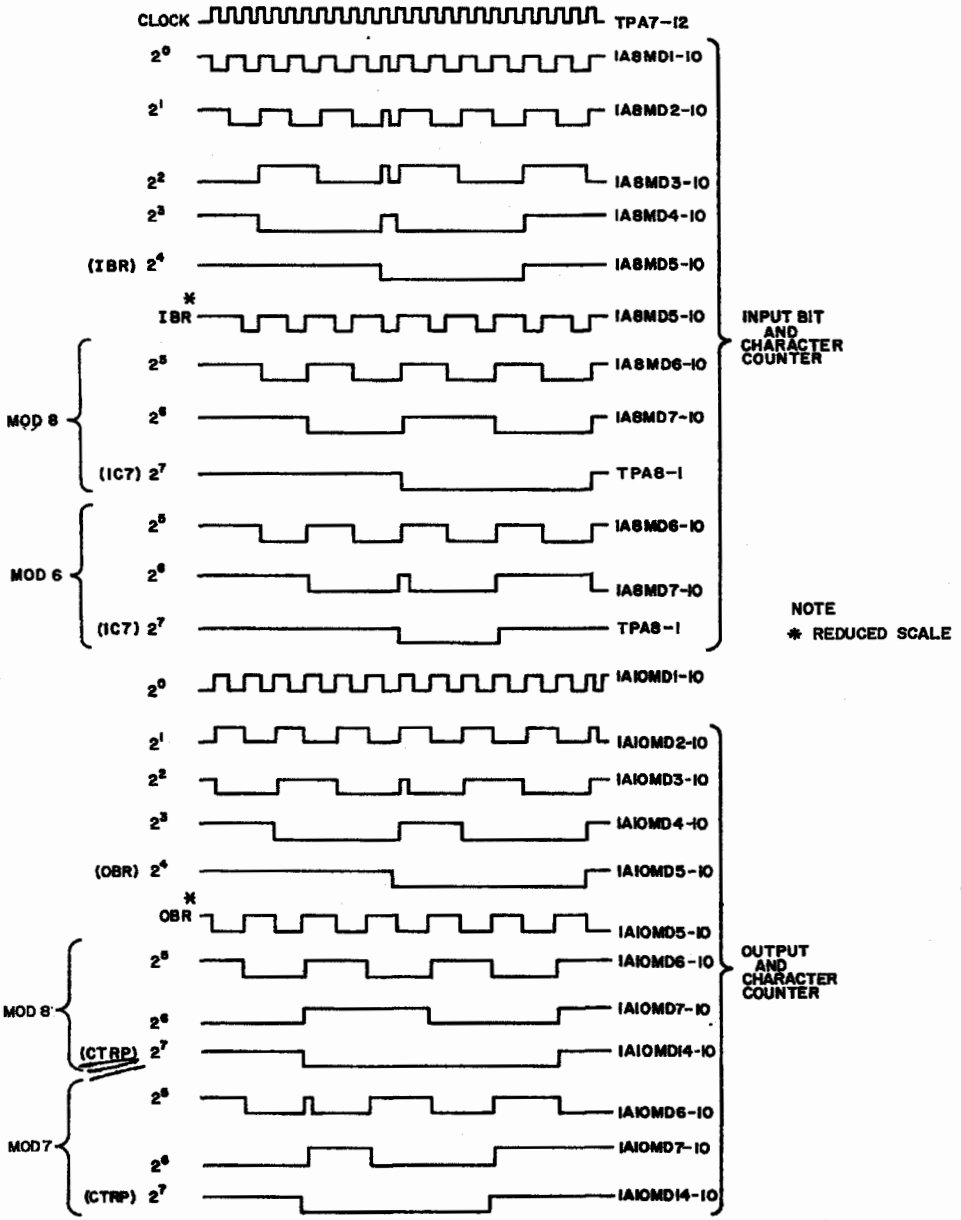


Figure 4-44.—Timing Diagrams (Sheet 2).

phasing. The generation of clock pulses causes the first five stages of the input bit rate and character counter to generate IBR pulses. The last three stages of the input bit rate and character counter generate the input character pulses (IC7). The type of input character pulse is dependent upon the operational mode of the system. For purposes of clarity, both the six and eight bit characters will be explained. The last three stages of the input counter are used to generate IC7 pulses in the eight bit mode. The same three stages when controlled by feedback delete two counts and produce IC7 pulses in the 6 bit mode.

(a) Eight bit character generation.—Figure 4–44 (sheet 2) illustrates the generation of the first IBR pulse. In order to generate an eight bit character it is necessary that the three flip-flops in the character counter be set to one. By observing the generation of the IBR pulses and the corresponding output from the three input character counter flip-flops this becomes apparent. Table 4–3 illustrates the generation of the eight IBR pulses and the generation of the eight bit character pulse. The output signal of flip-flop A8 MD14 is called IC7. The generation of the next IBR pulse will begin the process over with the output from the three flip-flops being 011.

TABLE 4-3

GENERATION OF INPUT COUNTER EIGHT BIT CHARACTER PULSE

IBR Pulse	Input Character Counter Flip-Flop Outputs		
MD5	MD6	MD7	MD14
Initial State	1	1	1
1	0	1	1
2	1	0	1
3	0	0	1
4	1	1	0
5	0	1	0
6	1	0	0
7	0	0	0
8	1	1	1

(b) Six bit character generation.—When the six bit character is required the count of the input character counter is inhibited for two counts, as shown in figure 4–44 (sheet 2) and Table 4–4. The output signal of flip-flop A8 MD14 is called IC7. The generation of the next IBR pulse will repeat the process. The input counter circuit functions are discussed in more detail in paragraphs 4403*b*(1) and 4403*b*(2).

TABLE 4-4

GENERATION OF INPUT COUNTER SIX BIT CHARACTER PULSE

IBR Pulse	Input Character Counter Flip-Flop Outputs		
MD5	MD6	MD7	MD14
1	0	1	1
2	1	0	1
3	0	0	1
4	1	0	0
5	0	0	0
6	1	1	1

(4) *Output bit rate and character pulses.*—The output bit rate and character counter consists of eight stages divided into two separate functions. The first five stages combine to generate the output bit rate pulse (OBR) and the last three combine to generate the output character pulse (CTRP). During the phasing mode the output bit rate counter will generate eight bits per character pulse. Upon the completion of phasing, the output bit rate counter will generate seven bits per character pulse which indicate that the KW–7 is in either the indicator or normal mode. The first five stages of the output bit rate and character counter count down the clock pulses (divide by 25) to generate the OBR pulses. The last three stages of the output bit rate and character counter counts down the OBR pulses to generate the output character pulses. The type of output character generated is dependent upon the present operational mode of the equipment. For purposes of clarity both the seven and eight bit characters will be explained.

(a) Eight bit character generation.—Figure 4–44 illustrates the generation of the first OBR pulse. This is accomplished in the same manner as that for the eight bit character pulse being generated by the input bit rate and character counter. The only difference between the generation of the OBR and the IBR is the initial output of the output character counter. The input character counter was initially set to a 111 output. The output character counter is set to a 101 output because the output from the three flip-flops must perform more than one function. The various additional functions performed by these flip-flops will be covered in the detail theory portion of this section and need only be mentioned here to clarify the initial use. Figure 4–44 (sheet 2) and table 4–5 illustrate the generation of the eight OBR pulses and the generation of the eight bit character pulse (CTRP). The CTRP signal corresponds to the output of flip-flop A10MD14. The generation of the next OBR pulse will begin the process over with the output from the three flip-flops being 001.

TABLE 4–5

GENERATION OF OUTPUT COUNTER EIGHT BIT CHARACTER PULSE

OBR Pulse	Output Character Counter Flip-Flop Outputs		
MD4	MD6	MD7	MD14
Initial State	1	0	1
1	0	0	1
2	1	1	0
3	0	1	0
4	1	0	0
5	0	0	0
6	1	1	1
7	0	1	1
8	1	0	1

(b) Seven bit character generation.—When the seven bit character is required, one count of the eight possible counts is bypassed by feedback. By observing the count illustrated on figure 4–44 (sheet 2) and table 4–6 this becomes apparent. The generation of the next OBR pulse will repeat the process. The output counter circuits are discussed in more detail in paragraphs 4403c(1) and 4403c(2).

TABLE 4-6

GENERATION OF OUTPUT COUNTER SEVEN BIT CHARACTER PULSE

OBR Pulse	Output Character Counter Flip-Flop Outputs		
MD4	MD6	MD7	MD14
Initial State	1	0	1
1	0	0	1
2	0	1	0
3	1	0	0
4	0	0	0
5	1	1	1
6	0	1	1
7	1	0	1

c. *Loop Input Circuit (fig. 4-45).*—The loop input circuit is employed during send operation.

(1) *Theory of operation.*—The function of the loop input circuit is to convert the transmitted message from the sending teletypewriter into digital information which can be processed by the sending KW-7's extensor and control. The conversion of the teletypewriter message into digital information is accomplished by converting the opening and closing of the teletypewriter TD or keyboard contacts into voltages which represent logical ONEs and ZEROs.

(2) During message transmission, the output contacts of the teletypewriter open and close in accordance with the transmitted messages. The output contacts of the teletypewriter are connected to pin 1 of the loop input module. Whenever the contacts close, pin 1 is grounded, cutting off transistor Q1. With Q1 cutoff, its collector output approaches the collector supply voltage (+6 volts.) This positive voltage is applied to the base of Q2 through diode CR2 and RC network C2 and R7. This positive voltage turns off Q2 and allows the collector voltage to drop from 0 volts to −6 volts. The output from Q2 is applied to the base of Q3 where inversion takes place with the collector output (pin 3) approaching 0 volts. The output from the loop input circuit, pin 3 is applied to pin 5 of the Schmitt trigger (fig. 4-33). The theory of the Schmitt trigger has been discussed previously and need not be repeated here. It will suffice to explain that the Schmitt trigger reshapes the output from the loop input module. A logical ONE pulse output from the Schmitt trigger represents the closing of the teletypewriter TD or keyboard contacts. A logical ZERO pulse output from the Schmitt trigger represents the opening of the teletypewriter TD or keyboard contacts. Normally the inclusion of the loop input circuit would not be necessary in that the opening and closing of the TD or keyboard contacts can be used by the Schmitt trigger. Due to sliding of the relay contacts when they open or close, a fast series of bounce pulses (chatter) appears at the input to the Schmitt trigger as a "staircase" voltage. The steps of this waveform are not sufficient to trigger the Schmitt trigger. The integration of the loop input circuit reduces the fast series of pulses to a gradual rise (or fall). This is accomplished through the use of the RC network, C2 and R7.

d. *Line Input Circuit (fig. 4-45).*—The line input circuit is used during receive operations.

(1) *Theory of operation.*—The line input circuit converts the transmitted message from the sending KW-7 into digital information that can be processed by the receiving KW-7's extensor and control. This is accomplished by converting the line input current into voltages which represent logical ONE's and ZERO's. The line input circuit consists of the LINE current selector switch, the line input relay, loop input circuit, and the Schmitt trigger employed by the loop input circuit.

(2) The transmitted message from the sending KW-7 is applied to pins 2 and 3 on the line input relay 1A18K1. A bias current is applied to pins 1 and 8 of the line input relay from the line input selector switch. When the sending KW-7 is operating in the neutral mode of transmission, the transmitted message consists of 60/20 milliamperes of current for a mark and 0 milliamperes of current for a space. When a mark is applied to the line input relay, the +60/20 milliampere current overcomes the bias current applied to pins 1 and 8. This action closes the line input relay which in turn applies a ground to pin 1 of the loop input circuit. When a space is applied to the line input relay, there is zero current. This action causes the bias current to release the line input relay which then removes the ground from pin 1 of the line input circuit. When the KW-7 is operated in the polar mode of operation, the transmitted message consists of +30/20 milliamperes of current for a mark and −30/20 milliamperes for a space. No bias current is applied to the line input relay during polar operation. The line input relay is operated by the +30/20 milliamperes each time a mark is received. This action causes the line input relay contacts to apply a ground to pin 1 of the line input circuit. The line input relay is released by the application of the −30/20 milliamperes of current each time a space is received. This action causes the line input relay contacts to

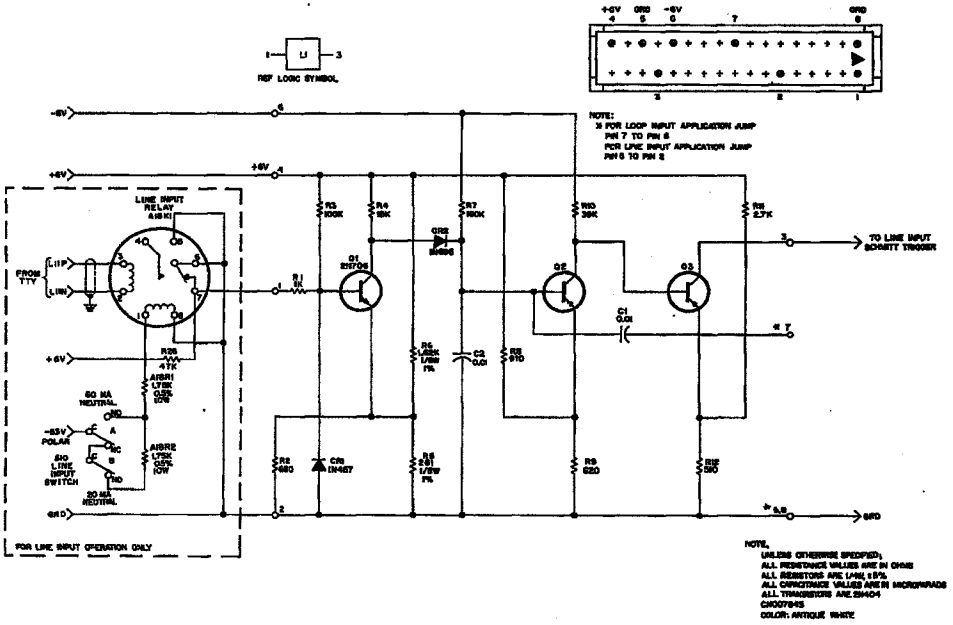


Figure 4-45.—Loop Input/Line Input Schematic Diagram.

remove ground from pin 1 of the loop input circuit. The theory of operation for the line input circuit and Schmitt trigger is identical to that described in the preceding paragraph with but one difference; during line input operation it is necessary to jumper pin 2 to pin 5 of the loop input circuit. This effectively puts R2 and R5 in parallel and allows more current to flow through the line input relay contacts by reducing the bias on transistor Q1.

e. *Noise Source (fig. 4-46).*—The noise generation circuit produces ten microsecond bursts of band limited noise which are used by the randomizer to produce a random stream of ONEs

and ZEROs. The noise source consists of two noise generators, two noise amplifiers, a special one-shot multivibrator, and a noise gate. Two noise generators and two noise amplifiers are used so that the KW-7 can continue operating if one pair fails.

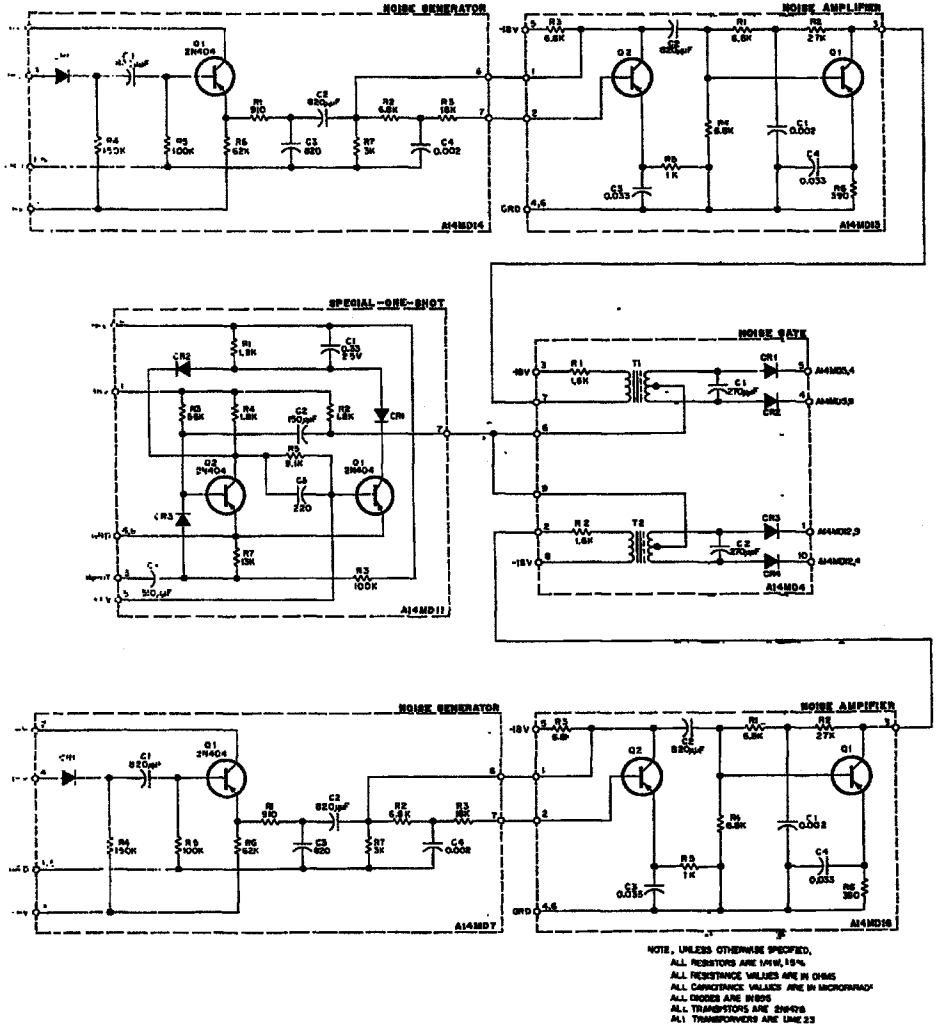
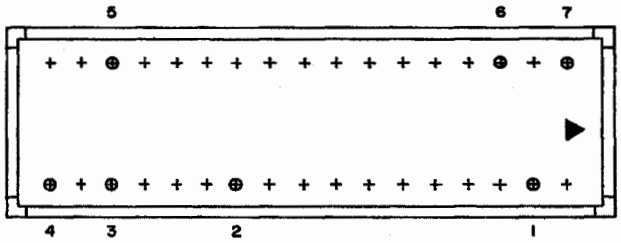
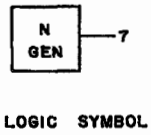


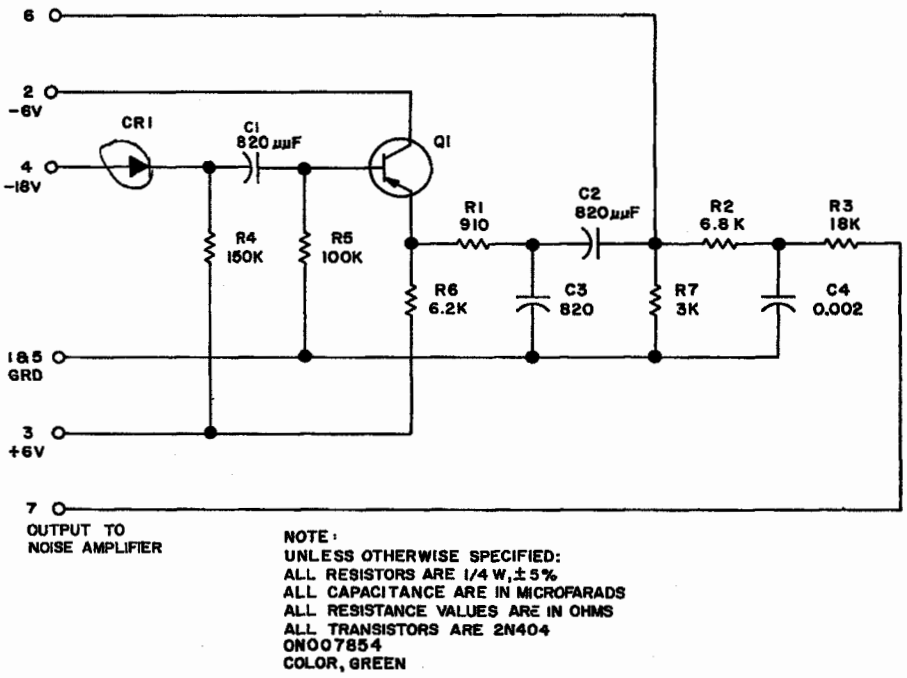
Figure 4-46.—Noise Source, Schematic Diagram.

(1) *Noise generator (fig. 4-47).*—Reverse-biased diode CR1 generates random noise which is coupled via emitter follower Q1 to an audio bandpass filter comprising R1, R2, R3, R7, C2, C3, and C4. The random noise output of the filter, pin 7, is applied to the noise amplifier.

(2) *Noise amplifier (fig. 4-48).*—The noise from the noise generator is amplified by noise amplifier Q2 and noise amplifier Q1. The load circuit of Q1 (pin 3) is part of the noise gate circuit described below.

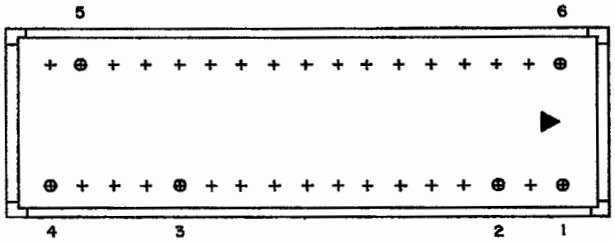




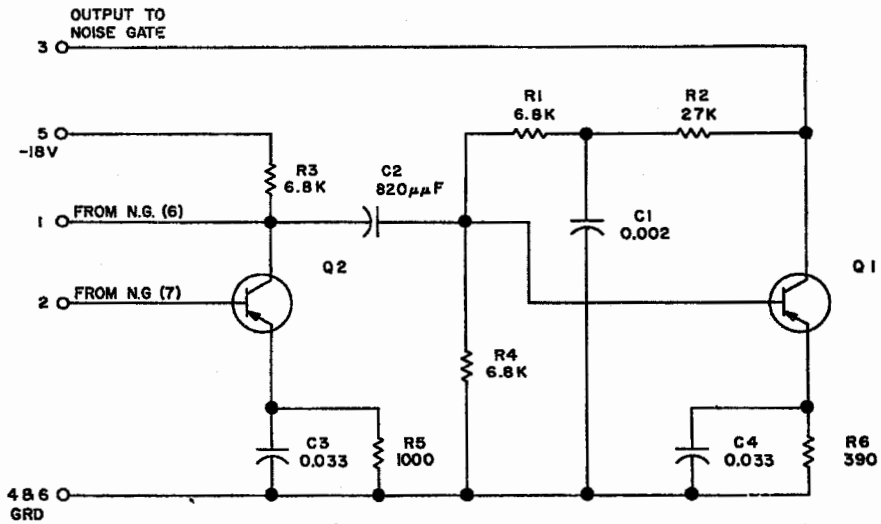


NOTE:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 W, ± 5%
ALL CAPACITANCE ARE IN MICROFARADS
ALL RESISTANCE VALUES ARE IN OHMS
ALL TRANSISTORS ARE 2N404
ON007854
COLOR, GREEN

Figure 4-47.—Noise Generator, Module Schematic Diagram.

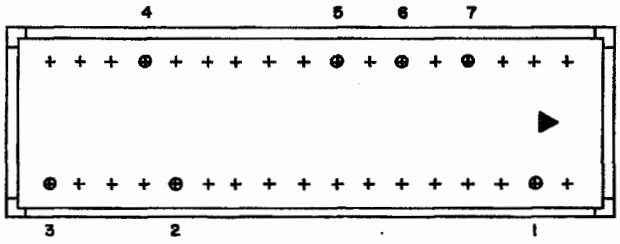


LOGIC SYMBOL

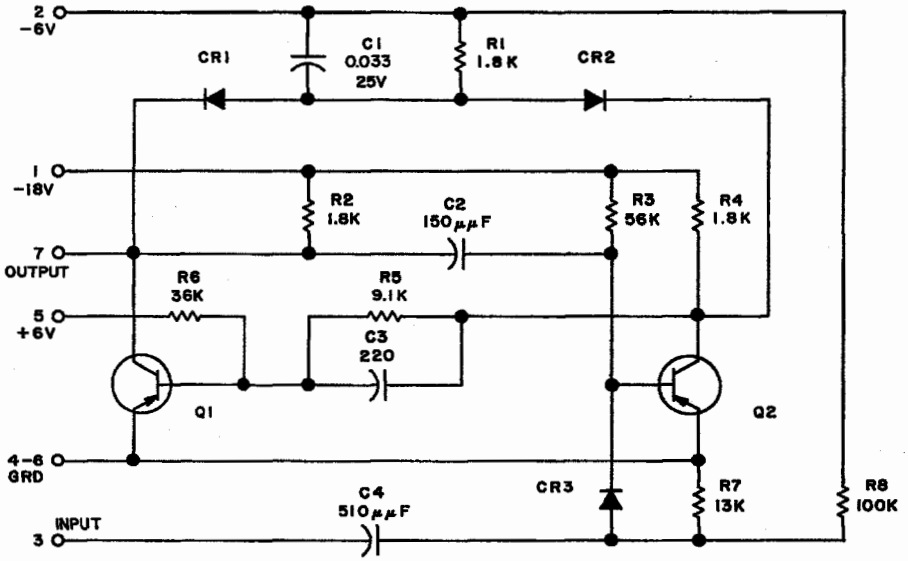


NOTE:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4 W, ±5%
ALL CAPACITANCE VALUES ARE IN MICROFARADS
ALL RESISTANCE VALUES ARE IN OHMS
ALL TRANSISTORS ARE T-2239
ON007853
COLOR: LIGHT/MEDIUM GREEN

Figure 4-48.—Noise Amplifier, Module Schematic Diagram.



LOGIC SYMBOL



NOTE: UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/4 W ± 5 %
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROFARADS
ALL TRANSISTORS ARE 2N404
ALL DIODES ARE IN695
ONOO7851
COLOR; LIGHT GREEN

Figure 4-49.—Special One Shot, Module Schematic Diagram.

(3) *Special one-shot (fig. 4-49).*—The positive-going transitions of the OBR1 pulses are coupled via capacitor C4 and diode CR3 to the input of the special one-shot multivibrator comprising Q1 and Q2. A gate pulse output from the one-shot is taken from pin 7 and applied to the secondary center tap of transformers T1 and T2 of the noise gate circuit.

(4) *Noise gate circuit (fig. 4-50).*—Resistor R1 and the primary of transformer T1 complete the collector circuit for the second noise amplifier. T1 couples the random noise to diodes CR1 and CR2. Gating pulses from the special one-shot multivibrator are applied to the center tap of the T1 secondary; these gating pulses occur at the OBR repetition rate, and serve to back-bias or forward-bias diodes CR1 and CR2, thus controlling the noise coupled through the diodes to the output. The circuit at the bottom of the illustration operates the same way.

4403. Extensor and Control Detailed Theory.—The detailed theory of operation for the extensor and control explains the theory of operation for each functional block described in Section 4300. The theory of operation for each functional block is explained in terms of logical inputs and outputs (ZERO and ONE). Each logic diagram of a functional unit is supported by text which defines the individual inputs and outputs.

a. *Clock Pluse Generating Circuit (fig. 4-51).*—The clock pulse generating circuit controls the generation of the basic timing (clock) pulses used in the input and output bit rate and character counters; in addition the circuit maintains synchronism between the sending and receiving KW-7's. The circuit consists of a ÷ 10 counter, a deletion counter, a gated counter, a variable counter, and the phase correction logic.

(1) *÷10 counter.*— The 1-megacycle (mc) output from the time standard is fed to the ÷ 10 counter consisting of flip-flops A7-21, A7-20, A7-19, and A7-18. These flip-flops divide the 1-mc input frequency by 10 to give a 100-kilocycle (kc) output. The four flip-flops are connected in series, with the output of a given stage being applied to the input of the following stage. Each flip-flop divides the input frequency by two. The use of four flip-flops normally results in a division by 16 rather than a division by 10; however feedback from the fourth flip-flop to the second and third flip-flops deletes six counts from the total count, allowing operation as a ÷ 10 counter. The output from pin 3 of the fourth stage is fed to flip-flop A7-17 (the ÷ 2 counter) which divides the 100-kc input by two to give a 50-kc output. A jack is provided on the input to flip-flop A7-17 to provide an input for an external master 100-kc oscillator. At sites having multiple KW-7's, the external 100-kc oscillator could serve as a common pulse source replacing the function of each time standard and ÷ 10 counter in all KW-7's at the site. The external 100-kc pulse source, if used, would be divided by 2 to 50 kc in flip-flop A7-17.

(2) *Deletion counter.*—The 50-kc output ÷ 2 is fed to the deletion counter (A7-1 through A7-4), gated counter flip-flop A7-11, and to the phase correction logic. The deletion counter is similar to the ÷ 10 counter in that it also uses feedback, by way of AND gates A7-13A and A7-13B, to permit operation as a ÷ 10 counter. Each time the output from pin 3 of A7-4 changes from a ZERO to a ONE, gates A7-13A and A7-13B reset A7-2 and A7-3, deleting six counts from the total count, and giving a division by 10 instead of 16. The output from pin 10 of the first stage (A7-1) is applied to NOR gate A7-9B. The 5-kc output from pin 10 of the fourth stage (A7-4) is fed to the phase correction circuit, and to NOR gate A7-9B. Either this signal, or the one from the first stage, will give a ZERO output on pins 12, 13 of A7-9B.

(3) *Gated counter.*—The gated counter provides a variable frequency signal, centered at 22.5 kc, to the variable counter. The output frequency of the gated counter is shifted slightly up or down in order to maintain the receiving KW-7 in synchronism with the

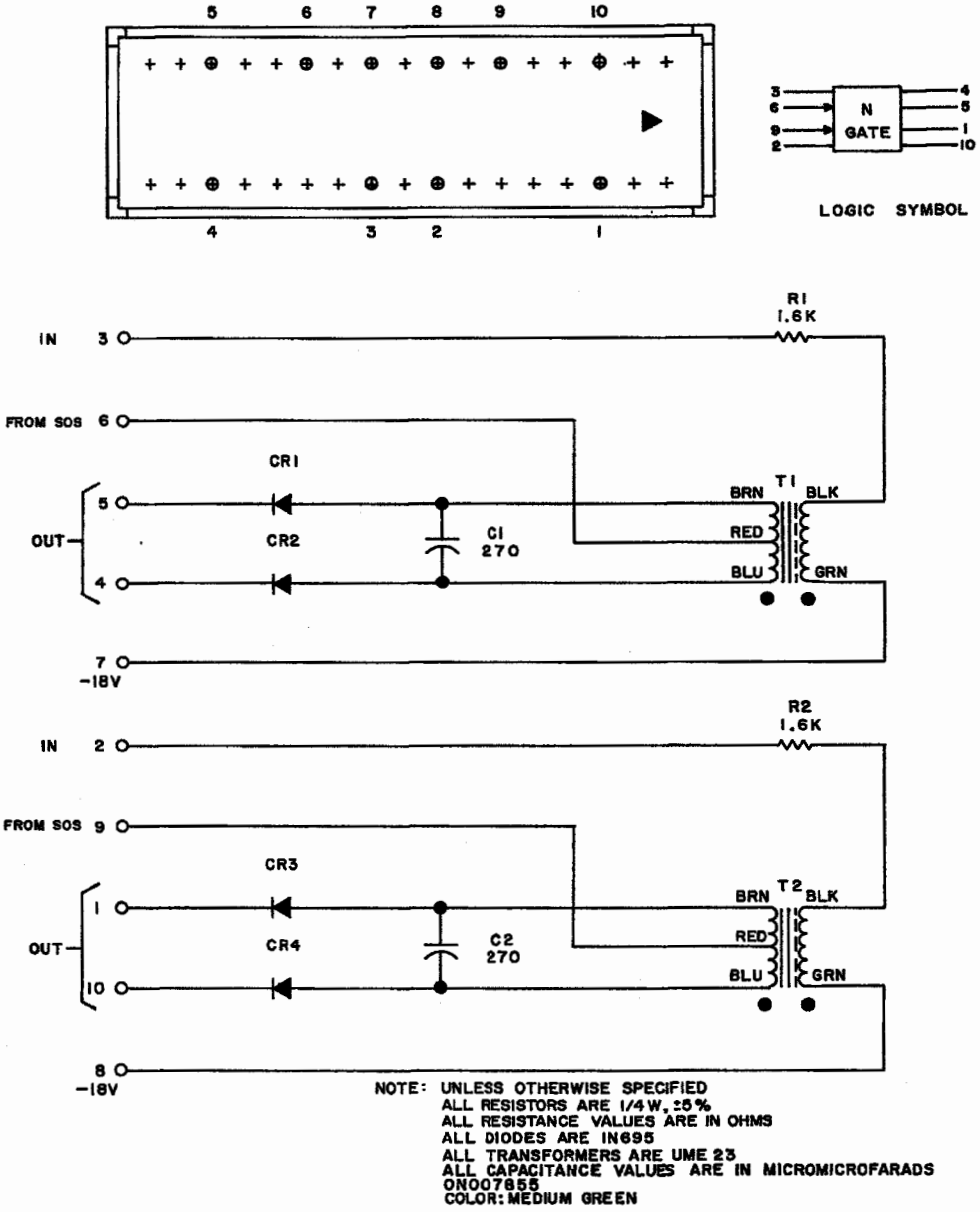


Figure 4-50.—Noise Gate, Module Schematic Diagram.

sending KW-7. The gated counter consists of flip-flop A7-11 and NOR gates A7-10A and A7-10B.

(a) First, consider how the gated counter would operate if inputs 5 and 6 of A7-10A and inputs 9 and 10 of A7-10B are held at ZERO. Under these conditions, A7-11 and the two NOR gates operate as an ordinary complementing ÷ 2 counter, delivering a 25-kc signal to A7-12.

(b) Next, consider the operation when the KW-7 is in the send mode. As soon as the 5 KC SLOW RESET becomes a ONE, the output of A7-9B goes to ZERO, and the output of A7-9A goes to ONE, enabling input 7 of A7-8 and allowing 50 kc to set A7-8 to ZERO. This places a ZERO enable on input 6 of A7-10A and input 10 of A7-10B. Referring to the waveform chart shown in figure 4-51, it is seen that ten 50 kc pulses occur during the interval from t_1 to t_3. During this same interval, A7-9B outputs a ONE for the first 20 microseconds, from t_1 to t_2, which disables A7-10A and A7-10B, and prevents the first 50 kc pulse from triggering A7-11. From t_2 to t_3, A7-10A and A7-10B are again enabled, allowing A7-11 to operate as a complementing ÷ 2 counter for the next nine 50-kc pulses. At t_3, the output of A7-9B again goes to ONE, preventing the eleventh 50-kc pulse from triggering A7-11. Thus A7-11 is prevented from responding to every tenth 50 kc pulse. In one second, therefore, A7-11 would be triggered 45,000 times, and would be prevented from triggering 5,000 times. The output frequency is then 45,000 divided by two, or 22,500 cps. This frequency does not change as long as the KW-7 is sending, since there are no $\overline{\text{LINE IN}}$ transitions available to trigger A7-8 or A7-16, which in turn would alter the countdown cycle.

(c) Finally, consider the gated counter operation when th KW-7 is in receive mode. At this time the counter is used to provide a variable countdown of the 50-kc signal in order to achieve and maintain exact synchronism between the local clock and the 22.5-kc clock in the sending KW-7. Synchronism, or lack of synchronism, is detected by using two sample signals, START·$\overline{\text{OBR1}}$ and OBR·BIT1, to examine the stop-start transitions of the $\overline{\text{LINE IN}}$ signal. START·$\overline{\text{OBR1}}$ lasts for one-half baud and occurs immediately before the predicted time of occurrence of the stop-start $\overline{\text{LINE IN}}$ transition. OBR·BIT1 begins at the end of the above time, and lasts for one-half baud after the predicted time of occurrence of the start-stop $\overline{\text{LINE IN}}$ transmission. If the line in STOP-START transition occurs during START·$\overline{\text{OBR1}}$, the receiver clock is running too slow and must be speeded up. Conversely, if the $\overline{\text{LINE IN}}$ STOP-START transition occurs during OBR·BIT1, the receiver clock is running too fast and must be slowed down. When $\overline{\text{LINE IN}}$ stop-start transition occurs exactly at the partition between the two time periods the receiving KW-7 is in sync with the sending KW-7.

(d) Slow phase correction, or a speedup in the local clock frequency, is accomplished in the following manner. First, observe that with the absence of $\overline{\text{LINE IN}}$ information, A7-16 is always in the ZERO state, SLOW is a ZERO enable on input 7 of A7-9B, and the output of A7-9B is a ONE when A7-1 and A7-4 are in the ZERO state (that is, for 20 microseconds out of every 200 microseconds). In order to speed up the local clock, the output of A7-9B must be kept at ZERO during this 20-microsecond interval. Now, if the local clock is lagging the sending clock, the stop-start transition of $\overline{\text{LINE IN}}$ occurs during the interval preceding the predicted time, setting A7-16 to ONE. A7-16 drives the output of A7-9B to ZERO, enabling input 5 of A7-10A and input 9 of A7-10B; A7-9B also drives the output of A7-9A to ONE enabling input 7 of A7-8. 50 kc sets A7-8 to ZERO, placing a ZERO enable on input 6 of A7-10A and input 10 of A7-10B. With inputs 5 and 6 of A7-10A and 9 and 10 of A7-10B now enabled, A7-11 then operates as a complementing counter.

(e) Fast phase correction, or a slowdown in the local clock frequency, is accomplished in the following manner. If the local clock is leading the sending clock, the stop-start transition of $\overline{\text{LINE IN}}$ occurs during the OBR·BIT1, time interval setting A7–8 to ONE. The ONE output of A7–8 disables A7–10A and A7–10B, stopping A7–11. In order to restart A7–11, the output of A7–9B must be ZERO, as it will be, on the average 90 percent of the time. Assuming the output of A7–9B is ZERO, A7–9A enables input 7 of A7–8, the next 50 kc pulse resets A7–8 to ZERO, and A7–11 resumes counting. If A7–9B is a ONE A7–8 will not be reset to ZERO until the first 50 kc pulse after A7–9B goes to a ZERO. This assures the normal deletion pulse.

(4) *Variable counter.*—The nominal 22.5 kc signal from A7–11 is applied to stage A7–12, where it is divided by two, giving 11.25 kc. This 11.25 kc signal is applied to a variable counter composed of flip-flops A7–14, A7–7, A7–6, A7–5, and AND gates A7–13C, A7–13D, A7–13E and A7–13F. The variable counter divides its input frequency by 10, 9, or 6, depending upon the setting of WPM SPEED SELECTOR switch S7. With S7 set to 60 WPM, gates A7–13C and A7–13F are disabled, while A7–13D and A7–13E are enabled. When output 3 of A7–5 goes from ZERO to ONE, a reset pulse is fed via gates A7–13D and A7–13E, to flip-flops A7–7 and A7–6. This action deletes six counts from the total, permitting operation as a ÷ 10 counter. The output frequency under these conditions will be 11.25 kc divided by 10, or 1125 cps. If S7 is set to 67 WPM, gates A7–13C, A7–13D, and A7–13E are enabled. When output of A7–5 goes from ZERO to ONE, a reset pulse is fed via gates A7–13C, A7–13D, and A7–13E, to flip-flops A7–14, A7–7, and A7–6. This deletes seven counts from the total, permitting operation as a ÷ 9 counter, and giving an output frequency of 11.25 kc divided by 9, or 1250 cps. If S7 is set to 100 WPM, gates A7–13D, A7–13E, and A7–13F are enabled. When output 3 of A7–6 goes from ZERO to ONE, a reset pulse is applied via gate A7–13F to input 4 of A7–5, causing output 3 of A7–5 to go from ZERO to ONE. A second reset pulse is now applied via gates A7–13D and A7–13E, to flip-flops A7–7 and A7–6. This action deletes ten counts from the total, permitting operation as a ÷ 6 counter. The output frequency is now 11.25 kc divided by 6, or 1875 cps.

b. Input Counter Circuit (fig. 4–52).—The input bit rate and character counter controls the generation of the IBR and IC7 pulses. These pulses are used to sample the input information bit rate and character rate. The input bit rate and character counter is divided into two logical functions; the generation of the IBR (input bit rate) and the generation of the IC7 (input character) pulses. The following discussion considers each function separately.

(1) *Input bit rate counter.*—The input bit rate counter is comprised of a five-stage counter (flip-flops A8–1 through A8–5) and three AND gates (A8–13A through A8–13C). Each flip-flop, when changing state from ZERO to ONE, generates a pulse which triggers the following flip-flop; transitions from ONE to ZERO have no effect. Without the AND gates, the counter would divide by 32. The AND gates, however, apply feedback which causes the counter to divide by 25. An initial count of 11011, reading from left to right, is inserted into the counter by a MISS pulse applied to pin 6 of A8–3 and to pin 12 of A8–1, A8–2, A8–4, and A8–5. Each clock pulse applied to A8–1 deletes one count from the total. After 11 clock pulses have been applied to A8–1, the count is 00001. After 12 clock pulses, the count is 11110. The transition of A8–5 from ONE to ZERO drives $\overline{\text{IBR1}}$ from ZERO to ONE, causing AND gates A8–13A through A8–13C to reset A8–1, A8–2 and A8–3. This deletes seven counts, dropping the total from 11110 to 00010. Counting continues until 25 clock pulses have been applied to A8–1, at which time the counter is back to its original state, 11011.

(2) *Input character counter.*—The input character counter, consisting of flip-flops A8–6, A8–7, A8–14, AND gates A8–13D, A8–13E, and NOR gate A8–16B, is a three-stage

counter which generates the input character pulses (IC7); an additional function is the generation of gating signals for the input counter set generator. The input character counter must divide the IBR frequency by 8, that is, generate an 8-bit IC7 pulse, at all times except when the equipment is receiving information from the sending teletypewriter during send normal operation, during indicator, and plain asynchronous modes. Under the latter conditions, the counter divides the IBR frequency by 6 to generate a 6-bit IC7 pulse. The ÷ 8 and ÷ 6 operations are performed in the following manner. When an 8-bit character is to be generated, the MOD 6 and PA signals applied to gates A8–13D and A8–13E are ZEROS, and both gates are disabled. A8–6, A8–7, and A8–14 now operate as a conventional divide-by-eight counter, and an 8-bit IC7 pulse appears at output 10 of A8–14. A 6-bit character will be generated, when the CIPHER-PLAIN-REMOTE switch is set to PLAIN ASYNCHRONOUS mode and also when data is present in the send normal mode. When either the MOD 6 or PA signal is ONE, A8–13D or A8–13E will be enabled. Each time output 3 of A8–14 goes from ZERO to ONE, a pulse is applied to input 4 of A8–7. This pulse resets A8–7, deletes two counts from the total, and produces a 6-bit character at output 10 of A8–14. NOR gate A8–16B outputs a ONE to the receive phasing P&I indicator and set generating circuit when both inputs are ZERO. The input counter set generator in turn generates a MISS pulse which resets all stages in the input bit rate and input character counters. The action is shown in a timing diagram located on figure 4–52.

c. *Output Counter Circuit (fig. 4–53).*—The output counter logic generates the following timing pulses: OBR (output bit rate), OBR1, OBR2, $\overline{\text{OBR1}}$, CTRP (output character rate), $\overline{\text{CTRP}}$, $\overline{\text{CTRP1}}$, START, $\overline{\text{START}}$, STOP, $\overline{\text{OBR·BIT1}}$, P, $\overline{\text{P}}$, Pd, and $\overline{\text{Pd}}$. The circuit consists of the output bit rate counter, the output character counter, the start and stop generators, the $\overline{\text{OBR·BIT1}}$ generator, the P pulse generator, and the Pd pulse generator.

(1) *Output bit rate counter.*—The output bit rate counter is used to retime the 7.42 baud input data into 7.0 baud output data. The output bit rate counter is a five-stage counter comprising flip-flops A10–1 through A10–5 and AND gates A10–9A through A10–9C. Without the AND gates, the counter would divide the CLOCK frequency by 32, however, the AND gates feed reset pulses back to the first three stages, deleting seven counts for an overall division ratio of $32-7=25$, The seven pulses are deleted in two separate steps, as follows. A SET pulse sets the counter to an initial count of 00111 (decimal 28). Each CLOCK pulse applied to A10–1 deletes one count from the total. After 12 CLOCK pulses have been applied to A10–1, the counter contains a count of $28-12=16$. Sixteen expressed in binary form is 00001, which indicates that A10–1, A10–2, A10–3, and A10–4, are in the ZERO state, and A10–5 is in the ONE state. The thirteenth CLOCK pulse reduces the count to 15(11110), at which time A10–5 goes from the ONE state to the ZERO state. This causes the $\overline{\text{OBR1}}$ output of inverter A10–11 to go from ZERO to ONE, resetting A10–3 to ZERO via AND gate A10–9C. With A10–3 reset to ZERO, four counts are deleted from the total, leaving a count of $15-4=11$ (11010). The counter now counts normally for the next 11 CLOCK pulses until zero (00000) is reached. The next CLOCK pulse sets A10–1 through A10–5 to ONE. The total count is now 31 (11111). However, this condition can only exist momentarily, because the ZERO-to-ONE transition of A10–5 causes the input to inverter A10–10A to go from ONE to ZERO. The OBR2 output of A10–10A goes from ZERO to ONE, resetting A10–1 and A10–2 to ZERO via AND gates A10–9A and A10–9B. With A10–1 and A10–2 reset to ZERO, three counts are deleted, giving a count of $31-3=28$ (00111). This is the same condition that existed when the count down started, so that the cycle is now ready to be repeated. The counter output signal OBR (output bit rate) is, as described previously, 1/25 the CLOCK frequency.

(2) *Output character counter.*—During send phasing, each input character consists of 8 bits. At all other times, it consists of 7 bits (start bit, 5 information bits, stop bit). Therefore, the output character counter (flip-flops A10–6, A10–7, and A10–14, plus AND gate A10–9D) must divide the frequency of the OBR signal send by 7 during indicator and normal and by 8 at all other times.

(a) During phasing, the I&N signal on input 19 of AND gate A10–9D is a ZERO disable which allows A10–6, A10–7 and A10–14 to operate as an ordinary ÷ 8 counter.

(b) During indicator and normal, I&N is a ONE enable. A SET pulse sets the counter to an initial count of 5 (101), (reading from left to right). The first OBR pulse deletes one count from the total, leaving 4 (001). The second OBR pulse deletes another count, leaving 3 (110). This condition, however, is unstable because A10–14, in going from the ONE state to the ZERO state, applies a reset pulse to A10–6 via AND gate A10–9D. With A10–6 reset to ZERO, one count is deleted, leaving a count of 2 (010). After two more OBR pulses, the counter contains a count of zero (000). The next OBR pulse sets A10–6, A10–7, and A10–14 to ONE, giving a count of 7 (111). The next two OBR pulses delete two counts, leaving 5 (101). The counter is now back to its initial state, ready for another cycle. The counter output, CTRP, is inverted by A10–21A to form the $\overline{\text{CTRP1}}$ signal which is applied to the TD step circuit.

(3) *Start generator.*—The start generator A10–12A produces a START pulse during the first bit of each character. The START pulse is required during send cipher operation to prevent encipherment of the start baud of each character. Inputs to A10–12A are $\overline{\text{OC5}}$, $\overline{\text{OC6}}$, and $\overline{\text{CTRP1}}$. The waveform chart shown in figure 4–53 indicates that during a given countdown cycle these three signals are simultaneously ZERO only for the duration of one bit. A10–12B inverts the START pulse to produce a $\overline{\text{START}}$ pulse which is used for phase correction.

(4) *Stop generator.*—Similarly, stop generator A10–13A produces a STOP pulse during the last bit of each character to prevent encipherment of the stop baud. Inputs to A10–13A are $\overline{\text{OC5}}$, $\overline{\text{OC6}}$, and $\overline{\text{CTRP}}$. The waveform chart indicates that these signals are simultaneously ZERO only for the duration of one bit; however, this condition occurs seven bits later than the START pulse.

Note: The two preceding paragraphs describe the generation of the START and STOP pulses during indicator and normal. During phasing, the START and STOP pulses are generated in a similar manner, but the STOP pulse occurs eight bits later than the START pulse.

(5) *$\overline{\text{OBR}}$·BIT1 generator.*—During receive operation, the $\overline{\text{OBR}}$·BIT1 pulse is used in conjunction with the START $\overline{\text{OBR1}}$ pulse (refer to phase correction circuit) to sample the stop-start transitions of the incoming data (LINE IN), comparing the actual time of occurrence with the predicted time of occurrence. If the two times are not coincident, the phase correction logic generates an appropriate correction signal. As illustrated below, the sample interval is divided into two periods. The first period, from t_1 to t_2, is determined by START $\overline{\text{OBR1}}$, while the second period, from t_2 to t_3, is determined by OBR·BIT1. The predicted time of occurrence of the $\overline{\text{LINE IN}}$ stop-start transition is at t_2. If the transition occurs at this time, the receiving KW–7 is in the sync with the sending KW–7, and no phase correction is necessary. However, if the transition occurs between t_1 and t_2, the receiving KW–7 is lagging the sending KW–7, and the phase correction logic increases the local clock frequency. Conversely, if the transition occurs between t_2 and t_3, the receiving KW–7 is leading the sending KW–7, and the phase correction circuit reduces the local clock frequency. The $\overline{\text{OBR}}$·$\overline{\text{BIT1}}$ generator (A10–13B and A10–10C) generates the $\overline{\text{OBR}}$·$\overline{\text{BIT1}}$ pulse which occurs immediately after the end of the START pulse, and lasts for half the duration of one bit. Inputs to NOR gate A10–13B are, OC5, $\overline{\text{OC6}}$, and $\overline{\text{CTRP1}}$. The waveform

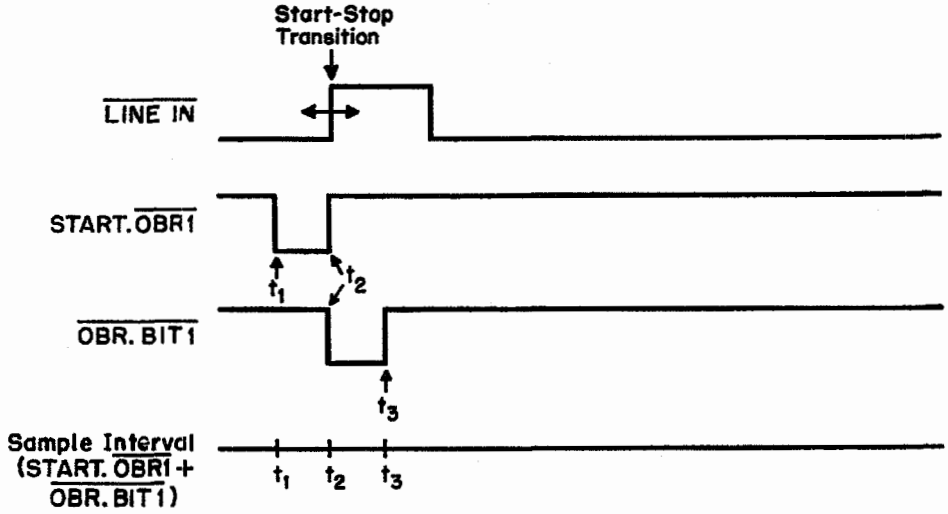


chart in figure 4–53 shows that these signals are simultaneously ZERO when, OC5 = ZERO, OC6 = ONE, and CTRP = ONE. During this interval, that is, during the first half of the first bit, A10–13B places a ONE on input 9 of inverter A10–10C which in turn produces a ZERO $\overline{OBR \cdot BIT1}$.

(6) *P pulse generator.*—The P pulse generator (A10–9E and A10–20) generates a P pulse at the start of each character unless a break condition exists. This pulse occurs after the stop bit of each character, and is used to reset various flip-flops in the send phasing logic and the send and shift transfer circuit. The $\overline{BREAK}$ signal on input 20 of AND gate A10–9E is a ONE enable if no break has occurred. Each time CTRP goes from ZERO to ONE, A10–9E produces a ONE pulse which triggers one-shot multivibrator A10–20. A10–20 produces a P pulse which has a duration of 34 microseconds. A10–20 is prevented from producing a P pulse during SET 1 by a ONE applied to input 8 via truncated diode A10–10B; a P pulse at this time would establish undesired conditions in other portions of the extensor and control. Inverter A10–21B inverts the P pulse to produce $\overline{P}$.

(7) *Pd pulse generator.*—The Pd pulse generator (A10–9F and A10–19) produces a Pd pulse which occurs immediately after the end of the $\overline{P}$ pulse. The Pd pulse is used to trigger circuits in the send and shift transfer logic which, because of transfer delays, cannot be triggered by P. At the end of the P pulse, when the P is going from ZERO to ONE, AND gate A10–9F produces a ONE pulse which triggers one-shot multivibrator A10–19. A10–19 generates a Pd pulse having a ONE duration of 34 microseconds. Inverter A12–16 inverts Pd to produce $\overline{Pd}$.

d. Phase correction circuit (fig. 4–54).—The phase correction circuit corrects any difference in frequency between the time standard in the receiving KW–7 and the time standard in the transmitting KW–7. The circuit is composed of the slow test gate, the slow phase detector, the fast test gate, and the fast phase detector.

(1) *Slow test gate.*—If the local KW–7 timing is lagging the sending KW–7, slow test gate A7–15B will produce a SLOW GATE (SG) pulse for one-half the duration of the START bit of each character during indicator and normal operation, (receive mode). A7–15B has the following inputs: $\overline{I\&N}$ (ZERO at all times except during phasing); SEND 1 (ZERO during receive); $\overline{START}$ (ZERO during start bit of each character); and OBR1

(ZERO for one-half the duration of a bit). When all four inputs are simultaneously ZERO, A7-15B delivers a ONE SG pulse to the slow phase detector.

(2) *Slow phase detector.*—The SG level from A7-15B enables input 2 of slow phase detector A7-16. If a LINE IN pulse occurs while SG is present, slow phase detector A7-16 is triggered to the state where output 3 (SLOW) is a ONE. This condition prevails until A7-16 is reset by the next SLOW RESET pulse from the clock pulse generating circuit.

(3) *Fast test gate.*—Fast test gate A7-15A is enabled by I&N and $\overline{\text{SEND 1}}$ only during indicator and normal phases of receive operation. A7-15A places a ONE enable on input 2 of fast phase detector A7-8 during OBR·BIT1, which is a ZERO for one-half baud after the predicted time of occurrence of the LINE IN stop-start transition. If the receiving KW-7 clock is leading the sending KW-7 clock, the LINE IN transition will occur while the A7-15A output is ONE, setting A7-8 to ONE.

(4) *Fast phase detector.*—If a LINE IN stop-start transition occurs while FAST GATE is present on input 2 of fast phase detector A7-8, it is switched to the ONE state at output 3 (FAST) is a ONE. This condition prevails until A7-8 is reset by the next 50 KC fast reset pulse from the clock pulse circuit, unless input 7 is inhibited by a ZERO ÷ 10 DELETION pulse from the clock pulse circuit.

e. *Data Input Circuit (fig. 4-55).*—The data input circuit allows the LOOP IN signal from the loop input circuit, or LINE IN signal from the line input circuit, to be fed to the key generator, data extensing logic, and send normal logic. The circuit is composed of loop input gate and the line input gate.

(1) *Loop input gate.*—The loop input gate allows the loop input signal LOI2 from the local teletypewriter to be fed to the input gate during normal send operation, if phasing characters from another KW-7 have not been detected. The loop input gate consists of the loop input integrator A11-15, Schmitt trigger A11-8, NOR gate A11-20A, inverter A11-20B, and NOR gate A11-9.

(a) Input signals to NOR gate A11-20A are $\overline{\text{PC0}}$, $\overline{\text{PC1}}$ and $\overline{\text{SEND 1}}$; $\overline{\text{PC0}}$ and $\overline{\text{PC1}}$ are both ZERO when the phasing counter is inactive, that is, when no phasing information is being received from another KW-7. $\overline{\text{SEND 1}}$ is ZERO during send operation. Therefore, when these two conditions are met, A11-20A transfers a ONE to inverter A11-20B, which in turn places an $\overline{\text{SLE}}$ ZERO enable on input 7 of A11-9. Input 10 to A11-9, $\overline{\text{NORMAL 3}}$, is a ZERO enable during normal operation. The PTS line on input pin 3 of A11-9 will be a ZERO as long as LOI2 data is actively triggering the loop input circuit. If loop input data stops, a 10 second delay occurs before the PTS signal becomes a ONE to inhibit NOR gate A11-9, forcing the LOIG output to a ZERO.

(b) Teletypewriter signal LOI2 is applied to loop input integrator A11-15, which removes spike sand spurious voltages from the LOI2 signal. The output of A11-15 is shaped into rectangular LOIST pulses by Schmitt trigger A11-8. These pulses are applied to one input of NOR gate A11-9. If $\overline{\text{SLE}}$, $\overline{\text{NORMAL 3}}$, and PTS are all ZERO, A11-9 transfers LOIG directly to NOR gate A8-18A, and also through the LOOP OUTPUT INHIBITOR switch S8 (in the ALLOW position) to NOR gate A11-3B. If the loop output is not desired (i.e. when the two-wire loop adapter unit is being used) the LOOP OUTPUT INHIBITOR switch will open the circuit when placed in the INHIBIT position.

(c) NOR gate A8-18A passes either loop information or line information. The operation of the data input circuit is such that either the LOIG or LINE IN signal, but not both, can exist at the input of A8-18A. The reason for this is that the start baud of the LOIG signal sets MOD 6 flip-flop to a ONE, (fig. 4-62) which disables NOR gate A8-17B. This prevents generation of the LINE IN signal and places a ZERO enable on input 6 of A8-18A. Under these conditions, ABIN consists of

loop information. MOD 6 remains ONE until the end of the last LOIG information baud, at which time it returns to ZERO and remains at that level until the start baud of the next LOIG character. If there is no loop activity, LOIG is a constant ONE which places a ONE disable on input 9 of NOR gate A11–9. This drives the output of A11–9 to ZERO, placing a ZERO enable on input 7 of A8–18A. ABIN now consists of line information from A8–17B. Inverter A8–18B inverts ABIN to form $\overline{\text{ABIN}}$.

(d) NOR gate A11–3B controls the flow of information which is used to generate local copy. In normal send operation, MOD 6 is ONE during the start and information bauds of each LOIG character. This ONE drives the output of gate A11–3A to ZERO, enabling input 10 of A11–3B. The LOIG signal applied to input 9 of A11–3B now generates the GATED LOOP IN signal which is fed to the loop output logic for printing out local copy. However, if the KW–7 is operating in the receive plain asynchronous mode, the LIIST signal will be 7.42 baud asynchronous instead of the normal 7.0 baud synchronous. This signal does not have to be deciphered, and after synchronization by NSC flip-flop A11–18, can be fed to the local page printer without further processing. During receive plain asynchronous operation, the LOIST signal on input 9 of A11–9 is a ONE. This ONE results in a ZERO enable on input 9 of A11–3B. The $\overline{\text{PA}}$ and MOD 6 inputs to A11–3A are both ZERO, permitting the 7.42 baud asynchronous LIIST signal to be inverted and applied to input 10 of A11–3B. A11–3B inverts the signal and feeds it to the loop output circuit for generation of local copy.

(2) *Line input gate.*—The LINE IN signal is gated through the line input gate circuit by NOR gate A8–17B, during send normal operation, unless information is being received from the local teletypewriter. If the local teletypewriter is sending an input, the MOD 6 signal is a ONE, which inhibits the line input gate. During send phasing and indicator periods MOD 6 is a ZERO enable signal, but NOR gate A8–17B is then inhibited by a ONE $S \cdot \overline{N}$ signal.

(a) The line input gate circuit is composed by NOR gate A11–3A, nonsynchronous control flip-flop A11–18, NOR gates A8–15, A8–17A, and A8–17B. The MOD 6 signal is a ZERO enable during all receive operations, during send phasing and send indicator, and during send normal operation only is no information is being sent by the local teletypewriter. Thus the MOD 6 ZERO signal enables NOR gates A11–3A and A8–17B. The NORMAL 3 signal on input 5 of A8–17A is a ONE during normal operation, placing a ZERO $S \cdot \overline{N}$ enabling signal on pin 7 of A8–17B during send normal operation. The $\overline{\text{SEND 3}}$ signal on input 6 of A8–17A becomes a ONE during all receive operations placing a ZERO $S \cdot \overline{N}$ enabling signal on pin 7 of A8–17B. Thus the MOD 6 signal and the $S \cdot \overline{N}$ signal enable NOR gate A8–17B to gate LIIST through and produce the $\overline{\text{LINE IN}}$ signal which is applied to the phase correction circuit, the clock pulse generating circuit, the receive phasing circuit and to NOR gate A8–18A. Since LOIG is a constant ZERO (in the absence of loop activity) pin 7 of A8–18A will be enabled. Therefore, the $\overline{\text{LINE IN}}$ signal will be gated through A8–18A to produce ABIN data signals and $\overline{\text{ABIN}}$ (through NOR gate A8–18B) for application to other circuits throughout the KW–7. The $\overline{\text{LINE IN}}$ signal will be gated in the manner just described during all receive operations (except plain asynchronous) and during send normal providing no local teletype input is being applied.

(b) During receive plain asynchronous operation, LIIST is gated through A11–3A by the MOD 6 ZERO and $\overline{\text{PA}}$ ZERO signals which enable A11–3A. At this time the PA ONE signal inhibits A8–17B preventing occurrence of $\overline{\text{LINE IN}}$ at the output of A8–17B. The first bit of LIIST which passes through A11–3A, sets a ZERO into non-synchronous flip-flop A11–18. The ONE $\overline{\text{NSC}}$ signal produced on pin 3

of A11–18 is sent to the receive phasing circuit where it causes a MISS pulse to be generated. This, in turn, sets the input counter in synchronization with the input character. The input counter (fig. 4–52) counts for one character time. When LIIST was gated through A11–3A, besides setting a ZERO into A11–18 it also was applied to pin 10 of A11–3B. NOR gate A11–3B was previously enabled by a constant ONE LOIG on pin 9. Therefore LIIST passes through A11–3B as gated loop in data for application to the loop output circuit. The input counter generates IBR pulses which synchronize the transfer of data through the loop output circuits to the page printer. After one character time has elapsed the input counter generates an IC7 signal which sets non-synchronous flip-flop A11–18 back to ONE. As each teletypewriter character is received asynchronously, the circuit operation just described is repeated while in receive plain asynchronous mode.

f. Send Phasing Circuit (fig. 4–56).—The send phasing circuit generates the SEND levels which are used within the KW–7. This circuit also energizes the SEND indicator lamp when the KW–7 is in the SEND mode of operation. The send phasing circuit is composed of the following: the SEND switch, toggle flip-flop A6–7, NOR gate A6–20, send flip-flop A6–5, BG flip-flop A6–6, AND gate A6–11, power inverters A6–12, A6–13A, and A6–13B, lamp driver A11–19, and inverter A11–5.

(1) Prior to the initiation of send operation, flip-flops A6–7 and A6–5 have been set to the ZERO state by a POWER SET pulse via diodes A6–16A and A6–16B. Send operation is initiated by depressing the SEND switch, placing a ONE enable on input 7 of toggle flip-flop A6–7. The next P pulse sets A6–7 to the ONE state, placing a ONE enable on input 7 of send flip-flop A6–5, and on input 1 of BG flip-flop A6–6; since the BG flip-flop has already been set to the ZERO state by a SET pulse the BG ZERO disable remains on input 2 of A6–5.

(2) Meanwhile, the output counter is counting continuously. As soon as the output counter reaches the state where OC6 and $\overline{\text{CTRP}}$ are both ZERO, NOR gate A6–20 outputs a ONE to input 8 of send flip-flop A6–5, setting A6–5 to the ONE state. A6–5 generates a ONE which is applied to the indicator control logic and to input 7 of BG flip-flop A6–6. The SEND button is now released, after five seconds, placing a ONE enable on input 2 of A6–7. The next P pulse resets A6–7 to the ZERO state, giving a ZERO-to-ONE transition at output 3 of A6–7. This sets the BG flip-flop to the ONE state, placing a ONE enable on input 2 of A6–5; the ONE enable is necessary for the generation of a SET signal in case phasing must be re-initiated at some later time.

(3) The SEND ONE condition brought about by the sequence described above prevails until, 1) a POWER SET signal occurs, as might be caused by an alarm or break condition or, 2) the KW–7 detects four phasing characters on its line-in circuit. In the latter case, a LIG (lock in gate) signal appears at input 16 of AND gate A6–11. This signal resets A6–5 to the ZERO state, and sets the SEND signal to ZERO. The local KW–7 automatically is shifted from send to receive operation.

(4) SEND is inverted by power amplifier A6–12 to from $\overline{\text{SEND 1}}$. $\overline{\text{SEND 1}}$ in turn is inverted by power amplifier A6–13A to form SEND 2.

(5) $\overline{\text{SEND}}$ is inverted by power amplifier A6–13B to form SEND 1. The latter signal is inverted by inverter A11–5 to form $\overline{\text{SEND 2}}$.

(6) During send operation, the $\overline{\text{SLE}}$ signal from the data logic is a ZERO. This gives a ONE at pin 4 of lamp driver A11–19, energizing the SEND lamp and a ZERO at pin 12 energizing the remote send lamp.

g. Receive Phasing, P&I Indicator, and MISS Pulse (Counter Set) Generating Circuit (fig. 4–51).—The receive phasing, P & I indicator, and counter set generating circuit performs three major functions. It synchronizes the timing of the receiving KW–7 to the timing of

the sending KW-7, provides a visible indication to show when the KW-7 is operating in the phasing or indicator modes of operation, and generates MISS pulses which reset the input counter. The logic is composed of receive phasing circuit, the P&I indicator circuit, and the MISS pulse generating circuit.

(1) *Receive phasing circuit.*—The receive phasing logic synchronizes the timing of the receiving KW-7 to the timing of the send KW-7. The circuit is made up of the T8 generator, the phasing drive generator, and the phasing counter.

(a) T8 generator.—The T8 generator (flip-flop A8-8) produces T8 pluses having a pulse width of 9/25 of a baud at the frequency of the input character pulses. These pulses are used during receive phasing to establish synchromisim between the receiving KW-7 and the sending KW-7. In order to synchronize, the timing of the input counter is shifted until T8 brackets the stop-start transition of the $\overline{\text{LINE IN}}$ signal. The IC7 input character pulses from the input character counter are applied to flip-flop A8-8 setting A8-8 to the ONE state. The $\overline{\text{IC0}}$ output of input bit rate counter is applied to the input of A8-8 while the $\overline{\text{IC3}}$ output of the input bit rate counter is applied to input 2 of A8-8. A8-8 is reset when the $\overline{\text{IC0}}$ and $\overline{\text{IC3}}$ outputs of the bit rate counter are ONES. Since this occurs after a count of nine clock pulses, the pulse width of the T8 pulse is 9/25 of a baud. The IC7 signal applied to input 8 resets A8-8 to its initial state. The T8 pulses are fed to the phasing drive generator, while the $\overline{\text{T8}}$ pulses are fed to the send normal logic.

(b) Phasing drive generator.—The phasing drive generator (flip-flop A8-9) detects the coincidence of the stop-start transition of the $\overline{\text{LINE IN}}$ characters with the T8 pulses from the T8 generator. If the stop-start transition occurs during the T8 pulse, the phasing drive generator produces a logical ZERO PHASING DRIVE pulse and a logical ONE $\overline{\text{PHASING DRIVE}}$ pulse. However, if the stop-start transition does not occur during T8, the phasing drive generator produces a logical ZERO $\overline{\text{PHASING DRIVE}}$ pulse and a logical ONE PHASING DRIVE pulse. The T8 output of the T8 generator is applied to flip-flop A8-9. Since input 2 is grounded, the flip-flop goes to the ONE state. The LINE IN signal is applied to input 8 of the flip-flop. If the logical ONE start bit of the $\overline{\text{LINE IN}}$ character occurs during the logical ONE T8 signal, A8-9 will be reset to the ZERO state. However, if the start bit of the $\overline{\text{LINE IN}}$ character does not occur during T8, the flip-flop will remain in the ONE state. The output from the ONE side of the flip-flop is applied to AND gate A8-21B. The other input to A8-21B is the $\overline{\text{IC7}}$ input character pulse. If flip-flop A8-9 remains in the ONE state when the $\overline{\text{IC7}}$ input character pulse is applied, A8-21B will produce a logical ONE output. However, if A8-9 is in the ZERO state when the $\overline{\text{IC7}}$ input character pulse is applied, A8-21B will produce a logical ZERO output since it is inhibited by a logical ZERO signal from the flip-flop. A ONE pulse from A8-21B triggers one-shot multivibrator A8-20. The pulse output from A8-20 is applied to set driver A8-19, which delivers a MISS pulse to the input control circuit and to the receive phasing circuit. The MISS pulse resets the T8 generator and the phasing drive generator to their initial states.

(c) Phasing counter.—The phasing counter is a conventional two-stage flip-flop counter which consists of A8-10 and A8-11. The phasing counter divides the PHASING DRIVE pulses by four. The two flip-flops are connected so that the output from the one side of A8-10 is used as a trigger input to A8-11. When the first $\overline{\text{PHASING DRIVE}}$ pulse triggers flip-flop A8-10, it goes to the ZERO state. Therefore, the trigger pulse applied to A8-11 will be a logical ZERO and have no effect on the flip-flop. When the second $\overline{\text{PHASING DRIVE}}$ pulse triggers A8-10, the flip-flop goes to the ONE state. This action produces a logical ONE trigger pulse which sets A8-11 to ZERO. A8-10 and A8-11 continue to change state

whenever triggered by a logical ONE trigger pulse. However, each flip-flop must be triggered twice to produce a logical ONE output. Therefore, four logical ONE $\overline{\text{PHASING DRIVE}}$ pulses are necessary for the PC1 output of the second stage of the flip-flop to be a logical ONE.

(2) *MISS pulse generating circuit.*—The MISS pulse generating circuit, composed of inverter A8–15A, AND gates A8–21A through A8–21E, one-shot multivibrator A8–20, and set driver A8–19, produces a MISS pulse which resets the input counter and receive phasing logic. AND gates A8–21A through A8–21E have a common output, which is applied to one-shot multivibrator A8–20. This arrangement permits triggering A8–20 when any one of the following conditions is realized:

(a) AND gates A8–21C, A8–21D, and A8–21E are permanently enabled by the ground connection to inputs 8, 20, and 18 respectively; therefore one-shot A8–20 will be triggered by a ZERO-to-ONE transition of the non-synchronous control flip-flop, a POWER SET pulse, or a ZERO-to-ONE transition of $\overline{\text{FL}}$.

(b) AND gate A8–21A aids in detection of phasing in the following manner. If the receiving KW–7 is in synchronism with the sending KW–7, IC6 and IC7, from the input character counter, will always be ONE's during the ZERO-to-ONE transition of the $\overline{\text{LINE IN}}$ signal. This condition will place a ONE on the input of inverter A8–15A, and a ZERO disable on input 15 and AND gate A8–21A. With A8–21A disabled, the ZERO-to-ONE transition of the $\overline{\text{LINE IN}}$ signal is prevented from triggering one-shot A8–20, no MISS pulse is generated to reset the phasing counter, and the phasing counter continues counting phasing characters. However, if the receiving KW–7 is not in synchronism with the sending KW–7, either IC6 or IC7 will be a ZERO during the ZERO-to-ONE transition of the $\overline{\text{LINE IN}}$ signal, placing a ZERO on the input of A8–15A. This will place a ONE enable on input 15 of A8–21A. With A8–21A enabled, the ZERO-to-ONE transition of the $\overline{\text{LINE IN}}$ signal triggers one-shot A8–20. A8–20 generates a MISS pulse which resets the input character counter to 111. This shifts the input character counter timing so that the next $\overline{\text{LINE IN}}$ transition will occur during T8 time, which is the condition required for synchronism.

(c) AND gate A8–21B resets the phasing counter if phasing is started but not completed. Assume that only one legitimate phasing character is received instead of the four required for successful phasing. The PHASING DRIVE signal enables input 19 of A8–21B for 9/25 of a baud. During this interval $\overline{\text{IC7}}$ does not undergo a ZERO-to-ONE transition, so that A8–21B does not trigger one-shot A8–20. However, if a second phasing character is not received, the PHASING DRIVE signal is left at ONE, permitting the next ZERO-to-ONE transition of $\overline{\text{IC7}}$ to trigger one-shot A8–20. A8–20 generates a MISS pulse which resets the phasing counter for another phasing cycle.

(3) *P&I indicator circuit.*—The P&I indicator circuit allows the operator to visually determine when the KW–7 is operating in the phasing or indicator modes of operation. The P&I indicator circuit, comprising NOR gate A3–21 and lamp driver A10–8, must complete the operating path for the P&I indicator lamp during phasing and indicator phases of both send and receive operations. The lamp driver completes the operating path for the P&I indicator lamp whenever it is fed with a ZERO input. Since a NOR gate produces a ZERO output when any of its inputs is a ONE, NOR gate A3–21 will cause the lamp driver to light the P&I indicator lamp if any of its inputs is ONE. The $S \cdot \overline{N}$ signal from the data input logic is applied to input 7 of A3–21. The $S \cdot \overline{N}$ signal is a ONE during phasing and indicator phases of send operation, causing the lamp driver to complete the operating path for the P&I indicator. The $\overline{\text{PC0}}$ and $\overline{\text{PC1}}$ outputs of the phasing counter are also applied to A3–21. During phasing, either $\overline{\text{PC0}}$ and/or $\overline{\text{PC1}}$ is ONE. This condition causes the lamp driver to complete the circuit for the P&I indica-

tor lamp during phasing of receive operation. The BG·$\overline{NO}$ signal applied to input 5 of A3-21 is a ONE only during indicator, thereby causing the P&I indicator lamp to be illuminated during indicator period. The output from pin 12 of lamp driver A10-8, causes the remote lamp, if connected, to be energized at the same time as the P&I lamp.

h. S. T. Power Set, Power Set, and Generator Circuit (fig. 4-58).—The S. T. power set, power set, and counter set generator circuit generates the SET and SET 1 pulses for use throughout the extensor and control and in the key generator.

(1) *S. T. Power set generator.*—The ST POWER SET pulse is generated in the following manner. When power is applied to the KW-7, the time delay generates a negative-going ramp voltage which, after approximatley 200 milliseconds, reaches the critical level required to fire Schmitt trigger A6-15. A6-15 transfers a step voltage to inverter A6-16. The positive-going transition of the output of A6-16 constitutes the ST POWER SET pulse which is fed to the break generating circuit and to AND gate A6-21C.

(2) *Power set generator.*—The POWER SET pulse occurs for any one of the conditions described below. AND gates A6-21A, through A6-21E are connected together to form a five-input OR gate. The output of this OR gate fires one-shot multivibrator A6-14 which, in turn, generates a POWER SET pulse. A6-14 is triggered when the KW-7 is switched from plain to cipher or from cipher to plain, when an ST POWER SET pulse occurs, during alarm testing, or when a BREAK condition exists.

(3) *Set and set 1 generator.*—The SET and SET 1 pulses occur for any one of three conditions as described below: AND gates A6-1, A6-11, and A6-21F are connected together to form a three-input OR gate. The output of this OR gate fires one-shot multivibrator A6-19, which generates a SET 1 pulse directly, and a SET pulse indirectly by means of set driver A6-18. The OR gate inputs are a POWER SET pulse to A6-1, a LIG (LOCK IN GATE) pulse to A6-11, or a SEND pulse to A6-21F.

i. Indicator Control and Normal Generating Circuit (fig. 4-59).—The indicator control and normal generating circuit detects when the KW-7 has successfully completed phasing and generates a control signal to initiate the indicator phase of operation. The circuit comprises the BG generator, the lock in gate, and the normal generator.

(1) *BG generator.*—The BG generator (AND gate A6-11A and flip-flop A6-6) produces the $\overline{BG}$ control signal to initiate the indicator phase of operation when the KW-7 has successfully completed phasing. When the SEND switch is released, signifying the end of send phasing, the send control generates a BG TRIGGER pulse which is applied to input 8 flip-flop A6-6. A6-6 goes to the ONE state, and BG is generated. To ensure that the flip-flop is in the ZERO state when send phasing is initiated, the $\overline{BG\ TRIGGER}$ pulse from the send control resets the flip-flop to the ZERO state. When receive phasing has been successfully completed, the lock in gate generates a ONE LIG signal. The LIG signal enables pin 10 of AND gate A6-11A, so that the next OCO pulse sets A6-6 to the ONE state. The SET pulse applied to input 6 of A6-6 performs the same function as the $\overline{BG\ TRIGGER}$. A $\overline{BG}$ output is also taken from flip-flop A6-6 and applied to the data input circuit and the indicator circuit.

(2) *Lock in gate.*—The lock in gate (AND gate A8-13 and flip-flop A8-12) detects when the receiving KW-7 has successfully completed phasing. Whenever the phasing counter reaches a count of four before being reset, it generates a PC1 pulse which is applied to input 8 of flip-flop A8-12. The PC1 pulse sets A8-12 to the ONE state and generates a ONE LIG signal. This occurs only when receive phasing has been successfully completed. A8-12 must be reset before phasing is initiated and after phasing has been completed. This is accomplished by the MISS pulse from the counter set generator, the CLX pulse from the indicator circuit, and the SEND 1 signal from the send flip-flop (fig. 4-56). The MISS pulse and SEND 1 signals ensure that the flip-flop will be reset

prior to phasing. The CLX pulse is applied to AND gate A8–13. Since A8–13 is permanently enabled by the ground connection on pin 15, the CLX pulse is always able to reset the flip-flop. This ensures that the lock in gate will be reset after the completion of phasing.

(3) *Normal generator.*—The normal generator generates the NORMAL and $\overline{\text{NORMAL}}$ pulses during the normal phase of operation. This allows the KW–7 to begin normal operation as soon as the indicator phase has been completed. The normal generator consists of AND gate A6–11B, flip-flop A6–3, power amplifiers A6–8A and A6–8B, and stage 2 of shift register SRA in the data extensing circuit.

(a) The normal generator must produce a logical ONE NORMAL signal when the indicator phase of operation has been completed, when the KW–7 is operating in the plain mode, or when an alarm test is being performed. During phasing, the set generator presets flip-flop A6–3 to its ZERO state. This action prevents A6–3 from producing the ONE NORMAL control signal prematurely.

1. When indicator phase of operation is completed, the indicator character control generates a logical ONE 12 LETTERS COUNT. When the next P pulse occurs, the INDICATOR DELAY signal becomes ONE (see fig. 4–60, A6–4 pin 3) setting A6–3 to the ONE state, and generating a ONE NORMAL 1 and a ZERO $\overline{\text{NORMAL}}$ 1 signal. The delay between the occurrence of 12 LETTERS COUNT and ONE NORMAL 1 is required to allow the data extensing circuit enough time to process the indicator information.

2. Operation of the normal generator during plain mode of operation is similar to that during indicator, except that the INDICATOR DELAY signal becomes ONE as a result of a P pulse applied to A6–4. The indicator character control is triggered by a single ZERO as a result of detecting a blank character in SRA2. The normal flip-flop (A6–3) is set immediately by the INDICATOR DELAY signal, instead of waiting for 12 blank and 12 letter characters to be counted.

3. Operation of the normal generator during alarm test is as follows: the AT4A signal from the alarm test switch enables input 8 of AND gate A6–11B. An OCO pulse from the output counter sets A6–3 to ONE, generating a ONE NORMAL 1 signal.

(b) The NORMAL 1 signal is taken from the ONE output of A6–3. This signal is inverted by A6–8B to produce the $\overline{\text{NORMAL}}$ 2 signal. The $\overline{\text{NORMAL}}$ 1 control signal is taken from the ZERO output of A6–3, and inverted by A6–8A to produce the NORMAL 2 signal.

j. Indicator Circuit (fig. 4–60).—In order to increase message security, the indicator logic ensures that enciphering and deciphering will begin at a different point in the Fibonacci cycle each time a message is to be transmitted. The indicator logic consists of the following major circuits: blanks detector A9–21B, letters detector A9–21A, internal break detector A10–17B, indicator delay flip-flop A6–4, and the indicator counter comprising flip-flops A12–2, A12–3, A12–5, A12–6, A12–7, AND gate A12–4C, and stage SRA2 of the data extensing circuit (fig. 4–61).

(1) During the indicator phase of operation, random ONE's and ZERO's are being shifted out of shift register X (SRX). The duration of the indicator phase is determined by the time required for the occurrence of 12 ZERO's followed by 12 ONE's (normally this occurs within 7 to 15 seconds).

(2) A SET pulse sets indicator delay flip-flop A6–4 to the ONE state, making the INDICATOR DELAY signal a ONE. A SET 1 pulse is applied to input 3 of AND gate A10–15A which triggers one-shot A10–16. A10–16 generates an ICR pulse which sets all stages of the indicator counter to ONE. The ZERO $\overline{\text{INDC}}$ output on pin 3 of A12–7 enables input 7 of blanks detector NOR gate A9–21B. Since the NORMAL

2 applied to input 9 of A9-21B is ZERO enable during indicator, A9-21B will output a ONE whenever SRX5 is ZERO. This ONE enables input 19 of AND gate A12-4B; A12-4B triggers one-shot A12-1 at $\overline{Pd}$ time. The pulse output from A12-1 flips stage one of the indicator counter, injecting a count of one into the counter. This sequence continues, with an additional count injected at $\overline{Pd}$ time whenever SRX5 is ZERO.

(3) The indicator counter is basically a ÷ 16 counter, with reset feedback from stage four (A12-6) to stage three (A12-5). After 8 counts have been applied to A12-2, output 3 of A12-6 goes from ZERO to ONE, applying a ONE pulse via AND gate A12-4C to input 4 of A12-5. This ONE resets A12-5, deletes four counts from the total, and forces the indicator counter to divide by 12 instead of 16.

(4) After the indicator counter has counted 12 ZEROS a ZERO-to-ONE transition at output 10 of A12-6 flips A12-7 to the ZERO state, with a ZERO INDC signal now appearing on output 10 of A12-7. This ZERO enables input 6 of letters detector NOR gate A9-21A; simultaneously, a ONE $\overline{INDC}$ signal disables input 7 of blanks detector A9-21B. In the manner described in paragraph 3 above, the indicator counter now counts until a total of 12 ZEROS has appeared on $\overline{SRX5}$; this is equivalent to counting 12 ONES on SRX5. After the 12th ONE is counted, output 10 of A12-7 goes from ZERO to ONE, setting indicator delay flip-flop A6-4 to the ZERO state, and driving the INDICATOR DELAY signal to ZERO.

(5) The last ONE stored in SRX5 must now be shifted to the line output circuit before normal operation is begun. This shifting requires a time interval of seven bauds. After shifting is completed, a P pulse flips indicator delay flip-flop A6-4 to the ONE state, returning the INDICATOR DELAY signal to ONE. The ZERO-to-ONE transition of the INDICATOR DELAY signal triggers the normal generator and starts the normal phase of operation.

(6) As soon as normal operation begins, NORMAL 2 goes to ONE, disabling BLANKS detector A9-21B and LETTERS detector A9-21A. $\overline{NORMAL\ 2}$ goes to ZERO, enabling input 9 NOR gate A10-18A. When LIIST goes from ONE to ZERO, A10-18A transfers a ONE to AND gate A10-15C, which in turn triggers one-shot A10-16. A10-16 generates an ICR pulse, resetting the indicator counter or verifying an existing reset condition. The indicator counter is now ready to detect a line break.

(7) Line break detector NOR gate A10-18B is enabled as follows: BRLO (Break Receive Lock Out) is set to ZERO by placing the BREAK FUNCTION switch in the OFF position, $\overline{NORMAL\ 2}$ is ZERO during normal operation; and BRK is ZERO except when the operator initiates a lock break. Therefore, A10-18B transfers a ONE each time LINE IN becomes ZERO. This ONE enables input 20 of AND gate A12-4A. A12-4A triggers one-shot A12-1 at Pd time and the indicator counter registers one count. If no break occurs, the next ONE-to-ZERO transition of the LIIST signal triggers one-shot A10-16 via A10-15C, and the indicator counter is reset. However, if a break occurs, LIIST remains at ZERO. Since a ONE-to-ZERO transition of LIIST is required to trigger one-shot A10-16, an ICR pulse is not generated to reset the indicator counter. The counter now proceeds to count one break character for each Pd pulse. If the break remains for the duration of 12 characters, that is, if LIIST has not returned to ONE by the time the indicator counter registers 12 counts, flip-flop A12-7 is set to ZERO, making $\overline{INDC}$ a ONE. This ONE triggers the break generator; the break generator in turn stops the equipment and indicates a break condition.

(8) If the local KW-7 begins printing garbled text, or if for some reason the local KW-7 must break the network, the operator depresses the BREAK switch which makes the $\overline{BRK}$ signal, on input 9 of NOR gate A10-17B and the LIOD (line out digital) signal on input 10 of A10-17B, both ZERO. The ONE which now appears on the output of A10-17B enables input 20 of AND gate A12-4A. A12-4A triggers one-shot A12-1 at the Pd rate and the indicator counter registers one count for each Pd pulse. When

the counter reaches a count of 12, as described above, the $\overline{\text{INDC}}$ output of flip-flop A12–7 becomes a ONE, causing the break generator to stop the equipment. See paragraph 4403*o* for complete description of the break generator circuit.

(9) CLX gate A10–17A permits the KW–7 to skip the indicator phase when the unit is in plain mode of operation. A blank character is always generated by the transmitting KW–7 as soon as phasing is completed. This blank character normally tells the receiving KW–7 to go into indicator phase. However, in plain mode, no indicator phase is necessary, so that the receiving unit may go from phasing directly into normal mode.

(a) When a blank character is stored in shift register A, (SRA) SRA2 will be ZERO during $\overline{\text{P}}$ time. Since NORMAL 1 and $\overline{\text{BG}}$ are both ZERO during phasing, A10–17A will transfer a ONE CLX pulse at $\overline{\text{P}}$ time. Power amplifier A10–11 inverts CLX, placing a ZERO $\overline{\text{CLX}}$ on input 3 of AND gate A6–1. The PLAIN input on pin 19 of A6–1 is a ONE enable only during plain operation. At the end of the $\overline{\text{P}}$ pulse, when P goes from ZERO to ONE, $\overline{\text{CLX}}$ also goes from ZERO to ONE, giving a ONE pulse at the output of A6–1. This pulse sets indicator delay flip-flop A6–4 to the ZERO state, making the INDICATOR DELAY signal ZERO. The next P pulse resets A6–4 to the ONE state, producing a ZERO-to-ONE transition of the INDICATOR DELAY signal. The ZERO-to-ONE transition of the INDICATOR DELAY signal starts the normal mode of operation, as previously described. The PLAIN input also activates the PLAIN indicator lamp.

(b) The ZERO to ONE shift of $\overline{\text{CLX}}$ also sets indicator and normal flip-flop A6–10 to the one state giving a ONE I&N signal and a ZERO $\overline{\text{I\&N}}$ signal. The ZERO $\overline{\text{I\&N}}$ signal is applied as an enabling level to the phase correction circuit. The ONE I&N signal is applied to enable a gate which deletes one count in the output character counter during indicator and normal. This delete function is needed to change the eight bit character length used in send phasing to a seven bit character length used in send indicator and send normal. The ONE I&N level is also applied to the key generator W activity monitor as an enabling level.

(c) Inverter A6–20A produces $\overline{\text{PLAIN}}$ by inverting the PLAIN signal from the PCR switch. $\overline{\text{PLAIN}}$ is applied to the S.T. power set circuit, triggering a POWER SET pulse when the KW–7 is switched to cipher operation.

(10) SRA2. Shift Register A, stage 2, (fig. 4–61) is used during the indicator phase of both send and receive modes of operation. During the indicator phase of send operation, shift register A samples the M2B noise signal from the random noise generator (see alarm circuit) and produces either a LETTERS ENABLE (SRA2 ONE) or a BLANKS ENABLE (SRA2 ZERO). During the indicator phase of receive operation, shift register A samples the input signal and detects whether a letter or blank character was generated by the indicator function of the sending KW–7. This is done in order to start processing data at the same point in both Fibonacci cycles. During the normal phase of send, shift register A stores the input characters from the data input circuit. During receive SRA only stores ZEROS. The output of SRA during the normal phase is only used when the KW–7 is operating in the send mode.

(a) Send indicator operation.—The ABIN input to SRA5 is inactive during send indicator. Random pulses (M2B) from the random noise generator circuit are sampled at $\overline{\text{CTRP}}$ time by AND gate A9–10A. If M2B is a ONE, SRA2 is set to ZERO, enabling input 5 of CLX gate A10–17A. At $\overline{\text{P}}$ time the CLX gate loads a ZERO into all stages of SRX. (See fig. 4–61.) It should be remembered that SRX will automatically fill with ONES shifted in at OBR rate if $\overline{\text{CLX}}$ is not loading ZEROS in SRX. If M2B is a ZERO, SRA2 is left in the ONE state, disabling the CLX gate and preventing SRX from being loaded with ZEROS After SRA2 is sampled, it is reset to ONE at Pd time by a ONE from AND gate A9–10B.

(b) Receive indicator operation.—During receive indicator, SRA2 is used to vote on the nature of the received character—that is, whether the character is a LETTER or a BLANK. The operation of SRA2 in conjunction with the CLX gate is similar to the operation described in subparagraph (a) above, with the following differences. M2B is now inactive while ABIN consists of the received information. If the received information is a LETTER, SRA2 will be in the ONE state at P time, disabling the CLX gate and allowing SRX to shift ONES. If the received information is a BLANK, SRA2 will be in the ZERO state at P time, enabling the CLX gate and forcing SRX to shift ZEROS.

k. Data Extensing Circuit (fig. 4-61).—During send normal, the data extensing circuit retimes the loop input data so that it can be synchronized with internal KW-7 timing. The circuit comprises three five-stage shift registers, designated SRA, SRB, and SRX. Input data is stored alternately in SRA and SRB, and then transferred to SRX. From SRX, the data is shifted out, one bit at a time, to the key generator, where it is combined with key to form cipher. Operation of the data extensing circuit during receive is similar to the operation during send, the only important differences being the rate at which input data is supplied and the use of SRA.

(1) *Send operation.*—During send operation, the data extensing circuit converts 7.42 baud synchronous ABIN data (from a free-running local teletypewriter) to 7.0 baud synchronous data which is processed through the KW-7. This conversion is not required, however, if a 7.0 baud step TD is used in conjunction with the TD step circuit in the KW-7. With a 7.0 baud step TD, the input data is synchronous 7.0 baud information. In this case, the data extensing circuit simply converts the input teletypewriter information into data which can be processed through the KW-7. This conversion is performed in the following manner.

(a) The first ABIN character is sequentially stored, in SRA, (one bit at a time) with a total time of 7.42 bauds required to complete storage. At Pd time this character is transferred to SRX and then immediately shifted out of SRX at the OBR rate. Since there is no fixed time relationship between the loading of SRA and the occurrence of Pd, Pd can occur immediately after SRA is loaded, or it can occur up to a full character time later.

(b) Similarly, the second ABIN character is stored in SRB, transferred to SRX at Pd time, and immediately shifted out of SRX at the OBR rate.

(c) The third ABIN character goes into SRA, from SRA into SRX, and from SRX to the key generator. The fourth character goes into SRB, and so on. Thus all odd-numbered characters go to SRA and all even-numbered characters into SRB.

(d) It should be noted that the SRX read-out rate (7.0 bauds per character) is greater than the data read-in rate (7.42 bauds per character) when free running teletypewriter is being used. If input data is arriving continuously with no time lapse between characters, the SRA-to-SRX or SRB-to-SRX transfer time will advance 0.42 baud per character, so that after a certain time the transfer will be attempted before SRA or SRB is fully loaded. The send normal circuit detects when this condition is about to occur, by examining the data available in SRA and SRB, and generates a signal which inhibits the transfer until the data character is fully loaded into SRA or SRB. This signal also inhibits the key generator so that pure key is not transmitted in the absence of data; during this interval the KW-7 transmits a speed differential lockup (all mark) character. Normal operation resumes as soon as the data character has been fully loaded into SRA or SRB.

(e) During send, the input counter is synchronized to the loop input data from the local teletypewriter. The output of the counter, IBR, is used to sample the input data.

(2) *Receive operation.*—Receive operation differs from send operation in two respects. First, retiming of the input data is not necessary. This is because the input data is always occurring at 7.0 bauds per character, since it is coming from another KW–7 instead of a local teletypewriter. Second, SRA is used only to check the validity of the incoming data (validity is defined as at least one ZERO information bit per character). This validity check or voting process in SRA is actually performed by stage SRA5 of the SRA register. During receive normal SRA5 is initially set to a ONE. However, SRA will be shifted only by ZERO bauds during receive normal operation. At $\overline{p}$ time if stage SRA5 contains a ZERO, the message (M) flip-flop in the output control circuit (fig. 4–64) will be set to ONE, indicating that a valid character has been received in SRB and can be transferred to the local page printer. If stage SRA5 contains a ONE at $\overline{P}$ time the M flip-flop will be set to ZERO and the invalid character present in SRB will be transferred to SRX but will be inhibited in the output circuits. The contents of SRA are examined at P time, and reset to zero 34 microseconds later at Pd time. The data itself is routed continuously through SRB to SRX.

(3) *Shift Register B.*—Shift register B SRB comprises the following circuits: flip-flops A9–16, A9–17, A9–18, A9–19, A9–20; AND gates A11–6A and A11–6B; SHIFT B one-shot multivibrator A11–14; and AND gates A9–12E, A9–12F, A9–9F, A9–10F, A9–13C. Allowing for the differences in inputs, the following detailed discussion of SRB can be considered applicable to SRA; however, during the indicator phase SRA performs a special function which is described in the indicator logic theory. SRB accepts a serial input and delivers a parallel output. This means that information is fed into the register serially one bit at a time. After all bits in a given character are contained in the register, they are read out in parallel, (simultaneously) into SRX. Information input to the register consists of the ABIN and $\overline{\text{ABIN}}$ levels applied to pins 7 and 2, respectively, of flip-flop A9–16. Depending upon which level is a ONE and which is a ZERO, A9–16 will be set to the ZERO or ONE state when a SHIFT B pulse is applied to pins 1 and 8. Assume that $\overline{\text{ABIN}}$ is ONE, enabling input 7 of A9–16, and that ABIN is ZERO, inhibiting input 2 of A9–16. When a SHIFT B pulse appears on pins 1 and 8, A9–16 is set to the ZERO state, with a ONE appearing on pin 10 and a ZERO on pin 3. The output of A9–16 now determines which way A9–17 will be set when the second SHIFT B pulse occurs. When the second SHIFT B pulse does occur, the ZERO which was in A9–16 is shifted into A9–17, leaving A9–16 ready to accept the second input bit. The ZERO state of A9–17 determines which way A9–18 will be set by the third SHIFT pulse and so on. A five-bit character is stored as follows:

Bit 1 read into A9–16
Bit 1 shifted from A9–16 into A9–17
Bit 2 read into A9–16
Bit 1 shifted from A9–17 to A9–18 and bit 2 shifted from A9–16 to A9–17
Bit 3 read into A9–16
Bit 1 shifted from A9–18 to A9–19, bit 2 shifted from A9–17 to A9–18, and bit 3 shifted from A9–16 to A9–17, etc.

It is seen that every time a shift B pulse occurs, each bit is shifted one stage to the right, and the first stage is ready to accept a new bit from the ABIN and $\overline{\text{ABIN}}$ lines. This sequence continues until all five bits of a given character have been read into the register. After the register is full, a TRB (transfer B) pulse is applied to the pulse input of AND gates A9–12E, A9–12F, A9–9F, A9–10F, and A9–13C. Any gate having a ONE present on the level input will deliver a ONE to SRX. Thus, if bits 2 and 4 had been ZEROs, AND gates A9–10F and A9–12F would now generate ONES which would set A9–11 and A9–7 of SRX to the ZERO state. The SHIFT B pulse is synchronized to the input bit rate when in the send mode or to the output bit rate when

in the receive mode. This operation is accomplished by AND gates A11–6A and A11–6B, in conjunction with one-shot multivibrator A11–14. When in the send mode, SBG is ONE and the $\overline{\text{IBR1}}$ signal triggers A11–14 by way of A11–6A; similarly, when in the receive mode $\overline{\text{SEND}}$ is ONE, and the $\overline{\text{OBR1}}$ signal triggers A11–14 by way of A11–6B. The SHIFT B pulse from A11–14 is a ONE with a duration of 34 microseconds.

(4) *Shift register SRX.*—SRX differs from SRA and SRB in that it accepts a parallel input and delivers a serial output. That is, all bits of a given character are read in simultaneously and, at some later time, read out sequentially. In the absence of data from SRA or SRB, the OBR1 signal applied to the ONE side of stage SRX5 (A9–6) causes SRX to continuously shift out ONES via A9–15. However, if SRA or SRB introduces a ZERO into a given stage, this ZERO will be shifted one stage to the right by each OBR1 pulse. For example, if a ZERO is loaded into SRX4 (A9–7), this ZERO will appear at the output of A9–15 four OBR1 times later.

l. Send Normal Circuit (fig. 4–62).—The send normal circuit determines the counting rate of the input counter, and controls the transfer of loop information into the data extensing circuit. Major send normal circuits are MOD 6 flip-flop A11–10, loop information detector A11–16, and the send-shift-transfer function comprising NOR gates A12–8A, A12–11A, A12–11B, AO flip-flop A12–9, BO flip-flop A12–10, AND gate A12–4, and one-shot multivibrator A12–15.

(1) *Loop information detector.*—The loop information detector A11–16 detects the start bit of each character from the data input circuit, and gates the data extensing circuit accordingly. The MOD 6 generator controls the counting mode of the input counter.

(a) At some prior time, a SET pulse has set flip-flops A11–10, A11–16, and A11–17 to the states where MOD 6 is ZERO, FL is ONE, and FLD is ZERO. FLD and $\overline{\text{PCO}}$ enable NOR gate A11–9, placing a ONE enable on input 7 of A11–10 and input 2 of A11–16. These conditions prevail until the arrival of the start bit of a LOIG character from the data input circuit. This start bit triggers flip-flops A11–10 and A11–16 to the ONE and ZERO states, respectively, driving MOD 6 to ONE, FL to ZERO, and $\overline{\text{FL}}$ to ONE. The ZERO-to-ONE transition of MOD 6 causes the input counter to shift from MOD 8 (phasing detection mode) to MOD 6, the ZERO FL enables input 10 of NOR gate A12–8A and input 3 of NOR gate A12–8B, the ZERO-to-ONE transition of $\overline{\text{FL}}$ resets the send phasing logic and sets A11–17 to the ONE state, placing a ONE disable on input 6 of NOR gate A11–9. The output of A11–9 goes to ZERO, disabling input 7 of A11–10 and input 2 of A11–16; A11–10 and A11–16 are now immune to any further LOIG activity.

(b) A11–16 and A11–17 are kept disabled for the next 6 bauds of the LOIG character and are then enabled before the arrival of the next character as follows. One baud time after the end of the last information baud, $\overline{\text{T8}}$ goes from ZERO to ONE. This sets A11–16 to the ONE state, placing a ZERO enable on input 7 of A11–11 and a ONE enable on input 7 of A11–17. The M signal from the output control circuit goes from ONE to ZERO at P time enabling input 6 of NOR gate A11–11. A11–11 enables input 2 of A11–10. On the trailing edge of $\overline{\text{P}}$, A11–10 is set to ZERO, MOD 6 goes to ZERO, and the input counter reverts to MOD 8 operation in order to look for phasing information if any should become available on the line input. Meanwhile, with FL as a ONE enable on input 7, A11–17 is set to ZERO by the next IBR pulse. FLD becomes ZERO, enabling input 6 of A11–9. A11–9 places a ONE enable on input 7 of A11–10 and input 2 of A11–16 making them ready to detect the start baud of the next character.

(c) If another KW–7 initiates phasing before the next LOIG character, $\overline{\text{PCO}}$ becomes ONE, disabling input 7 of A11–10 via A11–9. A11–10 is now unable to respond

to LOIG, MOD 6 remains ZERO, and the input counter continues MOD 8 operation. However, if no phasing signal occurs, A11-10 is set to ONE by the next LOIG, and the entire cycle repeats.

(2) *Send shift transfer.*—The send and shift transfer functions are performed by shift B NOR gate A12-8A, shift A NOR gate A12-8B, AO flip-flop A12-9, BO flip-flop A12-10, MOD 2 adder A12-11A and A12-11B, AND gate A12-4, one-shot multivibrator A12-15, and inverter A12-12. These circuits control the flow of data into shift registers A and B. AO flip-flop A12-9 determines whether data is shifted into SRA or SRB. MOD 2 adder A12-11A and A12-11B determine if data is available in SRA or SRB for shifting into SRX. BO flip-flop A12-10 determines whether data is shifted into SRX.

(a) As described above, the LOIG start bit sets FL to ZERO. This ZERO enables input 10 of shift B gate A12-8A and input 3 of shift A gate A12-8B. At some prior time a SET pulse has set both A12-9 and A12-10 to the ONE state, placing a ZERO enable on input 6 of shift A gate A12-8B and a ONE disable on input 9 of shift B gate A12-8A. Since $\overline{\text{SEND 3}}$ is ZERO during send operation, A12-8B transfers a ONE SAG (shift A gate) to the receive normal circuit and to input 7 of A12-9. The SAG gate permits the first LOIG character to be shifted into SRA at the input bit rate via AND gate A11-6B and one-shot A11-7 which produce a SHIFT A pulse. At the end of the LOIG character, IC7 sets A12-9 to ZERO, disabling A12-8B in order to prevent further data insertion into SRA.

(b) Input 9 of A12-8A is now a ZERO enable. The second LOIG character sets FL to ZERO, driving the SBG (shift B gate) output of A12-8A to ONE. The SBG gate permits the second LOIG character to be shifted into SRB at the input bit rate. SBG also enables input 2 of A12-9, so that after the second LOIG character is fully registered in SRB, an IC7 pulse can reset A12-9 to ONE. When IC7 resets A12-9, A12-8A is disabled. A12-8B is enabled, and the third LOIG character goes into SRA. This alternate shifting of data into SRA and SRB continues as long as LOIG is active.

(c) The MOD 2 adder (A12-11A and A12-11B) determines whether information has been shifted into SRA or SRB, that is, whether information is available for shifting into SRX. As described above, the first LOIG character triggers the generation of SAG, which allows A12-9 to be set to ZERO at IC7 time. A12-9 puts a ZERO enable on input 5 of NOR gate A12-11A. Since the SET pulse has already set A12-10 to ONE, a ZERO enable also exists on input 6 of A12-11A. A12-11A therefore has a ONE output which enables input 10 of AND gate A12-4; this ONE is also applied to the output control circuit to indicate that data is available. At Pd time, A12-4 triggers one-shot A12-15, which sets A12-10 to ZERO via inverter A12-12. A12-10 places a ONE disable on input 6 of A12-11A, and a ZERO enable on input 9 of A12-11B. When BO flip-flop A12-10 is set to ZERO, the BO output shifts from a ONE to a ZERO. This ZERO BO signal is inverted by NOR gate A12-12 (fig. 4-61) to generate a ONE TRA (TRANSFER A) signal, which is applied to AND gates A9-12A and B, A9-9D, A9-10D, and A9-13A. The TRA signal causes the AND gates to transfer the contents of register SRA to register SRX.

(d) The second LOIG character triggers the generation of an SBG signal, allowing A12-9 to be set to ONE at IC7 time. With A12-9 in the ONE state, a ZERO enable is placed on input 10 of A12-11B. A12-11B outputs a ONE which again enables input 10 of A12-4, and indicates to the output control circuit that data is available. At Pd time, A12-4 triggers one-shot A12-15, producing a ONE CSM signal, which is inverted to a ZERO $\overline{\text{CSM}}$ signal by NOR gate A12-12. This $\overline{\text{CSM}}$ ZERO signal is applied to NOR gate A12-13B in the receive normal logic

(fig. 4-60). A12-13B was previously enabled by a ZERO BO level. Therefore the $\overline{\text{CSM}}$ signal produces a ONE TRB (TRANSFER B) signal on pin 11 of A12-13B. The TRB signal is applied to AND gates A9-12E and F, A9-9F, A9-10F, and A9-13C, causing the contents of register SRB to be transferred to register SRX. The trailing edge of the ZERO $\overline{\text{CSM}}$ pulse produced by NOR gate A12-12 also sets BO flip-flop A12-10 back to the ONE state. The original conditions have now been re-established, and the entire cycle will be repeated for the next two LOIG characters.

(e) If free-running teletypewriter equipment is used, the SRX read out rate (7.0 bauds per character) is faster than the data read in rate (7.42 bauds per character) on the loop input. If loop input (LOIG) characters are arriving continuously with no time lapse between characters, the SRA to SRX or SRB to SRX transfer time will advance 0.42 baud per character, so that eventually a transfer will be attempted before a complete character has been shifted into SRA (or SRB). When this happens the transfer to SRX is blocked, and SRX shifts out a speed differential lockup (all mark) character containing all ONE bauds. Meanwhile, the partially shifted SRA (or SRB) register shifts until a complete character is loaded, then normal operation resumes. The send normal circuit responds to an attempted early transfer to SRX in the following manner, if register SRA contains only a partial character. The Pd pulse (which occurs at a 7.0 baud output character rate) eventually will be applied to AND gate A12-4 before shifting in SRA is complete. (The Pd pulse sets up the transfers from SRA to SRX or SRB to SRX.) If shifting had not been completed in SRA both AO flip-flop A12-9 and BO flip-flop, A12-10 would be in the ONE state, causing a ZERO SNA output from the MOD 2 adder (NOR gates A12-11A and B). This ZERO SNA signal will inhibit AND gate A12-4 and prevent one shot A12-15 from being triggered at Pd pulse time. The BO flip-flop A12-10 will not be set to ZERO, since a $\overline{\text{CSM}}$ ZERO-to-ONE shift from A12-15 via A12-12 was inhibited. Since BO flip-flop A12-10 did not change state, the BO output will not produce a ZERO-to-ONE TRA (Transfer A) signal at the output of NOR gate A12-12. Thus the premature transfer of SRA to SRX is inhibited. Now the SRX register will automatically shift out ONE bauds generated by flip-flop A9-6, at an OBR rate, producing a speed differential lockup character on the line. Concurrently, the SRA register shifting will be completed and then a normal SRA to SRX transfer will occur immediately after the speed differential lockup was shifted out of SRX.

(f) In the absence of LOIG activity, a ONE disable will remain on input 5 of A12-11A and input 9 of A12-11B at all times. The resulting ZERO at the common output of A12-11A and A12-11B will indicate to the output control circuit that no data is available.

m. Receive Normal Circuit (fig. 4-63).—During receive normal mode, the SRA register has the special function of voting on valid characters by shifting only, when impulsed by ZERO bauds present in the input character. At the same time each input character is shifted into SRB, and then transferred to the SRX register. (Alternate loading of characters first into SRA, then into SRB for transfer to SRX is not required in receive normal mode, because received LINE IN data is 7.0 baud synchronous, and does not require extensing.)

(1) The receive normal circuit generates the shift A pulse in NOR gate A11-5, AND gate A11-6A and ONE SHOT A11-7. In receive mode, the SEND 1 level on pin 6 of A11-5 will be a ZERO enable, and each time the ABIN signal on pin 7 contains a ZERO baud, A11-5 will apply a ONE enable level to pin 20 of AND gate A11-6A. When $\overline{\text{IBRI}}$ becomes a ONE pulse, A11-6A will trigger ONE SHOT A11-7, producing a SHIFT A pulse to shift SRA each time a ZERO baud is present in a character.

(2) While the ABIN character is being voted on, in SRA, it is being shifted normally into SRB. After the character is fully shifted into SRB, the receive normal logic generates a TRB pulse to transfer the contents of SRB into SRX. NOR gate A12-13A is used in receive normal mode to generate the TRB pulse. The SEND 2 and $\overline{\text{NORMAL 2}}$ signals will both be ZEROs during receive normal. Thus, a ONE TRB pulse will be produced once per character, each time a ZERO $\overline{\text{Pd}}$ pulse occurs, and will transfer the contents of SRB to SRX.

(3) During normal send operation SEND 1 is ONE, disabling NOR gate A11-5. SAG enables input19 of AND gate A11-6B (SAG) in a one for every odd loop input character (LOIG), as explained in the theory of operation for the send normal circuit. A11-6B triggers one-shot A11-7 on each $\overline{\text{IBR1}}$ pulse to give a Shift A pulse.

n. Output Control Circuit (fig. 4-64).—The output control circuit controls the transmission of the key signal when the KW-7 is in the normal phase of operation, and insures that the carriage of the local page printer will be in the letters (lower case) position before arrival of line input. Major circuits of the output control circuit are the output control and the downshift gate.

(1) *Output control circuit (send operation).*—During send operation, the output control circuit develops a signal which disables the auto key generator circuit when no data is available for transmission. This is necessary to prevent pure key on the line when text information is not being fed into the KW-7 loop circuit. The output control circuit is composed of NOR gate A12-14A and M flip-flop A12-21. In normal send operation, a ZERO $\overline{\text{NORMAL 2}}$ signal is applied to input 10 of NOR gate A12-14A. If no more loop input data is being read into the shift registers, the SNA gate signal from the send normal circuit will be ZERO, enabling input 7 of A12-14A. The last character stored in SRA or SRB is now shifted into SRX and sent out on the line. At $\overline{\text{P}}$ time, A12-14A transfers a ONE to input 8 of A12-21. This ONE, in combination with the SEND ONE on input 7 of A12-21, sets A12-21 to ZERO, generating a ONE $\overline{\text{M}}$ and a ZERO M. The ONE $\overline{\text{M}}$ disables the auto key generator and the line out circuits in the key generating circuit, preventing the transmission of pure key in the absence of text. The ZERO M signal is applied to the send normal circuit, where it is gated with $\overline{\text{FL}}$ to form a gate signal which permits resetting of the input counter and enabling of the loop input circuits. This sets up the equipment for receipt of loop information if such becomes available. When loop input information again is available, the send normal circuit generates a ONE CSM pulse which collector-sets A12-21 to the ONE state via truncated diode A12-16A, restoring the auto key generator and the line out circuits to normal operation.

(2) *Output control circuit (receive operation).*—In receive operation, NOR gate A12-14A is inactive. Instead, NOR gate A12-14B and AND gate A12-4 are used to sample SRA5 at $\overline{\text{P}}$ time. SEND 2 and $\overline{\text{NORMAL 2}}$ are both ZERO during receive operation, allowing $\overline{\text{P}}$ to produce a ONE at the output of A12-14B. If line information is available, SRA5 will be ZERO at $\overline{\text{P}}$ time, disabling A12-4. On the other hand, if line information is not available, SRA5 will be ONE at $\overline{\text{P}}$ time, allowing A12-4 to base-set A12-21 to the ZERO state. The M output of A12-21 disables the local loop output, while the $\overline{\text{M}}$ output disables the auto key generator. The reason for stopping the auto key generator is that the auto key generator in the sending KW-7 also stops when no information is available. Thus, when information again becomes available both auto key generators will start in synchronism.

(3) *Downshift gate.*—The downshift gate consists of inverter A6-16, downshift flip-flop A11-21, and NOR gate A12-16B. It generates a downshift signal for the local page printer as soon as the KW-7 begins the normal phase of operation. Downshifting is done to insure that the carriage of the page printer will be in the lower case (letters) position when the first character of the text arrives. This is based on the assumption

that the first character will be a letter, as will usually be the case; if the first character is a numeral, it will normally be preceded by an upshift signal.

(4) An initial SET pulse sets downshift flip-flop A11-21 to the ZERO state, placing a ONE enable on input 7 of A11-21 and a ZERO on input 10 of NOR gate A12-16B. Since input 9 of A12-16B is normally at ZERO, A12-16B outputs a constant ONE LOCO. When the KW-7 enters the normal phase of operation, the $\overline{\text{NORMAL 1}}$ signal, on input 6 of inverter A6-16, goes from ONE to ZERO, giving a ZERO-to-ONE transition of NORMAL 3 on input 8 of A11-21. This sets A11-21 to the ONE state, placing a ONE enable on input 2 of A11-21 and a ONE disable on input 10 of A12-16B. The LOCO output of A12-16B goes to ZERO. One baud time later, OBR1 resets A11-21 to ZERO, and the LOCO output of A12-16B returns to ONE. The page printer recognizes this one-baud ZERO level of the LOCO signal as a downshift command, and drops the carriage to the letters position if it is not already there.

o. Break Generating Circuit (fig. 4-65).—The break generating circuit gives a visible indication of a line break and allows the receiving operator to signal the sending operator that such a condition exists.

(1) An ST POWER SET pulse initially sets break flip-flop A6-9 to ZERO, generating a ONE $\overline{\text{BREAK}}$ signal and a ZERO BREAK signal. These signals allow the KW-7 to go through phasing and indicator and begin normal operation. The NORMAL 1 signal on input 7 of A6-9 becomes a ONE enable after the KW-7 successfully completes phasing and indicator. If text is being satisfactorily received, the indicator counter is continually being reset and is unable to generate a ONE $\overline{\text{INDC}}$ pulse at input 8 of A6-9. However, if a break occurs, the indicator counter counts until 12 successive break characters have been received, and then generates a ONE $\overline{\text{INDC}}$ pulse which sets A6-9 to the ONE state, making $\overline{\text{BREAK}}$ a ZERO and BREAK a ONE. (See par. 4403*j*(8).) The $\overline{\text{BREAK}}$ signal disables the P pulse generator, in the output counter circuit, turns on lamp driver A6-12, which energizes the BREAK LAMP and provides drive to energize the remote break lamp if the remote control unit is being used. The BREAK signal triggers the POWER SET and MISS pulse generators.

(2) Five manually operated switches are provided in the break generating circuit. These are the BREAK, REMOTE BREAK, BREAK RESTORE, REMOTE BREAK RESTORE and the BREAK FUNCTION switches. The BREAK and REMOTE BREAK switches allow the receiving operator to generate a ONE BRK and a ZERO $\overline{\text{BRK}}$ signal when he observes garbled text or when he wishes to assume command of the network. The ONE BRK signal disables the line output register of the Fibonacci feedback, loop output and line output circuit, causing the local KW-7 to transmit a break signal which stops the sending KW-7 and triggers a break indicator in all other receiving units in the network. The ZERO $\overline{\text{BRK}}$ signal resets the local indicator counter. In order to relieve the break condition in his own unit so that he may begin sending, the local operator must depress the BREAK RESTORE switch. This switch forces break flip-flop A6-9 to ZERO, restoring BREAK to ZERO and $\overline{\text{BREAK}}$ to ONE.

(3) The break condition will also be automatically relieved if another KW-7 initiates phasing. When this occurs, the indicator control circuit of the local KW-7 achieves lock and generates an LIG (lock in gate) signal which sets break flip-flop A6-9 to ZERO by way of AND gate A6-11.

(4) The BREAK FUNCTION switch disables the break indication circuits when radio transmission is used. This is necessary to eliminate the breaks which may otherwise result from signal fadeout. When the BREAK FUNCTION switch is closed, $\overline{\text{BRK}}$ and BRLO are constant ONES. $\overline{\text{BRK}}$ renders the indicator counter insensitive to LIOD (line out digital), while BRLO performs the same function for LINE IN.

p. *Audible Alarm Circuit (fig. 4-66).*—The audible alarm function is performed by alarm NOR gate A13-8A, NOR gate A13-9, inverter A13-8B, power amplifier A13-10, resistor A14-15 and audible indicator LS1. An audible alarm will be sounded when the BREAK, BUZ 1, or PLAIN signal is a ONE. The BREAK signal becomes ONE when the line opens. The BUZ 1 signal becomes a ONE if an alarm condition causes the line output control relay (A5-K1) to become deenergized. The BUZ 1 signal can also be a ONE if, during testing, the line input control relay (A5-K1) is deenergized and the ALARM TEST switch is placed in the 10 position. The PLAIN signal is a ONE during the plain mode of operation, so that an audible warning is always sounded when transmitting plain text. The alarm can be disabled for troubleshooting by opening the ALARM DISABLE switch. With a ONE on any input of NOR gate A13-8A, a ZERO enable appears on pin 6 of NOR gate A13-9, allowing A13-9 to pass a train of clock pulses to inverter A13-8B. The output of A13-8B is amplified by power amplifier A13-10 and applied via a 56 ohm resistor (A14-15) and the PCR switch to the audible alarm indicator (LS1). The circuit path to LS1 will be completed in all positions of the PCR switch except REMOTE. In REMOTE, the circuit path is completed to the audible alarm in the remote control unit.

4404. Key Generator Detailed Theory.—The detailed theory of operation for the key generator explains the theory of operation for each functional block described in Section 4300. The operation for each functional block is explained in terms of two logic levels, ZERO (−6 V) and ONE (0 V). Each logic diagram of a functional unit is supported by text which describes circuit operation in terms of input and output timing as related to overall equipment operation.

a. *Primary Key Generating Circuit (fig. 4-67).*—The primary key generating circuit generates the five primary timing pulses; $\overline{s}$, $\overline{t}$, $\overline{r}$, $\overline{q}$, and $\overline{p}$. The circuit consists of the Fibonacci shift register, a patchboard permuter, and five combiners.

(1) *Fibonacci shift register.*—The Fibonacci shift register generates the main key stream (P stream) used in the KW-7. The Fibonacci consists of inverter A4-13 and thirty-nine flip-flops (A1-1 through A1-16, A2-1 through A2-14, A2-20, A2-21, and A4-1 through A4-7). These stages will be referred to as FIB1, FIB2, etc. The 39 flip-flop stages are connected as a conventional shift register. The shift register is preset to its initial state by a SET pulse from the extensor and control. Stages FIB1 through FIB16 are preset to the ONE state, stages FIB17 through FIB35 to ZERO, and stages FIB36 through FIB39 to ONE. When triggered by F DRIVE pulses, a pattern of ONES and ZEROS is shifted through the register. The flip-flops are arranged so that each stage except FIB1 changes its state upon application of an F DRIVE pulse providing the preceding stage is in the opposite state. If the preceding stage is in the same state, the flip-flop does not change state. The operation of FIB1 is as follows. The A output of the feedback circuit is applied to input 7. The A output is also applied to input 9 of inverter A4-13. The $\overline{A}$ output of the inverter is applied to input 2. When triggered by an F drive pulse, FIB1 will change from the ONE state to the ZERO state only if the A output of the feedback circuit is a ZERO, and will change from the ZERO state to the ONE state only if the A output of the feedback circuit is a ONE.

(2) *Permuter.*—The permuter provides a means of manually changing the main key pattern generated by the Fibonacci shift register. The permuter consists of 30 patch cords. The Fibonacci ends of the patch cords are used to connect the outputs from 30 of the 31 pluggable flip-flop stages of the Fibonacci shift register to the $\overline{t}$, $\overline{s}$, $\overline{r}$, $\overline{q}$, and $\overline{p}$ combiners according to a preassigned key list which is changed at specified intervals. The combiners ends of the patch cords are semi-permanently attached to the permuter and will not normally be changed unless system security has been jeopardized.

(3) *Combiners.*—The combiners combine the 30 Fibonacci output signals that are selected by the permuter and produce five key timing signals, called $\overline{p}$, $\overline{q}$, $\overline{r}$, $\overline{s}$, and $\overline{t}$. Each combiner consists of four −3 input NOR gates connected to a common output. If

all three inputs of a given NOR gate are simultaneously ZERO, the common output is a ONE. However, if at least one input of every gate is ONE, the common output is ZERO. The $\bar{s}$ combiner also has provisions for a PLAIN signal input which inhibits the output of the $\bar{s}$ combiner when the KW-7 is operating in the plain mode. The outputs from combiners $\bar{s}$ and $\bar{t}$ are applied to the drive pulse generating and pulse deletion circuit. The outputs from combiners $\bar{p}$ through $\bar{r}$ are applied to the secondary key generating circuit.

b. Drive Pulse Generating and Pulse Deletion Circuit (fig. 4-68).—The drive pulse generating and pulse deletion circuit performs two functions. First, it generates F DRIVE pulses for the Fibonacci and KG pulses for various other functions in the key generator. Second, it interrupts the Fibonacci cycle by occasionally deleting an F DRIVE pulse.

(1) *Drive pulse generator.*—The drive pulse generator, comprising NOR gate A4-19 and power amplifier A4-21, generates KG pulses at the output bit rate if the KW-7 is either in indicator or normal phase of operation and is not in the plain mode. The $\overline{I\&N}$ signal applied to input 6 of A4-19 is a ZERO enable whenever the KW-7 is in indicator or normal phase of operation. The plain signal applied to input 7 is a ZERO enable except during plain operation. Therefore, during indicator and normal phase of cipher operations, A4-19 produces a ONE $\overline{KG}$ each time OBR is ZERO. Power amplifier A4-21 inverts $\overline{KG}$ to produce KG. KG generates F DRIVE pulses by triggering one-shot A6-2 via AND gate A6-1. A6-1 is disabled if $\overline{\text{SPECIAL POINT U}}$ becomes ZERO, as described in paragraph (2) below.

(2) *Pulse deletion.*—The pulse deletion circuit dilates the Fibonacci cycle by occasionally deleting an F DRIVE pulse. The circuit is so arranged that two successive pulses cannot be deleted. Principal circuits of the pulse deletion circuit are a MOD 2 adder and a ONE-to-ZERO detector.

(a) The MOD 2 adder (A4-16A, A4-17A, A4-18, A4-17B) performs an EXCLUSIVE OR (half addition) of the $\bar{t}$ and $\bar{s}$ outputs of the primary key generating circuit. In this operation, the sum is derived without taking into account any possible carries. The essential functional feature of a MOD 2 adder is that its output is a ONE when the two inputs are unlike, and a ZERO when they are alike, as will be evident from an examination of the following truth table.

EXCLUSIVE OR Truth Table

Input $\bar{t}$	Input $\bar{s}$	$t\bar{s}$	$\bar{t}s$	Output $C = \bar{t} \oplus \bar{s}$
0	0	0	0	0 + 0 = 0
0	1	1	0	1 + 0 = 1
1	0	0	1	0 + 1 = 1
1	1	0	0	0 + 0 = 0

(b) Flip-flop A4-8 and NOR gate A4-15B compose the ONE-to-ZERO detector. Neglecting the MOD 2 adder signals on inputs 2 and 7 of A4-8, it is seen that a SET pulse initially sets A4-8 to the ZERO state, placing a ONE on input 7 of A4-15B. This makes the output of A4-15B a ZERO, which in turn drives the output of inverter A4-16B to ONE. This ONE enables AND gate A6-1, allowing the KG pulses to trigger one-shot A6-2. A6-2 generates the F DRIVE pulses which shift the Fibonacci register.

(c) Assume that the MOD 2 adder output is a ONE, enabling input 7 of A4-8. The leading (positive-going) edge of the next KG pulse triggers A4-8 to the ONE state, placing a ZERO on input 7 of A4-15B; the output of A4-15B is held at ZERO,

however, by the ONE on input 6. A4–16B maintains the ONE enable on A6–1 and the F DRIVE pulses continue to be generated. Now assume that the MOD 2 adder output goes to ZERO. A4–8 will remain in the ONE state for one baud time until the next KG pulse. During this interval both inputs to A4–15B are ZERO, forcing A4–15B to deliver a ONE to A4–16B. The output of A4–16B goes to ZERO, disabling A6–1 and causing one F DRIVE pulse to be deleted. The next KG pulse resets A4–8 to ZERO, and the F DRIVE pulses are again generated in the normal manner.

(d) As stated previously, two successive F DRIVE pulses cannot be deleted. The reason for this is that SPECIAL POINT U cannot remain at ZERO for more than one baud time; as will be evident from an examination of the waveform chart of figure 4–68. The A4–8 output is the complement of the MOD 2 adder output, but delayed one baud time. SPECIAL POINT U is a ZERO disable only when these two outputs are simultaneously ZERO and since this condition can only exist for one baud time. SPECIAL POINT U can only have a duration of one baud time. Therefore, only a single F DRIVE pulse can be deleted.

c. *Secondary Key Generating Circuit (fig. 4–69).* The secondary key generating circuit combines the outputs from the primary key generating circuit to produce two secondary key timing pulses, X and W. The logic comprises a $\overline{q}\cdot\overline{r}$ reentry adder, an accumulator, a Y delay, a P delay, a Y·P adder, and a Y·S adder.

(1) *$\overline{q}\cdot\overline{r}$ re-entry adder.*—The $\overline{q}\cdot\overline{r}$ re-entry adder consists of two inverters (A4–18 and A4–19) and two NOR gates (A4–20A and A4–20B). It is a re-entry adder which adds the output of the $\overline{q}$ and $\overline{r}$ combiners to produce $\overline{T}$. The output of the adder is a ZERO when $\overline{q}$ and $\overline{r}$ are opposite in polarity, and a ONE when $\overline{q}$ and $\overline{r}$ are the same polarity.

(2) *Accumulator.*—The accumulator (A4–11A, A4–11B, and A4–10) is a gated flip-flop which changes its state when pulsed by a KG DRIVE pulse only if $\overline{T}$ is ZERO. $\overline{T}$ is applied to NOR gates A4–11A and A4–11B. Input 9 of A4–11B is connected to the ZERO side output of A4–10, while input 6 of A4–11A is connected to the ONE side output of A4–10. A4–10 will complement when triggered by a KG DRIVE pulse only when the output of the gate connected to the non-conducting side is a ONE. A4–10 has been initially set to ONE by a SET pulse from the extensor and control, so that a ZERO enable exists on input 9 of A4–11B. The initial polarity of $\overline{T}$ depends upon the arrangement of the permuter patch cords. Assume that $\overline{T}$ is a ONE. This places a ZERO disable on inputs 2 and 7 of A4–10 and prevents KG from triggering A4–10. Now assume that $\overline{T}$ becomes ZERO, and enabling input 8 of A4–11B. The output of A4–11B becomes ONE, enabling input 2 of A4–10. KG sets A4–10 to ZERO, placing a ZERO enable on input 6 of A4–11A. If $\overline{T}$ remains ZERO until the next KG pulse, A4–10 will be set to ONE due to the ONE enable on input 7. A4–10 will remain in the ONE state until the $\overline{T}$ goes to ZERO, again enabling A4–11B, and A4–10 is complemented by the KG pulse.

(3) *Y delay.*—The Y delay (flip-flop A4–9) gives the same output as the accumulator but delayed one baud time. The accumulator output determines whether the state of A4–9 will be changed by KG. A4–9 is initially set to the ONE state by the set pulse. Since input 7 of A4–9 is a ONE enable due to the initial ONE set of A4–10, the KG pulses can do nothing more than verify the existing ONE state. When A4–10 changes state, input 7 of A4–9 becomes a ZERO disable, while input 2 becomes a ONE enable. One baud time later, KG sets A4–9 to ZERO. Subsequent KG pulses are ineffective until A4–10 again changes state, restoring the ONE enable on input 7 of A4–9. One baud time later, KG sets A4–9 to ONE.

(4) *P delay.*—The P delay circuit (flip-flop A3–7 and inverter A3–21) delays the P output from the primary key generating circuit for one baud time, i.e., the interval between

two KG pulses. Operation of the P delay is essentially the same as the Y delay, except that the complementary input gate signals for A3-7 are derived from an inverter (A3-21) instead of a flip-flop.

(5) *Y·P adder.*—The Y·P adder, A3-15A and A3-15B, is a MOD 2 adder which adds the outputs of the Y and P delay circuits to produce secondary key signal X. Operation of this circuit is the same as that of the MOD 2 adder described in the drive pulse generating circuit except that the required complementary input signals are obtained from flip-flops instead of inverters.

(6) *Y·S adder.*—The Y·S adder, A3-19, A3-18A, and A3-18B, is a MOD 2 adder which adds YN−1 and s to produce secondary key signal W. The complement of one signal, $\overline{YN-1}$, is derived from a flip-flop (A4-9) instead of the usual inverter.

d. *Auto Key Circuit (fig. 4-70).*—The auto key circuit increases key depth by generating a modified key signal which is a function both of the previously transmitted cipher Z1, and the secondary key signal X. This modified key signal is called the auto key, or V. The auto key circuit comprises the E gate, the Z1 gate, the X·Z adder, the auto key register the auto key drive inhibitor, the auto key drive generator, and the $\overline{V}$ combiner.

(1) *E and Z1 gates.*—The E gate (A3-14) and the Z1 gate (A3-17 and A3-19) control the flow of information into the X·Z adder (A3-11, A3-12A, A3-10A, A3-10B). In receive normal operation, $\overline{\text{NORMAL 3}}$ and SEND 2 are both ZERO, enabling E gate A3-14. These ZEROs also enable inputs 8 and 9 of NOR gate A3-17, causing A3-17 to place a ONE disable on input 8 of Z1 gate A3-19. The $\overline{E}$ or $\overline{Z}$ input to the X·Z adder at this time consists of $\overline{E}$. In send normal operation, the E gate is disabled by SEND 2, which is ONE at this time, while the Z1 gate is enabled by the ZERO output of NOR gate A3-17. The $\overline{E}$ or $\overline{Z}$ input to the X·Z adder will now be $\overline{Z1}$.

(2) *X·Z adder.*—The X·Z adder generates an L signal by performing a MOD 2 addition of the X key stream and the $\overline{E}$ or $\overline{Z}$ output of the E or Z1 gate. This L signal steers flip-flop A3-2 in the auto key register; if a ONE L enables input 7 of A3-2, the ZERO $\overline{L}$ output of inverter A3-9A disables input 2 of A3-2, allowing the A KEY DRIVE pulse to set A3-2 to the ONE state. A3-2 remains in the ONE state until L becomes ZERO and $\overline{L}$ becomes ONE, after which time the A KEY DRIVE pulse sets A3-2 to ZERO.

(3) *Auto key register.*—The auto key register, (Q register) consists of flip-flops A3-2 through A3-6. It is a conventional five-stage shift register. A3-2 through A3-4 is set to the ONE state and A3-5 through A3-6 is set to the ZERO state by a SET pulse from the extensor and control. When the register is triggered by the A KEY DRIVE pulses, a pattern of ONEs and ZEROs is shifted through the register from left to right. The register is so arranged that each flip-flop, except A3-2, changes its state upon receipt of an A KEY DRIVE pulse, if the preceding stage is in the opposite state. Each output from the shift register forms one input to the $\overline{V}$ combiner.

(4) *Auto key drive inhibitor.*—The auto key drive inhibitor (NOR gate A3-8A) inhibits the auto key drive generator at all times except during the time of the five information bits of each character. The $\overline{M}$ signal on input 8 is ZERO whenever a character is being received or transmitted. START, on input 6, is ZERO except during the start bit of each character. STOP, on input 7, is ZERO except during the stop bit of each character. Therefore, the only time that the output of A3-8A is a ONE enable for input 2 of flip-flop A3-1 is during the five information bits of a character.

(5) *Auto key drive generator.*—The auto key drive generator (flip-flop A3-1 and inverter A3-8B) generates the A KEY DRIVE pulses which drive the auto key register. These pulses have the same repetition rate as the KG pulses. They occur only when input 2 is enabled by a ONE from the auto key drive inhibitor. A3-1 is initially set to the ONE state by a SET pulse from the extensor and control. Output 3 of A3-1

now places a ZERO disable on input 7, preventing $\overline{KG}$ from triggering A3–1 as long as input 2 is ZERO. When input 2 becomes ONE (during the five information bits of a character), $\overline{KG}$ sets A3–1 to the ZERO state, making output 3 of A3–1 a ONE. This ONE enables input 7 of A3–1 and drives the A KEY DRIVE output of inverter A3–8B to ZERO. A KEY DRIVE remains ZERO until the next ZERO-to-ONE transition of KG sets A3–1 to ONE. A KEY DRIVE simultaneously goes to ONE and triggers the auto key register.

(6) *$\overline{V}$ combiner.*—The $\overline{V}$ combiner, composed of NOR gates A3–9B, A3–11B, A3–12B, and A3–13, combines the X and $\overline{X}$ signals, from the secondary key generating logic, with the outputs of the auto key register, producing a signal arbitrarily called $\overline{V}$. $\overline{V}$ can be expressed logically as $\overline{V} = (Q1 \cdot \overline{Q4} \cdot \overline{X}) + (\overline{Q1} \cdot Q2 \cdot \overline{Q5}) + (\overline{Q3} \cdot Q5 \cdot X) + (\overline{Q2} \cdot Q3 \cdot Q4)$.

e. Final Key Generating and Key Adding Circuit (fig. 4–71).—The final key generating and key adding circuit performs two functions. It generates the final key signal (K), and also adds this signal to plain text to produce cipher, or to cipher to produce plain text. Principal circuits are the final key generator, the key adder, and the start-stop gate.

(1) *Final key generator.*—The final key generator is the W·V adder which comprises A3–13, A3–14, A3–20A, and A3–20B. This adder performs a MOD 2 addition of the secondary key signal W, from the secondary key circuit, and the $\overline{V}$ auto key stream from the auto key circuit. This MOD 2 addition produces the final key signal K, which is applied to the key adder. Two additional outputs, $\overline{W}$ and V, are applied to the alarm circuit.

(2) *Key adder.*—The key adder, comprising A3–17A, A3–16A, and A3–16B performs a MOD 2 addition of final key K and the E output from the data extensing circuit. It should be remembered that E will be plain text during send operation and cipher during receive operation. Thus, during send the MOD 2 addition of E and K gives cipher while during receive the same process gives plain text. The output of the key adder, Z1, is applied to the start-stop gate and to the key alarm circuit.

(3) *Start-stop gate.*—The start-stop gate, comprising inverter A3–19A and NOR gates A13–19B and A13–18A, ensures that the start and stop bauds of a character will be transmitted in plain text. A13–19B is disabled by a ONE START only during the start baud of a character. A13–18A is disabled by a ONE STOP only during the stop baud of a character. Therefore, the Z1 output of the key adder is transmitted through A13–19B and A13–18A to Z2 inverter A13–17B and Z3 inverter A13–18B at all times except during the start and stop bauds of a character. Z2 inverter A13–17B inverts the output of A13–18A and delivers a Z2 signal to the line and loop output circuits. Z2 will be plain text if the KW–7 is receiving and cipher if the KW–7 is transmitting. Z3 inverter A13–18B delivers a Z3 signal, which is identical with Z2, to the Fibonacci feedback circuit.

f. Fibonacci Feedback, Loop Output, and Line Output Circuit (fig. 4–72).—The Fibonacci feedback, loop output, and line output circuit performs the following three functions: 1) provides feedback to the Fibonacci which causes the Fibonacci register to start at a random point in its cycle, 2) controls the flow of information to the loop output circuit, and 3) controls the flow of information to the line output circuit. The following discussion is broken down according to the three functions.

(1) *Fibonacci feedback circuit.*—The Fibonacci feedback circuit provides random generation of the initial key stream produced by the Fibonacci shift register. The circuit consists of a power amplifier, the feedback Z gate, the feedback 35 gate and the Fibonacci feedback adder.

(a) Feedback 35 gate A4–12A and feedback Z gate A4–12B, in conjunction with power amplifier A4–21, control the $\overline{35}$ or $\overline{Z3}$ input to the Fibonacci feedback adder. During phasing and indicator NORMAL 2 is ZERO, the $\overline{NORMAL\ 3}$ out-

put of power amplifier A4–21 is ONE, A4–12B is enabled, and A4–12A is disabled. The output of A4–12B at this time is $\overline{Z3}$, which is applied to the Fibonacci feedback adder. During normal operation, NORMAL 2 is ONE, the $\overline{\text{NORMAL 3}}$ output of power amplifier A4–21 is ZERO, A4–12B is disabled, and A4–12A is enabled. The output of A4–12A at this time is $\overline{35}$, which is applied to the Fibonacci feedback adder.

(b) The Fibonacci feedback adder, comprising A4–13, A4–14A, and A4–14B, generates an A signal which is the result of a MOD 2 addition of the 39th Fibonacci stage output and either $\overline{35}$ or $\overline{Z3}$. During indicator operation, the A signal is 39 $\oplus$ Z3 while during normal operation A is 39 $\oplus$ 35. In either case, the A signal determines the pattern of ONEs and ZEROs which will be shifted through the Fibonacci shift register.

(2) *Loop output circuit.*—The loop output circuit gates the plain message to the loop circuit during both send and receive operations. Major circuits are the loop Z2 gate, the gated loop in gate, the bit rate gate, and the loop output register.

(a) *Loop Z2 gate.*—The loop Z2 gate, A11–4A, passes Z2 only when Z2 consists of plain text, that is, only when a character is being received during normal receive operation. Gating signals to A11–4A are SEND, $\overline{\text{NORMAL 2}}$ and LOCO. SEND is a ONE disable during send operation and a ZERO enable during receive normal. $\overline{\text{NORMAL 3}}$ is a ZERO enable during normal phase of both send and receive operations. LOCO is a ZERO enable only during the time a character is being received or transmitted. Therefore, A11–4A produces an inverted Z2 signal only during the time a character is being received in normal phase of operation. If any input to A11–4A becomes a ONE, the output of A11–4A becomes a ZERO.

(b) *Gated loop in gate.*—The gated loop in gate, A11–4B, passes the GATED LOOP IN signal only when the latter consists of plain text information, that is, only during send operation. A11–4B also inhibits GATED LOOP IN when an ALARM signal is generated by the alarm circuit, thus preventing the possibility of transmitting information after a malfunction occurs. Gating signals to A11–4B are $\overline{\text{SEND 1}}$ and ALARM. $\overline{\text{SEND 1}}$ is a ZERO enable only during send operation. ALARM is a ZERO enable except when the alarm circuit detects a malfunction. Therefore, A11–4B produces an inverted GATED LOOP IN ($\overline{\text{LOOP IN}}$) signal when the KW–7 is sending properly.

(c) *Bit rate gate.*—Bit rate gate A11–13A and A11–13B allows loop output register A11–12 to be triggered by IBR pulses during send operation, or by OBR1 pulses during receive operation. In send operation, $\overline{\text{SEND 1}}$ is a ZERO enable on input 9 of A11–13A, while SEND 1 is a ONE disable on input 7 of A11–13B. Under these conditions, A11–13B transfers inverted IBR pulses while A11–13A is disabled. In receive operation, $\overline{\text{SEND 1}}$ is a ONE disable on input 9 of A11–13B, while SEND 1 is a ZERO enable on input 7 of A11–13A. A11–13A now produces an inverted OBR1 pulse.

(d) *Loop output register.*—Loop output register A11–12 stores the LOOP OUT information until triggered by the pulses from A11–13A or A11–13B. A11–12 is initially set to the ONE state by a SET pulse on input 12. If $\overline{\text{LOOP IN}}$ is ZERO, input 2 of A11–12 will be disabled, while a ONE from inverter A11–11 will enable input 7. The next LOOP OUT DRIVE pulse therefore can do no more than verify the existing ONE state of A11–12. However, if $\overline{\text{LOOP IN}}$ is ONE, input 2 is enabled and input 7 is disabled. The next LOOP OUT DRIVE pulse sets A11–12 to the ZERO state, where it will remain until triggered back to the ONE state by the first LOOP OUT DRIVE pulse to occur after $\overline{\text{LOOP IN}}$ returns to ZERO. The output of A11–12 is the LOOP OUT digital signal (LOOD).

(3) *Line output.*—The line output circuit gates the transmitted message to the line output circuit. The circuit comprises the following circuits: line E gate, line Z2 gate, GZO–GEO gate, and the line output register.

(a) *Line E gate.*—Line E gate A13–16B supplies phasing and indicator information (E) to the line output register during the phasing and indicator phases of send operation. The $\overline{S \cdot N}$ signal applied to input 9 of A13–16B is a ZERO enable only during phasing and indicator phases of send operation. At this time, the E output of inverter A13–17, which is applied to input 10 of A13–16B, is inverted to form the GEO (gated E out) signal. GEO is applied to input 6 of GZO–GEO gate A5–5A, and to the alarm circuit.

(b) *Line Z2 gate.*—Line Z2 gate A13–16A passes plain or ciphered information (depending on the mode of operation) to the line output register during send normal operation. Gate signals applied to A13–16A are $\overline{\text{NORMAL 3}}$ and $\overline{\text{M. NORMAL 3}}$ is a ZERO enable during normal phase of operation, while $\overline{M}$ is ZERO when information is being transmitted or received. Therefore, when information is available during send operation, A13–16A inverts the Z2 signal to form GZO (gated Z out), which is fed to input of GZO–GEO gate A5–5A.

(c) *GZO–GEO gate.*—GZO–GEO gate A5–5A supplies inverted GEO pulses to inverter A5–5B during phasing and indicator phases of send operation and inverted GZO pulses during normal operation. The output of A5–5A is applied directly to input 7 of line output register A12–17; it is also inverted by inverter A5–5B and applied through contacts 7 and 4 of normally energized relay A5K1 to input 2 of A12–17. Relay A5K1 is energized in the following manner: ALARM and $\overline{\text{SEND 1}}$, on inputs 8 and 9 of NOR gate A5–11A, are both ZERO when the KW–7 is sending properly. The resulting ONE output from A5–11A drives the output of NOR gate A5–11B to ZERO. This in turn drives the output of power amplifier A5–9 to ONE, placing an energizing potential across the coil of A5K1. If the KW–7 goes into receive operation, or if an alarm condition occurs, $\overline{\text{SEND 1}}$ or ALARM will become ONE, driving the output of A5–11A to ZERO. This ZERO, in combination with the normally ZERO PLAIN signal on input 7 of A5–11B, places a ONE on the output of A5–11B and a ZERO on the output of A5–9. A5K1 becomes deenergized, disabling input 2 of line output register A12–17. In addition, the ONE ALARM signal is fed via contacts 2 and 8 of K1 to the BUZ 1 line. The diode across the coil of A5K1 protects power amplifier A5–9 by providing a path for the negative surge which appears on terminal 1 of K1 at the instant A5K1 is deenergized. This also insures that the relay is immediately deenergized when an alarm condition occurs.

(d) *Line output register.*—Line output register A12–17 stores the line out information until OBR2 time. A12–17 is initially set to the ONE state by a SET pulse from the extensor and control. If the line output from GZO–GEO gate A5–5A is ONE, OBR2 cannot trigger A12–17. However, when the line output from A5–5A becomes ZERO, a ZERO disable is placed on input 7 of A12–17, and a ONE enable is applied to input 2 via inverter A5–5B and contacts 4 and 7 of K1. OBR2 now sets A12–17 to the ZERO state. A12–17 remains in the ZERO state as long as the line output is ZERO. After line out returns to ONE, the first OBR2 pulse resets A12–17 to ONE. If a break condition occurs, a ONE BRK signal will collector-set output 3 of A12–17 via diode A12–16. This signal will hold A12–17 in the ZERO state until break condition is eliminated.

g. Fibonacci, I&N Failure and PTS Alarm Circuit (fig. 4–73).—The Fibonacci, I&N failure and PTS alarm circuit generates an alarm indication if 1) the W stream does not undergo at least on ZERO-to-ONE transition during a given eight character period, 2) the 39 stream does not undergo a transition from ZERO to ONE or ONE to ZERO during a given eight

character period, 3) the A stream does not become ONE at least during a given eight character period, (which means that the Fibonacci is generating an alternating output), 4) The I&N flip-flop fails to generate a ONE in the normal mode of operation, 5) 10 seconds elapses with no data transmission in the send plain mode (This condition is optional). The following circuit comprises the Fibonacci and I&N failure alarm.

(1) *Fibonacci alarm.*—The Fibonacci alarm consists of the alarm generator, the Fibonacci and W activity monitor and the Fibonacci alternation detector.

(a) *Alarm generator.*—The alarm generator is made up of NOR gate A5–4A, inverter A5–4B, AND gates A5–12C and A5–12B, alarm control flip-flop A5–10, inverter A5–8B, and lamp driver A5–9. Flip-flop A5–10 is initially set to the ZERO state by a SET pulse from the extensor and control. This produces a ZERO ALARM signal at output 10 of A5–10, a ZERO ALARM 1 at output 2 and 14 of inverter A5–8B, and a ZERO at outputs 6 and 10 of lamp driver A5–9. The ZERO ALARM 1 enables the gated loop in gate in the fibonacci feedback, loop output, and line output circuit. A5–10 can be set to the ONE state (including an alarm condition) by a ONE pulse from AND gate A5–12C, by a ONE pulse from AND gate A5–12B. AND gate A5–12B produces a ONE pulse if there is GEO (gated E out) activity when the KW–7 is in the normal mode. The following paragraphs describe how these situations can occur.

(b) *Fibonacci and W alarm monitor.*—The Fibonacci and W alarm monitor consists of the following circuits: CTRP gate A13–1B; ÷8 counter A13–2, A13–3, A13–4 and power amplifier A13–10; W stream monitor A5–2, P stream monitor A5–1; AND gate A5–12A and ACT gate A13–20B, A13–21A, A13–19, and A13–21B. The Fibonacci and W alarm monitor generates an alternation sample pulse (ASP) which undergoes a ZERO-to-ONE transition once every 8 characters (56 bauds), and uses this pulse to examine the activity of the W and 39 streams. The Fibonacci and W alarm monitor also generates the activity signal (ACT) which provides the KW–7 with the system capabilty of providing an indication when transmitting plain text information. This indication (ACT) is found at the PTS (Plain Text Safety) connector, J6.

1. I&N, on input 9 of inverter A13–1A, is a ONE during indicator and normal phases of operation, making the $\overline{\text{I\&N1}}$ signal on input 7 of CTRP gate A13–1B a ZERO enable. PLAIN, on input 8 of A13–1B, is a ZERO enable if the KW–7 is in the cipher mode. Therfore, A13–1B produces a ONE pulse at the CTRP rate. This pulse is applied to the ÷ 8 counter where its repetition rate is divided by eight to give an $\overline{\text{ASP}}$ pulse which occurs once every 8 characters. Power amplifier A13–10 inverts $\overline{\text{ASP}}$ to form ASP, which is applied to W stream monitor A5–2, P stream monitor A5–1, Fibonacci alternation detector A5–3, and gate A5–12C.

2. W stream monitor A5–2 may initially go to the ONE or ZERO state. Assume that A5–2 goes to the ZERO state, placing a ONE enable on its own input 7. At some later time, ASP sets A5–2 to the ONE state, making the W ALARM output a ONE. This ONE drives the output of NOR gate A5–4A to ZERO, which in turn drives the output of inverter A5–4B to ONE, enabling input 10 of AND gate A5–12C. A5–12C, however, does not produce a ONE at this time because the ONE enable on input 10 must be available at least 40 microseconds before ASP. Returning to A5–2, the $\overline{\text{AT2A}}$ signal on input 2 is ONE enable except during testing. If the W stream is being generated properly, a ZERO-to-ONE transition of $\overline{\text{W}}$ will occur before the next ASP pulse and will set A5–2 back to ZERO, removing the ONE enable on input 10 of AND gate A5–12C. This prevents A5–12C from generating a ONE at ASP time, which would set alarm control flip-flop A5–10 to the ONE state and cause an alarm indication.

If, however, the W stream has no activity, a ZERO-to-ONE transition will not occur before the next ASP pulse, and the ONE enable will remain on input 10 of A5–12C. At ASP time, A5–12C produces a ONE which sets A5–10 to ONE, generating an alarm indication.

3. P stream monitor A5–1 operates in a manner similar to the W stream monitor, with the difference that the only requirement for proper P stream generation is a transition either from ONE to ZERO or from ZERO to ONE during a given 8-character period. $\overline{\text{ATIA}}$, on input 2 of A5–1 and input 18 of AND gate A5–12A, is a ONE enable except during testing. If a P stream transition occurs between two ASP pulses, either $\overline{\text{P}}$ or P will go from ZERO to ONE. If $\overline{\text{P}}$ (39) goes from ZERO to ONE, A5–1 will be set to the ZERO state via input 1; if P (39) goes from ZERO to ONE, A5–1 will be set to ZERO via AND gate A5–12A.
4. ACT gate A13–20B provides the ACT signal which is applied to the PTS (plain text safety) circuit. When transmitting plain text, ACT is a varying signal whose content depends on the character being transmitted. When the equipment is in the plain send mode and no data is transmitted, the ACT signal is a ONE. If this condition persists for 10 seconds, the PTS circuit generates a signal which inhibits the loop input circuit. The SEND 2 signal from the send phasing circuit is applied through power amplifier A13–21B and truncated diode A13–19 to terminal 4 of A13–20B. In the send mode SEND 2 is a ONE. The power amplifier inverts the signal and a ZERO is coupled to terminal 4 of the ACT gate. Another input to the ACT gate is the PLAIN signal which is inverted by power amplifier A13–21A and applied to terminal 9 of A13–20B. When sending plain text PLAIN is a ONE. Because of the inversion performed by the power amplifier a ZERO is coupled to terminal 9 of the ACT gate. Since these two inputs are ZEROs, the output of the ACT gate is determined by the remaining input, the $\overline{\text{ABIN}}$ signal. $\overline{\text{ABIN}}$ varies with the input data being transmitted from the input teletypewriter. When $\overline{\text{ABIN}}$ is a ZERO, ACT is a ONE. Conversely, when $\overline{\text{ABIN}}$ is a ONE, ACT is a ZERO. When no data is being transmitted, $\overline{\text{ABIN}}$ is a ZERO and the ACT signal is a ONE. After a 10-second period of no transmission, the PTS circuit (if active) inhibits the loop input.

(c) *Fibonacci alternation detector.*—The Fibonacci alternation detector (A5–3) causes an alarm indication if the Fibonacci begins to generate an alternating output.

1. Inputs to the Fibonacci alternation detector are an ASP pulse which occurs once every 8 characters, a KG pulse which occurs at the start of each baud, and an A signal which the Fibonacci generates by performing a MOD 2 (EXCLUSIVE OR) addition of the outputs of stages 35 and 39. As long as the Fibonacci is operating properly, A will be a ONE for at least one baud during a given 8 character interval. When A is ONE, input 2 of flip-flop A5–3 is enabled, allowing a KG pulse to set A5–3 to the ZERO state. This places a ONE on output 3 and a ZERO on output 10. The ONE on output 3 enables input 7, allowing the next ASP pulse to reset A5–3 to the ONE state. Output 10 of A5–3 now becomes a ONE which drives the output of NOR gate A5–4A to ZERO. This ZERO is inverted to a ONE by inverter A5–4B, enabling input 10 of AND gate A5–12C. However, due to the inherent delay through A5–4A and A5–4B, this ONE enable arrives too late to open A5–12C for the same ASP pulse which triggered A5–3. If the Fibonacci is operating properly, some activity will occur before the arrival of the next ASP pulse, so that the A signal will at some time enable input 2 of A5–3, allowing KG to set A5–3 to the ZERO state. When A5–3 returns to the ZERO state, the ONE enable is removed from input 10 of AND gate A5–12C, and the next ASP pulse is prevented from

generating a ONE at the output of A5-12C. If, however, no Fibonacci activity occurs between the time A5-12C is enabled and the arrival of the next ASP pulse, the next ASP pulse generates a ONE at the output of A5-12C. This ONE triggers alarm flip-flop A5-10, causing an alarm indication.

2. The circuity which develops the A pulse is capable of detecting pure alternation in the following manner. If the Fibonacci is generating a pure alternation, stages 35 and 39 will always be in the same state at any particular instant, as shown below:

Stage	35	36	37	38	39
State	1	0	1	0	1
	0	1	0	1	0

Since the A pulse is developed by an EXCLUSIVE OR addition of the outputs of stages 35 and 39, and since these outputs are always identical, the A pulse is always ZERO. Therefore, A pulse cannot enable input 2 of flip-flop A5-3, and the ONE on output 10 of A5-3 will remain. This ONE enables AND gate A5-12C as described in the previous paragraph. Upon receiving an ASP pulse, A5-12C triggers flip-flop A5-10, which in turn generates an alarm indication.

(2) *I&N alarm detector.*—The I&N alarm detector, A5-8A, triggers an alarm indication if the I&N flip-flop is not set to ONE during the normal mode of operation (this is a prerequisite for activity in the Fibonacci register). The inputs to A5-8A are $\overline{\text{NORMAL 2}}$ and I&N. During normal operation $\overline{\text{NORMAL 2}}$ is a ZERO. If, for any reason, I&N is also a ZERO, a ONE is generated at the output of A5-8A. This is an enable signal which is applied to input 7 of alarm flip-flop A5-10. The next $\overline{\text{OBR1}}$ pulse sets A5-10 to ONE generating an alarm indication. An additional alarm function is provided by a signal from the Fibonacci feedback alarm circuit. Generation of this signal is discussed in a following paragraph.

h. Fibonacci Feedback Alarm Circuit (fig. 4-74).—The Fibonacci feedback alarm logic checks the operation of the Fibonacci feedback circuit by comparing the A output with another signal which will always be the complement of A if A is being generated properly. The circuit consists of the Z2 gate, the 35 gate, the 39·A adder, and the Fibonacci feedback comparator.

(1) *Z2 gate and 35 gate.*—Z2 gate A5-15A and 35 gate A5-16A have a common output which is connected to input 9 of inverter A5-15B and input 7 of NOR gate A5-17A. At any given time either the Z2 gate or the 35 gate, but not both, will be enabled. The Z2 gate is enabled by a ZERO NORMAL 2 during indicator. At this time the input to inverter A5-15B and NOR gate A5-17A will be $\overline{\text{Z2}}$. The 35 gate is enabled by a ZERO $\overline{\text{NORMAL 2}}$ during normal operation, so that the input to A5-15B and A5-17A at this time is $\overline{35}$.

(2) *39·A adder.*—The 39·A adder performs a MOD 2 addition of the 39 signal from the Fibonacci, and the A signal which is fed back to the first stage of the Fibonacci. The 39 $\oplus$ A output of the 39·A adder is applied directly to input 10 of NOR gate A5-17A and through inverter A5-18B to input 3 of NOR gate A5-17B.

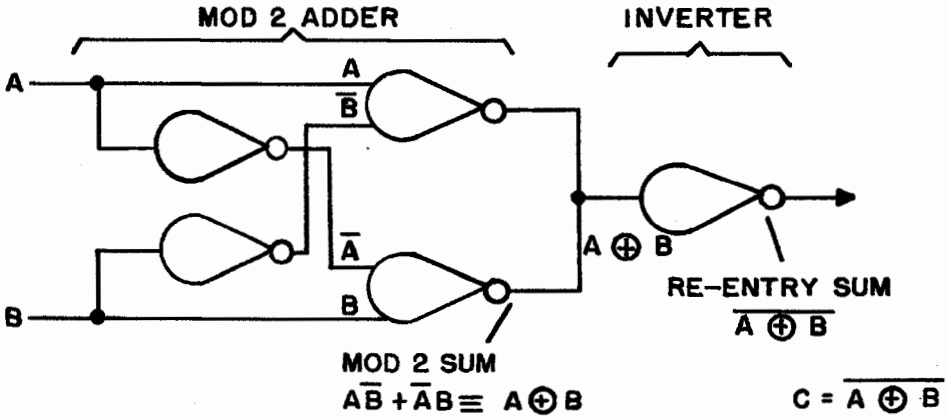
(3) *Fibonacci feedback comparator.*—The Fibonacci feedback comparator (A5-15B, A5-18B, A5-17A, A5-17B) performs a re-entry addition of 39 $\oplus$ A and $\overline{\text{Z2}}$ or $\overline{35}$. Re-entry (EXCLUSIVE NOR) addition can be considered as the complement of MOD 2 (EXCLUSIVE OR) addition, as shown below:

Inputs = A and B						Output (sum) = C
MOD 2:	$C = A\overline{B}$	+	$\overline{A}B$	$\equiv$	$A \oplus B$	
Re-entry:	$C = AB$	+	$\overline{A}\,\overline{B}$	$\equiv$	$\overline{A \oplus B}$	

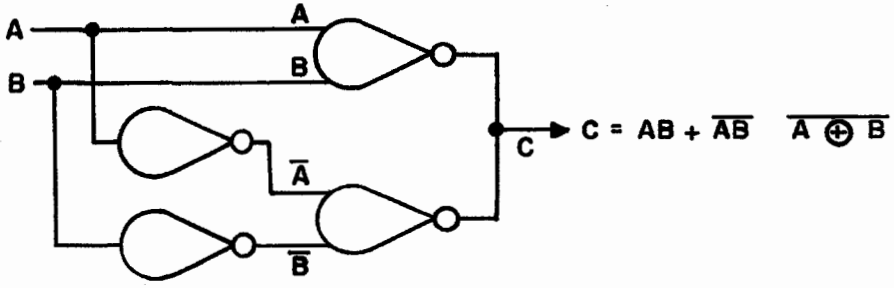
Exclusive NOR Truth Table

Input A	Input B	AB	$\overline{AB}$	Sum C = AB + $\overline{AB}$ = $\overline{A \oplus B}$
0	0	0	1	0 + 1 = 1
0	1	0	0	0 + 0 = 0
1	0	0	0	0 + 0 = 0
1	1	1	0	1 + 0 = 1

Examination of the table above reveals that the re-entry sum $\overline{A \oplus B}$ is the complement of a MOD 2 addition of A and B. The MOD 2 adder can be modified to perform re-entry addition by connecting an inverter to the output, as shown below:



However, a simpler method is to rearrange the two input inverters, as is done in the feedback comparator:



The essential functional feature of the re-entry adder is that it outputs a ONE when the inputs are alike, and a ZERO when they are unlike. Operation of the Fibonacci feedback comparator can be more easily understood by examining the composition of the Fibonacci feedback signal A. During the indicator phase, A is formed by MOD 2 adding cipher and the output of stage 39 of the Fibonacci. During the normal phase, A is formed by MOD 2 adding the outputs of stages 35 and 39 of the Fibonacci. As

explained in a preceding paragraph, the common output of the Z2 and 35 gates during indicator is $\overline{Z2}$, and during normal is $\overline{35}$. Thus, during indicator, the feedback comparator performs a re-entry addition of $\overline{Z2}$ and 39 $\oplus$ A to obtain ZERO. During normal, the comparator performs a re-entry addition of $\overline{35}$ and 39 $\oplus$ A to obtain ZERO. From this it is seen that, as long as the Fibonacci feedback is being generated properly, the output of the feedback comparator will always be ZERO, and input 20 of AND gate A5-12 will never be enabled. However, if a malfunction occurs in the generation of the Fibonacci feedback, the output of the Z2 or 35 gate will at some time be different from the 39 $\oplus$ A output, causing the feedback comparator to produce a ONE enable to A5-12. At KG time, A5-12 produces a ONE pulse to the Fibonacci alarm circuit, triggering an alarm indication.

i. Key Alarm Circuit (fig. 4-75).—The key alarm logic checks the formation of the key signal. The circuit consists of the alarm W·V adder, the alarm key adder, and the key comparator. In order to understand the operation of the key alarm circuit, it will be helpful to recall that final key is obtained by MOD 2 adding the V and W streams from the secondary key generator, and that the MOD 2 sum of cipher and plain text equals the MOD 2 sum of the V and W streams from the secondary key generator.

(1) *Alarm W·V and alarm key adders.*—The alarm key adder (A5-14A and A5-14B) performs a MOD 2 addition of cipher Z1A and plain text E to produce K, while the alarm W·V adder performs a MOD 2 addition of V and W to produce K. The outputs of these two adders must always be equal if the KW-7 is operating properly.

(2) *Key comparator.*—The key comparator (A5-21A, A5-13A, A5-13B, A5-21B) performs a MOD 2 addition of the outputs from the alarm key adder and the alarm W ·V adder. As long as these two signals are identical, signifying correct circuit operation, the output of the key comparator will be ZERO. If a malfunction occurs, the signals will no longer be identical, and the comparator will pass a ONE to the alarm generator circuit. AT3A on inputs to A5-13B and A5-21B are to check the circuit during alarm test.

j. Alarm Test Switch (fig. 4-76).—The ALARM TEST switch provides a means for testing the operation of the Fibonacci and I&N alarm circuit, the alarm circuit, the Fibonacci alarm circuit, and the key alarm circuit.

(1) *OFF position.*—$\overline{AT1B}$, $\overline{AT2A}$, and $\overline{AT2B}$ are connected to ground via 3.6 K resistors. $\overline{AT1A}$ is connected to ground through a 300 ohm resistor.

(2) *Position 1.*—$\overline{AT1A}$ and $\overline{AT1B}$ are connected to −6 V via terminal 1 of deck C.

(a) $\overline{AT1A}$ is applied to the P stream monitor of the Fibonacci and loop activity alarm circuit (fig. 4-73), preventing the monitor from being reset at the required time. If the monitor is operating properly, it will produce a signal which permits the alarm generator to be set at ASP time, giving an alarm indication.

(b) $\overline{AT1B}$ is applied to the RNA1 motion detector (A13-5) in the alarm circuit, preventing the detector from being reset at the required time. If the detector is operating properly, it will produce a signal which will allow a motion alarm (MI) indication to be generated.

(3) *Position 2.*—$\overline{AT2A}$ and $\overline{AT2B}$ are connected to −6 V via terminal 2 of deck C.

(a) $\overline{AT2A}$ prevents the W stream monitor of the Fibonacci and loop activity alarm circuit from being reset at the required time. If the W stream monitor is operating properly, it will produce a signal which allows the alarm generator to be set at ASP time, giving an alarm indication.

(b) $\overline{AT2B}$ prevents the RNA2 motion detector (A13-6) of the alarm circuit from being reset at the required time. If the detector is operating properly, it will produce a signal which will allow a motion alarm indication to be generated.

(4) *Position 3.*—AT3A and AT3B (M2B) are connected to ground via terminal 3 of deck C.

(a) AT3A is applied through a diode to the output of SEND·NORMAL gate B in the alarm circuit. This causes the $\overline{S \cdot N}$ signal to enable the input of the MOD 2A adder. AT3A is also applied through diodes to the Fibonacci feedback adder. This causes the A stream to be a constant ZERO, thus checking the operation of the Fibonacci alternation detector.

(b) Simultaneously, AT3B (M2B) grounds the output of the MOD 2B adder. If the randomizer circuitry is operating properly, M2A activity will be present, so that when M2A goes to ZERO, the inputs to the MOD 2C adder are unequal and the MOD 2C adder produces a ONE which enables the motion indication flip-flop to be set to ONE at OBR2 time. This in turn will cause the MI lamp to be illuminated.

(5) *Position 4.*—AT4A and AT4B are connected to ground via terminal 4 of deck C.

(a) AT4A disables the Fibonacci feedback comparator (Fibonacci feedback alarm circuit)and the key comparator (key alarm circuit), preventing these circuits from triggering an alarm.

(b) AT4A is applied through a diode to the output of the MOD 2A adder in the alarm circuit, clamping the M2A signal to ground.

(c) Simultaneously, AT4B is applied to the output of SEND·$\overline{\text{NORMAL}}$ gate B in the alarm circuit, causing the $\overline{S \cdot N}$ signal to become a ZERO at the input of the MOD 2B adder. If the randomizer circuitry is operating properly, M2B activity will be present, so that when M2B goes to ZERO the inputs to the MOD 2C adder are unequal and the MOD 2C adder produces a ONE which enables the motion indication flip-flop to be set to ONE at OBR2 time. This in turn will cause the MI lamp to be illuminated.

(d) AT4B is also applied to AND gate A6–11 which permits the normal flip-flop in the normal generator circuit to be set to the ONE state, generating a ONE NORMAL 1 causing the GEO gate to trigger the alarm.

(6) *Position 5.*—AT5 and SOS are connected to ground via terminal 5 of deck C.

(a) AT5 disables one section of the 39 · A adder in the Fibonacci feedback alarm circuit, causing the ~~adder~~ NOR output to be a constant ZERO. If the Fibonacci feedback comparator is operating properly, it will generate a ONE output which will cause an alarm indication.

(b) With SOS connected to ground, a constant ONE is applied to SOS alarm detector A13–20. If this detector is working properly it will produce a ZERO output which will result in the generation of a motion alarm indication.

(7) *Position 6.*—AT6 (39·A) is connected to ground via terminal 6 of deck C. AT6 makes the output of 39·A adder a constant ONE. (Refer to Fibonacci feedback alarm circuit.) If the Fibonacci feedback comparator is operating properly, it will generate a ONE output which will cause an alarm indication. (To perform this check, the unit must be in the SEND mode.)

(8) *Position 7.*—AT7 is connected to ground via terminal 7 of deck C. AT7 makes the output of the alarm W · V adder (key alarm circuit) a constant ONE. If the key comparator and alarm key adder are operating properly, the comparator will produce a ONE output which will trigger an alarm indication.

(9) *Position 8.*—AT8 is connected to ground via termianl 8 of deck C. AT8 makes the output of the alarm key adder (key alarm circuit) a constant ONE. If the alarm W·V adder and key comparator are operating properly, the comparator will produce a ONE output which will trigger an alarm indication.

(10) *Position 9.*—NORMAL 1 is connected to ground through terminal 10 of deck C. As a result of this, the $\overline{\text{NORMAL 2}}$ signal applied to I&N alarm detector A5–8 is a ZERO. At the same time a ground is applied to the power set circuit through terminal 10 of deck B. This results in the generation of a set pulse which sets the I&N flip-flop to ZERO.

Thus, the I&N signal which is applied to A5-8 is a ZERO. If A5-8 is operating properly, it will produce a ONE output which will trigger an alarm indication on input 7 of the alarm control flip-flop, which will generate an alarm indication.

(11) *Position 10.*—AT10A (ALARM 1) is connected to ground via terminal 10 of deck C. ALARM 1 (AT10A) is applied via contacts 2 and 8 of relay A5K1 (Fibonacci feedback, loop output, and line output circuit), to input 8 of NOR gate A13-8(audible alarm circuit). If the audible alarm circuit is operating properly, the audible indicator will produce a clock-frequency continuous tone.

(12) *Position 11.*—POWER SET is connected to ground via terminal 11 of deck C. POWER SET resets a portion of the KW-7 circuitry and triggers the SET and SET 1 generators. SET and SET 1 reset the remaining portions of the circuitry. This is done in order to remove abnormal conditions introduced during the alarm test procedure.

k. Randomizer and Alarm Circuit (fig. 4-77).—The randomizer and alarm circuit consists of the randomizer and its corresponding alarms. The randomizer generates a random sequence of ONEs and ZEROs during the indicator phase, while the alarm circuit performs a check of randomizer operation, giving a visible warning in case of malfunction. Principal circuits of the randomizer and alarm circuit are the following: two noise generators, two noise amplifiers, a gate control, a noise gate, eight inverter isolators, a MOD 2B adder, a MOD 2A adder, a MOD 2C adder, a motion indication flip-flop, and two motion detection flip-flops.

(1) *Noise generators.*—Noise generators A14-14 and A14-7 generate band limited random noise signals which are amplified by noise amplifiers A14-13 and A14-6. The outputs of the noise amplifiers are applied to noise gate A14-4, which is opened at $\overline{\text{OBR1}}$ time by gate control A14-11. When noise gate A14-4 is open, the output from A14-13, and its complement, are applied to flip-flop A14-12, while the output from A14-6, and its complement, are applied to flip-flop A14-5. Flip-flops A14-12 and A14-5 generate random noise outputs RNA1, $\overline{\text{RNA1}}$, RNA2, and $\overline{\text{RNA2}}$. These outputs, which may exist in any one of four possible configurations of ONEs and ZEROs, are applied via inverter isolators A14-10A, A14-10C, A14-9A, A14-9C, A14-2A, A14-2C, A14-3A, and A14-3C, to the MOD 2B adder (A14-8A and A14-8B), and to the MOD 2A adder (A14-1A and A14-1B).

Note: The KW-7 can function satisfactorily on only one noise generator. Two generators are used in order to avoid compromising system security in the event one generator fails.

(2) *MOD 2B adder.*—The MOD 2B adder (A14-8A, A14-8B), generates a random M2B signal which determines whether shift register A, in the data extensing circuit, will produce a ONE or a ZERO at any particular instant during indicator. M2B is formed by a MOD 2 addition of two random signals, RNA1 and RNA2, from the noise generating circuits. $\overline{\text{S}\cdot\text{N}}$ is applied via diodes A14-10B and A14-9B to inputs 5 and 3 and 4 and 10 of NOR gates A14-8A and A14-8B. $\overline{\text{S}\cdot\text{N}}$ is ZERO during phasing and indicator, enabling A14-8A and A14-8B. At this time, A14-8A and A14-8B MOD 2 add the outputs of isolators A14-10A, A14-10C, A14-9A, and A14-9C. These outputs are $\overline{\text{RNA1}}$, RNA2, $\overline{\text{RNA2}}$, and RNA1, respectively. The output of MOD 2 adder A14-8A and A14-8B is the M2B signal which triggers stage 2 of SRA in the data extensing circuit. Signal AT3B which is tied to the M2B line, is normally ZERO during operation, but can be made a ONE for testing by setting the ALARM TEST switch to position 4.

(3) *MOD 2A adder.*—The MOD 2A adder (A14-1A and A14-1B) generates a second random signal, M2A, which is identical to M2B. This signal is used to check the generation of M2B. $\overline{\text{S}\cdot\text{N}}$ is applied via diodes A14-2B and A14-3B to inputs 5 and 3 and 4

and 10 of NOR gates A14-1A and A14-1B. $\overline{S \cdot N}$ is ZERO during phasing and indicator, enabling A14-1A and A14-1B. At this time, A14-1A and A14-1B MOD 2 add the outputs of inverter isolators A14-2A, A14-2C, A14-3A, and A14-3C; these outputs are $\overline{RNA2}$, RNA1, $\overline{RNA1}$, and RNA2, respectively. The common output of A14-1A and A14-1B is the M2A signal which is applied to the MOD 2C adder. Test signal AT4A, tied to the M2A line, is normally ZERO but can be made a ONE for testing by setting the ALARM TEST switch to position 3.

(4) *MOD 2C adder.*—The MOD 2C adder (A13-14A, A13-13A, A13-14B, A13-13B) checks the operation of the MOD 2B adder by comparing its output with that of the MOD 2A adder. Since the MOD 2A and MOD 2B adders have identical inputs, their outputs should be identical at all times, and the MOD 2C output should be ZERO at all times. If a malfunction occurs in the M2B circuitry, M2B will no longer match M2A, and the MOD 2C output will become a ONE. This ONE will enable input 10 of AND gate A13-12A.

(5) *Motion Detection Flip-Flops.*

(a) AND gate A13-12A is used to set motion detection flip-flop A13-7 to the ONE state if the MOD 2C adder detects a difference between M2A and M2B. A ONE enable on input 10 of A13-12A allows the next OBR2 pulse to produce a ONE pulse on input 9 of A13-7. This ONE sets A13-7 to the ONE state, producing a ONE at input 7 of A13-20. A13-20 generates a ZERO which is applied to input 9 of lamp driver A13-11A. A13-11A produces a ONE (ground return) for the motion indication (MI) lamp, which becomes illuminated. This does not lockup the output of the KW-7.

(b) The MI lamp will also be illuminated, indicating a malfunction in the noise generating circuit, if RNA1 or RNA2 fail to undergo a transition from ZERO to ONE at least once every 8 characters. This indication occurs in the following manner: Signals $\overline{AT1B}$ and $\overline{AT2B}$ are ONES (except during testing), enabling input 7 of motion detection flip-flop A13-5 and input 2 of motion detector flip-flop A13-6. Assume that RNA1 and RNA2 are being generated satisfactorily, and are changing from ZERO to ONE at least once every 8 characters. The ZERO-to-ONE transitions trigger A13-5 and A13-6 to the ZERO state. This places a ZERO disable on pin 8 of AND gate A13-12B, a ZERO disable on pin 7 of motion indication flip-flop A13-7, a ONE enable on pin 2 of motion indication flip-flop A13-5, and a ONE enable on pin 7 of motion detection flip-flop A13-6. The next ASP signal, which occurs once for every 8 characters, is unable to trigger motion indication flip-flop A13-7 due to the ZERO disable on pin 7. However, the ASP signal is able to trigger motion detection flip-flops A13-5 and A13-6 due to the ONE enable on pins 2 and 7, respectively. This places a ONE enable on pin 8 of A13-12B and on pin 7 of A13-7. Assume a malfunction now occurs in the generation of the RNA1 pulse, and no transition from ZERO to ONE occurs before the arrival of the next ASP pulse. Flip-flop A13-5 remains in the ONE state, and continues to apply a ONE enable to AND gate A13-12B. The next ASP pulse reaches A13-7 via A13-12B, setting A13-7 to the ONE state. A13-7 turns on the MI lamp by way of A13-20 and lamp driver A13-11A, and a malfunction is indicated. Next, consider the alternative case where RNA1 is generated satisfactorily, but RNA2 fails. The previous ASP pulse triggered A13-6 to the ONE state, placing a ONE enable on pin 7 of A13-7. If RNA2 does not trigger A13-7 by undergoing a ZERO-to-ONE transition before the next ASP pulse, the next ASP pulse will trigger A13-7 to the ONE state, and the MI lamp will be turned on via A13-20 and lamp driver A13-11A.

(6) *SOS alarm.*—Gate A13-20, operating in conjunction with lamp driver A13-11A and the MI lamp, provides an alarm indication if the SOS signal becomes a constant ONE.

SOS is applied to input 6 of A13-20. If this signal is a constant ONE, a ZERO is coupled to the input of lamp driver A13-11A. This produces a ONE at the lamp driver output and illuminates MI lamp DS3. It should be noted that the normal SOS signal is a series of positive-going pulses of very brief duration. The duty cycle of this signal is so low that it cannot result in the illumination of the MI lamp.

(7) *Motion test.*—The motion detection and indication circuits may be tested by setting the ALARM TEST switch to positions 1 and 2. In position 1, the ALARM TEST switch places a ZERO disable on pin 7 of flip-flop A13-5, preventing this flip-flop from being set to the ONE state by RNA1. The first ASP pulse triggers A13-5 to the ONE state, placing a ONE enable on pin 8 of AND gate A13-12B. The second ASP pulse triggers A13-7 by way of A13-12B, and the MI lamp becomes illuminated. Similarly, when the ALARM TEST switch is in position 2, RNA2 is unable to set A13-6 to the ZERO state. The first ASP pulse sets A13-6 to ONE, placing a ONE enable on pin 7 of A13-7. The second ASP pulse sets A13-7 to ZERO, and the MI lamp becomes illuminated.

(8) *Motion stop.*—Since the random M2B pulses from the noise generating and MOD 2 adder circuits are required only during the indicator phase of operation, some provision must be made to stop the M2B pulses as soon as indicator is completed. This function is performed by send normal NOR gate B, A15-15. The two inputs to A13-15, NORMAL 3 and $\overline{\text{SEND 3}}$, are ZERO during indicator, placing a ONE on the input of power amplifier A13-11B. A13-11B inverts the ONE, placing a ZERO enable on A14-8A, A14-8B, A14-1A and A14-1B. At the end of indicator operation, NORMAL 3 becomes a ONE, giving a ZERO output from A13-15. A13-11B now places a ONE disable on A14-10B, A14-9B, A14-2B, and A14-3B, stopping the generation of M2A and M2B pulses.

l. Line Output Circuit (fig. 4-78).—The line output circuit converts the LIOD (line out digital) output of the line output register to a teletypewriter signal suitable for line transmission. When LIOD is a ONE, a mark is transmitted to the line and when LIOD is a ZERO, a space is transmitted to the line. The line output circuit comprises emitter follower DA1-Q1, differential amplifier, A18Q3 and A18Q4, line out relay A18K2, and ~~an~~ output filters. A18Q3 and A18Q4 form a differential amplifier which drives the two windings of line out relay A18K2. Operation of the differential amplifier is such that when one transistor is "on" (conducting heavily), the other is "off" (open circuit). When LIOD is a ONE, the emitter of Q1 is approximately at ground potential, making LIOA approximately +2 volts and LIORV approximately +0.5 volts. LIOA cuts off A18Q3 while LIORV turns on A18Q4, energizing the 2-3 winding of A18K2. A18K2 is a polar latching relay whose operation is similar to that of a flip-flop; for example, when the 2-3 winding is energized, the armature will go to pin 7 and remain there even though the energizing current is removed from the coil. When LIOD is a ZERO, the emitter of Q1 drops to approximately −6 volts, making LIOA approximately −3.5 volts and LIORV approximately −3 volts. LIOA turns on A18Q3, energizing the 1-8 winding of A18K2, while LIORV simultaneously turns off A18Q4, deenergizing the 2-3 winding of A18K2. The armature of A18K2 goes to pin 7 and stays there until LIOD again becomes a ONE. Resistors A18R7 and A18R8 and capacitors A18C3 and A18C4 comprise an arc-suppression network that protects the contacts of relay A18K2.

m. Loop Output Circuit (fig. 4-79).—The loop output circuit couples the LOOD (loop out digital) output of the loop output register to the local page printer. During send operation LOOD represents the plain text version of the message which is being transmitted, so that at this time the page printer produces local copy which can be used to monitor the loop-input information. During receive operation, LOOD represents the receive message in plain text form, so that the page printer at this time prints the message which originated at the sending KW-7. The loop output circuit comprises current source driver DA2-Q1, con-

stant current source A18Q7–Q8, differential amplifier, A18Q5–Q6, emitter follower DA1–Q2, and voltage regulator A18Q1.

(1) Current source driver DA2–Q1, regulates the operation of constant current source A18Q7–Q8, enabling these transistors to furnish a constant 20 or 60 ma current to the differential amplifier. For 20 milliampere operation, the LOOP CURRENT selector switch A14–S1 is set to the 20 MA position, connecting the base of DA2–Q1 to +6 V via DA2–R3 and DA2–R4; the emitter of A18Q7 is connected to +6 V via DA2–R4. Under these conditions, the current through DA2–Q1 is of such magnitude that the sum of the collector currents of Q7 and Q8 can be set to 20 milliampere by adjusting LOOP OUTPUT ADJUST R10. With the LOOP CURRENT selector switch set to 60 MA, the current through DA2–Q1 allows the sum of the A18Q7 and A18Q8 currents to be adjusted to 60 milliamperes. Almost all of the output current flows through the emitter-to-collector circuit of A18Q7, with A18Q8 contributing only a small portion of the total. Assume that the LOOP CURRENT selector switch is in the 20 MA position. If the output current attempts to rise above 20 milliamperes, the emitter current of A18Q7 will increase, making the lower end of DA2–R4 less positive. Since the base of DA2–Q1 obtains its bias from the drop across DA2–R4, the base current of DA2–Q1 will increase, causing DA2–Q1 to draw more collector current. This in turn will make the tap of IR10 more positive, reducing the base current of A18Q8. A18Q8 in turn reduces the base current of A18Q7, lowering the output current to its nominal value.

(2) When LOOD is a ONE, the emitter of DA1–Q2 is approximately at ground potential and the base of A18Q6 is one or two volts above ground. A18Q6 is cut off, and the full 20 or 60 milliampere output of the constant current source flows through A18Q5, the first filter, the selector magnet coil of the page printer, the second filter, DA3–L1 and A18R3 to −53 volt source.

(3) When LOOD is ZERO, the emitter of DA1–Q2 is at approximately −6 V and the base of A18Q6 is one or two volts negative. A18Q5 is cut off, and the entire 20 or 60 milliampere output of the constant current source is carried by A18Q6, A18R6, DA3–L1, and A18R3 to −53 V. This action acts as a dummy load on the power supply during the spacing condition, thereby creating a constant current demand from the power supply. In summary, when LOOD is ONE, the page printer selector magnet coil is energized, and when LOOD is ZERO the selector magnet coil is deenergized.

(4) Voltage regulator A18Q1 regulates the voltage applied to the differential amplifier. If the voltage at the junction of A18R3 and A18R4 becomes more negative, Zener diode DA3–CR1 conducts more heavily, supplying more base current to A18Q1. A18Q1 draws more current, pulling the junction of A18R3 and A18R4 back toward ground potential. If the voltage at the junction becomes more positive, the regulator draws less current and drives the junction in a negative direction.

4405. Remote Control Unit, Detailed Theory.—The following paragraphs discuss the detailed theory of remote control unit operation. The function of all switches, indicators and other internal components are described, as well as the control and data signals which enter or leave the remote control unit. The general relationship of remote control unit functions to system operation is also discussed.

a. General.—The remote control unit may be connected to the KW–7 by a cable with a maximum length of 500 feet to provide both remote control of the KW–7 and data paths between the KW–7 and the teletypewriter equipment.

b. Remote Control Unit Schematic Analysis (fig. 4–80).—Remote control of the KW–7 is possible, provided the KW–7 PCR switch is placed in the REMOTE position. With the KW–7 set for remote control the KW–7 SEND and BREAK switches are disabled. The

SEND and BREAK switches on the remote control unit now have remote control over the KW-7. In addition the remote control unit PC switch now assumes control of PLAIN and CIPHER modes.

(1) Now that the remote control unit is operational, the KW-7 applies several conditions on input jack J1 of the remote control unit. These are as follows: ground on pins J1-D and J1-g, −6 volts DC on pins J1-V and J1-f, −53 volts DC on pin J1-c, shield grounds on pins J1-T and J1-d, SEND RETURN (ground) on pin J1-F, BRGRR (ground) on pin J1-B, +6 volts DC on pin J1-a and a signal ground on pin J1-S.

(2) When the PC switch on the remote control unit is set to PLAIN ASYNC −6 volts DC is applied to illuminate the PLAIN light, a ONE PAR signal is sent out on pin J1-W, and a ZERO $\overline{\text{PAR}}$ signal is sent out on pin J1-Z.

(3) If the PC switch is set to the PLAIN SYNC position, the PLAIN light is illuminated again, the PAR signal is changed to a ZERO and the $\overline{\text{PAR}}$ is changed to a ONE and both are sent out for control in the KW-7.

(4) As the PC switch is changed from PLAIN SYNC to the CIPHER position, the PLAIN light is turned off and the CIPHER light is illuminated. In addition the PAR and $\overline{\text{PAR}}$ signals remain as a ZERO and ONE respectively.

(5) The ACT signal from the KW-7 enters the remote control unit on pin J1-L, and is sent out on pin J2-E to the plain text safety unit (PTS). With the KW-7 in the send plain normal mode and with keyboard data being entered continuously, the ACT signal follows the input baud signal. If keyboard data stops and allows the ACT signal to remain at a ONE level, for 10 or more seconds, the plain text safety unit (if one is used) will apply a ONE PTS signal into the remote control unit on pin J2-C and out on pin J1-e to inhibit the loop input gate circuit in the KW-7. The plain text safety unit must be reset before the keyboard operator can resume sending plain test information. The PTS signal routed through the remote control unit normally rests at a ZERO level unless keyboard activity stops for 10 or more seconds. The +6 volts DC entering the remote control unit on pin J1-a and leaving on pin J2-B is applied as a bias voltage in the plain text safety unit circuits.

(6) When the remote SEND switch is pressed a ONE level received on pin J1-Y, transmits an SE2 signal to set the toggle flip-flop in the KW-7, starting the send phasing. Release of the remote SEND switch transfers a ONE SE1 out on pin J1-E to reset the toggle flip-flop. When send mode was initiated a ZERO SELR signal from the KW-7 was received on pin J1-J (in the remote control unit) and inverted to a ONE by the lamp driver (A1-MD1) to illuminate the SEND light. See figure 4-37 which shows the schematic of the remote lamp driver. (A1-MD1).

(7) When phasing and indicator modes occur in the KW-7 a ZERO P&I L signal is sent to the remote control unit on pin J1-M, inverted by the lamp driver to a ONE which illuminates the P&I light.

(8) A break condition can be initiated by depression of the remote BREAK switch which transfers a ONE level from pin J1-B to pin J1-A and sends out a BRK ONE signal to the indicator circuit in the KW-7. This BRK signal resets the indicator counter and sets up the generation of BREAK signals which reset the KW-7. The ONE BRK signal also resets the KW-7 line output register. A BRLR ZERO signal is received in the remote control unit during break generation on pin J1-K, and is inverted by the remote lamp driver to a ONE level which illuminates the remote BREAK light. Depression of the remote BREAK RESTORE switch sends a ONE $\overline{\text{BREAK}}$ signal out on pin J1-C to the KW-7 to reset the break generating circuit and prepare for normal operation.

(9) If an alarm condition occurs in the KW-7, a ZERO ALLR signal is received in the remote control unit on pin J1-H, inverted by the remote lamp driver to a ONE which

illuminates the remote ALARM light. During the KW-7 alarm condition a ONE AUDO 2R signal is also received in the remote control unit on pin J1-N which sounds the LS1 AUDIBLE ALARM.

(10) When the KW-7 is in send normal mode with the TD step switch in the STEP position, the remote control unit will receive a ONE PCL signal, once per character, on pin J1-b to trigger the TD STEPPING RELAY K-1 coil. The -53 volts DC on pin J7-E is normally jumpered to provide operating voltage for the K-1 coil. The contacts of relay K-1 (wired through filter FL-7 to pin J7-B and directly to J7-C) impulse a stepping magnet in the transmitter-distributor at a character rate. The transmitter-distributor is connected to the remote control unit by an eight foot cable connected to J7. The R-C network across the K1 relay contacts and CR2 across the K1 relay coil provide suppression.

(11) A teletypewriter keyboard and or transmitter-distributor can be connected to the remote control unit on Loop Input-1 connector J4 and/or Loop Input-2 connector J3 of the remote control unit to provide LOIZR data input signals. These signals flow through filter FL-4 in the remote control unit and out on pins J1-U (signal) and J1-S (signal ground) through a cable to the KW-7. When only one loop input is used on the remote control unit, dummy connector PC1 is placed on the unused Loop 1 Input plug, connecting J3-C to J4-C. Loop output data from the KW-7 enters the remote control unit on lines LOON2R (Pin J1-R) and LOOP (Pin J1-P) and is routed through filter FL-5 and FL-6 to LOOP OUT 1 and 2 on connectors J5 and J6. The remote control unit loop outputs can be connected to one or two page printers or other types of teletypewriter receivers. If only one loop output is used, dummy connector PC2 is placed on the unused loop output receptacle to jumper pins J5-C to J6-C.

4406. Two-Wire Loop Adapter Detailed Theory.—This section presents the detailed theory for the two-wire loop adapter operation. The discussion includes descriptions of internal data paths and the relationship of the two-wire loop adapter to both the KW-7 and the teletypewriter equipment.

a. General.—The loop-in circuit of the KW-7 is designed for use with low-level (approximately 80 microamperes) input signals from the teletypewriter keyboard or TD. The KW-7 loop-out circuit provides either 20 or 60 milliampere output signals for the home teletypewriter printer. Because the loop-in and loop-out currents differ, four wires are required for connecting teletypewriter equipment to the loop circuits of the KW-7. Under special applications, the teletypewriter equipment is operated at a 20 or 60 milliampere signal level in a series loop (providing "home" copy on the page printer) on a two-wire system. To make this system compatible with the KW-7, a special device called the two-wire loop adapter has been constructed. Also a LOOP ALLOW/LOOP INHIBIT switch has been inserted in the KW-7 to inhibit the loop-out signal when the two-wire loop adapter is employed. The KW-7 loop output is connected by cable to jack J3 of the two-wire loop adapter, and the KW-7 loop input is connected to jack J1 of the adapter unit. The series connected teletypewriter is connected to jack J2 of the adapter unit.

b. Two-Wire Loop Adapter Schematic Analysis (fig. 4-81).—The two-wire loop adapter will be discussed first for send operation and then for receive operation.

(1) During send operation either the remote teletypewriter keyboard or TD will enter 20/60 milliampere signals on jack J2 of the two-wire loop adapter. Concurrently, the series connected remote page printer will copy the message being sent. The input teletypewriter signals will flow through the bridge rectifier composed of diodes CR2, CR3, CR4, CR5. In the absence of teletypewriter signals, a steady current of 20 or 60 milliamperes keeps relay K1 energized and also flows through the current path on pins 7 and 6 of electronic relay K2. The 20 or 60 milliampere current will be set by LOOP

switch S1 during equipment installation, depending upon the signal current rating of the teletypewriter equipment used. As the teletypewriter signals pass through the bridge rectifier and trigger relay K1 at a baud rate, the K1 contacts connect 80 miro-ampere teletypewriter signals at jack J1. These low level signals are routed from the loop adapter unit to the KW-7 loop input. The LOOP ALLOW/LOOP INHIBIT switch on the KW-7 will be set to the LOOP INHIBIT position to prevent occurrance of teletypewriter signals on the KW-7 loop output, which would other-wise be routed back to the two-wire loop adapter on jack J3 and cause interference.

(2) During receive operation, the KW-7 will receive 7.0 baud signals on its LINE INPUT, and produce 20/60 milliampere signals on the LOOP OUTPUT which are routed to jack J3 of the two-wire loop adapter. These high level signals trigger electronic relay K2 which in turn produces 20/60 milliampere signals in the K2 relay current path at pins K2-6 and 7. These 20/60 milliampere signals pass through the bridge rectifier circuit and out on jack J2 to print the received message on the page printer. Although relay K1 is also triggered during receive mode, the effect of the 80 microampere signals produced is not felt at the loop output since, as was previously indicated, the LOOP ALLOW/LOOP INHIBIT switch will be set in the LOOP INHIBIT position while the two-wire loop adapter is being utilized.

4407. Functional Remote Control Unit.—The following paragraphs contain a discussion of the functional remote control unit detailed theory. The function of all switches, indicators and other internal components is described as well as the control signals which are received or generated in the functional remote control unit.

a. General.—The functional remote control unit can be connected to the KW-7 by a cable with a maximum length of 500 feet to provide remote control of the KW-7. In addition the functional remote control unit receives control signals from the KW-7. These control signals in turn are sent to a remote transmitter-distributor.

b. Functional Remote Control Unit Schematic Analysis (fig. 4-82).—When the functional remote control unit is connected into the system the KW-7 PCR switch is placed in the REMOTE position. In this position the KW-7 PCR switch provides (via a remote cable) a remote ground on pins J1-D and J1-g −6 volts DC on pins J1-V and J1-f, and −53 volts DC on J1-c in the functional remote control unit. The presence of ground and −6 volts illuminates the READY light, indicating that the functional remote control unit is operational.

(1) With the KW-7 PCR switch in the REMOTE position, the KW-7 SEND switch is deactivated and the SEND switch on the functional remote control unit now has control. Depression of the remote SEND switch places a ONE on the SE2 line (pin J1-Y) for setting the toggle flip-flop in the KW-7 to initiate send phasing. Upon release of the remote SEND switch a ONE is placed on the SE1 line (pin J1-E) of the functional remote control unit to reset the toggle flip-flop in the KW-7. When the KW-7 goes into send mode a ZERO SELR signal is received by the functional remote control unit on pin J1-J. This ZERO is inverted by a remote lamp driver (A1-MD1) to a ONE signal which illuminates the remote SEND lamp. See figure 4-37 for the schematic of the remote lamp driver.

(2) When the KW-7 is in phasing and indicator mode a ZERO P&I L signal isr eceived on pin J1-M. This ZERO signal is inverted by the remote lamp driver (A1-MD1) to provide a ground (ONE) level which illuminates the remote P&I lamp in the functional remote control unit.

(3) If an alarm condition occurs in the KW-7, a ONE AUDO2R signal is received in the functional remote control unit on pin J1-N which causes the LS1 AUDIBLE ALARM to sound. The KW-7 alarm condition also causes the functional remote control unit

to receive a ZERO ALLR signal on pin J1–H. This ZERO signal is inverted by a remote lamp driver (A1–MD1) to a ONE signal which illuminates the remote ALARM light.

(4) Providing the KW–7 is in send normal mode and the CONTINUOUS switch is in the STEP position, the functional remote control unit will receive a ONE PCL signal, once per character on pin J1–b to impulse the TD STEPPING RELAY (K1) coil. The −53 volts DC on pin J2–E will be jumpered to pin J2–D to apply −53 volts DC to pin 1 of the K1 relay coil. The contacts of relay K1, which close repetitively, are wired to pins J2B and J2C, and through an external cable impulse the stepping magnet in the transmitter-distributor at a character rate. Resistor R1 and condenser C1 in series provide arc suppression to protect the K1 relay contacts. System grounds are connected to the functional remote control unit on pins J1–j and J2–A. The FL–1 filter in the K1 relay contact circuit is provided to eliminate noise.

(5) The major difference between the remote control unit and the functional remote control unit are:

(a) The functional remote control can operate only in the cipher mode, whereas the remote control may operate in the cipher, plain synchronous or plain asynchronous modes.

(b) The functional remote control handles only control signals, whereas the remote control handles both control signals and data signals.

4408. Power Supply (fig. 4–83).—The power supply furnishes all DC voltages required within the KW–7. These voltages are regulated to remain within ±1% of their nominal values under widely varying input voltage and output load conditions. The supply is designed to operate from 115 or 230 VAC, 45 to 440 cps, or from a 21 to 31 VDC source. Output voltages are summarized in the following table.

Output Voltage	Maximum Load
+6 V	280 ma
−6 V	2.0 amps
−18 V	37 ma
−24 V	275 ma
−53 V	175 ma

Major sections of the power supply are the input section, the +6 V source the −6 V source, the −24 V source, the −18 V source and the −53 V source.

a. Input Section.—The input section permits the power supply to operate from any of three power sources: 115 VAC, 45 to 440 cps; 230 VAC, 45 to 440 cps; or 21 to 31 VDC. The input section is made up of a power transformer and a DC-to-AC converter.

(1) *Power transformer.*—For 115 VAC operation, primaries 1 and 2 of power transformer T1 are connected in parallel; for 230 VAC operation, the same windings are connected in series. These connections are automatically made by setting the 115/230 V switch, on the filter assembly, to the desired voltage.

(2) *The DC-to-AC converter.*—The DC-to-AC converter, comprising Q11, Q12, primary 3 of T1, and saturating transformer T2. It is used when the KW–7 is to be operated from a 21-to-31 VDC source. The DC-to-AC converter is a Jensen oscillator which develops a 400 to 500 cps 40 V peak-to-peak square wave across primary 3 of T1. The following discussion covers the initial start-up and one cycle of oscillation. Q11

and Q12 act in a push-pull arrangement, with the transistors alternately "on" (drawing heavy current) and "off" (drawing little current). When DC input power is first turned on, a negative voltage is applied via R39 to the center tap of T2 and to capacitor C19. The negative voltage back-biases diode CR25, which behaves as an open circuit, allowing capacitor C19 to begin charging. As C19 charges, the center tap of T2 goes negative, applying a forward bias via T2, R36 and R38 to the bases of Q11 and Q12. Since Q11 and Q12 can not have identical characteristics, one will turn on faster than the other. Assume that Q11 turns on faster. The increasing current through Q11 induces a voltage in primary 3 of T1, which in turn induces a voltage in secondary 1. Secondary 1 produces a current in the primary of T2. This current is of such polarity that the induced secondary voltage on terminal 5 of T2 is negative, further increasing the base current to Q11 and reinforcing the original turn-on current supplied through R39. The above cycle now builds up in a regenerative fashion until T2 saturates, causing the Q11 base current to level off. The collector current of Q11 momentarily stabilizes, the flux in the core of T1 becomes a constant and primary 3 of T1 no longer induces a voltage in secondary 1 of T1. With current no longer available in the primary of T2, the flux in T2 collapses, causing the base voltage of Q11 to become positive with respect to the emitter and the base voltage of Q12 to become negative with respect to the emitter. The collector current in Q11 decreases and the collector current in Q12 increases until T2 again saturates. As soon as T2 saturates, the Q12 collector current momentarily stabilizes, the current in the primary of T2 begins to decrease, and the entire sequence reverses. This alternate conduction, first of one transistor and then the other, continues as long as DC input power is available. After the initial start-up, diode CR25 becomes forward biased by the base currents of Q11 and Q12, thereby furnishing a low-impedance DC path from terminal 4 of T2 to the common emitter circuit. Resistor R37 limits the current through CR25 to a safe value. Diode CR35 protects the converter in case the DC source is accidentally connected incorrectly by blowing the fuse in the source output line. CR26 and CR27 are Zener diodes which protect Q11 and Q12 by limiting switching transients to 68 volts. Further transient protection is provided by the switching buffer network R40 and C20. Relay K1 insures that the DC/AC converter is deactivated when the power supply is operated from an AC source. The coil of the relay is connected across the DC input terminals. With no DC input voltage the relay is deenergized and the converter circuit is isolated from T1.

b. +6-V Source.—The +6-V source operates from secondaries 2 and 3 of T1. Secondary 2, CR1, CR2, and C1 provide a positive bias via R3 to the base of Q4 and emitter of Q2. Diodes CR3 and CR4 are connected across secondary 3 in a full-wave rectifier arrangement, furnishing approximately 10 volts across filter capacitors C2 and C3. Series regulator Q4 is connected between the rectifier output and the load. Load voltage is maintained at a constant +6 volts by automatically varying the collector-to-emitter resistance of Q4 in inverse proportion to load requirements: that is, if the load increases, the resistance of Q4 decreases, and if the load decreases the resistance of Q4 increases. The resistance of Q4 is varied in the following manner: Resistor R5 maintains a bias current for Zener diode CR5, and CR5 in turn furnishes a constant reference voltage of +4.3 V to the base of amplifier Q3. The emitter of Q3 is connected to a voltage divider (R6, R7, R8, R10) which is in parallel with the load. Assume that the load voltage begins to drop because of an increase in load current. This drop in load voltage is applied through the voltage divider to the emitter of Q3, making the emitter less positive with respect to the base. The Q3 collector current increases, causing the collector voltage of Q3 and the base voltage of emitter follower Q2 to become less positive. Q2 draws more base current and supplies more base current to Q4. Q4 conducts more heavily and its collector-to-emitter resistance drops, pulling the output voltage back up to 6 volts. The output voltage is set to exactly

6 volts by adjusting variable resistor R7, which sets the quiescent operating point of Q3. Sensistor RT1 is a positive-temperature-coefficient resistor which compensates for changes in transistor characteristics caused by temperature variations within the KW-7. R1 and C4 comprise a stabilizing network which reduces parasitic oscillations.

c. *−6 V Source.*—The −6 V source operates from secondary 5 of T1. CR8, CR9, CR10 and CR11 are connected in a full-wave bridge arrangement which furnishes approximately 10 VDC across filter capacitor C7. Series regulator Q1 is connected between ground and the positive output of the rectifier. The −6 V output is taken directly from the negative output of the rectifier. Operation of the −6 V regulator is the same as operation of the +6 V regulator, the only important difference being an extra emitter follower between amplifier Q7 and series regulator Q1. This emitter follower is necessary because the greater load current, 2 amperes maximum, requires that more base current be supplied to Q1.

d. *−24 V Source.*—The −24 V source operates from secondary 7 of T1. Diodes CR15, CR16, CR17, and CR18 are connected in a full-wave bridge arrangement which furnishes approximately 40 VDC across filter capacitors C12, C13, and C14. Operation of the −24 V regulator is the same as that of the +6 V regulator, the only significant difference being the addition of an extra resistor (R33) in the voltage divider network. The resistance of R33 is such that the voltage drop across the rest of the divider is the same as the drop across the +6 V regulator, thus allowing the same basic regulator circuit to be used in both the +6 V regulator and the −24 V regulator. C16 is a stablizing capacitor which prevents the voltage at the junction of R32 and R33 from changing during heavy load transients.

e. *−18 V Source.*—The −18 V source (CR22, CR23, CR21, CR20, R34, and R35) operates from the −24 V source. Terminal 1 of R34 is held at −15.9 volts by the sum of the drops across Zener diodes CR21 and CR23. Terminal 3 of R34 is held at −18.8 volts by the sum of the drops across CR21 and CR22. R34 is adjusted so that the output voltage (terminal 2) is exactly −18 volts. The voltage drop across diode CR20 decreases with increasing temperature, balancing out changes in the characteristics of CR21, CR22, and CR23 caused by temperature variations.

f. *−53 V Source.*—The −53 V source operates from secondary 9 of T1. Diodes CR30, CR31, CR32, and CR33 are connected in a full-wave bridge arrangement which furnishes approximately 70 volts across filter capacitor C22. Operation of the −53 V regulator is the same as that of the −6 V regulator, the only significant difference being the addition of two resistors, R21 and R31, to the voltage divider. These resistors are chosen so that the drop across the remainder of the voltage divider is 6 volts, thus allowing the same basic regulator circuit to be used both for the −6 V regulator and the −53 V regulator. Capacitors C25 and C26 stabilize the voltage at the junction of R9 and R21 during heavy load transients.

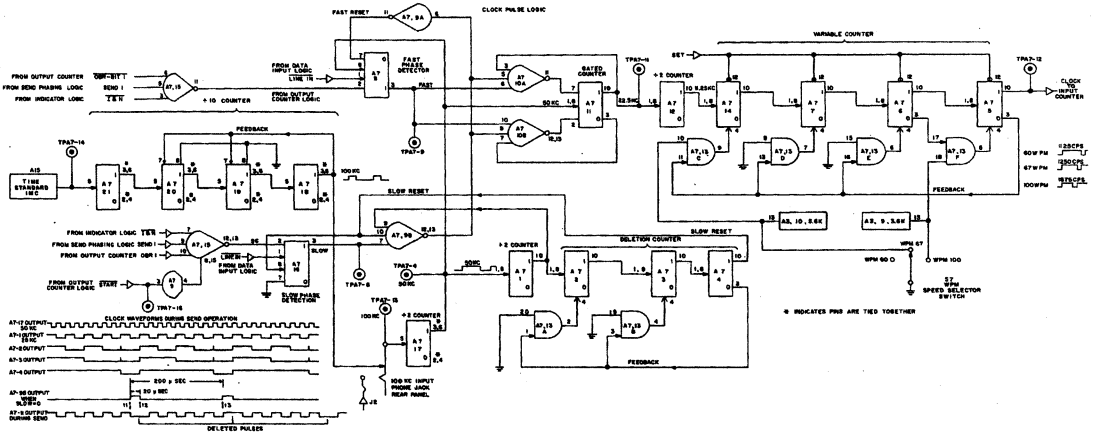


Figure 4-61.—Clock Pulse Generation, Logic Diagram.

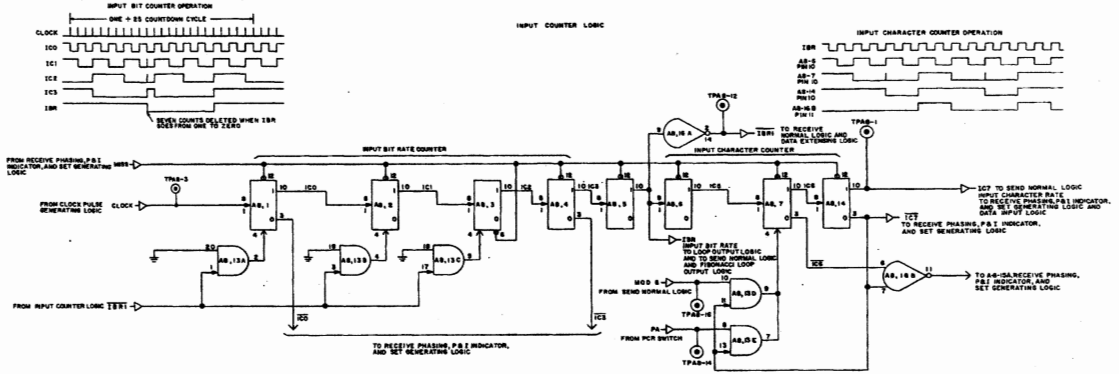


Figure 4-83.—Input Counter, Logic Diagram.

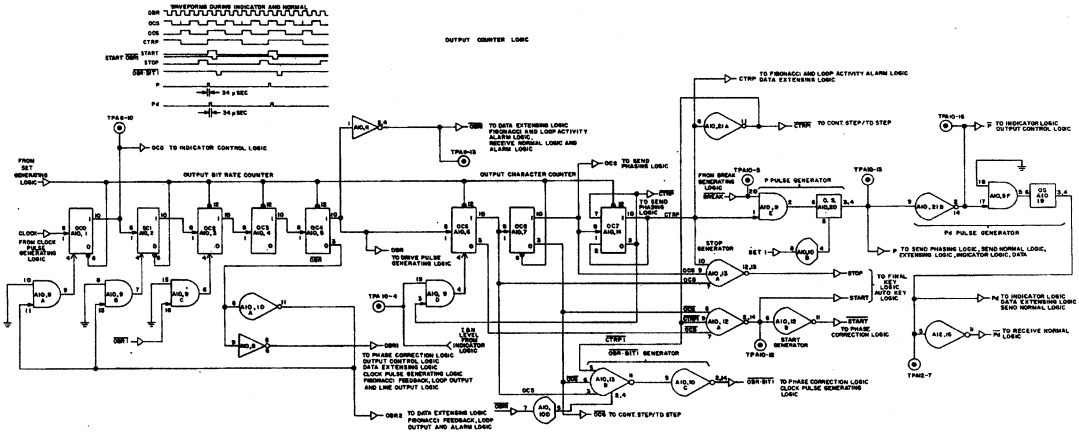


Figure 4-53.—Output Counter, Logic Diagram.

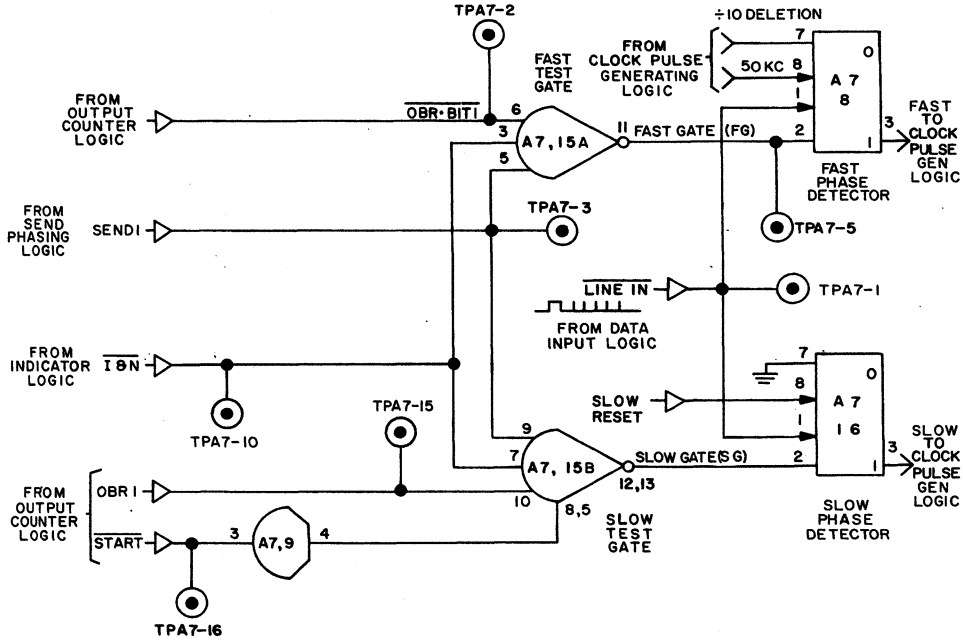


Figure 4-54.—Phase Correction, Logic Diagram

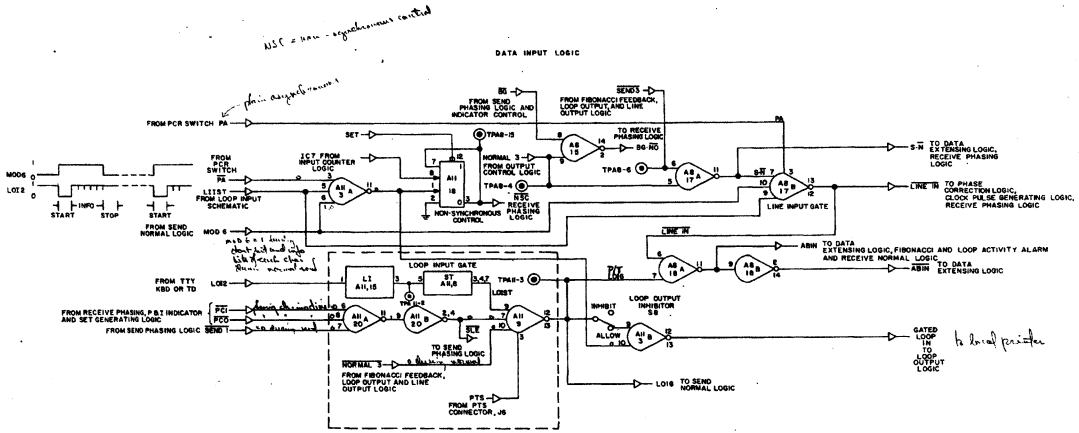


Figure 4-55.—Data Input, Logic Diagram.

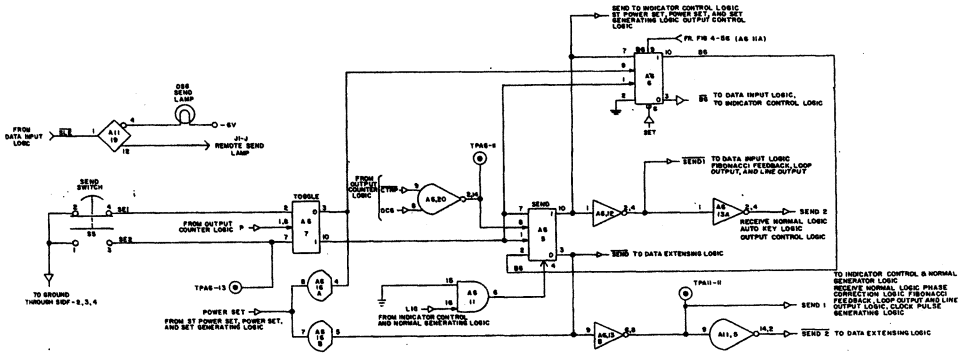


Figure 4-56.—Send Phasing, Logic Diagram.

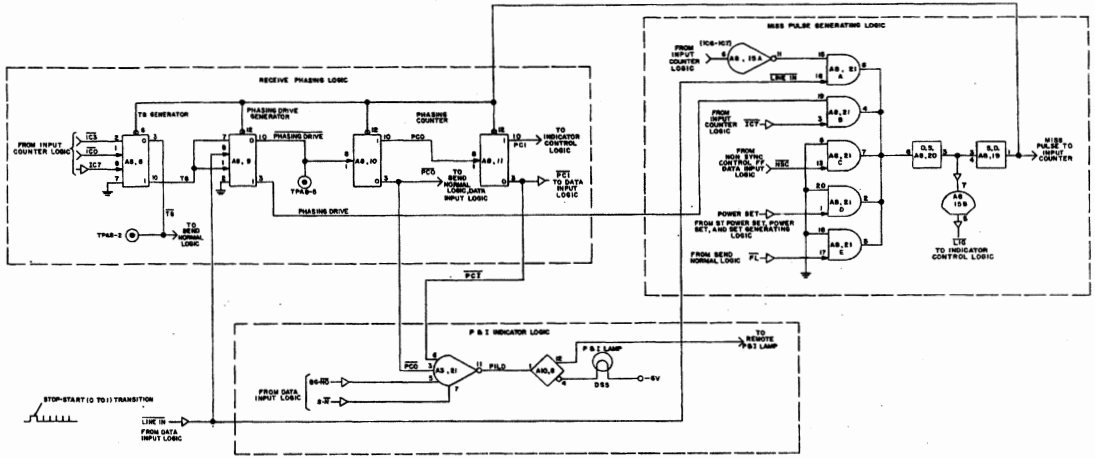


Figure 4-57.—Receive Phasing, P&I Indicator and Set Generating Logic Diagram.

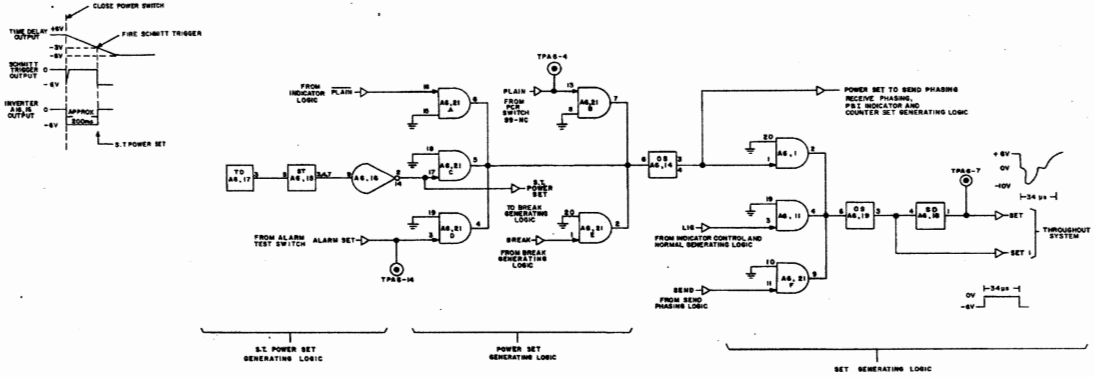
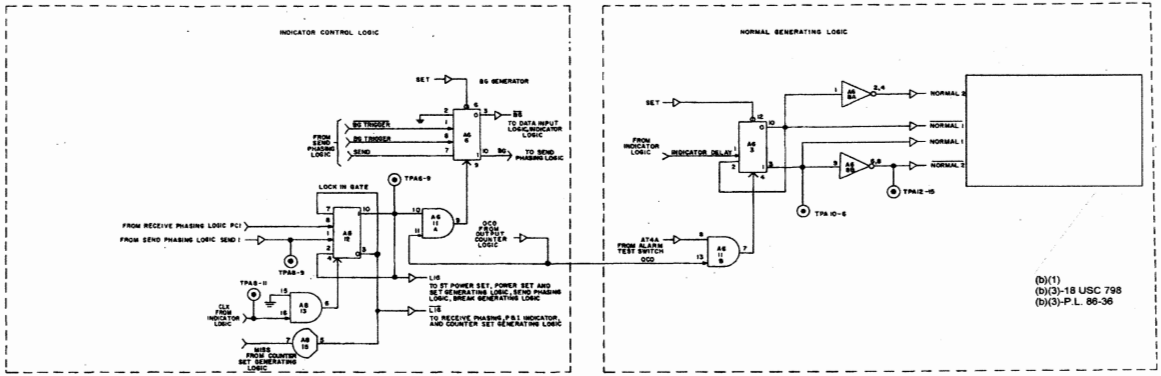


Figure 4-56.—ST Power Set, Power Set and Set Generating Logic Diagram.



(b)(1)
(b)(3)-18 USC 798
(b)(3)-P.L. 86-36

Figure 4-59.—Indicator Control Logic Diagram.

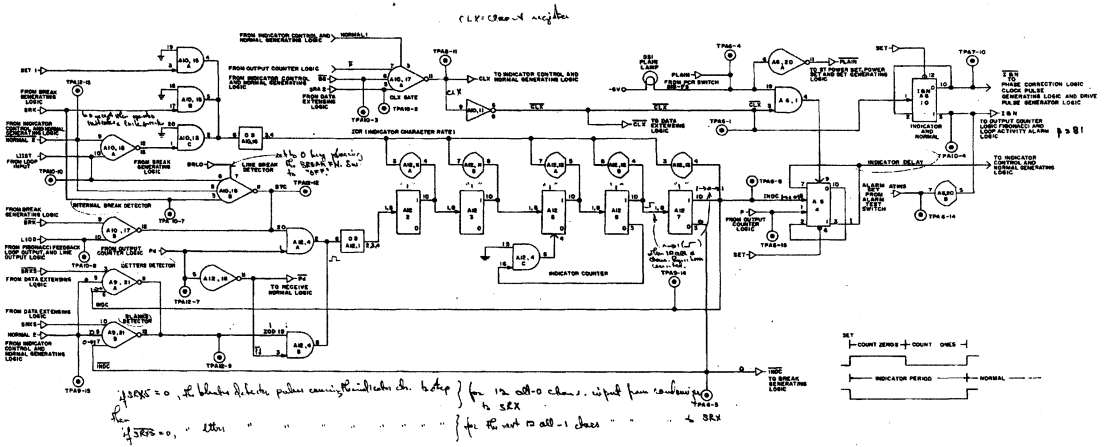


Figure 4-60.—Indicator Logic Diagram.

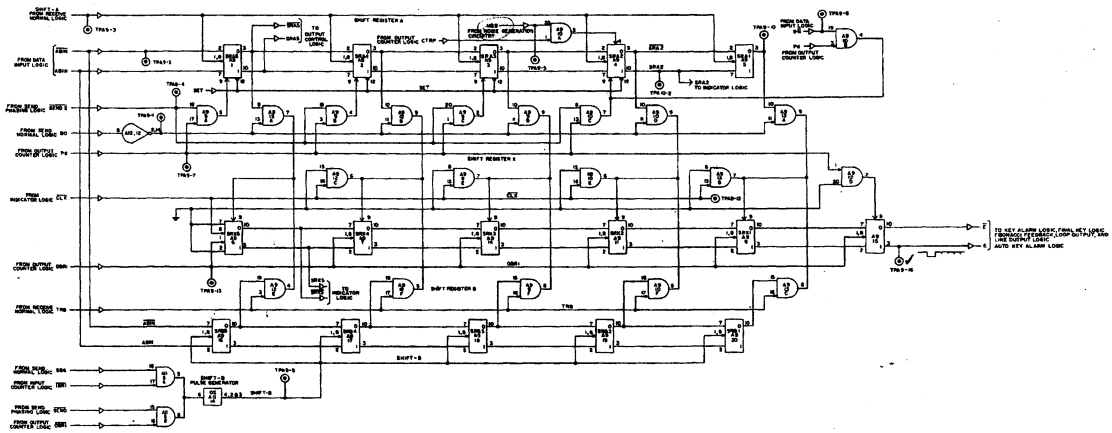


Figure 4-61.—Data Extensing Logic Diagram.

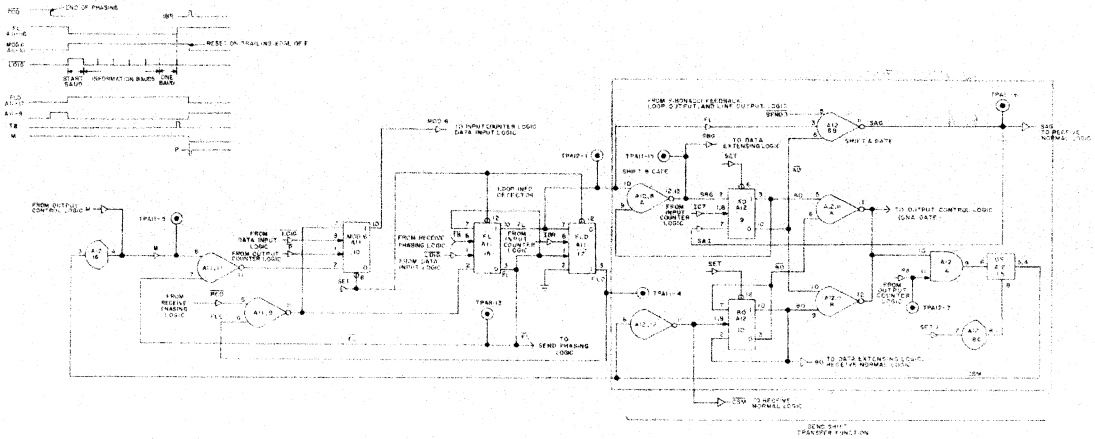


Figure 4 62. Send Normal Logic Diagram.

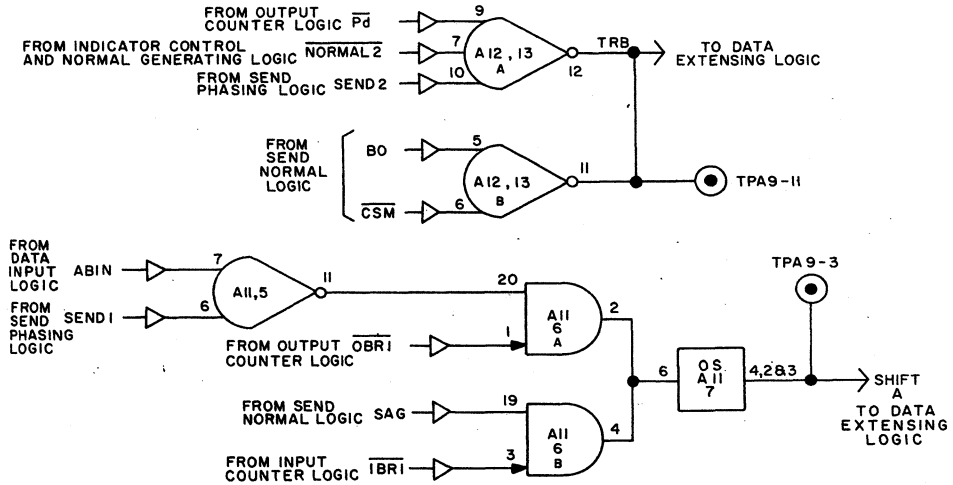


Figure 4-63.—Receive Normal Logic Diagram.

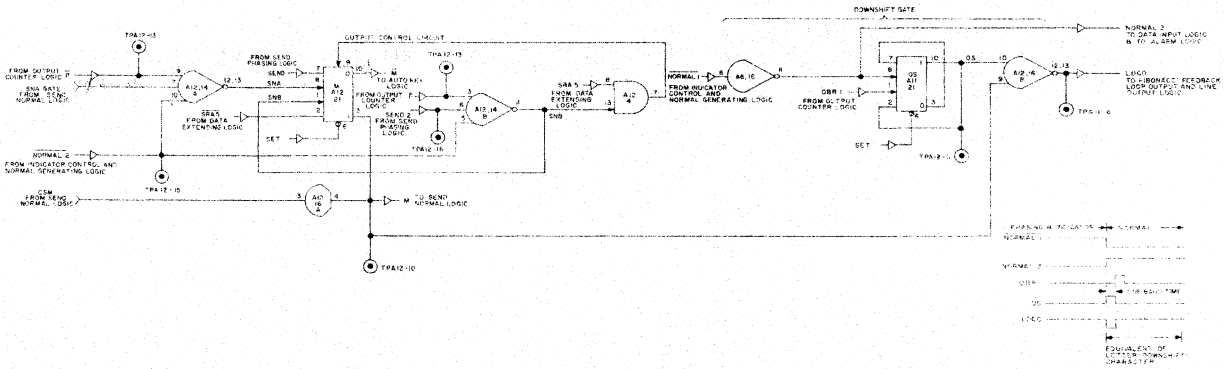


Figure 1-61. Output Control Logic Diagram.

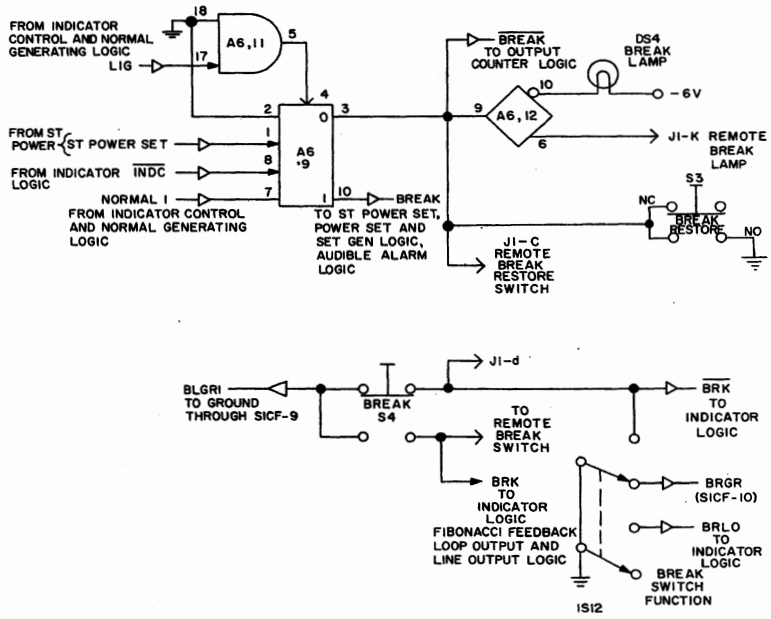


Figure 4-65.—Break Generating Logic Diagram.

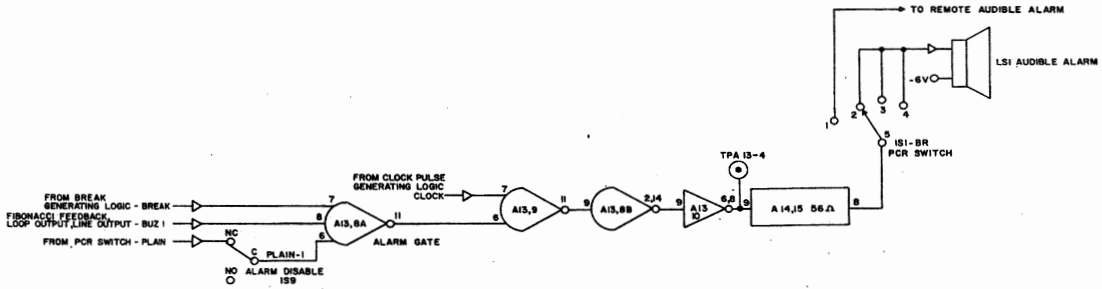


Figure 4-46.—Audible Alarm Logic Diagram.

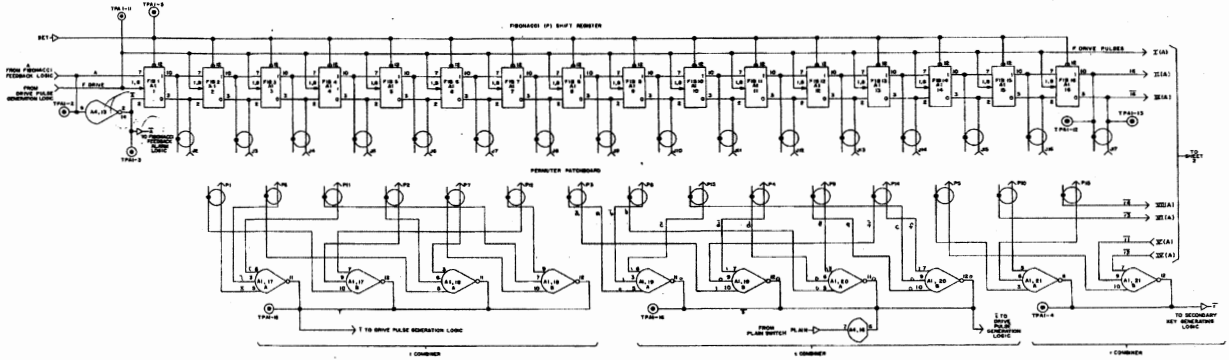


Figure 4-47.—Primary Key Generating Logic Diagram (Sheet 1).

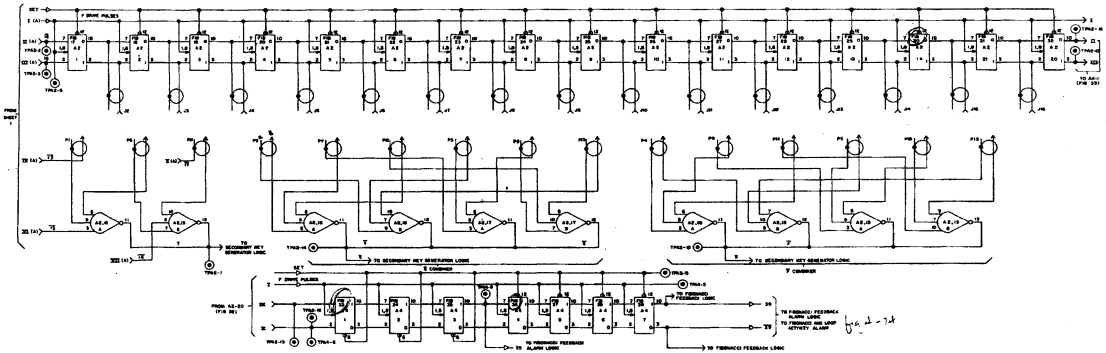


Figure 4-57.—Primary Key Generating Logic Diagram (Sheet 2).

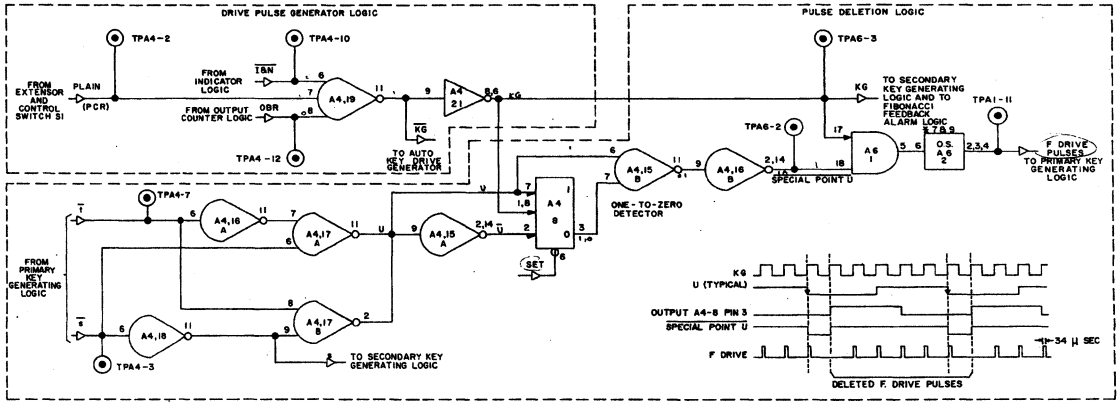


Figure 4-68.—Drive Pulse Generating and Pulse Deletion Logic Diagram.

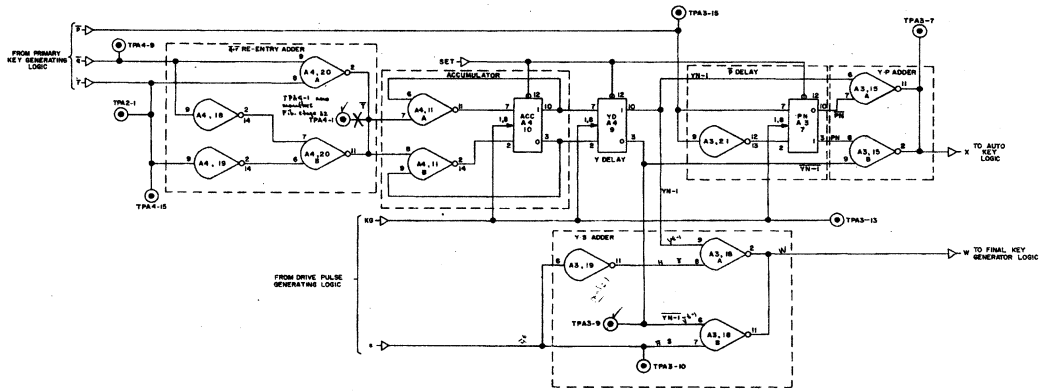


Figure 4-68.—Secondary Key Generator Logic Diagram.

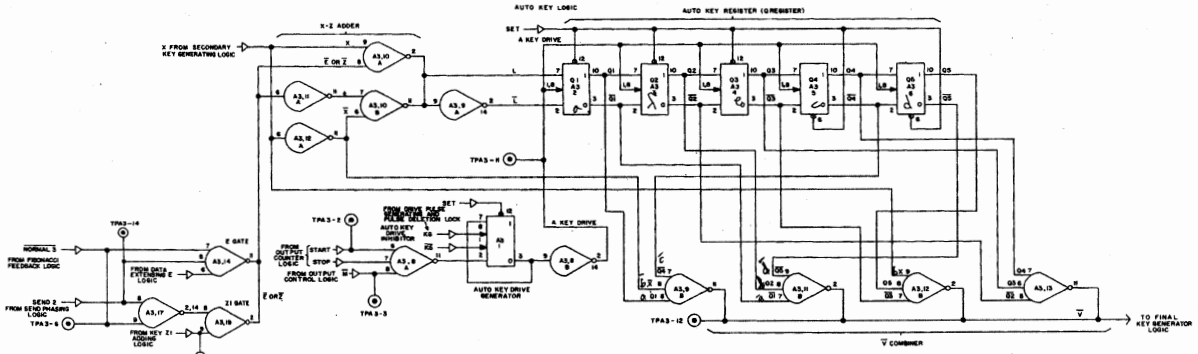


Figure 4-70.—Auto Key Logic Diagram.

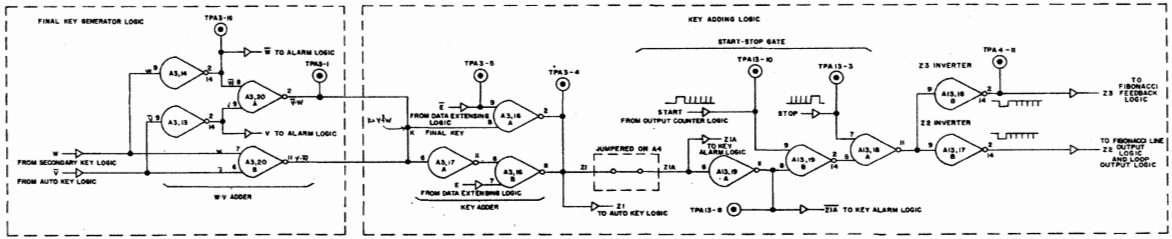


Figure 4-71.—Final Key Generating and Key Adding Logic Diagram.

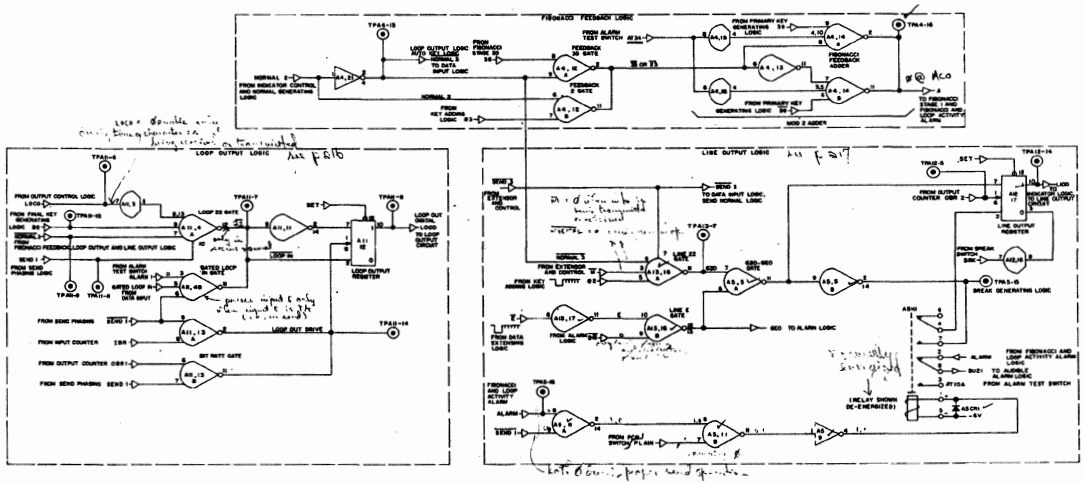


Figure 4-72.—Fibonacci Feedback Loop Output and Line Output Logic Diagram.

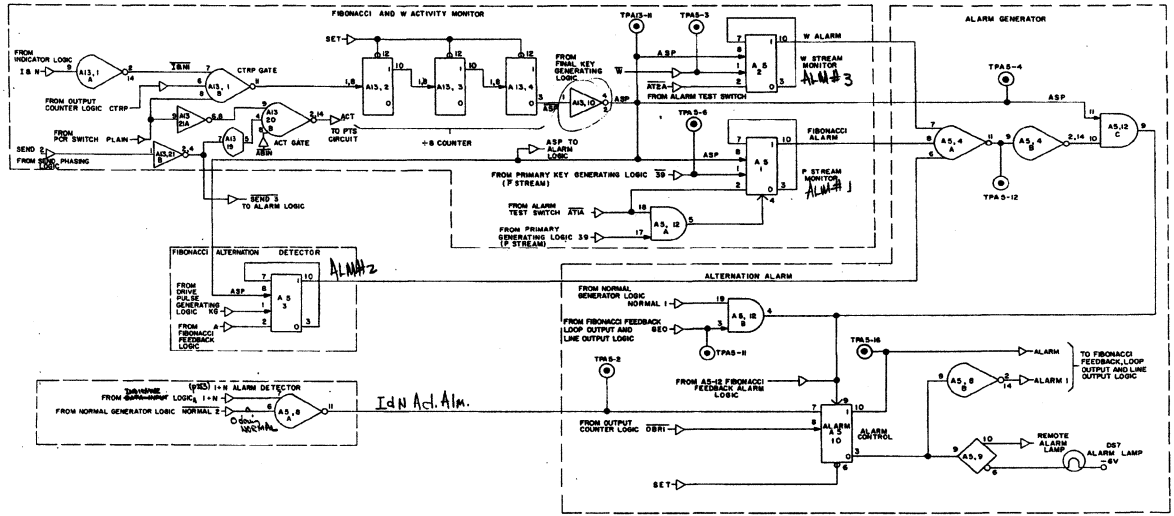


Figure 4-73.—Fibonacci, I&N Failure and PTS Alarm Logic Diagram.

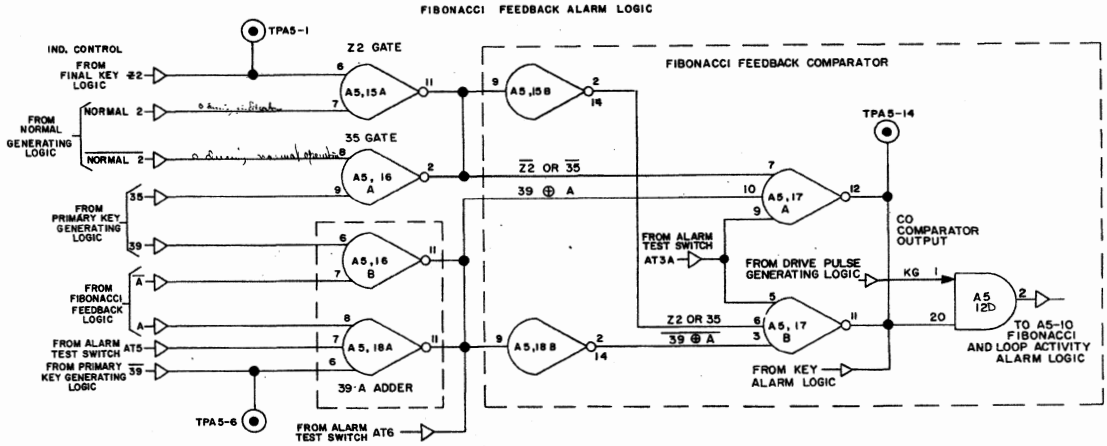


Figure 4-74.—Fibonacci Feedback Alarm Logic Diagram.

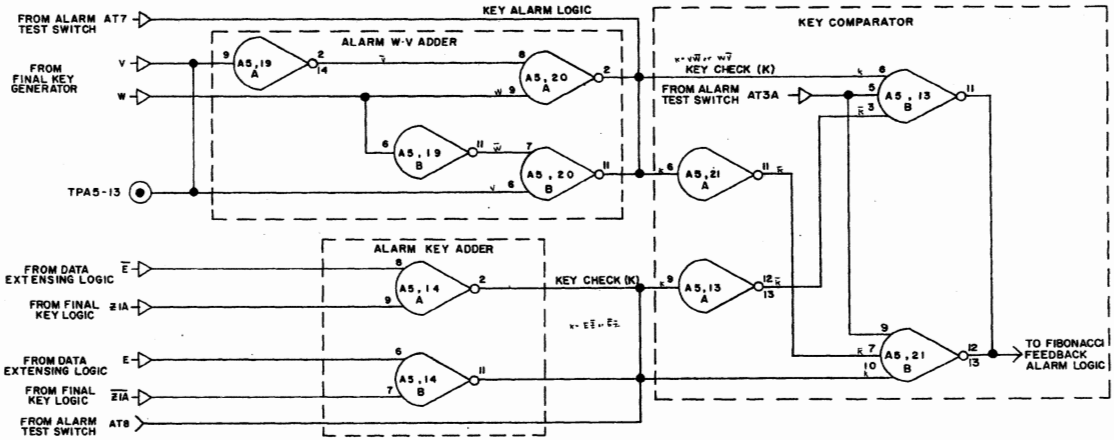


Figure 4-75.—Key Alarm Logic Diagram.

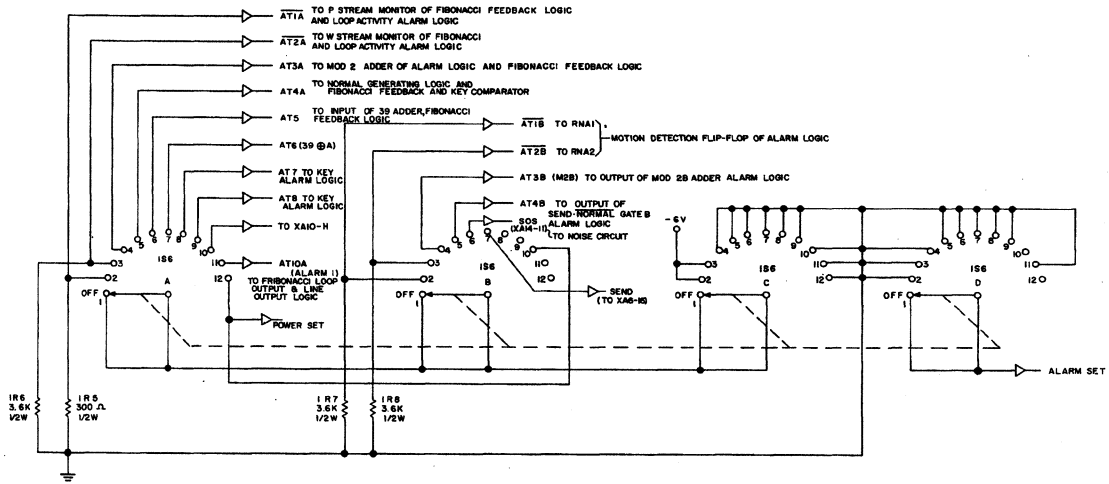


Figure 4-76.—Alarm Test Switch, Schematic Diagram.

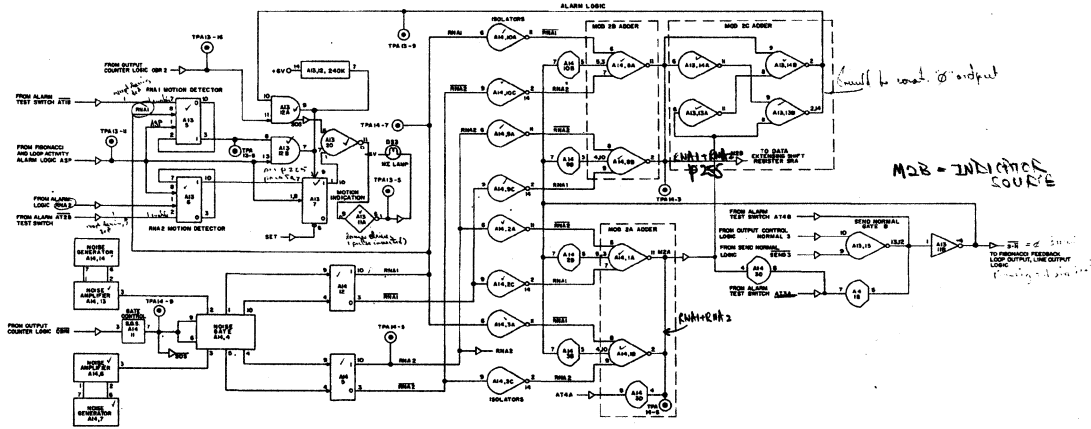


Figure 4-77.—Randomizer and Alarm Logic Diagram.

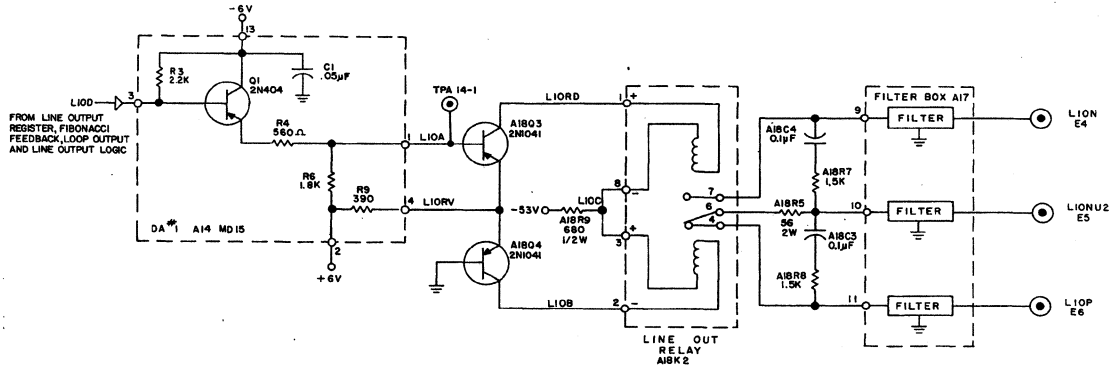


Figure 4-78.—Line Output Circuit, Schematic Diagram.

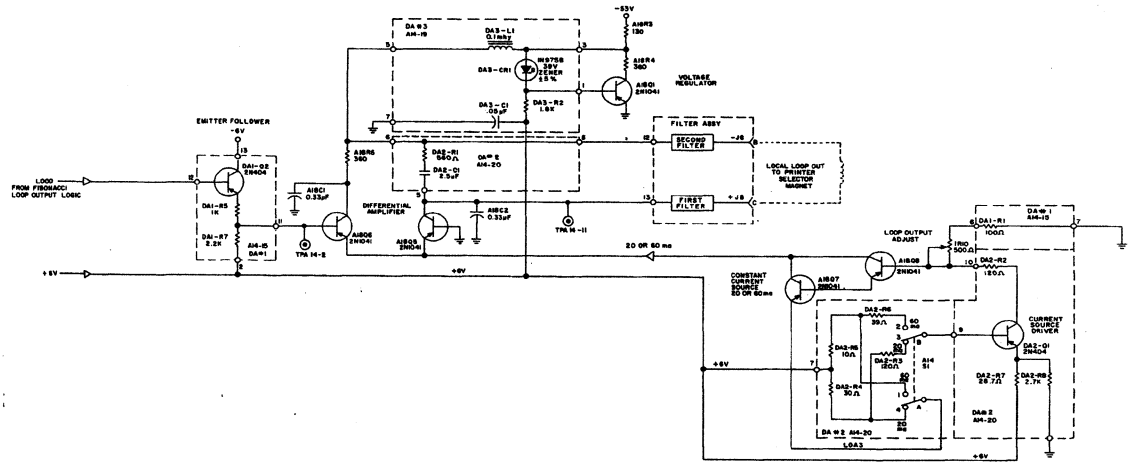


Figure 4-79.—Loop Output Circuit, Schematic Diagram.

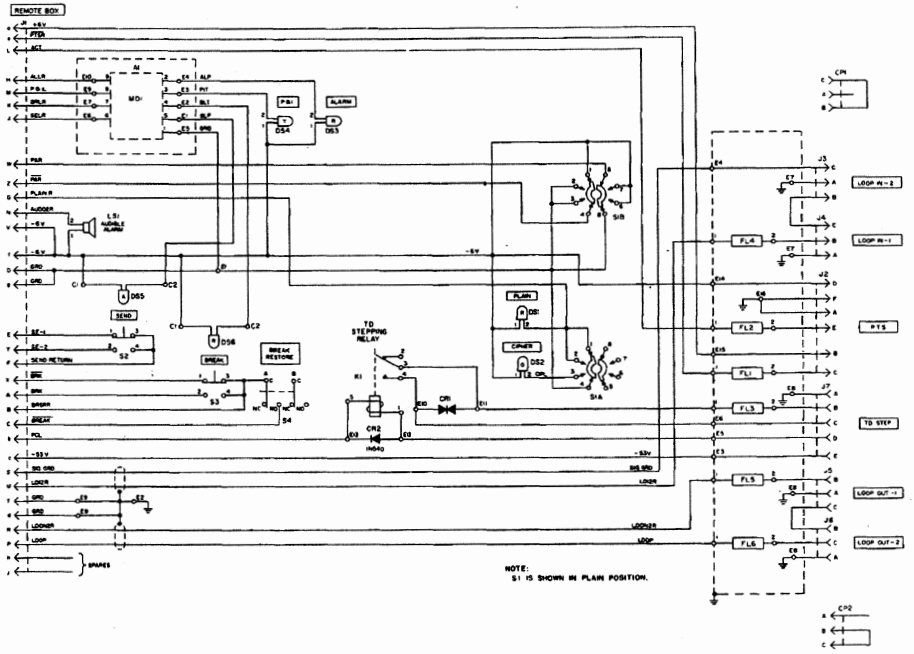
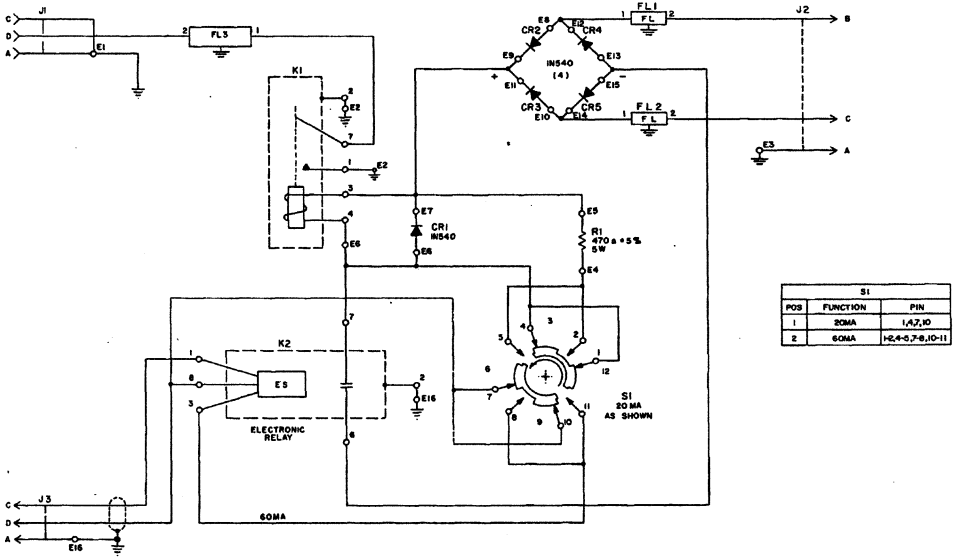


Figure 4-80.—Remote Control Unit, Schematic Diagram.



S1		
POS	FUNCTION	PIN
1	20MA	1,4,7,10
2	60MA	1-2,4-5,7-8,10-11

Figure 4-81.—Two-Wire Loop Adapter Unit, Schematic Diagram.

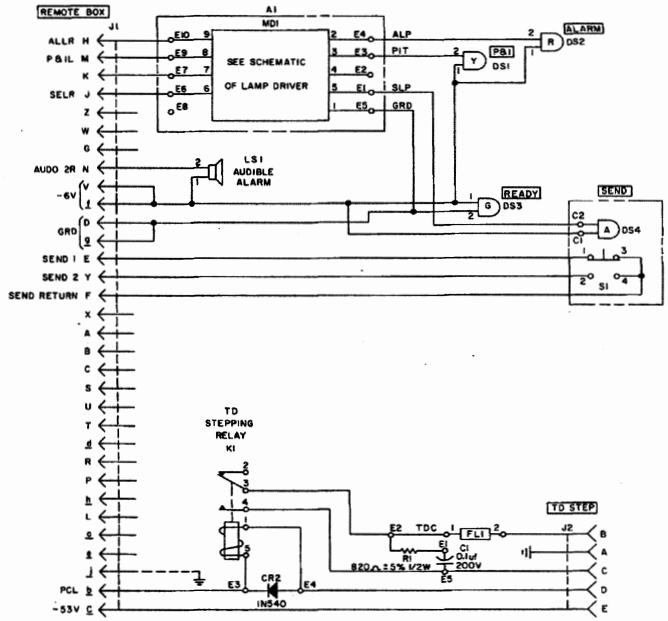


Figure 4-82.—Functional Remote Control Unit, Schematic Diagram.

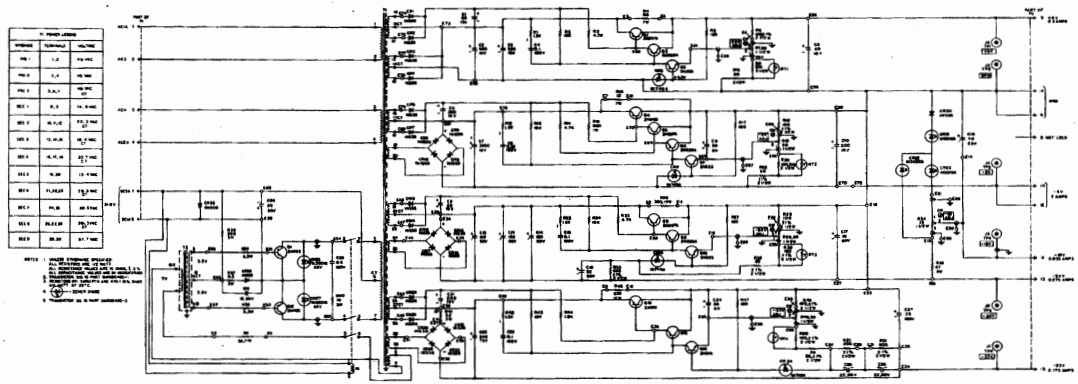


Figure 4-52.—Power Supply, Schematic Diagram.

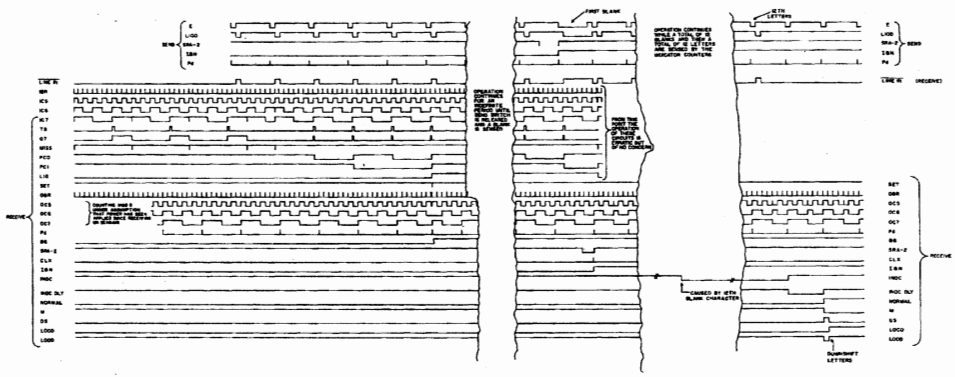


Figure 4-84.—Receive Phasing and Synchronization during Phasing and Indicator.

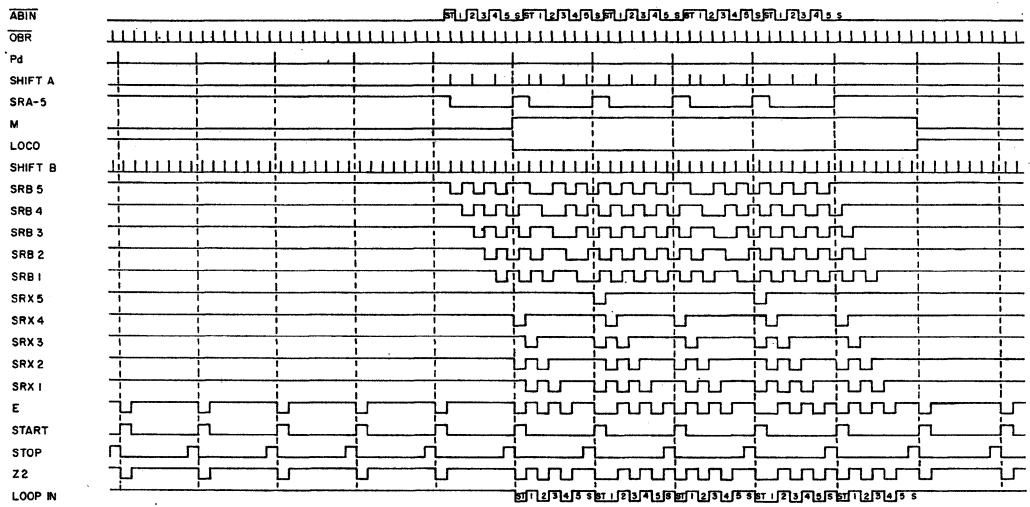


Figure 4-85.—Extensor and Control Operation in Receive Plain.

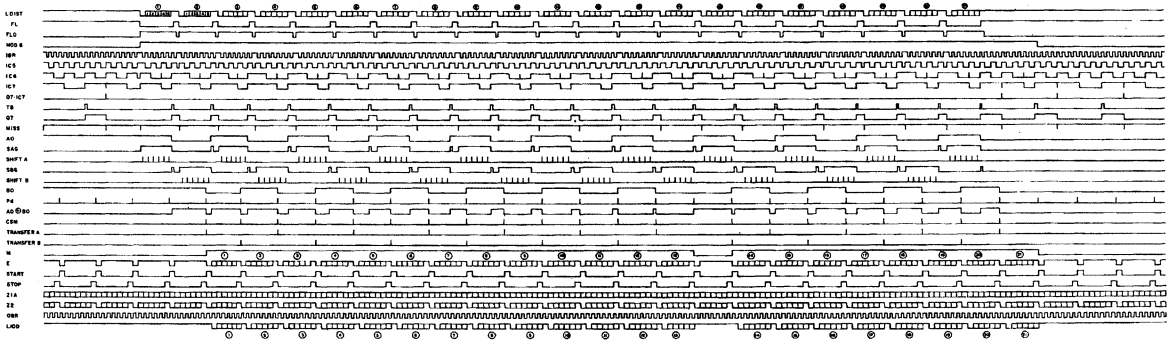


Figure 4-36.—Extensor and Control Operation in Send Cipher.

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