TECHNICAL MANUAL

R-2307/U

RECEIVER, DUAL, VLF-HF

CUBIC COMMUNICATIONS
A member of the Cubic Corporation family of companies
305 Airport Rd., Oceanside, CA 92054

TECHNICAL MANUAL

R-2307/U

RECEIVER, DUAL, VLF-HF

5 kHz to 30 MHz

CONTRACT N60921-84-C-A152

NAVAL SURFACE WEAPONS CENTER

ISSUE 2.3

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ISSUE 2.3 INSTRUCTION SHEET

Issue 2.3 is an update package to issue 2.1 and/or issue 2.2 of the R-2307/U technical manual. Issue 2.2 changes are also included in issue 2.3. Refer to page i in this package, and replace or insert the changed pages as indicated. Discard this instruction sheet when the change is done.

LIST OF CHANGES FOR ISSUE 2.3

The following pages contain changes made to this document since the publication of issue 2.1 and 2.2. Issue 2.2 changes are also included in Issue 2.3. Only the pages listed and the corresponding page on the opposite side of the sheet have been changed. Issue 2.3 pages are identified in the title block of each changed page.

Title/blank (replace)

i/ii (replace)

iii/iv (replace)

2-3/4 (replace)

2-7/8 (replace)

2-9/10 (replace)

3-2/blank (replace)

3-7/8 (replace)

4-3/4 (replace)

4-7/8 (replace)

4-9/10 (replace)

4-11/12 (replace)

4-13/14 (replace)

4-15/16 (insert)

4-17/18 (insert)

4-19/20 (insert)

7-3/blank (replace)

7-4/blank (replace)

7-5/blank (replace)

7.4-1/2 (replace)

7.4-3/blank (replace)

7.5-3/4 (replace with 7.5-3/blank)

7.5-4/blank (insert)

7.19-1/2 (insert)

7.19-3/blank (insert)

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1.0 INTRODUCTION

The R-2307/U is a high performance multi-mode receiver tuning the frequency range from 5 kHz to 30 MHz and having usable performance from 50 KHz to 30 MHz. The intended use of this receiver is in manually operated or remote controlled arrays of two or more receivers in groups of two receivers. Each receiver in the chassis may be assigned a unique address and can be operated in groups of up to 14 receivers via an IEEE-488 remote control bus or in groups of up to 32 receivers via a special purpose parallel bus. A complete set of front panel controls and displays is also provided.

The type of remote control bus, selection of bandpass filter bandwidths, and external reference frequency (10 or 1 MHz) are option items selected at the time of order of this receiver. These items may be changed in the field if required. Contact the factory or procuring agency for details.

Receivers are comprised of individually shielded module assemblies. Modules for two complete receivers are mounted in a single 19 inch by 5.25 inch rack mount chassis having common control bus, audio, and AC power connectors. Each receiver has individual RF input and IF output connections and individual power supplies with individual power switches. One external frequency standard input connector and one frequency standard output connector with a single internal/external frequency standard selector switch is provided for each two-receiver assembly.

Manual operation of this receiver is by means of a 20 button keypad used for selection of frequency, mode, BFO and IF shift, manual gain, and other parameters. A manual adjustment knob is also provided for control of many of the above parameters. The display for this receiver includes frequency, mode, bandwidth, and AGC time constant as well as (when selected), BFO and IF shift, manual gain, threshold for squelch or scan stop, and other parameters. Each unit also contains a light bar type meter for indication of signal strength, audio signal level, or relative frequency of the input signal.

Operation of this receiver may also be entirely under the control of the computer system operator via the remote control bus. Choice of tuned frequency, mode, BFO offset (when the CW mode is selected), AGC time constant, and other parameters is all performed through the system console. Consult the computer system operator's manual (if available) for further information.

By proper selection of mode, bandwidth, BFO offset, gain control, AGC time constants, and other parameters, the operator is able to detect and demodulate a wide variety of signals include amplitude modulated, on/off keyed, and single sideband signals including full carrier, reduced carrier, and suppressed carrier signals. Frequency shift keyed signals can be demodulated as single sideband suppressed carrier signals or as true FM signals. All detector outputs are available as fixed level audio signals on a 600 ohm balanced line and the FM detector output is also available as a DC coupled signal on a single ended line. Headphone jacks are provided on both front and rear panels -- the signal level on these headphone jacks is controlled by a front panel volume control.

First IF output signals at 40.455 MHz and second IF output signals at 455 KHz are brought out for display or analysis by other equipment.

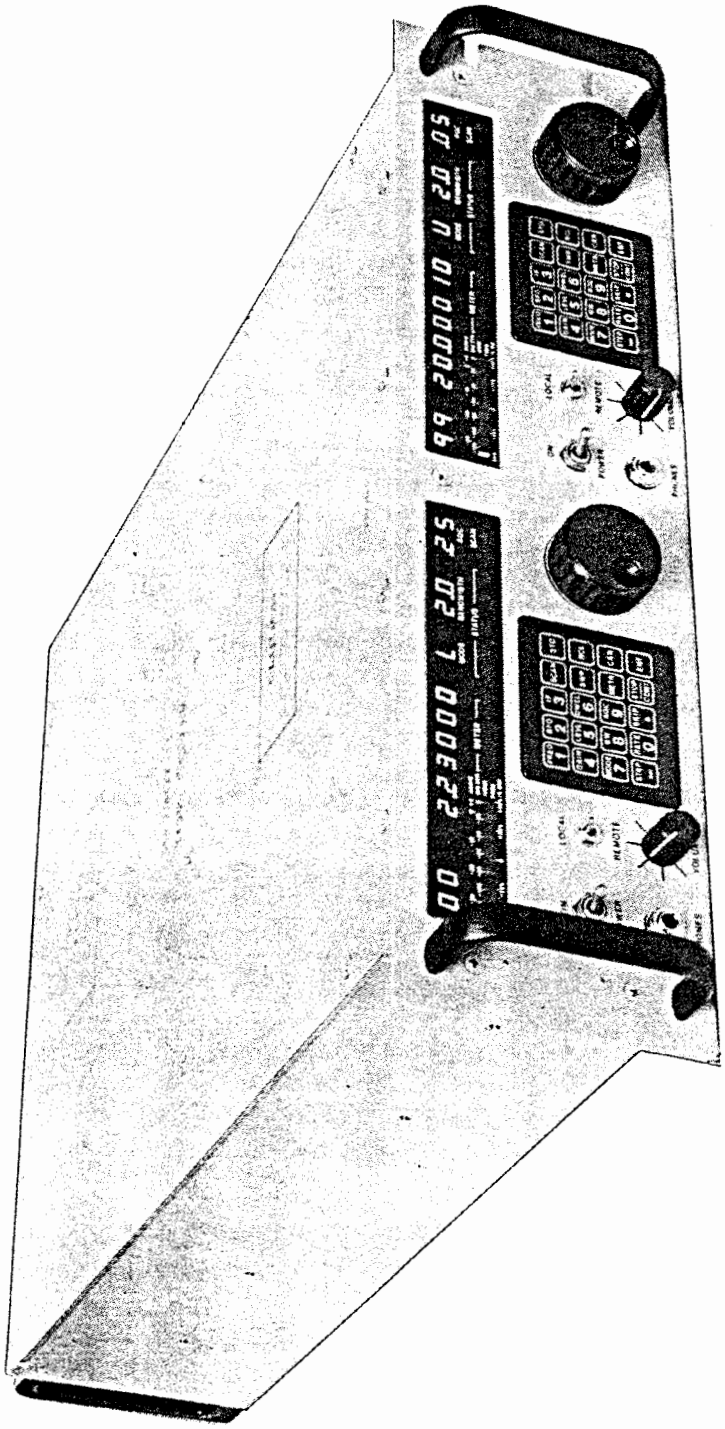


FIGURE 1-1
FRONT VIEW PHOTOGRAPH

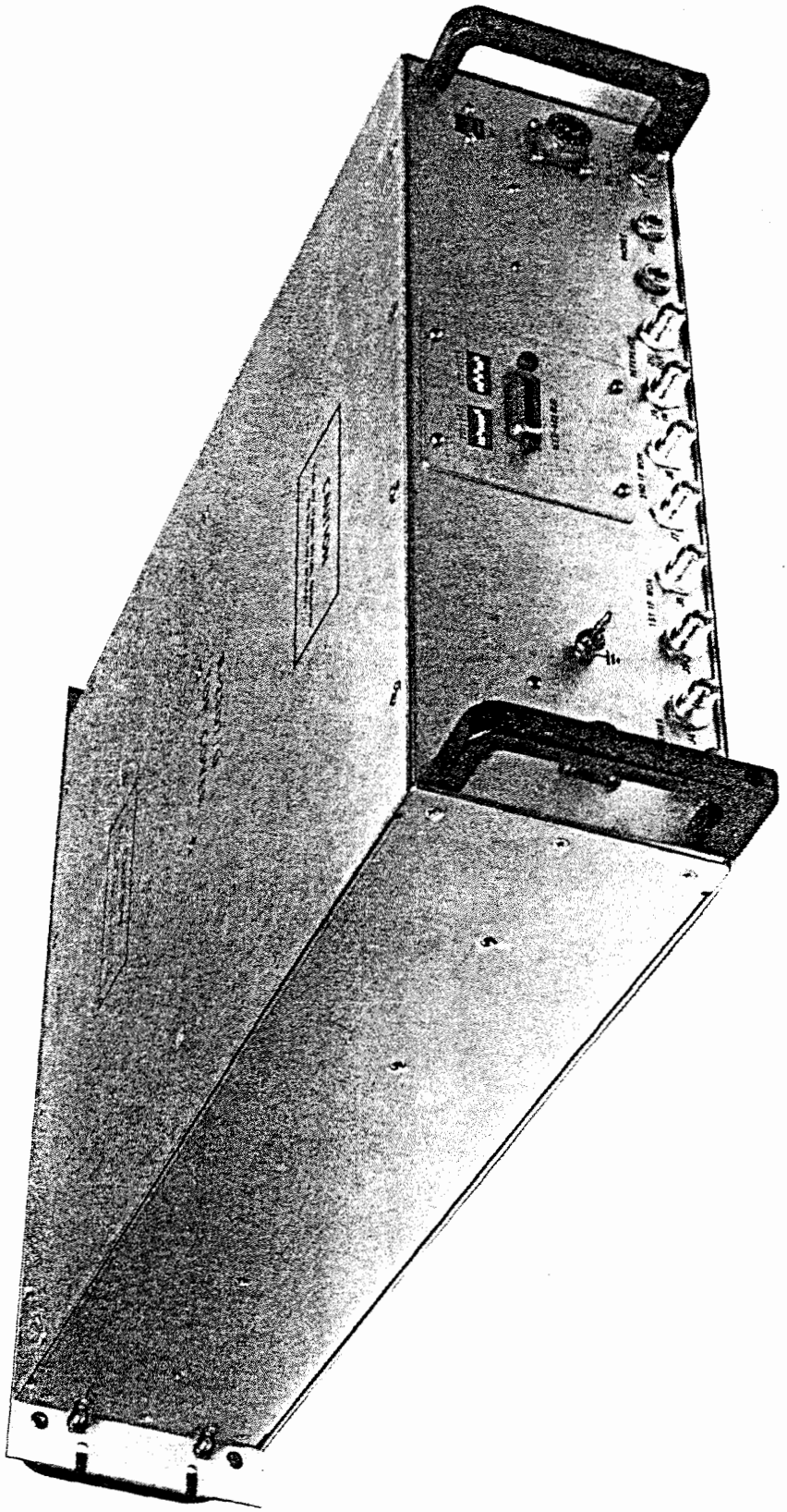


FIGURE 1-2
REAR VIEW PHOTOGRAPH

2.0 SPECIFICATIONS

2.1 PERFORMANCE

2.1.1 Frequency

Range	5 kHz - 30 MHz (Tunes to 0 Hz, optimum above 50 kHz)
Resolution	10 Hz steps
Accuracy	1 part per million over temperature range .01 parts per million per week aging
External Standard	Input/Output: 10 MHz, 0 dBm, 50 ohms
Synthesizer Lock Time	5 ms typical, 15 ms worst case

2.1.2 Modes

Selectable	LSB, USB, AM, CW, FM
Always Active	FM Video

2.1.3 RF Section

Input	50 ohms, TNC female	
Input VSWR	less than 3:1	
Protection	Withstands application of RF power up to 100 Volts RMS from a 50 ohm source without damage.	
Noise Figure	13 dB maximum above 1600 kHz, Slightly degraded below	
Sensitivity for 10 dB SINAD (above 1600 kHz)	SSB (2 kHz Bandwidth)	-118 dBm
	CW (500 Hz Bandwidth)	-124 dBm
	AM (8 kHz Bandwidth, 90% modulation)	-110 dBm

2.1.4 Preselection

RF input filter in eight bands covering 1.6-30 MHz in approximate one half octave bands. Band selection automatic and switched by PIN diodes. Filter shape factor approximately 8 to 1. Filters used below 1.6 MHz relay switched for low signal distortion.

Frequency bands as follows:

Band	Frequencies (MHz)	Band	Frequencies (MHz)
1	0.000 to 0.4999	6	4.800 to 6.8999
2	0.500 to 1.5999	7	6.900 to 9.8999
3	1.600 to 2.2999	8	9.900 to 14.2999
4	2.300 to 3.2999	9	14.300 to 20.4999
5	3.300 to 4.7999	10	20.500 to 30.0000

2.1.5 IF Section

IF Frequencies	First IF: 40.455 MHz Second IF: 455 kHz

IF Bandwidth

First IF Bandwidth:	Second IF Bandwidths (Selectable)
- 6 dB; 10 kHz min -60 dB; 30 kHz max	a. - 6 dB; 500 ± 50 Hz -60 dB; 4 kHz max
	b. - 6 dB; 1000 ± 50 Hz -60 dB; 5 kHz max
	c. - 6 dB; 2000 ± 100 Hz -60 dB; 5 kHz max
	d. - 6 dB; 4000 ± 200 Hz -60 dB; 10 kHz max
	e. - 6 dB; 8000 ± 400 Hz -60 dB; 20 kHz max
	Other bandwidths optional on special order only

2.1.6 AGC RF derived in selected bandwidth.

a. Fast attack, selectable hold, fast release

Attack Time	15 ms maximum
Hold Time (Selectable)	
Zero	15 ms maximum
Short	50 ms nominal
Medium	250 ms nominal
Long	3 seconds nominal
Off	Remote gain control only
Release Time	200 ms maximum

b. Average type -- AM mode only using Envelope detector

Attack and release time constant 220 milliseconds nominal

AGC Range	120 dB minimum
AGC Threshold	0.5 uV (-6 dB audio reference level at 50 uV)
AGC Disable	Automatic Gain Control or Manual Gain Reduction
Manual Gain Control	0 to 127 dB gain reduction with AGC disabled

2.1.7 Interference Immunity

IF Rejection	100 dB typical
Image Rejection	90 dB typical
Spurious Responses	-130 dBm equivalent or less for -50 dBm input signals
Generated Spurious	-123 dBm input equivalent or less, 2 to 30 MHz
Cross Modulation	Unmodulated wanted signal of 100uV together with a modulated (30% at 1 kHz) unwanted signal of 250mV spaced 100 kHz apart produces less than 10% cross modulation of wanted signal.
Blocking	Attenuation of a wanted RF signal of 50 uV and caused by an unmodulated unwanted signal of 1V spaced 100 kHz away, less than 3 dB.
Inherent Oscillator Re-radiation	1 uV, worst case from antenna connector into 50 Ohms.
Intermodulation Distortion (typical)	The 3rd order I.M. products resulting from two input signals at -20 dBm each less than -120 dBm.

2.1.8 I/O Signals (All connectors per two receiver assembly)

Outputs:

First IF (Wideband)	40.455 MHz with 1 MHz minimum bandwidth, 50 Ohms at approximately 10 dB gain from input (2 TNC females)
Second IF	455 kHz at selected bandwidth and nominal 0 dBm level 0 ± 3 dBm over AGC range (2 TNC Females)
Synthesizer Reference	0 dBm, 50 ohm output, 10 MHz standard (1 MHz optional) (1 TNC Female per assembly)
Audio	
Envelope or Product Frequency	0 ±3 dBm, 600 ohms balanced (with AGC active) .5 V/kHz AC coupled (4 V p-p maximum) Pair contacts on AUDIO connector (2 per assembly)
FM Video (always present)	1 V per kHz (positive sense, DC coupled) 93 ohm single ended Coax contacts on AUDIO connector (2 per assembly)
Signal Strength	Digital format on bus (8 Bit) (on BUS connector) Analog voltages on AUDIO connector (2 per assembly) (0 to + 5 VDC)

Inputs:

Synthesizer Reference	50 mV minimum, 10 MHz (1 MHz optional) (1 TNC Female)
Antenna	2 TNC Females per assembly

2.1.9 Remote Control via IEEE-488 or Parallel Bus (One only)

2.1.9.1 Receiver Functions -- (with IEEE-488 Module)

a. Selected Frequency (10 Hz increments)
b. Mode: LSB, USB, AM, CW, or FM
c. IF Bandwidth (.5, 1, 2, 4, or 8 kHz) (2 kHz only in LSB or USB modes)
d. BFO Frequency (± 9.99 kHz shift in 10 Hz steps)
e. IF Shift (± 9.99 kHz shift in 10 Hz steps)(1.4 kHz in LSB or USB modes)
f. Automatic or Remote Gain Control
g. AGC Hold Time (0, 50, 250, or 3000 msec) Note: AM selects average AGC
h. IF Gain (0 to -127 dB reduction in 1 dB steps with AGC disabled)
i. Start and Stop of Sweep and Scan Functions

2.1.9.2 IEEE-488 Bus Functions

With the units delivered starting in September of 1985 (serial number A126 and above), the formerly optional IEEE-488 module became standard. Earlier units may be retrofit as required. With the IEEE-488 module and correct software installed, the receiver implements the following IEEE-488 bus functions:

Code	Description	Comments
SH1	Source Handshake	Standard
AH1	Acceptor Handshake	Standard
T5	Talker	No Extended Capability
L3	Listener	No Extended Capability
SR1	Service Request	Rear Panel switchable SRQ enable
RL1	Remote, Local	REM and GTO, no LLO
DC0	Device Clear	Not implemented
DT0	Device Trigger	Not implemented

Interface — Driver and receiver circuits are Bus compatible. Receivers contain Bus terminating resistors and have 500 mV hysteresis. Drivers are three-state devices, capable of driving up to 15 other Bus compatible devices. Power up/down protection is included to prevent transmitting invalid data to the Bus.

Format — Sixteen lines, eight data and eight for control status message. Data transfer is byte serial using a three-wire handshake per IEEE-488 Standard.

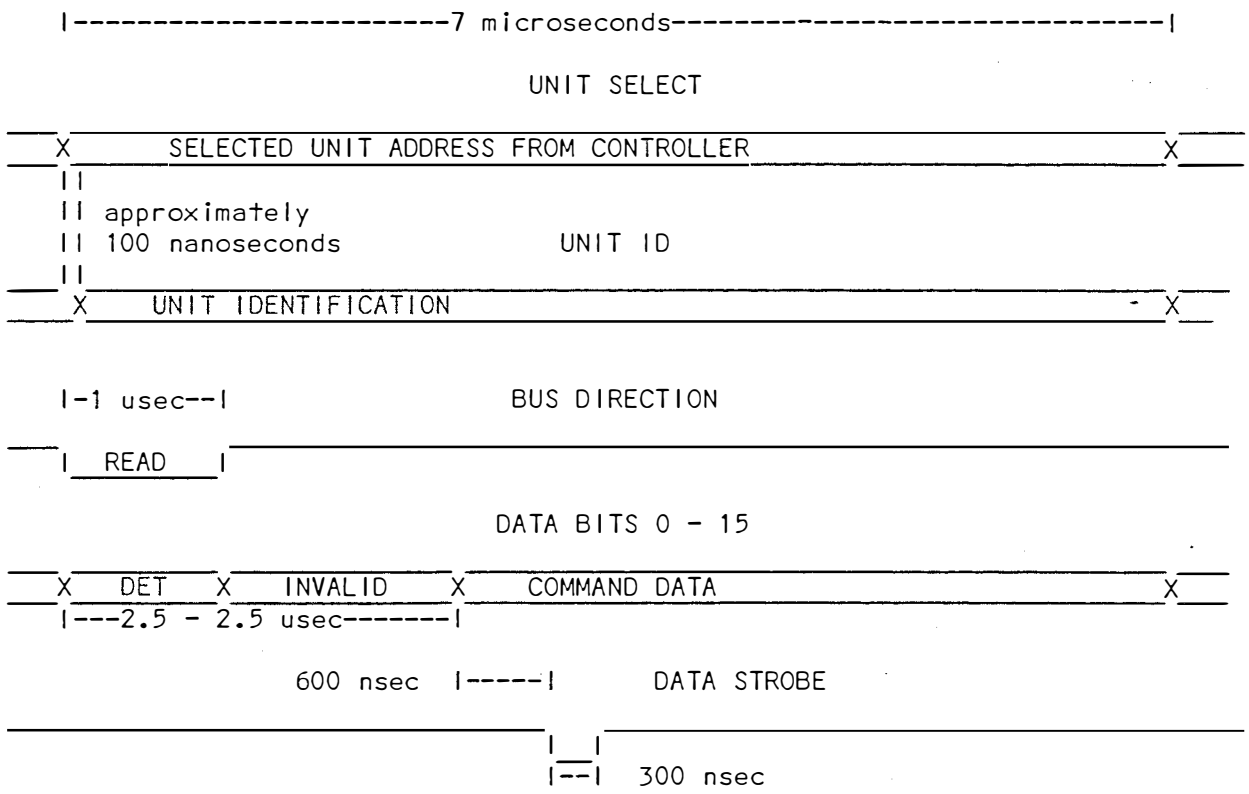
Transfer Rates — Data transfer rates is typically 11K bytes/sec when talking and 5K bytes/sec when listening.

2.1.9.3 Receiver Functions -- (with parallel bus interface)

a. Selected Frequency (10 Hz increments)
b. Detector: Envelope, Product, Frequency, or AM
c. IF Bandwidth (.5, 1, 2, 4, or 8 kHz)
d. BFO Frequency (±7.99 kHz shift in 10 Hz steps)
e. Automatic or Remote Gain Control
f. AGC Hold Time (0, 50, 250, or 3000 msec) Note: AM selects average AGC
g. IF Gain (0 to -127 dB reduction in 1 dB steps with AGC off)

2.1.9.4 Parallel Bus Timing

Data timing for any one word in accordance with figure below. Unit select for any one unit to be placed on bus from controller for approximately 7 usec every 120 usec. Four words of command data required for full control. (Approximately 480 microseconds to send all 4 words).



2.1.9.5 Parallel Bus Format

Bits in any word defined in table below:

```
Data Bus Bits  15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
Word 0        * 0   0*AGC(2) *DET(2) * BANDWIDTH *   REMOTE GAIN  (7 bits)   *
                       msb                          lsb
               Remote Gain data is dB of gain reduction (0 to 127 dB)
               AGC:  01 = Remote Gain Reduction, 10 = Automatic Gain Control
               Detector:  01 = Env., 10 = FM, 11 = Product, 00 = AM
               Bandwidth:  000 = .5 kHz,  001 = 1 kHz, 010 = 2 kHz,
                           011 =  4 kHz,  100 = 8 kHz, others not used
               Note:  AM detector selects average AGC

Data Bus Bits  15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
Word 1        * 0   1* HOLD  * ± *BFO 1kHz(3) * BFO 100 Hz(4) * BFO 10 Hz(4) *
                                    msb     lsb msb         lsb  msb        lsb
              AGC Hold: 00 = 0 msec,  01 = 50 msec, 10 = 250 msec, 11 = 3 sec.
              BFO Offset: 1 = +, 0 = -
              BFO Frequency: BCD positive true offset from IF center
              Note:  AM detector selects average AGC

Data Bus Bits  15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
Word 2        * 1   0* 10 MHz* 1 MHz (4 bits)*100 kHz(4 bits)*10 kHz (4 bits)*

Word 3        * 1   1* unused* 1 kHz (4 bits)*100 Hz (4 bits)*10 Hz  (4 bits)*
                          msb         lsb msb         lsb msb         lsb
              Frequency Data: BCD Positive true for filter center frequency

Data Bus Bits  15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
Read Cycle    * X   X*not used* RFDU BAND*FLT*   Signal Strength (8 bits)    *
                any                              msb                       lsb
              Signal Strength data is Binary,positivetrue
              Fault:  1 = Fault, 0 = no fault
              RFDU BAND for external radio frequency distribution unit
                   000 = 1 to 1.69999 MHz,    001 = 1.7 to 3.19999 MHz
                   010 = 3.2 to 4.79999 MHz,  011 = 4.8 to 6.99999 MHz
                   100 = 7.0 to 10.29999 MHz, 101 = 10.3 to 14.99999 MHz
                   110 - 15 to 21.99999 MHz,  111 = 22 to 30 MHz
```

2.1.9.6 Parallel Bus (all bus signals are TTL levels).

Data -- 16 line bi-directional (Positive true)
Unit Select -- 5 line control (Positive true)
Function Select -- 3 line control (Not used by unit)
Unit ID -- 5 line tri-state status (Positive true)
Function ACK -- 3 line tri-state status (Not used by unit)
Data Strobe -- 2 line differential control (Revised from previous issue)
Bus Direction -- 2 line differential control (Revised from previous issue)

2.1.9.7 Parallel Bus Unit Select Address and ID Code

Programmed via internal jumper plugs. Select and ID codes independently programmable.

2.1.10 Front Panel Keypad Control Functions

The following functions on the receiver are controlled from the front panel keypad. Keys may have single or dual functions. All functions are for each receiver in the chassis.

2.1.10.1 Single Function Keys

STO — Saves current frequency, mode, bandwidth, BFO offset, IF Shift, AGC hold time, manual gain setting, channel lockout (skip) flag, scan threshold, step size and scan dwell time in designated channel memory.

RCL — Puts frequency, mode, bandwidth, and AGC hold time from designated channel memory in display. Recalls also BFO offset, IF Shift, AGC hold time, and manual gain setting for use by receiver if ENTER key pressed. Recalls channel lockout (skip) flag, scan threshold, and scan dwell time for resetting if desired.

CAN — Cancels current keypad operations (before ENT key press), returns unit to previous state. Disables knob control changes.

ENT — Causes current displayed frequency, mode, bandwidth, BFO offset, IF Shift, AGC hold time, manual gain setting, and signal threshold to be programmed into receiver. Disables knob control of numerical functions.

METR — Alternate press toggle the meter between signal strength, audio, and frequency.

RATE — Sequences tuning rate between 10 Hz, 100 Hz, and 1 kHz per step or 1 dB per step on main adjustment knob and adjustment knob lock. Rate indicated by intensifying significant digit in main display. Knob lock indicated by not intensifying digit.

2.1.10.2 Dual Function Keys

SCAN / STOP — Starts scan of memory channels from channel recalled and entered to channel recalled just before SCAN key press at approximately 40 channels per second (25 msec per channel). Uses frequency, mode, bandwidth, BFO offset, IF Shift, AGC hold time, and manual gain setting from memory. Omits any channel with skip flag set. Pauses on each frequency for a time period adjustable by main adjustment knob. Stops scan on channel with signal above programmed and stored threshold for programmed and stored dwell time.

Causes SCAN or SWEEP to stop on current channel or frequency. Allows adjustment of any receiver parameter while stopped.

SWP / CONT — Starts sweep of frequency bands determined by parameters in memory channels. May sweep one band selected by even numbered channel recalled and entered sweeping to frequency stored in next higher odd numbered channel or all bands from odd numbered channel recalled and entered to channel recalled just before SWP key press.

Starting with first frequency in even numbered channel for sweep, uses frequency, mode, bandwidth, BFO offset, IF Shift, AGC hold time, and manual gain setting from memory. Sweep increment is set by stored step size and frequency is changes at approximately 50 frequencies per second. Pauses on each frequency for a time period adjustable by main adjustment knob. Halts sweep on frequency with signal above programmed and stored threshold for programmed and stored dwell time then continues sweep. Stops sweep at frequency stored in next odd numbered channel, then restarts sweep under control of frequency and other paramenters stored in next even numbered channel. Contines with sweep parameters set by even numbered channels and stop frequency set by frequency in odd numbered channels. Omits any sweep range designated by skip flag set in even numbered channel.

Causes stopped SCAN or SWEEP to be continued from current channel or frequency.

2.1.10.3 Keys That Open the Numeric Function

FREQ (1) Allows adjustment of frequency by adjustment knob. If numeric key pressed, allows keypad entry of frequency. Enter key terminates numeric entry. Display indicates "Fr" and frequency of RF input (7 digits plus decimal point at MHz).

BFO (2) Allows adjustment of BFO offset by adjustment knob. If numeric key pressed, allows keypad entry of offset frequency. Enter key terminates numeric entry. Display indicates "bF" and offset frequency of BFO (3 digits plus sign plus decimal point at kHz).

IF (3) Allows adjustment of IF shift by adjustment knob. If numeric key pressed, allows keypad entry of shift frequency. Enter key terminates numeric entry. Display indicates "IF" and shift frequency of IF (3 digits plus sign plus decimal point at kHz).

GAIN (4) Allows adjustment of RF gain by adjustment knob. If numeric key pressed, allows keypad entry of RF gain. Enter key terminates numeric entry. Display indicates "GA" and RF gain reduction in dB (3 digits).

LEVL (5) Allows adjustment of threshold level for scan or sweep stop by adjustment knob. If numeric key pressed, allows keypad entry of threshold level. Enter key terminates numeric entry. Display indicates "L" and threshold level in dBm (3 digits).

DWEL (6) Allows adjustment of time for dwell during scan or sweep operations when signal is sensed to be above programmed threshold by adjustment knob. If numeric key pressed, allows keypad entry of dwell time. Enter key terminates numeric entry. Display indicates "d" and dwell time in seconds (1 digit).

STEP (-) Allows adjustment of step size used in frequency sweep. Minus sign used for BFO offset, IF shift, and threshold offset only.

2.1.10.4 Sequential Function Keys (Numeric function not opened)

MODE (7) — Sequences mode selection between LSB, USB, AM, FM, and CW. Indicated by single letter on mode display (L, U, A, F, or C)

BW (8) — Sequences IF bandwidth between 0.5, 1.0, 2.0, 4.0,or 8.0 kHz. Approximate bandwidth indicated on display.

AGC (9) — Sequences AGC hold time between zero, 0.05, 0.25, 3.0 seconds and off. (Manual gain control only in off position). Indicated by numbers indicating approximate hold time. Blank when AGC disabled (off).

SKIP (.) — Alternate presses toggle the channel skip flag used during scan of memory channels. Indicated by SKIP annunciator.

2.1.11 Front Panel Displays

The following parameters are displayed on the front panel of the receiver. All functions are for each receiver in a 2 receiver assembly.

FUNCTION DISPLAY — Two alphanumeric characters -- 00 through 99 for store or recall, F for frequency, bF for BFO offset, IF for IF shift, GA for Gain, L for threshold level, d for dwell time, SE for step size adjustment, OF for threshold offset adjustment, blank otherwise.

MAIN DISPLAY — Seven digits numeric plus decimal points and minus sign. Used for the following functions:

FREQUENCY -- 7 digits plus . at MHz -- normal display

BFO Offset -- sign (blank or -) plus 3 digits and . at kHz -- displayed during BFO offset adjustment only.

IF Shift -- sign (blank or -) plus 3 digits and . at kHz -- displayed during IF shift adjustment only.

RF GAIN -- minus sign plus 3 digits -- displayed during RF gain adjustment only

THRESHOLD -- minus sign plus 3 digits -- displayed during threshold adjustment only.

DWELL TIME -- 1 digit -- displayed during dwell time adjust only

MODE DISPLAY — Single character -- L, U, A, C, or F

BANDWIDTH — Two characters plus decimal point indicating approximate bandwidth in kHz -- 0.5, 1.0, 2.0, 4.0, or 8.0.

AGC DISPLAY — Two digits plus decimal point indicating approximate hold time in seconds (.00, .05, .25, 3.0, or blank for MGC only)

ANNUNCIATORS

AUDIO	indicates that meter reads mode selected audio level
FREQ	indicates that meter reads relative frequency
REM	indicates that control of unit is via remote control bus
FAULT	indicates an internal detected fault
KPAD	indicates keypad entry is active, display does not necessarily indicate current frequency.
SKIP	indicates channel is skipped during scan operations

METER; 20 segment light bar meter, calibrated from -120 to 0 dBm for signal strength, -35 to + 4 dBm for audio, -50% to + 50% of IF BW for frequency.

2.1.12 Other Front Panel Controls and Functions

All functions are for each receiver in a 2 receiver assembly.

POWER ON/OFF SWITCH -- toggle type circuit breaker

LOCAL/REMOTE SWITCH -- small toggle switch for taking positive local control or allowing remote control function (Not IEEE-488 standard).

MAIN ADJUSTMENT KNOB -- 1.75 inch diameter knob on optical shaft encoder

VOLUME -- Adjusts audio level to phones jack tip and ring contacts

PHONES JACK -- Tip and ring contacts driven independently by selected mode audio. Series resistor in each circuit to protect amplifier from short circuit due to use of single circuit phone plug.

2.1.13 Rear Panel Controls

Reference Selector -- One Internal/External switch for each 2 receiver assembly.

Address Selector (IEEE-488 only) -- Two 8 position switches for selecting individual bus addresses and talker only, listener only, and SRQ enable functions.

2.1.14 Connectors (all on rear panel) per 2 receiver assembly.

RF	Antenna	TNC Female	(2 per assembly)
IF	First IF	TNC Female	(2 per assembly)
IF	Second IF	TNC Female	(2 per assembly)
REF	Reference In	TNC Female	(1 per assembly)
REF	Reference Out	TNC Female	(1 per assembly)

IEEE-488 BUS (24 cont.) Amphenol Blue Ribbon IEEE-488 stacking connector
or
PARALLEL BUS (38 cont.) MS3122A22-38P or Burndy G2B22-38PNH
(2 per assembly) on chassis, mates with cable commector
MS3126F22-38S or Burndy G6F22-38SNH

AUDIO (12 contacts) MS3122A14-92P or Burndy G2B14-92PNH
(1 per assembly) on chassis, mates with cable connector
MS3126F14-92S or Burndy G6F14-92SNH

POWER (4 contacts) MS3122A10-4P or Burndy G2B10-4PNH
(1 per assembly) on chassis, mates with cable connector
MS3126F10-4S or Burndy G6F10-4SNH
(Line on pins A and C, Ground on Pins B and D)

PHONE JACKS Rear panel phone jacks connected in parallel with
(2 per assembly) front panel phone jacks

2.1.15 Running Time Meter

Each receiver in each two-receiver assembly has a 0 to 9999 hour running time meter included. This meter operates whenever the front panel power switch is turned on and the unit is connected to AC power. The meters are mounted on the rear panel and visible from the rear of the unit.

2.1.16 Power Requirements

100 - 130 VAC or 200 - 260 VAC (selectable)
47-420 Hz, 40 watts maximum per receiver.

2.2 ENVIRONMENTAL REQUIREMENTS

2.2.1 Temperature

-20°C to +60°C Operating
-40°C to +70°C Storage

Tested to MID-STD-810D, Method 501.2, Table 501.2-111 and MIL-STD-810D, Method 501.2, Table 2.2-1.

2.2.2 Relative Humidity

Humidity test per MIL-STD-810D, Method 507.2, Procedure I, Temperature 50°C, Figure 507.2-1, 5 total cycles.

2.2.3 Shock and Vibration

Shock per MIL-STD-810D, Method 516.3 Figure 516.3-4 20g 11 ms sawtooth, 30g 11 ms in one axis

High impact shock per MIL-S-910C.

Vibration per MIL-STD-810d, Method 514.3, Figure 514.3-36 $W_o = .003g^2/Hz$ (Random)

2.2.4 Electromagnetic Emission and Susceptibility

In conformance with the applicable provisions of MIL-STD-461B, class A1a as applicable to Navy and Air Force procurements.

Filtering in conformance with MIL-STD-461B, section 4.2.1.

Requirements per MIL-STD-461B as follows:

CE01 Conducted Emissions, Power and Interconnecting Leads, Low Frequency (up to 15 kHz)
CE03 Conducted Emissions, Power and Interconnecting Leads, 0.015 to 50 MHz
CE07 Conducted Emissions, Power Leads, Spikes, Time Domain
CS01 Conducted Susceptibility, Power Leads 30 Hz to 50 kHz
CS02 Conducted Susceptibility, Power Leads 0.05 to 400 MHz
CS06 Conducted Susceptibility, Spikes, Power Leads
RE01 Radiated Emissions, Magnetic Field, 0.03 to 50 kHz
RE02 Radiated Emissions, Electric Field, 14 kHz to 10 GHz
RS01 Radiated Susceptibility, Magnetic Field, 0.03 to 50 kHz
RS02 Radiated Susceptibility, Magnetic Induction Field, Spikes and Power Frequencies
RS03 Radiated Susceptibility, Electric Field, 14 kHz to 40 GHz

2.3 PHYSICAL REQUIREMENTS

2.3.1 Construction

All chassis and module assemblies use chem-film treated aluminum alloy and stainless steel hardware in accordance with the provisions of sections 3.4.9.13 and 3.4.11.2 (j) of MIL-E-16400. No steel or other materials subject to destructive corrosion are used.

The front panel is painted with semi-gloss light gray enamel in accordance with the requirements of MIL-E-15090, Class 2, Type II or Type III, color number 26307 of FED-STD-595, with black legends and handles. Finish of all painted surfaces is in accordance with the provisions of section 3.4.11.3 of MIL-E-16400.

2.3.2 Maintainability

Access to replaceable module assemblies is by means of 1/4 turn captive fastners. Modules are secured with 1/4 turn captive fasteners. Correct module position in assembly indicated by a diagonal stripe on the module top surfaces.

2.3.3 Size

Modules for two complete receivers are packaged in one standard 5.25" X 19" rack panel and chassis with provisions for mounting slides. Slides are furnished if specified on the purchase order. Recommended slide is Chassis-Trak model C-300-S-118, Option Revision C (single hole mounting).

Depth, including protective handles, does not exceed 23" behind the front panel. Connectors on the rear panel are inside the handle dimensions and are protected by the handles and chassis from contact with any flat surface large enough to contact both handles simultaneously at any angle of contact. The rear handles include a receptacle for a standard ATR tapered locating pin. One pair of Barry 3098-005-000 pins furnished with each 2-receiver assembly.

2.3.4 Weight

Approximately 47 pounds for one chassis containing modules for two receivers not including mounting slides (optional items).

2.3.5 Reliability

The calculated Mean Time Between Failures is approximately 5000 hours per receiver unit (2 units per assembly) when calculated using the methods and failure rates of MIL-HDBK-217D with failure rates of unrated components calculated using the methods of MIL-HDBK-217D.

3.0 INSTALLATION

3.1 UNPACKING AND INSPECTION

Examine the shipping carton for damage before unpacking the unit. If the carton is damaged, open the carton in the presence of an agent of the shipping carrier if possible. If the carton is not damaged, retain the carton and packing materials for inspection if damage is found after the unit is unpacked.

Open the carton and remove the foam packing material on top of the unit. Lift the unit free of the carton. No packing materials are required or provided inside the unit. Replace the foam packing material in the carton. The carton may be saved for possible re-shipment if required.

Upon unpacking, inspect the unit for obvious external damage. Pay particular attention to dents or bent sheetmetal. If damage is evident, remove the top and bottom covers of the unit and inspect for further damage such as modules removed from their mounts or damaged circuit boards. Do not attempt to operate the unit if such damage is noted until further checks are made.

3.2 MOUNTING

The unit is designed for table top or rack panel mounting in a fixed or mobile environment in a relatively protected location. The unit is not water proof but is considered dustproof and will withstand normal interior exposure.

If slide mounting is to be used, securely mount the outer section of the slides to the rack cabinet being sure to select the correct mounting holes for the front flanges and the rear brackets. Before tightening the mounting screws securely, slide the chassis assembly into the rack mounted portion of the slides and adjust the hardware position as required for a smooth siding fit. Securely tighten all hardware. After securing all cables to the rear of the unit, insure that the proper 10-32 screws are used to secure the panel of the receiver assembly to the rack.

If the unit is not to be mounted on chassis slides, insure that a suitable shelf or angle bracket is used to support the weight of the unit and that the unit is suitably braced to prevent movement in the event of motion of the vehicle or platform in which it is installed. If it is not installed in a vehicle or other mobile platform, it may not be necessary to brace the unit against movement. The weight of the unit must, however, be adaquately supported. The rear protective handles on the unit contain recesses to accommodate standard ATR tapered locating pins to prevent movement of the receiver chassis. After mounting the unit, be sure to install the proper screws on the front panel to secure the receiver assembly.

CAUTION: DO NOT SUPPORT THE WEIGHT OF THE UNIT BY THE FRONT PANEL ONLY. USE CHASSIS SLIDES OR A SUITABLE SUPPORT SHELF

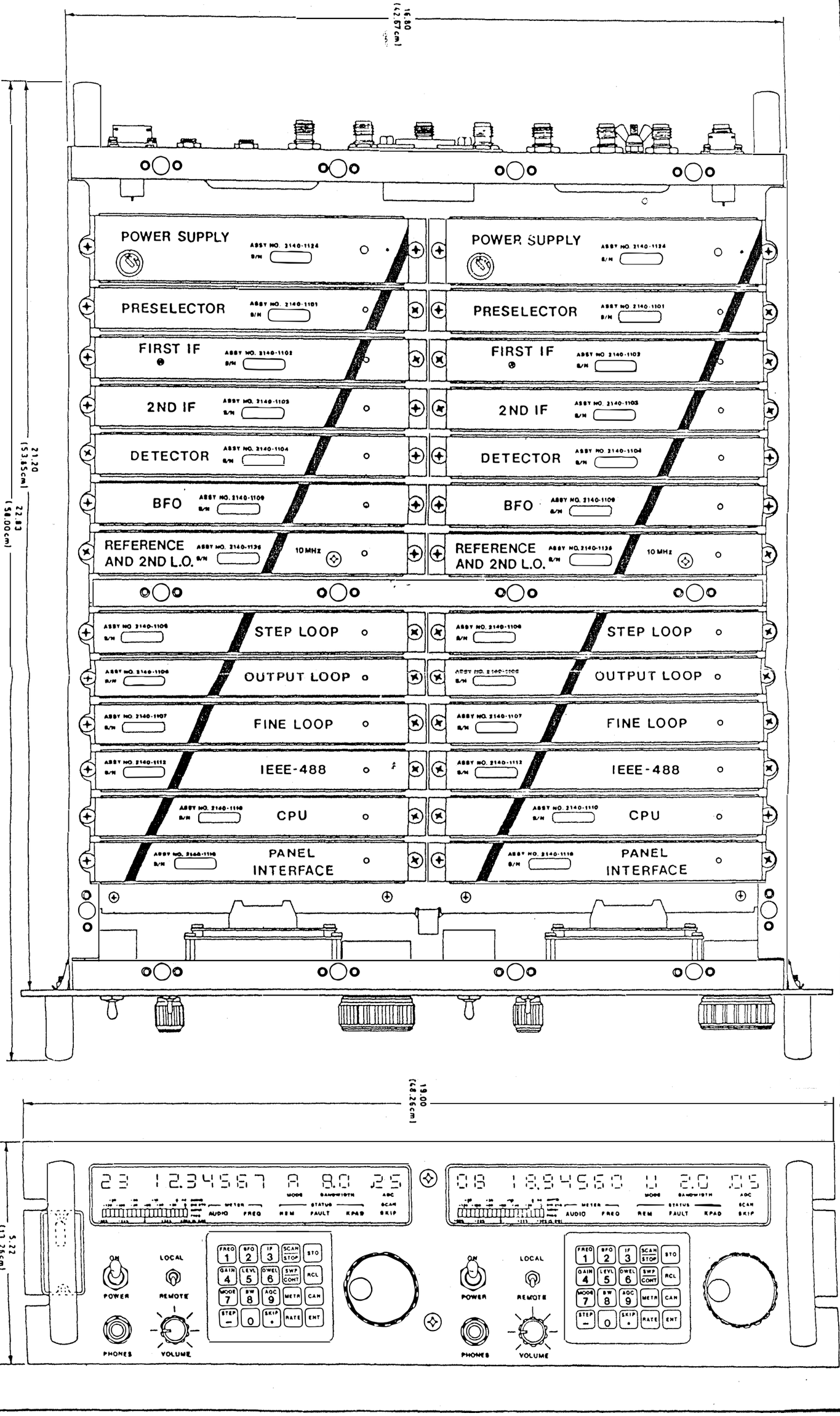
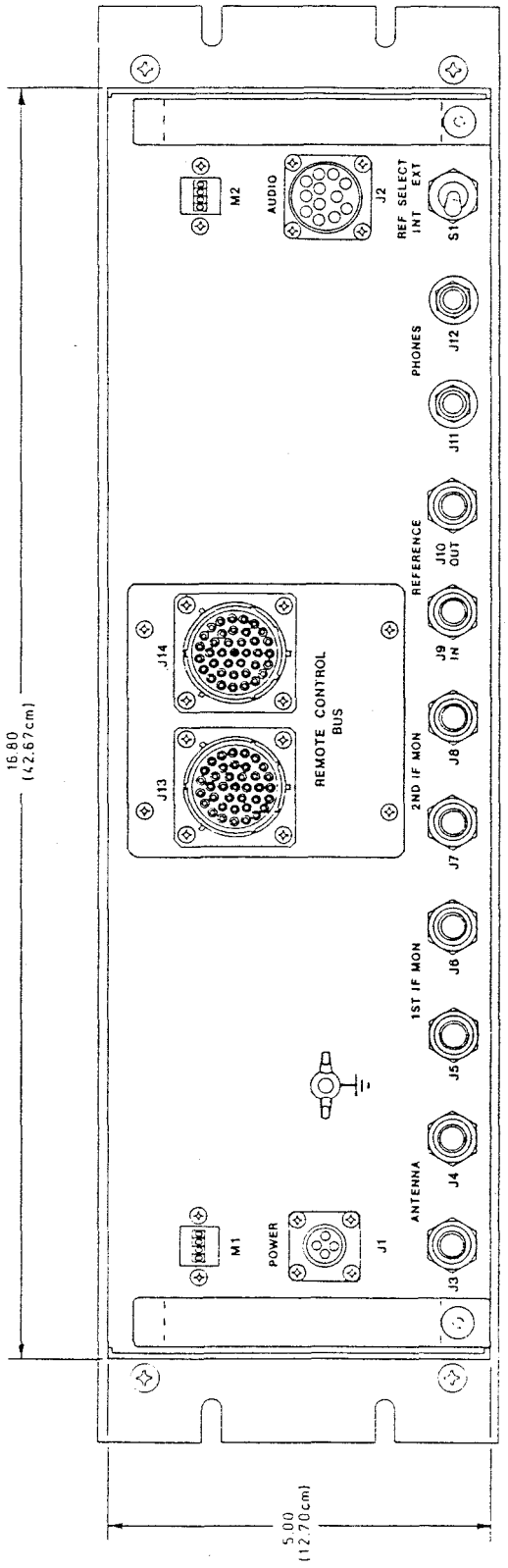
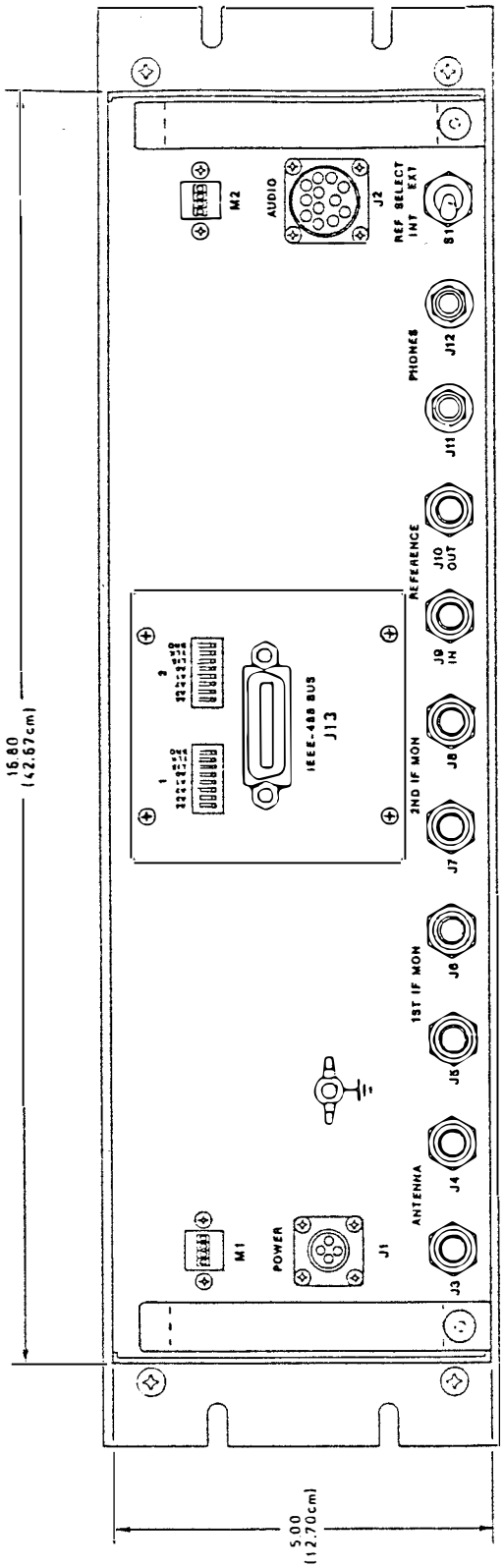


FIGURE 3-1
OUTLINE AND MOUNTING DRAWING



PARALLEL BUS INTERFACE

FIGURE 3-2
REAR PANEL PICTORIAL



IEEE-488 BUS INTERFACE

FIGURE 3-3
REAR PANEL PICTORIAL

3.3 POWER

The unit is powered from either a source of 100 to 130 VAC or 200 to 260 VAC, 47 to 400 Hz. One power connector is used per two receiver assembly and each receiver has its own power control circuit breaker.

The AC power connector (J1) is a military standard type having crimp type male contacts. The power cable has the socket type contacts. Pins A and C are used for the AC line while pin B is used for ground. If the power cable used is the shielded type, pin D may be used for the shield. Both pins B and D are connected to chassis ground.

A mating cord set is provided having a U.S.A. standard 3 pin plug for 115V service. Should a different plug be required, either cut off the U.S.A. standard plug and replace it with the desired plug or replace the cord set. The U.S.A. standard cord uses the black wire for the AC line live side, the white wire for the AC line neutral, and the green wire for chassis ground. Only the green wire is connected to the chassis. International color code for these functions uses a brown wire for the AC line live side, a light blue wire for the AC line neutral, and a green wire with a yellow tracer for the chassis ground. Either type of color code may be found in the power cable.

The unit will normally be marked with the line voltage for which it was set at the factory if the factory setting was for 220 VAC operation. Unless otherwise specified, the unit will be set to be operated from a source of 110 VAC. If the line voltage available is not as marked or if there is some doubt as to how the unit is set, remove the top cover of the assembly by undoing the 1/4 turn captive fasteners. The power supply modules are in the rear of the assembly.

Determine the AC line voltage available. If it is in the range of 100 to 130V, set the rotary switch on the power supply module to the 110V position. If the available line voltage is in the 200 to 260V range, set the rotary switches to the 220V position.

CAUTION: BE SURE THAT THE VOLTAGE SELECTOR SWITCH IS SET TO THE CORRECT POSITION FOR THE LINE VOLTAGE AVAILABLE FOR BOTH RECEIVERS IN THE TWO-RECEIVER ASSEMBLY.

3.4 ANTENNA

Connect the antennas to be used to the ANTENNA TNC receptacles on the rear panel. A separate antenna connection is made to each receiver in the assembly. As viewed from the rear of the chassis, the antenna connector on the left (J3) is connected to the receiver chassis on the left while J4 is connected to the receiver on the right. This means that the receiver connected to the antenna via J4 is controlled from the right side of the front panel and vice versa. The impedance presented to the antenna will be approximately 50 ohms with a VSWR of less than 3 to 1.

3.5 FREQUENCY STANDARD

The unit is designed to use either its internal frequency standard or an external frequency standard where very high accuracy is required. The internal frequency standard provides an overall frequency accuracy of approximately 1 part per million (30 Hz at the highest frequency).

With the rear panel REF SELECT switch set to the INT position, the rear panel REFERENCE OUT TNC receptacle (J10) will provide an output from the internal standard in receiver number 2 (right side as viewed from the rear, left side as viewed from the front) for frequency measurement or other uses. Output frequency is 10 MHz (optionally 1 MHz on special order) and is approximately a sine wave. Output level is approximately 0.6V peak-to-peak and the unit can deliver this voltage into a 50 ohm load.

With the rear panel REF SELECT switch set to the EXT position, the rear panel REFERENCE IN TNC receptacle (J9) will accept an input from an external frequency standard. The unit will require a sine or square wave at 10 MHz (optionally 1 MHz) with a level of 0.1V to 2V peak-to-peak. Input impedance is approximately 1K ohms. The signal from the external fequency standard will be repeated on the REFERENCE OUT receptacle (J10) at the same level as the internal frequency standard. NOTE: When operating from an external standard, both receivers must be turned on to insure proper operation.

Set the selector switch to the desired position. If required, connect coaxial cables from the frequency standard receptacles to a frequency measuring device, another receiver, or an external frequency standard as required.

3.6 WIDEBAND 1st IF MONITOR OUTPUT

A wideband 1st IF MON(itor) output from each receiver in the assembly is available on separate rear panel TNC receptacles. This signal is centered at 40.455 MHz with a bandwidth of approximately 1 MHz. The signal level at this output is approximately 10 dB larger than the signal level into the antenna input. This output may be used for wideband reception modes or connected to a suitable spectrum analyzer. As with the ANTENNA connectors, the connector on the left (J5) is connected to the receiver on the left and vice versa for J6.

3.7 2nd IF MONITOR OUTPUT

A narrowband 2nd IF MON(itor) output is available from both receivers in the assembly on rear panel TNC receptacles. This signal is centered at 455 kHz with a bandwidth determined by the selected bandwidth. The signal level at this output is established by the AGC circuits to be approximately -3 to +3 dBm into a 50 ohm load over an input signal level range of -110 dBm (1 microvolt) to -10 dBm. As previously, the connector on the left (J7) is connected to the receiver on the left and vice versa for J8.

3.8 AUDIO AND ANALOG CONNECTOR

Each two-receiver assembly has a common audio and analog connector for the two receivers. This connector (J2) is a military standard type with crimp type male contacts. The cable end has socket type contacts. The connections to this connector are as follows:

MS CONNECTOR	SIGNAL OR CONTROL	REMARKS
A (1)	RCVR 1 AUDIO	600 Ohm Balanced Pair
A	RCVR 1 AUDIO RTN	0 dBm nominal level
B (2)	RCVR 2 AUDIO	600 Ohm Balanced Pair
B	RCVR 2 AUDIO RTN	0 dBm nominal level
C (3)	SPARE	
D (4)	SPARE	
E (5)	RCVR 1 FM VID	1 V/KHz coax, DC coupled video
E	RCVR 1 FM SHIELD	
F (6)	RCVR 2 FM VID	1 V/KHz coax, DC coupled video
F	RCVR 2 FM SHIELD	
G (7)	RCVR 1 STR ANA	0 to + 5V RF signal strength
H (8)	RCVR 1 AUD COM	Ground
J (9)	RCVR 2 STR ANA	0 to + 5V RF signal strength
K (10)	RCVR 2 AUD COM	Ground
L (11)	SHIELD (CHASSIS)	Chassis ground
M (12)	SPARE	

NOTE: Each balanced audio pair and FM video coaxial cable is connected to a single pin in the MS connector. In each case, both contacts are made by a single mating pin.

3.9 IEEE-488 BUS CONNECTOR

If the unit is configured for remote control using an IEEE-488 bus, connection to the bus is made with a standard IEEE-488 bus connector (24 pin ribbon type). A commercially manufactured cable should be used for this connection. Make sure that both the cable and connectors are completely shielded. The receiver bus connector is located on the receiver's rear panel.

Cable requirements for the IEEE-488 bus are determined by the actual system design. Refer to the hardware installation instructions provided with the Bus Controller. The bus cables may be connected in either a "star", "daisy-chain", or any combination of the two. The total cable length must not exceed 20 meters (65.5 feet) or 2 meters (6.5 feet) for each bus device connected, whichever is less. The IEEE-488 bus connector on the receiver's rear panel is of the type specified in the IEEE-488-1972 standard and uses metric studs. Make sure the locking devices are engaged on all connectors in the system.

3.10 IEEE-488 ADDRESSING AND SRQ FUNCTIONS

Each individual receiver's bus address is selectable from 0 through 30 at the rear panel address switches using 5 of the 8 switches provided. The other 3 switches are used to enable the Talker Only, Listener Only, and SRQ Enable functions. In normal operation, the talker only and listener only functions are not enabled and the receiver functions both as a talker and a listener. The SRQ Enable function may be used if desired by the system controller software.

Each receiver in the chassis has individual address and function switches located on the rear panel.

Each receiver must be configured to a unique bus address so that the controller can send information to it independently of other devices on the bus. This is done by setting the address switches on the rear panel to the desired address between 0 and 30. The address switch has eight small switches that can be in either the up (on) position or the down (off) position. The address is set into the five left most switches in a binary code with switch number A4 as the most significant bit and switch number A0 as the least significant bit. Use the following table to determine the binary code required:

TABLE 4-1
ADDRESS SWITCHES

BUS ADDRESS	CODE 43210	BUS ADDRESS	CODE 43210	BUS ADDRESS	CODE 43210
0	00000	10	01010	20	10100
1	00001	11	01011	21	10101
2	00010	12	01100	22	10110
3	00011	13	01101	23	10111
4	00100	14	01110	24	11000
5	00101	15	01111	25	11001
6	00110	16	10000	26	11010
7	00111	17	10001	27	11011
8	01000	18	10010	28	11100
9	01001	19	10011	29	11101
				30	11110

NOTE: 0 = SWITCH DOWN, 1 = SWITCH UP

For all normal applications, set the T and L switches to the down position and the S switch to the up position.

If the switches are changed while the power is applied, the POWER switch must momentarily be turned off and then back on for the unit to recognize the new address. When choosing addresses, be sure that the number selected is not in use by any other device on the bus.

3.11 PARALLEL BUS CONNECTOR

If the unit is configured for remote control via the parallel control bus, there will be two bus connectors (J13 and J14) on the connector plate on the rear panel of the assembly. The two connectors are wired in parallel and may be used to daisy chain multiple units together. The connector used is a military standard type with crimp type male contacts. The cable end uses socket type contacts. The connections to these connectors are as follows:

SIGNAL	CONNECTOR	SIGNAL	CONNECTOR	SIGNAL	CONNECTOR
D0	H	D13	L	STROBE	e
D1	G	D14	K	BUS DIR	f
D2	F	D15	J	BUS GND	g
D3	E	SEL0	T	SHIELD	h
D4	D	SEL1	U	SPARE	i
D5	C	SEL2	W	SPARE	j
D6	B	SEL3	X	SPARE	k
D7	A	SEL4	Y	SPARE	m
D8	S	ID0	Z	SPARE	n
D9	R	ID1	a	SPARE	p
D10	P	ID2	b	SPARE	r
D11	N	ID3	c	SPARE	s
D12	M	ID4	d		

At the request of the controlling organization for the parallel bus (Electronic Support Systems, Inc. (ESSI)), the pin connections for this bus have been changed starting with parallel bus option units delivered starting in September of 1985. The new pin connections are as follows:

SIGNAL	CONNECTOR	SIGNAL	CONNECTOR	SIGNAL	CONNECTOR	
D0	T	D13	D	ID3	f	
D1	S	D14	C	ID4	e	
D2	R	D15	B	ID5	d	(NOT USED)
D3	P	SEL0	c	-STROBE	k	
D4	N	SEL1	b	+STROBE	m	
D5	M	SEL2	a	-BDIR	n	
D6	L	SEL3	Z	+BDIR	p	
D7	K	SEL4	Y	-HYT	r	
D8	J	SEL5	X (NOT USED)	+HYTE	s	
D9	H	SEL6	W (NOT USED)	BUS GND	A	
D10	G	ID0	j	SHIELD	V	
D11	F	ID1	h			
D12	E	ID2	g			

3.11 PARALLEL BUS SELECT AND ID CODES

Before beginning operations, the unit select address and unit ID codes must be set. These codes are set by means of jumper plugs internal to the respective bus interface modules. If the codes are not known or if it is desired to change these codes, remove the top cover of the assembly by undoing the 1/4 turn captive fasteners and remove the Bus Interface modules (BIM). Remove the front cover of the BIM (with the tabs covering the connector access slots) and set the jumpers according to the instructions for system operation.

The two sets of jumpers must be set in accordance with the following table for both the select and ID codes.

JUMPER	SELECT OR ID CODE															
POSITION	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

JUMPER	SELECT OR ID CODE															
POSITION	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

It will be found advisable to mark the select and ID codes set on the top surface of the individual Bus Interface Modules and also to mark these codes on the rear surface of the units. Marking in this way will eliminate the need to disassemble the units later in order to determine the codes used. The receiver is normally furnished with write-on type labels both on the rear panel and on the top of the bus interface modules.

3.13 CONTACTS

CONTACTS FOR R-2307/U PARALLEL BUS, AUDIO, AND POWER CONNECTORS

The following contacts are identified for use on external cabling for use on the R-2307/U parallel bus, audio, and AC power connectors. The appropriate contact must be chosen to be suitable for the type of wire used.

All contacts are to be attached to the wire by suitable crimp tools or by the use of the applicable heat gun and holding fixtures. The Burndy contacts are crimp type while the Raychem contacts are solder type. These contacts are not intended to be soldered to the wire using ordinary soldering irons.

The reference to installation tool includes both the crimp tool and the required die set or, in the case of the Raychem contacts, the heat gun, shield, and holding fixture. The instructions given by the contact manufacturer must be followed exactly. The completed contact and wire assembly is inserted into the connector without the use of any specific tool. Use the Burndy RX16D11-D1 extraction tool for all contacts. Unless otherwise noted, all part numbers are Burndy part numbers.

1) SOCKET CONTACTS FOR SINGLE WIRE

WIRE SIZE	INSULATION DIAMETER	PART NUMBER	INSTALLATION TOOL
28	.028-.037	RC28M-1D28	M8ND/N24RT-10 or M10S-1/S-9/SL-40
24/26	.035-.062	RM24M-9D28	M8ND/N24RT-10 or M10S-1/S-9/SL-40
20/22	.046-.062	RM20M-13D28	M8ND/N20RT-30 or M10S-1/S-10/SL-40
20/22	.060-.090	RM20M-12D28	M8ND/N20RT-30 or M10S-1/S-10/SL-40

2) SOCKET CONTACTS FOR TWISTED PAIR WIRE

WIRE STRAND	INSULATION DIA. MAX.	PART NUMBER	INSTALLATION TOOL
24/26	.049	RCDX60-19D28	M10SG8
24/26	.028	RCDX60-31D28	M10S-1/S-80/SL-105
22/26		RAYCHEM D-602-0239	RAYCHEM AA-400/979663 or CV-5700/MG-7 AT-1319/AT-1319-12 FIXTURE

3) SOCKET CONTACTS FOR COAXIAL CABLE

CABLE TYPE	PART NUMBER	INSTALLATION TOOL
174	RCDX60-32	M10S-1/S-80/SL-107
188/316	RCDX60-36	M10S-1/S-80/SL-107
174/178/ 179/316	RAYCHEM D-602-0-219	RAYCHEM AA-400/979663 or CV-5700/MG-7 AT-1319/AT-1319-12 FIXTURE

4.0 OPERATION

The receiver can be operated either by an operator using the front panel controls or remotely using a computer or bus controller. The receiver may be supplied with a remote control interface for an IEEE-488 bus, a special parallel bus, or other remote control interface as ordered.

When operating the receiver, it is ordinarily desirable to set the receiver parameters in the following manner for signals having the indicated characteristic.

Signal	Bandwidth	Mode	AGC	BFO or IF Shift	Remarks
AM Voice	4 or 8 kHz	AM	N/A	N/A	Average AGC
SSB Voice	2 kHz	LSB or USB	.25	1.4 kHz	Automatic from panel
SSB Voice	4 kHz	CW	3.0	IF ± 2.3 kHz	Wideband Voice
CW Morse	.5 kHz	CW	.25	BFO .8 TO 1kHz	Operator Preference
SSB Data	.5 or 1 kHz	CW	.05	BFO 1 to 3 kHz	Narrow Band data
SSB Data	1 to 4 kHz	CW	.05	BFO 1 to 3 kHz	Wide Band data
FSK Data	.5 or 1 kHz	Frequency	.05	N/A	Narrow Band date
FSK Data	1 to 4 kHz	Frequency	.05	N/A	Wide Band data
Pulse	8 kHz	AM	Off	N/A	Manual gain reduction
Sweep	8 kHz	CW	0.0	BFO 1 kHz	Search for Unknown

When operating from the parallel bus, CW, LSB, or USB modes are selected by using the product detector and varying the BFO offset as required. When receiving data or voice signals in the CW mode using the product detector, the BFO offset may be varied to provide an output signal of the correct pitch.

The LSB and USB modes select the bandwidth to be 2 kHz and the IF shift to be 1.4 kHz automatically with no operator intervention necessary or possible.

It is important to note that the receiver frequency set for all but LSB or USB modes is the center of the information band and does not bear any particular relationship to the carrier frequency for SSB voice or data signals while receiving in the CW mode. The IF shift function may be used to shift the apparent bandwidth with respect to the indicated frequency in the CW mode or the BFO offset may be used to vary the apparent pitch of the signal centered on the indicated frequency. Using IF shift, the apparent pitch remains the same while the position of the bandwidth varies with respect to the carrier frequency.

In all cases using the CW mode, the BFO signal is used to substitute for the carrier signal and the true carrier frequency will be equal to the indicated receiver frequency plus the BFO offset with a zero beat condition. The BFO offsets will be negative for USB signals and positive for LSB signals.

The frequency detector can be used to demodulate or determine the frequency shift of FSK data signals. A more optimum detection process will be to use the product detector in CW mode and process the resultant tones through a suitable audio modem. This technique will take advantage of narrower bandwidth filters in the audio modem and can result in data copy even in cases where selective fading has temporarily removed one of the tones.

4.1 MANUAL OPERATION

Manual operation is performed using the 20 button keypad, front panel displays, and adjustment knob. The front panel volume control is used to vary the signal level to the headphone jacks only and does not affect the level of signal supplied to the 600 Ohm balanced line. To select manual operation, set the front panel LOCAL/REMOTE switch to the LOCAL position and turn the power switch on. The receiver will power up with the frequency and other parameters last set into it before power was removed.

In order to adjust the receiver parameters, locate the parameter desired to be changed or reviewed below. Follow the instructions and indications listed and refer to the control panel pictorial in Figure 4-1.

4.1.1 Normal State -- Press CAN or ENT for the normal state

In the normal state (that is, no attempt is being made to change any of the numeric parameters), the display indicates the following information:

Function -- If the frequency and other parameters have been recalled from memory, this display indicates the 2 digit memory indication, otherwise the display is dark.

Frequency -- Display indicates the frequency in MHz -- carrier frequency in LSB or USB, center frequency in the other modes. The digit selected for tuning will be of higher intensity.

Mode -- A single letter -- L for LSB, U for USB, C for CW, A for AM, F for FM.

Bandwidth -- 2 numeric digits and a decimal point indicating the nominal bandwidth -- 0.5, 1.0, 2.0, 4.0, or 8.0 KHz

AGC -- 2 numeric digits and a decimal point indicating the nominal AGC hold time -- 0.0, .05, .25, and 3.0. Display is dark if manual gain control has been selected.

METER -- 2 annunciators, if neither one is illuminated, the bargraph meter indicates RF signal strength; if the AUDIO annunciator is illuminated, the meter indicates audio output level; if the FREQ annunciator is illuminated, the meter indicates the relative frequency of the input signal with respect to the band center -- each bar represents 5% of the bandwidth selected.

REM -- Dark annunciator in local control

FAULT -- Dark annunciator in the absence of a fault

KPAD -- Dark annunciator

SKIP -- Annunciator used in Scan operations only.

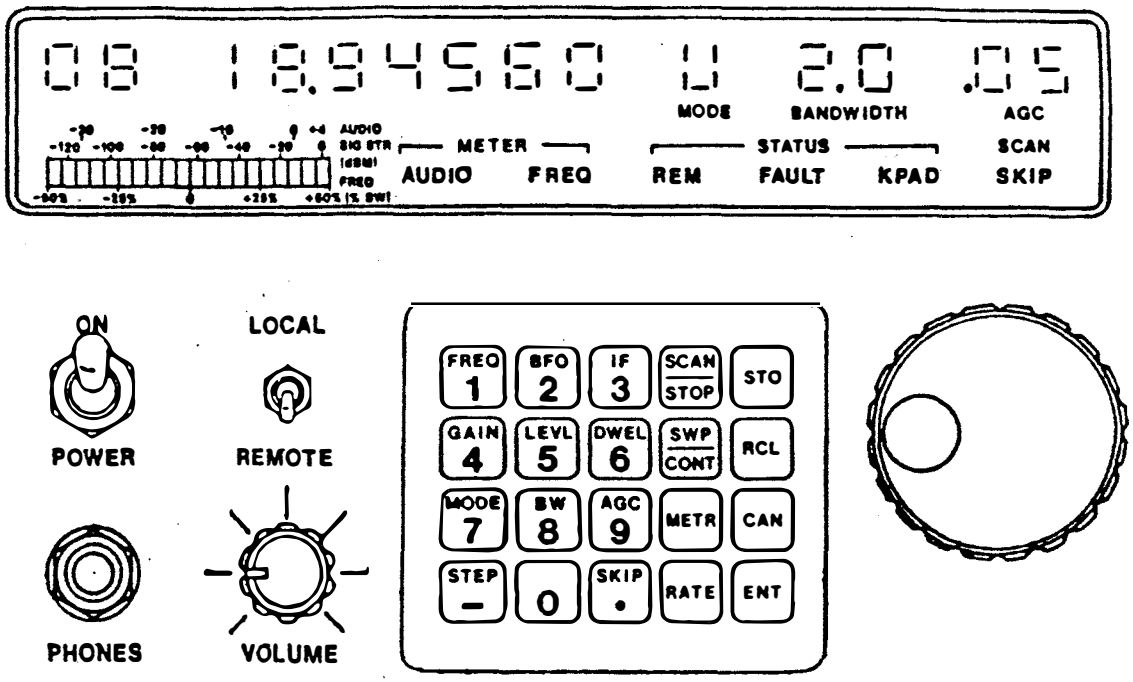


FIGURE 4-1
CONTROL PANEL PICTORIAL

4.1.2 Direct Function Changes

MODE -- Press the MODE (7) key from the normal state
Observe the MODE letter change, select the mode desired
C is CW, A is AM, L is LSB, U is USB, and F is FM

BANDWIDTH -- Press the BW (8) key from the normal state
Observe the BW value change, select the bandwidth desired
Note that bandwidth is always 2.0 in LSB or USB

AGC -- Press the AGC (9) key from the normal state
Observe the AGC hold time value change from off (dark), 0.0, .05, .25, and 3.0 seconds

METER -- Press the METR key from the normal state
Observe the meter annunciators change from dark to AUDIO to FREQ to dark again and observe the bargraph meter indication change accordingly.

When the annunciator is dark, the meter indicates input signal strength (when AGC is enabled) from -120 to 0 dBm (into 50 Ohms). Each segment of the display represents approximately 6 dB. When AGC is disabled, the manual gain control can be used to position the indication to the middle of the meter scale.

When the annunciator indicates AUDIO, the meter indicates audio output level to the 600 Ohm line from -30 to +4 dBm (with a 600 Ohm load). Each segment of the display represents approximately 2 dB.

When the annunciator indicates FREQ, the meter indicates the approximate frequency of the signal with respect to the center of the IF bandwidth. Each segment of the display represents approximately 5% of the total IF bandwidth (400 Hz with 8 kHz BW, 200 Hz with 4 kHz BW, 100 Hz with 2 kHz BW, etc.).
Note: when exactly on the center frequency, both segments on either side of 0 should be observed to be flashing.

RATE -- Press the RATE key from the normal state.
Observe the 10 Hz, 100 Hz, and 1 kHz digit in the frequency display successively intensify. This function will select the digit that the adjustment knob will change when the FREQ key is later pressed. The BFO offset and IF shift functions automatically shift to the 10 Hz rate if the 100 Hz or 1 kHz rates are selected.

SKIP -- Press the SKIP (.) key from the normal state.
Observe the SKIP annunciator alternately illuminate and go dark. This function is used to indicate memory channels to be skipped during a scan operation and frequencies to be skipped during a sweep operation.

4.1.3 Knob or Numeric Entry

FREQUENCY -- Press the FREQ (1) key from the normal state.
The function display should show "Fr"
The adjustment knob is enabled for the intensified digit
Digits to the right of the intensified digit will go to zero
when the adjustment knob is moved
The receiver follows the displayed value
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required
The receiver stays at the last frequency
Press CAN to cancel data or ENT to enter data
Receiver is now at new frequency
The KPAD annunciator should be dark

BFO OFFSET -- Press the BFO (2) key from the normal state.
The function display should show "bF"
The display should show the current BFO offset or "OFF"
The adjustment knob is enabled in CW mode only
The adjustment knob is enabled for 10 Hz increments
The receiver follows the displayed value
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required in CW mode only
The receiver stays at the last BFO offset
Press CAN to cancel data or ENT to enter data
Receiver is now at new BFO offset
The KPAD annunciator should be dark

IF SHIFT -- Press the IF (3) key from the normal state.
The function display should show "IF"
The display should show the current IF shift or "OFF"
The adjustment knob is enabled in CW mode only
The adjustment knob is enabled for 10 Hz increments
The receiver follows the displayed value
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required in CW mode only
The receiver stays at the last IF shift
Press CAN to cancel data or ENT to enter data
Receiver is now at new IF shift
The KPAD annunciator should be dark

RF GAIN -- Press the GAIN (4) key from the normal state.
The function display should show "GA"
The adjustment knob is enabled for 1 dB adjustment steps
The receiver follows the displayed value if AGC is off
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required
The receiver stays at the last gain reduction
Press CAN to cancel data or ENT to enter data
Receiver is now at new RF gain if AGC is off
The KPAD annunciator should be dark

LEVEL -- Press the LEVL (5) key from the normal state.
The function display should show "L"
The display should show the current level for squelch or scan stop
The adjustment knob is enabled for 1 dB adjustments steps
The receiver follows the displayed value
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required
The receiver stays at the last threshold
Press CAN to cancel data or ENT to enter data
Receiver is now at new level for squelch or scan stop
The KPAD annunciator should be dark
Data must be stored in a channel memory for scan or sweep stop

DWELL -- Press the DWEL (6) key from the normal state.
The function display should show "d"
The display should show the current dwell time for scan or sweep stop
The adjustment knob is enabled for one second adjustment steps
1 through 9 indicates dwell time, 0 indicates extended dwell
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press another number as required
The receiver stays at the last dwell time
Press CAN to cancel data or ENT to enter data
Receiver is set for new dwell time for scan or sweep stop
The KPAD annunciator should be dark
Data must be stored in a channel memory to be effective

STEP -- Press the STEP key from the normal state.
The function display should show "SE"
The display should show the current step size for sweep
The adjustment knob is enabled for .1 kHz step size
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press keys for the desired step size
Press CAN to cancel data or ENT to enter data
Receiver is set for new step size during sweep
The KPAD annunciator should be dark
Data must be stored in a channel memory to be effective

4.1.4 Store and Recall Functions

STORE -- Press the STO key from the normal state.
The function display should show 2 dashes.
Press 2 numeric keys in succession (00 through 99).
All channel data is stored in the memory indicated.

RECALL -- Press the RCL key from the normal state.
The function display should show 2 dashes.
The KPAD annunciator should be illuminated.
Press 2 numeric keys in succession (00 through 99) and/or
Use the adjustment knob to increment or decrement the channel
The display should show the recalled parameters.
The receiver remains at the last entered frequency.
Press CAN to cancel data or ENT to enter data, or;

Press the BFO (2) key to review the BFO offset recalled.
Press the IF (3) key to review the IF shift recalled.
Press the GAIN (4) key to review the RF gain recalled.
Press the LEVL (5) key to review the squelch level recalled.
Press the DWELL (6) key to review the dwell time recalled.
The adjustment knob can be used to recall data from all channels.

Press CAN to cancel recall or ENT to enter data.
The KPAD annunciator should be dark.
Receiver is on recalled frequency if ENT key pressed.
Receiver is on previous frequency if CAN key pressed.
Press skip key, SP will appear in the channel display.
Press ENT to clear skip memory at this point.

Note: Recalled memory numbers remain illuminated as long as no parameters are changed from keypad. If any parameter is changed, memory numbers are no longer displayed. New parameters must be stored to be placed back in memory.

ERASE -- To clear all memory channels of all entered data and replace data with a frequency of 10 MHz, AM mode, 8 kHz bandwidth:
Press RCL . . 9 1 1 ENT

4.1.5 Scan and Sweep Operations

All scan and sweep operations are performed from the condition where one channel has been recalled from memory and entered (using the ENT key) into the receiver. Scan is the sequential recall from memory of all channel parameters from a series of channels while sweep is the sequential entry of a series of frequencies using parameters set from one even numbered recalled channel and incrementing or decrementing the frequency as required until the frequency equals the frequency of an adjacent odd numbered channel. Multiple frequency bands can be covered in the sweep process.

Scan or sweep stop is performed when a signal is observed to be greater than the stored and recalled threshold level and the scan or sweep remains stopped for the recalled dwell time. If the recalled dwell time indicates 0, the scan or sweep will stop until the signal level falls below the threshold level. Scan or sweep rate is under the control of the adjustment knob and can also be stopped or continued under keypad control.

SCAN / STOP -- Recall and enter the desired numbered channel for scan start.
Recall, but do not enter the desired numbered channel for scan stop (may be higher or lower in number than for start).
Press the SCAN key.
The function display should show "OF".
The adjust knob will be enabled for threshold offset adjustment, and/or the keypad will be enabled for threshold offset adjustment.
The offset is + or - dB from the stored threshold level
Press ENT to start the scan
The receiver will sequentially scan from the start channel to the stop channel and continue.
The scan will stop if the signal level is above the stored level as modified by the offset adjustment.
The scan will restart at the end of the stored dwell time.
The receiver will skip all channels having the SKIP status stored.
Rotate the adjustment knob counter-clockwise to slow the scan.

Press the SCAN/STOP key to stop the scan.
The adjustment knob will be enabled for frequency adjustment.
At this point, any receiver parameter may be changed under keypad and/or knob control as required.
Press the SKIP key if is desired to skip this channel on the next and successive scans.
Press the SWP/CONT key to continue the scan from stop.
Press the CAN key to leave the scan mode from stop.

Quick reference:

RCL ## ENT RCL %% SCAN * ENT**

Where ## is the start channel, %% the stop channel, and *** the offset.

SWEEP / CONT -- Recall and enter the even numbered channel containing the start frequency for sweep.
Recall, but do not enter, the odd numbered channel containing the stop frequency. This may be several or many channels away from the channel selected for start.
Press the SWP key.
The function display should show "OF".
The adjust knob will be enabled for threshold offset adjustment, and/or the keypad will be enabled for threshold offset adjustment.
The offset is + or - dB from the stored threshold level
Press ENT to start the sweep.
The receiver will use the parameters in the even numbered channel recalled and entered.
The receiver will increment or decrement the frequency by the entered step size as required until the frequency equals the frequency in the next highest odd numbered channel.
The sweep will stop if the signal level is above the stored level as modified by the offset adjustment.
The sweep will restart at the end of the stored dwell time.
The receiver will skip all frequencies having the SKIP status stored in the even numbered channel at the start of each sweep.
The sweep will continue from the next even numbered channel.
The sweep will continue until the odd numbered channel recalled just before the press of the SWP key is reached.
The sweep will restart from the even numbered channel recalled and entered.
Rotate the adjustment knob counter-clockwise to slow the sweep.
Press the SCAN/STOP key to stop the sweep at any time.
The adjustment knob will be enabled for frequency adjustment.
At this point, any receiver parameter may be changed under keypad and/or knob control as required.
Press the SKIP key if it is desired to skip this frequency on the next and successive sweeps.
Press the SWP/CONT key to continue the sweep from stop
Press the CAN key to leave the sweep mode from stop

Quick reference:

RCL ## ENT RCL %% SWP * ENT**

Where ## is the start channel, %% the stop channel, and *** the offset.

CLEAR SKIP MEMORY -- Clears all frequencies from the sweep skip memory.
From the normal state, press RCL, SKIP, 2, ENT.
"Fn" appears in the status display when SKIP is pressed.
"SP" appears in the status display when 2 is pressed.

4.1.6 Software Version

To display the current software version perform the following:

SOFTWARE VERSION -- From the normal state, press RCL, SKIP, 1, ENT.
"Fn" appears in the status display when SKIP is pressed.
"Sn" appears in the status display when 1 is pressed.
The current software version is displayed in the main display.

4.2 REMOTE OPERATION USING IEEE-488 BUS

The R-2307 can be operated under remote control, using an IEEE-488 bus, if the optional IEEE-488 bus module, bus connector, and appropriate software is installed. To operate in the remote mode, set the front panel REMOTE/LOCAL switch to the REMOTE position. When the switch is in the REMOTE position, the controller determines whether the R-2307 is in the remote or local mode; the controller can command the R-2307 to enter the local mode. When the controller commands the R-2307 to enter the local mode, the front panel REM indicator will extinguish.

4.2.1 IEEE-488 Bus Description

The IEEE-488 bus uses a party-line bus structure consisting of 16 signal lines. Devices are connected in parallel to the bus and information is passed in a byte serial/bit parallel fashion. Refer to IEEE Std 488 for a complete description of the IEEE-488 bus.

The interface functions for each component are performed within the component so that only passive cabling is needed to connect the system. The cables connect all instruments, components, and the controller of the system in parallel to the signal.

The 16 signal lines are divided into three major functional groups: bus management lines, handshake lines, and data lines. There are five bus management lines, three handshake lines, and eight data lines. Data and message transfer is asynchronous.

Devices connected to the bus may be talkers, listeners, or controller. Only one controller may be used on the bus. The controller dictates the role of each of the other devices by setting the ATN (attention) line true and by sending talk or listen addresses on the data lines. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data. All others ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while the ATN is true), all other talkers will automatically be unaddressed.

The bus management lines conduct an orderly flow of information across the bus. The five bus management signals are as follows:

Name	Mnemonic	Description
Attention	ATN	Causes all devices to interpret data on the bus as a controller command. When ATN is true, the bus is placed in the "Command Mode". That is, all devices on the bus interpret data on the eight data lines as commands. When ATN is false, the bus is placed in the "Data Mode". That is, all active listeners on the bus interpret data on the eight data lines as data.
Interface Clear	IFC	Clears the bus. Sets the bus to an idle state.
Service Request	SRQ	Alerts the controller to a need for communication.
Remote Enable	REN	Enables devices to respond to remote program control when addressed by the controller.
End or Identify	EOI	Indicates last byte of multibyte sequence.

The three handshake lines coordinate the transfer of data over the bus. Transfer is asynchronous and the transfer rate automatically adjusts to the speed of the source and acceptor. The transfer rate will be that of the slowest active device. The three handshake lines are: Data Valid (DAV), Not Ready for Data (NRFD), and Not Data Accepted (NDAC). The DAV signal is sent by the source to indicate that the byte on the eight data lines is valid. The NRFD and NDAC signals are sent by the acceptors to indicate when they are ready for data and when they have accepted data. The following table defines the three handshake lines:

Name	Mnemonic	Description
Data Valid	DAV	Indicates that data on the bus is valid. All active devices on the bus can accept the byte as true information.
Not Ready for Data	NRFD	Indicates that a device is not ready to accept data.
Not Data Accepted	NDAC	Indicates that the data byte has not yet been read from the bus.

The eight bidirectional data lines (DIO1 - DIO8) are used to transfer data bytes along the bus. Which device sends and which devices receive the byte is determined by the bus management signals. How long the byte remains on the bus is determined by the handshake lines.

The R-2307 acts as a talker and a listener. The SRQ function is selectable by means of a switch on the rear panel. If the SRQ function is disabled, the R-2307 will not be able to demand controller attention for communication. Two other switches on the rear panel are used to select unaddressed "Talk Only" and "Listen Only" modes.

4.2.2 Listen Data Sequence

When the R-2307 is addressed to listen, it accepts data from the bus. This information is used to set the operating parameters of the R-2307. The following table contains an alphabetical listing of the listen protocol for the R-2307.

Function to Set	Message Format	Description
AGC hold time	A*	Where * represents a letter (Z,S,M,L,O) indicating the AGC hold as follows: Z = Zero (0) S = Short (50 ms) M = Medium (250 ms) L = Long (3 seconds) O = Off (manual)
BFO	B±123	Where ± represents "+" or "-" sign and the digits 1 through 3 represent the BFO frequency (digit 1 = 1 kHz increments, digit 2 = 100 Hz increments, and digit 3 = 10 Hz increments). Valid in CW mode only.
Cancel	K	Current command is immediately cancelled.
Clear	CL	Clears all channel memory locations (default to 10 MHz, AM mode).
Clear Skip	CS	Clears Skip Memory function.
Continue scan or continue sweep	CO	Causes R-2307 to resume scanning or sweeping.

Function to Set	Message Format	Description
Dwell time	D#	Where # represents the dwell time after signal detection in scan or sweep. Digits 1 through 9 represent the dwell time in seconds. Digit 0 indicates a dwell time lasting as long as a signal is present.
Frequency	F1234567	Where digits 1 through 7 represent the operating frequency. The most significant digit is 1 (10 MHz) while the least significant digit is 7 (10 Hz).
Gain	G123	Digits 1 through 3 represent the IF gain reduction in dB (digit 1 = 100 dB increments, digit 2 = 10 dB increments, and digit 3 = 1 dB increments).
IF bandwidth	W#	Where # represents a number from 0 - 5 indicating the IF bandwidth. The narrowest bandwidth is represented by digit 0 while the widest bandwidth is represented by the digit 5.
IF shift	I±123	Where ± represents "+" or "-" sign and the digits 1 through 3 represent the frequency IF frequency (digit 1 = 1 kHz increments, digit 2 = 100 Hz increments, and digit 3 = 10 Hz increments). Valid in CW mode only.
Local Control	T	Radio front panel REMOTE/LOCAL switch must be in the REMOTE position. Puts the R-2307 in the local mode. Front panel REM annunciator extinguishes.
Mode	M*	Where * represent a letter indicating the mode. The letters and modes are: L = LSB F = FM U = USB E = Envelope C = CW A = AM
Offset	O±##	Where ± represents a "+" or "-" sign and ## represents the number of dB between the stored threshold level to be used for scan stop, sweep stop, or squelch opening. (±30 dB maximum limit).

Function to Set	Message Format	Description
Recall	RC##	Where ## represents the two digits of the memory channel from which to recall the stored parameters of the R-2307. Recalled data is entered immediately. The recalled channel data may be used as the starting channel for scan or sweep operations. If sweep operations are required, the recalled channel number must be an even number (see SC## and SW## below).
Remote Control	X	Radio front panel REMOTE/LOCAL switch must be in the REMOTE position. Returns the R-2307 to the remote condition.
Reset Dump	RD	Allows AGC voltage to be smoothly adjusted during remote frequency changes. Used for remote fine tuning or sweep.
Scan of memory	SC##	Where ## represents the two digits of channels the highest memory channel to be scanned. The scan starts at the memory channel most recently recalled.
Set Dump	SD	Causes AGC voltage to be dumped when remote frequency changes are sent from the interface. Used for remote scan.
Signal level	L123	Digits 1 through 3 represent the signal level at which the squelch opens, the scan stops, or the sweep stops (digit 1 = 100 dB increments, digit 2 = 10 dB increments, and digit 3 = 1 dB increments of the signal below 1 milliwatt).
Skip	SK	Sets the skip flag for scan or sweep function. - If used in normal state this command must be followed by the store command (ST##). This stores the skip flag in the preset channel designated by ##. The receiver will skip all preset channels with the skip flag set during future scan functions.

Function to Set	Message Format	Description
		- If used when the receiver is stopped on a preset channel during the scan function, the skip flag is stored in the current preset channel automatically (Store command not required). The receiver will skip all preset channels with the skip flag set during future scan functions. - If used when the receiver is stopped on a frequency during the sweep function, the skip flag is stored with the frequency in a separate memory location used for skip flags (100 maximum). A rotating buffer causes new entries to overwrite the oldest entry when the 100 limit is reached. The receiver will skip all frequencies with the skip flag set during future sweep functions.
Skip, Remove	NSK	Removes the skip flag. This command must be followed by a store command in the normal state (refer to Skip command).
SRQ Control Command	Q##	Where ## are two ASCII characters representing a hexadecimal byte between 00 and 3F to control the SRQ function activation on the bus. This byte masks (bit value = 0) or activates (bit value = 1) the appropriate function in the receiver to activate a SRQ. i.e. If the receiver faults when Bit 2 = 1, the receiver will activate the SRQ flag. All the bits are set (all bits = 1) during power up. When set, the bit positions represent the following functions: Bit 0 - When the receiver breaks squelch Bit 1 - When the receiver closes squelch Bit 2 - No fault to fault status change Bit 3 - Fault to no fault status change Bit 4 - Receiver switched from Local to Remote Bit 5 - Receiver switched from Remote to Local

Function to Set	Message Format	Description
		To define the ACSII characters, use the following table: 1ST NIBBLE: BIT NO. 5 = 2; 4 = 1 2ND NIBBLE: BIT NO. 3 = 8; 2 = 4; 1 = 2; 0 = 1 For example: If all the bits are set the 1st nibble value is 3 (2 + 1), and the 2nd nibble value is 15 (8 + 4 + 2 + 1). If the 2nd ASCII CHARACTER TOTAL has a value between 10 and 15, use the following table to determine the hexadecimal value: 10 = A, 11 = B, 12 = C, 13 = D, 14 = E, 15 = F An ASCII character is sent for each nibble, so the ASCII character sent in the above example would be: "3F".
Step	SE##	Where ## is the step size to be used to calculate the next frequency during a sweep. The digits in ## represent 100 Hz increments -- SE33 would indicate step sizes of 3.3 kHz.
Stop scan or stop sweep	SP	Stops scan or sweep operations.
Sweep of frequency	SW##	Where ## represents the two digits of the highest odd numbered memory channel from which to take the sweep stop frequency. The sweep starts at the frequency of the memory channel most recently recalled. Scans or sweeps at approximately 35 channels/Sec.

All characters are sent using ASCII code. The command sequence must be terminated by the carriage return and line feed characters. Only one command can be sent per message. The controller must wait for the R-2307 to process the command before sending further commands. The R-2307 automatically sets the NDAC and the NRFD lines high when it receives data across the bus. In normal IEEE-488 bus operation, this would indicate that the R-2307 is ready to receive more information. This, however, is not the case with the R-2307. The R-2307 sends the NDAC and NRFD signals high upon reception of data so that other operations on the bus will not be held up while the R-2307 is processing the data sent to it. Essentially, this means that the speed of bus operation is greatly enhanced because the controller does not have to wait until the unit has finished processing the data, as would be the case if normal handshake routines were used. The IEEE handshake is held off after an LF is received from the host. It is completed when the busy bit is set.

If the controller needs to send multiple commands to the R-2307, it must execute a serial poll between commands to determine the status of the R-2307. The R-2307 will return a status byte to the controller indicating its condition, that is, busy or not busy. The controller must check the status of the receiver by testing the BUSY bit (bit 3) in the serial poll response and ensure it is not set before sending another command. Refer to paragraph 4.2.4 for further information about the serial poll status byte.

The following table lists the IEEE-488 capabilities, both universal and addressed, as they are implemented in the R-2307.

Identification	Description/Capability
SH1	Source handshake, complete capability, no states omitted
AH1	Acceptor handshake, complete capability, no state omitted
T5	Basic talker, serial poll, talk only mode, will stop talking if addressed to listen, and no states omitted
L3	Basic listener, listen only mode, and will stop listening if addressed to talk
SR1	Service request, complete capability, no states omitted
RL1	Remote local, complete capability, no states omitted
PP0	Parallel poll not implemented
DC0	Device clear not implemented
DT0	Device trigger not implemented
C0	No controller functions implemented
E2	Tri-state data bus driver

4.2.3 Talk Data Sequence

When the controller commands a R-2307 to talk, the R-2307 responds with status information. The controller specifies what operating parameter the R-2307 is to return. The controller command for status information is a letter followed by "?". The following is an alphabetical list of controller status requests.

NOTE: Refer to paragraph 4.2.2 for radio response definitions.

Controller Status Req.	Radio Response	Description
A?	A*	What is the AGC hold time? (Zero, Short, Medium, Long, or Off.
B?	B±123	What is the BFO offset? (Reported as actually set, even if not used).
D?	D#	What is the scan/sweep dwell time?
F?	F1234567	What is the frequency setting?
G?	G123	What is the IF gain reduction?
I?	I±123	What is the IF shift? (Reported as actually set, even if not used).
L?	L123	What is the scan/sweep stop or squelch threshold level?
M?	M*	What is the receive mode? (AM, CW, Lower Sideband, Upper Sideband, FM, or Envelope)
O?	O±##	What is the offset threshold level?
SE?	SE12	What is the step size?
SS?	SS123	What is the signal strength?
Q?	Q##	What is the SRQ control status? (## represents a hex byte from 00 to 3F.
R?	----	What is the complete status of the receiver? (See note for response).
W?	W#	What is the IF bandwidth?

NOTE: The following represents the receiver response to the R? request:

R? Response = F1234567B±123I±123G123L123W#A*M*D#SE12SS123

Complete Status Report Sections

F1234567	B123	I123	G123	L123	W#	A*	M*	D#	SE12	SS123
Frequency	BFO	IF Shift	Gain	Thresh.	Bandwidth	AGC	Mode	Dwell	Step	Sig Str

4.2.4 Serial Poll Status Byte

Because the R-2307 automatically sets the NDAC and NRFD lines high upon receipt of commands and data, it is necessary for the controller to poll the R-2307 if it is going to send another set of commands or data to the same unit. This prevents the controller from sending data to a unit that is not actually ready to receive data even though the NRFD line is high.

The status byte (in response to a serial poll) is as follows:

Bit 7	6	5	4	3	2	1	0
FAULT	SRQ		SQUELCH	BUSY	ERROR	REMOTE SWITCH	

FAULT - R-2307 fault status. Updated when radio is given another command.
SRQ - IEEE SRQ status
SQUELCH - When high, the R-2307 has an open squelch.
BUSY - indicates the R-2307 is busy and not ready for another command.
REMOTE SWITCH - When high, Remote/Local switch in REMOTE position.

When the R-2307 is configured as a talker and a listener and the SRQ function is enabled, it sets the SRQ line true any time the conditions enabled by the "Q" command are true.

4.2.5 Talk Only Mode

When the unit is set to be a talker only, by means of the rear panel selector switch, it will send a complete status report message any time the SRQ status is set. Only one device on the bus may be a talker only. The talk only function is useful when an unaddressed printer is connected to the bus and is used for logging frequencies where activity is sensed. The talk only mode can not be used if there is a controller on the bus as a command conflict will result.

4.2.6 Listen Only Mode

When the unit is set to be a listener only, by means of the rear panel selector switch, the unit will respond to all messages sent on the bus regardless of address. The receiver will talk only if specifically addressed. When addressed to talk, the receiver can send status information on the bus.

4.3 REMOTE OPERATION USING PARALLEL BUS

If the optional parallel bus module, bus connector board and appropriate CPU software is installed, the receiver may be operated under remote control using the parallel bus and a suitable bus controller. To operate in this manner, set the front panel LOCAL/REMOTE switch to the REMOTE position. If the controller takes control, the REM annunciator on the display panel will be lighted. Note that the front panel LOCAL/REMOTE switch has positive control over the remote control function.

Remote operation using the parallel bus is similar to operation using the IEEE-488 bus except that certain parameters are not commanded on the parallel bus. It is not possible, for example, to program the receiver to scan or sweep automatically using internal parameters. All scan or sweep operations must be performed directly using the system controller.

Likewise, it is not possible to store or recall any channel information using the parallel bus. In addition, threshold level for squelch break is not settable using the parallel bus. Whenever remote operation is called for, the receiver squelch is set open and the audio output line is active at all times.

When receiving signals using the product detector, the BFO offset must be adjusted to accommodate the type of signal being received. For normal single sideband voice, the normal bandwidth would be 2 or 4 kHz with a BFO offset of 1.4 or 2.3 kHz respectively.

When reading signal strength via the parallel bus, care should be taken to insure that the data is valid by comparing two successive readings. As the processor in the CPU module is not synchronized with the bus operations, the data placed in the bus buffer may occasionally be changed during a read cycle. This may result in an incorrect value being read on the bus during this cycle.

5.0 OPERATIONAL MAINTENANCE

Operational maintenance procedures are limited to occasional cleaning of the unit when required, isolation of faulty modules when the faults occur, and replacement of the faulty modules by complete module replacement. No internal adjustments or component replacement is to be performed at the operational level -- these functions are performed by an authorized repair depot.

5.1 FAULT ISOLATION

When operating the receiver from the front panel, the operator should be alert to potential fault conditions that would prevent the unit from operating normally. Many types of faults will cause the FAULT annunciator to be illuminated but other types of faults will not cause the fault condition to be sensed internally. A serious lack of sensitivity or low noise level should be suspected to be due to a non-sensed fault condition.

When operating the receiver from the remote control bus, the bus controller should monitor the fault condition on the bus. If this condition is observed to be set true (that is to the fault condition), the receiver can be assumed to be inoperative. If the receiver is set to receive a known test signal and no output is detected, the receiver can also be assumed to be inoperative. In the former case, the fault detectors within the various modules and the fault indicating light emitting diodes (LEDs) on the top surface of the modules can be used to isolate the fault to the failed module. If the receiver is inoperative and the fault condition is not indicated on the bus or by the module indicators, external test equipment can be used to isolate the failed module. Of course, suspected modules can be simply replaced one at a time with known good modules until the failed module is located.

Many cases of suspected fault are simply the failure of the AC power to the unit. However, this can be discovered relatively easily. Insure that the front panel circuit breakers are in the ON position and that the displays on the front panel are illuminated. If the displays are not illuminated, insure that AC power is available to the rear panel power connector.

One possibility that should never be overlooked in the event of an indicated fault is that the external frequency reference (if used) may be inoperative or that the rear panel reference selector switch may be in the wrong position. Try placing the reference selector in the INT position and examining the status of the unit over the bus again.

If a fault is suspected, remove the top cover from the unit by turning all 1/4 turn captive fasteners counter-clockwise and lifting off the cover. Use a #2 Phillips screwdriver in good condition and press down on the handle of the screwdriver to insure good contact with the fastener head to avoid damage either to the fastener or to the screwdriver.

Insure that power is applied to the unit and that the unit is set to a valid frequency within its range and that all other parameters are set to normal values. If no response is obtained from the unit and it has been determined that AC power is available, the Panel Interface or CPU modules may be suspected. If either one of these modules have failed, no response will be obtained.

Several modules contain fault detectors and indicators. Note that not all modules have fault LEDs installed. Only those modules that generate or use internally generated signals are tested for faults and display the fault condition. The modules with fault detectors are: Power Supply, 1st IF, Detector, Output Loop, Step Loop, Fine Loop, BFO, and Reference.

In the event of a fault indication, inspect the LEDs on the tops of the modules and determine if one or more are illuminated. Note that modules for two separate receivers are in the one chassis assembly. The fault isolation tables presented herein are also summarized by the tables inside the top cover of the receiver.

If only one fault indicator is illuminated, go to section 5.1.1. If more than one fault indicator is illuminated, go to section 5.1.2. If no fault indicators are illuminated and a suitable signal generator, oscilloscope, and other test equipment is available, go to section 5.1.3.

5.1.1 One Fault Indicator Illuminated

If only one of the fault indicators is illuminated, a good assumption is that the failure is within the indicated module. In the event of a failure in the wiring or in the output circuitry of another module, the other module listed below should also be investigated for possible failure. The following tables identify the possible failure modes.

LIGHT ON	FAILURE MODE
Power Supple Module	Low voltage from power supply
1st IF Module	Loss of 1st or 2nd Local Oscillator signal
Detector Module	Loss of BFO Signal
Output Loop Module	Loss of phase lock
Step Loop Module	Loss of phase lock
Fine Loop Module	Loss of phase lock
BFO Module	Loss of phase lock

LIGHT ON	OTHER MODULES WITH POSSIBLE FAILURES
1st IF Module	Output Loop Module, Reference and 2nd LO Module
Detector Module	BFO Module
Output Loop Module	Step Loop Module, Fine Loop Module, Reference Module
Step Loop Module	Reference Module
Fine Loop Module	Reference Module

5.1.2 Multiple Fault Indicators Illuminated

If multiple fault indicators are illuminated, finding the failed module is obviously more complicated. A simple process of reasoning should identify the most likely source of the problem. The power supply is obviously involved with all modules but other sources of multiple faults may not be so obvious. The following table may serve to help find the one failed module.

LIGHTS ON	SUSPECT MODULE
1st IF and Output Loop Modules only	Output Loop Module
1st IF and Reference Modules only	Reference Module (2nd LO)
Output Loop and Step Loop Modules only	Step Loop Module
Output Loop and Fine Loop Modules only	Fine Loop Module
Reference and Fine, Step, or BFO Modules	Reference Module or external ref.
Detector and BFO Modules only	BFO Module
Fine, Step, and Output Loop Modules	Reference Module or external ref.

5.1.3 No Fault Indicators Illuminated

If no fault indicators are illuminated and the unit still does not operate correctly, the trouble most likely lies within one of the modules without fault detectors. This generally will be within of the modules in the received RF path; namely the Preselector, 1st IF, 2nd IF, or Detector modules. A complete failure of the receiver at all frequencies, bandwidths, and modes could be caused by a failure in any of the above modules. Certain types of partial failures, however, can be attributed to specific modules by following the following diagnostic table.

SYMPTOMS OF FAILURE	SUSPECT MODULE
No Display	Power Supply Module Display Board Panel Interface
No Function at all	CPU Module
Inoperative on one band only (reference section 2.1.4)	Preselector Module
Inoperative on one bandwidth only	2nd IF Module
Inoperative on one detector mode only	Detector Module

In the event that the suspect module cannot be isolated by the above table, certain rear panel monitor connections can be used to locate the possible problem. The minimum test equipment required will be an RF signal generator covering at least part of the frequency range to 30 MHz and an oscilloscope or other signal monitoring instrument having usable response to at least 40 MHz.

The following text describes one possible procedure to follow in order to isolate faults not resulting in fault light operation. A table summarizing these tests is presented on the bottom of this page.

Set the receiver to 0.0000 MHz and observe the output signal at the 1st IF monitor jack with the Oscilloscope. This signal should be 40.455 MHz with a level of approximately 300 millivolts peak-to-peak. This observation will confirm the operation of the 1st LO portions of the frequency synthesizer (Step, Fine, and Output Loop modules) and will confirm the operation of the 1st LO driver and 1st IF monitor amplifiers in the 1st IF module.

Set the receiver to any convenient frequency above 10 MHz using the remote control bus. The output level on the Oscilloscope connected to the 1st IF Monitor jack should be less than 50 millivolts peak to peak.

Apply a signal at a level of -10 dBm (0.07 volts RMS into 50 Ohms) to the Antenna connector of the receiver section being tested at that frequency set above. The output level on the Oscilloscope connected to the 1st IF Monitor jack should be approximately 250 millivolts peak-to-peak. If it is, the gain through the preselector module and the 1st mixer section of the 1st IF module is probably satisfactory. If this observation is not made, suspect the Preselector or 1st IF modules and replace one or both of them.

If the signal observation made just above is verified to be approximately 250 millivolts peak-to-peak, connect the Oscilloscope to the 2nd IF monitor connector. Insure that the receiver AGC is turned on and that 0 dB gain reduction is programmed into the receiver. Reduce the amplitude of the signal applied to the Antenna connector towards -100 dBm. The signal on the Oscilloscope should be approximately 600 millivolts peak-to-peak over the entire range at a frequency of 455 kHz. If it is not, suspect the 1st IF, 2nd IF, or detector modules and replace them.

NO FAULT LEDS INDICATING; ALL BANDS, BANDWIDTHS, AND DETECTORS INOPERATIVE

VERIFY AC POWER AVAILABLE AND FRONT PANEL LIGHT ILLUMINATED _____

VERIFY REFERENCE SELECTOR IN INTERNAL POSITION _____

VERIFY BUS INTERFACE AND CPU MODULES OPERATIONAL _____

TESTS USING SIGNAL GENERATOR AND OSCILLOSCOPE:

FREQUENCY	SIGNAL	TEST POINT	VALID OBSERVATION	SUSPECT IF NOT VALID
0.000	NONE	1st IF MON	300 mv p-p, 40.455 MHz	1st IF Module
10 MHz	NONE	1st IF MON	50 mv p-p, 50.455 MHz	1st IF Module
10 MHz	-10 dBm	1st IF MON	250 mv p-p, 40.455 MHz	Preselector, 1st IF
10 MHz	-10 dBm	2nd IF MON	600 mv p-p, 455 kHz	1st IF, 2nd IF, Det.
10 MHz	-100dBm	2nd IF MON	600 mv p-p, 455 kHz	Detector Module

5.2 MODULE REPLACEMENT

The procedure for replacement of any of the shielded modules is very easy but care should be taken to avoid damaging any of the connectors or fasteners.

CAUTION

Switch OFF the power to the unit before removing or replacing a module.

When a suspected failed module is located, loosen the 1/4 turn captive fasteners located at the base of the module by using a #2 Phillips screwdriver in good condition. Press down firmly on the screwdriver handle and turn the fastener 1/4 turn counter-clockwise. The fastener should be observed to pop free and rise slightly. Using a module extraction tool or a pair of flat bladed screwdrivers, pry up gently on the top ears of the module to release the module from the connectors and lift the module free of the assembly.

Replacement of a module is the reverse of the above procedure, taking great care to avoid damaging the connectors when reinstalling the module. Insure that the module is correctly located in the chassis and oriented to the front of the unit and that the connectors on the bottom of the module and the connectors on the chassis assembly are aligned. The module position in the chassis is indicated on the outline and mounting drawing and the diagonal stripe on the top of the module also serves to indicate the correct module position. The stripe should form a continuous line from front to rear in the chassis with no noticeable offset.

Note that all connectors have a D shape. Be sure that the wide sides of the D are aligned on both connectors. On the modules with both a coaxial cable connector and an ordinary wire connector, the connector without the coaxial cables should be mated first. When both connectors are aligned, press the module firmly down to seat the connectors. Using the #2 Phillips screwdriver again and pressing firmly down, turn the captive fasteners clockwise 1/4 turn until they are locked into position.

When all modules have been replaced and the unit is restored to an operating condition, replace the top cover. Using the #2 Phillips screwdriver and pressing firmly down, turn the captive fasteners clockwise 1/4 turn until they are locked into position.

5.3 REPLACEABLE MODULES

The following list of modules, boards, and components constitute the repair parts available at the operational maintainence level. Board level components are normally replaced only at the depot maintainence level and are not listed in this manual. Part numbers listed for modules, boards, and components are assigned by the manufacturer, Cubic Communications Inc.

Description	Number	Remarks
Power Supply Module	2140-1124	
Preselector Module	2140-1101	
First IF Module	2140-1102	
Second IF Module	2140-1103	Standard Filters
Detector Module	2140-1104	
Step Loop Module	2140-1106	
Output Loop Module	2140-1105	
Fine Loop Module	2140-1107	
BFO Module	2140-1109	
Reference and 2nd LO Module	2140-1146	1 MHz External Reference (Opticnal)
Reference and 2nd LO Module	2140-1135	10 MHz External Reference (Standard)
CPU Module less Program	2140-1110	Program Memory required per options
Panel Interface Module	2140-1116	
Parallel Bus Interface Mod.	2140-1111	Optional, standard on S.N. below A126
Parallel Bus Connector Plate	2143-1112	Optional, new design (ESSI)
IEEE-488 Bus Interface Mod.	2140-1112	Standard starting with S.N. A126
IEEE-488 Bus Connector Plate	2142-1107	Standard starting with S.N. A126

Note: The program memory chip to be installed in the CPU module must be specified for the installed receiver configuration. The parallel bus and IEEE-488 bus require a different program memory chip as does any non-standard filter configurations. If an older version program memory chip is being replaced, the program number and revision letter must be specified. Otherwise, the current version program memory chip will be supplied by the manufacturer. These numbers can be found on labels applied to the program chip as well as the CPU module housing.

Front Panel Assembly	2143-1102	Complete with display and audio boards
Display Board	2140-2016	
Audio Board	2140-2019	
Keypad	2140-4301	
Keypad Overlay	180-004	New design starting with S.N. A126
Display Filter	2142-1506	
Large Knob	211-095	
Small Knob	211-096	
Circuit Breaker Assembly	2143-1107	
Shaft Encoder Assembly	2140-1122	
Phone Jack	342-040	
Potentiometer (Volume)	052-197	
Toggle Switch (Remote)	172-081	
Hour Meter Assembly	2140-1119	

Connectors, wire harnesses, motherboards, and other items are also replaceable at the operational level. Consult the provisioning parts list for details.

6.0 THEORY OF OPERATION

This section outlines the general theory of operation of the receiver. The specific operation of the various circuit boards and modules is presented in section 7 of this manual. Refer to the Block Diagram in Figure 6-1 for the modules and circuits discussed in this section.

6.1 RECEIVER SECTION

For the purposes of this discussion, the receiver section consists of those modules that process the incoming signal. The synthesizer and control sections are separately discussed. The modules in the receiver section are the Preselector, 1st IF, 2nd IF, and Detector modules plus the audio board.

6.1.1 Preselector Module

The incoming signal is applied through the rear panel RF connector to the Preselector Module. If power is applied to the unit and if the RF signal level is below approximately 1 watt, the signal is applied to the half-octave filter section through a protective relay. The RF detector will sense excess RF power and open the relay to protect the filters if required. The module is also protected by a gas tube transient suppressor that will conduct in the presence of very high voltage transients, such as those caused by static electrical discharge, as well as an initial high level signal pulse occuring before the protection relay has had a chance to open.

The half-octave bandpass filters serve to exclude out-of-band energy that could result in receiver spurious responses and also serve to reduce the local oscillator signal that may be conducted from the mixer in the 1st IF module. The filters operating above 1.6 MHz are PIN diode switched while the filters for the lower frequencies are relay switched. Relay switching is used for the lower frequencies as PIN diodes have excess distortion at low frequencies. PIN diodes are used at the higher frequencies to minimize switching time while changing frequencies and also for long term reliability reasons.

The preselector module also includes a low noise, high dynamic range, grounded gate FET amplifier. This amplifier serves to compensate for the loss in the preselector filters and the 1st mixer and thus preserve a low noise figure but it's gain is held to a low value in order to hold the signals applied to other circuits in the receiver to a minimum level and thus insure maximum dynamic range consistant with the required noise figure. The amplifier is switched out of the circuit when frequencies below 1.6 MHz are selected as it is not needed in these frequencies and the compromises required to operate in the lower frequencies would degrade the performance in the most needed 1.6 to 30 MHz range.

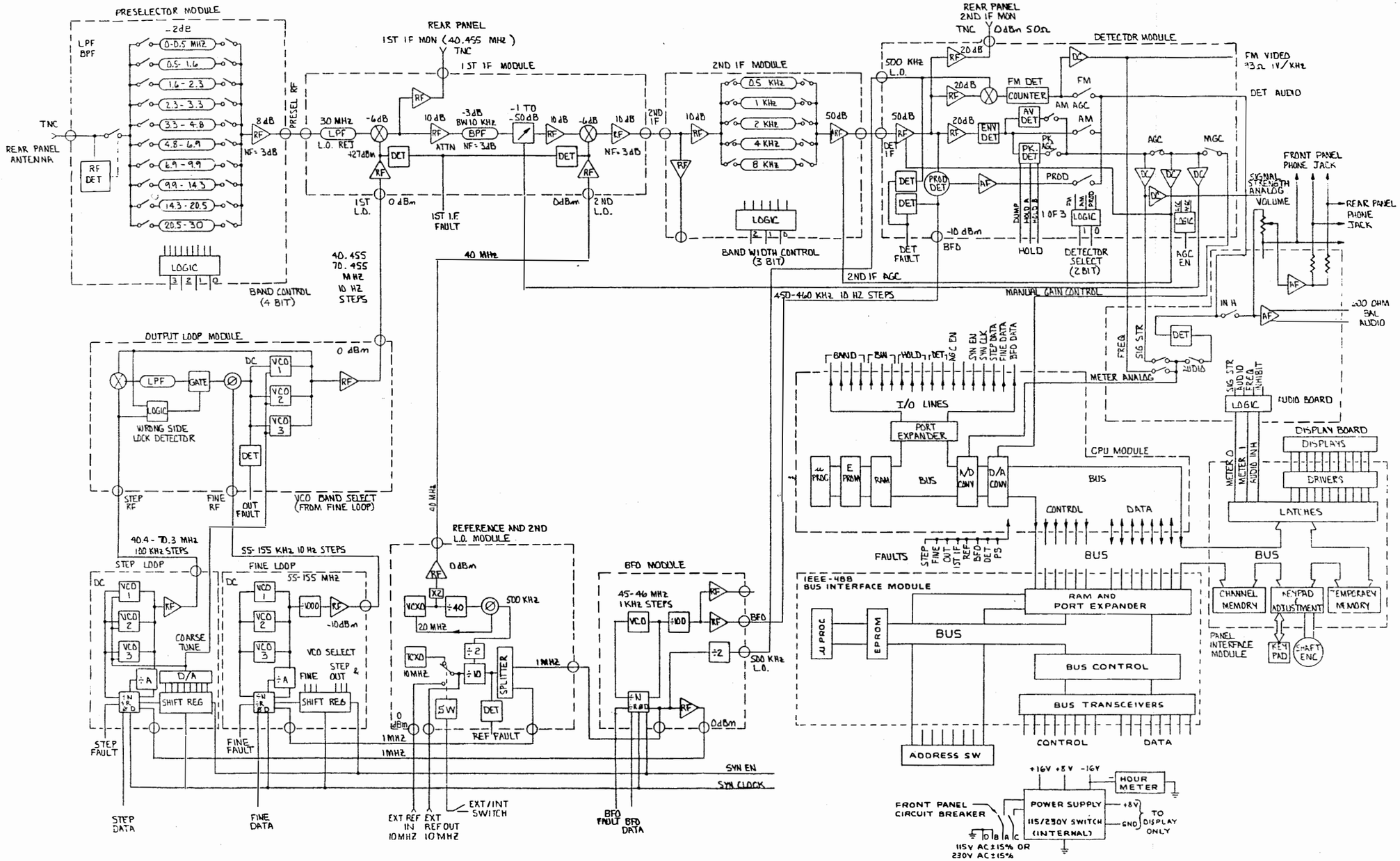


FIGURE 6-1
BLOCK DIAGRAM

6.1.2 1st IF Module

The signal applied to the 1st IF module is filtered through a 30 MHz low pass filter designed to reject the local oscillator signal and prevent it from being radiated from the antenna as well as rejecting signals at the 1st IF frequency of 40.455 MHz from being impressed on the receiver.

The 1st IF module converts the input signal to the 1st intermediate frequency centered on 40.455 MHz in the first mixer. This is a very high level double-balanced diode mixer operating with +27 dBm (1/2 watt) of local oscillator signal. The output of this mixer is amplified with a grounded gate FET amplifier designed to terminate the mixer at all signal frequencies and to present a low noise figure with moderate gain.

A signal is output from the 1st IF module after the mixer but before the filter for test purposes or for analysis by other equipment.

The 1st IF filter serves to exclude signals outside a nominal 10 kHz bandwidth from the remainder of the receiver -- particularly the 2nd mixer.

The output from the 1st IF filter is attenuated (when required by signal level) by a PIN diode attenuator and amplified in another grounded gate FET amplifier exhibiting low noise figure and moderate gain. The PIN diode attenuator is only used to reduce the signal level when input signals greater than approximately -80 dBm are applied to the unit.

The second mixer converts the signal at the 1st intermediate frequency (40.455 MHz) to the second intermediate frequency (455 kHz) by mixing it with the 2nd LO signal at 40.000 MHz. This mixer is also followed by a grounded gate FET amplifier serving to terminate the mixer in a 50 Ohm load while exhibiting a low noise figure and moderate gain.

6.1.3 2nd IF Module

The 2nd IF module contains the 5 selectable bandwidth IF filters (ranging from 0.5 to 8.0 kHz) and the first stage of significant gain. The amplifier stage before the filters has only moderate gain and serves mainly to isolate the filters from the input port. The amplifier stage after the filter has approximately 50 dB of signal gain and can be controlled in gain over a 50 dB range.

6.1.4 Detector Module

The detector module is used to demodulate the signal in the manner selected and to derive the signals used for automatic gain control and signal detection. The signal input to this module is first amplified by an amplifier having a maximum gain of approximately 50 dB.

Amplitude modulated and pulse type signals are demodulated in the envelope detector. The output from this detector is itself peak detected and used for AGC and metering purposes. An averaging circuit is used to derive the AGC signal when receiving amplitude modulated signals with the AM mode selected.

Suppressed and reduced carrier signals are demodulated in the product detector. This circuit mixes the incoming signal with the BFO signal and the resulting difference signal is the desired demodulated signal.

Frequency modulated signals are demodulated in the FM detector. This circuit mixes the 2nd IF signal at approximately 455 kHz with another signal from the BFO module (in the synthesizer section) at 500 kHz. The resulting signal at approximately 45 kHz is applied to a pulse count type discriminator for demodulation. This type of discriminator is used because of its superior linearity as compared to other types and the signal is converted to a lower frequency before demodulation to optimize the stability and gain of the discriminator.

The output from the FM detector is used in two ways. When the FM mode is selected, its AC coupled output is applied to the audio circuit. At all times, its DC coupled output signal is applied to the FM video line for monitoring by external equipment. In addition, the FM video signal can be monitored by the CPU module (in the computer section) for metering purposes.

The AGC circuit is a hold or hang type circuit with selectable hold time constants. This type of AGC circuit has the characteristic of holding the IF gain constant for a period of time after the signal is sensed to be removed instead of immediately increasing the gain. When receiving voice type signals, this characteristic has the effect of eliminating the noise increase between syllables and can thus considerably improve the apparent signal to noise ratio on this type of signal. When used on signals exhibiting rapid fading, the shorter hold times can be selected.

The gain control voltage from the CPU module is applied to this module in order to achieve manual or remote gain control. When this mode is selected, the automatic gain control circuits are disconnected. In this mode, the output of the peak detector is monitored and manual or remote gain control is used to control the signal amplitude in the middle of the detector's output range. Only a few dB of manual gain control is required to control the signal amplitude over the entire useful range of this detector.

6.1.5 Audio Board

The Audio board contains the 600 Ohm balanced line transformer, the headphone amplifier, and the analog select switch for metering purposes. The detector for the audio level meter function is also contained on this board. The Audio board is mounted directly behind the Display board in the front panel area.

6.2 SYNTHESIZER SECTION

The synthesizer section is used to derive the various signals used for signal conversion and demodulation. The modules in the synthesizer section are the Output Loop, Step Loop, Fine Loop, Reference, and BFO modules.

6.2.1 Output Loop Module

The Output Loop module provides the 1st LO signal to the 1st mixer (in the 1st IF module) by phase locking a voltage controlled oscillator to the sum of the Step and Fine Loop module frequencies. This module contains three voltage controlled oscillators (VCOs) operating over the range of 40.455 to 70.455 MHz, a mixer taking the difference between the Step Loop and Output Loop signals, and a phase detector operating on the output signal from the mixer and the Fine Loop signal. Logic circuits are included to insure that the Output Loop locks only to the sum of the Step and Fine Loop signals and not to the difference frequency.

6.2.2 Step Loop Module

The step loop operates over the range of 40.400 to 70.400 MHz in 100 kHz steps by phase locking a VCO to a reference frequency of 100 kHz. This module contains three VCOs to cover the range and a complex integrated circuit that serves to vary the number by which the VCO frequency is divided (divide by N). This IC also contains a divider for the 1 MHz reference signal (divide by R) and the required phase detector as well as the control for the two modulus frequency divider (divide by A). A shift register is used to capture serial data from the CPU module (also used to program the variable dividers) in order to provide coarse tuning voltages to the Step and Output Loop modules.

6.2.3 Fine Loop Module

The Fine Loop module provides a signal to the Output Loop module in the range of 55 to 155 kHz in 10 Hz steps. It does this by dividing the output of one of three VCOs operating from 55 to 155 MHz by a factor of 1000. This technique allows for a VCO reference frequency of 10 KHZ (thus allowing for rapid phase lock loop acquisition) with an output step size of 10 Hz. The division by 1000 also substantially improves the spectral purity and frequency jitter of the output signal. The same complex IC as used in the Step Loop is used here and the shift register is used to select the VCO in use in all three synthesizer loop modules.

6.2.4 Reference Module

The Reference module provides the stable 1 MHz signal required by all synthesizer modules. This module can use the internal temperature compensated crystal oscillator (TCXO) or can use the externally supplied reference signal. The standard design for this receiver uses an external 10 MHz reference frequency. On special order, a reference module using an external frequency of 1 MHz can be obtained.

The Reference module also provides the 2nd LO signal at 40 MHz by using a voltage controlled crystal oscillator (VCXO) operating at 20 MHz and comparing 1/40 of this signal frequency with 1/2 of the 1 MHz reference frequency (500 kHz). The second harmonic of the VCXO at 40 MHz is used for the 2nd LO signal. Operation in this manner insures adequate pull range in the VCXO under all conditions of crystal tolerance and temperature.

6.2.5 BFO Module

The BFO module provides a signal in the range of 445 to 465 kHz in 10 Hz steps to the product detector in the Detector module. It does this by dividing the output of one VCO in the range of 44.5 to 46.5 MHz by a factor of 100. The reference frequency for the VCO is 1 kHz so the output step size is then 10 Hz. The same type of complex IC used in the Step and Fine Loop modules is used in this module. The 500 kHz signal required by the Detector module is supplied by dividing the 1 MHz reference signal by a factor of 2.

6.3 CONTROL SECTION

The control section of the receiver is that section that performs all of the control functions including interface to the remote control bus, synthesizer data, receiver band and bandwidth, AGC and detector select, and all front panel controls and displays. The modules in the control section are CPU, Panel Interface, Bus Interface, and the Display board.

6.3.1 CPU Module

The CPU module contains the microprocessor with its associated program memory, a small amount of random access memory used for temporary registers and calculations, the analog to digital (A/D) converter used for the metering functions, the digital to analog (D/A) converter for providing remote or manual gain control, and port drivers to provide serial data to the synthesizer modules as well as parallel outputs to the receiver modules. All functions of the receiver are under the control of the program memory contained within the CPU module.

6.3.2 Panel Interface Module

The panel interface module contains the output ports to operate the displays, the input ports to sense the keypad and adjustment knob operations, the channel memory to store up to 100 channels of frequency and other information, and the temporary memory to store the frequency and other parameters upon loss of power and to restore the receiver to its last condition upon restoration of power.

The channel memory and the temporary memory both use non-volatile mode storage techniques that do not require a battery or other source of power to retain the information. The storage life for this information is essentially unlimited but the components have a write cycle limitation of several 10s of thousands of cycles. It can be expected that these components may have to be replaced after several years of operation -- particularly if the power is repeatably cycled. For this reason, these components are placed in sockets.

6.3.3 IEEE-488 Bus Interface Module

The IEEE-488 Bus interface module contains its own microprocessor and program memory to interface with the control bus plus a set of output ports that are read by the microprocessor in the CPU module as memory locations. The IEEE-488 Bus Interface module handles all handshaking on the bus without disturbing the operation of the CPU.

6.3.4 Parallel Bus Interface Module

The Parallel Bus Interface module is composed of a number of data latches used as storage registers that are triggered to capture the data when the select code applied to the bus matches the select code set into the unit by the internal jumper plugs. The bus latches the data at a rate determined only by the bus and is independent of any operation in the CPU module. The CPU reads the contents of these registers as memory locations on its own timing cycle and uses this data to control the frequency synthesizer and other receiver functions.

6.3.5 Display Board

The Display board contains all of the LED display elements plus the digit select and segment select drivers. The display is organized as 3 groups of 6 digits having 8 segments each. Normal intensity digits are turned on for 2 milliseconds every 16 milliseconds (a refresh rate of 62.5 Hz) while the intensified digit (when enabled) is turned on for 6 milliseconds every 16 milliseconds. Current switching transistors and current limiting resistors are located on the rear side of this board.

This board also contains connectors for interface of the keypad signals to the motherboard. No function is performed on these signals except for the connection to the motherboard.

7.0 DETAILED CIRCUIT DESCRIPTION

This section of the manual describes the functions of the various components and circuits of the circuit boards and shielded module assemblies. Detailed fault isolation and correction instructions are not included as these functions are usually performed at the authorized repair depot. Complete component assembly location drawings and schematic diagrams are included for each module or circuit board as are parts lists organized by schematic component designator. The part number listed in the parts lists is that assigned by the receiver manufacturer, Cubic Communications, Inc. The manufacturer's name and part number listed is that of one possible manufacturer of the part -- others may be found on the circuit boards.

The distinction between circuit boards and modules in this section is simply that circuit boards that are mounted in the completely shielded enclosures are referred to as modules and that circuit boards that are mounted in some other way are referred to simply as boards.

Each individual module or board is described in an individual section of this manual. Each section is individually numbered. The module names and sections are as given below:

Refer to the receiver interconnect diagram shown in Figure 7-1 for the coaxial cable and motherboard connections. Refer also to the rear panel interconnection diagram in Figure 7-2 and the motherboard schematic in Figure 7-3 together with the motherboard signal list in Table 7-1.

In most cases, no component replacement or adjustments will be performed at any location other than an authorized repair depot. Should any adjustments be required, an appropriate extender module will be required. Different modules may require different extender modules. For reference only, the following extender module types are available.

5 Coax, 1-25 pin	2 High Voltage, 1-25 Pin	2-25 Pin
Preselector	Power Supply	CPU
1st IF		IEEE-488 Bus Interface
2nd IF		Parallel Bus Interface
Detector		
Output Loop		
Step Loop		2-37 Pin
Fine Loop		
Reference		Panel Interface
BFO		

7.1 PRESELECTOR MODULE

The Preselector module performs the task of filtering the input signal through a set of bandpass filters having a bandwidth of approximately one-half octave and providing amplification to compensate for the losses in these filters.

Refer to the component assembly drawing and the schematic diagram for this module in Figures 7.1-1 and 7.1-2 respectively.

The incoming RF signal from the rear panel connector is applied to the module to the coaxial connector in position 1 of P1 on the Preselector Module. Protective relay K1 is initially open when the receiver is turned off but is energized (closed) when the receiver is powered up by the current applied to the base of Q2 through resistor R21. In the event of RF signal levels in excess of approximately 1 watt, the voltage divider of R19 and R20 will apply the signal to diode CR12 which conducts, turning Q1 on. This turns Q2 off and opens the relay, thus protecting the circuitry in the module from excess power. The module is also protected by a gas tube transient suppressor, E1, that will conduct in the presence of very high voltage transients, such as those caused by static electrical discharge, as well as initially high level signal pulses occuring before the protective relay has had a chance to open.

C93 couples the RF signal to one of the 8 bandpass filters above 1.6 MHz or one of the 2 low pass filters below 1.6 MHz. Taking, for example, the bandpass filter for the highest frequency band, 20.5 to 30 MHz, PIN diodes CR1 and CR2 are turned on -- all other diodes are turned off by means of the voltage developed across R1 and R6 respectively. The signal is transformed to a higher impedance by C1 and C2, resonated by L4, and coupled via resonant circuit L3 and C83 to L5, and transformed down to the nominal impedance by C3 and C4. The other bandpass filters are similar while the filters operating below 1.6 MHz are conventional low pass filters.

The half-octave bandpass filters serve to exclude out-of-band energy that could result in receiver spurious responses and also serve to reduce the local oscillator signal that may be conducted from the mixer in the 1st IF module. The filters operating above 1.6 MHz are PIN diode switched while the filters for the lower frequencies are relay switched. Relay switching is used for the lower frequencies as PIN diodes have excess distortion at low frequencies.

BDC to decimal decoder U3 selects the proper filter through line driver U2 for the bandpass filters, or Q3 and Q4 for the lowpass filters. The resulting filtered RF is coupled by C67 to the input of the low-noise, high dynamic range, grounded gate FET amplifier Q5. Constant current biasing is accomplished by Q6 and associated components. The amplifier is switched out of the circuit by relays K6 and K7 (through diodes CR23 or CR24) when frequencies below 1.6 MHz are selected. The output from the module is passed through the coaxial cable connector inserted in position 5 of P2.

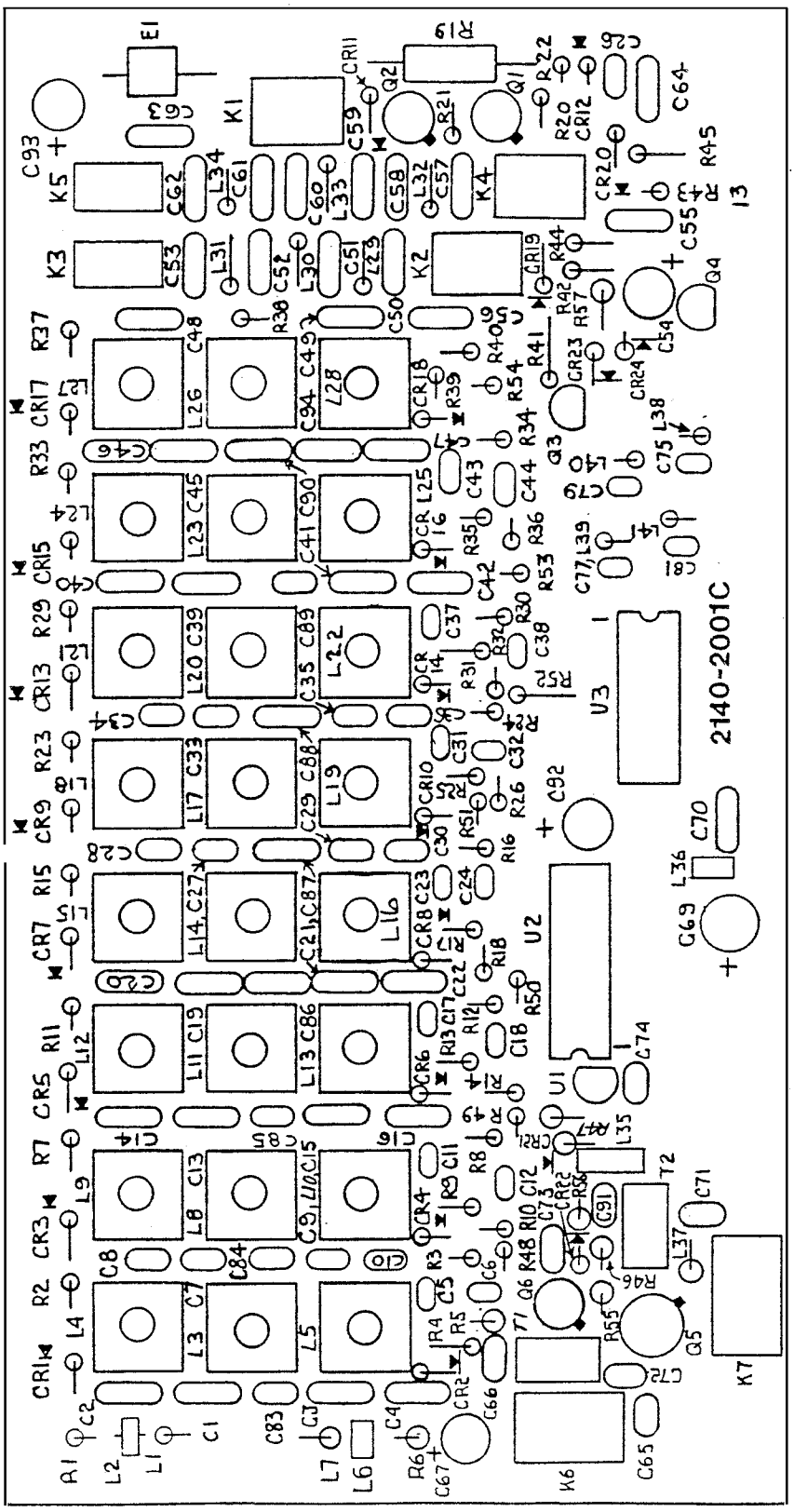


FIGURE 7.1-1
PRESELECTOR MODULE ASSEMBLY DRAWING

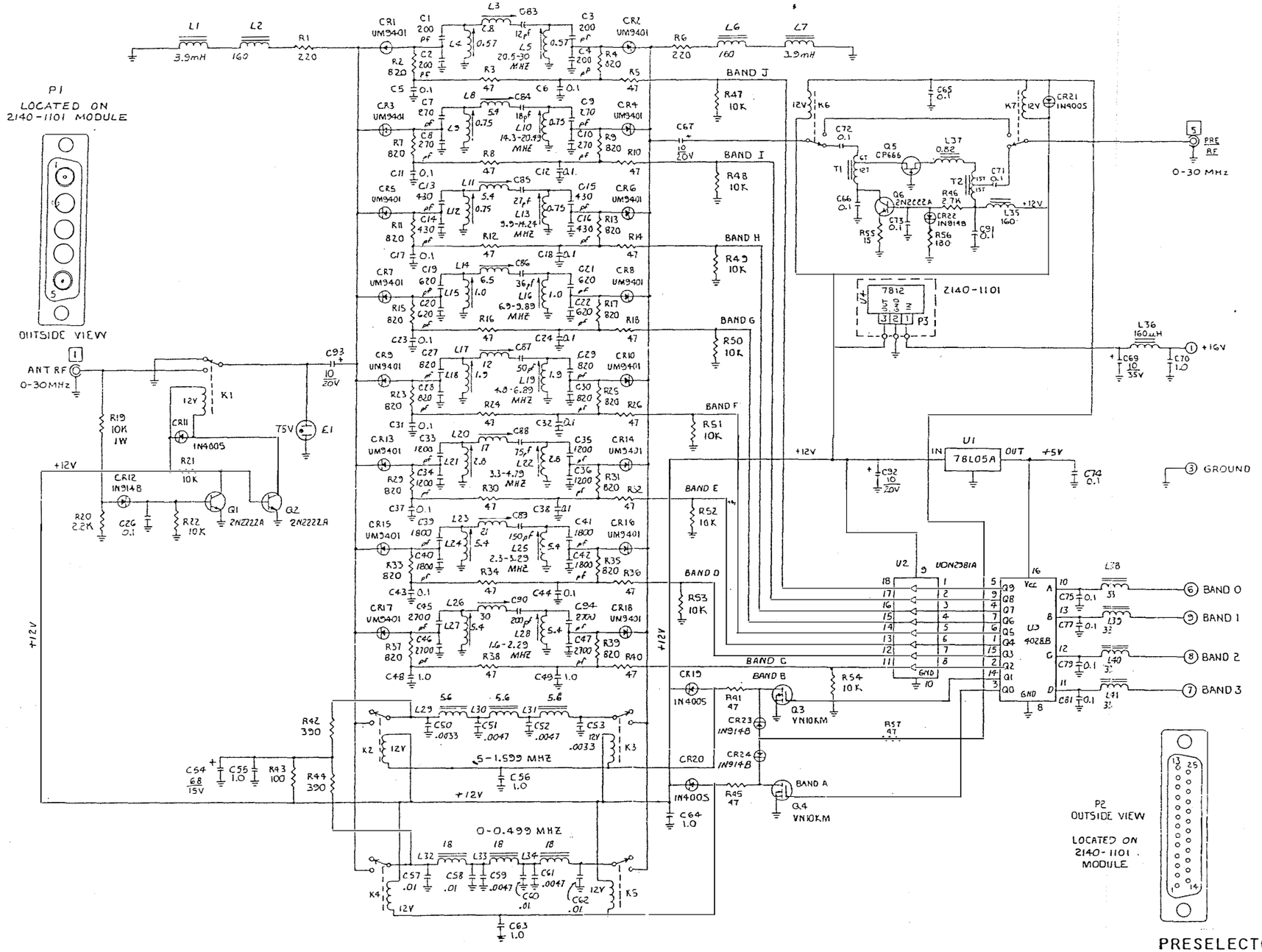


FIGURE 7.1-2
PRESELECTOR MODULE SCHEMATIC

ADJUSTMENTS: No adjustments are required in normal service. In the event of damage to any of the bandpass filters, the following adjustments may be made at the repair depot only using a suitable sweep signal generator, detector, and display device. A tracking signal generator and associated spectrum analyzer are recommended.

Apply the input signal to the rear panel RF input connector. Observe the output signal at the coaxial cable connector in position 5 of P1 in the 1st IF Module location (with the module removed from the receiver chassis).

FREQUENCY	ADJUST	ADJUSTMENT CRITERIA
25 MHz	L3,L4,L5	Maximum flat bandpass between 20.5 and 30 MHz
16 MHz	L8,L9,L10	Maximum flat bandpass between 14.3 and 20.5 MHz
12 MHz	L11,L12,L13	Maximum flat bandpass between 9.9 and 14.3 MHz
8 MHz	L14,L15,L16	Maximum flat bandpass between 6.9 and 9.9 MHz
6 MHz	L17,L18,L19	Maximum flat bandpass between 4.8 and 6.9 MHz
4 MHz	L20,L21,L22	Maximum flat bandpass between 3.3 and 4.8 MHz
3 MHz	L23,L24,L25	Maximum flat bandpass between 2.3 and 3.3 MHz
2 MHz	L26,L27,L28	Maximum flat bandpass between 1.6 and 2.3 MHz
1 MHz	None	Maximum flat bandpass between 0.5 and 1.6 MHz

CONNECTIONS:

P1, position 1 -- RF input, 0 to 30 MHz
P1, position 5 -- RF output, 0 to 30 MHz
P2, pin 1 -- + 16 VDC
P2, pin 6 -- Band select 0, 5V logic levels
P2, pin 9 -- Band select 1, 5V logic levels
P2, pin 8 -- Band select 2, 5V logic levels
P2, pin 7 -- Band select 3, 5V logic levels

The band select lines have logic signal levels as follows:

FREQUENCY	3	2	1	0
0.0-0.5 MHz	LOW	LOW	LOW	LOW
0.5-1.6 MHz	LOW	LOW	LOW	HIGH
1.6-2.3 MHz	LOW	LOW	HIGH	LOW
2.3-3.3 MHz	LOW	LOW	HIGH	HIGH
3.3-4.8 MHz	LOW	HIGH	LOW	LOW
4.8-6.9 MHz	LOW	HIGH	LOW	HIGH
6.9-9.9 MHz	LOW	HIGH	HIGH	LOW
9.9-14.3 MHz	LOW	HIGH	HIGH	HIGH
14.3-20.5 MHz	HIGH	LOW	LOW	LOW
20.5-30.0 MHz	HIGH	LOW	LOW	HIGH

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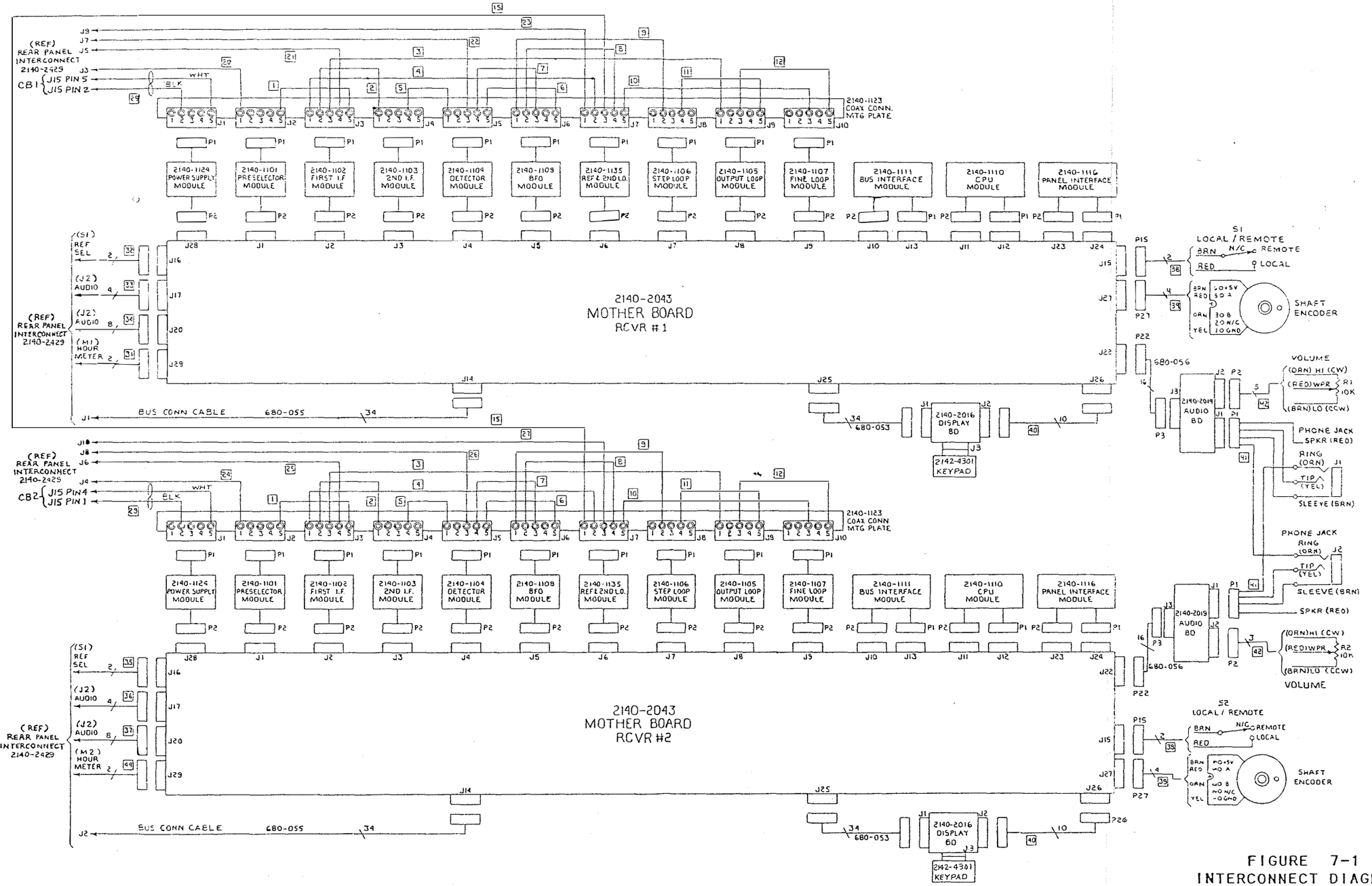

FIGURE 7-1
INTERCONNECT DIAGRAM

7.2 1st IF MODULE

The 1st IF module converts the input signal to the first intermediate frequency of 40.455 MHz, filters this signal, and converts the 1st IF signal to the second intermediate frequency of 455 kHz. The gain of this module is controlled by the automatic or manual gain control functions at the higher levels of gain reduction in excess of approximately 50 dB gain reduction. Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.2-1 and 7.2-2 respectively.

Signal from the Preselector Module is applied to the 1st IF module through the coaxial cable connector in position 5 of P1. The signal is filtered through a multisection lowpass filter having attenuation notches. This filter is comprised of inductors L1, L2, L3, and L4 and associated capacitors.

Z1 is a very high level double-balanced diode mixer, utilizing a +27 dBm (0.5 watt) 1st LO signal of 40.455 to 70.455 MHz. The input signal in the range of 0 to 30 MHz is upconverted to 40.455 MHz in this mixer. The mixer output is split at this point; one signal is used to drive amplifier Q11 and emitter-follower Q10 for external monitoring purposes, the other to drive low-noise/moderate gain, grounded gate FET amp Q2. Constant-current biasing for Q2 is provided by Q3 and associated components. The LO signal level is detected by CR7 and is used both for 1st LO power leveling and fault detection purposes.

The first IF filter F1 serves to exclude signals outside a nominal 10 kHz bandwidth from the remainder of the receiver. The filter output passes through the PIN diode attenuator formed by CR1, CR2 and CR3, before going to the second grounded gate FET amplifier Q4. The PIN diode attenuator is driven by U1A and Q1. Constant-current biasing for Q4 is provided by Q5 and associated components. PIN diode attenuation occurs only when input signal levels are greater than approximately -80 dBm or when the signal gain is reduced by more than 50 dB.

The 1st IF signal output of Q4 at 40.455 MHz is coupled by C31 to the input of the second mixer Z2. This mixer uses the +17 dBm 2nd LO signal at 40.000 MHz to produce the 2nd IF signal centered around 455 kHz. Again, a low noise, moderate gain grounded gate FET transistor (Q6) is used to terminate the mixer in a 50 ohm load. Bias for Q6 is provided by Q8, and associated components. The output signal at 455 kHz is passed through emitter follower transistor Q7 to the output coaxial cable connector in position 2 of P1.

The 1st LO signal that is applied to the first mixer Z1 at a level of +27 dBm, initially arrives on the board from the Output Loop Module at a level of 0 dBm via the coaxial cable connector in position 3 of P1. The 1st LO is amplified by Q16 to a level determined by the automatic level control network consisting of detector diode CR7, operational amplifier U2A, transistor amplifier Q15, and PIN diode CR9. LO Level control R60 sets a DC reference for U2A. Q14 drives transformer T5, the center-tapped input transformer to a push-pull Class B amplifier formed by Q12 and Q13. Output transformer T4 drives the LO port (pin 8) of the first mixer Z1. A failure in the LO signal or LO driver circuitry as detected by CR7 will result in the FAULT line being set low and the FAULT LED being illuminated.

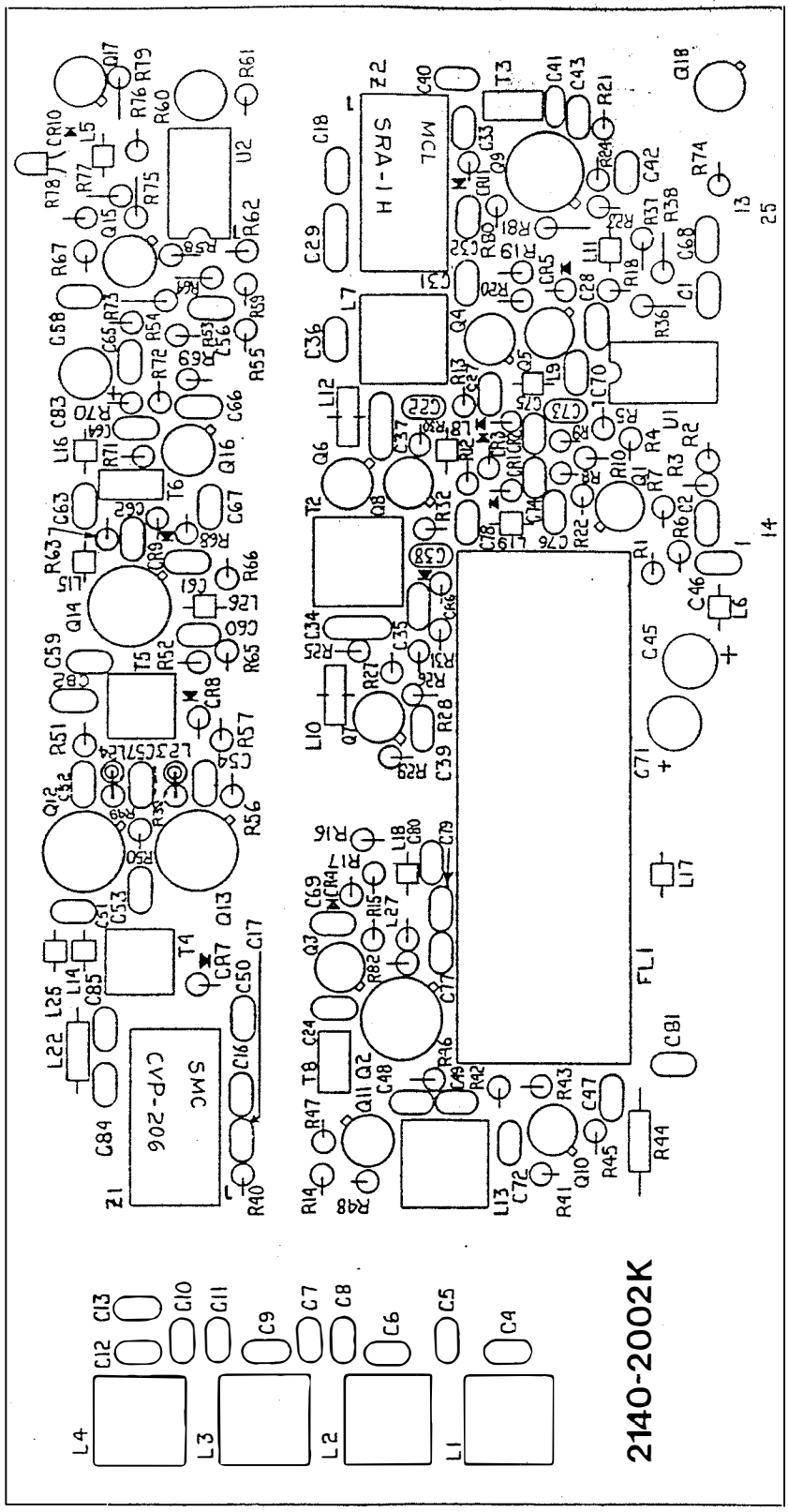

FIGURE 7.2 - 1
1st IF MODULE ASSEMBLY DRAWING

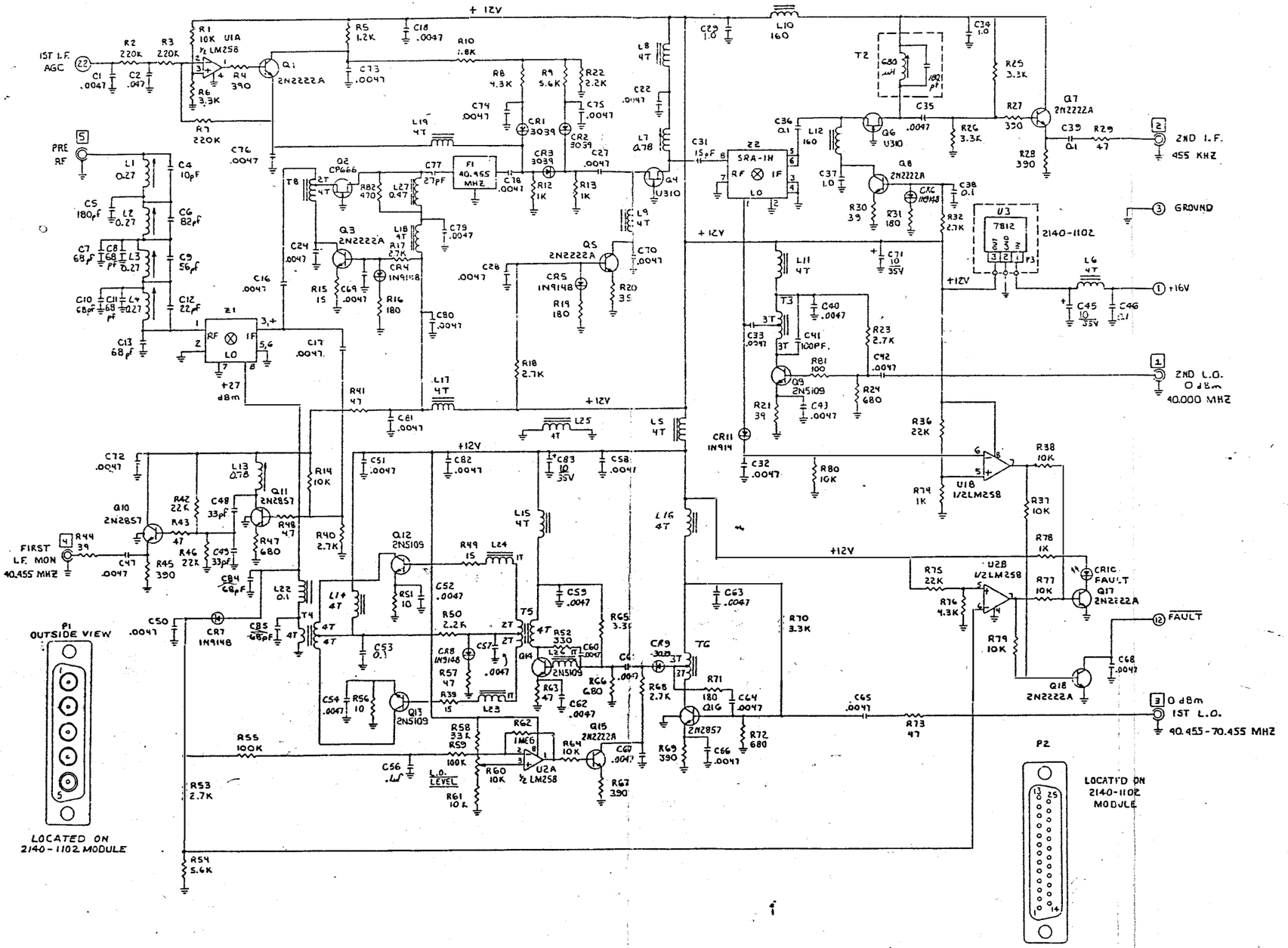

FIGURE 7.2-2
1st IF MODULE SCHEMATIC

The 2nd LO signal on the coaxial cable connector in position 1 of P1 is a 0 dBm signal at 40.000 MHz. The output of 2nd LO amplifier Q9 drives the LO port (pin 1) of the second mixer, Z2, at a level of +17 dBm. A fault detecting circuit consisting of CR11 and U1B and associated components monitor the level of the 2nd LO signal and lights the fault LED if the level drops too low in a similar manner as a fault in the 1st LO driver.

ADJUSTMENTS: No adjustments are required in normal service. In the event of damage to any of the components, the following adjustments may be made using a suitable sweep signal generator, spectrum analyzer, and oscilloscope with a 10 to 1 probe.

1st LO Level:

Before beginning the test, verify that the output from the Output Loop Module applied to the coaxial connector in location 3 of P1 in the 1st IF module is approximately 0 dBm.

Connect the oscilloscope probe to pin 8 on Z1 with the ground lead to the nearest circuit ground. Adjust potentiometer R60 on the 1st IF Module for an indicated level of 10 v p-p at all receiver frequencies from less than 1 MHz to 30 MHz. If a variation is noted over the frequency range, adjust R60 as required for minimum deviation from 10 v p-p over the frequency range.

1st IF Monitor:

Connect the spectrum analyzer to the rear panel 1st IF Monitor jack. With all receiver modules installed, set the receiver frequency to 0.0000 MHz. Adjust L13 for maximum level on the spectrum analyzer at 40.455 MHz.

2nd IF Output:

Connect the spectrum analyzer to the coaxial cable connector in position 1 of P1 in the 2nd IF module location (with the 2nd IF module removed). Set the receiver frequency to 0.000 MHz. Set the spectrum analyzer to observe 455 kHz and adjust T2 for maximum level on the spectrum analyzer.

Input Filter:

This procedure requires a preselector module modified to bypass all bandpass filters and is normally performed only at the factory. The output of a tracking signal generator is applied to the input of the specially modified preselector module and the input to a spectrum analyzer from pin 1 on mixer Z1 is applied through a 1000 ohm resistor. For more details, the factory test procedure is available.

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Adjust the spectrum analyzer controls to sweep the tracking signal generator from 0 to 50 MHz. Adjust L1, L2, L3, and L4 for a maximally flat response from 0 to 30 MHz with maximum attenuation at 40 MHz and above. The maximum attenuation in the range of 2 to 30 MHz should be not more than 2 dB below the frequency of minimum atenuation.

CONNECTIONS:

P1, position 1 -- 2nd LO input. 40.000 MHz, 0 dBm
P1, position 2 -- 2nd IF output, 455 kHz
P1, position 3 -- 1st LO input, 40.455 to 70.455 MHz, 0 dBm
P1, position 4 -- 1st IF monitor output, 40.455 MHz
P1, position 5 -- RF input, 0 to 30 MHz

P2, pin 1 -- +16 VDC
P2, pin 3 -- Ground
P2, pin 12 -- Fault, low for fault (common with other fault lines)
P2, pin 13 -- -16 VDC (not used in this module)
P2, pin 22 -- 1st IF AGC, 0 to +8 VDC

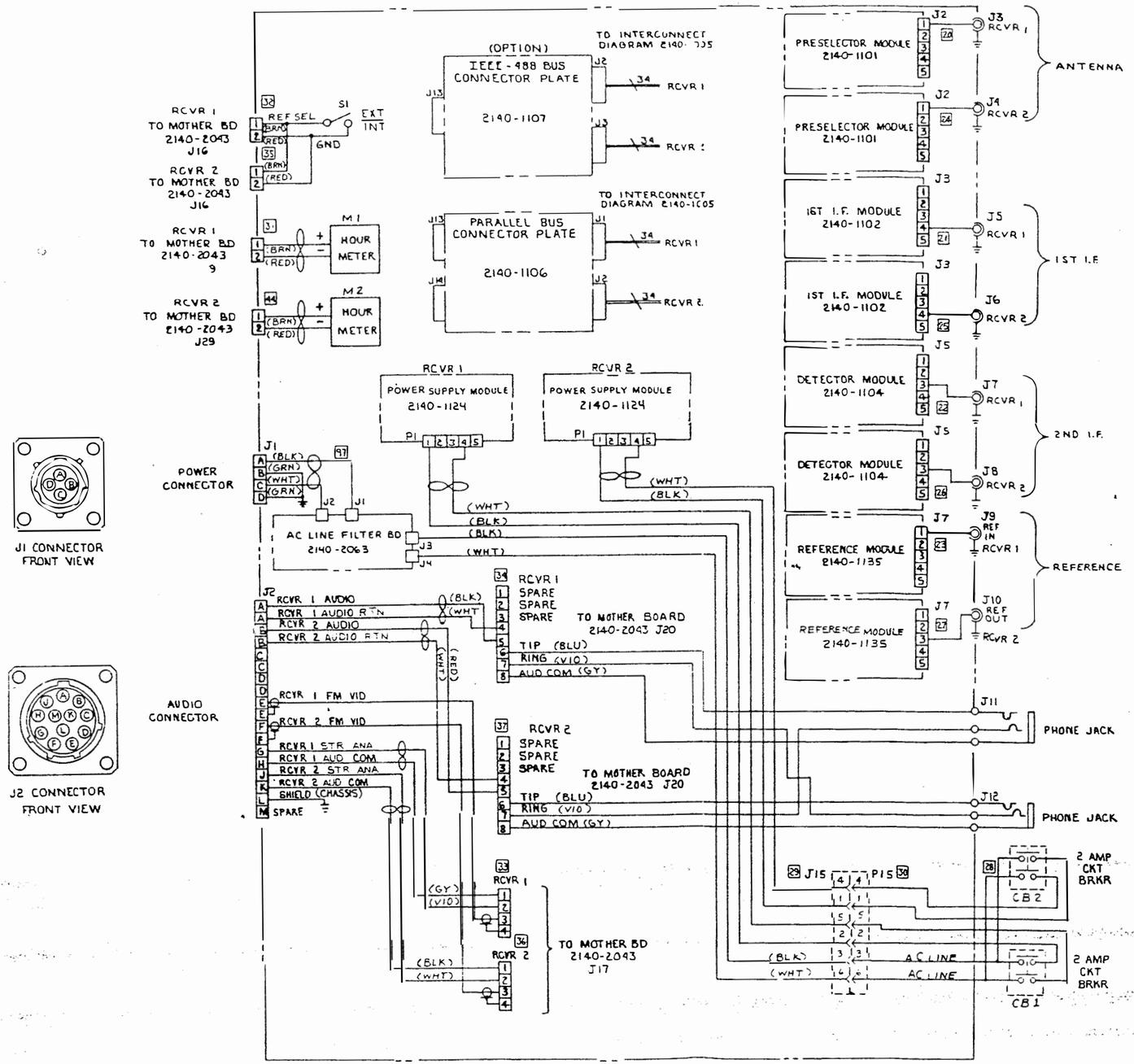

FIGURE 7-2
REAR PANEL INTERCONNECT

7.3 2nd IF MODULE

The 2nd IF module filters the signal at 455 KHz through one of 5 selectable filters and provides approximately 50 dB of signal gain to this signal. The gain in this module is controlled using the automatic or manual gain control functions.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.3-1 and 7.3-2 respectively.

The 2nd IF signal, originating in the 1st IF Module, appears at the coaxial connector in position 1 of P1 and made available to the gates of the field effect transistor (FET) stages Q2, Q5, Q8, Q12, Q15, and Q20. Additionally, Q17 is used to provide an independent output that is not filterd for use in other model receivers using this module that also have an independent sideband mode. This output is made available on the coaxial cable connector in position 2 of P1.

Filters FL1 through FL6 are used to provide the required bandwidth for the receiver. The filter bandwidths shown are nominal and other bandwidths may be substituted on special order.

Filter selection is made by BCD to Decimal Decoder U1, which brings the Q line corresponding to the desired bandwidth HI, while the remaining 5 lines stay LO. If (for illustration) Filter 1 were selected, FET switch Q1 would pull its drain LO, putting a LO on the source of Q2, causing it to conduct, thus enabling that filter. Common-emitter amplifier Q3 would also be enabled thus providing signal to integrated circuit amplifier U2. The gain of U2 may be controlled under automatic AGC, or manual gain control. Maximum gain may be up to 50 dB. Q10 provides the output signal through the coaxial cable connector in position 4 of P1.

ADJUSTMENTS: No adjustments are normally required. If U2 or T1 are replaced, T1 may be adjusted for maximum level while receiving a signal.

CONNECTIONS:

P1, position 1 -- 2nd IF input, 455 KHz
P1, position 4 -- 2nd IF output, 455 KHz

P2, pin 1 -- +16 VDC
P2, pin 3 -- Ground
P2, pin 4 -- BW 0, 5 V logic levels (selects filters in binary code)
P2, pin 5 -- BW 1, 5 V logic levels (selects filters in binary code)
P2, pin 7 -- BW 2, 5 V logic levels (selects filters in binary code)
P2, pin 10 -- 2nd IF AGC, 0 to +10 VDC
P2, pin 12 -- Fault (not used in this module)
P2, pin 13 -- - 16 VDC (not used in this module)

The filter select lines are activated in a binary coded fashion to select the desired filter.

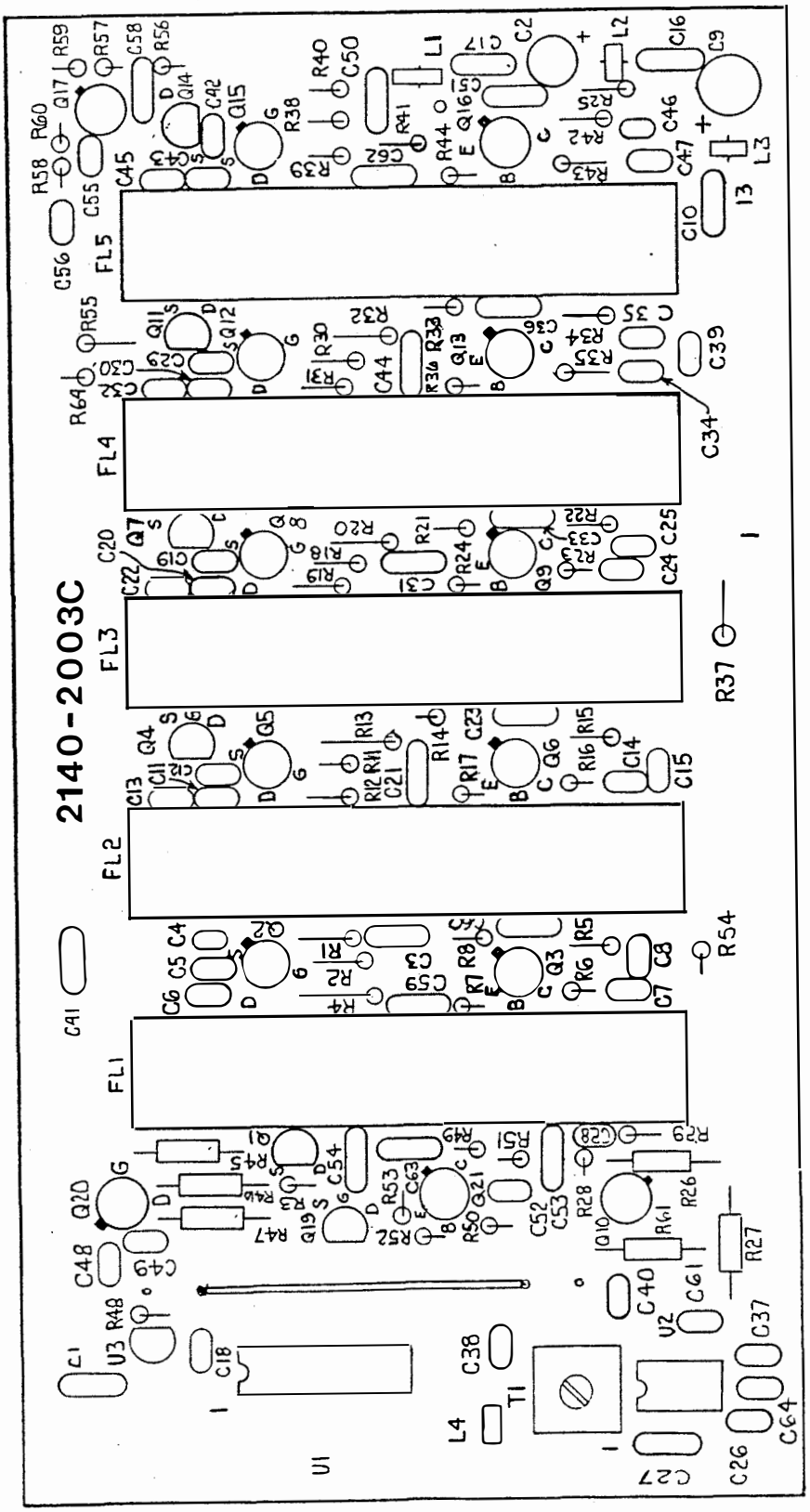

FIGURE 7.3-1
2nd IF MODULE ASSEMBLY DRAWING

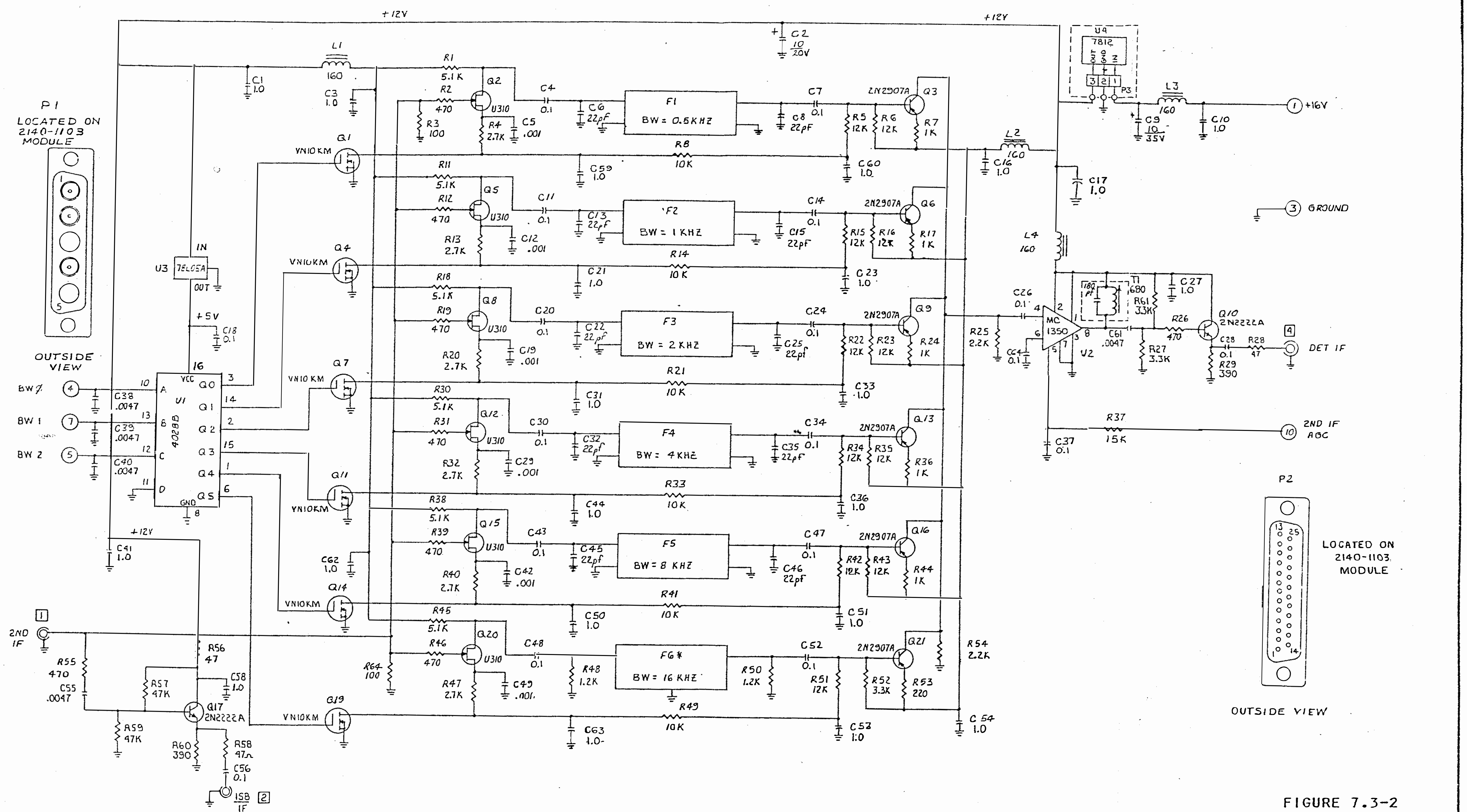

FIGURE 7.3-2
2nd IF MODULE SCHEMATIC

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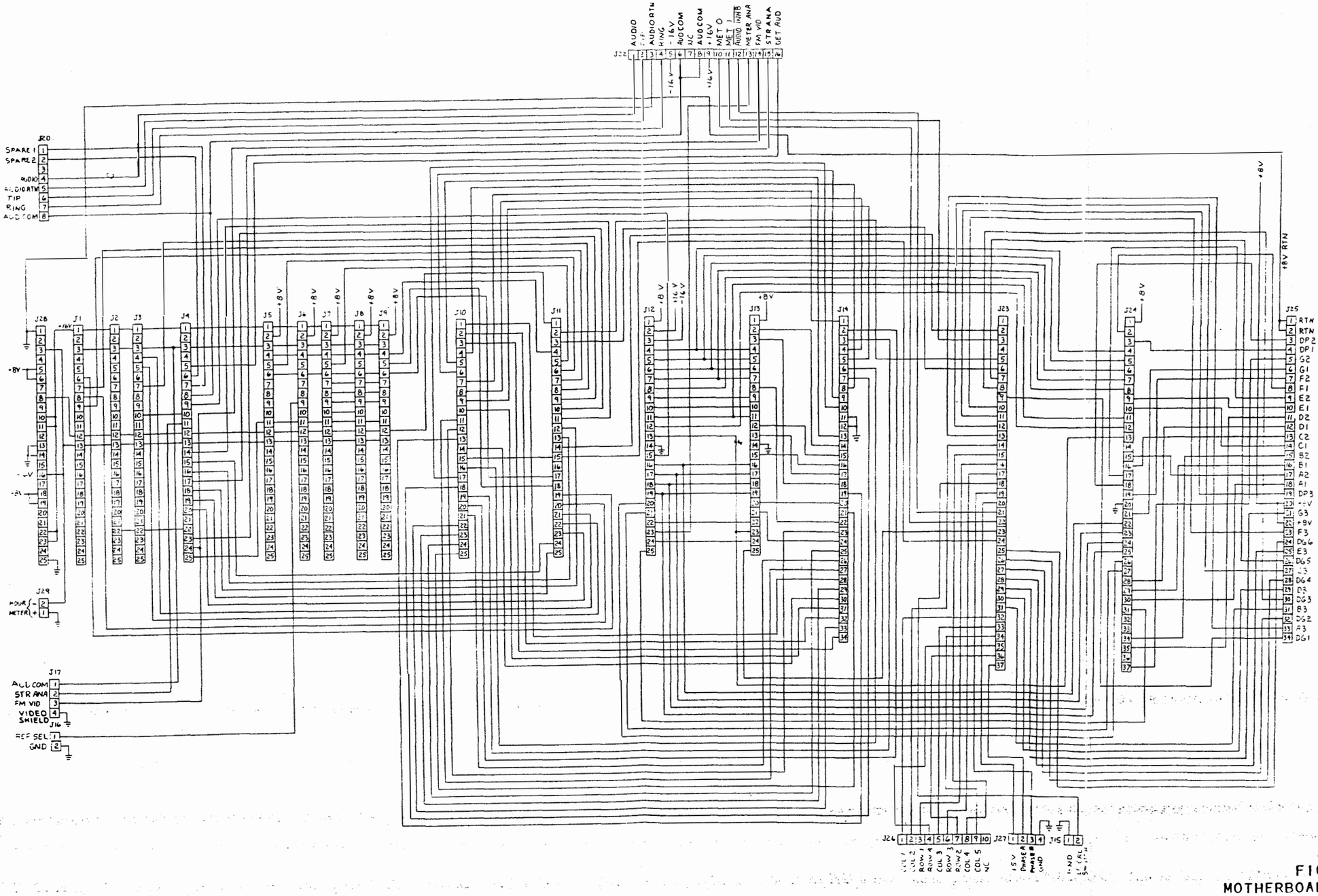


FIGURE 7-3
MOTHERBOARD SCHEMATIC

7.4 DETECTOR MODULE

The Detector module demodulates the signal in any selectable mode and uses the amplitude of the signal to operate the automatic gain control and signal strength metering functions.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.4-1 and 7.4-2 respectively.

The signal at 455 kHz is applied to the module via the coaxial cable connector in position 1 of P1. The overall gain of the receiver is adjusted by means of potentiometer R9 so as to meet the requirements for AGC threshold, sensitivity, linearity, and other requirements.

U2 is an IF amplifier providing up to 50 dB of signal gain. Its output is filtered by the tuned circuits made up of L3, L4, and C31 so as to reduce any wideband noise contributed by the amplifiers on the detector side of the filters in the 2nd IF module.

The output of the filter is buffered by emitter follower Q3 and applied to the FM detector, envelope detector, and product detector circuits.

Begining with the FM Detector, a 500 kHz L.O. signal from the BFO module is applied to the coaxial cable connector in position 4 of P1. This signal is amplified by Q1 and applied to mixer U13 as the local oscillator signal for this mixer. The amplitude of the signal at this point is detected by CR1 and CR2 and used as one input the the module fault detector.

The signal from the IF amplifier is further amplified by Q2 and applied as the RF signal to mixer U13. The mixer takes the difference between the LO at 500 kHz and the signal at approximately 455 kHz and produces an output signal at approximately 45 kHz. U5 converts the analog signal at its input to a sequence of square waves at the same frequency. This process removes all amplitude variations in the signal and provides a trigger signal to U6.

U6A is a one-shot multivibrator triggered by the signal from U5. The output from U6 thus consists of a series of fixed width pulses having a frequency equal to the input frequency. The pulse width is chosen so that a signal at 45 kHz produces approximately a 37-63 duty cycle pulse wave. A lower frequency produces a lower duty cycle while a higher frequency produces a higher duty cycle.

The output from U6 is filtered by the fourth order lowpass filter comprised of U7A and U7B and associated capacitors and resistors. The output of this filter is then a DC voltage proportional to the deviation of the input frequency from the center frequency that can vary at a rate allowed by the low pass filter. This voltage is applied to buffer amplifier U12. R97 is adjusted so that the output voltage is 0 VDC for a signal exactly at the receiver tuned frequency. This signal is taken from the receiver as the FM VIDEO output for use by external equipment.

The output from the lowpass filter is also applied to audio select switch U8R for use by the internal audio amplifiers.

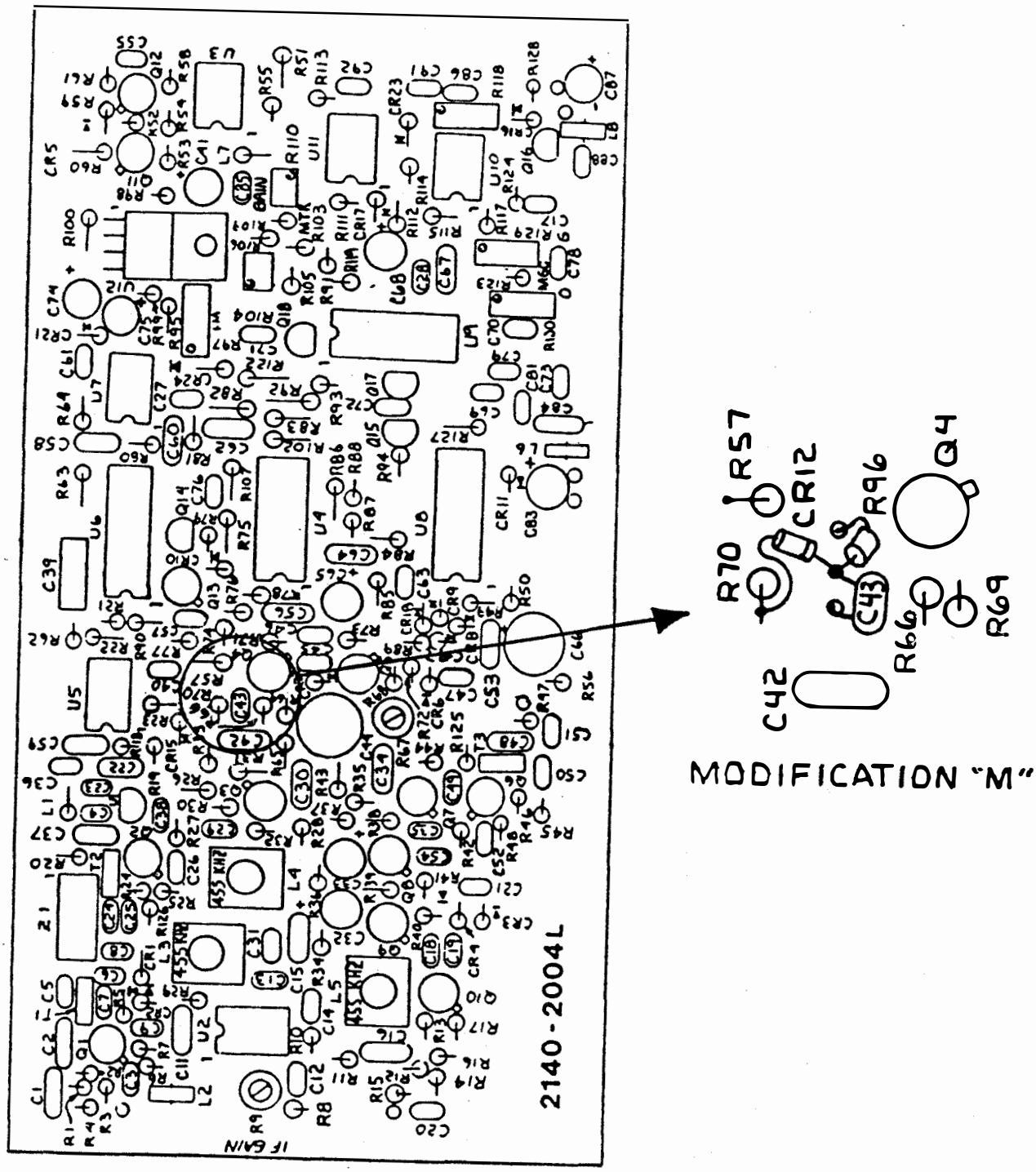
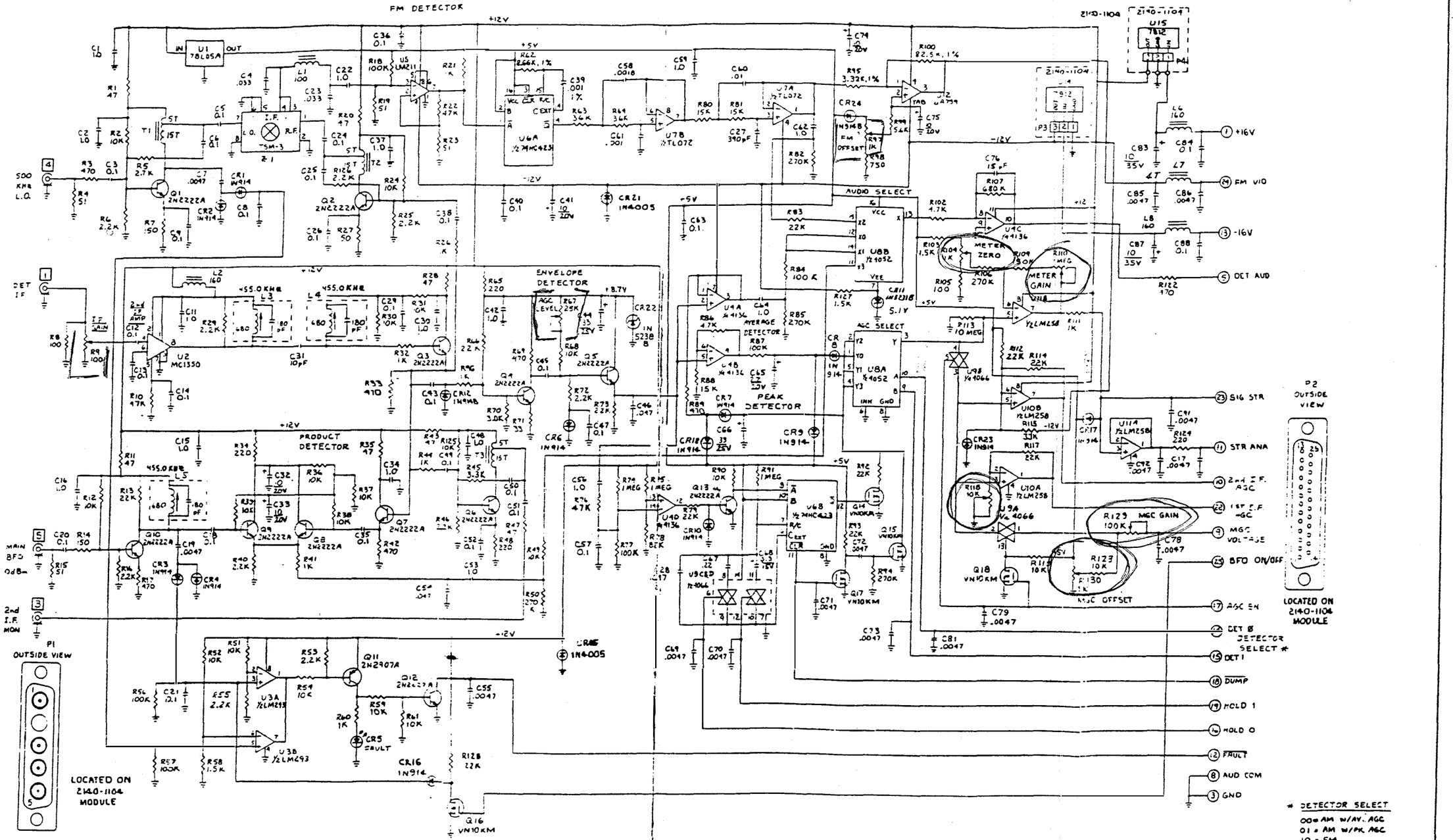


FIGURE 7.4-1
DETECTOR MODULE ASSEMBLY DRAWING



4 ☐ REFERS TO COAXIAL CONNECTOR PART NUMBER.

3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

REFERENCE DESIGNATORS NOT USED
C93, CR19, L9, Q16, R130, *4, U15
REFERENCE DESIGNATORS NOT USED
C88, R114, C77, R108, C82, R101, R121, R120, CR13, CR14

FIGURE 7.4-2
DETECTOR MODULE SCHEMATIC

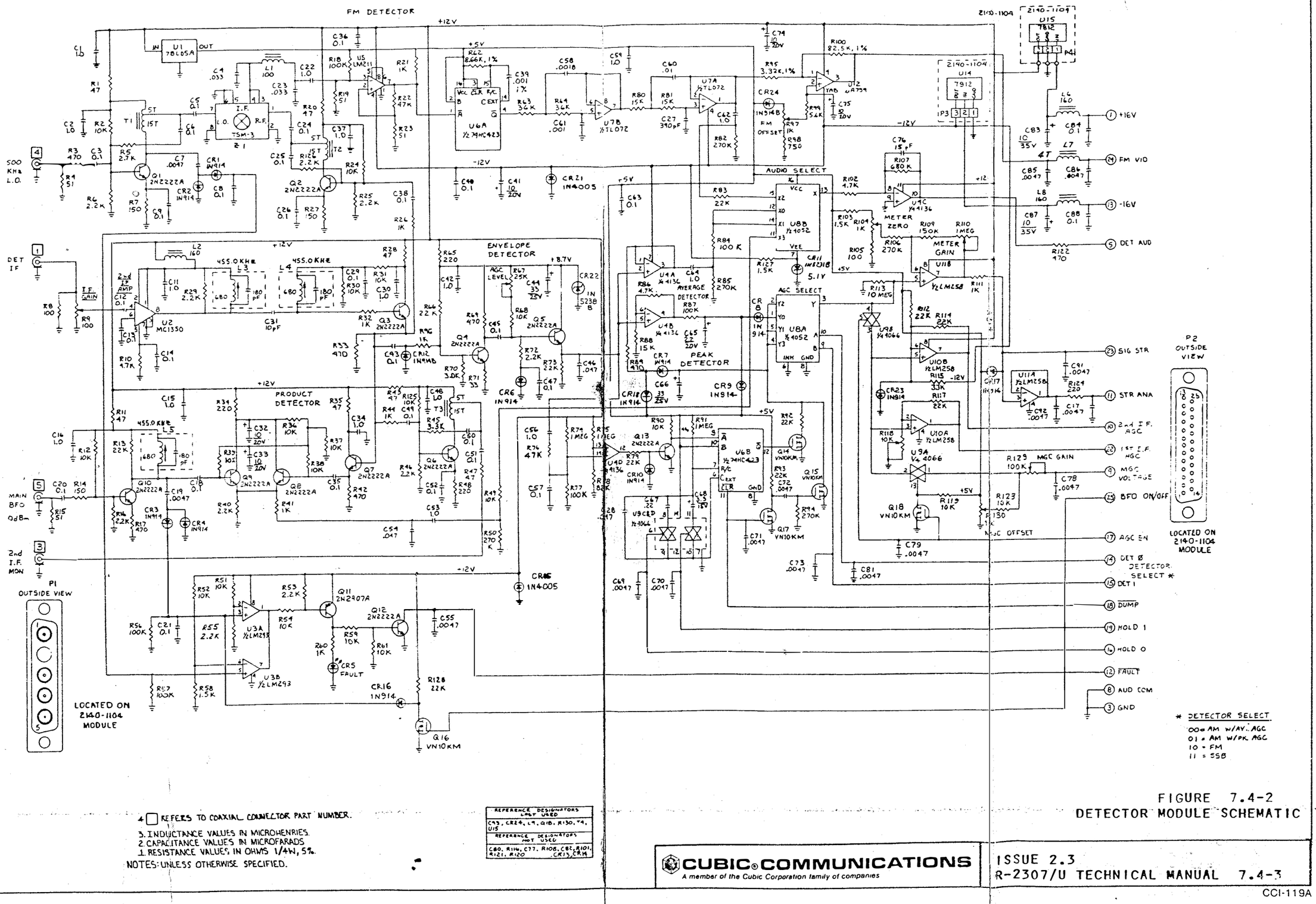


FIGURE 7.4-2
DETECTOR MODULE SCHEMATIC

The signal for the envelope detector is amplified by Q4 and applied to the detector transistor, Q5. This is a so-called infinite impedance detector biased just to the edge of conduction by the current through R67 and R68 divided by R72 and CR6. The audio output from this detector is buffered by U4A and applied to audio switch U8B.

The DC output from this detector is averaged through U4B and R87-C65 for use as an AGC voltage when the AM mode is selected. The DC output is peak detected through CR7 for use as an AGC voltage when the LSB, USB, or CW modes are selected. R89 and C66 determine the attack time for peak AGC. C66 and R92 determine the discharge time for peak AGC.

The hold time for peak AGC action is determined by the timing of re-triggerable one-shot U6B. Variations in signal amplitude caused by modulation result in the one-shot being re-triggered through U4D and Q13. When these variations cease, the one-shot times out after a time determined by the value of C28, C67, and C68. These capacitors are selected by the Hold time select lines Hold 0 and Hold 1. For short hold time, only C28 is used. Medium hold time uses both C28 and C67 while long hold time uses C28 and C68. The Dump command (given by the CPU when AGC hold time is changed or during sweep and scan operations) times out U6B immediately and, in addition, Q15 discharges C66 in the shortest possible time.

Suppressed or reduced carrier signals are demodulated in the Product Detector. Emitter follower Q7 drives the Product Detector composed of Q8 and Q9. This circuit simply mixes the 450 to 460 kHz BFO signal with the IF to produce the desired audio signal. C53 then couples the signal to pin 11 of the Audio Select switch U8B. The BFO signal is amplified by Q10 prior to being used in the product detector.

Amplifier transistor Q6 is used to provide a sample of the IF signal for use by external equipment.

The audio signal desired and the AGC mode are selected through U8B and U8A respectively. These are dual 4 input by 1 output analog switches operating under control of the DET 0 and DET 1 signals. When both these signals are low, inputs X0 and Y0 are selected corresponding to AM mode with average AGC. When DET 0 is high and DET 1 is low, inputs X1 and Y1 are selected and the receiver uses the envelope detector with peak AGC. This mode is ordinarily only available using the parallel bus. When DET 0 is low and DET 1 is high, the FM mode is selected using X2 and Y2 while both DET 0 and DET 1 high selects the product detector with peak AGC using the X3 and Y3 inputs.

The selected audio output is amplified in integrated circuit U4C and passed to the audio board mounted behind the display board on the front panel.

The signal strength voltage from the selected detector is processed by operational amplifiers U11B and U11A. Meter zero and gain controls (R104 and R110 respectively) are used to set the signal stength voltage range between 0 and +5 V. The output from U11B is applied to the analog to digital converter in the CPU module by means of a metering analog switch on the audio board while the output from U11A is provided for use by external equipment.

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Automatic or manual gain control for the receiver is determined by the state of the AGC EN signal applied through pin 17 of P2. When this signal is high, U9B (pins 3, 4, and 5) is on while U9A (pins 1, 2, and 13) is off by means of Q18 being turned on. This applies a voltage from the selected detector to U10B and U10A, the 2nd IF and 1st IF AGC amplifiers respectively and the gain is controlled automatically. When the AGC EN signal is low, the state of these two sections of U9 is reversed and the gain control voltage is derived from the digital to analog converter in the CPU module. This corresponds to manual gain control. R129 and R130 are used to convert the nominal 0 to +5 V output from the D/A converter to the values reguired by the gain control system.

The fault detection circuitry consists of dual comparator U3, transistors Q11 and Q12, Fault LED CR5 and associated components. U3A compares a sample of the BFO signal to a preset reference, while U3B samples the 500 kHz L.O. signal. In either case, an absence of signal produces a low output which is applied to the base of PNP transistor Q11. With Q11 turned on, LED CR5 is biased to conduct. Q11s collector goes high, turning NPN Q12 on. Q12s collector is pulled low, and this is applied to pin 12 of P2, the FAULT/ line to the CPU module. The BFO ON/OFF signal is used to disable the BFO fault detection circuitry in the AM and FM modes when the BFO signal is not used or applied to the module.

ADJUSTMENTS:

The following adjustments are normally made only after a component replacement following a repair. In the event that the Detector Module is placed in another receiver chassis or if the 1st IF or 2nd IF modules are replaced, it is possible that the AGC THRESHOLD, IF GAIN, METER ZERO, METER GAIN, MGC OFFSET, or MGC GAIN controls may require adjustment in order to make the audio output level or meter indications accurate. Do not make these adjustments unless it is absolutely necessary as some of the adjustments may interact.

Unless otherwise noted, all adjustments below are made with the receiver in CW mode with the frequency of the receiver set to the signal generator frequency and the BFO offset set to 1.00 kHz. Select the 2.0 kHz bandwidth, .25 second AGC, and IF shift of 0.000 kHz. The MGC controls are adjusted in manual gain adjust mode with the gain reduction set to the values indicated. The audio signal is observed at the 600 Ohm balanced output with a 600 ohm termination.

ADJ	FUNCTION		ADJUST FOR
L5	BFO tuning	--	maximum DC level at cathode of CR3
L3	SIGNAL tuning	--	maximum audio at P2, pin 11, -73 dBm input signal
L4	SIGNAL tuning	--	maximum audio at P2, pin 11,, -73 dBm input signal
R67	AGC THRESHOLD	--	0 dBm audio output, -73 dBm input signal
R9	IF GAIN	--	-17 dBm audio output with no signal input
R104	METER ZERO	--	bargraph indication of -100 dBm with -100 dBm input
R110	METER GAIN	--	bargraph indication of -20 dBm with -20 dBm input
R130	MGC OFFSET	--	0 dBm audio with signal = -100 dBm and gain = -27 dB
R129	MGC GAIN	--	0 dBm audio with signal = -20 dBm and gain = -107 dB
R97	FM OFFSET	--	0 bargraph indication (FREQ meter) on frequency

R67-R9, R104-R110, and R130-R129 may be interactive in adjustments

CONNECTIONS:

P1, position 1 -- IF input, 455 KHz
P1, position 3 -- IF monitor, 455 KHz, 0 dBm
P1, position 4 -- 500 KHz LO, 0 dBm
P1, position 5 -- BFO, 450 to 460 KHz, 0 dBm, CW, LSB, or USB modes only

P2, pin 1 -- +16 VDC
P2, pin 3 -- Ground
P2, pin 5 -- Detector Audio, 2 V p-p
P2, pin 8 -- Audio Common
P2, pin 9 -- MGC Voltage, 0 to + 5 VDC
P2, pin 10 -- 2nd IF AGC, 0 to + 10 VDC
P2, pin 11 -- Signal Strength Analog, 0 to + 5 VDC
P2, pin 12 -- FAULT/, low for fault
P2, pin 13 -- -16 VDC
P2, pin 14 -- DET 0, 5 V logic
P2, pin 15 -- DET 1, 5 V logic
P2, pin 16 -- Hold 0, 5 V logic
P2, pin 17 -- AGC Enable, +5 VDC for AGC, 0 for MGC
P2, pin 18 -- DUMP/, low pulse for dump
P2, pin 19 -- Hold 1, 5 V logic
P2, pin 22 -- 1st IF AGC, 0 to + 10 VDC
P2, pin 23 -- SIG STR, 0 to + 5 VDC
P2, pin 24 -- FM Video, 0 ± 1 Volt per KHz
P2, pin 25 -- BFO ON/OFF, low in CW, LSB, and USB, high in FM and AM

J1 — PRESELECTOR (P2)

PIN	DESCRIPTION
1	+16 V
2	NC
3	GND
4	NC
5	NC
6	BAND Ø
7	BAND 3
8	BAND 2
9	BAND 1
10	NC
11	NC
12	FAULT
13	-16 V
14	NC
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC

J2 — 1ST I.F. (P2)

PIN	DESCRIPTION
1	+16 V
2	NC
3	GND
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	NC
12	FAULT
13	-16 V
14	NC
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	1ST IF AGC
23	NC
24	NC
25	NC

J3 — 2ND I.F. (P2)

PIN	DESCRIPTION
1	+16V
2	NC
3	GND
4	BW Ø
5	BW 2
6	NC
7	BW 1
8	NC
9	NC
10	2ND IF AGC
11	STR ANA
12	FAULT
13	-16 V
14	NC
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	1ST IF AGC
23	NC
24	NC
25	NC

J4 — DETECTOR (P2)

PIN	DESCRIPTION
1	+16 V
2	NC
3	GND
4	NC
5	DET AUD
6	SPARE
7	SPARE
8	AUD COM
9	MGC VOLTAGE
10	2ND IF AGC
11	STR ANA
12	FAULT
13	-16 V
14	DET Ø
15	DET 1
16	HOLD Ø
17	AGC EN
18	DUMP
19	HOLD 1
20	PBØ
21	NC
22	1ST IF AGC
23	SIG STR
24	FM VID
25	BFO ON/OFF

J5 — BFO (P2)

PIN	DESCRIPTION
1	+16 V
2	+8 V
3	GND
4	SYN EN
5	BFO DATA
6	SYN CLK
7	NC
8	NC
9	NC
10	NC
11	BFO ON/OFF
12	FAULT
13	-16 V
14	TP-LOOP CV
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC

J6 — REFERENCE (P2)

PIN	DESCRIPTION
1	+16V
2	+8V
3	GND
4	SYN EN
5	NC
6	SYN CLK
7	NC
8	NC
9	REF SEL
10	NC
11	BFO ON/OFF
12	FAULT
13	-16V
14	TP-LOOP CV
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC

J7 — STEP LOOP (P2)

PIN	DESCRIPTION
1	+16V
2	+8V
3	GND
4	SYN EN
5	STEP DATA
6	SYN CLK
7	VCO LO
8	VCO HI
9	VCO MID
10	COARSE TUNE
11	BFO ON/OFF
12	FAULT
13	-16V
14	TP-LOOP CV
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC

J8 — OUTPUT LOOP (P2)

PIN	DESCRIPTION
1	-16V
2	+8 V
3	GND
4	SYN EN
5	NC
6	SYN CLK
7	VCO LO
8	VCO HI
9	VCO MID
10	COARSE TUNE
11	BFO ON/OFF
12	FAULT
13	-16V
14	TP-LOOP CV
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC

J9 — FINE LOOP (P2)

PIN	DESCRIPTION
1	+16 V
2	+8 V
3	GND
4	SYN EN
5	FINE DATA
6	SYN CLK
7	VCO LO
8	VCO HI
9	VCO MID
10	NC
11	BFO ON/OFF
12	FAULT
13	-16 V
14	TP LOOP CV
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC

J10 — BUS INTERFACE (P2)

PIN	IEEE-488	PARALLEL
1	D8	D8
2	D6	D6
3	D5	D5
4	D3	D3
5	D1	D7
6	ATN	STROBE
7	NRFD	SEL 4
8	EOI	SEL 2
9	IFC	SEL Ø
10	TLK EN	
11	ASW Ø	ID4
12	ASW 2	ID2
13	ASW 4	IDØ
14	D7	D1
15	WR	WR
16	D4	D4
17	D2	D6
18	SRQ	BUS DIR.
19	NDAC	
20	DAV	SEL 3
21	REN	SEL 1
22	SRQ EN	
23	LIS EN	
24	ASW 1	ID 3
25	ASW 3	ID 1

J11 — CPU (P2)

PIN	DESCRIPTION
1	FAULT
2	INTA
3	IO/M
4	SYN EN
5	STEP DATA
6	BFO DATA
7	BAND 1
8	BAND 3
9	BW 1
10	AGC EN
11	DET Ø
12	DUMP
13	HOLD Ø
14	INTR
15	WR
16	RESET OUT
17	SYN CLK
18	FINE DATA
19	BAND Ø
20	BAND 2
21	BW Ø
22	BW 2
23	PBØ
24	DET 1
25	HOLD 1

J12 — CPU (P1)

PIN	DESCRIPTION
1	+8V
2	+16V
3	-16 V
4	ADR/DAT 1
5	ADR/DAT 3
6	ADR/DAT 5
7	ADR/DAT 7
8	A9
9	A2
10	AØ
11	RD
12	EN4
13	ALE
14	GND
15	MGC VOLTAGE
16	ADR/DAT Ø
17	ADR/DAT 2
18	ADR/DAT 4
19	ADR/DAT 6
20	A8
21	A10
22	A1
23	METER ANA
24	BI
25	EN5

J13 — BUS INTERFACE (P1)

PIN	IEEE-488	PARALLEL
1	+8V	
2		D15
3		D13
4	ADR/DAT 1	
5	ADR/DAT 3	
6	ADR/DAT 5	
7	ADR/DAT 7	
8		D9
9	A2	
10	AØ	
11	RD	
12		D11
13		D12
14	GND (BUS GND)	
15		D14
16	ADR/DAT Ø	
17	ADR/DAT 2	
18	ADR/DAT 4	
19	ADR/DAT 6	
20		D8
21		D10
22	A1	
23	ALE	
24	BI	
25	RINT	

J28 — POWER SUPPLY (P2)

PIN	DESCRIPTION
1	GND
2	NC
3	-16V
4	NC
5	+8V
6	-5V
7	NC
8	FAULT
9	NC
10	+16V
11	+16V
12	NC
13	GND
14	GND
15	NC
16	-16V
17	NC
18	+8V
19	+8V
20	NC
21	NC
22	+16V
23	+16V
24	NC
25	GND

J14 — BUS INTERFACE

PIN	IEEE-488	PARALLEL
1	NFRD	SC4
2	DAV	SC3
3	NDAC	
4	EOI	SC2
5	IFC	SCØ
6	D4	D4
7	SRQ	BD
8	D3	D5
9	ATN	ST
10	D2	D6
11	GND	GND
12	GND	GND
13	D1	D7
14	GND	D15
15		D11
16	GND	D14
17		D12
18	GND	D13
19	AØ	IDØ
20	GND	D8
21	A1	ID1
22	GND	D9
23	A2	ID2
24	GND	D10
25	A3	ID3
26	REN	SC1
27	A4	ID4
28	D8	DØ
29	LIS EN	
30	D7	D1
31	TLK EN	AØ
32	D6	D2
33	SRQ EN	A1
34	D5	D3

J23 — PANEL INTERFACE (P2)

PIN	DESCRIPTION
1	NC
2	INTR
3	MET 1
4	NC
5	INTA
6	IO/M
7	DG5
8	DG3
9	DG1
10	SEG F3
11	SEG DP3
12	SEG C3
13	SEG A3
14	COL 2
15	COL 4
16	ROW 1
17	ROW 3
18	LOCAL
19	ENCODER PHASE B
20	+5V
21	INH
22	MET 2
23	RINT
24	WR
25	DG6
26	DG4
27	DG2
28	SEG E3
29	SEG G3
30	SEG D3
31	SEG B3
32	COL 1
33	COL 3
34	COL 5
35	ROW 4
36	ROW 2
37	ENCODER PHASE A

J24 — PANEL INTERFACE (P1)

PIN	DESCRIPTION
1	+5V
2	SEG F1
3	SEG DP1
4	ADR/DAT 1
5	ADR/DAT 3
6	ADR/DAT 5
7	ADR/DAT 7
8	A9
9	SEG E1
10	SEG C1
11	RD
12	EN 4
13	ALE
14	NC
15	SEG A2
16	SEG C2
17	SEG E2
18	SEG DP2
19	SEG F2
20	GND
21	SEG G
22	ADR/DAT Ø
23	ADR/DAT 2
24	ADR/DAT 4
25	ADR/DAT 6
26	A8
27	A10
28	SEG D1
29	SEG B1
30	SEG A1
31	EN5
32	NC
33	NC
34	SEG B2
35	SEG D2
36	NC
37	SEG G2

TABLE 7-1
MOTHERBOARD SIGNAL LIST

7.5 AUDIO BOARD

The Audio board provides amplification of the audio signal from the Detector Module for application to the headphones jacks and the 600 Ohm balanced line audio output from the receiver, the detection of audio signal level for metering purposes, and the signal selection gate for metering purposes.

Refer to the component assembly drawing and the schematic diagram for this board shown in Figures 7.5-1 and 7.5-2 respectively.

The audio signal from the Detector Module enters at J3 pin 16 and is applied to both the Metering Select and the Audio Inhibit circuitry. U3B simply acts as a switch to pass or inhibit the audio signal under CPU control to provide the squelch function. The Audio Inhibit line on J3 pin 12 is set high to enable the signal at the U3B output. A low on this line disables (inhibits) the signal.

C24 couples the audio signal both to the front panel volume control potentiometer (through J2/P2), and to buffer amplifier U2A. U2B drives the primary of transformer T1, which produces a 600 ohm balanced line signal. L1, L2 and C5 through C8 form a filter designed to exclude external RF signals from the audio amplifiers. Audio from the Volume Control on the front panel drives amplifier U6, whose filtered output signal is made available to the front panel headphone jack via J1.

Meter Select switch U3A serves as a 1-pole/4-throw switch under CPU control. When selected, the audio signal is processed by detector U1B (with CR2 and CR3), peak detector U1C (with CR4 and C3) and associated components for analog level, and is subsequently routed to U3 pin 13. The FM video signal at P3 pin 14 is converted to a 0 to +5V signal level by U1A, and is routed to U3 pin 12 in the same manner as the detected Audio signal. The Signal Strength analog line from the Detector module is connected to U3 pin 11.

The CPU module selects the desired signal for metering purposes via the MET 0 and MET 1 select lines on J3, pins 10 and 11 respectively. The selected signal is thus made available to the A/D converter on the CPU module via the Meter Analog line on J3, pin 13. The signal strength signal is used for squelch as well as scan or sweep stop purposes in addition to front panel bargraph metering while the other signals are selected only when those metering functions are required.

ADJUSTMENTS: NONE

CONNECTIONS:

J1 Headset Jack connection

1 Audio ground for headphones
2 Optional speaker connection
3 Ring contact on Headset jack
4 Tip contact on Headset jack

J2 Volume Control connection

1 Audio ground (Volume Control low)
2 Volume Control wiper
3 Volume Control high

Note: Ground connections to board only, not to chassis

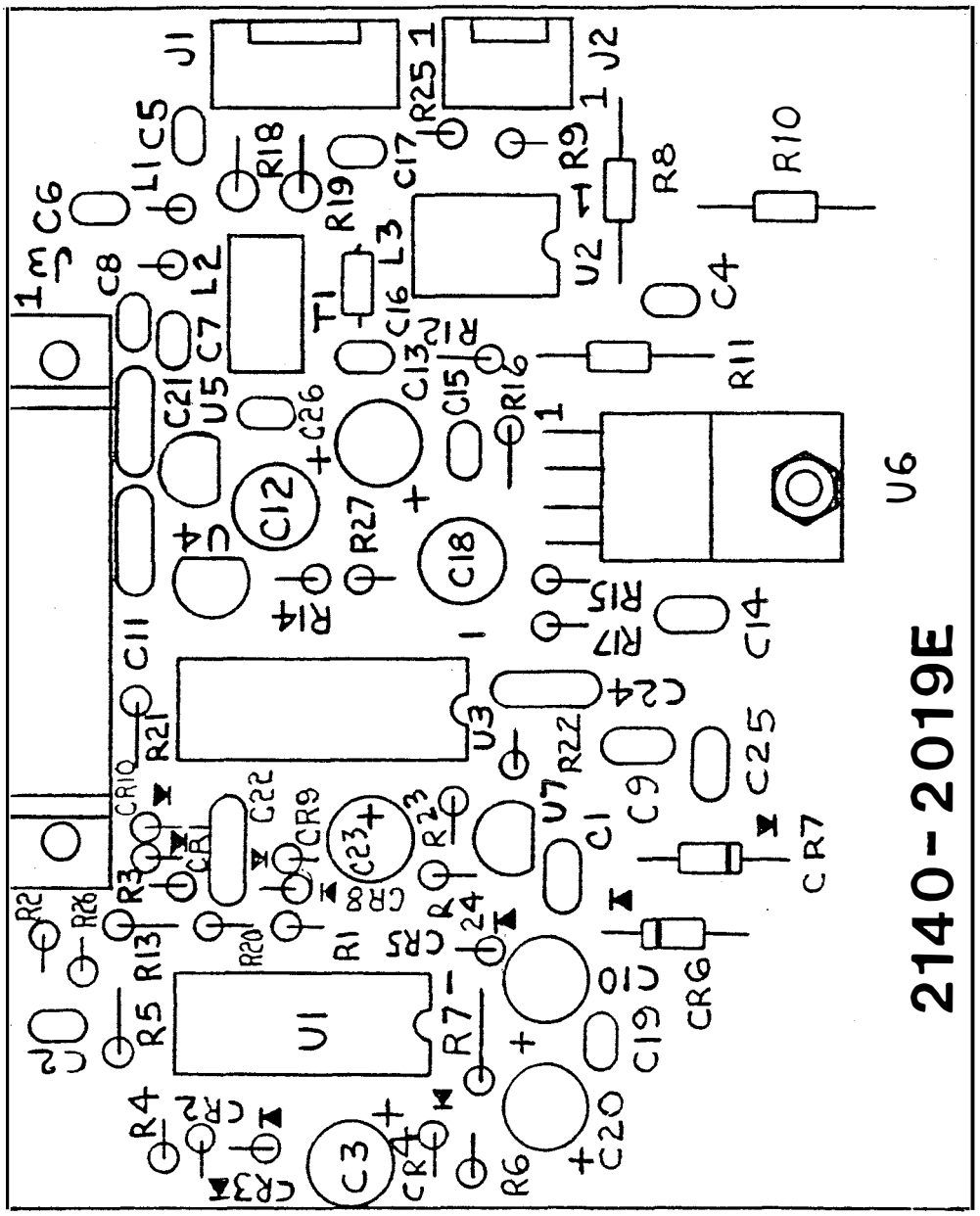
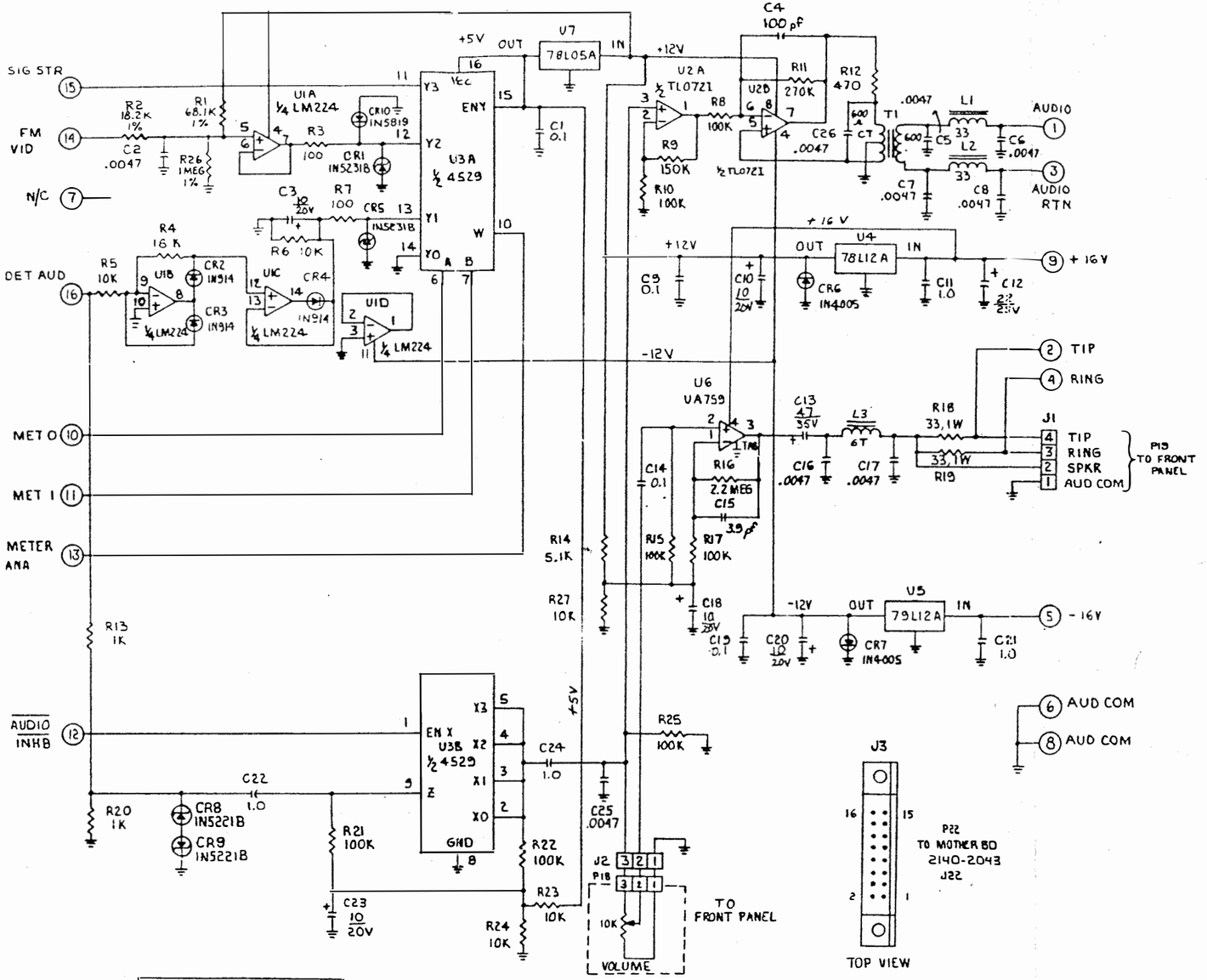


FIGURE 7.5 - 1
AUDIO BOARD ASSEMBLY DRAWING



REFERENCE DESIGNATORS NOT USED	
REFERENCE DESIGNATORS LAST USED	
R27 T1 C26 L3 CR10 J3 U7	

4. AUD COM GROUNDED AT DETECTOR MODULE ONLY
3. INDUCTANCE VALUES IN MICROHENRIES
2. CAPACITANCE VALUES IN MICROFARADS
1. RESISTANCE VALUES IN OHMS 1/4W, 5%
NOTES: UNLESS OTHERWISE SPECIFIED

FIGURE 7.5-2
AUDIO BOARD SCHEMATIC DIAGRAM

CONNECTIONS: (Continued)

J3 -- connector to motherboard

Pin 1 -- 600 Ohm balanced audio (Paired with Pin 3)
Pin 2 -- Headphones audio, tip
Pin 3 -- 600 Ohm balanced audio (Paired with Pin 1)
Pin 4 -- Headphones audio, ring
Pin 5 -- - 16 VDC
Pin 6 -- Audio Ground (Not chassis ground except at detector module)
Pin 7 -- No connection
Pin 8 -- Audio Ground (Not chassis ground except at detector module)
Pin 9 -- + 16 VDC
Pin 10 -- MET 0 (Binary meter selection)
Pin 11 -- MET 1 (Binary meter selection)
Pin 12 -- Audio Inhibit (Low when audio inhibited)
Pin 13 -- Meter Analog (0 to + 5 VDC to CPU)
Pin 14 -- FM Video (From Detector)
Pin 15 -- Signal Strength analog (From Detector)
Pin 16 -- Detector Audio (From Detector)

7.6 OUTPUT LOOP MODULE

The Output Loop module provides the 1st LO signal to the 1st mixer (in the 1st IF module) by phase locking a voltage controlled oscillator to the sum of the Step and Fine Loop module frequencies. This module contains three voltage controlled oscillators (VCOs) operating over the range of 40.455 to 70.455 MHz, a mixer extracting the difference between the Step Loop and Output Loop frequencies and a phase detector comparing this difference frequency with the Fine Loop frequency. Logic circuits are included to insure that the Output Loop locks only to the sum of the Step and Fine Loop signals and not to the difference frequency.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.6-1 and 7.6-2 respectively.

The three VCOs in this module are Hartley type oscillators, organized by frequency into a LO range (40.4550 to 48.7499 MHz), MED range (48.7550 to 58.6499 MHz) and HI range (58.6550 to 70.4550 MHz). These ranges correspond to receiver tuned frequency 0 to 8.2990, 8.3 to 18.1990, and 18.2 to 30 MHz respectively.

These three circuits are nearly identical. Looking at the HI range VCO (for example), it is comprised of junction field effect transistor (JFET) Q1, transformer T1, trimmer capacitor C2, varactor diodes CR1 and CR2, and associated components. NPN Transistor Q2 is used to select the particular VCO under control of the VCO select lines on P2, pins 7, 8, and 9. Diode CR3 provides signal detection for oscillator amplitude control while PIN diode CR4 couples the output of the oscillator to the other circuits.

Coarse tuning voltage originates in the Step Loop Module, and fine control voltage is provided by the output of the Loop Amplifier U5A. The individual VCO Select lines come from the Fine Loop shift register (CPU driven) on P2 pins 7, 8 and 9. VCO Select requires a logic high to enable.

Emitter-follower amplifiers Q7 and Q19 serve as buffers for the output of the selected VCO to isolate the VCO from the other signals in the module. Feedback amplifier Q8 provides the output signal from this module via the coaxial cable connection in P1, position 1 for application to the 1st IF module.

The signal from Q19 is applied both to the mixer circuit of Z1 through amplifier Q12 and the wrong-side-lock detector of U2 through U1D.

The Step Loop signal, input on the coaxial cable at P1 position 5, is passed by emitter-follower Q9 and placed on Pin 1 of Mixer Z1. This signal is also applied to the wrong-side-lock detector U2 through U1A.

The mixer (Z1) takes the difference in frequency between the Step Loop and Output Loop frequencies and passes this difference frequency through the low pass filter of L6, L7, and capacitors C62, C63, and C65. This difference signal is then applied to the Level Shifter circuit composed of Q13, Q14 and associated components which transforms the analog signal to a logic level signal. The logic level output of the Level Shifter is then applied to the gates of U3 to the phase detector U4.

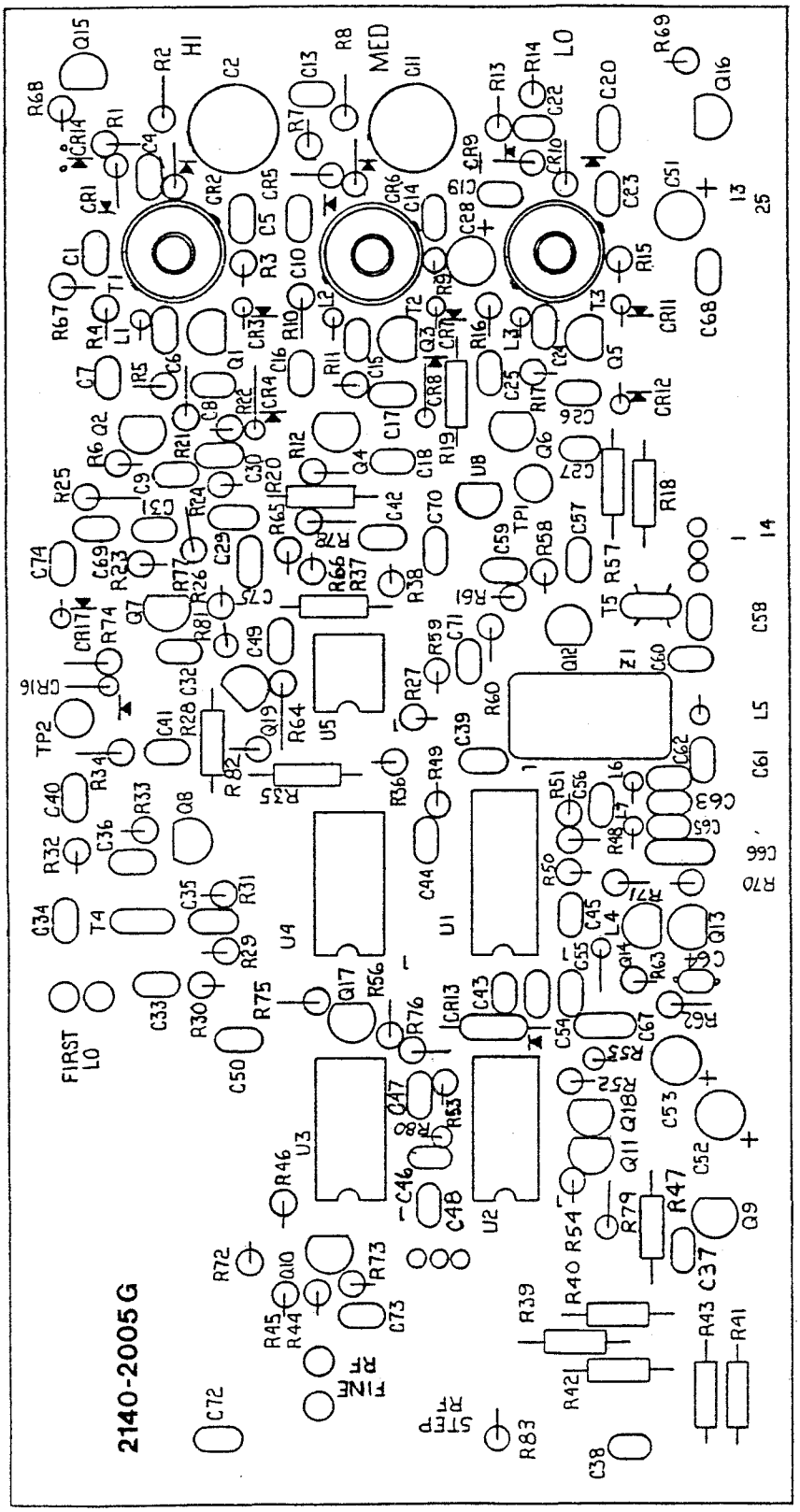


FIGURE 7.6 - 1
OUTPUT LOOP MODULE ASSEMBLY DRAWING

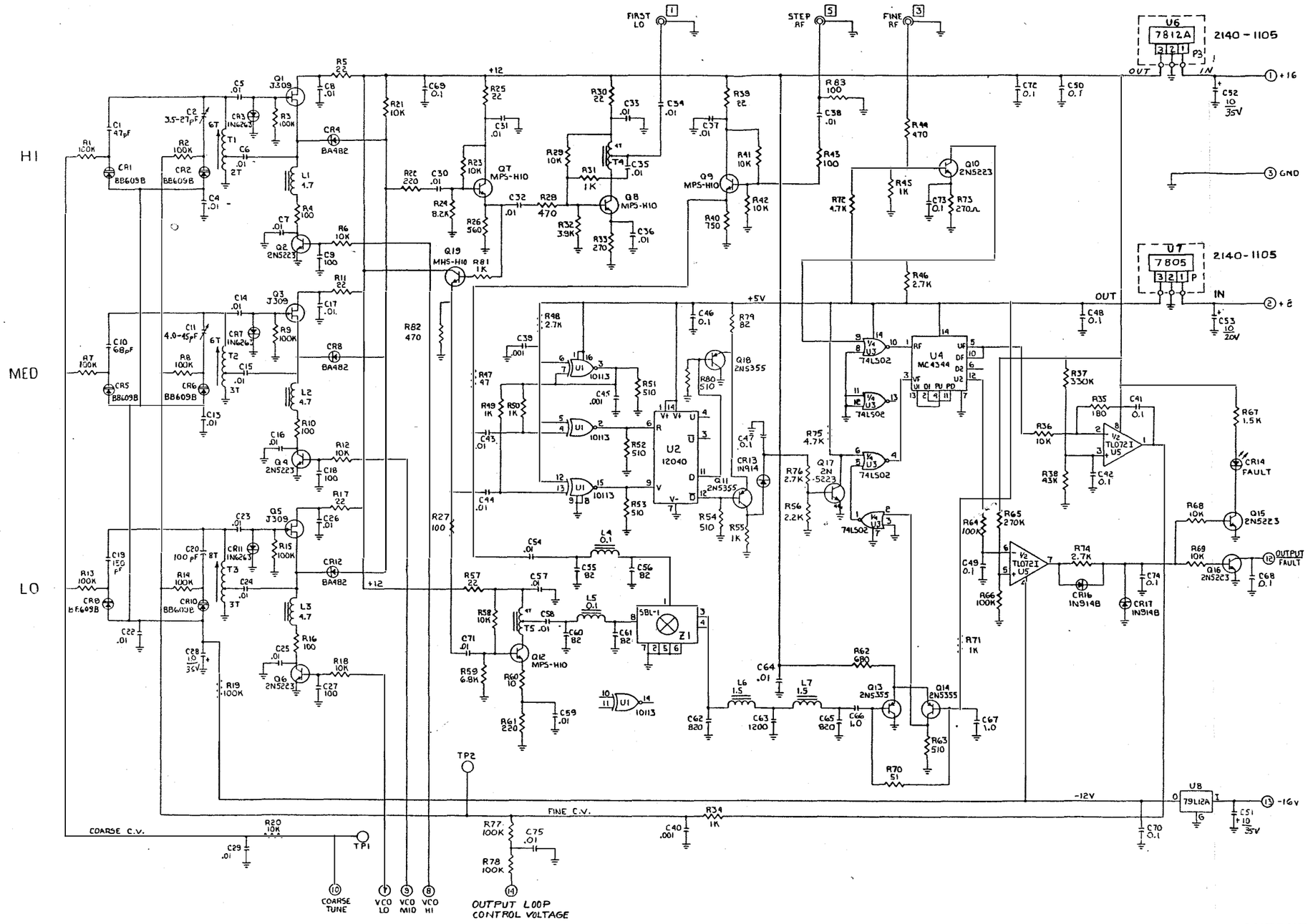


FIGURE 7.6-2
OUTPUT LOOP MODULE SCHEMATIC

The second input of Phase Detector U4 orignates in the Fine Loop Module. The coaxial cable in P1, position 3 passes this 55 to 155 kHz signal to amplifier Q10, through NOR gate U3C and on to the pin 1 input port of U4. The difference frequency signal from Z1 is applied to pin 3 of U4.

Two of the outputs of this phase detector are operative. The U2 signal on Pin 12 drives the Out-of-Lock Fault Detector circuit through U5B and the UF and DF signals on pins 5 & 10 drive the Loop Amplifier, U5A. The output from U5A on pin 1 provides the Fine Control Voltage applied to varactors CR2, CR6 and CR10 in the three VCOs.

The fault output of Phase Detector U4 pulses low when the loop is not locked. U5 pin 7 goes high at this time, turning Q15 on, biasing fault LED CR14 to conduct and become illuminated. Similarly, transistor Q16 is turned on, placing a low on the Output Fault line on P2, pin 12.

The Wrong-side Lock Detector (U2) is a phase/frequency comparator whose emitter-coupled-logic (ECL) output signals are converted to 5 volt saturated logic levels by emitter coupled matched pair transistors Q11 and Q18. These transistors operate to pulse Q11 on and off at the difference frequency rate when the Output Loop frequency is greater than the Step frequency. CR13 conducts on the positive pulses, charging C47, and turning Q17 on. This places a low logic level at NOR gate U3B pin 6 allowing normal operation by passing the difference frequency signal from U3A. If U2 detects the Output frequency to be less than the Step frequency, Q11 turns off, as does CR13, placing a high at U3B, pin 6. This disables the input to U4, pin 3 and causes the selected VCO to be driven to a higher frequency.

When the wrong-side-lock detector circuit senses that the Output Loop frequency is higher than the Step Loop frequency, the phase detector, U4, operates so that the difference between the Output Loop and Step Loop frequencies is equal to the Fine Loop frequency and the difference frequency is phase locked to the Fine Loop frequency.

ADJUSTMENTS: No adjustments are required in normal service. In the event of component replacement or drift in characteristics, the following VCO adjustments may be made:

Connect an Oscilloscope through a 10 to 1 probe to TP2. This test point is also connected to pin 14 on P2 on the module motherboard connector. Set the vertical controls to DC coupling, .5 V/division (Including the probe division)

THIS PAGE IS INSERTED FOR USER NOTES

T3,

Tune the receiver in turn to each of the following frequencies: 0.0 MHz, 3.9 MHz and 8.2 MHz. Observe the Oscilloscope and check if the voltage at TP2 remains inside the limits of 0.0 VDC ±2.0 V for each frequency . If not, observe the trend in voltage. If these voltages remain within 2.0 V of each other for each of the three frequencies, adjust T3 so the voltage at the middle of the 3 frequencies is 0.0 VDC.

T2, C11

Perform the procedure substituting the following frequencies:
8.3 MHz, 13.0 MHz, 18.1 MHz

If the voltage tends to increase with increase in frequency, reduce the capacitance (less mesh) of C11 a small amount and adjust T2 for 0.0 VDC at TP2 at the center frequency. If the voltage tends to decrease for an increase in frequency, increase the capacitance of C11 (more mesh) a small amount and adjust T2 for 0.0 VDC at TP2 at the center frequency. Repeat step 2 until first criterion is met (0.0 VDC ±2.0 V on all three frequencies).

NOTE: It is normal for C11 to be nearly fully meshed when done.

T1, C2

Perform the procedure substituting the following frequencies:
18.2 MHz, 23.8 MHz, 30.0 MHz

NOTE: Trimmer cap C2 should not be fully meshed when done.

The output level on the coaxial cable in position 1 should be between 140 and 300 mV peak to peak into a 50 Ohm load.

CONNECTIONS:

P1, position 1 -- 1st LO output
P1, position 3 -- Fine Loop RF input to module
P1, position 5 -- Step Loop input to module

P2, Pin 1 -- + 16 VDC
P2, Pin 2 -- + 8 VDC
P2, Pin 3 -- Ground
P2, Pin 4 -- SYN EN (synthesizer enable signal, not used in this module)
P2, Pin 6 -- SYN CK (synthesizer clock signal, not used in this module)
P2, Pin 7 -- VCO LO (high to select)
P2, Pin 8 -- VCO HI (high to select)
P2, Pin 9 -- VCO MED (high to select)
P2, Pin 10 -- Coarse Tune Voltage
P2, Pin 12 -- Fault (Low in fault -- common with other faults in receiver)
P2, Pin 13 -- - 16 VDC
P2, Pin 14 -- Test Point, loop control voltage

7.7 STEP LOOP MODULE

The Step Loop module provides a phase locked signal from 40.4 to 70.4 MHz in 100 kHz steps to the Output Loop module. It uses the 1 MHz reference frequency from the Reference module and serial data from the CPU module.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.7-1 and 7.7-2 respectively.

The three VCOs in this module are Hartley type oscillators, organized by frequency into a LO range (40.4 to 48.6 MHz), MED range (48.7 to 58.5 MHz) and HI range (58.6 to 70.4 MHz). These frequency ranges correspond to receiver tuned frequencies of 0 to 8.2999, 8.3 to 18.1999, and 18.2 to 30 MHz respectively.

These three circuits are nearly identical. Looking at the HI range VCO (for example), it is comprised of junction field effect transistor (JFET) Q1, transformer T1, trimmer capacitor C2, varactor diodes CR1 and CR2, and associated components. NPN Transistor Q2 is used to select the particular VCO under control of the VCO select lines on P2, pins 7, 8, and 9. Diode CR3 provides signal detection for oscillator amplitude control while PIN diode CR4 couples the output of the oscillator to the other circuits.

The output of the selected VCO is coupled by C30 to the base of NPN buffer Q7 and amplified by Q8 for input to the Output Loop Module. Q7s emitter output is also used to drive the frequency input of dual modulus prescaler U1, a divide by 20 or 21 device (selectable via pin 1). U2, which receives its frequency input from U1, is a multi-function synthesizer chip, incorporating programmable divider, reference divider, and phase detector into a single package. In addition to the 1 MHz Step Reference, U2 also receives data, clock and enabling inputs from the CPU under program control.

Shift register U4 provides Digital to Analog Converter U3 with the 8-bit information necessary for it to drive operational amplifier U5B. The output from U5B, pin 7, is an analog voltage (±8 V) used as input to the VCOs as a coarse tuning control voltage (TP1). In line with the coarse tuning voltage is a noise reduction filter composed of C29, R20, C56 and R36. Diodes CR17 through CR20 act as a speed-up circuit when new frequencies are selected.

Synthesizer circuit U2 generates the fine tuning control voltage at pin 5 (TP2) which is applied to the cathodes of varactors CR2, CR6 and CR10 and provides a lock detector signal for input to the one-shot multivibrator U6A. This lock detector signal input (from U2 pin 7) pulses when the loop is not locked. U6A and associated components form the fault detector circuit. When the U6A pin 7 output goes low during a no-lock condition, PNP transistor Q9 is biased to conduct, turning Fault indicator LED CR16 and transistor Q10 on, putting a low on the module Fault line.

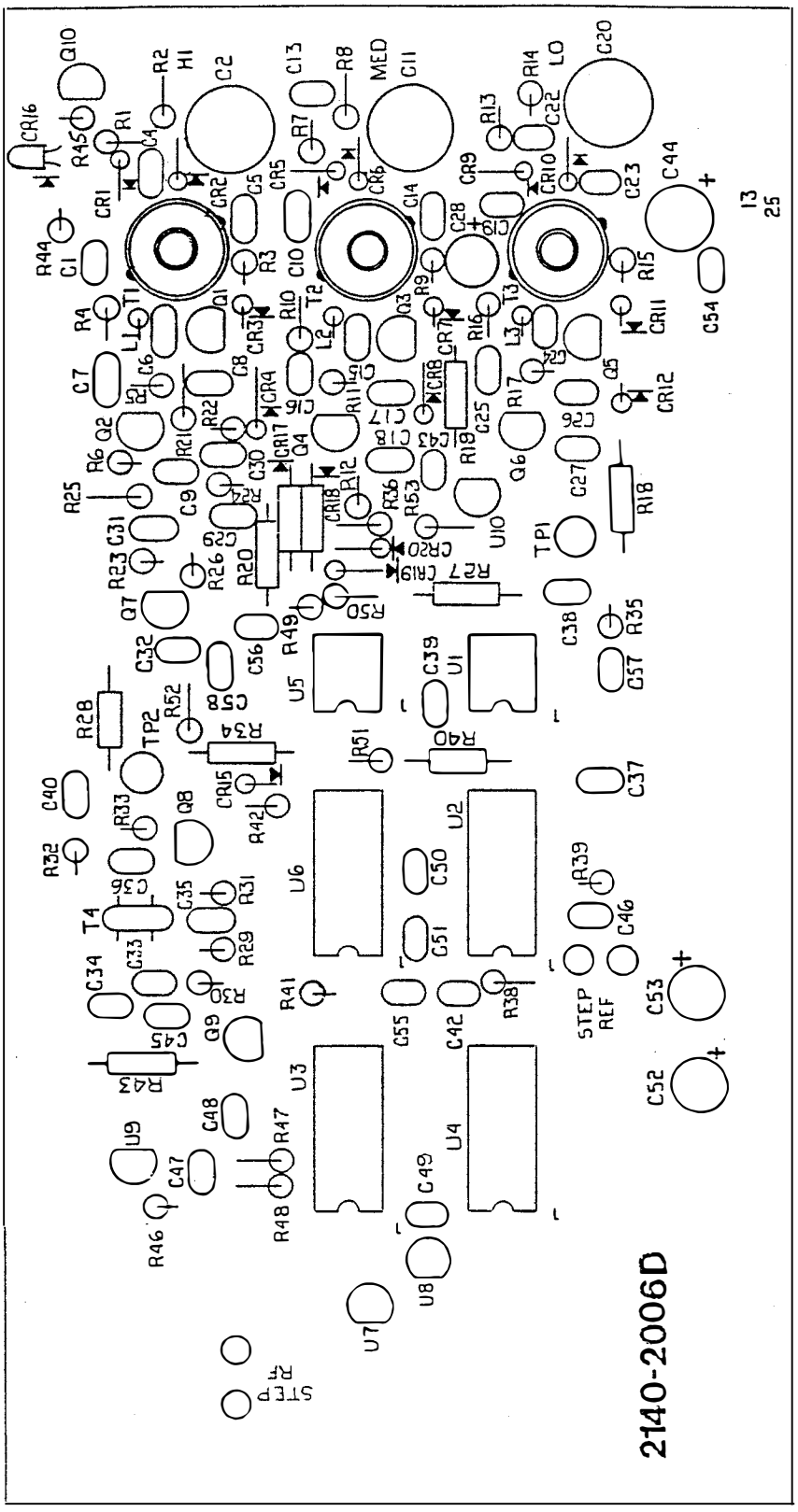


FIGURE 7.7 - 1
STEP LOOP MODULE ASSEMBLY DRAWING

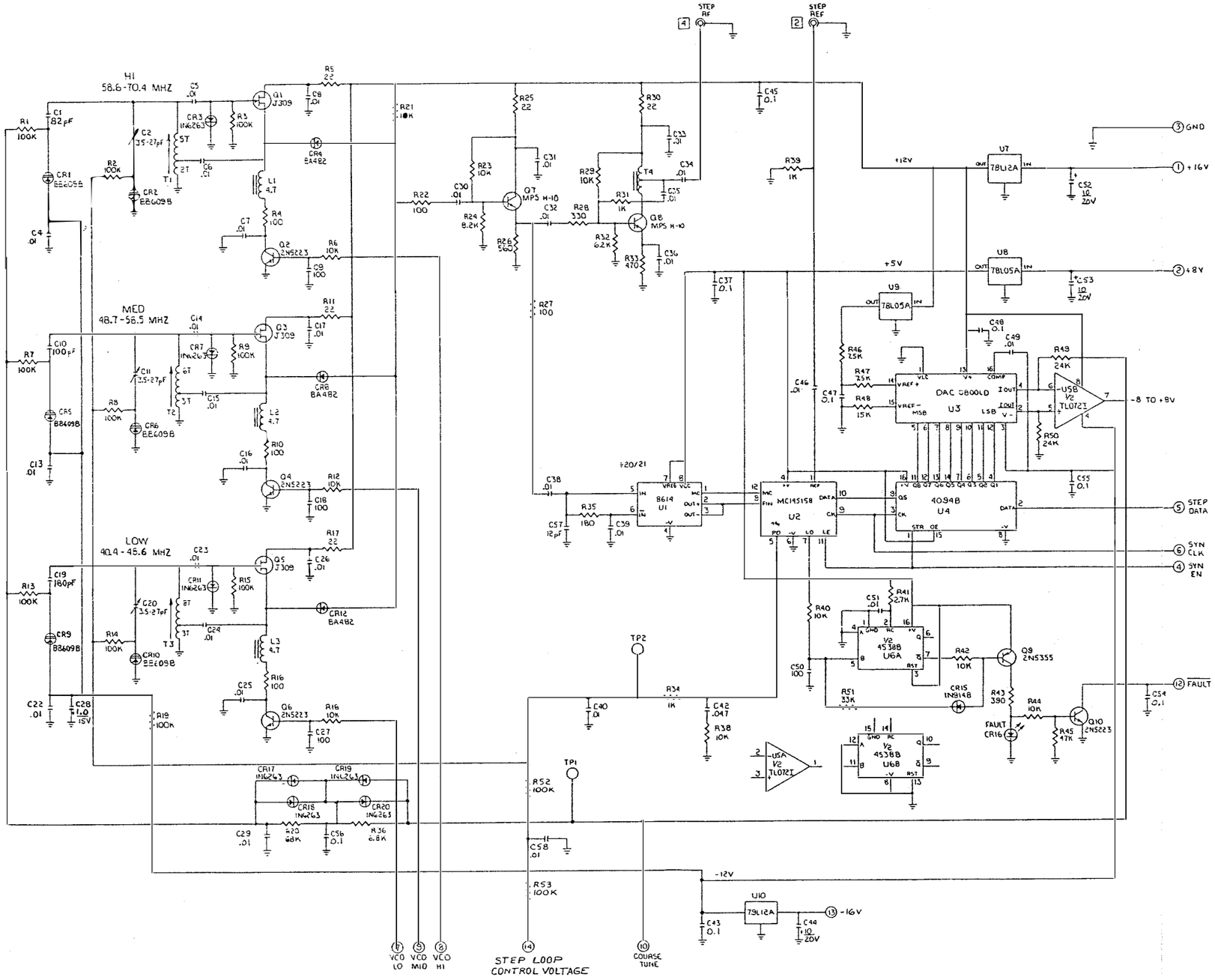


FIGURE 7.7-2
STEP LOOP MODULE SCHEMATIC

ADJUSTMENTS: No adjustments are required in normal service. In the event of component replacement or drift in characteristics, the following VCO adjustments may be made:

Connect an Oscilloscope through a 10 to 1 probe to TP2. Set the vertical controls to DC coupling, .5 V/division (Including the probe division)

T3, C20

Tune the receiver in turn to each of the following frequencies: 0.0 MHz, 3.9 MHz and 8.2 MHz. Observe the Oscilloscope and check if the voltage at TP2 remains inside the limits of 2.5 VDC ±0.5 V for each frequency . If not, observe the trend in voltage. If these voltages remain within 0.5 V of each other for each of the three frequencies, adjust T3 so the voltage at the middle of the 3 frequencies is 2.5 VDC. If the voltage tends to increase with increase in frequency, reduce the capacitance (less mesh) of C20 a small amount and adjust T3 for 2.5 VDC at TP2 at the center frequency. If the voltage tends to decrease for an increase in frequency, increase the capacitance of C20 (more mesh) a small amount and adjust T3 for 2.5 VDC at TP2 at the center frequency. Repeat step 2 until first criterion is met (2.5 VDC ±0.5 V on all three frequencies).

T2, C11 Perform the procedure substituting the following frequencies: 8.3 MHz, 13.0 MHz, 18.1 MHz

T1, C2 Perform the procedure substituting the following frequencies: 18.2 MHz, 23.8 MHz, 30.0 MHz

The output level on the coaxial cable in position 4 should be between 0.45 and 1.4 V peak to peak into a 50 Ohm load.

CONNECTIONS:

P1, position 2 -- Reference input, 1 MHz
P1, position 4 -- Step RF output from module to output loop

P2, Pin 1 — + 16 VDC
P2, Pin 2 -- + 8 VDC
P2, Pin 3 -- Ground
P2, Pin 4 — SYN EN (Synthesizer enable pulse to latch data)
P2, Pin 5 -- STEP DATA (Step Loop data)
P2, Pin 6 -- SYN CLK (Synthesizer data clock)
P2, Pin 7 -- VCO LO
P2, Pin 8 -- VCO HI
P2, Pin 9 -- VCO MED
P2, Pin 10 -- Coarse Tune Voltage
P2, Pin 12 -- Fault (Low in fault -- common with other faults in receiver)
P2, Pin 13 -- - 16 VDC
P2, Pin 14 -- Test point, Loop control voltage

THIS PAGE IS INSERTED FOR USER NOTES

7.8 FINE LOOP MODULE

The Fine Loop module provides a signal from 55 to 154.99 kHz in 10 Hz steps to the Output Loop module. It uses the 1 MHz reference frequency from the Reference module and serial data from the CPU module.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.8-1 and 7.8-2 respectively.

The three VCOs in this module are Hartley type oscillators, organized by frequency into a LO range (55.0 to 77.69 MHz), MED range (77.7 to 109.73 MHz) and HI range (109.74 to 154.99 MHz). These frequency ranges correspond to tuning of the receiver between 100 kHz increments with the LO range corresponding to xx.x0000 to xx.x2269 MHz, the medium range corresponding to xx.x2270 to xx.x5473 MHz, and the HI range corresponding to xx.x5474 to xx.x9999 MHz. xx.x represents any MHz and 100 kHz frequency. The oscillator generates these frequencies in 10 kHz steps.

These three circuits are nearly identical. Looking at the LO range VCO (for example), it is composed of JFET Q1, transformer T1, varactor CR1, and associated components. The individual VCO Select lines come from shift register U5 (CPU driven) at pins-11, 12 and 13. VCO Select requires a logic high to enable, applied to the base junctions of Q2, Q4 and Q6 for the LO, MED and HI ranges respectively.

The output of the selected VCO is coupled by C23 to emitter-follower Q7. The output is split at this point, one side driving Prescaler U3, the other inputing a Divide-by-1000 chain composed of U1 (divide by 40) and U2 (dual divide by 5). The 55 - 154.99 kHz output result (in 10 Hz increments) exits the module via the coaxial cable in P1, position 5 for input to the Output Loop Module.

U3 is a dual modulus prescaler (divide-by-32/33) device which both provides a signal to U4, and receives (a divide-by-A) instruction from U4. U4 is a multi-function synthesizer chip, incorporating programmable divider, reference divider and phase detector into a single package. In addition to the Prescaler frequency and 1 MHz Reference, U4 also receives data, clock and enabling inputs from the CPU under program control. Eight-bit shift register U5 interfaces incoming CPU serial data for VCO selection in all three Loop Modules, as well as data to multi-function U4 and the BFO ON/OFF data line (P2 pin 11) to the BFO Module itself.

The pin 7 (Lock Detector) output of U4 is a normally high signal which will pulse low in the event of an "out-of-lock" condition. Out of Lock Detector U7A (a retriggerable multivibrator) will sense this on its input and hold its pin 7 output low in response. PNP Fault Driver Q8 is biased on, enabling Fault LED CR11. With its base juction pulled high, NPN Q9 conducts and outputs a logic low from its collector to P2 pin-12 (FAULT/).

The pin 5 (Phase Detector) output of multi-function U4 is an analog voltage corresponding to the degree of phase or frequency error between the VCO frequency and the desired frequency. Loop Amp U6B then provides an amplified control voltage at pin 7 that is applied to the cathodes of varactors CR1, CR4 and CR7.

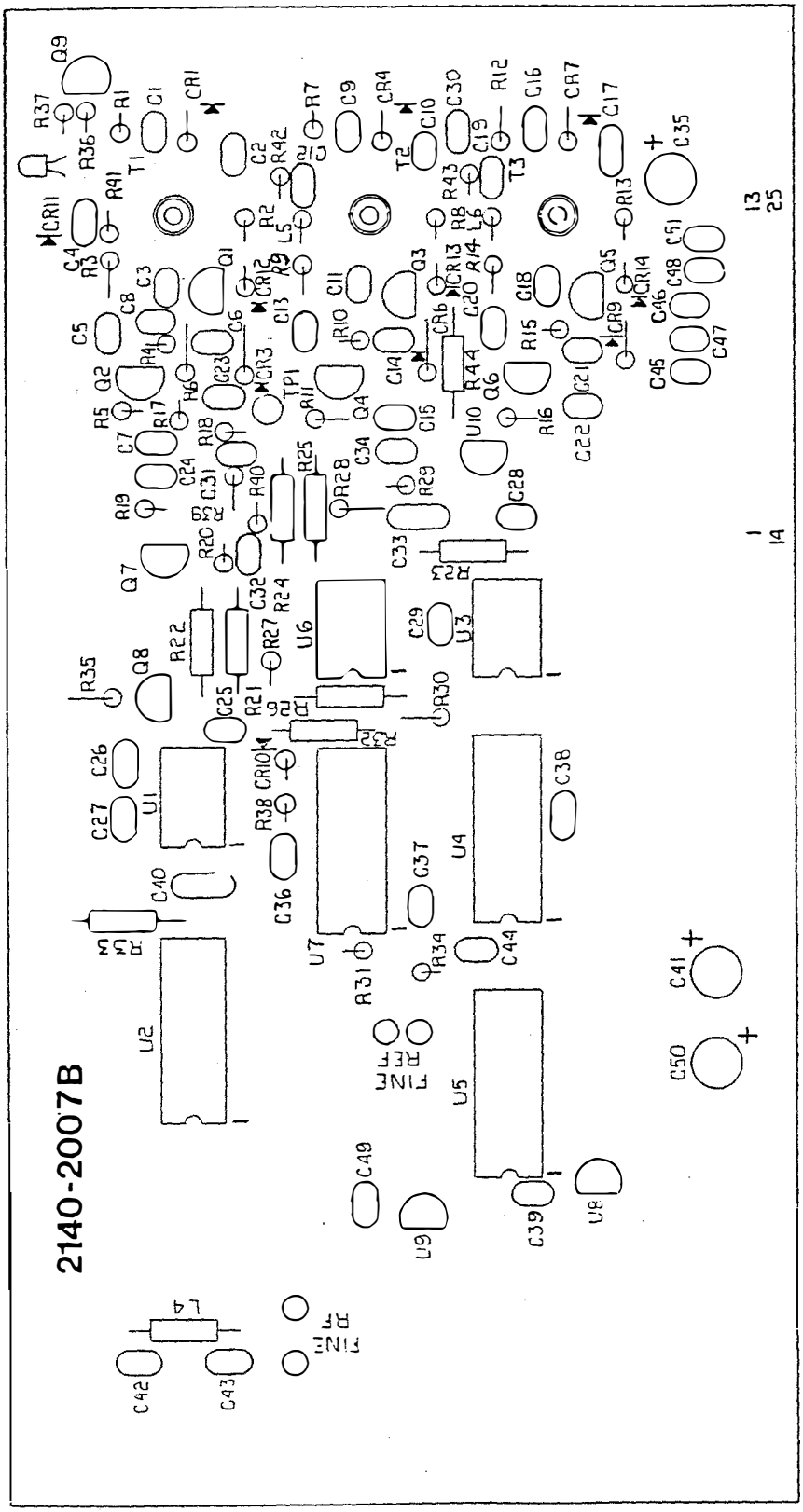


FIGURE 7.8-1
FINE LOOP MODULE ASSEMBLY DRAWING

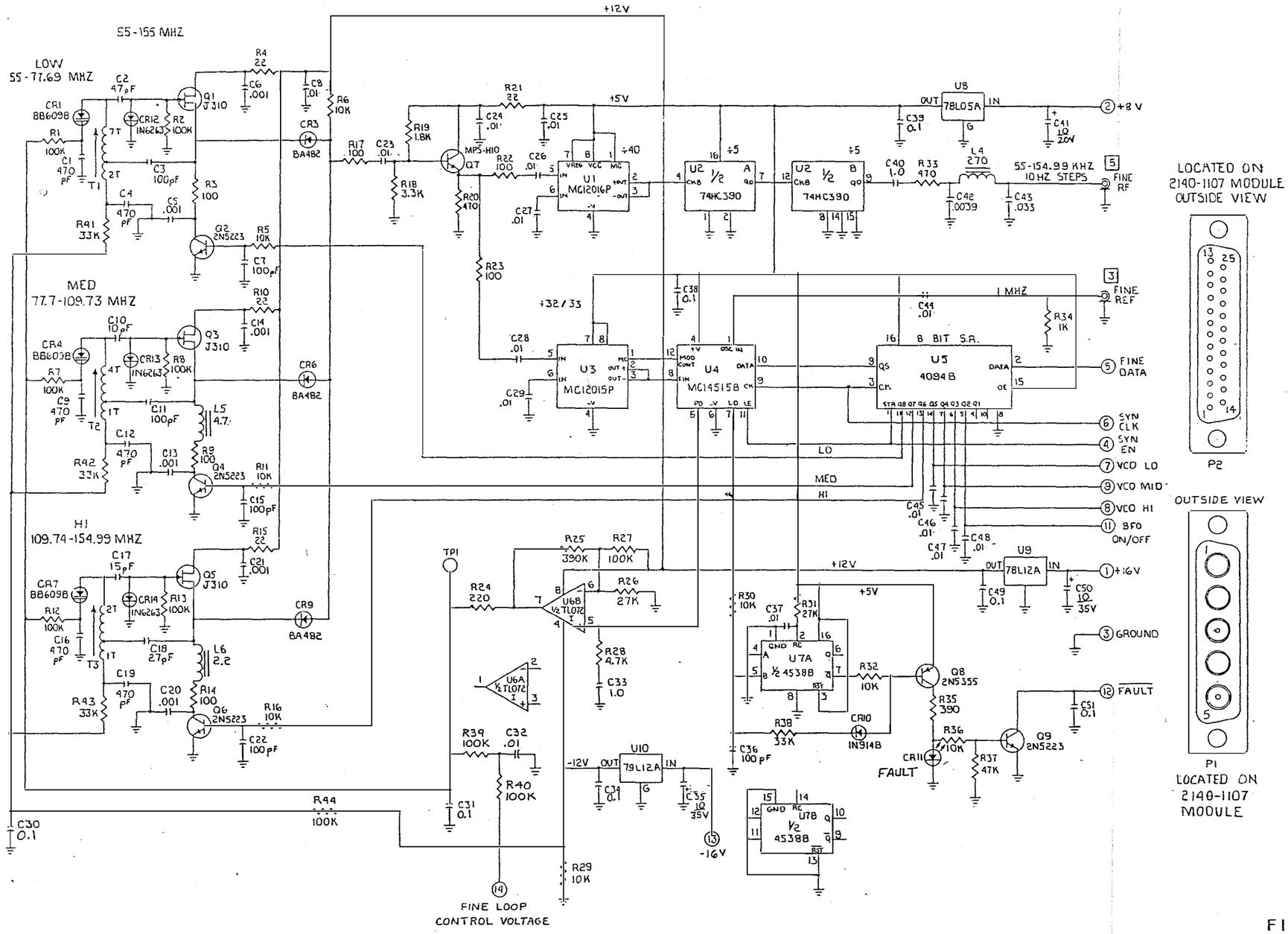


FIGURE 7.8-2
FINE LOOP MODULE SCHEMATIC

ADJUSTMENTS: No adjustments are required in normal service. In the event of component replacement or drift in characteristics, the following VCO adjustments may be made:

Connect an Oscilloscope through a 10 to 1 probe to TP1. Set the vertical controls to DC coupling, .5 V/division (Including the probe division)

T1

Tune the receiver to 10.02269 MHz with the IF shift set to 0.00 kHz. Observe the Oscilloscope and check if the voltage at TP1 is + 2 ± 0.5 VDC. If it is not, adjust T1 as required to make it so. Tune the receiver to 10.0000 Mhz and verify that the voltage at TP1 is less than -9 VDC.

T2

Repeat the above procedure except tune the receiver to 10.05473 and 10.02270 MHz respectively.

T3

Repeat the above procedure except tune the receiver to 10.09999 and 10.05474 MHz respectively.

The output level on the coaxial cable in position 5 should be greater than 0.25 V peak to peak into a 50 Ohm load.

CONNECTIONS:

P1, position 3 -- Reference input, 1 MHz
P1, position 5 -- Fine RF output from module to output loop

P2, Pin 1 -- + 16 VDC
P2, Pin 2 -- + 8 VDC
P2, Pin 3 -- Ground
P2, Pin 4 -- SYN EN (Synthesizer enable pulse to latch data)
P2, Pin 5 -- FINE DATA (Fine Loop data)
P2, Pin 6 -- SYN CLK (Synthesizer data clock)
P2, Pin 7 -- VCO LO
P2, Pin 8 -- VCO HI
P2, Pin 9 -- VCO MED
P2, Pin 11 -- BFO ON/OFF signal to BFO module
P2, Pin 12 -- Fault (Low in fault -- common with other faults in receiver)
P2, Pin 13 -- - 16 VDC
P2, Pin 14 -- Test point, Loop control voltage

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7.9 BFO MODULE

The BFO module supplies a phase locked signal from 445.01 to 464.99 kHz in 10 Hz steps to the Detector module. It uses the 1 MHz reference frequency from the Reference module and serial data from the CPU module.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.9-1 and 7.9-2 respectively.

The 1 MHz Reference frequency enters the Module via the coaxial cable in P1, position 2 where it is split for use by the 500 kHz L.O. circuit, a buffer amplifier to distribute this signal to other modules in the receiver, and the Multi-function Synthesizer chip U3.

The 500 kHz LO signal is used in the Detector module. This signal is obtained by passing the 1 MHz signal through NPN buffer amplifier Q4 which drives the pin 3 clock input port of divide-by-two counter U1A. Its output from pin 1 is filtered and placed on the 500 kHz L.O. output cable in P1, position 3.

The reference signal is also coupled through C25 to RF amplifier Q5 and associated components and is routed to the output on P1, position 1. This signal is amplified and buffered in this module rather than the Reference module due to the lack of enough coaxial cable connectors in the Reference module.

The VCO in this module is a Hartley type oscillator nearly identical with the VCOs found in the three Loop Modules. Its output range is 44.501 to 46.499 MHz in 1 kHz steps, and is composed of JFET Q1, transformer T1, varactor diode CR1, and associated components. NPN transistor Q3 acts as a switch to disable the VCO on computer command (through the Fine Loop Module shift register). Diode CR2 detects the oscillator signal to provide amplitude control and amplifier Q2 isolates the VCO from the other stages thus improving the stability of the oscillator.

U5 and U6A, both divide-by-10 counters, use the VCO output to generate a BFO frequency one one-hundreth the VCO frequency. This signal at 445 to 465 kHz in 10 Hz steps is filtered and output at P1 position 5 for use by the Detector Module. U6B is used to provide an auxillary BFO output for other types or models of receivers using the same module.

Dual Modulus Prescaler U2 is driven by the VCO frequency as well. This is a divide-by-64 or 65 device (selectable via pin 1). U3, which receives its frequency input from U2, is a multi-function synthesizer chip, incorporating programmable divider, reference divider and phase detector into a single package. In addition to the 1 MHz Reference, U3 also receives data, clock and enabling inputs from the CPU under program control. The pin 5 Phase Detector output of U3 is an analog voltage that is applied to the cathode of varactor CR1 in the VCO circuit, and serves as an error correction signal for the oscillator. The pin 7 Lock Detector output of U3 is normally high, pulsing low when the VCO is not locked on frequency. If the oscillator is not locked, U4A pin 7 goes low, biasing PNP Q6 to conduct, lighting the Fault LED CR4. As the Q6 collector goes high, NPN Q7 conducts, putting a low on the data FAULT line.

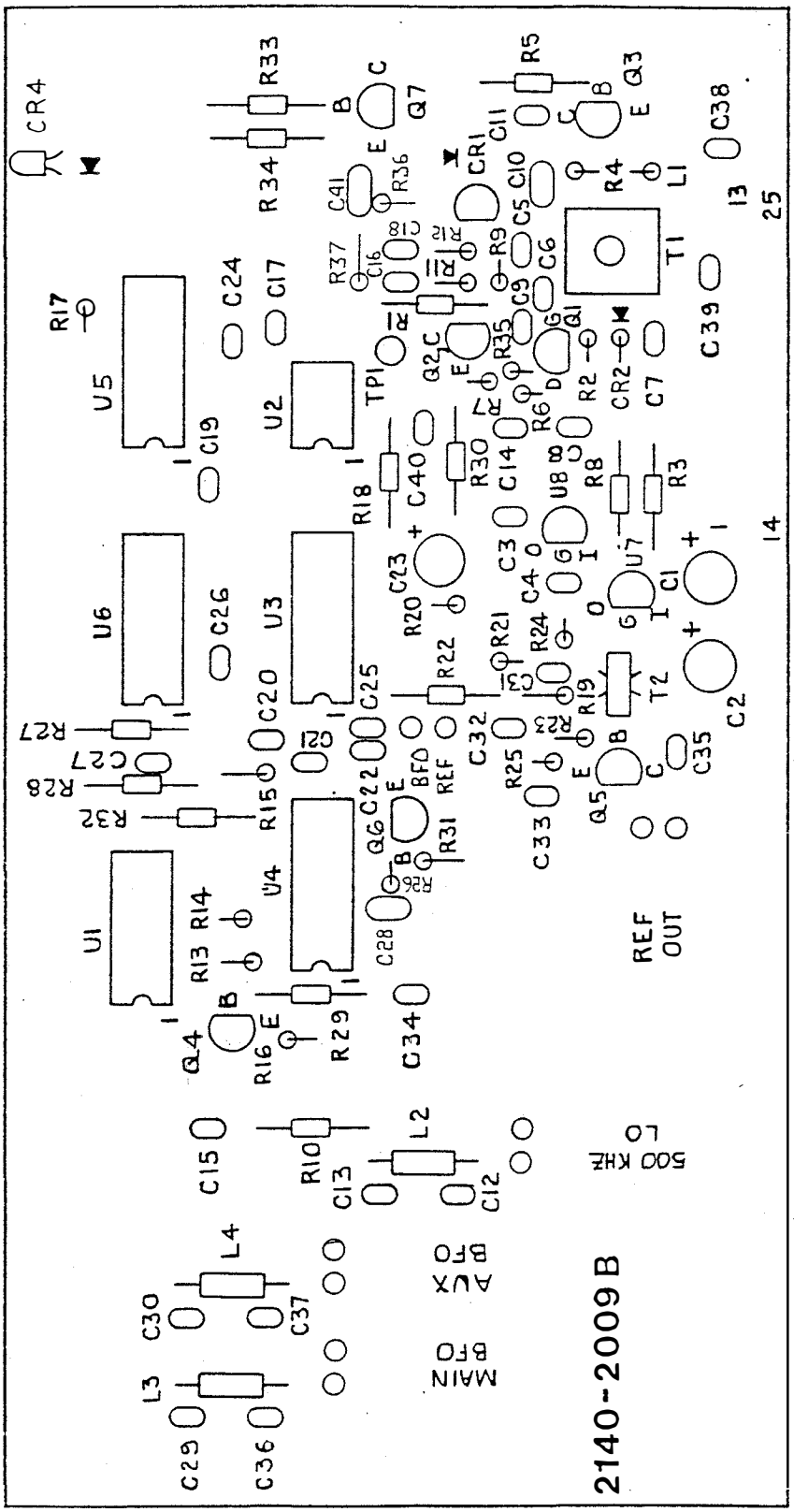

FIGURE 7.9-1
BFO MODULE ASSEMBLY DRAWING

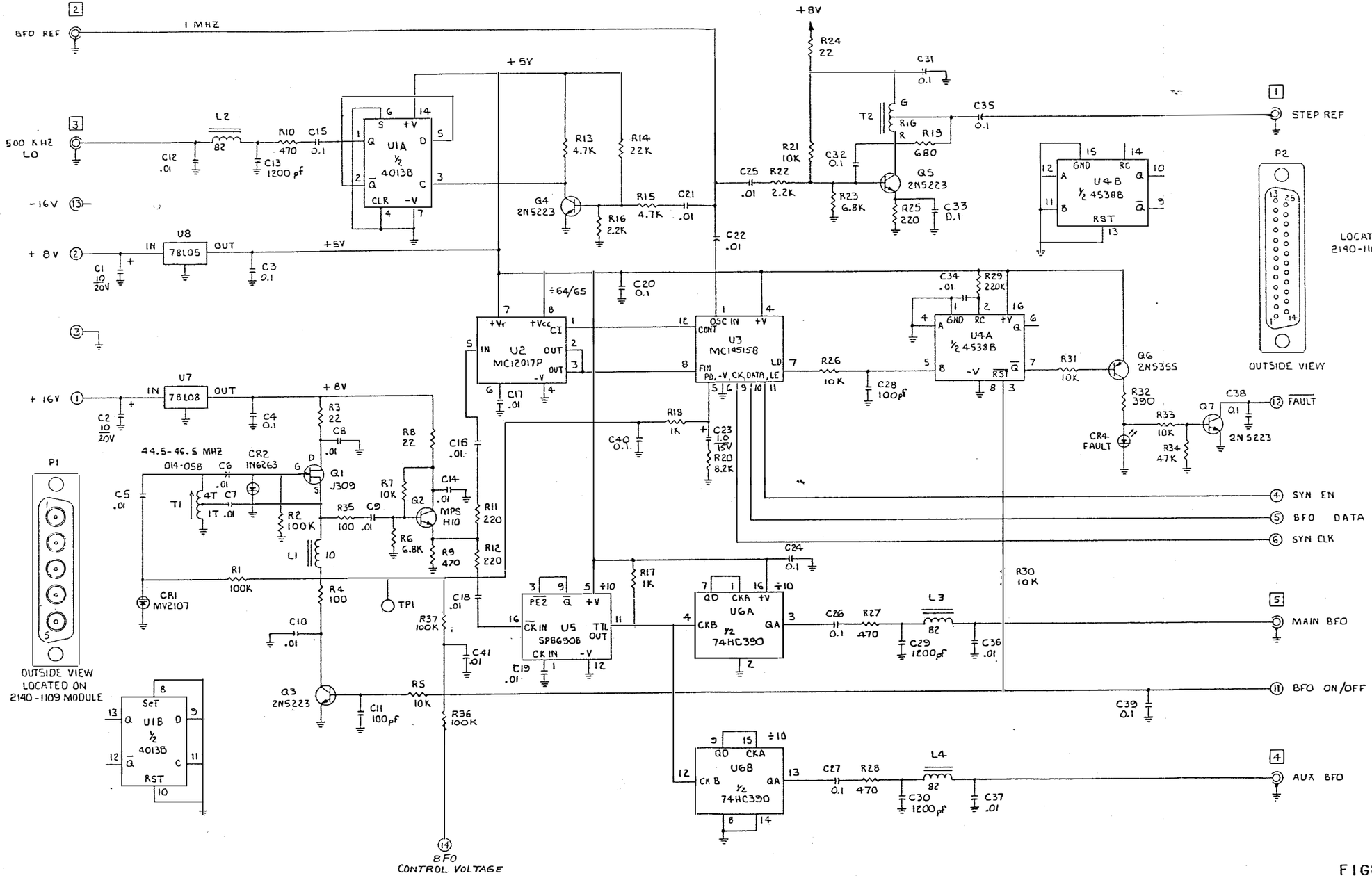

FIGURE 7.9-2
BFO MODULE SCHEMATIC

ADJUSTMENTS: No adjustments are required in normal service. In the event of component replacement or drift in characteristics, the following VCO adjustments may be made:

Connect an Oscilloscope through a 10 to 1 probe to TP1. Set the vertical controls to DC coupling, .5 V/division (Including the probe division)

T1

Tune the receiver to any frequency with the BFO offset and IF shift set to 0.00 kHz. Observe the Oscilloscope and check if the voltage at TP1 is + 2.5 ± 0.25 VDC. If it is not, adjust T1 as required to make it so.

Adjust the BFO Offset from -9.9999 to + 9.9999 kHz while observing TP1. The voltage should remain above + 2 VDC and below +3 VDC.

The output level on the coaxial cable in positions 4 and 5 should be between 0.45 and 0.90 V peak to peak into a 50 Ohm load at 445 to 465 kHz.

The output level on the coaxial cable in position 3 should be between 0.45 and 0.90 V peak to peak into a 50 Ohm load at 500 kHz.

CONNECTIONS:

P1, position 1 -- Reference output, 1 MHz to Step Loop
P1, position 2 -- Reference input, 1 MHz from Reference Module
P1, position 3 -- 500 kHz LO output, to Detector Module
P1, position 4 -- AUX BFO output, 455 kHz spare (for other model receivers)
P1, position 5 -- MAIN BFO output, 455 kHz to Detector module

P2, Pin 1 -- + 16 VDC
P2, Pin 2 -- + 8 VDC
P2, Pin 3 -- Ground
P2, Pin 4 -- SYN EN (Synthesizer enable pulse to latch data)
P2, Pin 5 -- BFO DATA
P2, Pin 6 -- SYN CK (Synthesizer data clock)
P2, Pin 11 -- BFO ON/OFF from Fine Loop module
P2, Pin 12 -- Fault (Low in fault -- common with other faults in receiver)
P2, Pin 13 -- - 16 VDC
P2, Pin 14 -- Test point, Loop control voltage

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7.10 REFERENCE and 2nd LO MODULE

The Reference module supplies the 1 MHz reference frequency to all synthesizer modules and the 40 MHz 2nd Local Oscillator signal to the 1st IF module.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.10-1 and 7.10-2 respectively.

Y1 is a temperature compensated crystal oscillator (TCXO) whose 10 MHz output is buffered by amplifier Q1 and applied to gate U1C. External reference signals (if used) are present at P1, on the coaxial cable in position 1, and drive buffer amplifier Q2. The output signal from Q2 is applied to gate U1A. The 1 MHz option Reference module is similar except that the frequency of the TCXO and external reference signals are 1 MHz.

If the external reference selector signal (REF SEL) applied to pin 9 of connector P2 is not low or grounded (as determined by the position of the rear panel reference selector switch), U1A is enabled and the external reference is selected. If the REF SEL signal is low, U1C is enabled and the internal reference is selected. The selected signal is gated by U1B and applied to U3A where it is divided in frequency by 10. The resultant 1 MHz signal used as a source of the reference frequencies used in the Step and Fine Loop Modules, as well as the BFO Module. The optional 1 MHz reference module has the divide by 10 circuit of U3A bypassed.

The undivided reference signal is applied to amplifier Q3 via the low pass filter comprised of C11, L1, and C12. This filter removes all harmonics of the reference signal thus providing a sinusoidal signal to the REF OUT coaxial cable in connector position 3 of P1.

The 1 MHz signal is applied to U4B and U4C that act as buffer amplifiers for the signals applied to the BFO and Fine Loop modules respectively. These outputs are also filtered to remove harmonics of the 1 MHz signal.

The 2nd L.O. signal is generated by the 20 MHz Voltage Controlled Crystal Oscillator (VCXO) comprised of crystal Y2, NPN transistor Q4, varactor CR2 and associated components. The output from Q4 is multiplied in frequency by two by Q5 and filtered by the tuned circuit consisting of T1 and C28. This signal at 40 MHz is further amplified and filtered by Q6 and T2/C33 before passing through the low pass filter comprised of C36, L4, and C37 and being applied to the 2nd Mixer of the receiver in the 1st IF module.

The 20 MHz VCXO signal is divided by 40 in U6 and applied to one input of U4D. The 1 MHz reference signal is divided by 2 in U3B and applied to the other input of U4D. U4D acts as a phase detector and corrects the frequency of the VCXO as required to make the 2nd LO output signal at 40 MHz exactly 40 times the frequency of the 1 MHz reference signal.

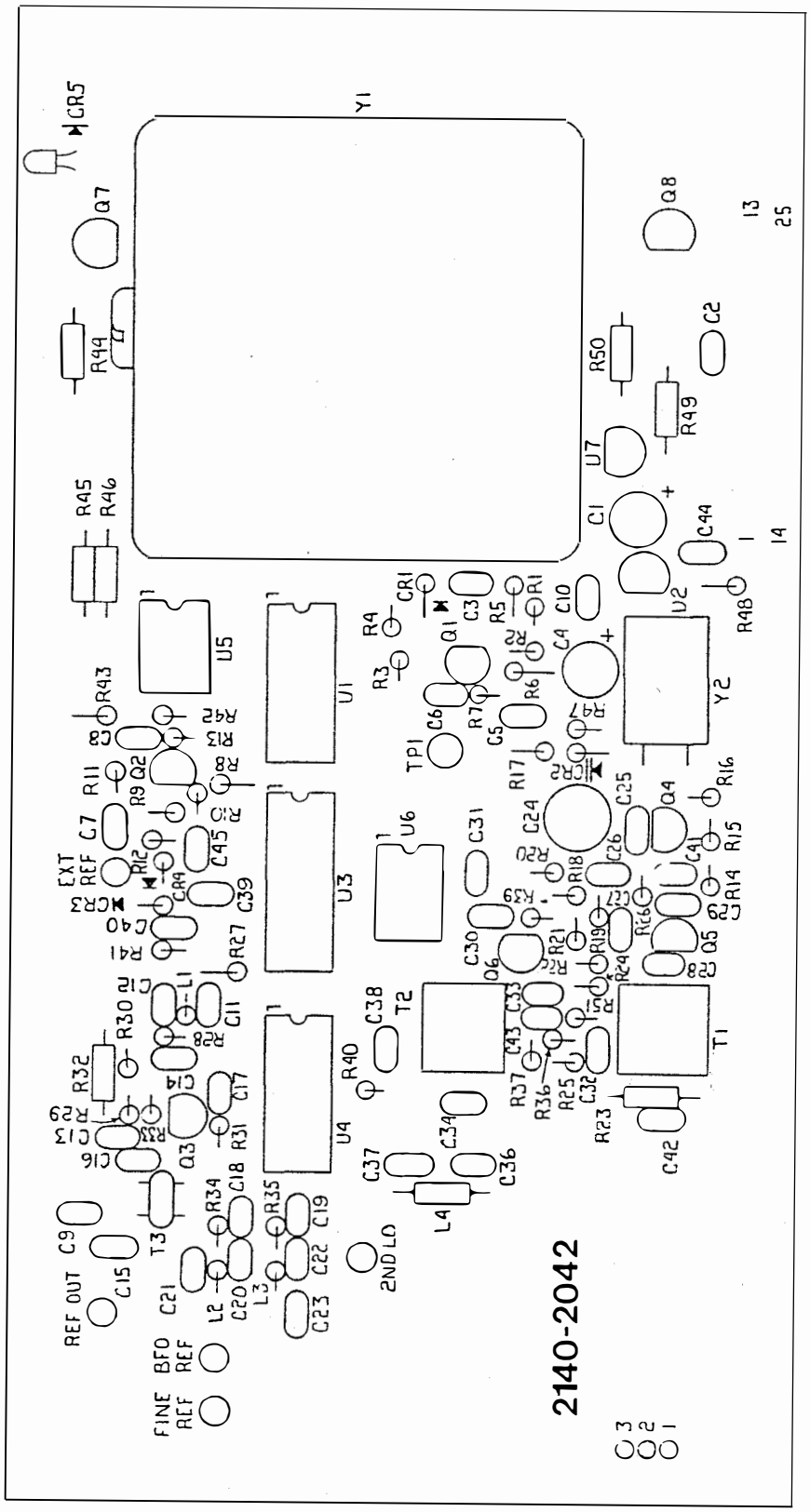

FIGURE 7.10-1
REFERENCE and 2nd L.O. MODULE ASSEMBLY DRAWING

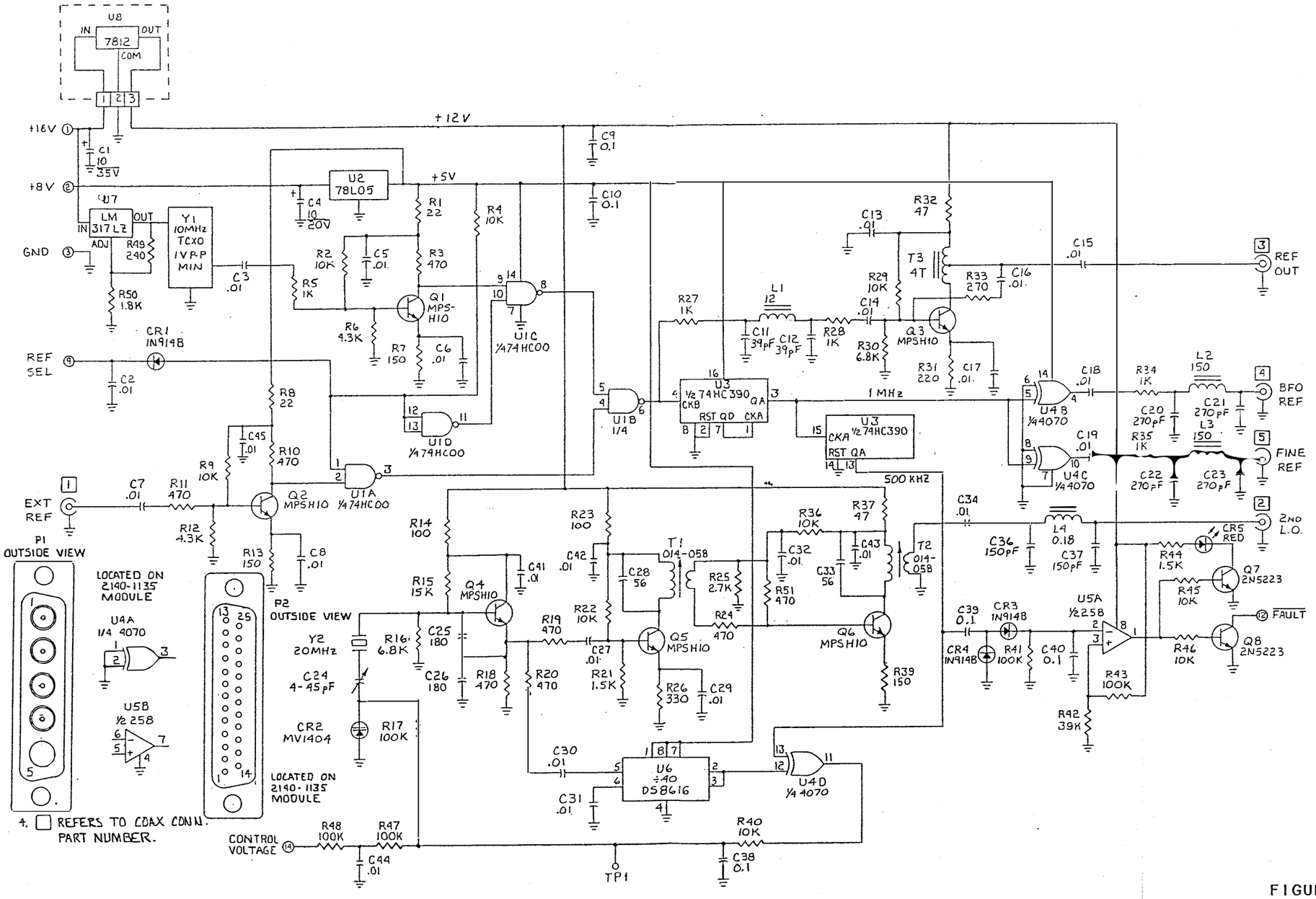

FIGURE 7.10-2
REFERENCE MODULE SCHEMATIC

ADJUSTMENTS:

Y1, adjustment screw

Insure that the rear panel REF SELECT switch is set to the INT position. Measure the frequency on the REF OUT coaxial cable in position 3 of P1. If this frequency is not exactly 10.000000 MHz (optionally 1 MHz), adjust the trimmer capacitor on Y1 through the hole in the top of the module. It will be necessary to remove the Phillips head screw to gain access to the adjustment and the screw should be replaced after the adjustment is made.

T1, T2

Adjust T1 and T2 for maximum 40 MHz output signal on the coaxial cable in position 2 of P1.

C24

Adjust C24 for a voltage of +2.5 ± 0.25 VDC on the testpoint connection to P2, pin 14.

CONNECTIONS:

P1, position 1 -- External Reference In, 10 or 1 MHz
P1, position 2 -- 2nd LO Out, 40 MHz
P1, position 3 -- Reference Out, 10 or 1 MHz
P1, position 4 -- BFO reference, 1 MHz
P1, position 5 -- Fine Loop Reference, 1 MHz

P2, pin 1 -- +16 VDC
P2, pin 2 -- + 8 VDC
P2, pin 3 -- Ground
P2, pin 9 -- Reference Selector (high for external, low for internal)
P2, pin 12 -- Fault (low for fault)
P2, pin 14 -- Test point, VCO control voltage

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7.11 CPU MODULE

The CPU module provides all the control signals to the various modules of the receiver from front panel control operations and data sent over the remote control bus.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.11-1 and 7.11-2 respectively.

U5 is a microprocessor chip performing all the receiver control functions. The application of DC power is sensed at pin 33 by the charge on C4 through R8. CR1 is used to discharge C4 quickly when power is removed. MOS-FET switch transistor Q1 is used by the processor to reset itself during a powerdown sequence by the port line from U6. This prevents inadvertent control states from being set into the receiver circuits.

The processor clock is crystal controlled by the 4.9152 MHz crystal (Y1) between pins 10 and 11 and associated components. Address lines A8 through A15 are found on pins 1 through 8. Pins 12 through 19 are bi-directional multiplexed Address and Data lines AD0 through AD7. Pin 21 is the Non-Maskable Interrupt line, which provides the indication of incipient loss of power by means of the voltage comparator comprised of U10a and associated voltage divider components.

Address Latch U9 provides EPROM U4 with address line 0 - 7 data under a (low) enable pulse at pin 11, which originates in the microprocessor. The Address Latch Enable (U5, pin 30) line controls both the Address Latch U9 and the Programmable Peripheral Interface (U6 pin 11), as well as the Panel Interface Module and the IEEE-400 or Parallel Bus Interface Module. This line is held high to enable data, and low to enable address information.

Program Memory is stored in U4, an erasable programable read-only-memory (EPROM). Chip Enable (CE/) is provided by the processor on address line A14. Output Enable is a low put on pin 22 by the processor Read line (U5 pin 32). This line also enables U6, 7 and 8, as well as other devices in the Panel Interface and Bus Interface Modules. U3 is an Address Decoder generating Chip Select signals for U6, 7 and 8, as well as other devices in the Panel Interface and Bus Interface Modules.

U6 is a programmable device known by the acronym RIOT (RAM, I/O ports, Timer) which upon processor prompt, interface (or in this case Read) program data to Output or control devices in the Preselector, 2nd IF, Detector, Step Loop, Fine Loop and BFO Modules. Timing is taken from the U5 pin 9 Clock output. I/O or Memory (IO/M) selection, in addition to Read and Write instructions, arrive directly from the microprocessor.

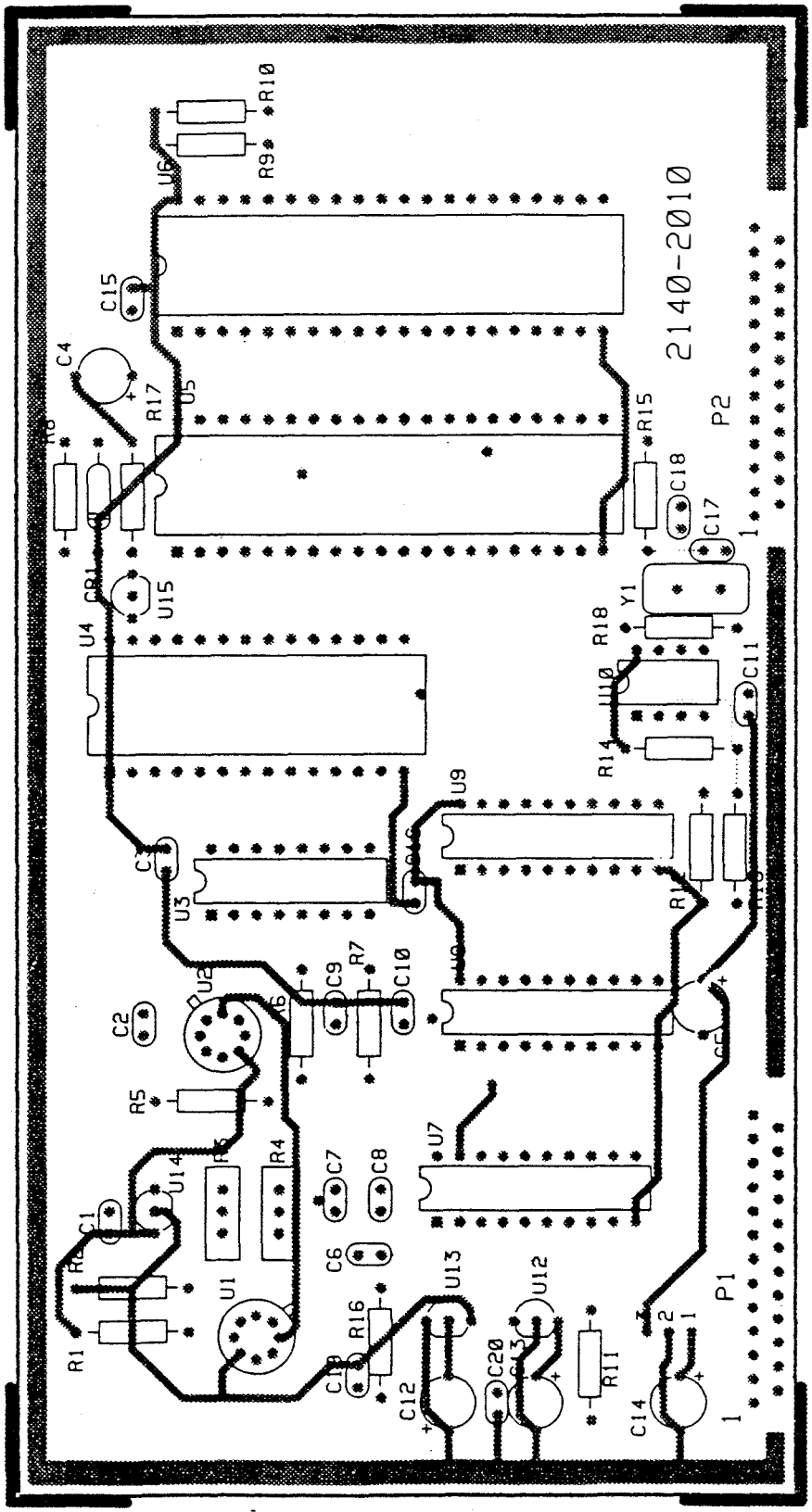

FIGURE 7.11-1
CPU MODULE ASSEMBLY DRAWING

	POWER SUPPLY CONNECTION PINS				
	I.C.	+5	GND	+12	-12
U5	NSC800	40	20		
U9	74HC573	20	10		
U3	74HC138	16	8		
U4	PRGM MeM	28	14		
U6	81C55	40	20		
U2	3130		4	7	
U8	ADC0804	20	10		
U7	DAC0832		10	20	
U1	3140			7	4
U10	258	8	4		

FIGURE 7.11-2
CPU MODULE SCHEMATIC

U7 (DAC0832) is a Digital to Analog Converter which provides an analog Manual Gain Control Voltage (0 to +5 VDC through op amp U1) to the Detector Module, from parallel digital data on the bus. Analog to Digital Converter U8 (ADC0804) receives an analog 0 to +5V Meter level from the Detector Module (via the Audio Board), and makes the digital equivalent data available to the multiplexed bus.

ADJUSTMENTS: NONE

CONNECTIONS:

P1

Pin 1	--	+8 VDC
Pin 2	--	+16 VDC
Pin 3	--	-16 VDC
Pin 4	--	ADR/DAT1
Pin 5	--	ADR/DAT3
Pin 6	--	ADR/DAT5
Pin 7	--	ADR/DAT7
Pin 8	--	A9
Pin 9	--	A2
Pin 10	--	A0
Pin 11	--	RD/
Pin 12	--	EN4
Pin 13	--	ALE
Pin 14	--	GROUND
Pin 15	--	MGC VOLTAGE
Pin 16	--	ADR/DAT0
Pin 17	--	ADR/DAT2
Pin 18	--	ADR/DAT4
Pin 19	--	ADR/DAT6
Pin 20	--	SPARE
Pin 21	--	A10
Pin 22	--	A1
Pin 23	--	METER ANALOG
Pin 24	--	BI
Pin 25	--	EN5

P2

Pin 1	--	FAULT/
Pin 2	--	INTA/
Pin 3	--	IO/M
Pin 4	--	SYN EN
Pin 5	--	STEP DATA
Pin 6	--	BFO DATA
Pin 7	--	BAND 1
Pin 8	--	BAND 3
Pin 9	--	BW 1
Pin 10	--	AGC EN
Pin 11	--	DET 0
Pin 12	--	DUMP
Pin 13	--	HOLD 0
Pin 14	--	INTR/
Pin 15	--	WR/
Pin 16	--	RESET
Pin 17	--	SYN CLOCK
Pin 18	--	FINE DATA
Pin 19	--	BAND 0
Pin 20	--	BAND 2
Pin 21	--	BW 0
Pin 22	--	BW 2
Pin 23	--	SPARE
Pin 24	--	DET 1
Pin 25	--	HOLD 1

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7.12 IEEE-488 BUS INTERFACE MODULE

The optional IEEE-488 Bus Interface module receives data from the remote control bus and makes it available to the CPU module.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.12-1 and 7.12-2 respectively.

The operations of this module are under the control of its own microprocessor, U2. Timing for this processor is provided by the 5.76 MHz crystal connected between pins 2 & 3, and is made available to U4 (the IEEE-488 Interface Controller) and U1 (the Port Expander) from pin 1 Timing Out. Bi-directional data to and from the CPU Module (via the mother board and U1) is applied to pins 27 through 34. Multiplexed address/data is output from U2 on pins 12 through 19. Pin 39 is the dedicated Request To Talk (TO) line. The Bus Interface Fault line is pin 35, which when high (true) forward biases Q1, pulling its collector low, thus enabling (lighting) Fault LED CR1. ALE/ pin 11 is the Address Latch Enable.

U1 is a RAM and Port Expander chip identical to U6 found in the CPU Module. As on U2, pins 12 through 19 are multiplexed address/data lines from the CPU module. Pins 21 through 28 are bi-directional data lines to the microprocessor. Rear panel Address switches input Service Request, Talk Enable, Listen Enable, and address ID selection data to pins 29 through 36 of U1 (and hence, to U2). Bus Interface, Read, Write and Address Latch Enable are applied to U1 on pins 8 through 11. Pin 37 (RINT/) is an interrupt request line to the Interrupt Controller.

U6 is an Address Latch device. It simply latches (transfers) address data from the data bus to U3 (EPROM) Program Memory on command (LE/, pin 11). Program memory data is read onto the bus from data lines D0 through D7.

The IEEE-488 Interface Controller, U4, regulates sequencing of control and data intelligence (under U2 control) to and from the rear panel IEEE-488 bus connector (via U5 & 7). Address/data bus lines D0 through D7 are found on pins 12 through 19. Pin 1 is the bus transceiver control line (high to transmit, low to receive). U5 and U7 are Bus Transceivers interfacing U4 and the rear panel (through the Mother Board). U5 handles data information, and U7 handles control information.

ADJUSTMENTS: NONE

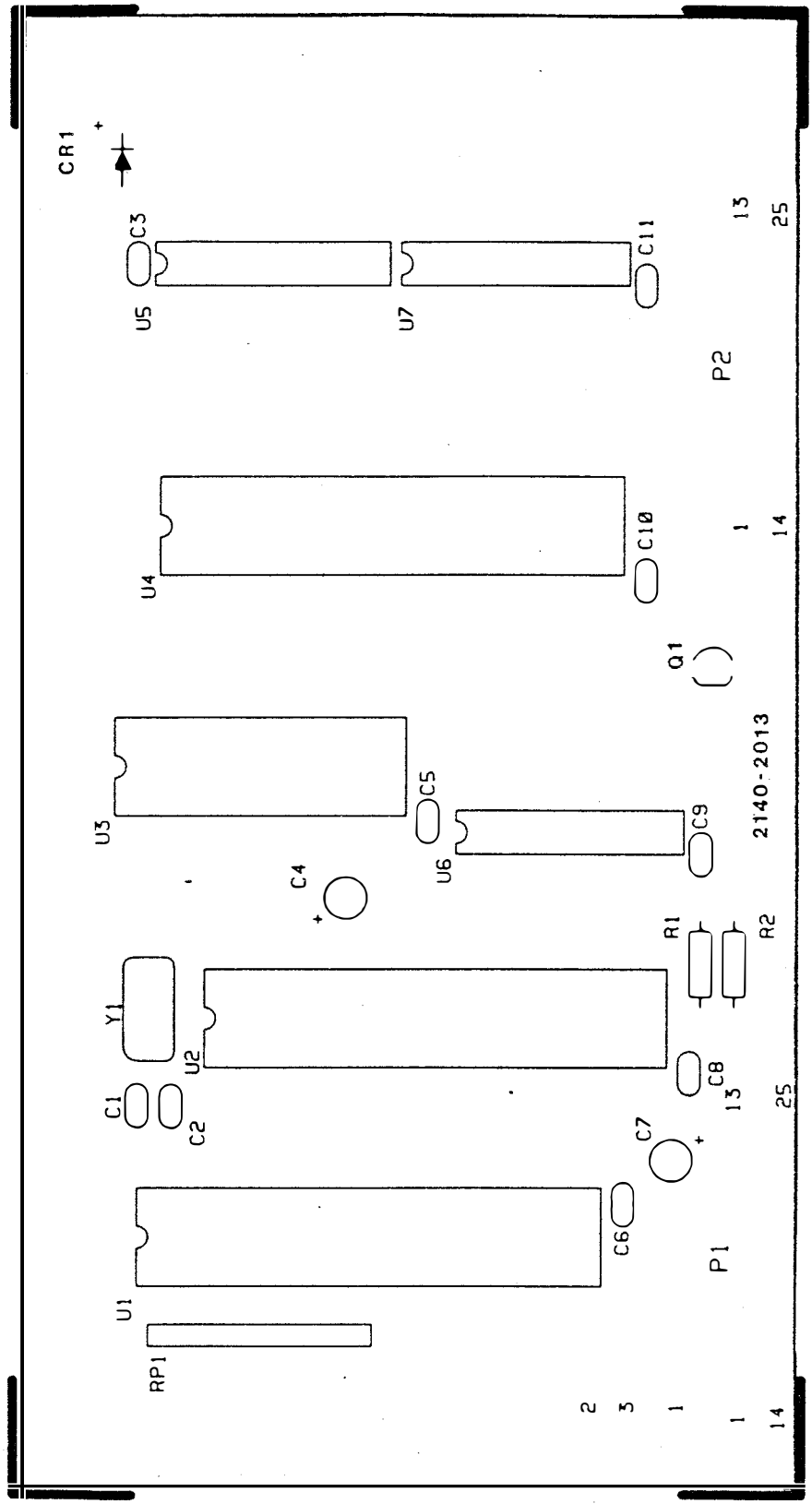


FIGURE 7.12-1
IEEE INTERFACE MODULE ASSEMBLY DRAWING

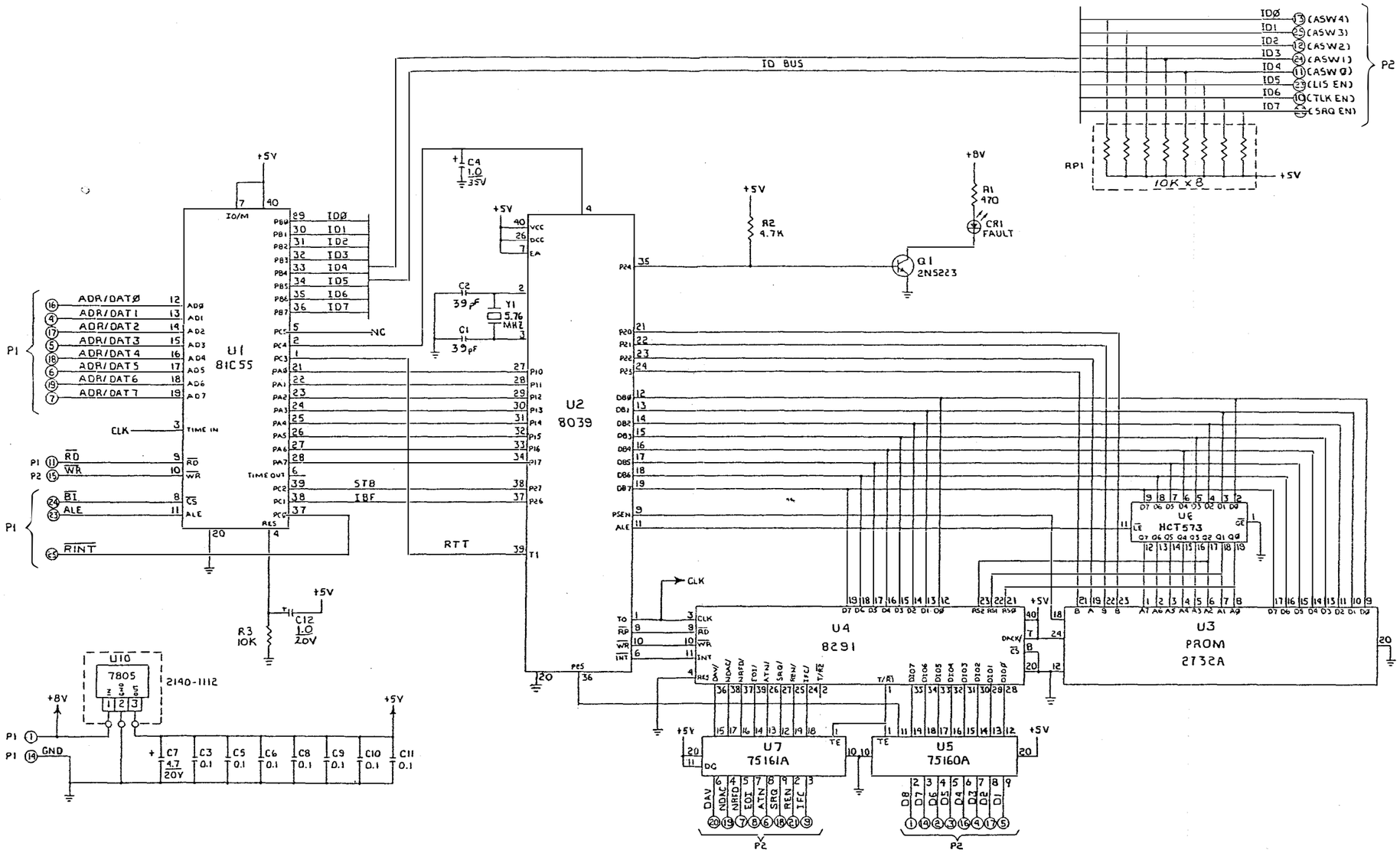


FIGURE 7.12-2
IEEE INTERFACE MODULE SCHEMATIC

7.13 IEEE-488 BUS CONNECTOR BOARD

Refer to the component assembly drawing and the schematic diagram for this board shown in Figures 7.13-1 and 7.13-2 respectively.

The IEEE-488 Bus Connector board provides the interconnection between the external bus connector and the internal ribbon cables and also provides for mounting of the two addressing switches. This board is only used when the optional IEEE-488 Bus Interface Module (and appropriate software) is installed. The connector switches (S1 and S2) are 8-position DIP configured, and set IEEE-488 bus status for Service Request Enable, Talk Only Enable, and Listen Only Enables, in addition to selection of one of thirty-one possible Address codes. Interconnection of the DIP switches and bus connector are through a ribbon cable to the Mother Board connection to the Bus Interface Module.

ADJUSTMENTS: NONE

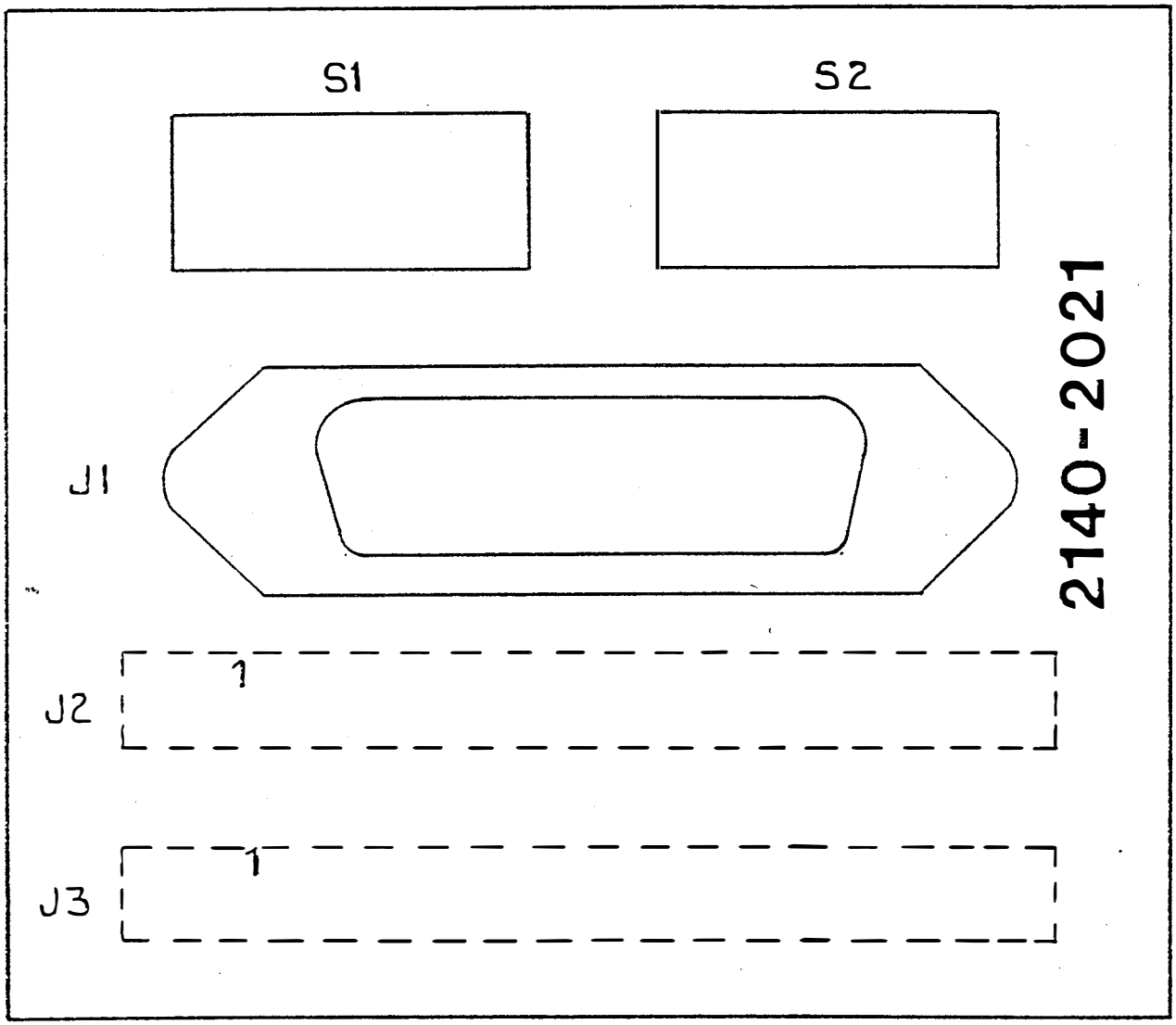


FIGURE 7.13-1
IEEE-488 BUS CONNECTOR BOARD ASSEMBLY DRAWING

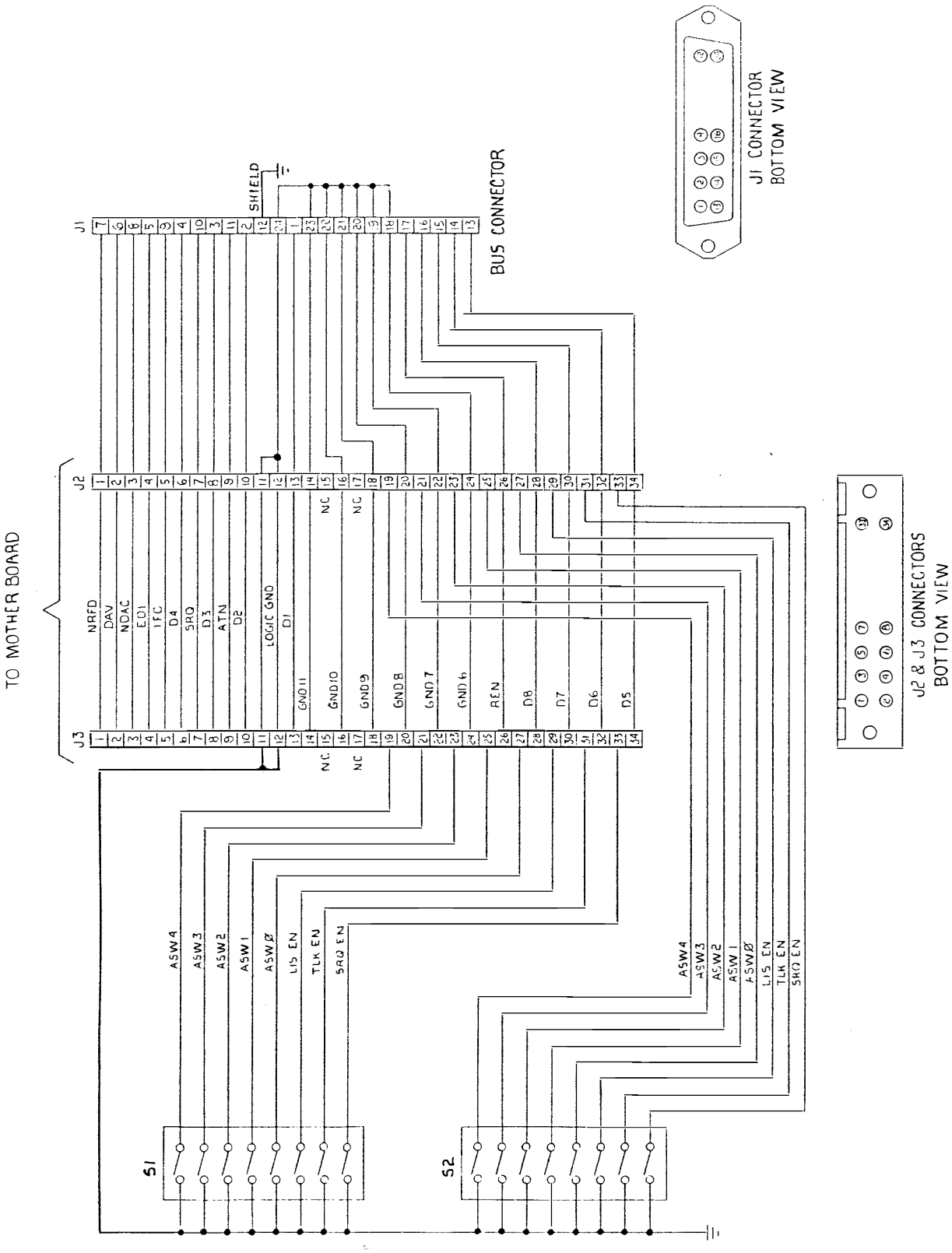


FIGURE 7.13-2
IEEE CONNECTOR BOARD SCHEMATIC

7.14 PARALLEL BUS INTERFACE MODULE

The standard Parallel Bus Interface module is composed of a number of data latches used as storage registers that are triggered to capture the data when the select code applied to the bus matches the select code set into the unit by the internal jumper plugs. The bus latches the data at a rate determined only by the bus and is independent of any operation in the CPU module. The CPU reads the contents of these registers as memory locations on its own timing cycle and uses this data to control the frequency synthesizer and other receiver functions.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.14-1 and 7.14-2 respectively.

Receiver data to be used by the bus is latched into U5 and U6 on pins 2 through 9 and is read into the 16-bit bus under an enable command (logic low) on pin 1 of both latches, delivered to it via bus transceiver U16 pin 12. U5 and U6 timing (CLK) inputs are driven by NOR gate U14, which in turn is input by the unit write (WR/) line, bus interface (BI/) line and an A0 line.

Incoming bus data is captured (latched) by U1-U4 and U7-U10. These latches are clocked by decoder U13 via the strobe line on the bus when the unit select address is true. The latch bank into which data is written is determined by the state of data lines D14 and D15.

The CPU module reads or writes data to the latches under the control of CPU address lines A0 through A2 via decoder U12. Data is read onto the multiplexed data bus from pins 12 through 19 (of the latches), at the CPU timing rate.

Data transfer from the bus into these "storage registers" is ultimately dependent upon a matching of Select Codes (i.e. is this the intended target unit on the bus?). Select Codes are set in a binary number determined by the placement of jumper plugs which impart a One or a Zero value (logic high or low, respectively). Bus transceiver U16 inputs select code data to 8-bit comparator U17 which will output a logic low when a match between the input code and Select Code is sensed. This low signal on pin 19 is used to turn off Q2 and Q5 which enables the pullup transistors on ID code bus transceiver U18 (via pin 11, PE -- pullup enable) and the data latches (U11 and U15) respectively. The low signal from U17, pin 19, also enables the zero state jumpers connected to ID code bus transceiver U18.

U18 is set to always output data to the bus via the connection of pin 1 (TE -- transmit enable) to the +5 VDC line. When the unit is not selected by means of the signal from U17, the pullup transistors are disconnected (by means of pin 11 of U18 being low) and all data inputs are held high (with the pull down transistors being turned off). When the unit is selected, the pullup transistors in U18 are enabled and the data inputs are allowed to be at the level determined by the ID Code jumpers.

The bus data transceivers U11 and U15 are allowed to place data on the bus lines only when both the correct select code is received (via Q5) and the bus direction line is set to the transmit mode (via Q4). Otherwise, the bus data transceivers are set to receive data.

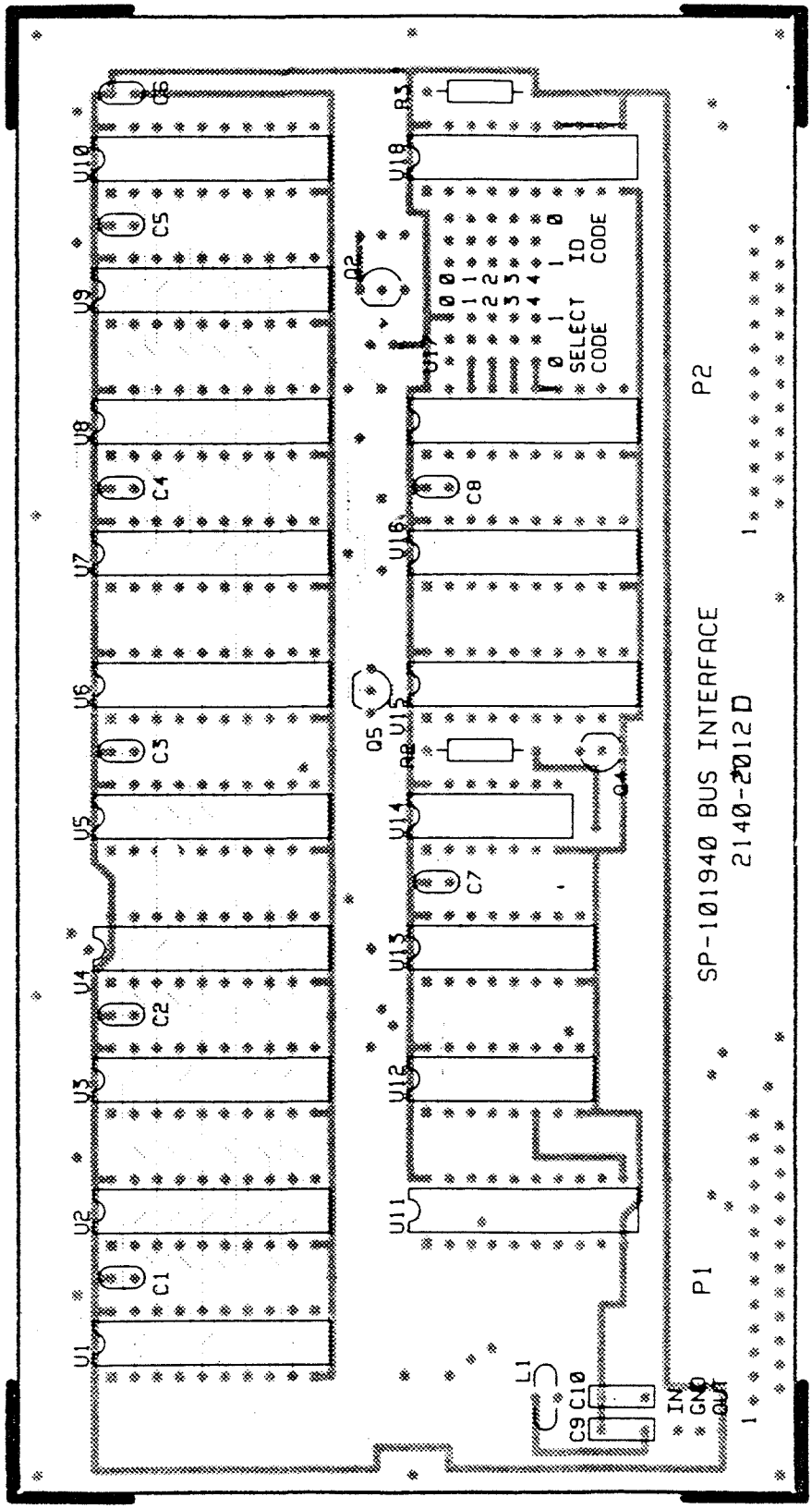


FIGURE 7.14-1
PARALLEL BUS INTERFACE MODULE ASSEMBLY DRAWING

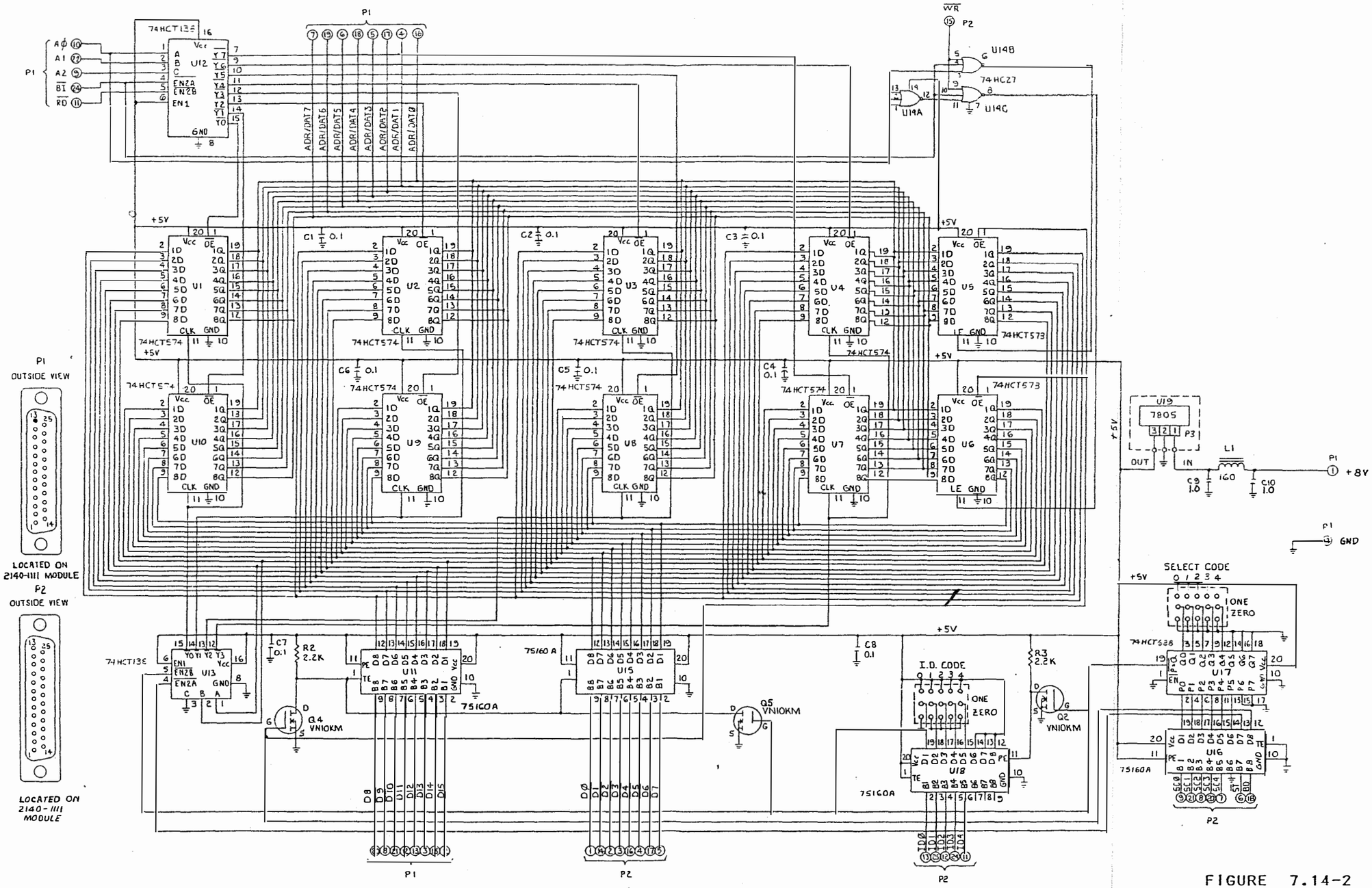
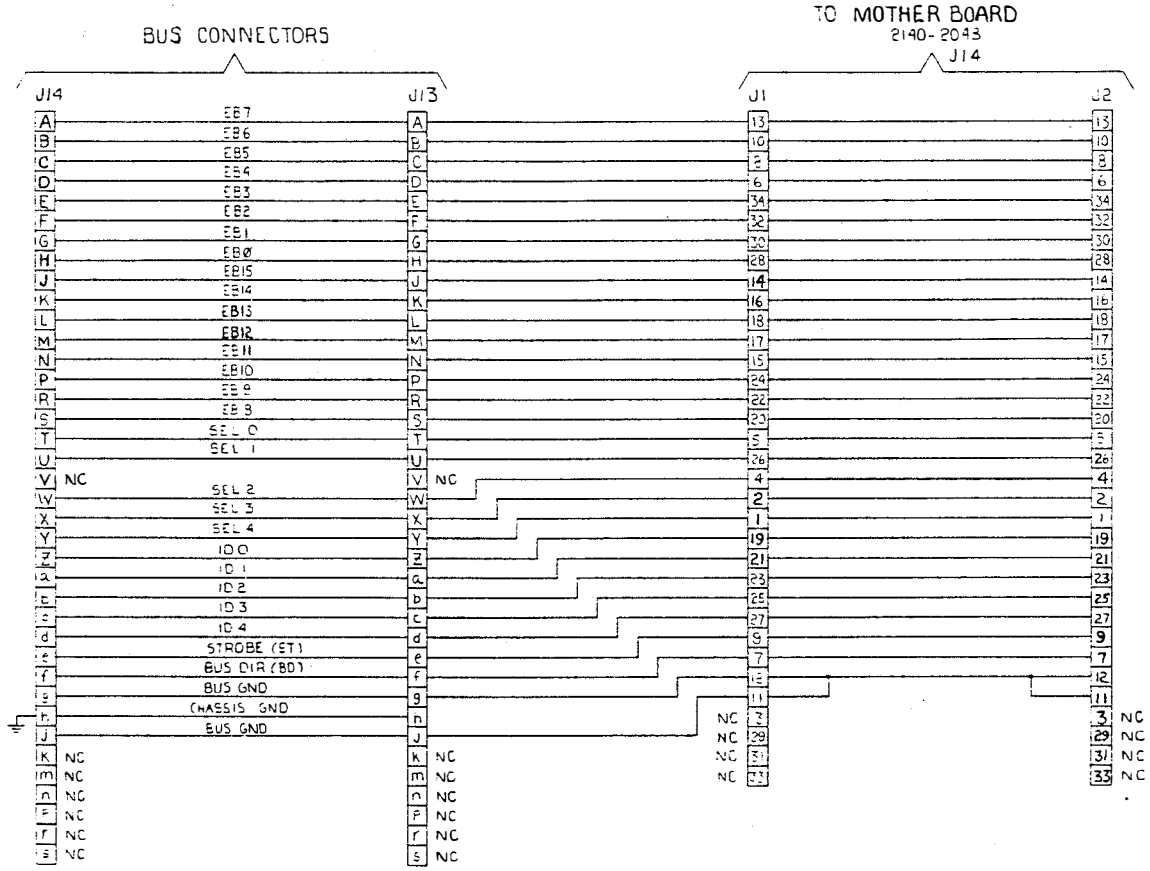


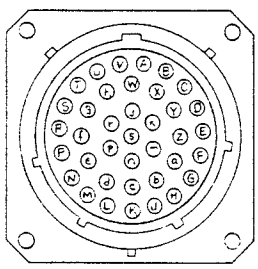
FIGURE 7.14-2
PARALLEL BUS MODULE SCHEMATIC

7.15 PARALLEL BUS CONNECTOR BOARD (Serial No. A125 and earlier)

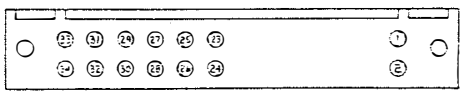
Refer to the schematic diagram for this board shown below. No assembly drawing is shown as this board consists only of two each of two types of connectors mounted on opposite sides of the circuit board. This board is obsolete with units manufactured in September 1985 and later.

The Parallel Bus Connector board provides the interconnection between the external parallel bus connector and the internal ribbon cables to the Parallel Bus Interface Modules when this remote interface is installed.





FRONT VIEW
J13 &J14 CONNECTORS



FRONT VIEW
J1& J2 CONNECTORS

FIGURE 7.15-1
BUS CONNECTOR BOARD SCHEMATIC DIAGRAM

Starting with special order units with serial numbers of A126 and later and specifing the modified ESSI bus, the schematic diagrams shown below and the bus receiver board assembly diagram on the next page apply.

The connector board provides for connections to the modified ESSI bus while the associated bus receiver board provides for conversion of the differential signals for bus direction and strobe to the logic levels required by the parallel bus interface board.

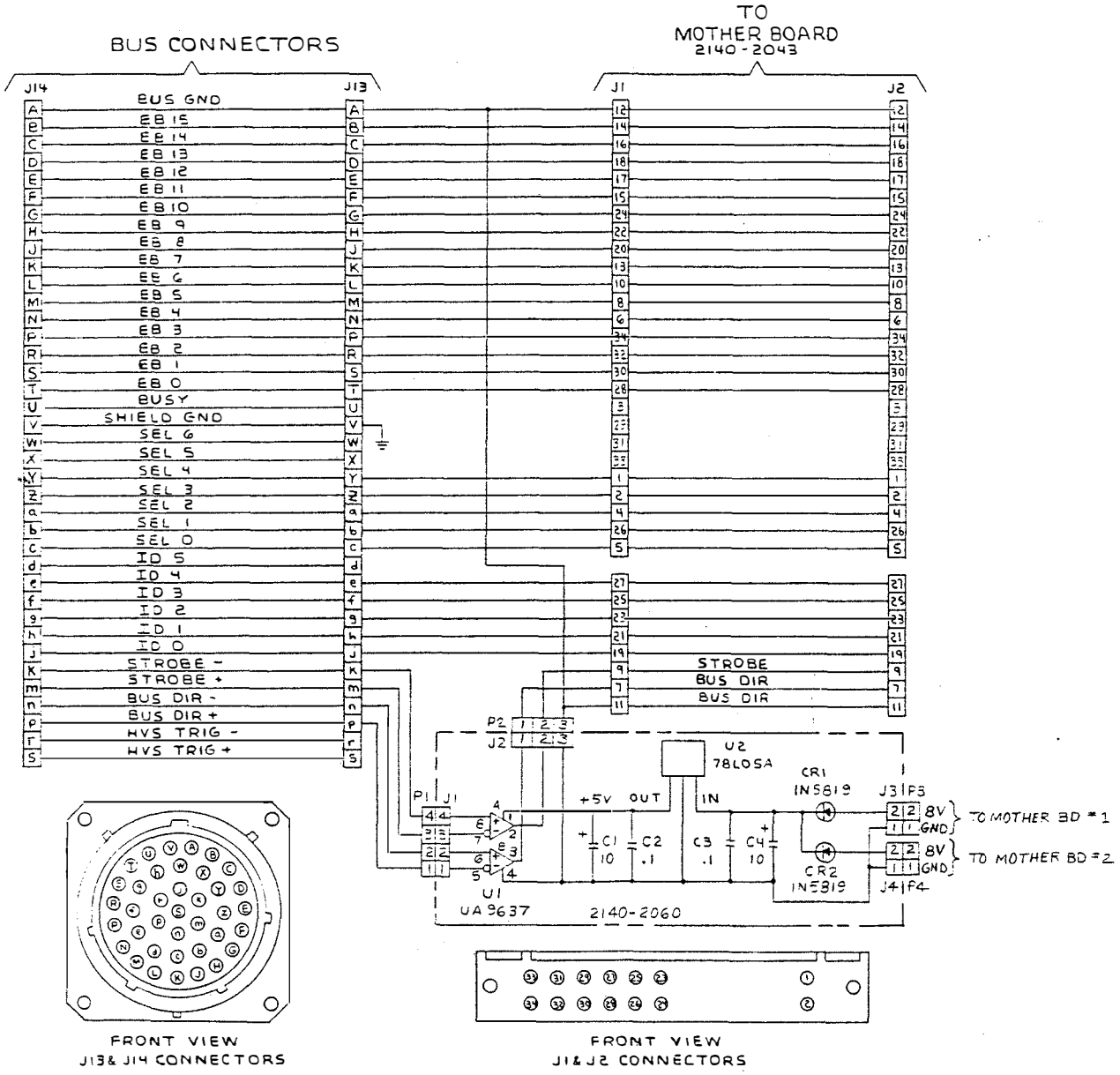


FIGURE 7.15-2
ESSI BUS CONNECTOR AND RECEIVER BOARDS SCHEMATIC DIAGRAM

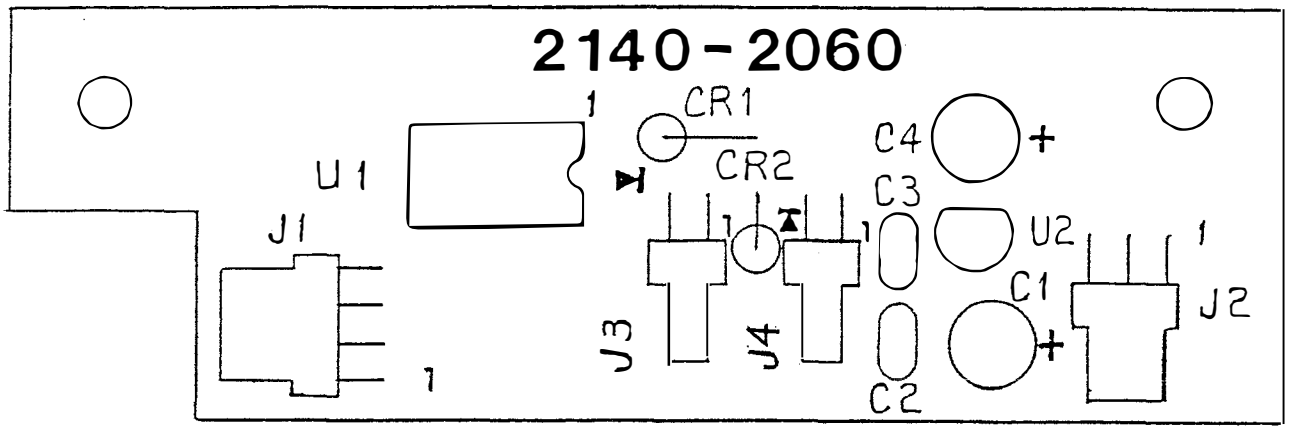


FIGURE 7.15-3
ESSI BUS RECEIVER BOARD ASSEMBLY DRAWING

7.16 POWER SUPPLY MODULE

The power supply module furnishes DC voltages to all modules from the AC power line. This power supply is a switching mode type to minimize power dissipation and heat build-up in the power supply and in the receiver chassis. All inputs and outputs are extensively filtered to prevent RF noise from the power supply from appearing in the signal path.

The power supply is packaged in a completely shielded module similar to the other modules in the receiver although the power supply module is slightly thicker than the other modules. This shielding serves also to isolate any RF noise generated in the power supply from the signal path.

Refer to the component assembly drawing and the schematic diagram for this module shown in Figures 7.16-1 and 7.16-2 respectively.

AC input voltage is applied to pins 2 and 5 of the high voltage input connector. This connector is similar to the coaxial connectors in many of the other modules except for the type of contact pin used. CR14 is a metal oxide varistor (MOV) used to clip high voltage transients that may be present.

The AC line radio frequency interference (RFI) filter is comprised of capacitors C28, C29, C30, bifilar wound dual RF choke L9, capacitors C25, C26, C27, separate RF chokes L7 and L8, and capacitor C21. Neon bulb DS1 and associated resistors is used to indicate a fault in the module under the control of optically isolated thrysistor U1 and will be discussed later.

Bridge rectifier CR13 converts the AC input voltage to DC and stores the resultant DC voltage in capacitors C20 and C22. Voltage selector switch S1 configures the rectifier for a full wave bridge in the 220 V position and for a full wave voltage doubler in the 110 V position. MOV device CR12 clips any high voltage transients that have passed through the initial MOV device while thermistors RT1 and RT2 limit the surge current into the capacitors when the unit is first turned on and the thermistors are cold or at the receiver ambient temperature.

The rectified DC voltage is applied to the primary winding (Pins 10 and 2) of power transformer T1 through field effect transistor (FET) Q4 and current sense resistor R26. The switching of Q4 under the control of integrated circuit U2 changes the DC voltage back into AC at a frequency of approximately 65 KHz with a controlled on-off ratio so as to regulate the effective voltage appearing across each of the transformer secondary windings. Diode CR2 together with C1, R8, and R9 provide transient suppression when Q4 is turned off.

When the unit is first turned on, FET Q1 is turned on by means of the voltage developed across R5 and R39. Zener diode CR1 limits the bias voltage applied to Q1 and Q2 is turned off initially. The conduction through Q1 provides an operating voltage for U2 which then pulses Q4 on and off to create the AC voltage. As a voltage is developed across the secondary winding between Pins 1 and 11 of T1, the DC voltage developed by CR3 across C24 then turns Q2 on and Q1 off. The operating voltage for U2 then is applied through CR5 and CR6. CR4 insures that the base-emitter junction of Q2 is never reverse biased by more than 0.7 volts.

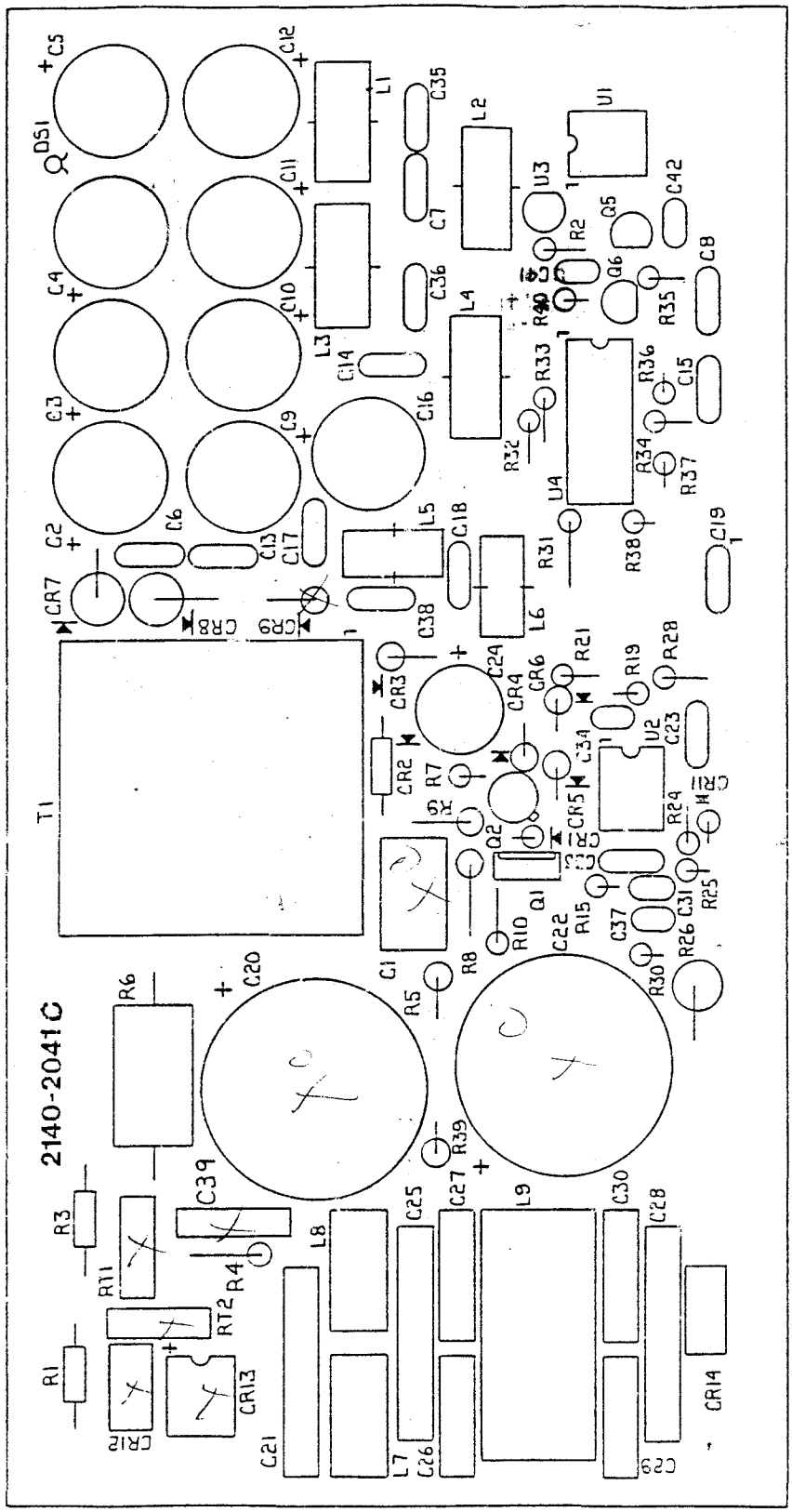


FIGURE 7.16-1
POWER SUPPLY ASSEMBLY

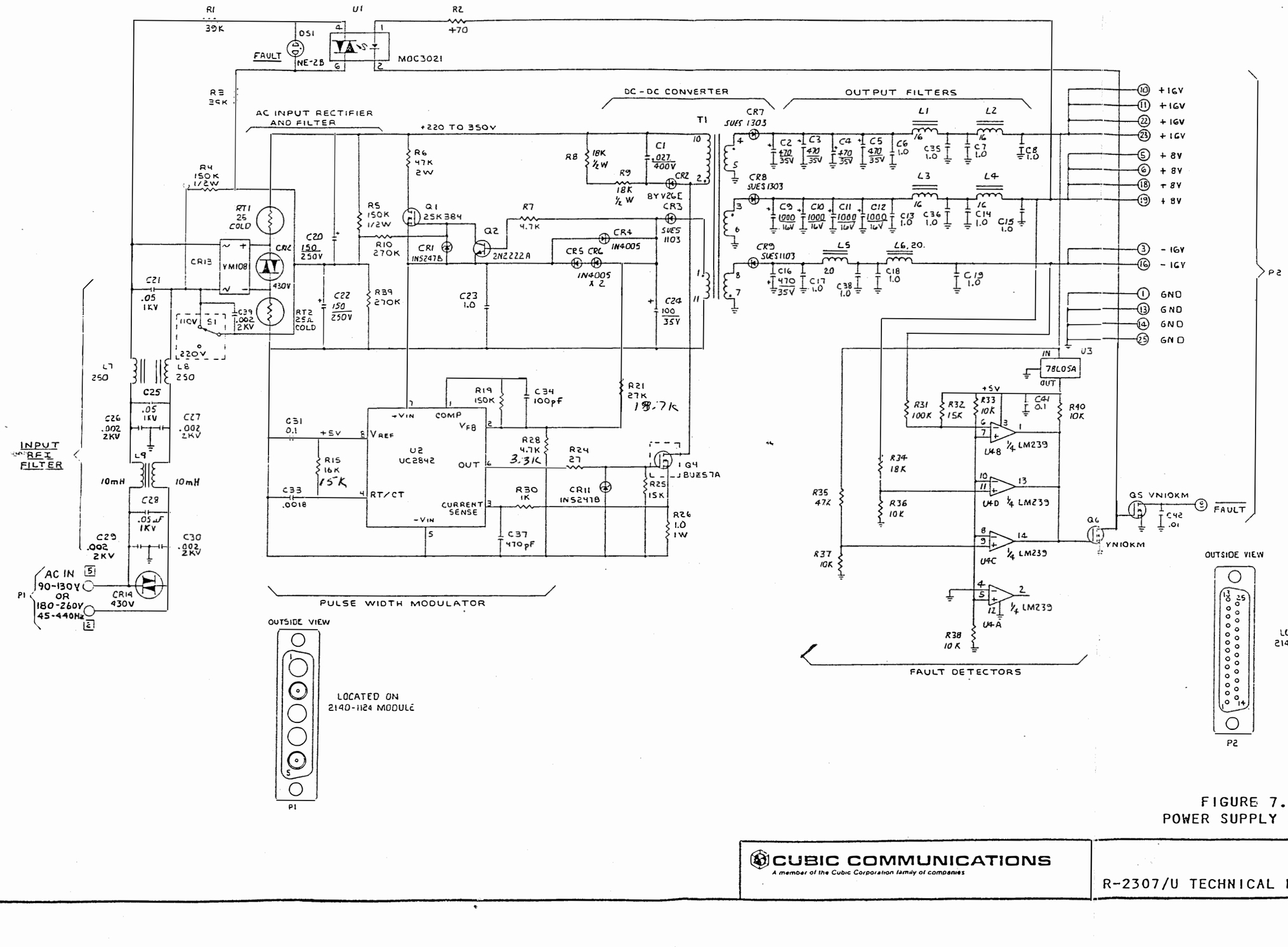


FIGURE 7.16-2
POWER SUPPLY SCHEMATIC

The DC voltage across C24 is sensed by integrated circuit U2 and is used to control the duty cycle of the AC voltage across the primary of T1. The regulation of this voltage thus serves to control the other voltages as desired for use by the other modules in the receiver. The voltage across R26 is sensed to insure that the peak currents through Q4 are not excessive such as those that may result from a component failure in the power supply or a short circuit on the output of the power supply.

Each of the three desired output voltages is developed in essentially a similar manner. Refering to the connections shown to the right of transformer T1 on the schematic diagram, each supply consists of a half wave rectifier diode, a set of energy storage capacitors, and an RFI filter consisting of alternate capacitors and inductors. These rectifier convert the AC voltage appearing across the transformer back into DC at the desired lower voltages. Thus the transformer, switching transistor, and output rectifiers serve to form a DC to DC converter.

Each of the separate output voltages is sensed by comparison with a reference voltage developed by voltage regulator U3. The separate comparator sections of U4 are summed in an OR connection at the input (gate) of Q6. Any voltage sensed to be below its fault threshold will cause a low voltage at the gate of Q6 thus turning it off and turning Q5 on. This causes the FAULT / at pin 8 of P2 to be low and signal a fault to the CPU module.

The fault condition resulting in the turning off of Q6 would also result in the light emitting diode (LED) section of U1 to be turned off, thus turning off the thyristor section and allowing DS1 to become illuminated. With the unit operating normally, Q6 is turned on thus allowing conduction through the LED section of U1 and DS1 is not illuminated. Note that operating DS1 from the AC line in this manner allows a fault to be indicated (at least on the module) with the no other components operating.

ADJUSTMENTS REQUIRED: NONE

CONNECTIONS AND VOLTAGE LIMITS:

AC Line -- Pins 2 and 5 of P1 (High Voltage Inserts)
100 to 130 or 200 to 260 VAC RMS

Ground -- Pins 1, 13, 14, and 25 of P2

+16V -- Pins 10, 11, 22, and 23 of P2
+15 to +17 VDC

-16V -- Pins 3 and 16 of P2
-15 to -17 VDC

+8V -- Pins 5, 6, 18, and 19 of P2
+7.5 to +8.5 VDC

Fault -- Pin 8 of P2
Low indicates fault condition (common with other faults)

THIS PAGE IS INSERTED FOR USER NOTES

7.17 PANEL INTERFACE MODULE

The primary functions of the Panel Interface Module are to sense operation of keypad and adjustment knob controls, provide drive signals for the front panel displays, and provide retention of channel data and current status of the receiver during power off-on cycles. Refer to the component assembly drawing and schematic diagram for this module shown in Figures 7.17-1 and 7.17-2 respectively.

Function decoding is accomplished by way of U1, a one of eight decoder which selects the proper chip into which to latch data via address lines A8 - A10. The EN5 signal and the IO/M signal from the CPU module enable the decoder.

Data for the display light emitting diodes on the front panel is latched into integrated circuits U2 through U5. During a decode, the data present on data lines AD0 - AD7 is strobed on the rising edge of the decode pulse into 8-bit latches U2 through U5. The information is multiplexed at a 2 millisecond rate under control of interrupts in the CPU module. U2 through U4 are used to latch the data corresponding to individual segments of each of 3 display digits (or elements) while U5 is used to select one of 6 groups of digits. Each group of 3 digits is normally selected for 2 milliseconds every 16 milliseconds while the bright digit used during adjustment knob operations is selected for 6 milliseconds each 16 milliseconds.

The keypad encoder U6 provides column strobe output signals to and row input sensing from the front panel keypad. When a key press is sensed, an interrupt is generated on the data available output (pin 13) that sets flip/flop U15. This generates an interrupt through the interrupt controller U11 which alerts the CPU to read the keypad data on the data outputs AD0 through AD4. The scan rate of the keypad controller is determined by C3 and is approximately 60 Hz. The keypad debounce delay is determined by C2 and is set for a delay of approximately 50 milliseconds.

Integrated circuit U8 serves several functions. When selected by U1, this IC latches data from the CPU module. MET0 and MET1 (pin 19 and pin 18) are utilized as select lines for signals on the front panel audio board that are to be used for bargraph metering purposes. The INH line (pin 17) serves as a mute control for audio to the headphone jacks on the front and rear panels and is also applied to the audio board.

Two outputs from U8 are used to control the operation of the power down memory, U12. One output (pin 16) selects the recall operation on power up while another output (pin 15) directs U12 to store the current data on power down.

The encoder direction set output from U8 (pin 14) sets the state of the direction flip/flop U15 to the correct polarity when the receiver is powered up. Subsequent pulses from the front panel shaft encoder set or reset this flop/flop which alerts the CPU, through the interrupt controller U11, that the shaft encoder is being turned and in which direction.

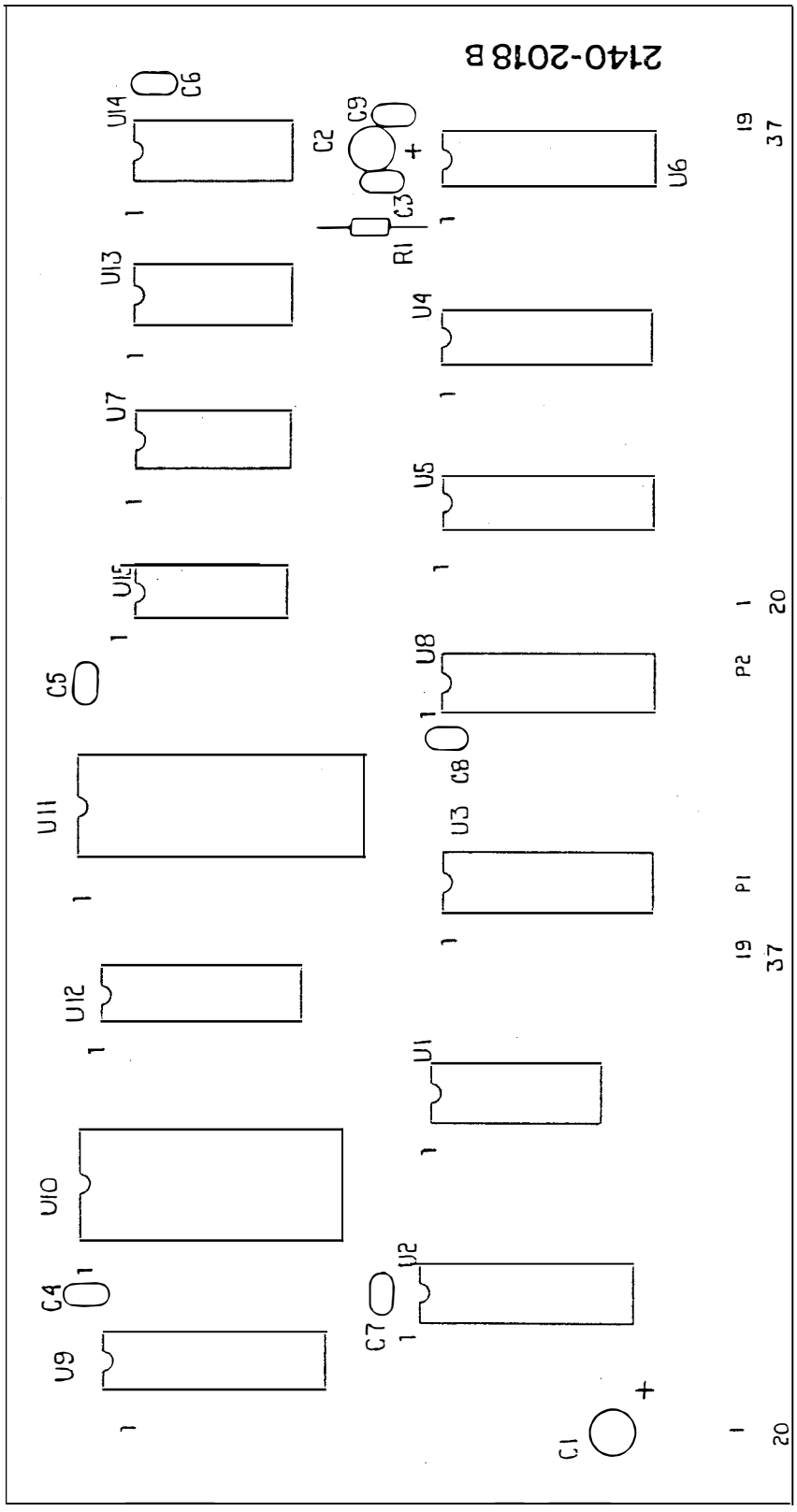


FIGURE 7.17-1
PANEL INTERFACE ASSEMBLY DRAWING

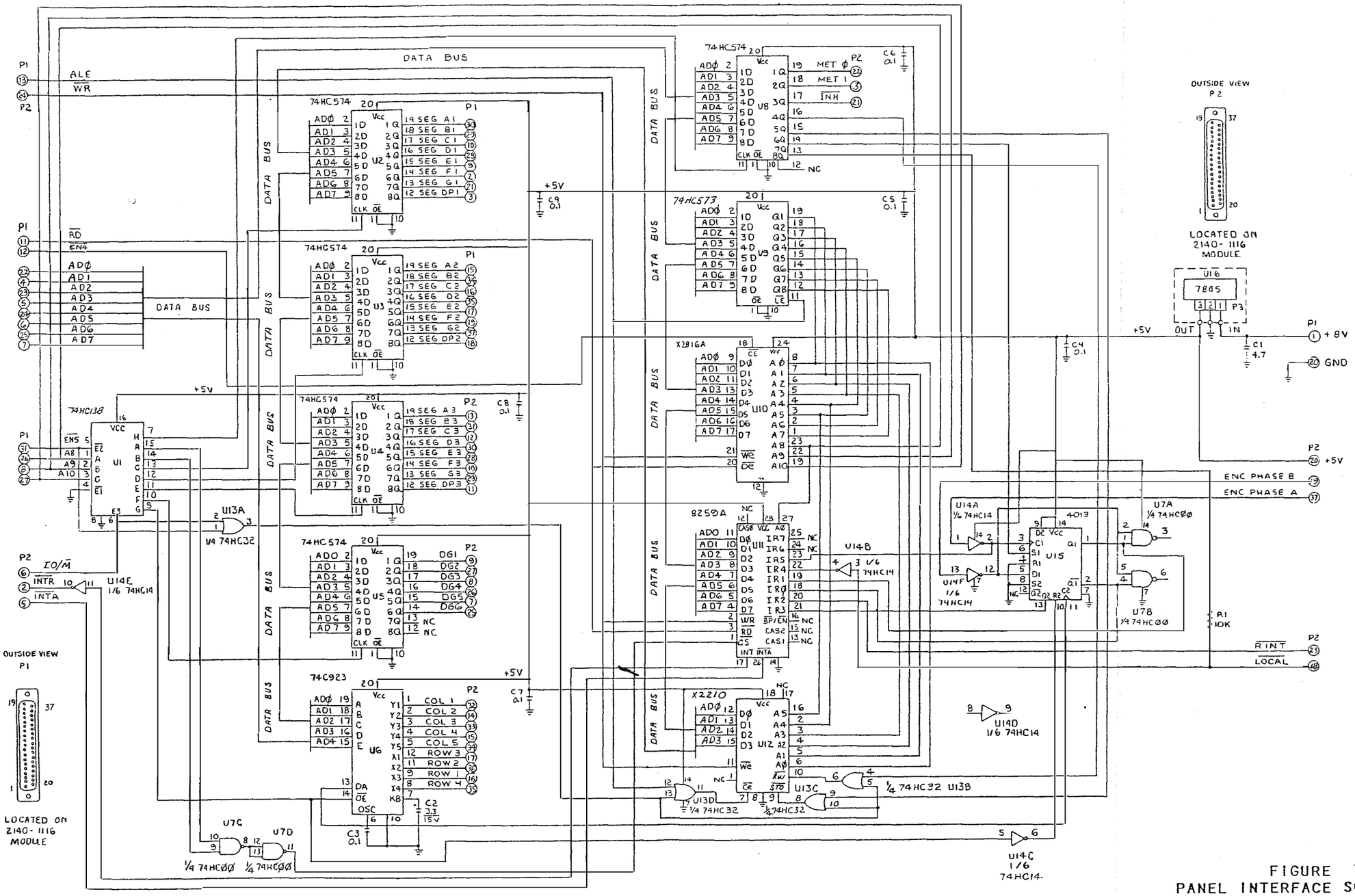


FIGURE 7.17-2
PANEL INTERFACE SCHEMATIC

The local/remote output from U8 (pin 13) sends pulses through resistor R1 to the interrupt controller, U11. When the switch is closed (local) no interrupts are generated and the CPU sets the local mode of operation. Opening the switch (remote) alerts the CPU to the remote mode of operation. Keyboard operations are disabled and the Remote operation is enabled in this mode.

Latching of address lines A0 through A7 is performed by U9 when the ALE (address latch enable) signal strobes the low order address lines into U9 from the address/data bus. Channel memory functions are accomplished by latching of address locations from U9 and chip select of U10 (pin 18) from function decoder U1 along with a low logic level on pins 20 or 21 during memory read and writes respectively. Address lines A8 through A10 are brought directly to U10.

Interrupt controller U11 is used to interrupt the CPU when a keypad operation, adjustment knob operation, or local/remote switch actuation occurs. The CPU then reads tha data from this chip to determine which operation has occurred and then acknowledges the interrupt to reset the controller.

The non-volatile random access memory (NOVRAM) U12 utilizes logic signals to control the presentation of four bit data bits on the bus. This prevents U12 from presenting its data on the bus during an active address cycle. Address selection is accomplished using address inputs A0 - A5 which are latched by U9. Pin 11, the write enable (WE/) controls the direction of data flow. Memory store and recall operations are directed by inputs latched in U8. Current data regarding frequency, mode, and other parameters are always written to the temporary memory portion of this chip. When an imminent loss of power is sensed, the CPU directs this temporary data to be stored. After a power up operation, the CPU calls for a recall operation to recall data from the non-volatile to the temporary memory portion of this chip. This data can then be read and used to restore the operation of the receiver to the conditions existing just before the power loss.

ADJUSTMENTS REQUIRED: NONE

THIS PAGE IS INSERTED FOR USER NOTES

CONNECTIONS AND SIGNALS:

P1

1	+8 VDC input
2	Segment F1 2 ms multiplex
3	Segment DP1 2 ms multiplex
4	AD1 Address and data bus
5	AD3 Address and data bus
6	AD5 Address and data bus
7	AD7 Address and data bus
8	A9 Address bus
9	Segment E1 2 ms multiplex
10	Segment C1 2 ms multiplex
11	RD/ Low for read
12	EN4/ Low for Channel Memory En.
13	ALE High for address true
14	No Connection
15	Segment A2 2 ms multiplex
16	Segment C2 2 ms multiplex
17	Segment E2 2 ms multiplex
18	Segment DP2 2 ms multiplex
19	Segment F2 2 ms multiplex
20	Ground
21	Segment G1 2 ms multiplex
22	AD0 Address and data bus
23	AD2 Address and data bus
24	AD4 Address and data bus
25	AD6 Address and data bus
26	A8 Address bus
27	A10 Address bus
28	Segment D1 2 ms multiplex
29	Segment B1 2 ms multiplex
30	Segment A1 2 ms multiplex
31	EN5/ Low for Port Enable
32	No Connection
33	No Connection
34	Segment B2 2 ms multiplex
35	Segment D2 2 ms multiplex
36	No Connection
37	Segment G2 2 ms multiplex

P2

1	No Connection
2	INTR Low for interrupt
3	MET1 Meter select (Binary)
4	No Connection
5	INTA Low for interrupt acknowledge
6	IO/M Low for memory, high for IO
7	DG5 2 ms out of 16 high
8	DG3 2 ms out of 16 high
9	DG1 2 ms out of 16 high
10	Segment F3 2 ms multiplex
11	Segment DP3 2 ms multiplex
12	Segment C3 2 ms multiplex
13	Segment A3 2 ms multiplex
14	Column 2 Keypad
15	Column 4 Keypad
16	Row 1 Keypad
17	Row 3 Keypad
18	Local Switch Ground for local
19	Encoder Phase B
20	+ 5 VDC
21	INH Low to inhibit audio
22	MET0 Meter select (Binary)
23	RINT Remote Interrupt
24	WR/ Low for write to memory or IO
25	DG6 2 ms out of 16 high
26	DG4 2 ms out of 16 high
27	DG2 2 ms out of 16 high
28	Segment E3 2 ms multiplex
29	Segment G3 2 ms multiplex
30	Segment D3 2 ms multiplex
31	Segment B3 2 ms multiplex
32	Column 1 Keypad
33	Column 3 Keypad
34	Column 5 Keypad
35	Row 4 Keypad
36	Row 2 Keypad
37	Encoder Phase A

7.18 DISPLAY BOARD

The display board contains all of the front panel display components and drivers for these components. The data is latched to the Display board from the Panel Interface module and converted to current levels necessary to drive the display LEDs.

Refer to the component assembly drawing and the schematic diagram for this assembly shown in Figures 7.18-1 and 7.18-2 respectively.

The display is organized as 3 groups of 6 digits having 8 segments each. Normal intensity digits are turned on for 2 milliseconds every 16 milliseconds (a refresh rate of 62.5 Hz) while the intensified digit (when enabled) is turned on for 6 milliseconds every 16 milliseconds.

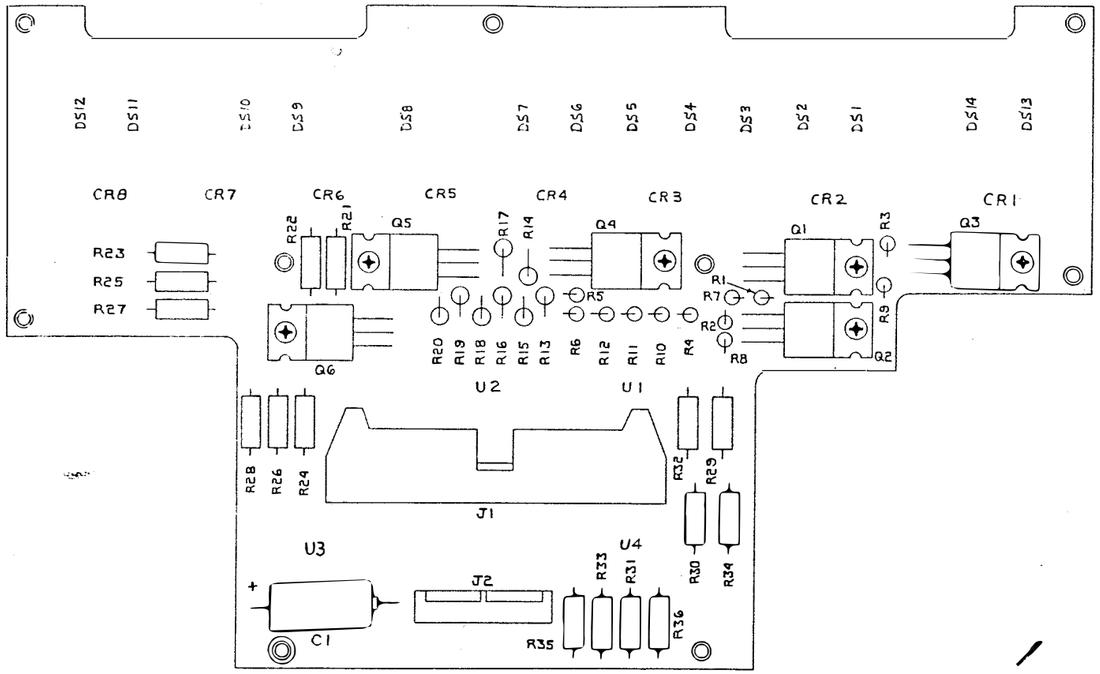
U1 through U4 are 8-channel drivers that receive Panel Interface Module data on J1. U1 serves as a driver for the PNP digit group driver transistors Q1 through Q6. These transistors, when biased to conduct, enable a group of 3 digits (i.e. Q1 enables DS1, 7 and 13).

Segment drivers U2 through U4 will, upon receipt of data, place logic levels on their parallel outputs necessary to illuminate the selected segments of the display elements. Since only one digit group at a time is enabled, the data from one segment driver is directed to only one digit. Bargraph displays CR1 and CR2 as well as annunciators CR3 through CR8 are treated as segments of digits. The resistors serve to control the current to each display LED.

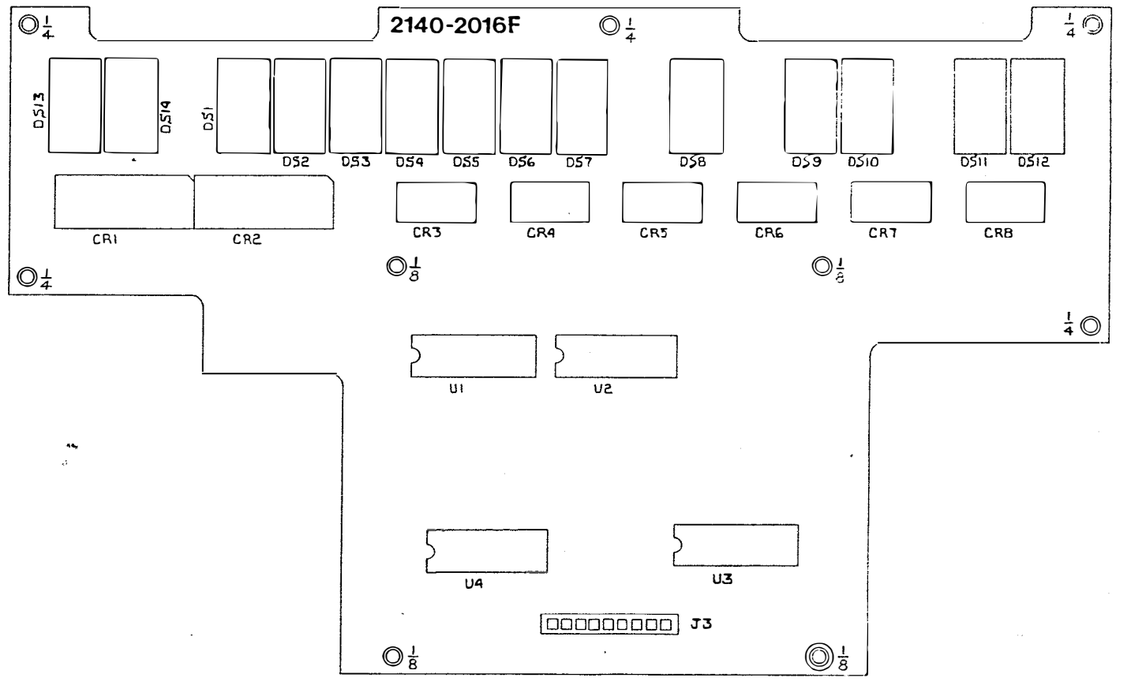
ADJUSTMENTS REQUIRED: NONE

CONNECTIONS: J1 ONLY

PIN	SIGNAL	PIN	SIGNAL
1	+8 RTN (Ground at power supply)	18	A1
2	+8 RTN (Ground at power supply)	19	DP3
3	DP2	20	+ 8 VDC
4	DP1	21	G3
5	G2	22	+ 8 VDC
6	G1	23	F3
7	F2	24	DG6
8	F1	25	E3
9	E2	26	DG5
10	E1	27	C3
11	D2	28	DG4
12	D1	29	D3
13	C2	30	DG3
14	C1	31	B3
15	B2	32	DG2
16	B1	33	A3
17	A2	34	DG1



BACK VIEW



FRONT VIEW

FIGURE 7.18-1
DISPLAY BOARD ASSEMBLY DRAWING

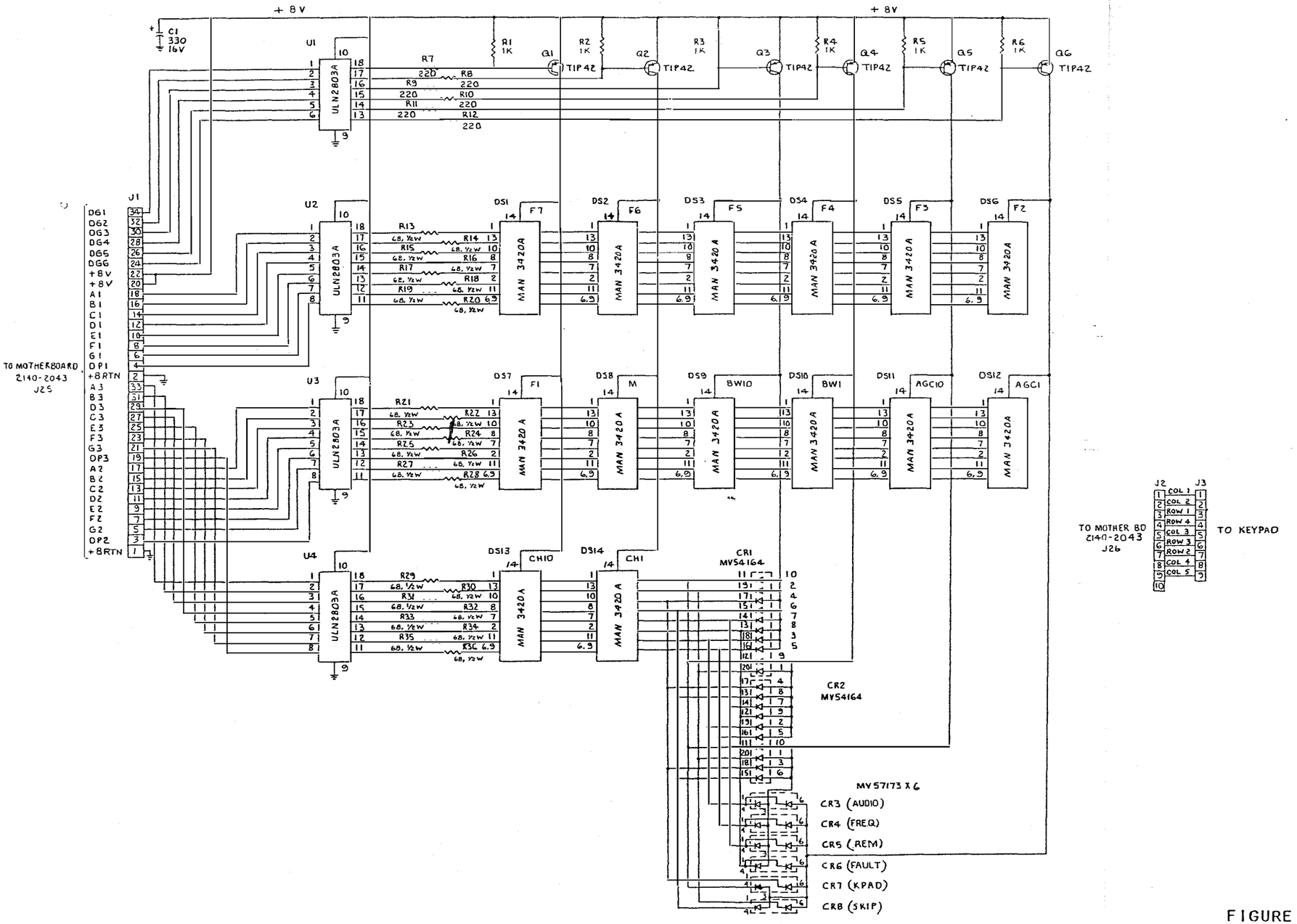


FIGURE 7.18-2
DISPLAY BOARD SCHEMATIC

AC LINE FILTER

The AC Line Filter circuits keep internally generated power supply switching noise off the AC input line.

See the corresponding board assembly drawing and schematic diagram.

RV1 is a metal oxide varistor (MOV) that clips high voltage transients on the AC input line. The additional components on the board make up the filter network. L1 - L4 isolate noise on each individual line, while L5 isolates any common node noise.

ADJUSTMENTS: No adjustments are required in normal service. If repair is required, send the complete board to the repair depot.

CONNECTIONS:

J1 - AC LINE HOT input

J2 - AC LINE NEUTRAL input

J3 - POWER SUPPLY HOT output

J4 - POWER SUPPLY NEUTRAL output

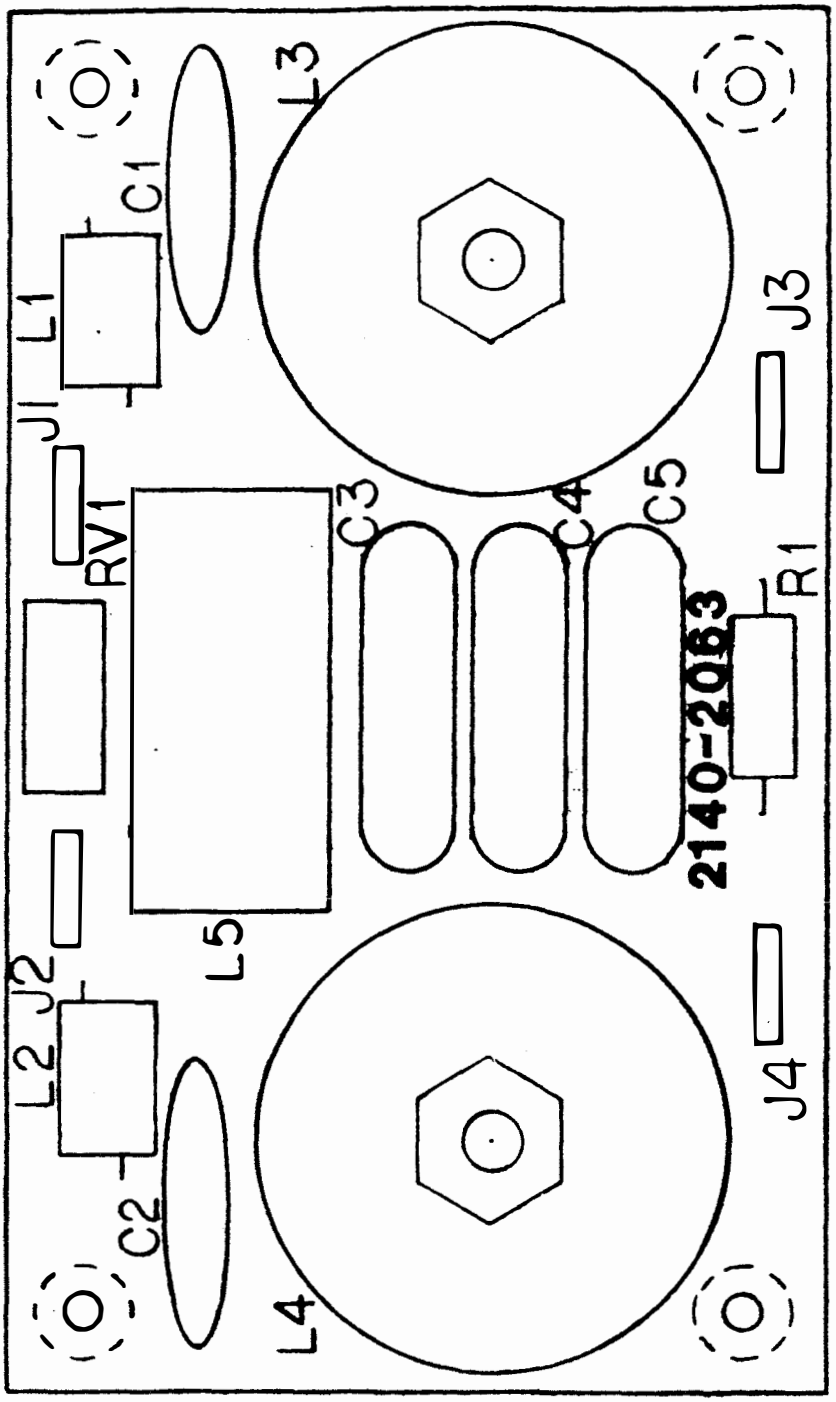


FIGURE 7.19-1
AC LINE FILTER BOARD ASSEMBLY DRAWING

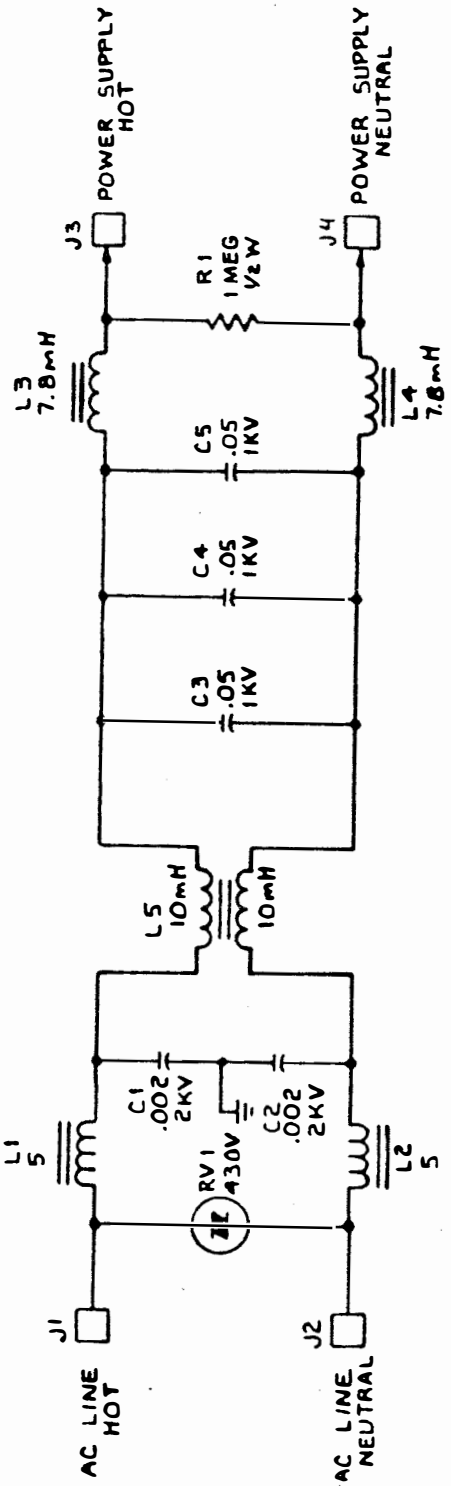


FIGURE 7.19-2
AC LINE FILTER BOARD SCHEMATIC

SERVICE BULLETIN

FOR

DUAL HIGH FREQUENCY RECEIVER MODEL NUMBER R-2307/U

POWER SUPPLY CAPACITOR REPLACEMENT

Bulletin No. 2307-9101

Cubic Defense Systems, Inc.
P.O. Box 85587
San Diego, California 92186-5587

Telephone: (619) 277-6780 Telefax: (619) 277-9353

Issue 1.2 12 November 1991

ELECTRONIC EQUIPMENT EVALUATION

NAVELEXSYSENGCEN PORTSMOUTH FORM 5989/2

2. JOB ORDER NO.	3. SERIAL NO.	3a. [illegible] NO.

1. EQUIPMENT (NOMENCLATURE)

2140-1124

5963-01-275-9382.

REMARKS

SERVICE BULLETIN 2307-9101

C20 and C22 - OLD 250V/150uF NEW - 250V/220uF

P/N - KMH250VN221M 25 X 25

C1 - OLD - 400V/.027uF NEW - 400V/.022-.033uF

P/N - KM1841-322/404

CR12 - REPLACED P/N HLZ480L40

RT1 + RT2 - REPLACED P/N KCC CL-190

C39 - REPLACED P/N .002M 3KVZ5U

C2 thru C5 and C16 - REPLACED P/N 470uF 50V

C9 thru C12 - REPLACED P/N 1000uF 25V

1.0 SCOPE.

This document contains information to check and replace (if necessary) filter capacitors in the R-2307/U Dual HF Receiver Power Supply module no. 2140-1124. The new components increase the mean time between failures (MTBF) of the module.

2.0 TOOLS REQUIRED.

The following tools (or equivalent) are required for this service bulletin:

- o ESD Solder Station
- o Replacement Tips (4) types - Std. Chisel .699"x.094, x-long Conical .984" x .008", SMD Flat 1.102" x .047" & Needle Point .669 x .008.
- o Desoldering Station
- o Desoldering Tips (3) sizes - .08 mm, 1.0 mm, and 1.3 mm
- o Needle-nose pliers
- o Soldering Iron (35 Watt Max.)
- o OO-SA Tweezers
- o Straight slot screwdriver
- o Full Flush Cutters
- o Pry-bar, small wood or plastic
- o Round-nose Plier
- o #1 Phillips Screwdriver
- o #2 Phillips Screwdriver
- o 3M Field Service Kit
- o Solder wick
- o Triclor Cleaning Solvent
- o Modification Kit, Cubic P/N 2307-9101-1

3.0 TEST PROCEDURES.

The following test procedures are included with this service bulletin:

- o Power Supply Module Test Procedure 2140-1824 contains procedures for module check out including test equipment requirements. This procedure should be performed after the module is modified.

- o Final Bench Test Procedure 2143-1801 contains test procedures for unit check out including test equipment requirements. This procedure is not required for module modification but is provided for reference only.

4.0 PROCEDURE.

<u>WARNING:</u> Set the front panel POWER switch to OFF and disconnect external power from the unit before performing the modification.

NOTE: The R-2307/U contains two modules of each type. These procedures apply to both modules in the chassis.

A. MODULE REMOVAL.

(1) Using a no. 2 Phillips screwdriver, push down, and turn all captive fasteners on the R-2307/U's top cover 1/4 turn counter-clockwise to release the fasteners.

(2) Remove the top cover.

(3) See figure 1, to identify Power Supply Module Assy No. 2140-1124.

NOTE: If both Power Supply modules in the chassis are identified as shown in Figure 4, the modification has been previously done. Proceed to step F. (4). If one or both of the modules are not identified as shown in figure 4, proceed to the next step.

(4) Using a no. 2 Phillips screwdriver, push down and turn the captive fasteners on the unmodified module's base 1/4 turn counter-clockwise to release the fasteners.

CAUTION: Do not use a sharp tool to pry up modules. Modules may be scratched or marred. Use a small wood or plastic pry-bar.

(5) Pry up on the top edge of the module to lift it from the chassis.

B. COMPONENT IDENTIFICATION.

(1) Using a no. 1 Phillips screwdriver, remove the front cover from the module.

(2) See Figure 2, and locate capacitors C22, C20, and C1.

(3) Refer to the table below.

Component	Old Value	New Value	Part No.
C22	250V/150μF	250V/220μF	KMH250VN221M25X25
C20	0250V/150μF	250V/220μF	KMH250VN221M25X25
C1	400V/.027μF (black)	400V/.022-.033μF (blue)	MKP1841-322/404

NOTE: Capacitor C1 is replace by a polypropylene capacitor that may range between .022 and .033μF.

(4) If capacitors with the old values are installed on the board, go to step C. If capacitors with the new values are installed on the board, go to step D. (5).

C. COMPONENT REMOVAL.

(1) Using a no. 1 Phillips screwdriver, remove the rear cover from the module.

(2) Locate Capacitor C22. (See Figures 2 and 3.)

(3) Using the soldering iron, solder sucker or solder wick, remove the solder from the leads on the trace side of the circuit board.

(4) Remove C22 from the board.

(5) Repeat steps (1) thru (4) for capacitors C20 and C1.

D. COMPONENT REPLACEMENT.

(1) Using the soldering iron, solder sucker, and cleaning solvent; clean the mounting surfaces of the circuit board where capacitors C22, C20, and C1 were just removed.

(2) Install capacitor with a value of 400V/.022 thru .033μF (blue) in C1 location and solder it to the board.

(3) Install capacitor with a value of 250V/220μF in C22 location and solder it to the board.

(4) Install capacitor with a value of 250V/220μF in C20 location and solder it to the board.

(5) Using a no. 1 Phillips screwdriver, replace covers on module.

(6) Use a felt tip marker or the label provided in the kit to identify the modified module as indicated by Figure 4.

E. CHECKOUT.

(1) Perform module test procedure 2140-1824.

(2) Check unit for proper operation.

F. MODULE INSTALLATION.

CAUTION: Ensure the module connectors are aligned correctly with the connectors in the chassis or the connectors may be damaged. Mate the standard connector first and then engage the coaxial connector.

(1) Orient and install the Power Supply Module in the chassis.

(2) Press the module firmly down to seat the connectors.

(3) Using a no. 2 Phillips screwdriver, press down firmly, and turn the captive fasteners 1/4 turn clockwise until they lock.

NOTE: If necessary, repeat steps A. (4) through F. (3) for the other Power Supply module in the chassis.

(4) Orient and place the top cover on top of the chassis.

(5) Using a no. 2 Phillips screwdriver, press down firmly, and turn the captive fasteners 1/4 turn clockwise until they lock.

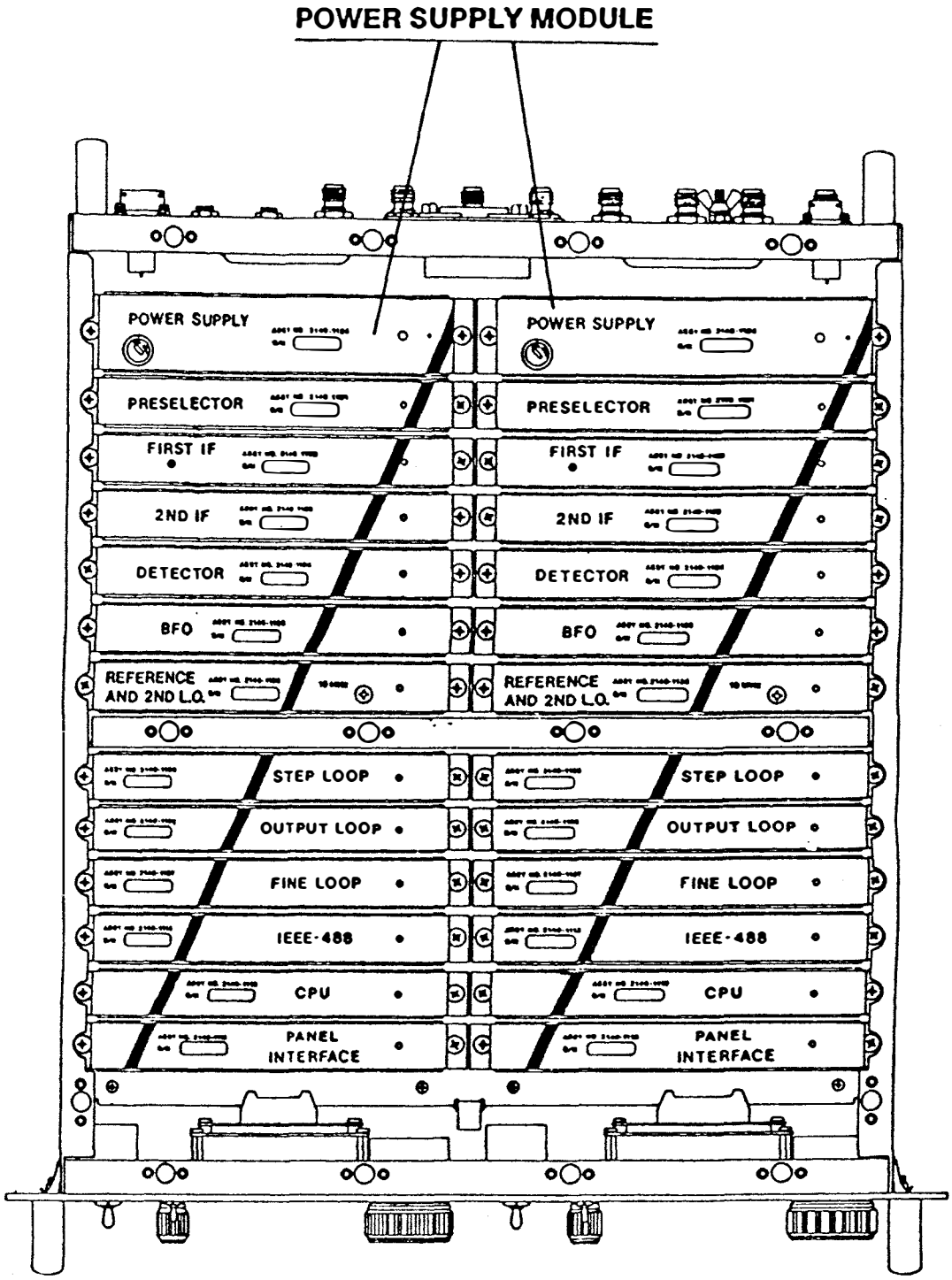


Figure 1. R-2307/U Top View.

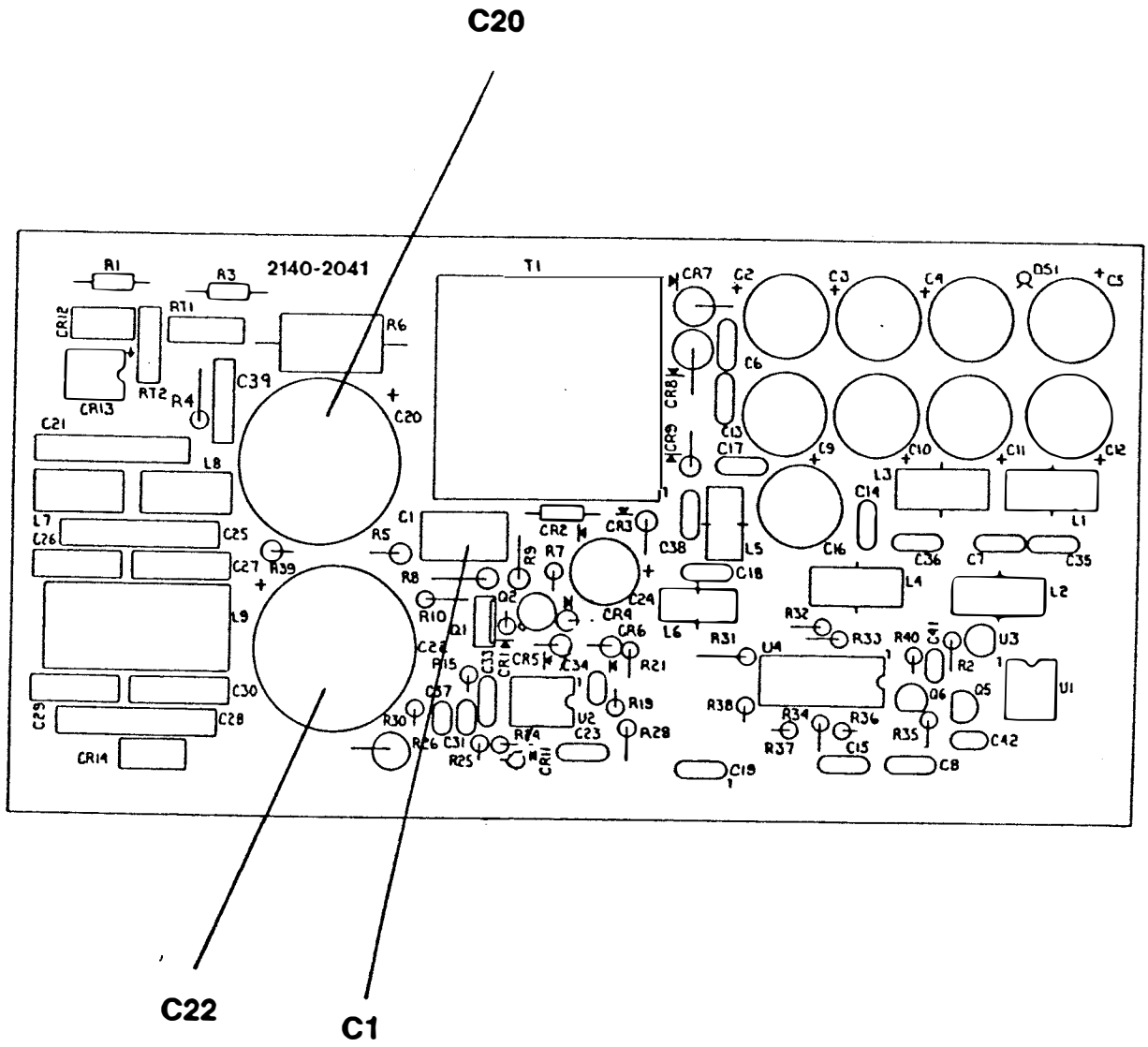


Figure 2. R-2307/U Power Supply Board - Component Side.

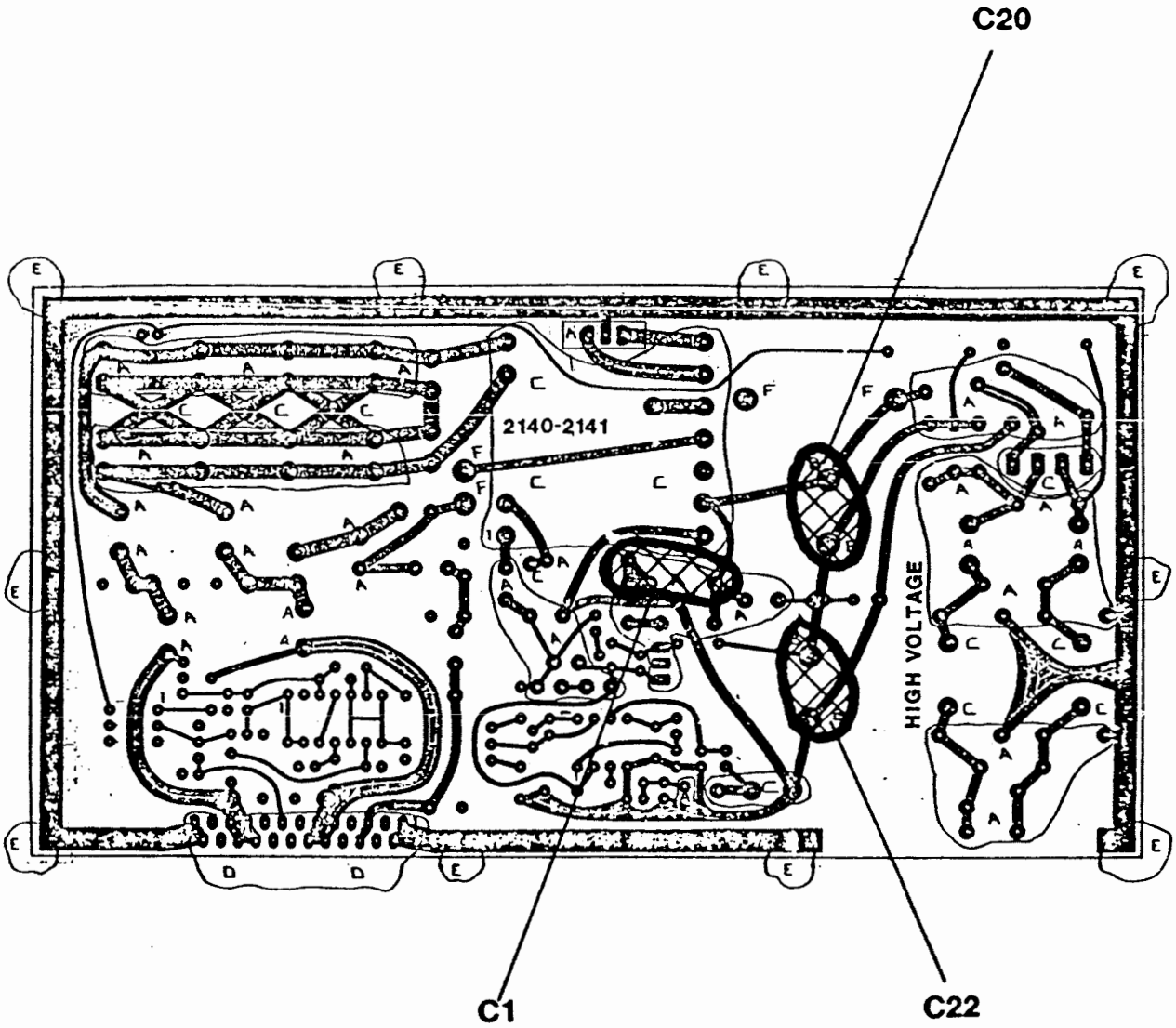


Figure 3. R-2307/U Power Supply Board - Foil Side.

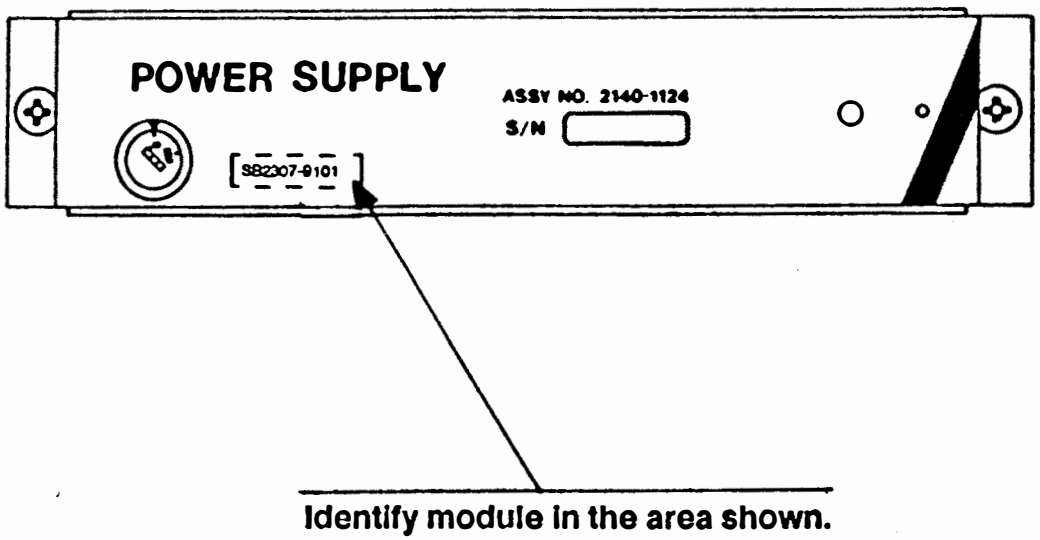


Figure 4. R-2307/U Power Supply Module - Modification Identification.