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BULLETIN 302B/RF
VOL 4 OF 5

TECHNICAL MANUAL MASTER AND SUPPLEMENTARY HIGH 3PEED TAPE SENDER, AND HIGH SPEED TAPE RECEIVER FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

(A MODEL)

This publication replaces all previously dated Army and Navy manuals, and the Air Force TO 31W4-2FG-1351 Vol 4 of 6 in part.

TELETYPE®
CORPORATION
5555 TOUHY AVENUE, SKOKIE, ILLINOIS

MARCH 1972

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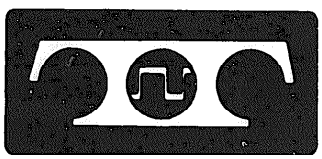
READER PLEASE NOTE: As of 8 September 1971, this BULLETIN consists of Five Volumes.



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INTRODUCTION

Bulletin 302B is a technical manual for the Master and Supplementary High Speed Tape Sender, and High Speed Tape Receiver used in the Multiple Address Processing System (MAPS). Volume 4 and 5 have been added to Bulletin 302B to include Radio Frequency Interference (RFI) Suppression features for the Multiple Address Processing System. These volumes are identified by an RF suffix and must be used with Volumes 1, 2, and 3 which contain information for standard cabinets. Volumes 1, 2, and 3 must be used with all sets whether rfi modified or not.

Volume 1 contains the Master, Supplementary, and Receiver sections, which provide description and theory of operation, installation, troubleshooting, adjustments, lubrication, and removal and replacement of components. Volume 1 must be used in conjunction with Bulletins 279B, Technical Manual High Speed Tape Punch (DRPE), and 301B, High Speed Tape Reader (DX Type).

Volume 2 contains the Master Sender wiring diagrams (actuals, schematics, and circuit card drawings). Volume 3 contains the Supplementary Sender and Receiver cabinet wiring diagrams (actuals, schematics, and circuit card drawings).

Volume 4 (302B/RF) contains Master, Supplementary Sender, and Receiver sections, which provide description and theory of operation, installation and checkout, and wiring diagram (actuals, schematics, and circuit card drawings) information used with rfi - equipped cabinets. Volume 5 (302B/RF) provides wiring diagrams (actuals, schematics, and circuit card drawings) for Master Sender cabinets with rfi features.

Each volume is made up of a groupof individual sections. The sections are separately identified by title and section number, and the pages are numbered consecutively, independent of other sections. The identifying nine-digit number appears on each page of the section in the upper right-hand corner of right-hand pages, and in the upper left-hand corner of left-hand pages.

To locate specific information, refer to the table of contents. Find the name of the involved component in column one and the title of the section in column two. The correct nine-digit section will then be found in column three. The sections are arranged in the order shown in the table of contents. Turn to page one of the section indicated where the contents of that section will be found (except where a section is small and does not require a listing of contents).

The sections comprising this bulletin are stocked separately and may be ordered individually if the entire bulletin is not required.

Note: For parts ordering information, refer to Bulletin 1208B/RF.

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TELETYPE CORPORATION
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MASTER AND SUPPLEMENTARY HIGH SPEED TAPE SENDER WITH RADIO FREQUENCY INTERFERENCE (RFI) SUPPRESSION FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

DESCRIPTION AND THEORY OF OPERATION

CONTENTS PAGE

1. GENERAL

1.01 This section provides a general description and theory of operation of radio frequency interference (RFI) suppression on the master and supplementary high speed tape senders. It is used with ref- to the standard literature as additional information relating to certain modules and components. There are also certain added new features used only on later ~~models, such as~~ external stop-send, bid retention, and **models, such as** sequence. Functional operation of the high speed tape senders is unchanged (Figures 1 and 2).

1.02 The basic function of RF1 suppression as applied to t&typewriter equipment is to provide shielding to suppress electrical field radiation from 1 kilo hertz to 1 giga hertz. Signal, clock, and electrical power inputs and outputs are the same as described in the standard MAPS sections.

2. DESCRIPTION

2.01 The new parts added to the tape senders consist of a conduit plate, function box assembly, capacitors, ground straps, latches and contacts.

2.02 The conduit plate has three 3/4 inch knockouts for clock and signal input and output cables. and one 1/2 inch opening for an ac power input circuit connector. The conduit plate is mounted in the cable opening at the bottom rear of the cabinet.

2.03 The junction box consists of a three terminal board, two 0.47 microfarad bypass capacitors, and wires to connect -with an existing ac input terminal hoard. Adjustable pawl fasteners are grounded and secure the front panel to the cabinet frame.

DX TAPE READER

2.04 Signal shielding for the DX tape reader consists of two 0.001 microfarad capacitors, two contact shorting assemblies, and a ground strap. The two capacitors are connected across the -28 volt dc and common of the code reading and verifying contacts.

2.05 The contact shorting assembly is connected to the code reading and verify contact mounting screws in such a manner that they are grounded to the reader top plate.

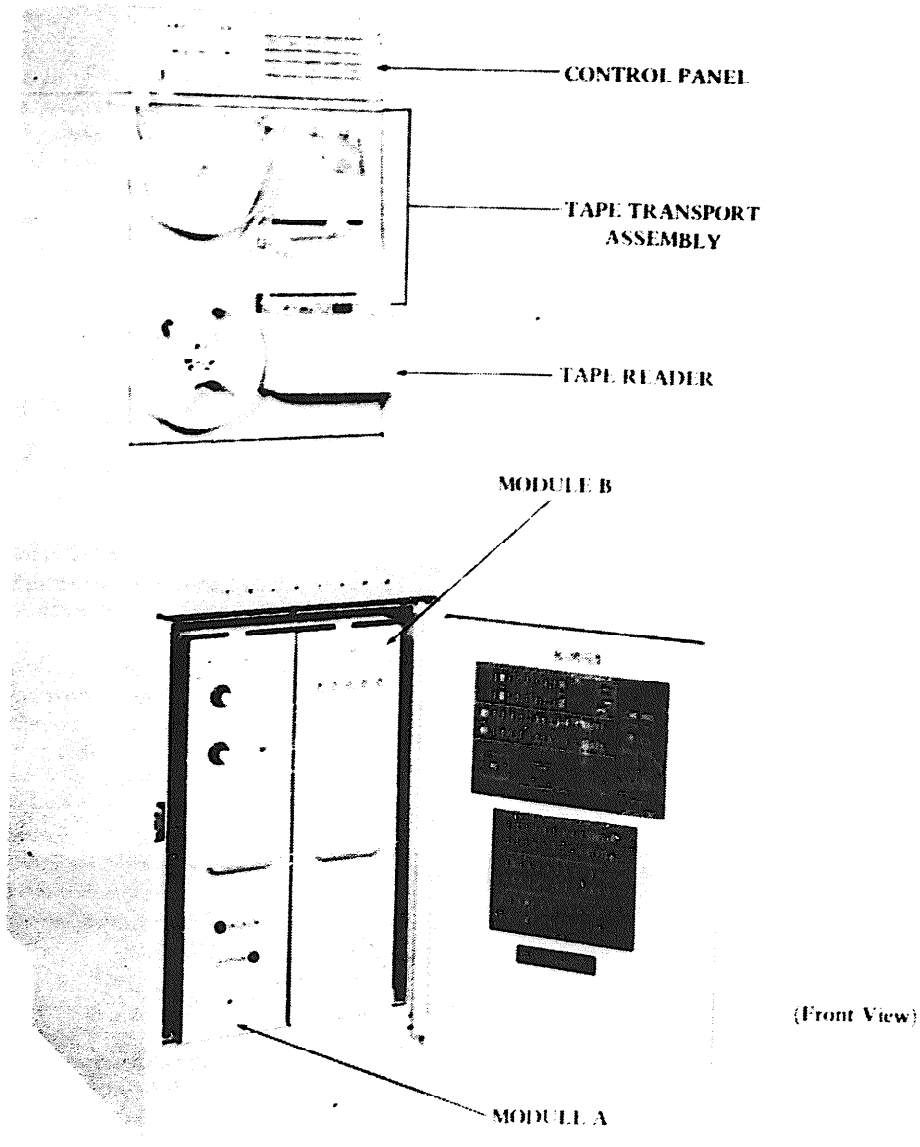
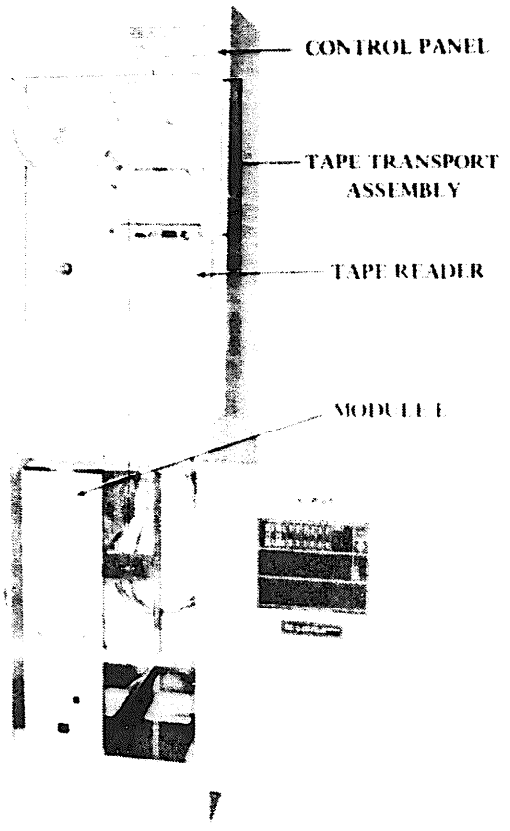


Figure 1. Master High Speed Tape Sender



(Front View)

Figure 2. Supplementary High Spread Tape Sender

Figure 2 Supplementary High Speed Tape Sender

The ground strap is connected to the base of the reader and its mounting bracket, providing a path to ground, bypassing the reader shock mounts.

EXTERNAL STOP SEND

2.06 The external stop-send capability provides the system with an external means of stopping the reader on the character after the one being read. The reader stops when a +6 volts is received at the input lead which is at -6 volts level under normal operating conditions. The reader continues transmitting in correct character frame when a -6 volt signal is received on this input lead.

BID RETENTION

2.07 A bid retention feature on the supplementary and master transmitters automatically retains the line after the manual STOP switch is operated, and the tape lid is lifted with the reader in the on-line condition. This allows the operator the option of stopping the reader during transmission, lifting the tape lid and removing the tape for possible editing. The tape may be replaced in the reader, the STOP switch released and transmission resumed without losing the on-line condition.

SOM CHARACTER SEQUENCE

2.08 The SOM sequence feature adds an additional letter V character at the beginning of the sequence. Each reader transmission is preceded by fourteen characters consisting of eight programmed identifying characters, one operator programmed character, one figure character, three numeric characters, and a letter character in that order (example: VZCZCABCX↑999↓).

2.09 The three numeric characters increase one count after each transmission. The counter can be manually reset to any count, including zero. The operator has the option of deleting a complete sequence by using the NUMBERS DELETE indicator switch. The message rate is limited to the maximum recycling rate of the counter (five times per second).

3. THEORY OF OPERATION

CONTROLS AND INDICATORS

3.01 Operator controls and indicators art located on the control panel at the top of each cabinet. The master and supplementary control panels are identical except for the message numbering indicator on the left ride of the master control panel. Additional controls are located on the front panels **of** the electronic modules in, the tower half of each cabinet behind protective doors. Parallel to serial **con**verter programming facilities arc located wthin the master transmitter logic module (Figures 3. 4. and 51

3.02 The VERIFIER/TAPE FEED (Figures 3 and 4) split alarm and pushbutton switch indicates an alarm in red, with the reset switch common to both alarms. External equipment alarms are accepted through a relay common to both alarms, providing the alarm transfer contacts.

3.03 The ABNORMAL TRAFFIC indicator lights when an abnormal traffic input signal is received from the external equipment.

3.04 When the reader is in the STOP condition. the STEP READ switch can be used to step the reader through a tape message, one character length (0.1 inch) for each operation of **the** switch. **The operator may use the** STEP **switch to manually** step the **reader at tunes** when there is no normally supplied step pulses.

3.05 Operating **the** STOP switch. illuminates **the switch indicator and stops the reader during transmission.** No other associated reader may **send at this** time. Operating the switch a second time, puts out the switch light, **and** restarts the **reader** and tape reading system.

3.06 **When** the POWER switch is operated, the switch indicator is illuminated and the switch activates electric power to the tape transport motor, tape re___ motor, and electronic modules.

3.07 When a bid to transmit has not been mitiated, operate the MOTORS switch. which illuminates the inductor and permits manual operation of the reader and tape winder motors.

3.08 The ON LINE indicator is illuminated when the reader has authorization to transmit.

3.09 The BID switch indicator is illuminated when operated and generates a bid to transmit when tape is in the reader.

3.10 When the NUMBER DELETE switch is operated and illuminated. the start of message sequence is not transmitted ahead of each transmission. At the end of each transmission the switch automatically resets to the normal (send number) mode and the indicator light is turned off.

3.11 **Circuit breakers are provided on the front** panel **of** the power supply module for overload protection. Should a circuit breaker trip to its off position, the normal procedure of turning off cabinet power before resetting the breaker should be observed

3.12 **The additional controls found on the front** panels **of the** electronic **modules in** the lower half of the cabinet are as follows:`

(1) Module A - CODE LEVEL selector switch 15. **6.** 7. **and** 8 levels); UNITS PER CHARACTER INTREVAL selector switch indicates synchronous or [illegible] **indicates synchronous or**

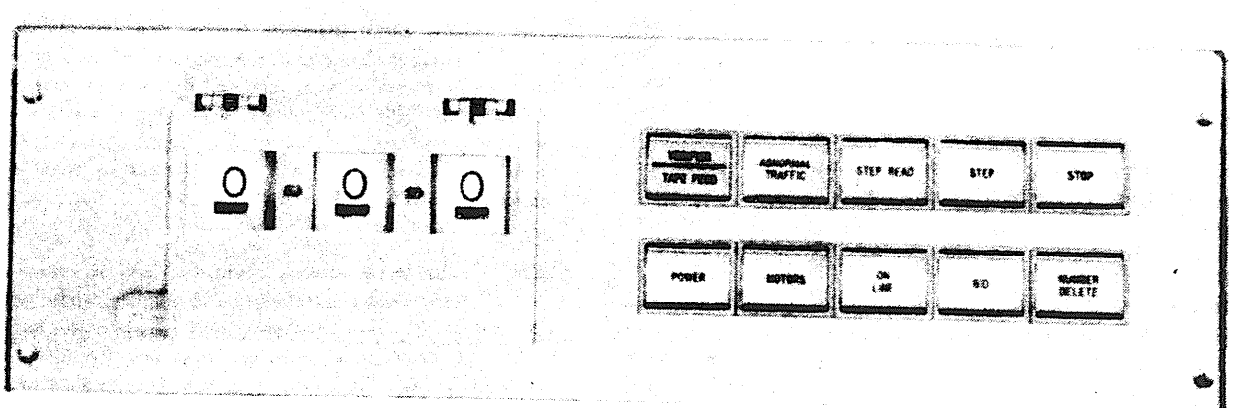


Figure 3 Master Control Panel

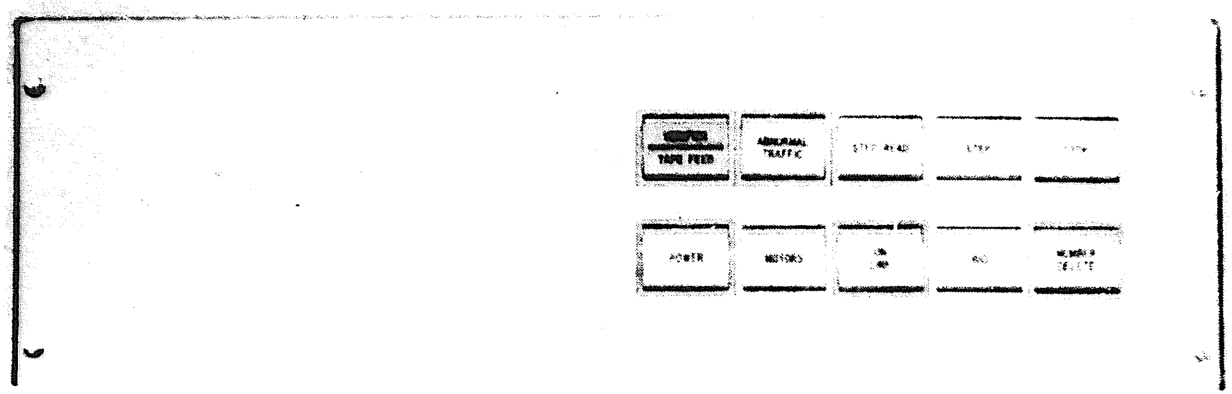


Figure 4 – Supplementary Control Panel

start-stop level numerals. SIGNAL MODE toggle switch indicates either START-STOP or SYNCHRONOUS operation.

(2) Module B – The SOM CHARACTER toggle switches (2, 3, 4, 5, and 6, one for each character bit, are operated in MARK or SPACE position to determine the [illegible] character in the start of message sequence.

(3) Module E – The module control panel contains some logic circuitry and [illegible] voltage circuit breakers; all other controls are contained in modules A and B in the master cabinet.

CIRCUIT DESCRIPTION

3.13 The 0 volt, and -6 volts on some internal leads are identified by a shaded corner in the logic symbol from which they originate. The [illegible] coupled inputs to logic elements are shown as half arrow heads. Half arrow heads indicate ac coupled pulse input.

3.14 The commonly used NOR logic element is identified by the designation EA within the [illegible] symbol. The output of the element is negative when [illegible] input is 0 volt. The output is 0 volt only if all inputs are negative. A special input, identified by an arrow entering a corner of the symbol, allows the addition of extra logic inputs to the element or connecting two or more elements together to obtain more inputs and greater load driving capability.

3.15 The flip-flop element is designated by a [illegible] box with a diagonal line across [illegible]. The priming voltage inputs are shown as half arrow heads and the setting voltage inputs by tail arrows. Prime [illegible] inputs are [illegible] enter the upper [illegible] of the symbol and prime 0 volt and set 0 signals enter the lower half of the symbol. An arrow entering the center of the symbol designates the set 1 and set 0 inputs are connected together.

3.16 If no priming inputs are shown, the prime 1 input is connected to the inverted output (lower half of the symbol) and prime 0 input is connected to the normal output (upper half of symbol). Each input pulse reverses the condition of the voltages on the normal and inverted outputs.

3.17 The pulse amplifier element is identified by a square box with the letters PA in the symbol. A half arrow head indicates the input. This element produces a pulse approximately two microseconds in duration whenever the input goes negative. When both inputs are used, a pulse is produced only when both inputs go negative.

3.18 A rectangle with the letters PA within the symbol represents the power amplifier element. This element has two inputs and can perform the NOR element function with approximately three times the load driving capability of [illegible] NOR (EA) element.

3.19 [illegible] element can be used either as a one shot [illegible] multivibrator and is identified by a square box with the letters DN within the symbol. Delay [illegible] pulse duration indicated, [illegible] the frequency is [illegible].

3.20 [illegible] input polar signals (+6 [illegible] volts) [illegible] signals (0 volt and -6 volts) [illegible] identified by a rectangular box [illegible].

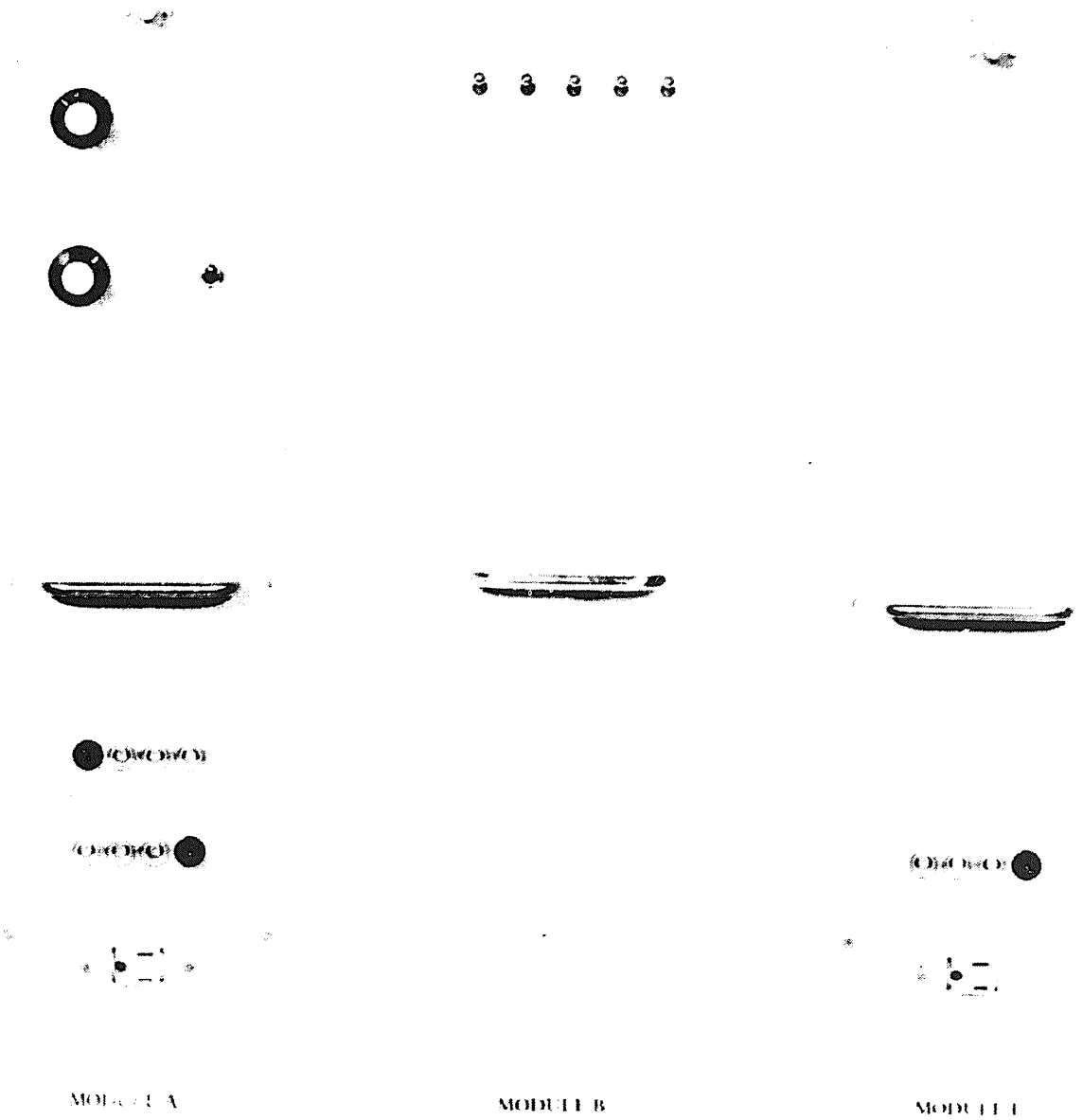


Figure 5 Master and Supplementary Modules

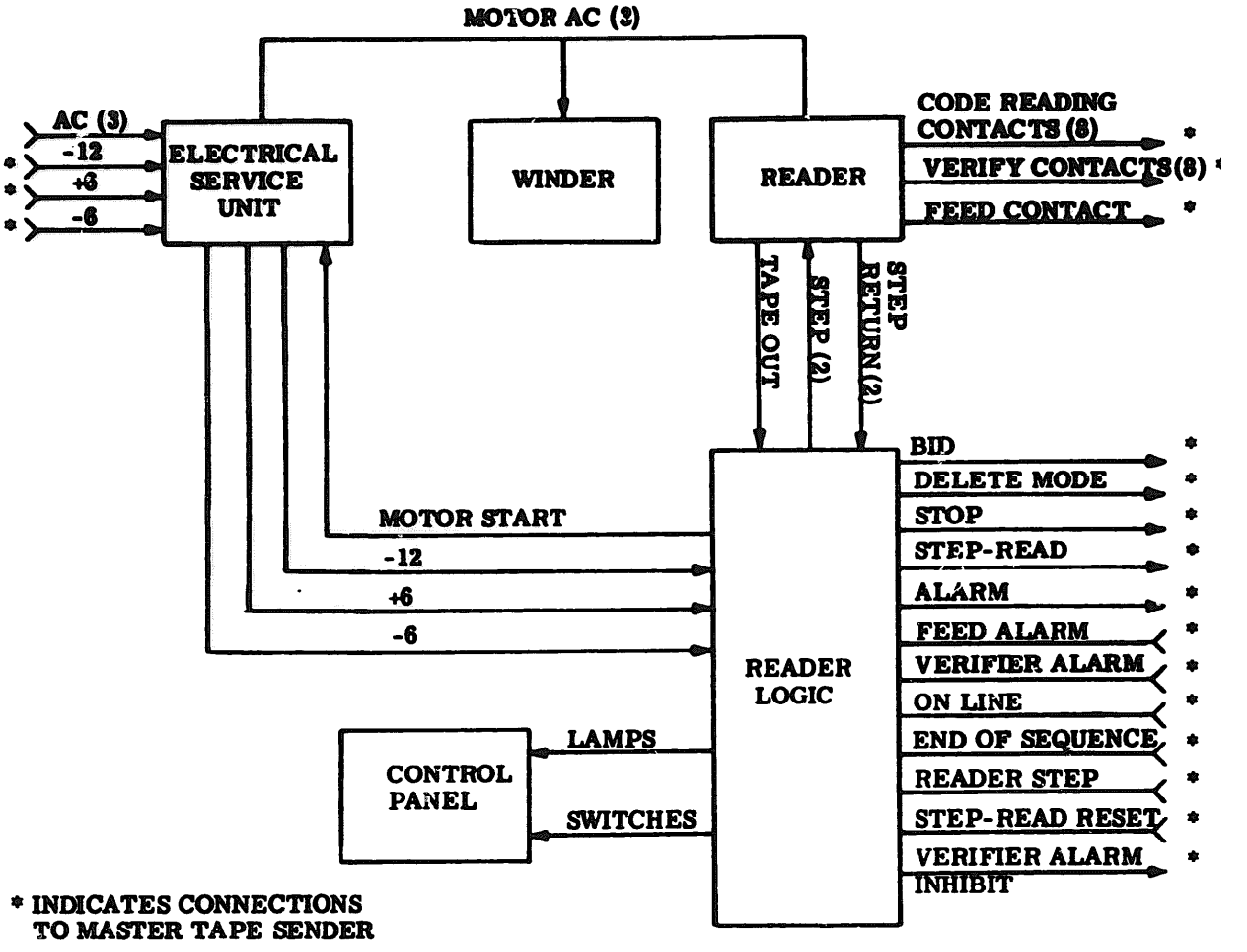


Figure 6 - Block Diagram for Supplementary High Speed Tape Sender

3.21 An output element translates neutral signal (0 volt and -6 volts) to output polar signals (+6 volts and -6 volts). It is identified by a rectangular box with OUTPUT printed within the symbol.

SUPPLEMENTARY READER LOGIC

3.22 The electronic logic circuits contained in module E are divided into the following four functional : bid circuitry, start of mo th delete circuitry, step circuitry, and alarm circ t of

A. Bid Circuitry

3.23 Insert the punched paper tape in the reading head.

The normally closed tape-out contact moves to its ng head. open Position which is connected to pin C8 of JE128. This es to its action- initiates the bid circuitry of the reader logic Refer to 28. This 7742WD, Sheet 2, Figure 6. Refer to

3.24 Pin C8 of JE128 assumes a negative voltage allowing the inverter ZE102 to saturate. The 0 volt voltage output at the inverter (pin 9) is applied to the input pin B30 he 0 volt pin B30,

LA-2D ZE103, **and pin B4 of LA-2A,** ZE118. At LA-2D it is inverted, **and** applied to pin A32, LA-1D, ZE103 together with the input at pin B32. When both inputs are negative, the output on pin B34 is **driven** to 0 volt which acts as a prime voltage **for setting the flip-flop** D-B **of** ZE110 into the set one state. (Pin B33 is at 0 volt and pin B34 at a minus voltage.)

3.25 The BID indicator switch may now be operated to **provide** a transition **at** the **input, pins A36, and** B36 of flip-flop D-B of ZE110. The voltage transition switches the flip-flop to the set one state. The **two** LA networks connected between the BID switch and the complementary input are connected **as** a dc (direct current) flip-flop, to prevent switch contact bounce from affecting the set input of the flipflop.

3.26 With flip-flop D-B of ZE110 in the set one state, **pin** B34 is driven negative and pin B33 is driven to 0 volt. The 0 volt is inverted by PA-1C of **ZE108** and applied to PA-1D of ZE108. The output, pin B1 **of** PA-1D of ZE108 is driven to 0 volt, energizing relay K2 **and the motor start** relay K1 through an isolating diode CR-B of ZE110.

3.27 The diode prevents relay **K2** from being energized when the MOTORS indicator switch (SF107) located on the control panel, is operated. Refer to 7742WD. Sheet 6 for the motor circuit. When energized, the **motor** start relay K1 starts the reader and tape winder **motors.** Energizing relay K2 lights the bid indicator lamp and motor indicator lamp. The diode connected between the bid lamp and motor lamp prevents the bid lamp from lighting when the MOTORS switch is activated.

3.28 The negative voltage at pin B34 on flip-flop D-B of ZE110 is inverted to 0 volt by PA-2C of ZE108 and applied to the input pin A32 on DY-A of ZE108 for a 500 millisecond one shot. The output pin A34 is driven to 0 **volt and remains there for** a period of 500 milliseconds, at this time it returns to a negative voltage. This negative transition is applied at the input pin A31 on PA-E of ZE108 and provides a positive puke at the output, pin A27.

3.29 This puke is again delayed by an identical delay - pulse amplifier network. The results are a total delay of one second from the time a negative transition was obtained at pin B34 on flip-flop D-B of ZE110 until a pulse is provided at pin 824 on flip-flop D-C of ZE110. The associated prime input pin A24 on flip-flop D-C of ZE110 was driven to 0 volt at the time flip-flop Q-B of ZE110 was initially switched by the BID indicator switch. The flip-flop D-C of ZE110 is switched, driving the inverted output pin B26, negative. This output is applied to the input, pin B25 on LA-1C of ZE114.

3.30 **The second input of** this element, pin A24, **is supplied** by the output on PA-1C **of** ZE108 which **-samples** the normal output pin B33 **on** flip-flop D-B of ZE110. The normal output of flip-flop D-B, having been driven to 0 volt at the time the BID switch was activated, allows PA-1C section of ZE108 to provide a -5 volts to pin A24 in LA-1C of ZE114. With both inputs on LA-1C of ZE114 at a negative voltage, the output pin A27 is driven to 0 volt. This 0 volt is supplied as a BID request signal to sequence control logic in the master transmitter cabinet.

3.31 The effect of inserting tape in the reader and operating the BID switch is to immediately start the reader and winder motors, and one second later provide a BID request signal.

3.32 After operating the BID indicator switch, the operator may cancel the bid request provided action is taken prior to the receipt of the on-line signal from the sequence control logic. This reset action is accomplished by operating the BID indicator switch a second time to obtain a positive transition at the complementary input pin A36 and B36 on flip-flop D-B **of** ZE110. The prime 0 volt input at pin B35 of ZE110 is at 0 volt due to the input pins B22 and B23 on LA-2C of ZE114, both being negative. The input pin B23 was driven negative through PA-1C of ZE108 at the time flip-flop D-B was first set.

3.33 The second input to LA-2C of ZE114 samples the on-line signal from the sequence control logic. As long as the on-line signal remains negative the flip-flop D-B of ZE110 is primed to be reset. When the on-line signal goes to 0 volt, the prime 0 volt input, pin B35 is driven negative and the option for resetting the flip-flop D-B with the BID indicator switch is removed.

3.34 Flip-flop D-B can now be reset only by a tape-out indication from the reader. This tape-out indication is a positive transition at the input pin 12 of inverter ZE102 where it is inverted and applied to pin B4 on LA-2A, ZE118. If pin B3 and pin B5 on LA-2A is negative at this time a positive transition will be applied at pin B32 and pin B27 on supplementary gates of ZE110, resetting flip-flops D-B and DC of ZE110. When these fiip-flops are reset the reader and winder motors are turned off and the bid request to the sequence control logic is removed.

3.35 The negative input at pin B5 on ZE118 is a result of LA-2B on ZE118 sampling either an off-line condition or an end of sequence. If neither of these conditions exist the input at pin B5 will be at 0 volt and the tape-out indication will be prevented from resetting the above mentioned flip-flops. This logic prevents an incomplete start of message sequence to be transmitted when the tape lid is released during the sequence. The negative input at pin B3 of ZE118 is a result of LA-2A of ZE116 (refer to 7742WD, Sheet 4) STOP switch not being activated. Pressing the STOP switch while the reader is on-line and reading tape. allows the output pin A9, of ZE116 to be driven to 0 volt and applied to pin A27, CRC on ZE112. The input pin B3, LA-2A on ZE118 is driven to 0 volt, preventing output pin A9 from being driven to 0 volt and resetting flip-flops D-B and D-C on ZE110.

3.36 The power on reset circuit at Position ZE202 is used to provide a collector set pulse to flipflops D-B and DC of ZE110, a predetermined time after power is turned on. This action insures that the bid circuitry is not bidding for the line when the equipment is initially turned on. The 150 ohm, 1 watt resistors shown across the various relay contacts driving indicator lamps, are used to keep a small amount of voltage across the filament of the lamp. This reduces the initial current surge and extends the life of the lamp.

B. Start of Message Delete Circuitry

3.37 The number delete circuitry provides the operator with the option of deleting the number sequence which normally precedes each message tape. Prior to operating the BID indicator switch, the operator determixes if the message tape requires a number sequence. If the number sequence is not necessary the NUMBER DELETE indicator switch is operated. This switch provides a positive transition at the input pin A36 and B36 on flip-flop D-B. ZE112, provided the on-line signal applied at pin B14 on LA-1B, ZE114 is negative. If this on-line signal is at 0 volt, indicating the associated transmitter is on-line, the indication from the NUMBER DELETE indicator switch is held at LA-1B of ZE114 and does not switch flip-flop D-B of ZE112. Refer to 7742WD. Sheet 3.

3.38 Assume the on-line signal applied at pin B14 on LA-1B of ZE114 is negative and the signal from the NUMBER DELETE indicator switch is presented to input pin A36 and B36 on flip-flop D-B of ZE112. This flip-flop will be switched to the one state. driving the output pin B34. negative. The signal is applied to input pin A4, PA-2D of ZE108, driving the output pin Al to 0 volt, which energizes relay K4 and lights the number delete lamp through the K4 relay contact.

3.39 The negative voltage at pin B34 of flip-flop ZE112-B is also applied to pin B26 on LA-1F of ZE103. This element is held at this time due to 0 volt being supplied to pin A21 from the output B6 on PA-1C of ZE108 (refer to 7742WD. Sheet 2). When the BID indicator switch is operated, flip-flop D-B of ZE110 is switched as described in 3.25. A 0 to -5 volt transition is applied to pin A24 on LA-PC and pin A21 on LA-IF of ZE103.

3.40 The output pin A27 of LA-1C, ZE103 is held at -5 volts due to the 0 volt present at input pin B25 and output pin B28 on LA-1F of ZE103 goes to 0 volt. The resulting positive transition at the output of LA-IF is used to set flip-flop D-C of ZE112 into the one state. driving the output pin B26, negative. This voltage level is inverted by LA-ID of ZE114 and applied to the sequence control logic in the master cabinet as a delete mode signal.

3.41 At the completion of the message tape. a tape-out indication is received from the tape-out contact at the reader. This indication resets the bid circuitry as described in 3.34, and provides a negative to 0 volt transition at pin B6 on PA-1C of ZE108, (refer to 7742WD. Sheet 2). This transition is applied to pin A30 of supplementary gate ZE112, resetting flip-flop D-B of ZE112. With the reset of flip-flop D-B. the NUMBER DELETE indicator lamp is extinguished.

3.42 During normal operation (not in the delete mode) the output pin B33. on flip-flop D-B of ZE112, is at -5 volts. This is applied to the input pin B25 on LA-1C of ZE103, and permits the negative bid signal transition at pin A24 as described in 3.40. The inverted signal is passed to flip-flop DC of ZE112 as a set zero signal. This provides a -5 volt indication at the delete mode output pin F7 of JE128.

3.43 At the completion of the start of message sequence a negative going transition is received from the master logic at JE128, pin E7. The signal is inverted by LA-2E, of ZE118, and applied to pin B31 of the supplementary gate ZE112 as a reset signal for flip-flop D-C of ZE112. This reset signal is allowed to pass, provided an on-line signal is present at the prime input pin A31 of the supplementary gate. When flip-flop D-C of ZE112 is reset. the delete mode indication to the master logic is changed to 0

volt. This permits the step pulses in the master logic to be diverted from the start of message generator to the associated reader.

C. Step and Read Circuitry

3.44 During reader operation, the operator has the option of stopping the reader and stepping it manually with the STEP READ indicator switch. When the STOP switch is operated, the associated STOP indicator lamp is lit and a voltage level change from 0 to -5 volts is obtained at pin B4 on LA-2A, ZE103. The switch output is fed through a dc flip-flop configuration, similar to the circuit described in 3.25 to remove contact bounce. (Refer to 7742WD, Sheet 4.)

3.45 When the reader is operating, the on-line signal input at pin B5 of LA-2A, ZE103 is -5 volts. As a result of the negative level being applied to pin B5 of LA-2A, ZE103 and the level change from 0 volt to -5 volts at pin B4 due to the STOP switch, the output pin A9 is driven to 0 volt. The 0 volt is used as a reader stop signal to the master logic and as a prime voltage to flip-flop D-F of ZE110.

3.46 In the master logic this signal is used to inhibit the stop pulses to the start of message (SOM) generator or the reader, thereby stopping operation. The prime voltage applied at pin A2 of flip-flop D-F permits the positive transition appearing at the set input pin A1, to switch the or the reader, thereby stopping operation. The prime voltage applied at pin A2 of flip-flop D-F permits the positive transition appearing at the set input pin Al, to switch the flip-flop, driving the output pin B3, to -5 volts. The positive transition at the input, pin **Al, is a** result of operating the STEP READ switch.

3.47 The output pin B3 of flip-flop D-F on ZE110 is inverted by LA-2E on ZE116 and supplied to the master logic as a step-read pulse. This pulse allows the reader to k stepped one character, and read by the reader to k transmitted on line, provided the stop switch is in-the stop position. When the **STOP** switch is operated again, returning it to its normal position, the reader is stepped automatically by the incoming step pulse rate.

3.48 The reader may be manually stepped (off-line) during periods when the reader is not normally being stepped by the incoming step puke rate. The STEP indicator switch output is fed to a dc connected flip-flop configuration, consisting of **LA-lB,** and LA-2B on ZE116. When the **STEP** switch is operated, a positive transition is obtained at the output pin **All** of this flip-flop and applied **to LA-1B,** ZE103 for inversion prior to king applied to the input pin B13 of LA-2B, ZE103.

3.49 If the second input pin B12 of LA-2B is negative at this tune, the input at pin B13 will be inverted and appear at the output pin **All.** The input level at pin B12 is 0 volt only when the STOP switch is in its normal position and at the time the on-line signal input at pin B23 of LA-2C, ZE103 is -5 volts. When this condition is met it is assumed the reader is normally king stepped by incoming step pulses and the manuai step indications are held.

3.50 The result is, the STEP switch is available for manually stepping the reader at times when it is not reading tape and being stepped by pulses received at pin D10 on JE128. Assuming the input pin B12 of LA-2B, ZE103 is at -5 volts, the manual step pulses at pin B13 appear inverted at the output pin A11. Then the pulses are inverted twice by LA-2F, ZE103 and LA-2F on ZE116.

3.51 At the output, manual step pulses appear as positive transitions which are applied to the driver assembly. The driver assembly, located in the tape transport assembly, functions to change the low-level stepping pulses to a power level adequate for energizing the reader stepping Coils. Th pulses are delivered **to** the driver assembly from two sources, one from the STEP switch described in 3.50, and **the** other from the sequence control circuitry in the master logic. They are applied to pin D10 an **JEl28.**

3.52 The LA-IA of ZE118 performs the function of preventing an alarm indication from occuring when the reader is restarted after it has been stopped and manually stepped with the STEP switch. This is required due to the characteristics of the verify logic explained in the following paragraphs.

3.53 Input pin **A7** of **LA-lA, ZE118** samples the condition of the STOP switch. When the STOP switch is in the stop condition, the input is -5 volts. **Pin B7 of LA-1A, ZE118 sa-ples** the on-line signal, -5 volts, which is on at this point. The third input pin, **A6** of **LA-1A, ZE118** samples the STEP switch output at pin **Al7** of **LA-1B. ZE103.** When the switch **is** operated, pin **A6** of **LA-1A, ZEll8 is** driven negative, with **all** three inputs of LA-1A, **ZE118** at -5 volts. The output pin **A10 is** driven **to** 0 volt. This positive transition is applied to the master cabinet logic where it is used to prevent an alarm on reader start-up when the contacts are sampled again.

3.54 When power is turned off at the supplementary cabinet, relays **Kl** and K2 provide an open circuit at the stop signal output, pin **Cl0 of JE128,** and the step-read signal output, pin C9 of JE128. When power is turned on, the relays are prevented from energizing for a period of 80 milliseconds, after being energized, the contacts close. At this time the two outputs have had time to stabilize at -5 volts and any transitions are prevented from being applied to the master logic.

D. Alarm Circuitry

3.55 Two types of alarms are contained in the reader logic circuitry: A verify error alarm and a reader feed error alarm. When either one of these errors occur, an indication is received at pin A8 or B8 of JE128. setting an associated flip-flop **D-D** or **D-E** of **ZE110.** The flip-flops are primed by the presence of an on-line indication from the master logic. When either of the two flip-flops is set, an

associated alarm lamp is lighted and a 0 volt indication is applied at pin A1 or B1 of LA-2E, ZE103. The output pin B9 of LA-2E, ZE103 is inverted by LA-1E, ZE116 and supplied to the verifier in the master logic as a 0 volt alarm signal. (Refer to 7742WD, Sheet 5.)

3.56 **If the alarm flip-flops were to come up in the alarm condition when power is turned on, an output of the alarm circuit is required at LA-1C, ZE116. This prevents an alarm indication to the master logic. Since an alarm at any one sender prevents operation at any other sender, this condition could interrupt the step pulses to an operating sender.**

3.57 Press the VERIFIER/TAPE FEED indictor switch **(ALARM RESET on schematic) to reset alarm flip-flops and extinguish the alarm lamp or lamps. An ON-LINE indicator lamp is lighted when the on-line signal is received. The indicator lamp is a signal to the operator when a particular reader is allowed to transmit after a line bid has been entered. Relay K3 performs the same function at the output of the alarm circuitry as relays K1 and K2 performed in the step and read circuitry described in 3.54.**

MASTER TRANSMITTER LOGIC

3.58 The master transmitter cabinet contains one DX type reader with the necessary tape handling equipment. The electronic **logic** and power supply is contained in two removable modules located in the lower part of the cabinet.

3.59 The electronic logic circuits in modules A and B are similar to the reader logic in module E except for the use of relays to open intercabinet signal lines when power is off. The controlling logic circuits contained in modules A and B are divided into five functional logic systems. They are arranged for controlling up to five external supplementary tape senders plus the associated master transmitter. Refer to Figure 7 for a block diagram. The logic circuitry consists of the following logic systems: reader logic, parallel to serial converter, sequence control, verifier, and start of message generator (SOM).

A. Reader Logic

Bid Circuitry

3.60 Insert the punched paper tape in the reading head. The normally closed tape-out contact moves to its open position which is connected to pin C8 of JA128. This action initiates the bid circuitry of the reader logic. Refer to Figure 7 and 7744WD. Sheet 2.

3.69 Pin C8 of JA128 assumes a negative voltage allowing the inverter ZA301 to saturate. The 0 volt output at the inverter (pin 9) isapplied to the input pin B30 of LA-2D, ZA103 and pin A5 of LA-IA, ZA303. At LA-2D it is inverted, and applied at pin A32 of LA-ID, ZA103 Text with the input at pin B32. When both inputs are Text the output on pin B34 is driven to 0 volt which acts as a prime for the inputs at pins A36, and B36 for setting flip-flop DB of ZA110.

3.62 The BID indicator switch may now be operated to provide a transition at the input pins A36, and B36, of flip-flop D-B, switching to the set one state. The two LA elements connected between the BID switch and the flip-flop set input are connected as a dc (direct current) flip-flop to eliminate contact bounce.

3.63 With flip-flop D-B in the set state, pin B34 is driven negative and pin B33 is at 0 volt. This 0 volt is inverted by PA-1C of ZA108 and applied to PA-1D of ZA108. The output pin B1, of ZA108 is driven to 0 volt energizing relay K2, and the motor start relay K1 through an isolating diode, ZA110. This diode prevents relay K2 from being energized when the MOTORS indicator switch is operated. With the motor start relay K1 energized the reader and tape winder motors start. When relay K2 is energized the BID and MOTORS lamps are lighted. The diode (CRG101) connected between the BID and MOTORS lamps prevents the BID lamp from being energized when the MOTORS indicator switch is operated.

3.64 The negative voltage transition at pin B34 on flip-flop D-B, of ZA110 is inverted by PA-2C of ZA108 and applied at the input pin A32 of delay DY-A of ZA108. The output pin A34 is driven to 0 volt and remains at 0 volt for a period of 500 milliseconds. when it returns to a negative voltage. This negative transition is applied at the input pin A31, of PA-E on ZA108, and provides a positive pulse at the output pin A27. This pulse is again delayed by an identical delay circuit, the ‘pulse amplifier network. This results in a total delay of one second from the time a negative transition was obtained at pin B34. on D-B of ZA110 until a pulse is provided at the set input pin B24. on D-C of ZA110.

3.65 The associated prime input pin A24, was driven to 0 volt at the time flip-flop D-B was initially set by the BID indicator switch. The D-C Rip-flop is switched driving the inverted output pin B26. to -5 volts. This output is applied to the input pin B25, of LA-1C. ZA114.

3.66 The second input of LA 1C, pin A24 is supplied by the output of PA-1C on ZA108 which samples the normal output of D-B. The normal output pin B33, of D-B is driven to 0 volt at the time the BID switch is activated and allows PA-1C of ZA108 to provide -5 volts to the input pin A24 of LA-1C on ZA114. With both inputs of LA-K, ZA114 negative, the output pi A27 is driven to 0 volt. This 0 volt is supplied to the sequence control logic as a bid request.

3.67 The effect of inserting tape in the reader and operating the BID switch. is to immediately start the reader and winder motors and one second later provide a bid request to the sequence control logic.

3.68 **After operating the BID switch, the operator may cancel the bid request by operating the BID switch a second time before receipt of the on-line signal from the sequence control logic. This reset action obtains a positive transition at the complementary input pins, A36 and B36 of flip-flop D-B on ZA110. At this time the prime one input pin, A35, is at -5 volts because the output pin, B33 on D-B, is at 0 volt. This 0 voltage is applied to the input pin, B32 of LA-1D, ZA103 driving the output of this element to -5 volts.**

3.69 **At the same time, the prime 0 input pin, B35, is at 0 volt because the input pins, B22 and B23 of LA-2C, ZA114 are both negative. The input pin, B23 was driven to -5 volts through PA-1C of ZA108 at the time flip-flop D-B was first switched to the bid condition. The second input to LA-2C, ZA114 is the on-line signal from the sequence control logic. As long as the on-line signal remains negative, D-B is primed to reset. When the on-line signal goes to 0 volt the prime 0 input pin B35 is driven to -5 volts and** the ability to reset D-B with the BID switch is removed.

3.70 Flip-flop D-B can now be reset only by a reader tape-out indication in the form of a positive transition at the input pin 12, **of** inverter ZA301 where it is inverted and applied to pin **AS** of LA-1A, ZA305. If pin B7 of LA-1A is negative, at this time a positive transition will be applied at pins B32 and B27 of supplementary gates in ZA110 resetting flip-flop D-B and D-C. When D-B and D-C are reset the reader and winder motors are turned off and the bid request to the sequence control logic is removed.

3.71 The negative input at pin B7 of ZA305 is a result of LA-1C, ZA321 sampling either an off-line condition or an end of sequence. If neither of these conditions exist, the input at pin B7 will be at 0 volt and the tape-out indication will be prevented from resetting flipflops D-B and D-C. This logic prevents an incomplete start of message sequence to be transmitted when the tape lid is released during the sequence. The negative input at A6 of ZA305 is a result of LA-2A, ZA116 (refer to 7742WD, Sheet 4) STOP switch not being activated. Operating the STOP switch while the reader is on-line and reading tape, allows the output pin A10 of ZA116 to be driven negative. The resulting negative voltage is inverted by LA-2A of ZA116 and the output of 0 volt is applied to the input pin A6 of ZA305. This 0 volt at pin A6 prevents the tape-out contact from resetting flip-flops D-B and D-C of ZA110.

3.72 The power on, reset circuit at ZA401, is used to provide a collector set pulse to flip-flop D-B and D-C, a predetermined time after power is turned on. This action insures that the bid circuitry is not biding for the line when the equipment is turned on.

Start of Message Delete Circuitry

3.73 The number delete circuitry provides the operator with the option of deleting the number sequence which normally precedes each message tape. Prior to operating the BID switch the operator determines if the message tape requires a number sequence. If not, **the operator presses** the NUMBER DELETE switch, providing **a positive transition** at the input pins A36 and B36 **of flip-flop D-B on** ZA112, if the on line signal applied at ***pin* B14 of LA-1B,** ZA114 is negative. If this on-line signal is at **0 volt, indicating** the associated transmitter is on-line, the signal from the NUMBER DELETE switch is held at LA-1B, ZA114 and **does** not switch D-B of ZA112. Refer to 7744WD. Sheet 3.

3.74 With the -5 volts on-line **signal applied to pin B14** of LA-1B, ZA114 th**e indication from the** NUMBER DELETE switch is presented to pins A36 and **B36** of flip-flop D-B on ZA112. The D-B will be switched to the one state driving the output pin B34 negative. This -5 volts is applied to the input pin A4 of PA-2D on ZA108, driving the output pin Al to 0 volt, which energizes relay K4 and fights the NUMBER DELETE lamp through K4 contacts.

3.75 The negative voltage at pin B34 of flip-flop D-B is also applied as a prime at pin B26 of LA-1F, ZA103. The LA-1C. ZA103 is inhibited at this time due to the 0 volt supplied at pin B25 from pin B33 on D-B. **When** the BID switch is operated and D-B of ZA110 is switched as described in 3.62, a 0 to -5 volt transition is applied to pin A24 of LA-1C and pin A21 of LA-IF. ZA103. The output pin A27, of LA-1C. ZA103 is held at -5 volts due to the 0 volt present at input pin B25.

3.76 The output pin B28 of LA-1F, ZA103 is allowed to go to 0 volt due to -5 volts present at its other **input pin, B26. The resulting positive transition at the output of LA-1F, ZA103 is used to set flip-flop D-C of ZA112 into the one state driving pin B26 to -5 volts. This level is inverted by LA-1D, ZA114 and applied to the sequence control logic** as **a number delete signal.**

3.77 At the completion of a message the tape-out indication is received from the tape-out contact at the reader. This signal resets the bid circuitry as described in 3.70 and provides a -5 volt to 0 volt transition at pin B6 of PA-1C, on ZA108. This transition is applied to pin A30 of supplementary gate ZA112 providing a reset signal for flip-flop D-B of ZA112. With the reset of D-B, ZA112 the NUMBER DELETE lamp is extinguished. Refer to 7**744WD,** Sheet 2.

3.78 During normal operation (not in the delete mo**de)** pint B33 of flip-flop D-B is at -5 volts. This is applied to the pin B25 of LA-1C, ZA103 and permits a negative transition at pin A24 (3.75) to be inverted and passed to the flip-flop **D-C** as a reset signal. This pro**vides -5** volts indication at the **dele**te mode output, pin F7 of **JA128.**

3.79 A negative going transition, is received from the **start of message (referred to as SOM – module B panel) sequence generator at pin E7 on JA128, upon completion of the SOM sequence. The signal is inverted by** LA-2C, ZA305 and **applied to pin B31 of supplementary gate**

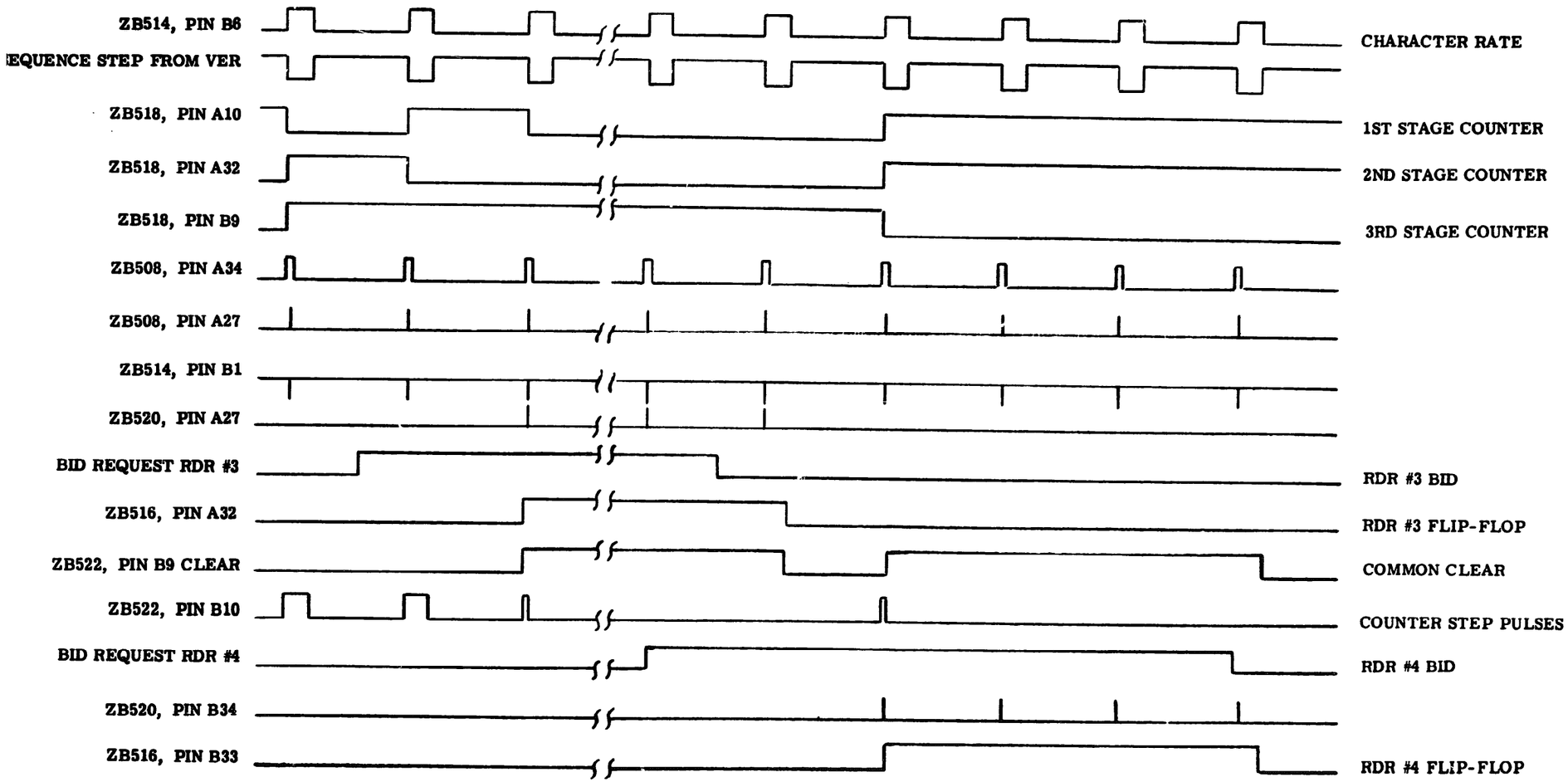


Figure 9 - Timing Diagram For Sequence Control

Figure 7 - Block Diagram for Master High Speed Tape Sender

ZA112 as a reset signal for flip-flop D-C. This reset signal is allowed to pass provided an on-line signal is present at the prime input pin A31, of supplementary D gate. When D-C is reset, the delete mode indication to the sequence control circuitry is changed to 0 volt. This permits the step pulses in the sequence control to be diverted from the SOM generator to the associated reader.

Step and Read Circuitry

3.80 During the reading operation, the operator has the option of stopping the reader and stepping it manually with the STEP READ switch. This circuit starts functioning when the STOP switch is operated and the associated STOP lamp is lighted. A level change from 0 to -5 volts is obtained at pin B4 of LA-2A, ZA103. Here again the output of a switch is fed through a dc (direct current) flip-flop configuration to remove contact bounce. Refer to

3.81 When the reader is operating, the on-line signal input at pin B5 of LA-2A, ZA103 is -5 volts. As a result of the negative level being applied to pin B5 of LA-2A, ZA103 and the level change from 0 to -5 volts at pin B4, due to the STOP switch output, pin A9 is driven to 0 volt. This 0 volt is used as a reader stop signal and as a prime to flip-flop D-F of ZA110. The signal is used to inhibit the step pulses to the SOM generator or the reader, thereby stopping operation.

3.82 The prime voltage applied at pin A2 of flip-flop D-F permits the positive transition, appearing at the set input, pin A1, to switch the flip-flop, driving the output pin, B3 to -5 volts. The positive transition at the input pin A1 is a result of operating the STEP READ switch. The output pin B3, of flip-flop D-F on ZA110, is inverted by LA-2E, ZA116 and supplied as a step read pulse. This pulse allows the reader to be stepped one character, and the character read by the reader to be transmitted on-line. To allow the reader to be stepped automatically by the incoming step pulse rate again, the operator presses the STOP switch returning it to the normal condition.

3.83 The reader may also be manually stepped off-line during periods when the reader is nor normally being stepped by the incoming pulse rate. The STEP switch output is fed to a dc connected flip-flop configuration consisting of LA-1B. and LA-2B on ZA116. When the STEP switch is operated. a positive transition is obtained at the output pin **A11,** on the dc flip-flop. This transition is applied to **LA-1B, ZA103,** for inversion prior to being applied to the nput pin B13, of **LA-2B. ZA103.**

3.84 If the second input pin, **B12** of LA-2B is negative at this time, the input at pin **B13** will be inverted and appear at the output pin, A11. The input level at pin **B12** is 0 volt only when the STOP switch is in its normal position and at the time the on-line signal input is at pin B23 of LA-2c. ZA103 -5 volts. When this condition is met it is assumed the reader is normally being stepped by the incoming pulse rate, the manual step indications must be held.

3.85 switch is available for stepping the reader manually except when the reader is normally reading tape and stepped by the incoming step pulse rate received at pin D10 of JA128.

3.86 Assuming the input pin B12 of LA-2B, ZA103 is at -5 volts, the manual step indications at input pin B13 appear inverted at the output pin, A11. Then they are inverted twice by LA-2F, ZA103 and LA-1F, ZA116. At the output the manual step indications appear as positive transitions which are applied to the driver assembly.

3.87 The driver assembly is located in the tape transport assembly and functions to change the low-level stepping pulses to a power level adequate for energizing the reader stepping coils. The stepping pulses delivered to the driver assembly come from two sources, one is the STEP switch described in 3.83, and the other is the sequence control circuitry in the master logic, which are applied to pin D10, JA128.

3.88 The LA-1A of ZA321 perform the function of preventing an alum indication from occuring when the reader is restarted after it has been stopped and manually stepped by means of the STEP switch. This circuit is required due to the characteristics of the verify logic.

3.89 The description of the following circuit is the same as described in 3.88. Input pin A7 of LA-1A, ZA321 samples the condition of the STOP switch. With the **STOP** switch in the stop condition, this input is -5 volts. Pin B7 of LA-1A, ZA321 samples the on-line signal which is -5 volts and on at rhis point. The third input pin, A6 of LA-1A. **ZA321** samples the **STEP** switch output at pin A17 of **LA-1B,** ZA103. When the STOP switch is operated again, pin A6 of LA-IA, ZA321 is at -5 volts. and the output pin A10 is driven to 0 volt. This positive transition is applied to the verifier logic where it is used to prevent an alarm on reader start-up when the contacts are again sampled.

Alarm Circuitry

3.90 There arc two types of alarms provided in the reader logic. a **VERIFIER** alarm and a TAPE FEED alarm. If either of these two errors occurs, an indication is received at pin **A8 or B8** of **JA128,** setting an associated flip-flop D-D **or D-E** of ZA110. These flip-flops arc primed by the presence of an on-line indication. When either of the two flip-flops is set, an associated alarm lamp is lighted and a 0 volt indication is applied at either pin Al or **B1** of LA-2E, ZA103. The output pin **B9** of **LA-2E.** ZA103 is inverted by **LA-1E.** ZA116 and supplied to the verifier as a 0 volt alarm signal. Refer to 7744WD, Sheer 5.

3.91 To reset the alarm flip-flops and extinguish the alarm indicator lamp or lamps. the operator presses the affected alarm switch An on-lilac indicator lamp is lighted when the on-line signal is received. This indicator lamp informs the operator when a particular reader is allowed to transmit after a bid for the line has been entered.

3.92 **The primary fur.ctions of the parallel to serial converter are as follows: (Refer to 7744WD, Sheets 6 and 7, and Figure 8 for block diagram).**

(a) Accepts an eight-level parallel signal, 0 volt for mark and -5 volts for a space, and converts this signal into a serialized signal output, +6 volts for mark, and -6 volts for space.

(b) Accepts a clock pulse input at the bit rate which determines the speed of operation.

(c) Provides a reader step pulse output at the character rate.

(d) Capability of working five through eight-level operation, start-stop or synchronous.

(e) Optional parallel signal output is provided.

3.93 **The parallel to serial** converter, hereafter referred to as converter. inclu**des** a four stage binary counter which is capable of a maximum count of 16. It is also capable of being reset at a specific count by the UNITS PER CHARACTER INTERVAL switch. hereafter referred to as UPC1 switch (module A). which will be explained laocr.

3.94 The counter is reset by a positive pulse coupled through diodes to the 1 side of flip-flops D-B. DC. DE, and D-F of ZA307. The positive pulse coupled to flip-flop D-B is first fed through the SIGNAL MODE switch (module A). When the SIGNAL MODE switch is in the START-STOP position. the 1 side of flip-flop D-B is reset to 0 volt by the reset pulse. When the SIGNAL MODE switch is in the SYNCHRONOUS position. the 0 side of flip-flop D-B is set to 0 volt by the reset pulse.

3.95 Clock pulses. +6 volts to -6 volts. arc fed to input circuit ZA302-A. pin 34. The input circuit converts the polar clock from 0 to -6 volts signal. 0 volt corresponding to a +6 volt input. while -6 volts corresponds to a -6 volt input. This neutral clock is inverted by LA-2D). ZA305 and fed to the input of the binary counter. The output of LA-2D on ZA305 also feeds LA-2B on ZA305. Since the clock has been inverted by LA-2D, ZA305 the counter counts at the negative going clock transitions. The outputs of all stages in the binary counter arc fed to power amplifiers which in turn feed the UPC1 switch. Refer to 7744WD, Sheet 10.

3.96 NOR gates LA-1A. LA-1B, LA-K, LA-1D, LA-1E, and LA-1F of ZA314 and LA-1B, LA-1D, and LA-1E of ZA305 and their associated OR gates ZA313-22, 21, 28, 19, 18, 17, 16, 15, and 14 detect the count in the counter. When the counter is reset in the start-stop mode, pins A32. B33 of LA 1D on ZA305, and pins A13 and B13 of OR gate ZA313-1 arc at -6 volts. The output of LA-1D, ZA2X305 is then dependent upon the other input pin B32.

3.97 **LA-1D, ZA305 samples the contents of flip-flop D-E of ZA319 when the counter is at the reset state. When there is a count of one in the counter, the output of LA-1E, ZA305 is dependent upon the input at pin B6 which samples flip-flop D-D of ZA319. Flip-flops D-F of ZA319, D-C, D-F, D-E, and D-D of ZA317; D-B, D-C, D-D, and D-E of ZA319 are sequentially sampled, each for the duration of the bit clock period. When the SIGNAL MODE switch is in the SYNCHRONOUS position, flip-flop D-E of ZA319 is not sampled.**

3.98 **The flip-flops mentioned in 3.97 stores information supplied from the verifier. If the one prime is at 0 volts, the flip-flop will store a mark when a complementary input is supplied a positive pulse. If the 0 prime is at 0 volt, the flip-flop will store a space. The primes for the storage flip-flops determine whether a mark or space is stored in a particular level. At the time a positive pulse is applied to the converter for reset, a character shift pulse is also applied to the complementary inputs of the storage flip-flops.**

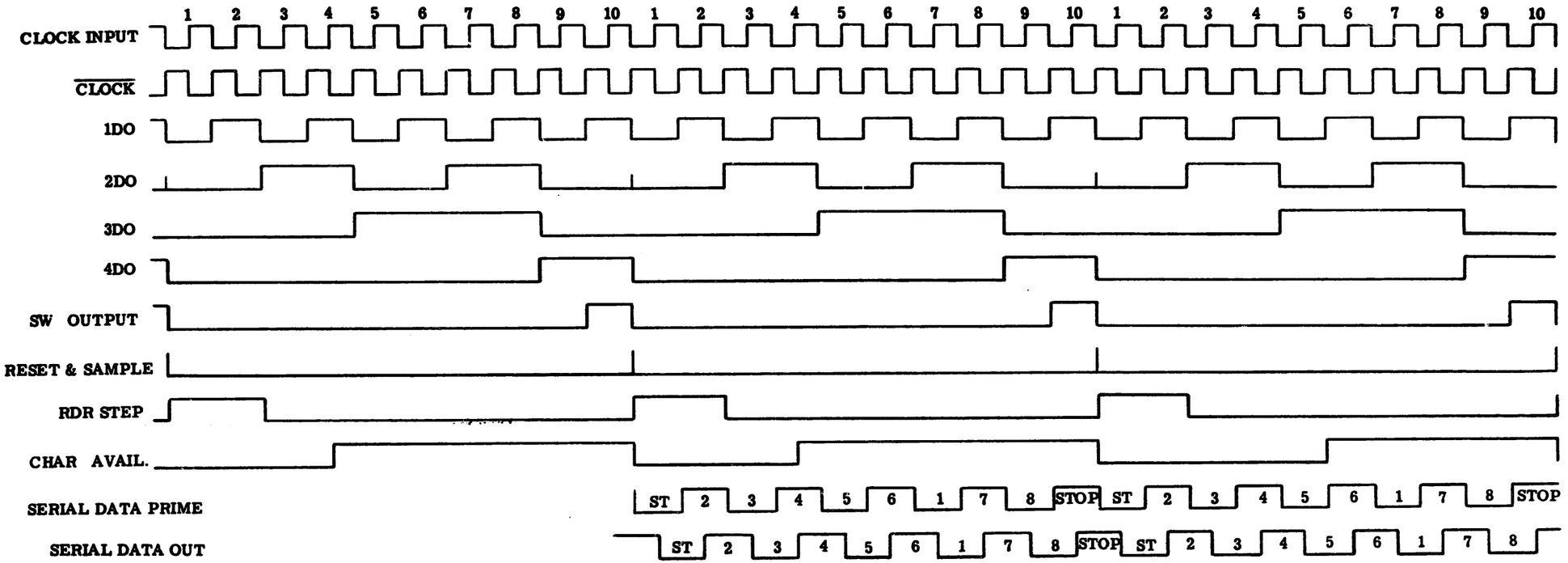
3.99 **The output of the storage flip-flops are fed to program board ZA316 where the customer has the option of either sampling the 1 or 0 sides of the flip-flops. When the 1 side is sampled, a mark at the input will be sampled as a mark at the output. If the 0 side is sampled, a** mark at the input will be sampled as a space.

3.100 The output of NOR gates LA**-1A, LA-1B, LA-1C,** LA-1D, LA-1E and LA-1F of **ZA314, and LA-1B,** and LA-1E of ZA305 are fed to LA-1F**, ZA305. The output** of LA-1D. ZA305 is fed to NOR gate **LA-1F, ZA305 only** when the **SIGNAL MODE switch is in the START-STOP** position. The output of **LA-1F**, ZA305 is the serial out**put. A** 0 volt output of LA**-1F, ZA305 represents a mark while a -6** volt level represents a space.

3.101 The counter can accept up to sixteen clock pulses before recycling. The number is dependent upon the position of the UPC1 switch. If the switch is positioned so the counter counts above eight, each subsequent clock pulse will generate a mark or stop condition, until the counter is reset and again samples the storage flipflops.

3.102 Levels eight, seven, and one from the verifier are fed through NOR gates 1-F. 1-D. and 2-D of ZA321, respectively. The outputs of these gates are fed to the converter. revels six, five, four, three and two from the verifier are fed directly to the converter. The character available signal from the verifier also feeds the converter.

3.103 The CODE LEVEL switch (module A), determines the number of code levels that arc transmitted. When the switch is in the five-level position a 0 volt level is fed to NOR gate 1-F, 1-D. and 2-D of ZA321 which inhibits these gates. When the switch is in the six-level position. NOR



SWITCH SET FOR 10 UPCI

Figure 8 - Timing Diagram for Parallel to Serial Converter

gates 1-F and 1-D are held and so on through seven and eight levels. When a level is held in this manner, a mark is generated when the storage flip-flop which stores that particular level is sampled.

3.104 The parallel signal output from the verifier is also passed through output circuits ZA323-S, ZA324-B, ZA325-A, ZA325-B, ZA324-A, ZA325-C, ZA324-C, and ZA323C. The output circuit converts its neutral input, 0 to -6 volts to a polar output +6 to -6 volts respectively. The output circuits drive integrators, and time constants are determined by the customer. The outputs of the integrators are optional parallel signal outputs.

3.105 The character available signal from the verifier is also fed to the set input two millisecond delay ZA311-A whose prime is permanently grounded. The normal output is fed to output circuit ZA326-A, and the auxiliary character available output is a two millisecond wide positive pulse.

3.106 The UPC1 switch is a four section switch which samples the outputs of the binary counter. The four poles of this switch are fed to NOR gate 1A of ZA303. Pin A8 of this gate is fed from OR gates ZA313-13 and 12 which sample the send number lead from the SOM generator. The send number is strapped to either JA128-G4, H4, G3, or H3. During the SOM sequence, the send number lead is a 0 volt which inhibits LA-IA of ZA303, and disables the UPC1 switch.

3.107 The output of LA-IA, ZA303 primes pin B4 of LA-2A, ZA303 for its other input pin ES. The latter gate thus samples the combined outputs of NOR gates 1-F, 1-D, 1-B and 1-C, of ZA303. Depending upon where the send number lead is strapped. one of the above named NOR gates will k primed while the others will be inhibited during the SDM sequence. The other inputs of these gates sample the outputs of the binary counter.

3.108 If the send number lead were strapped to JA-128H3. a count of nine in the counter will place a -6 volts at all the inputs of LA-1C. ZA303 which drives the output to 0 volt. This 0 volt level is fed to already primed LA-2A on ZA303 which inverts the signal and feeds -6 volts to the converter. This -6 volt level is then inverted again by NOR gate LA-2A and LA-2C of ZA314 and appears as a 0 volt level for a count of nine in the counter.

3.109 The outputs of NOR gates LA-2A and LA-2C of ZA314 are fed to PA-I' and PA-E of ZA311. When the next clock pulse steps the counter. the output of LA-1C of ZA303 drops to -6 volts. Consequently a negative transition appears at the input of PA-F. and PA-E of ZA311. The positive pulse resulting from the negative transition resets the counter to either 0000 or 0001 depending upon mode of operation.

3.110 The positive pulse at the output of PA-E, ZA311 is fed to the complementary inputs of the storage flip-flops. It is at this time that the information from the verifier is fed into storage and becomes the next character to be transmitted. The positive pulse is also fed to the set one input of flip-flop D-B of ZA317. Refer to 7744WD. Sheet 10.

3.111 At the end of the SOM sequence, the send number lead goes to -6 volts and holds LA-1C of ZA303 placing a -6 volt level at pin A8 of ZA303. NOR gate LA-IA, of ZA303 now samples the UPC1 switch. Depending on the position of this switch the counter is either reset on the sixth through sixteenth clock pulse (START-STOP) or fifth through sixteenth (SYNCHRONOUS).

3.112 Flip-flop D-B, ZA317 is reset when the counter steps to a count of two. The normal output of flip flop D-B is fed to LA-2E of ZA303. At the output of this gate there are negative pulses whose duration is either one or two clock pulses, depending upon the mode of operation. The interval between leading edges is determined by the UPC1 switch or send number strap connections (during the SOM sequence). This is the character interval. The output of NOR gate LA-2E of ZA303, the reader step lead, is fed to the verifier where it is used to generate various timing sequences.

3.113 The serial data output from LA-1F of ZA305 primes flip-flop D-D of ZA307. LA-1E of ZA303 inverts the serial data input applied to the prime 0 of the flip-flop in such a way that if the 0 side is primed, the one side prime is at -6 volts or the sequence may be reversed. The bit sample from the converter (which is at clock pulse time) is fed to the complementary input of flip-flop D-D, ZA307.

3.114 Previously it was stated that the counter was stepped by the inverted clock, with the bit sample at clock pulse time. Thus, flip-flop D-D is primed a half of a bit time before bit sample occurs. The output of flip-flop D-D is fed to output circuit ZA323-B where a +6 volt output represents a mark while -6 volt output represents a space.

3.115 A polar (+6 volts) abnormal traffic indication signal on input connector JA128 pin C4 is fed by external equipment to input circuit card ZA302. The output of this input card is fed to PA-1C of ZB1315. input pin A9. The output load of this power amplifier is from the coil of relay KB501-B.

3.116 With the abnormal traffic input positive, relay KB501-B is de-energized and the associated contacts arc open. Driving the abnormal traffic input negative energizes relay KB501-B. The relay contacts close providing a ground return for the abnormal traffic indicator lamp on the master and supplememtary reader cabinets.

C. Sequence Control

3.117 The sequence control logic assures that only one reader out of the six is capable of supplying signals to the verifier at any one time. (Refer to 7744WD, Sheets 13 and 14.) The circuitry shown on Sheet 13 provides for bid request inputs from up to six readers. Since the logic for each reader is identical, the sequence of operation will be described for reader number three only.

3.118 When a bid request (0 volt) is received at pin G2 of JB128 it is inverted twice by LA-X, ZB520 and LA-2F, ZB505. An inverted signal is taken from pin A26 of ZB520 to k applied to pin B25 of the flip-flop ZB516, D-C as a reset prime. The bid request input therefore primes the flip-flop at pin A24 in preparation for a set one input at pin B24. This pin receives a zero transition from the output of LA-1C, ZB520 at a time when all inputs of this gate go to a -5 volt level. Three of the inputs to this gate sample the output collectors of a three stage counter composed of flip-flops D-F, D-C and D-E, ZB518.

3.119 The one side of the first stage is sampled at pin B24, the one side of the second stage is sampled at pin B25, and the zero side of the third stage is sampled at pin A24. The fourth gate input is a character clock signal. The third step pulse input to the counter, along with the character clock input at pin A32 of LA-1C on ZB520, results in an output at pin A27 of ZB520 as shown in Figure 10. The bid signal input primes pin A24 of flip-flop DC. ZB516 at this time, as shown on Figure 10. The output of ZB520, pin A27 when applied to pin B24 of flip-flop DC, causes it to go to the set condition (Figure 10).

3.120 The resulting 0 volt at pin A32 of flip-flop D-C is also applied to NOR gate LA-1E. ZB522 where it is used as an inhibit signal for subsequent step pulses arriving at pin A2 of this gate. (Figure 9, shows these step pulses being inhibited.) The inverted output of flip-flop D-D, pin B26, which was driven to -5 volts when the flip-flop was set, drives PA-K, ZB508 into saturation.

3.121 The output pin B16 of the power amplifier provides a 0 volt on line signal to the reader logic. This signal is also applied to pin B5 of PA-2C, ZB508 driving the output pin B4 to -12 volts, de-energizing relay K-3. This opens the associated contacts and removes the ground normally supplied to the verifier logic, permitting the contacts of the associated reader to be sampled.

3.122 The inverted output side of flip-flop D-C. ZB516 also supplies a negative on-line signal to the sequence control logic. The timing diagram, Figure 9. shows the sequence of operation when reader three is given the on-line signal as described in the preceding **paragraphs. When** transmission for reader three is completed. reader four is given the on-line signal. The step clock gating circuitry. shown on 7744WD, Sheet 15, performs the function of directing the step pulses to the start of message generator or to any one of six readers. The gate network for all readers are identical so the operation for only reader one will be described.

3.123 Whether the step pulses are to be initially directed toward the start of message generator (normal condition) or the reader drive circuitry (delete mode) is dependent upon the delete prime input voltage from the reader logic. When in the normal condition (a start of message sequence is to proceed the message tape) this input voltage is negative. The negative voltage is applied at pin A7 of LA-IA, ZB524 and acts as a prime. It is inverted by LA-2E, ZB524 and applied as an inhibit signal to pin B14 of LA-1B, ZB524.

3.124 A second input to LA-IA, ZB524 is the negative on-lint signal (assuming reader one has the clear line to send) which is applied at pin B7 and also to pin B15 of NOR gate LA-1B, ZB524 as a prime voltage. Two of the three inputs to LA-IA, ZB524 are now primed. The third input, pin A6 receives negative read pulses from the output of LA-2B, ZB524, and LA-1B, ZB524 receives negative step pulses at pin A13. Since one input of LA-1B, ZB524 is at 0 volt, the output pin A17, remains at a negative voltage while the output pin A10 of LA-1A, ZB524 supplies positive pulses to the input pin B31 of LA-2D, ZB526.

3.125 The result is a negative pulse output at pin A28 which is supplied as a step pulse to the start of message generator. At the end of the fourteenth character start of message sequence the delete prime input from the reader logic changes to 0 volt. This drives the output of LA-1A. ZB524 to -5 volts and primes LA-1B, ZB524. The negative pulses appearing at pin A13 of this gate are inverted and appear at the output pin A17. as positive step pulses to reader one. These pulses are also fed to the verifier for alarm purposes.

D. Verifier

3.126 This logic accepts a step pulse from the parallel to serial converter at the character rate. The functions performed are listed in the three following groups:

(a) Inhibiting the step pulse in alarm conditions, and in the stop mode.

(b) Allow a step pulse to be passed when manually stepping the reader.

(c) Generate time slots within the character period, and reference the step pulse for reader contact sampling and verifying.

(d) Stopping the reader externally.

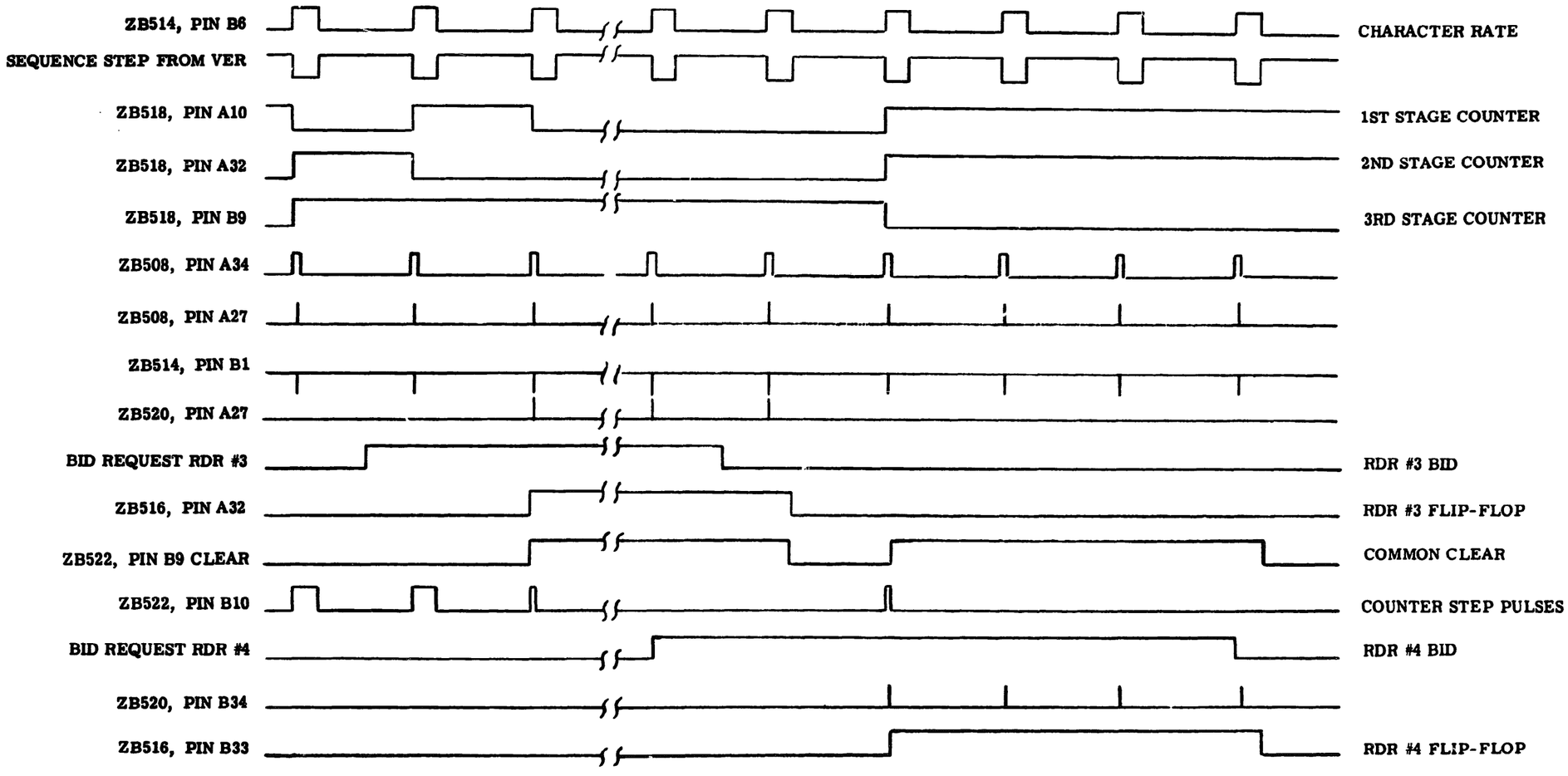


Figure 9 - Thing Diagram For Sequence Control

3.127 The **reader step** input is applied **at pin C2** of **JBl28** as a negative pulse (Figure 10). **This** pulse is **inverted by PA-2D). ZB514** and is **used to trigger a 50 microsecond delay (DY-A, ZB319).** The 50 microsecond delay is used **to delay** the application **of the step pulse** at the input, pin **A3 of PA-2D). ZB319** until after a reader stop **an** has had time to be applied to one of the **seven inputs to LA-1C, ZB324.** The reader **stop signal may be applied at** any time during reader operation or at the time a reader is given one on-line signal.

3.128 In the latter case **the** on-line to the reader logic occurs at reader step time. Therefore the reader stop signal from the master reader control or from any one of the five supplementary reader controls will be applied at one of the seven inputs to LA-1C, ZB324 at the reader step time, causing the input pin A4 of PA-2D, ZB319 to be driven to zero. disabling the input at pin A3. Fifty microseconds later the delayed step pulse will be applied at pin A3. This action permits **the** operator to bid for the line with the reader logic in the stop mode. Then manually step through the start-of-message sequence or the message tape when in the number delete mode. The seventh input to LA-1C, ZB324 pin B25, inhibits step pulses when an alarm condition is present. The eighth input to LA-1C, ZB324 pin A25, is applied through pol/neut converter ZA302 and **CR-B,** ZB108. This input is the remote stop-send signal which permits stopping the reader from a remote location.

3.129 Pulse amplifier PA-E, ZB319 provides a positive pulse at the trailing edge (negative transition) of the 50 microsecond delay (Figure **10).** The pulse is inverted by LA-X, ZB324 and applied to pin A3 of PA-2D, 28319. If a 0 volt (reader stop), signal is not present at any one of the eight inputs of LA-1C, ZB324 a positive level will appear at the output pin, A27. This level under normal conditions will be inverted by **LA-2B,** ZB522 and applied as a negative input at pin A4 of PA-2D, ZB319. The pulse appearing at pin A3 is **then** allowed to **pass** to the output pin A1, **as** a positive pulse.

3.130 If a 0 volt (reader stop) signal is present at one of the inputs to OR gate LA-1C, ZB324 (Figure 10) the output pin A27, is driven negative. This prevents the passage of step pulses at PA-2D, ZB319, pin **A3** by the presence of 0 volt at pin A4. The following paragraphs explain how a single step pulse is developed after a reader stop signal has been received.

3.131 A positive manual step signal is applied at one of the six inputs to LA-1A. ZB324 (Figure 10). It is inverted twice and used as a prime one pulse at pin **B14** of flip-flop D-D, ZB322 which is then set by the next step pulse. Flip-flop D-D and D-C, are normally in the reset state (pins B22 at 0 volt and A32 at -5 volts). When power is turned on, the flip-flops do not assume this state, the normal flow of step pulses at pins A22 and A25 will cause the flip-flops to be **driven into** this state.

3.132 When flip-flop D-D is set the output pin A22, is driven to -5 volts. Both inputs to LA-2C, ZB522 are now at -5 volts, allowing the output pin A26 to go to 0 volt which is used as a prime one input, for **flip-flop D-C, ZB322,** pin A24. On arrival of the next step pulse at pin **A25 this** flip-flop is driven to the set one state, allowing the output pin A32 to go to 0 volt [Figure **10). This** 0 **volt is** applied at pin **B12** of LA-2B, ZB522 and drives the output pin **A11,** negative.

3.133 The negative voltage at pin **A11 is** used as a **prime at** pin **A4 of PA-2D, ZB319. Fifty microseconds later** a negative pulse is applied at the second input pin **A3 of this gate** causing a positive pulse output at **pin A1 (Figure 10).** This pulse has the same time reference and is **used to perform** the same functions as the normal step pulse stream, but only one pulse is generated for each application of a manual step pulse.

3.134 After flip-flop D-C of ZB322 has **been set, it** primes itself and flip-flop D-D, ZB322 for **reset. The** output pin A32, is. 0 volt at this time. This 0 volt is applied at pin B22 of LA-2C, ZE522 and removes the prime one voltage at pin **A24** of ZB322. Pin B23 of flip-flop D-D and pin B25 of flip-flop D-C are primed for the following reader step pulse which resets both flip-flops.

3.135 The step pulses are passed through PA-2D, ZB319. The second input pin A4, of this element is -5 volts at this time. If there is no alarm indication from any one of the six readers as sampled by NOR gate LA-1E, ZB324 (7744WD, Sheet 19), and no voltage supplied to pin B25 of LA-1C, ZB324 or no external stop-send signal at pin 24 of JG106, the voltage at pin A4 of **PA-2D will** remain at -5 volts.

3.136 When an alarm indication is received. the voltage at pin A4 of the power amplifier is driven to 0 volt. This prevents step pulses appearing at pin **A3** to be passed to the output pin A1, thereby stopping reader operation. This 0 volt is **also** applied at the input pin B3. of PA-1D. **ZB319** (Sheet **19)** which de-energizces the alarm relay KB-501-A. When KB-501-A de-energizes. the transfer contact at pins **B1. C1,** and D1 of JB328 **changes** state. This indication of an alarm is supplied to external equipment.

3.137 During normal operating conditions reader step pulses are present at the output of **PA-2D). ZB319,** pin **A1.** From here the pulses are fed to the sequence control logic for stepping either the start of message generator or the reader. The step pulses arc also applied to the input pin A22 of the 800 microsecond delay DY-B. **ZB317.** The output is taken from the normal side, B27 and is au 800 microsecond positive pulse. At the trailing edge of this pulse. a positive pulse is developed by PA-F, ZB512. pin B11 (Figure 10), where it is inverted by PA-2C, ZB319 and applied as **a** negative reset pulse to the verifier logic.

3.138 **This reset pulse** the first of four time **slots** which are referenced to the step pulse and are developed within each character period. These time slots are used for reading and verifying the reader contact information. The reset pulse is used to reset the contact sampling circuit prior to reading a new character.

3.139 The second time slot is developed by 1.6 millisecond **delay,** DY-A, **ZB317** and **PA-F, ZB317.** The output pin B11 of ZB317 is inverted by **PA-2D,** 2B317 and is applied as a negative verifier sample pulse to the verifier logic. This pulse is used to sample the reader verifying contacts, and occurs 1.6 milliseconds after the reset pulse or 2.4 milliseconds after the step pulse (Figure 10).

3.140 The third time slot is developed by 110 microsecond delay **DY-B, ZB315** and **PA-E. ZB317.** This pulse is used to set the verifier alarm flip-flop D-B, ZB322 if a verifier error indication is present. The positive pulse output of pin **A27, ZB317 (Figure 10) is** inverted by LA-2D, ZB324 and applied to pin B5 of NOR gate LA-2A, ZB324. If the second input of this gate is -5 volts at this time, the pulse will be applied at the set one input pin A36, of flip-flop D-B, sampling the prime at pin A35 (refer to 7744WD, Sheet 19).

3.141 Pin B4 of LA-2A, ZB324 receives its voltage from the inverted output, Pin B10 of flip-flop DE, ZE322 (refer to 7744WD, Sheet 18). This flip-flop is normally reset, making the output 0 volt, due to the reset pulse being fed to the 50 microsecond delay, DY-B, ZB319. A pulse is also generated by PA-E, ZB512 and applied to the reset input pin **B12** of ZB322. The output pin B10, is not driven to -5 volts until an on-line and not send number signal is present at the prime one input pin A12, and a set pulse is applied at pin All.

3.142 This set pulse on pin All is developed by the 110 microsecond delay DY-A, ZB315, and PA-E, ZB315. It is the fourth and last time slot developed during the character period, and determines the time that the character being read by the reader contacts is placed in the verifier storage. This is the pulse that sets flip-flop D-E, driving pin B10 to -5 volts. Pin B4 of LA-2A, ZB324 (refer to 7744WD, Sheet 19) will not be primed until the first read pulse has occurred after an on-line is present. Therefore, the first verifier alarm sample pulse is inhibited.

3.143 The prime for the verifier alarm flip-flop D-B, ZB322 is applied at pin A35 and is supplied by the output of NOR gate LA-1B, ZB324. If all inputs of this gate are -5 volts the output is 0 volt (error condition). Input B15 is supplied by the start of message generator and is driven to 0 volt when this circuit is generating a sequence. This input inhibits a verifier alarm during the start of message sequence.

3.144 During normal reader stepping B15 of LA-1B, is at -5 volts and the second input pin A14, is at 0 volts until an error is detected. When an error is detected, input A14 is driven **negative** causing the output pin A17 to go to 0 volts, priming flip-flop D-B for the next alarm sample pulse.

3.145 When the verifier alarm flip-flop D-B is set, pin B33 goes from -5 volts to 0 volt, which is inverted by **PA-1C,** ZB319 and supplied as a negative alarm indcation to the reader logic. The alarm flip-flop is reset by the following reader step pulse applied it pin B36.

3.146 flip-flop D-F, ZB322 (refer to 7744WD, Sheet 18) is used to provide a character available signal to the parallel to serial converter and the signal gating. The flip-flop is normally reset by the delayed alarm sample pulse input at pin B1. When on on-line signal is received at the prime input pin A2, the next read pulse applied at pin A1 will set the flip-flop and provide a character available signal. It remains in this state until the next step pulse at pin B1, causes the flip-flop to reset.

3.147 If an on-line signal is still present for the next character, the following read pulse will again set the flip-flop to the character available state. This action continues until the on-line is removed or an alarm condition inhibits the read pulses causing the flip-flop to remain in the reset state.

3.148 To prevent generating a character on the line when in the external stop-send mode, a signal is received from a remote source on pin 24 of JG106 (which is normally at -6 volts). The output pin 9 of ZA302 is driven from -6 volts to 0 volt. This 0 volt is placed at input pin A25 of LA-1C and input pin Al2 of LA-2B, ZB324 through isolating diodes CR-E and CR-B of ZB108 respectively. The output pin 27 of LA-1C, ZB324 is driven negative. This puts 0 volt at input pin A4 of PA-2D, ZB319 and prevents the passage of step pulses at pin A3 of PA-2D, ZB319. The presence of 0 volt at input pin Al2 of LA-2B, ZB324 inhibits the step-read pulse at pin B12 of LA-2B, ZB324 to Pass to the output pin A11, thus preventing transmission.

3.149 The verifier logic performs the function of sampling the code reading and verifier contacts of the operating reader, placing the code reading information in storage and later clearing the storage with the verifier information. The outputs of the storage register, supply an alarm condition at the alarm sample time. if all levels of the registerare not properly cleared by the verifier information prior to this sample time.

3.150 Input provisions are made for 6 readers with 17 contacts per reader; 8 reading, 8 verify and 1 feed. Since the logic for all Ievels is identical, only level number one will be described.

3.151 Assuming reader number one is operating, the code reading contact indication is applied at pin A10 of JB228 (refer to 7744WD, Sheet 16). The verifier contact indication is applied at pin C10 of JE228, The contact

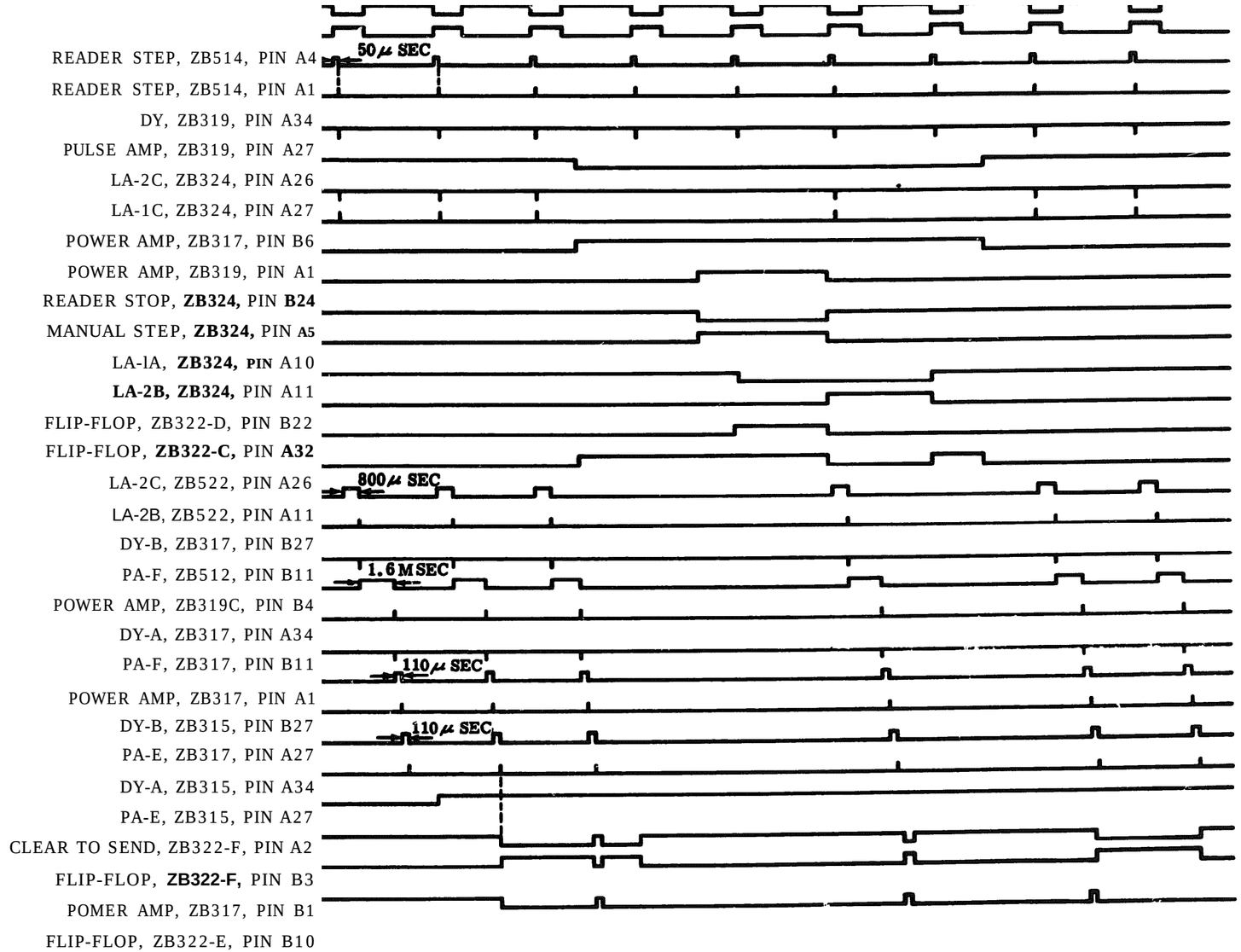


Figure 10 - Timing Diagram for Verifier

configuration for each input is as shown in the reference block. When the contact is detecting a hole (mark) it is closed to ground. When the contact is detecting no hole (space) it is open.

3.152 The code reading contact signal at pin **A10** of JB228 is applied to pin B26 of NAND **gate.** has been It will be permitted to pass to the output pin **A29,** sequence the inhibited input appearing at pin B6 of the **gate** only the opened. The other five inhibit inputs from the sequence control are held at ground at this time permitting only the contact signals from reader number one to be capable of supplying an output at pin A29.

3.153 When the contact detects a hole (mark) the output pin A29 of the gate goes to -5 volts. When a no hole (space) is detected the output is driven to 0 volt. These levels are inverted by LA-1D. ZB118 resulting in 0 volt for a mark and -5 volts for a space at the output pin B34. This output is applied to LA-2D, ZB118 which is connected in conjunction with LA-IF. ZB118 to function as a dc flip-flop.

3.154 With a mark being read by the contact, 0 volt is applied at pin B31 of LA-2D driving pin A28 to -5 volts. This -5 volts is applied to pin B36, of LA-1F. With the second input of this gate at -5 volts the output pin B28 is driven to 0 volts which is fed back to LA-2D at pin B30 clamping the network into the mark condition. The 0 volt present at the output of LA-1F is also applied to pin A29 of supplementary D gate ZB108 where it is used as a prime for the read sample pulse applied to pin B30.

3.155 The output of LA-2D which is -5 volts this time is applied at pin A30 of supplementary flip-flop ZB108 inhibiting the read sample pulse applied to pin B32. Flip-flop D-B, ZB108 is now primed to be set on the arrival of a read sample pulse, which will drive pin B33 to 0 volt. This mark condition will remain in storage until the next character.

3.156 At the beginning of the next character period, the reader is supplied a step pulse, 800 microseconds later a reset pulse is generated and supplied as a positive pulse to pin A34 of LA-1F, ZB118. At this time the reader has stepped and is now reading the next character due to the step command of the previous character. Assuming the character now being read is a space, the voltage applied at pin B31 of LA-2D is -5 volts.

3.157 When the reset pulse is applied to LA-1F. pin B28 is driven to -5 volts which is fed back to pin B30 of LA-2D. This results in pin A28 going to 0 volt and holding the output of LA-IF at -5 volts. The dc flip-flop has thereby been reset by the application of the reset pulse and is reset because the reader output is spacing.

3.158 **The next pulse occurring after the reset pulse is the verify sample pulse. This negative pulse is applied at pin** A7 **of** LA-1A, **ZB110 and is used to** sample **the output of the dc flip-flop network consisting of LA-2C and LD-2D,** 118. This output is applied to pin A6 of LA-IA.

3.159 **The gated NAND, ZB124-B is now sampling the readers verify contact, which at this time should be reading the bit previously under the read contact. Since that bit was a mark, the voltage at the gated output pin A31, is -5 volts. This -5 volts is inverted by LA-1C, ZB118 and applied to the input pin B23, of LA-2C, ZB118 driving the output to -5 volts. This voltage is sampled by the verify sample pulse.**

3.160 When it is -5 volts, **a** positive pulse is developed **at** the **output pin** A10, LA-1A of ZB110 which is applied to complimentary input pin **A36,** of flip-flop D-B. This pulse resets the flip-flop (which was set previously) driving pin B33 to -5 volts to remove the alarm indication.

3.161 The next time slot in the character period is the alarm sample pulse. This occurs 110 microseconds after the verify sample pulse. If the 0 volt at pin B33 of flip-flop D-B has not been removed by the verify sample pulse. the alarm sample pulse causes an alarm. If the code reading contact had supplied a space indication instead of a mark, flip-flop D-B would have been reset at the time of **the** read sample pulse.

3.162 One character after the read sample pulse, the verify contact would have indicated a space. which would have resulted in the inhibit voltage at the input of LA-1 A. This prevents the verify sample pulse from reaching the complementary input pin A36. of flip-flop D-B. The flip-flop remains in the reset state (pin B33 at -5 volts) and no alarm condition is detected by the alarm sample pulse which occurs 110 microseconds later.

3.163 All eight levels are treated in the same manner. When a mark is detected by the code reading contact. the storage flip-flop is set at the read sample time. If a space is detected the storage flip-flop is not set. One character later, if **a** mark is detected by the verify contact, a complementing input pulse is applied to the flip-flop. If a space is detected the complementing input pulse is inhibited and the flip-flop is not switched.

3.164 Logic identical to that described in the preceding paragraph pertaining to levels 5,6,7, and 8 appears on Sheet 17 (7744WD). The logic appearing on Sheet 20 is used for sampling and detecting a reader feed error. Gated NAND ZB120-A, samples the feed contact from up to six readers and supplies an output at pin A29. The six inhibit inputs from the sequence control logic determine which feed contact input will control the output. Only one is permitted to do so at any one time.

3.165 If any one of the six readers is receiving step pulses these step pulses will be gated and inverted at NOR 1F, ZB522. A step pulse will be developed by PA-F, ZB510 and applied as a step pulse to the four stage counter. The state of the four flip-flops is sampled by LA-1D, ZB324. If the counter is reset and then allowed to receive 15 step pulses, LA-1D, ZB324 will supply a 0 volt output at pin B34. This 0 volt level will be inverted by LA-1F, ZB324 and pubes, LA-ID, ZB324 will supply a 0 volt output at pin B34. This 0 volt level will be inverted by LA-1F, ZB324 and PA-2C, ZB514 and be supplied as a 0 volt feed **alarm** indication to the reader logic.

3.166 Normally pin A29 of ZB120-A is at -5 volts (feed contact closed). When the reader steps, the paper tape will move forcing the feed contact to open until the next feed hole is sensed by the contact. and will close again. The contact remains closed until the reader is stepped again and the contact will be forced open as before.

3.167 As a result of stepping the reader, a transition is obtained at pin A29 of ZB120-A. This positive transition is inverted by LA-21, ZB110 and applied to PA-1, ZB514. The positive pulse output of **PA-F** is applied as a reset pulse to the four stage counter.

3.168 The alarm indication is inhibited if the feed indication has been received prior to **15** step pulses, Had a feed indication not been received, the counter would not have been reset and an alarm indication would have been generated.

Signal Gating

3.169 The logic appearing on Sheet 12 (7744WD) performs the function of presenting to the Parallel to serial converter one of the three following signals:

(a) The output from the reader via the verifier register.

(b) The output of the start of message generator (SOM).

(c) The no character available signal (all levels marking).

3.170 In the no character available condition, -5 volts is applied to pin A8 of PA-X, ZB317. The output pin B4 is driven to 0 volt which is applied to eight second-level gates, driving the outputs to -5 volts. These -5 volt outputs arc inverted by eight inverters and supplied to the parallel to serial converter as 0 volt mark signals.

3.171 When the SDM generator is operating. the send number indication from the SOM generator is 0 volt. This is applied to all eight first level gates driving the outputs to -5 volts. This inhibits the reader information which is king sampled at the verifier storage.

3.172 The -5 volt outputs from the first level gates to applied to the inputs of the second level each second act **as** primes **at each** gate. A second input to each second level gate is a character available indication which is -5 volts at this time.

3.173 The two inputs of each second level NOR gate **servicing code levels 1, a** and 8 have all been supplied with -5 volts resulting in **a** 0 volt output from each gate. This is inverted and supplied as **a** -5 volt space indication to the parallel to serial comer. Since the start of message generator sequence is 5-level code only, the space indications on these remaining three levels are required to inhibit perforating these levels at the receiving set.

3.174 The output from the start of message generator is supplied to each of the five, three input second level gates, associated with code levels 2, 3, 4, 5, and 6. The 0 volt designates a mark and -5 volts designates a space. with the other two inputs primed as explained in the previous paragraph, the mark-space indication is inverted at the output of the NOR gates and again at the inverters resulting in 0 volt for a mark and -5 volts for a space. This information is supplied to the parallel to serial converter.

3.175 In the case where the reader is supplying information to the parallel to serial converter, this information is supplied at one of the inputs to each of the first level gates (0 volt is a space, -5 volts is a mark). The second input to the gates is supplied by the send number signal from the SOM generator which is -5 volts at this time. The data input is therefore inverted by the first level gates, and applied to the input of each of the second level gates.

3.176 A second input to each second level gate is the character available signal which is -5 volts at this time, as in the SOM generator output. At the output of the second level gates the reader information is 0 volt for space and -5 volts for mark. This is inverted by the inverters and applied to the parallel to serial converter as a 0 volt for mark and a -5 volts for space.

E. Start of Message Generator (SOM)

3.177 The start of message generator, referred to as the SOM generator, is explained in 2.28. The 14 character sequence is capable of being distributed at 2400 WPM, utilizing the five level Baudot code. The number display assembly (master control panel), gives a visual indication of the next number to be generated.

3.178 The SOM generator uses a four stage counter made up of flip-flops D-B, DC, D-E. and D-F, ZB307 (7744WD), Sheet 22). A detect network consisting of NOR gates LA-1 A. LA-1B, LA-1C, LA-1D, LA-1E, LA-1F, of ZB311, LA-1A, LA-1B. LA-1C, LA-1D, LA-1E, LA-1F, of ZB309 and LA-1A, LA-1D of ZB305 and LA-18 of ZB522,

which detects the count in the counter as the counter s
The outputs of the above named gates are numbered
through fourteen corresponding to the count which each
detects. The num

3.179 '44WD, Sheet gate LA-1D, ZB305 **detects the reset**
79 **The N**of the counter. The collectors of the
condition of the counter. The collectors of
flip-flops in the counter, feed NOR gates. which in turn
is **to** reduce the loading on each flip-flop in the counter.

3.180 When the counter leaves the reset condition there is at least one input of NOR gate LA-1D, ZB305 that is at 0 volt (7744WD, Sheet 23). For the duration of the SOM sequence the output of this gate is a -6 volts, this negative level is fed **to** PA-1D and PA-2D, ZB313 (7744WD, Sheet 22). Power amplifier PA-2D energizes relay KB501-C which energizes the stepping magnets located in the number display.

3.181 Relay KB501-C stays energized for the entire SOM sequence. When the counter resets, PA-2D de-energizes KB501-C and the stepping magnets. The number display steps one character. Therefore at reset, the number display steps and indicates the next message number to be sent.

3.182 The -6 volt level at pin B3 of PA-ID, ZB313 during the SOM sequence is inverted by this power amplifier, and fed to LA-1B of ZB324 (7744WD, Sheet 19) where it inhibits the verifier alarm during the SOM sequence. The output of PA-ID on ZB313 is also fed to the verifier, (7744WD, Sheet 12). During the SOM sequence, this output also inhibits the gates that sample the output of the reader.

3.183 The output of PA-1C, ZB313 (7744WD, Sheet 22), feeds three points:

(1) NOR gate LA-2F, ZB302 (7744WD. Sheet 25).

(2) Set input of DY-B, ZB512.

(3) Power amplifier PA-2C, ZB313.

During the SOM sequence. the -6 volt level appearing at the input of NOR gate LA-2F. ZB302 (7744WD, Sheet 25) is inverted and fed to the parallel to serial converter (Sheet 10) where it inhibits the UPCI switch (module A) for the duration of the SOM sequence.

3.184 The output of NOR gate LA-2F also feeds PA-ID, ZB315. During the SOM sequence, the -6 volt level at the output of this power amplifier primes the output gates of the SOM generator. At the end of the SOM sequence, the output of NOR gate LA-2F, drops to -6 volts, which enables the UPCI switch to perform its function. The output of PA-ID then inhibits the output gates of the SOM generator.

3.185 Upon reset of the SOM counter, a **positive transition appears** at **tbe output of PA-1C, ZA313, (7744WD, Sheet 22). This triggers DY-B, ZB512 since its** prime is permanently at 0 volt. The normal output is **fed to** NOR **gate LA-lC, ZB305 where it acts as an inhibiting factor for the SOM pulses which originate in the sequence control. When triggered, the delay times out** for 225 **milliseconds, inhibiting** NOR gate LA-1C.

3.186 **The purpose of applying 0 volt at pin A24, of** this **gate during this-period, is to prevent the counter from being re[illegible]. The delay is required due to the stepping mechanism which drives the number display. Since it takes a positive transition to trigger the delay, the delay will only be triggered when the counter reaches reset.**

3.187 The output of NOR gate LA-1C, ZB305 is **fed** through diode CR-C of ZB108 to the direct base input of NOR gate LA-1D, ZB305 (7744WD, Sheet 23). The positive SOM step pulses at this point prevent possible unwanted switching transients to appear at the output of NOR gate LA-ID, ZB305.

3.188 Upon receipt of the first SOM step pulse the counter steps off reset. The first gate in the detect network, LA-1A, ZB311 (7744WD, Sheet 23) detects the first count (all of its inputs are negative) and drives its output to 0 volt. During the first character interval, the other NOR gates in the detect network all have at least one 0 volt input, therefore the outputs of these gates are negative at this time.

3.189 For the first character it has been shown that the output of NOR gate LA-1A, ZB311 is 0 volt. This output is fed to NOR gates LA-IA, LA-1B, LA-1C, and LA-1D, ZB302 (7744WD, Sheet 25), where it is inverted and applied to the already primed gates LA-2E, LA-2B, LA-2C, and LA-2D, ZB302 producing a 0 volt level at the output of these gates, levels six, five, four and three respectively.

3.190 Since the input of gate LA-1E, ZB302 is at -6 volts during the first character, the output of this gate is at 0 volt. This level is inverted by output gate LA-2A, ZB302 producing -6 volts at the output of this gate. For the first character, level two is spacing while levels three, four, five and six arc marking, representing the letter V.

3.191 The second SOM step pulse steps the counter which drives the outputs of LA-IA, ZB311 to -6 volts and LA-1B, ZB311 to 0 volt (7744WD, Sheet 23), indicating a count of two in the counter. The 0 volt level at the output of LA-1B, ZB311 is fed to LA-1E, and LA-1A, ZB302 (7744WD, Sheet 25). Therefore the second character levels, three, four and five are spacing while levels two, and six are marking, generating the letter Z for the second character in the SOM (refer to 7744WD, Sheets 23 and 25).

3.192 The thid **through** eighth step pukes generate the appropriate characters. The ninth step pulse drives the output of **LA-1C,** ZB309 **to** 0 volt. which is inverted by **LA-1F,** ZB302 (7744WD, Sheet 25) and reinverted by PA-2C, ZB315. The five switches on the front panel of module **B permit** the operator to feed this 0 volt level at the output of PA-2C, ZB315 to OR gates **ZB304-22. 16, 7, 3,** and **10** for levels six, five, four, three and two respectively. This 0 volt level applied to these OR gates supplies a mark signal to these particular levels.

3.193 The tenth SOM generator step puke generates a figures character. During the eleventh step period the output of NOR gate LA-1E, ZB309 is 0 volt which is inverted by NOR gates LA-1E and LA-2E, ZB503 (7744WD, Sheet 24). The -6 volt level appearing at the outputs of the gates mentioned above, primes NOR gates LA-IA. LA-2A, LA-1B, LA-2B, and LA-1C, of ZB503. The outputs of these gates are therefore dependent upon their other inputs on pins A6, B4, B15, B12, and B25.

3.194 The inputs for the above named gates are supplied by the Baudot coded switch assembly located in the number display assembly. The outputs of these gates are fed to their number identifying inputs of OR gates ZB304-22, 11, 17, 20, and 21, and NOR gates LA-IA, LA-1B, LA-1C, LA-ID. and LA-1E of ZB302. Therefore, a -6 volt level at an input of NOR gates LA-IA, LA-2A, LA-1B, LA-2B, and LA-1C of ZB503 generates a mark in their respective level.

3.195 The next two numerical characters are generated by the same means, utilizing different levels of the Baudot coded switch. The fourteenth SOM step pulse generates a letters character during that interval. At this time the output of **PA-2C, ZB313 (7744WD.** Sheet 22) goes to -6 volts. The output of this power amplifier is fed to the reader logic (7744WD, Sheet 3). This -6 volt step is inverted and sets flip-flop DC of ZA112. The output of this flip-flop is fed to step clock gating (module B 7744WD, Sheet 15) where it prevents subsequent SOM step pulses from reaching the SOM counter and now permits the next reader step pulse to be fed to the reader logic on Sheet 4.

3.196 The fifteenth SOM step pulse causes the output of **NOR** gate **LA-lB, ZB522** to go to -6 volts. This negative transition is fed to PA-E, ZB313 (7744WD, Sheet 22) causing a positive pulse at its output. This pulse is coupled through diodes to the normal outputs of the flip-flops in the SOM counter, driving them to 0 volt, or the reset condition.

Master Transmitter Po

3.197 Alternating current (ac) **is connected at** TBG102(7744WD, Sheet7),and 0.47 microfarad bypass capacitors (for shielding purposes). The ac line is protected by circuit breaker **CRG101 (15** ampere). From this circuit breaker **(C6C101) power is** distributed to various components and assemblies throughout the **cabinet.** Power receptacle JA1 is provided and protected by its own 5 ampere circuit breaker. The POWER indicator switch controls power to all equipment in the cabinet by operating a silicon bidirectional switch SWG102. This switch provides power to the reader driver assembly (protected by its own 1-1/2 ampere circuit breaker). the power supply (protected by a 3 ampere circuit breaker). and to silicon bidirectional switch SWG 101.

3.198 The SWG101 switch is controlled by relay K1 and controls power to the reader and winder motors. Relay K1 is controlled by the MOTORS indicator switch, which controls the indicator lamp. Power amplifier PA-ID, ZA108 ca. turn on the motors even if the MOTORS switch is off by energizing K1 through CR-B. ZA110. This power amplifier also operates relay K2 which energizes the **BID** lamp and, through a diode. the MOTORS lamp. The diodes prevent a bid from being indicated when the MOTORS switch is turned on. The power amplifier input is shown on 7744WD, Sheet 2.

Supplementary Transmitter Power Distribution

3.199 The ac portions of this circuit (7744WD. Sheet 6) are exactly the same as those described in 3.197 and 3.198 except for a 10 ampere ac circuit breaker instead of 15 ampere, component designations and the addition of relay KF101. This relay operates when power is applied to the silicon bidirectional switch controlling the motors through the 4 ampere circuit breaker CBF102. When KF101 operates it connects the supplementary station equipment to the -12 volt, -6 volt, and +6 volt power supply leads. Each of these voltages is individually protected by a circuit breaker. PA-1D, ZE108 drives bid relay K2 as shown on Sheet 2.

Power Supply

3.200 The power supply (7744WD. Sheet 6) produces outputs of 28 volts. 48 volts, -12 volts. -6 volts, and +6 volts. Each of these outputs is associated with a separate winding on transformer VR1, and each output circuit has its own full-wave rectifier. filter capacitor. and bleeder resistor. VR1 is a ferroresonent transformer which compensates for power line voltage variations. The -6 volt and +6 volt outputs are electronically regulated. In the -6 volt regulator, transistors Q5 and Q6 are in parallel and connected

3.201 Transistor Q2 receives base current through R6 from the -12 volt supply. Some of this base current is diverted to ground through Q1 and CR11. Resistor R7 provides a drain for the leakage currents of Q5 and Q6. The CR11 maintains a constant voltage of -4.7 at the emitter of Q1 regardless of the current through Q1. Base current to Q1 is supplied from the output terminal through the voltage divider composed of R11, R10, and R9. If the output of the supply should go more negative the base of Q1 would go

3.202 The negative change would increase the base current of Q1, therefore increasing the collector current. This would make less current available for the base of Q2, causing a reduced current into the bases of Q5 and Q6 reducing the load voltage, correcting for the change. Similarly, if the load voltage should go less negative the base current of Q1 would be reduced, making more base current available for Q2. This would allow more current to flow through Q5 and Q6 returning the output voltage to its correct value. The +6 volt regulator operation is exactly the same as that of the -6 volt regulator except that only one series pass transistor is used.

MASTER AND SUPPLEMENTARY HIGH SPEED TAPE SENDER WITH RADIO PREQUENCY INTERFERENCE (RFI) SUPPRESSION FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

INSTALLATION AND CHECKOUT

CONTENTS PAGE

1. GENERAL

1.01 This section contains information necessary to install radio frequency interference **(RFI)** suppression equipment on standard master and supplementary high speed tape senders. It is used with **reference** to the standard (MAPS) literature as additional information relating to certain modules and components. The operating functions of the master and supplementary tape senders arc **unchanged.**

1.02 **Wiring diagram** sections contain pertinent actual and schematic wiring diagrams for rfi circuitry. Reference should be made to the appropriate wiring diagram for specific wiring information.

1.03 **All references to right or left, front or rear,** up or down, are made from a normal **operating** position in front of the cabinet. Clearances for service **and maintenance are necessary in front, rear, and** top **of cabinet. Tape** reader, tape handling, tape supply, electronic logic, and power supplies are accessible from the front of the cabinets.

2. UNPACKING

2.01 All equipment is packed for maximum protection during shipment. caution must be taken when unpacking the rfi modification parts cartons (one carton for master and supplementary cabinets and one carton for receiver cabinet) **to** prevent damage to the components. Observe all caution labels as well as any special instructions on the cartons. Small bags and loose parts should be kept with their associated components until used in the installation.

3. INSTALLATION

HIGH SPEED TAPE READER

3.01 Refer to Section 592-851-730TC before removing the DX reader from the cabinet. Disconnect the SO-pin connector from the receptacle at the rear of the tape reader, and remove the 50-pin receptacle from its mounting bracket. Remove the green ground lead from the mounting plate. Gut each TP328793 capacitor lead 1/2 inch in length.

3.02 Remove receptacle pins **10, 25, 27,** and 43, and remove plastic tubing. Solder the leads from two TP328793 capacitors to the rear portion of the pins (see CAUTION). Replace tubing over the pins and capacitor leads. Replace pins in the receptacle so one capacitor is across pins 10 and 25, and the other capacitor is across pins 27 and 43. Reinstall the receptacle in its mounting bracket, the green ground lead to the mounting plate, and reconnect the 50-pin connector.

CAUTION: DO NOT ALLOW SOLDER TO RUN DOWN ON FRONT PART OF PIN.

Note: Refer to appropriate parts literature for identification of components.

3.03 Install the TP333324 contact shorting assembly between the verify and code reading contact mounting screw heads and the reader top plate above the screw heads (Figure 1). **Remove** the nut and washers from the right hand lid latch mounting stud. Place the TP333335 position bar on the stud and over the contact shorting assembly . replace the nut and lockwasher only , Hold the position bar down firmiy on the contact shorting **assembly** while tightening the nut.

3.04 of the TP326778 ground strap under the mountin

3.05 inal end of the ground strap, a TP34432 flatwasher, and a TP112626 nut. tighten securely. Replace front cover and readjust reader position per Section 592 851 730TC.

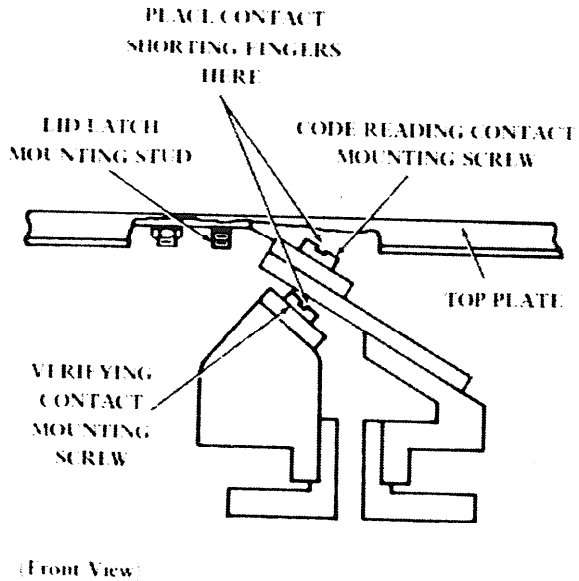


Figure 1. Tape Reading Contact Mounts

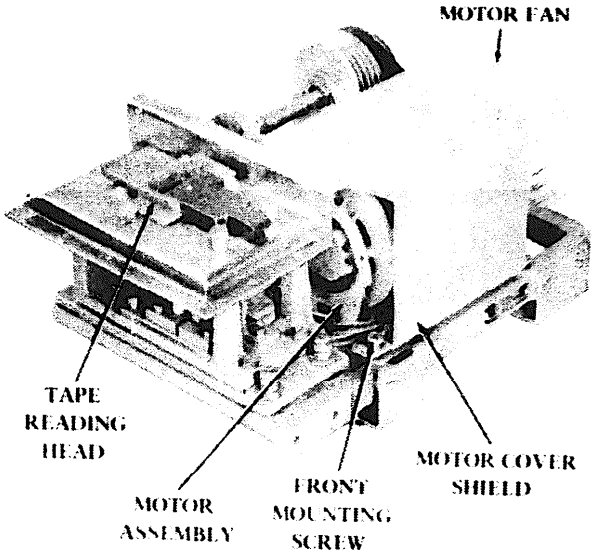


Figure 2. High Speed Tape Reader

TAPE TRANSPORT PANEL

TAPE TRANSPORT PANEL

in Figure 3 to layout and drill

3.06 holes for the panel latches. Install the two 333349 latches using washers and nuts accompanying the latches. Use two flat washers on the right latch only to compensate for single thickness stock. Place lockwashers between front face of latches and back of front panel. Latches should be positioned on panel to engage cabinet flange when latch pawl is turned clockwise.

Note: When securing front panel to cabinet, tighten adjustable pawl fasteners sufficiently to assure good metal to metal grounding connection.

REAR CABINET PANEL

REAR CABINET PANEL

3.07 Remove the captive screw from the rear cabinet panel, place a TP151572 lockwasher under the head of the screw and replace screw in panel.

CONDUIT PLATE

CONDUIT PLATE

3.08 Before installing the TP333314 conduit plate,

3.08 determine the number of 3/4 inch conduits to be used for signal and clock cables. Remove the number of knockouts necessary. If cables have connectors attached, insert the cables through the appropriate openings before installing the plate.

3.09 Position the plate on the underside of the cable opening in the lower rear section of the cabinet. Place flanged side of plate on top of the front flange of cable

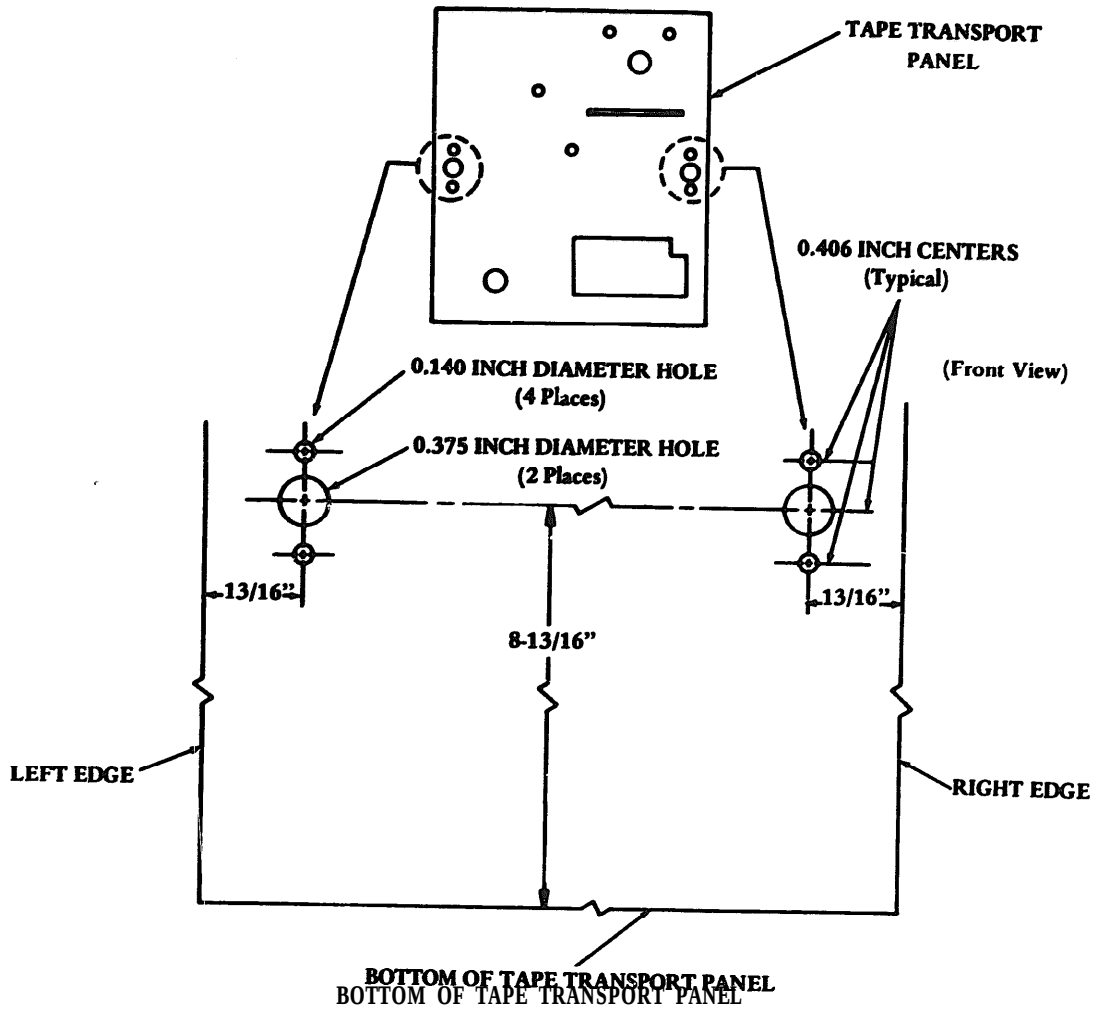


Figure 3 - Dimensions for Panel Latches

opening, raise rear of conduit plate up to bottom side of cable opening. Place bracket support TP333317 on inside of cable opening above conduit plate. Connect plate and bracket together by inserting seven TP151723 screws with lock-washers through mounting holes in the bracket support, tighten screws (Figures 4,5, and 6).

3.10 Insert. the 1/2 inch end of a 3/4 inch connector enlarger through the 1/2 inch conduit plate hole with the 3/4 inch end extending from under the plate. Screw on a locknut over the 1/2 inch end of the connector enlarger inside the cabinet, and tighten (Figure 6). Screw on a connector extension over the remaining threads of the connector enlarger and tighten. Screw on a locknut approximately 3/8 inches down on the connector extension.

3.11 Place 1/2 inch opening of junction box over 1/2 inch connector extension and rest box on locknut. Screw on another locknut inside the junction box to the connector extension. Position junction box so electrical connections can be made from rear of cabinet, tighten locknut.

CABINET CONNECTIONS

A. Electrical

3.12 To maintain rfi capabilities all electrical inputs and outputs to the cabinet should be routed through solid steel conduit (EMT). Connect terminal ends of TP333337 junction box power cable to terminal block TBF101 or TBG101 as shown in the following chart:

CHART 1

TBF 101 OR TBG 101	TP333337 CABLE WIRE
1	GREEN
3	WHITE
4	BLACK

B. AC connections

3.13 Use locknut on conduit connector to secure it to the connector enlarger. Feed wires into junction box and connect conduit to connector. Make necessary connections in junction box and **attach cover** with hardware provided.

C. Signal and Clock Connections

3.14 After the signal **and** clock cables are installed through the conduit plate, make connections as shown in wiring diagrams 7710WD and 7716WD.

4. CHECKOUT PROCEDURE

GENERAL

4.01 Checkout procedures should be made after installation is completed. These checkout tests should also be performed after routine servicing or correcting **extensive** troubles in the set. A physical inspection should precede all rfi tests to insure that all ground straps and shields are properly installed and all connections properly tightened.

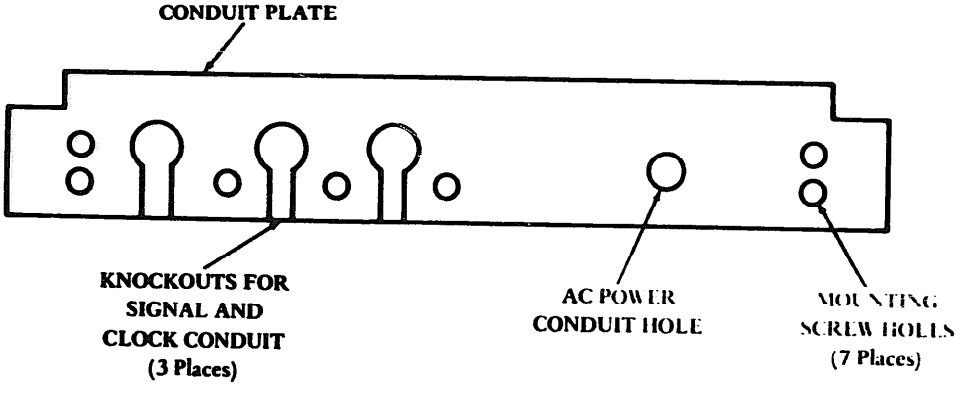


Figure 4 - Conduit Plate

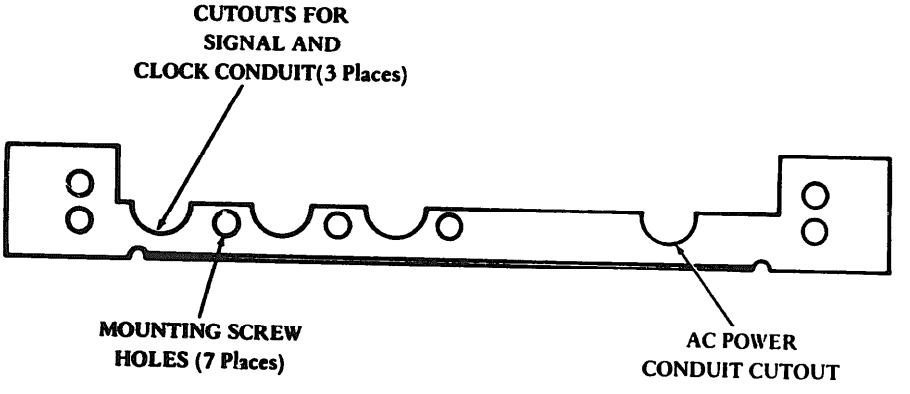


Figure 5 - Bracket Support

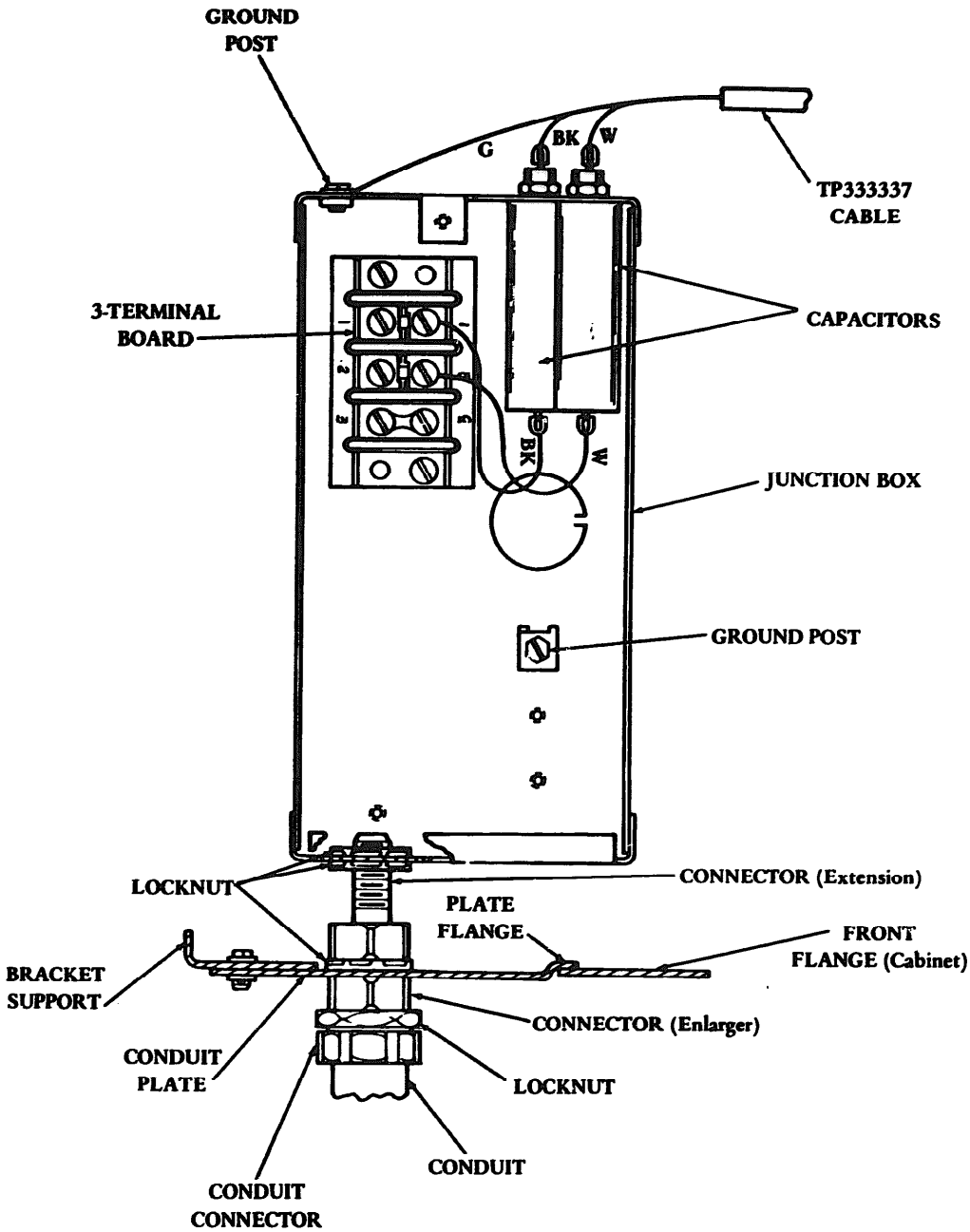


Figure 6 - Conduit Connection and Junction Box

Text The standard checkout procedure chart in Section 592-851-230TC should be used with this procedure to completely checkout each cabinet. When using the standard checkout chart with rfi equipped cabinets, the eighth SOM character received by the equipment will become the ninth SOM character received.

4.03 Checkout procedure for bid retention and external stop-send features is arranged in the following chart form. Each step is designed to be followed in sequence.

4.04 Sets with rfi components installed should be tested by setting up a functional system consisting of a receiver, and master or supplementary transmitter in an rfi shielded room. Primary power and interconnecting signal leads are to be enclosed in separate 3/4 inch electrical metal tubing conduit. A radio frequency (rf) quiet clock should be used for timing and must be in a shielded enclosure.

4.05 All mechanical adjustments and electrical continuity tests should be completed before rfi testing. To insure good shield connections, shield continuity tests should be made. The screen room should be free of all loose metallic parts, tools, wires, and nonessential test equipment.

4.06 Spectrum signature recording tests should be identified with the serial numbers of the units tested. Make notations for malfunctions encountered or abnormalities in rf measurements. Disconnect both sides of the screen room lighting circuits before making rfi tests.

RFI TEST

4.07 Make preliminary tests to assure proper operation of the system. Disconnect tape feed motors before making rfi tests to prevent triac noise. Test limits apply to data related signals only.

C H A R T 2

CHECKOUT PROCEDURE CHART FOR MASTER AND SUPPLEMENTARY RFI SENDER CABINETS

STEP	ACTION	VERIFICATION
1	Bid Retention	
	(a) Reader in on-line mode and reading tape. Operate STOP switch. Open tape lid and remove tape.	ON-LINE indicator remains lit.
	(b) Replace tape in reader and close tape lid. Release STOP switch.	Transmission is resumed.
2	External Stop-Send, Master Sender	
	(a) With the reader reading tape, apply +6 volts to input lead JG106-24 (normally -6 volts).	The reader stops on the character after the one being read when the +6 volts is applied.
	(b) Reapply the normal -6 volts to input lead JG106-24.	The reader resumes transmission in correct character frame.

4.08 Place the cabinets in a row facing the antenna approximately one foot apart. Center the antenna three feet in front of the cabinet group. When making tests with a vertical rod antenna setup, mount the cabinets and antenna on a common ground plane (aluminum foil or copper sheet one foot wide and appropriate length), connected to the shielded room walls (Figure 7). Electrical field limits are shown in Figure 8.

RADIATED TEST

4.09 Electric field radiated measurements can be made over the frequency range of 1000 hertz to 1.0 giga hertz. The dipole or vertical rod antennas should be placed three feet from the mechanism under test. Amplitude limits for data related signals are shown in Figure 9. Antenna test setups are shown in Figures 10 and 11.

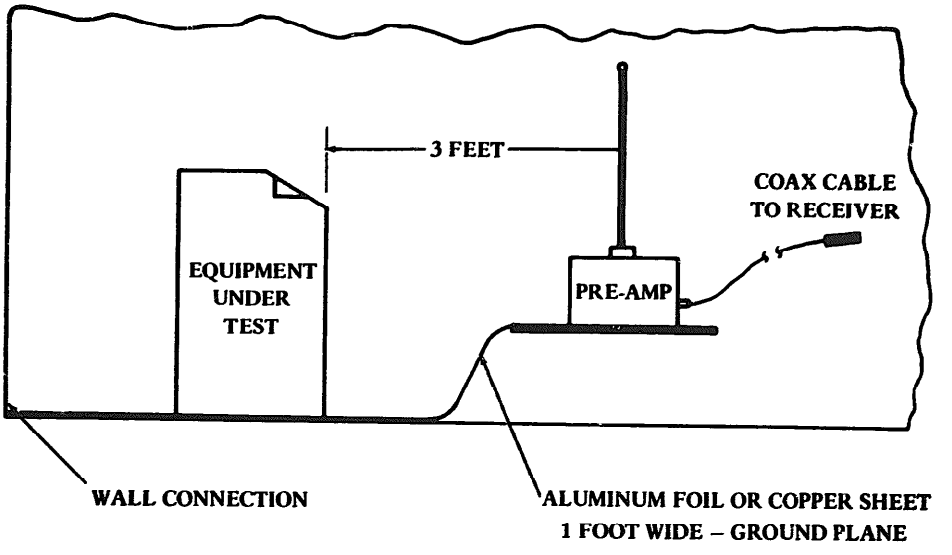


Figure 7 - Vertical Rod Antenna Test Setup

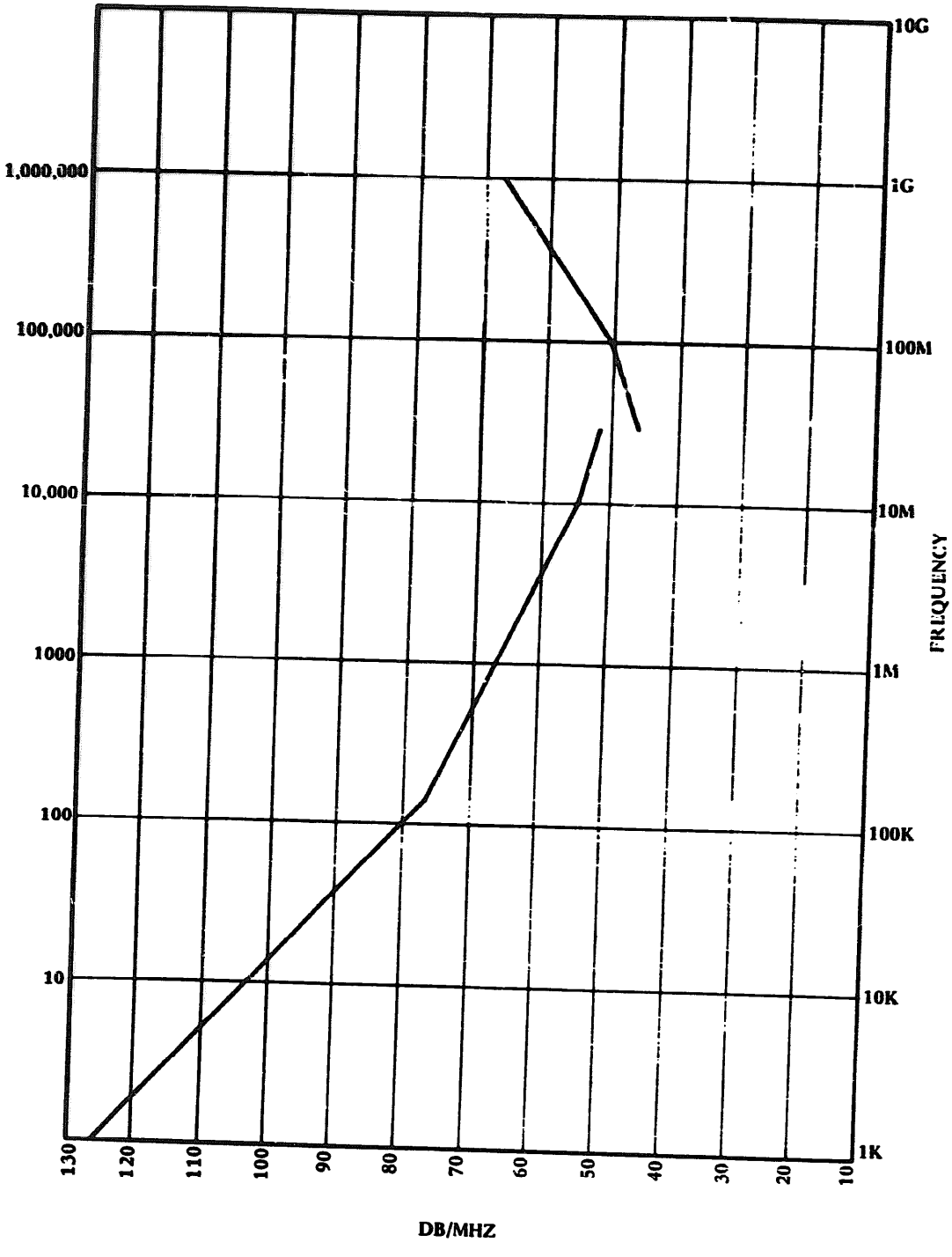


Figure 8 - Electrical Field Limits

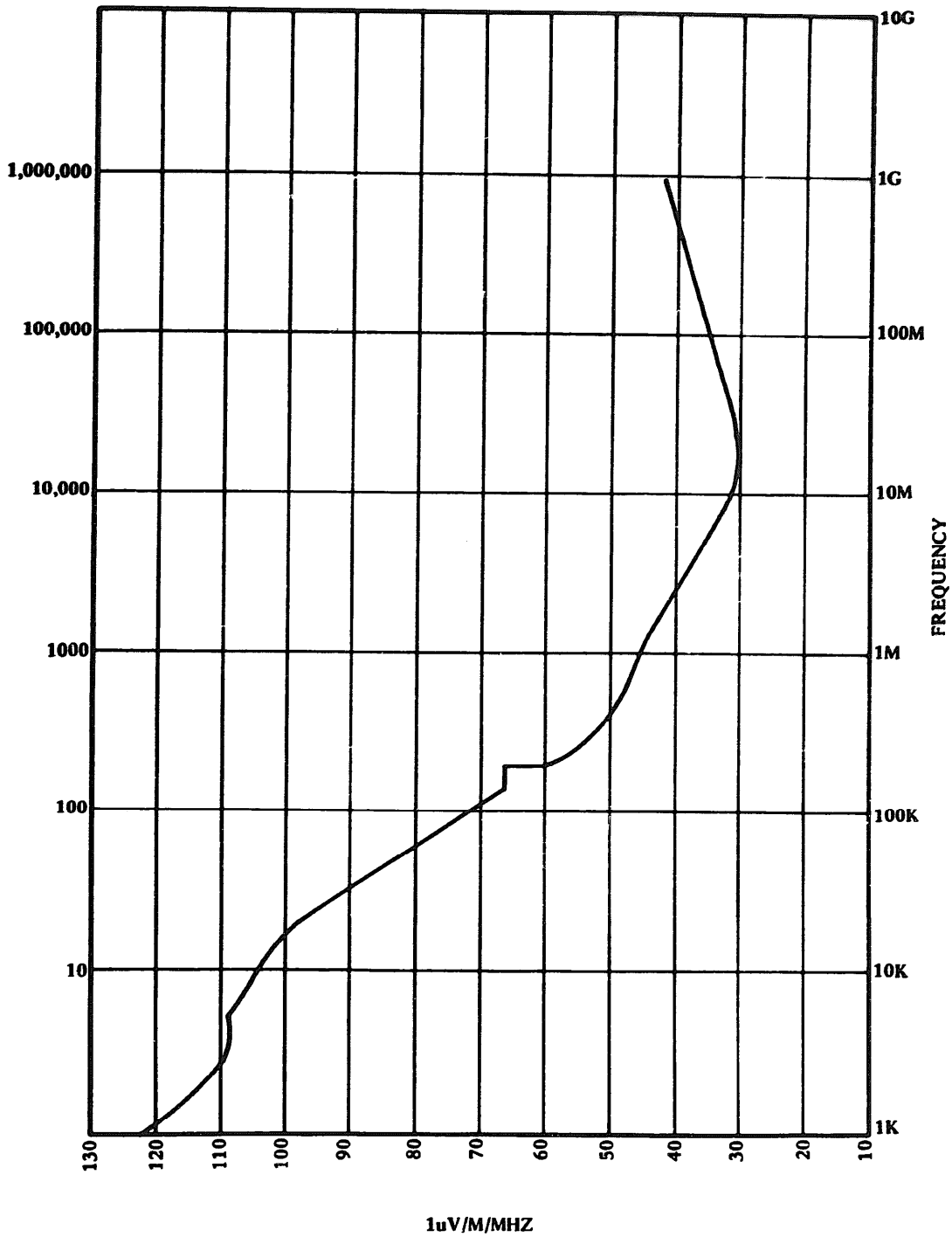


Figure 9- Electrical Field Radiated Limits

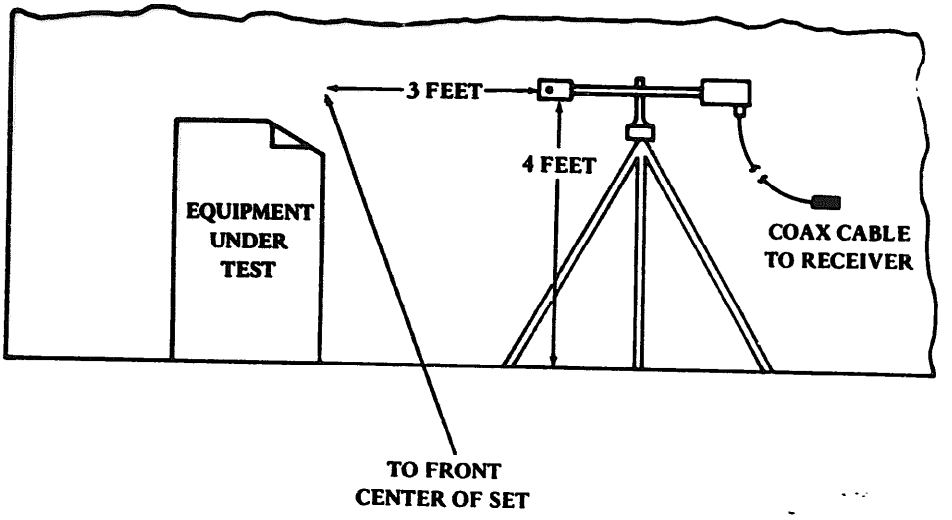


Figure 10 - Horizontal Dipole Antenna Test Setup

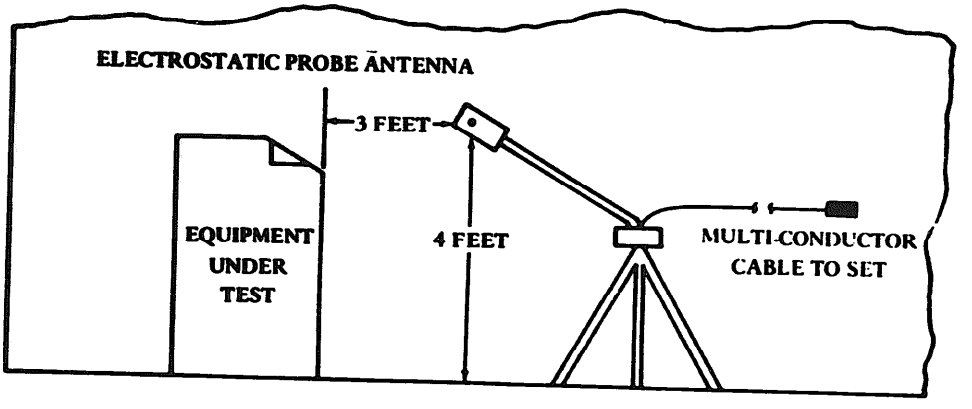


Figure 11 - Electrostatic Probe Antenna Test Setup

HIGH SPEED TAPE RECEIVER WITH RADIO FREQUENCY INTERFERENCE (RFI) SUPPRESSION FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

DESCRIPTION AND THEORY OF OPERATION

CONTENTS PAGE

1. GENERAL

1.01 This section provides a general description and theory of operation of radio frequency interference (RFI) suppression on the high speed tape receiver. It is used with reference to the standard (MAPS) literature for additional information relating to certain modules and components. Circuitry in this section reflects the new features added to the later models of the master and supplementary senders and rfi suppression. Functional operation of the high speed tape receiver is unchanged.

1.02 The basic purpose of rfi suppression as applied to teletypewriter equipment is to provide shielding to suppress electrical field radiation from 1 kilo hertz to 1 giga hertz. Signal, clock, and electrical power inputs and outputs are the same as described in the standard MAPS sections.

2. DESCRIPTION

2.01 The new parts added to the tape receiver consist of a conduit plate, junction box assembly, screens and frames, capacitors, ground strap, and wiring.

2.02 The conduit plate has three 3/4 inch knockouts for clock and signal cables, and a 3/4 inch opening for ac input conduit connectors. The junction box consists of a six terminal board for ac input connections, six 0.47 microfarad bypass capacitors, and wires to connect to the existing input terminal board.

2.03 Wire screens, and metal frames are attached in back of the plastic windows, providing shielding protection while maintaining visibility of the DRPE punches and tape feeding mechanisms (Figure 1). A ground strap provides a direct ground connection between the conduit plate and cabinet frame.

2.04 Each magnet driver card (Module C) is protected by an 0.02 microfarad capacitor connected across the output to suppress noise in the driver circuits.

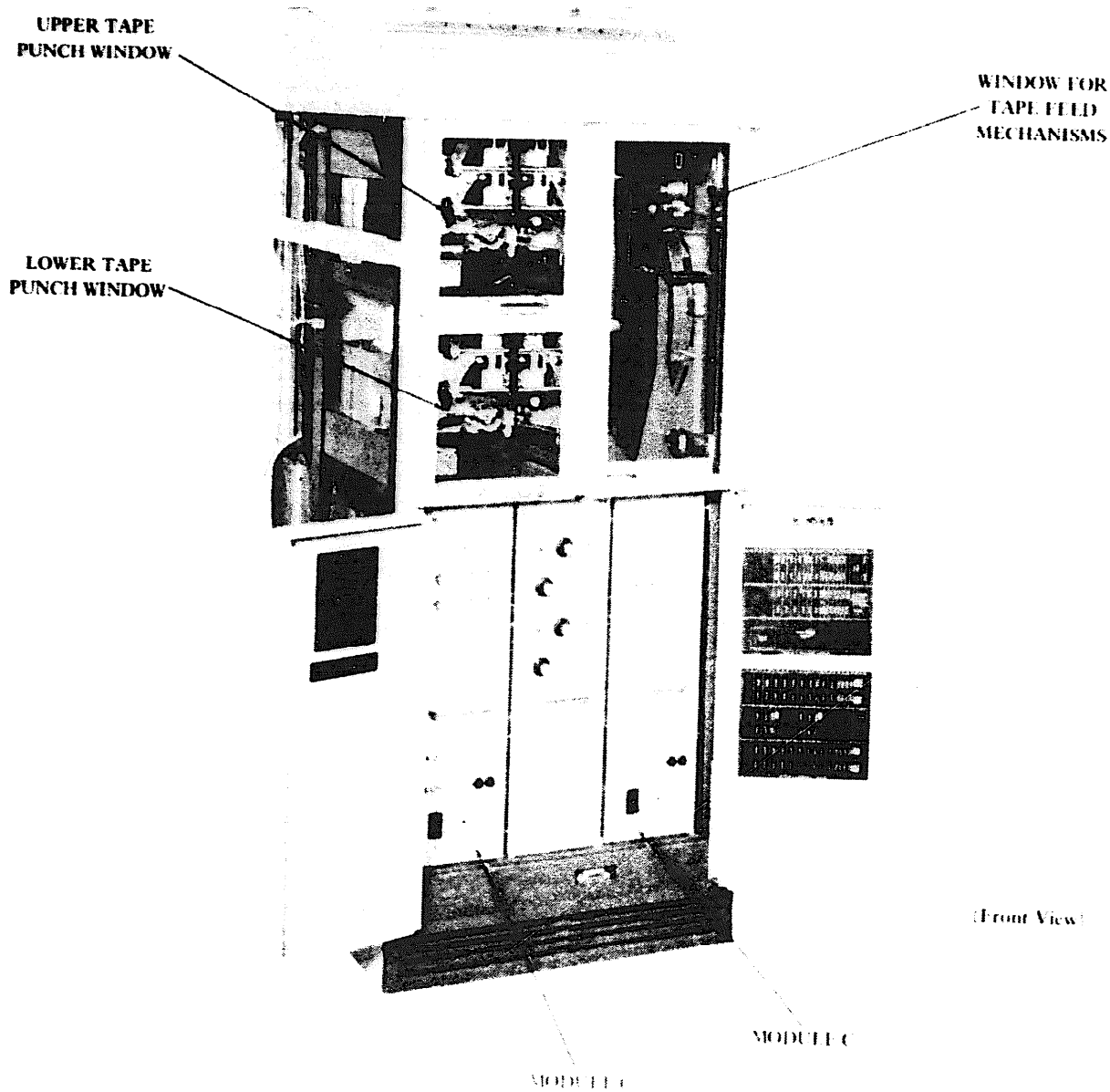


Figure 1 High Speed Tape Receiver

3. THEORY OF OPERATION

GENERAL

3.01 A detailed description of each circuit card is included in the drawing covering the card. The number of the drawing is the same as the part number of the card. The card part number and drawing number is obtained from the EC number of the card by deleting the prefix EC and adding a prefix of 172 for EC300 through EC499, 177 for EC500 through EC599, and 303 for EC600 through EC699. For example, the drawing number for EC359 is 172359, the drawing number for EC690 is 303690. Terminal board cards have the prefix TB, part numbers and drawing numbers for these cards are obtained by deleting TB and adding the prefix 149. For example, the drawing number for TB172 is 149172.

3.02 The equipment voltage levels are of three types:

(a) +6 volts, -6 volts on input and output leads

(b) 0 volt, -6 volts internally

(c) 0 volt, -5 volts on some internal leads, these leads are identified by a shaded corner in the logic symbol from which they originate.

The dc coupled inputs to logic elements are shown as half arrow heads. Full arrow heads are reserved for ac coupled (pulse) inputs.

3.03 The most commonly used logic element is the NOR element, identified by the designation LA within the logic symbol. The output of this element is negative if any input is at 0 volt. The output is 0 volt only if all inputs are negative. A special input to a NOR element, identified by an arrow entering a corner of the symbol, allows the addition of extra logical inputs to the element. The same results can be obtained by connecting two or more elements together to obtain more inputs plus greater load-driving capability.

3.04 The flip-flop element is symbolized by a rectangular box with a diagonal line across the lower half. The operation of this element is similar to that of a standard flip-flop, for example EC671, which contains priming inputs (half arrows) and setting inputs (full arrows). Arrows entering the upper half of the symbol designate prime 1 inputs, and arrows entering the lower half of the symbol designate prime 0 and set 0 signals.

3.05 An arrow entering the center of the symbol implies that the set 1 and set 0 inputs are connected together. If no priming inputs are shown this indicates that the prime 1 input is connected to the inverted output (lower half of symbol). This also indicates the prime 0 input is connected to the normal output (upper half of symbol). A flip-flop connected this way is called a complementing flip-flop or binary counter. Each input pulse reverses the condition of voltages on the normal and inverted outputs.

3.06 A pulse amplifier logic element is identified by a square box with the letters PA and a full arrow head input symbol. This element produces a pulse of approximately 2 microseconds duration whenever the input goes negative. When both inputs to this element are used, a pulse is produced only when both inputs are negative.

3.07 A power amplifier element is shown as a trapezoid symbol with the letters PA. This element has two inputs and can perform the NOR function. It has about three times the load-driving capability of an ordinary NOR (LA) element.

3.08 The delay element is symbolized by a square box with the letters DY. This element can be used as either a one-shot or a free-running multivibrator. Those used as one-shot delay elements have the pulse duration indicated. Those used as free-running multivibrators have the operating frequency indicated.

3.09 The input element translates the input polar signals (+6 volts and -6 volts) to the neutral (0 and -6 volt) signals used internally. The output element translates neutral signals to polar signals. The punch driver elements are described in Section 592-803-100TC.

3.10 The receiver is designed to accept both serial and parallel input signals. Serial signals may be synchronous or start-stop, and may represent 5-, 6-, 7-, or 8-level codes. They may contain from 5 to 16 units (bit times) per character interval. The signals may be received with one or more of the information bits inverted or interchanged in time sequence.

3.11 The CODE LEVEL and UNITS PER CHARACTER INTERVAL switches allow selection of the number of code levels to be used and the number of units per character. A strapping card controls the selection of bit inversion and bit sequence. When more than 9 units are received per character, the units over nine are ignored by the receiver.

3.12 The interconnecting cable between the receiver and its external signal source contains the following leads:

(a) Auxiliary data input (8 leads-parallel)

(b) Auxiliary sample input (parallel)

(c) Data input (serial)

(d) Clock input (serial)

(e) Urgent traffic input

(f) Bit output (8 leads-parallel)

(g) Character available output

(h) Circuit ground, +6 volts and -6 volts

(i) Frame ground

(j) Alarm output (3 leads)

CIRCUIT DESCRIPTION

3.13 A block diagram of the receiver is shown in Figure 2. The counter recognizes character boundaries in incoming serial data by counting the number of units in a character interval. The counter control permits selection of the number of units per character interval and provides for synchronizing the counter with the data. The serial-to-parallel converter stores incoming data bits until a complete character has been received. It includes storage for one character in addition to the character currently being received.

3.14 The punch drive circuits select the data to be punched and control the operation of the punch. The tape handling and alarm logic detect trouble, and alarm conditions, such as low tape, end of tape, tight tape, no tape, and full chad bin. The control panel contains the various controls used by the operator, and the indicators advise the operator as to the condition of the equipment. The reperforator, power supply, and circuits which distribute ac power to the various components of the set are not shown in Figure 2.

3.15 All indicator lamps in the equipment are controlled by relay contacts or by switches. The controlling contacts are shunted by 150 ohm resistors. These resistors allow a small amount of voltage across the lamp filaments keeping them warm but not enough to allow the lamp to light visibly. This decreases the initial surge of current, which increases the life of the lamps and the controlling contacts.

3.16 All relay windings are shunted by diodes which prevent voltage spikes from being generated when the relays are de-energized. The operator control switches are momentary in action, except BUSY OUT and POWER which are alternate action, push on, push off.

PUNCH DRIVER

3.17 The punch driver mechanisms and electrical components are described in detail in Section 592-803-100TC. The operation of the punch driver circuits are described in the following paragraphs. Refer to 7746WD, Sheet 4.

3.18 The input stage of a driver element is through a flip-flop. Pin 15 is a priming input and pin 22 is a setting input. Pin 30 corresponds to the inverted output brought out through a diode. The feed level is controlled by ZC324 so that a feed hole is punched whenever a punch command pulse appears on the common input to pin 22 of all driver cards. A level change occurs on the common pin 30 line when a hole is punched in any level, including the feed level. This level change allows the gated oscillator ZC120 to run.

3.19 The first pulse from ZC120 resets all drivers that were set and turns off its own turn-on signal. The circuit remains in this condition until another set pulse arrives. The four inputs to the punch driver primes are, data received serially, data received in parallel, blank feed out character, and feed out characters programmed into the switches on the front of the driver module. As levels 1 through 8 operate identically, only level 1 will be described in detail.

3.20 The output of ZC316, pin A10 will be 0 volt, conditioning ZC323 to punch the 1-level, if all inputs to the NOR gate are negative. Any positive input to the NOR gate may be viewed as inhibiting punching level 1. The blank feed bus connected to ZC316 pin A6 is negative unless blank feeding is in progress. The character feed bus connected to ZC316 pin A5 through switch SWC5 is negative unless character feeding is in progress. Opening switch SWC5 has the same effect as if ZC316 pin A5 were connected permanently to -6 volts. With the SWC5 switch open the character feed bus is unable to inhibit punching.

3.21 The receive parallel bus is at 0 volt only when parallel data is received. The receive serial bus is at 0 volt only when serial data is received. When the receive serial bus is at 0 volt and the other three feed busses are negative, ZC316 pin A26 is held negative. At this time ZC316 pin B10 is allowed to go positive if the level 1 input from the receiving distributor storage at JC328 pin C8 is negative, indicating a spacing bit. Therefore, punching in level 1 is inhibited. If the input from the receiving distributor storage is positive, ZC316 pin B10 is held negative so that level 1 is permitted to punch. When the receive parallel bus is at 0 volt and the other three feed busses are negative ZC316 pin B10 is held negative.

3.22 The output of ZC316 pin A26 goes to 0 volt if the auxiliary bit one input is negative, or to -6 volts if the input is positive. Therefore, punching is controlled by the auxiliary bit input signals. A pulse from ZC120, pin 7 causes a character to be punched, when pin 9 of this element goes positive. When power is first applied, relays K2 and K3 of ZC418 do not operate immediately because the winding of

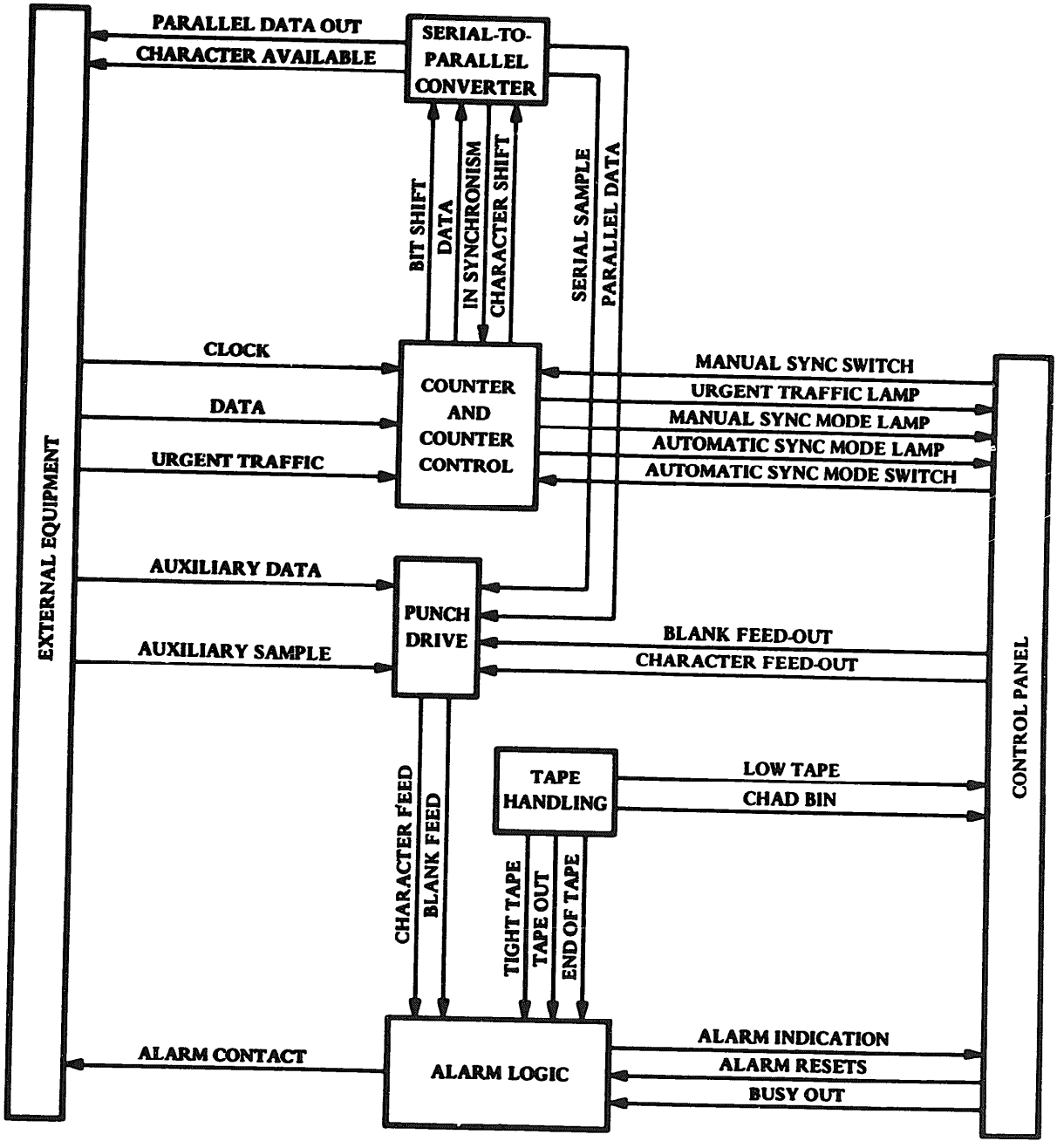


Figure 2 - Block Diagram of Receiver

K2 is connected with an R-C delay network (7746WD, Sheet 3). Relay K3 is then energized through the contact of K2. Before K2 and K3 operates ZC108, pin A12 and ZC112, pin A35 (Sheet 4) are held at 0 volt. Therefore ZC112, pin B27 is negative, pin A9 is at 0 volt, and pin A10 is negative.

3.23 A 0 volt on ZC313 pin A9 holds the blank feed bus negative and 0 volt on ZC313 pin B3 holds the character feed bus negative. With 0 volt on ZC112 pin A14, pin A17 is held negative, holding the receive parallel bus at 0 volt. The 0 volt on ZC112 pin B26 holds pin B28 negative. volt. The 0 volt on ZC1l2 pin B26 holds pin B28 negative, holding the receive serial bus at 0 volt. These conditions hold all punch level inhibit signals off (negative).

3.24 When K2 and K3 are operated ZC108 pin B11 (sheet 3) immediately produces a positive pulse. This acts through diode CR-B of ZC311 to drive ZC120 pin 9 positive, producing a pulse at ZC120 pin 7 punching a delete (rub-out) character. This is done because the punch pins may have partially perforated the tape when power was turned off. This would cause the punch to jam if a delete character were not punched over the partial perforations. Because of the inherent delay in the priming circuits, the delete character will be punched even if the punch prime leads go negative when K2 and K3 operates.

FEEDOUT CIRCUITS

3.25 With no traffic and K2 and K3 operated, ZC12O pin 9 is negative. A circuit consisting of two NOR elements is connected to the BLANK FEED switch (7746WD, Sheet 3). This circuit, sometimes called a latch, is used frequently in connection with switches to eliminate the effects of contact arcing. With the BLANK FEED switch released, a ground at ZC112 pin B23 holds pins A26 and A23 negative. The open at pin A24 allows pin A27 to go to 0 volt, while holding pin A26 negative. If the ground were removed from pin B23, the outputs of the two NOR gates would be unchanged.

3.26 Operating the BLANK FEED switch. grounds pin A24, while holding pin A27 and pin B22 negative. Pin A26 is at 0 volt with pin B23 open. If the ground were removed from pin A24 the state of the circuit would not change. Pin A26 goes to 0 volt as soon as the switch is operated and remains at that voltage, regardless of the contacts arcing, until the switch is released. The latch circuits composed of ZC112, LA-ID and LA-2D are connected to the CHARACTER FEED switch.

3.27 Operating either the CHARACTER FEED switch or the BLANK FEED switch, holds ZC110 pin B34 negative, allowing the multivibrator (MV-A) of ZC313 to run at a frequency of 105 hertz. Square waves from this element appear inverted at ZC307 pin A9, the 1050 wpm lead. At the same time the blank feed or character feed bus goes positive, because of the negative voltages at both inputs of the selected power amplifier element. The blank feed bus or the character feed bus controls priming of the punch drivers as described in 4.18 through 4.24.

3.28 The character feed bus enters ZC112, pin A13 and pin A34 to hold the receive parallel bus and receive serial bus at 8 volt during character feeding. This prevents parallel and serial input data from reaching the punch and interfering with character feeding. Incoming pulses on the 1050 wpm lead enter at ZC112 pin A5 (Sheet 4). Because all other inputs to this element are negative, the 1050 wpm pulses appear inverted at ZC112 pin A10. These pulses drive the punch drive power amplifier of ZC120 and cause the appropriate characters to be punched at a rate of 1050 per second.

3.29 A third character feed circuit is controlled by the CHARACTER FEED toggle switch on the front of the appropriate module C punch driver. This switch is connected to a modified version of the latch circuit described in 4.25. Operating the switch causes ZC112 pin B10 to go negative and pin B9 goes to 0 volt. This 0 volt from pin B9 drives ZC307 pin A10 negative. causing the character feed bus (ZC313 pin B1) to go positive. Negative voltage from pin B10 of ZC112 allows the 240 hertz multivibrator (MV-B) of ZC313 to run, producing pulses on the 2400 wpm lead. These pulses enter ZC112 pin A7 to cause the punch to operate as described previously.

PARALLEL RECEIVING

3.30 After relays K2 and K3 of ZC418 (7746WD, Sheet 3) have operated at the time of power turn-on both inputs to LA-2F of ZC112 are normally negative. This causes ZC112 pin B27 to be at 0 volt and pin 9 to be negative. When parallel data is to be received the auxiliary sample lead goes positive, driving ZC112 pin A9 (the parallel sample lead) positive. This sets flip-flop D-B of ZC311, placing pin B33 at 0 volt. Pin A17 of ZC112 is driven negative, causing the receive parallel) bus to go to 0 volt. At the same time all inputs to LA-IF of ZC112 are negative, causing pin B28 to go to 0 volt and holding the receive serial bus negative.

3.31 Under these conditions (3.30) the punch drivers are primed from the auxiliary bit input leads described previously (3.22). When the auxiliary sample lead

goes negative ZC112 pin A9 goes negative. allowing ZC112 pin A10 to go to 0 volt. The power amplifier ZC120 then emits a pulse which causes the character present on the auxiliary bit leads to be punched. For additional characters the auxiliary sample lead continues to be pulsed. and each negative going transition causes a character to be punched. When no more characters are to be punched the auxiliary sample lead remains negative.

SERIAL RECEIVING

3.32 Serial data is received and converted to parallel circuits to be described later. When a character is assembled and ready for punching, a 0 volt pulse appears at ZC112 pin B7 which was negative. This pulse drives ZC112 pin A10 negative and also resets flip-flop D-B of ZC311. With ZC311 pin B34 at 0 volt and pin B33 negative, the receive parallel bus is held negative and the receive serial bus is held at 0 volt.

3.33 The previous conditions prevent parallel data on the auxiliary bit leads from reaching the punch, and allow data from the serial-to-parallel converter circuits to reach the punch. For example, the first bit of a character received serially is applied to ZC316 pin B6 and appears inverted at pin B10 because the receive parallel bus is negative. If the bit in question is marking ZC316 pin B6 will be at 0 volt, pin B10 will be negative. and pin A10 will be at 0 volt to prime the punch driver.

3.34 At the end of the serial sample pulse (ZC112 pin B7). pin A10 of ZC112 will go positive causing the character for which the drivers are primed to be punched. Further serial sample pulses cause the punching of an additional character at the end of each pulse. When no more characters are to be punched the serial sample pulse lead remains negative.

ALARM CIRCUITS

3.35 The LOW TAPE and END OF TAPE mercury switches are mounted on an arm attached to the tape supply reel holder. The END OF TAPE **switch is** adjusted to close when the tape supply has been used beyond the point at which the LOW TAPE switch operates. The LOW TAPE switch does nothing more than light the LOW TAPE indicator to advise the operator that the tape supply is **used** up. The END OF TAPE switch cuts off the associated equipment that sends messages to the receiver (Figure 3).

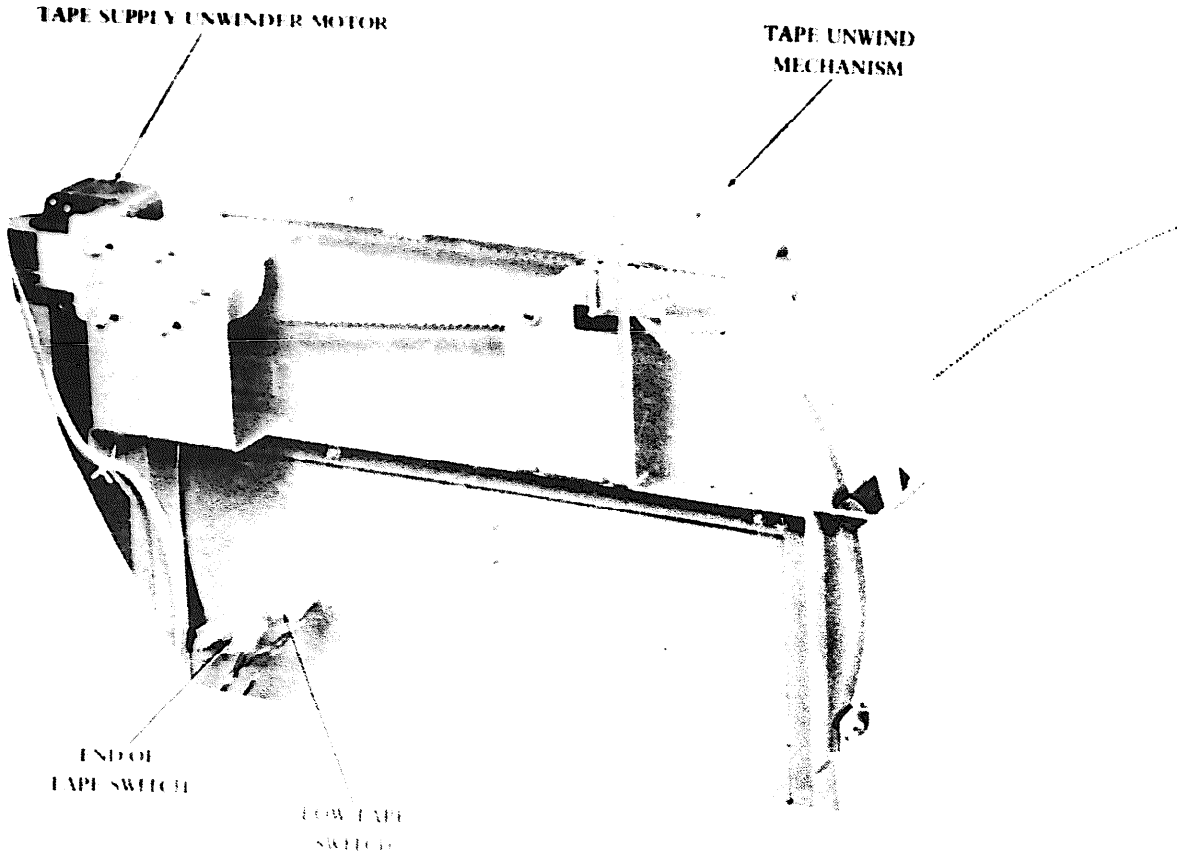
3.36 The **TAPE OUT switch arm is mounted on the** tape feed chute of the punch and closes if there is no tape in the tape path. The TIGHT TAPE contact isactuated by the punch tape supply tension lever when the tape loop in the punch becomes abnormally short. The CHAD BIN switch closes when the chad bin becomes full. as determined by weight (Figure 4). **Like** the LOW TAPE switch. this switch only lights an indicator when it operates.

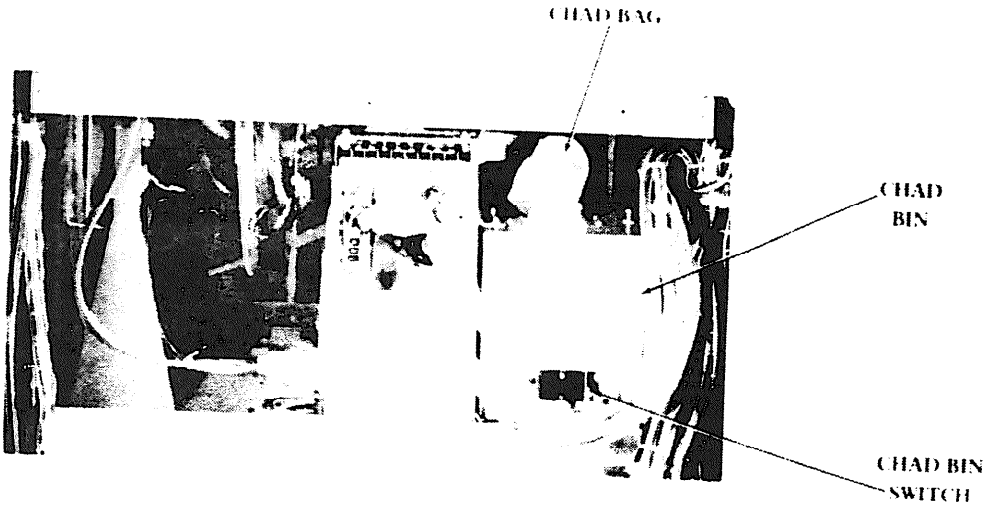
3.37 The NOR elements LA-1A and LA-2A of ZC110 form a latch circuit. When the END OF TAPE switch closes ZC110 pin A9 goes negative and pin A10 goes to 0 volt. Power amplifier PA-ID of ZC108 operates K4 of ZC318 to light the END OF TAPE lamp. An identical latch circuit involving LA-1B and LA-2B of ZC110, PA-2C of ZC108. and K3 of ZC318 controls the TAPE OUT lamp. Both of these latches are reset by pressing the associated END OF TAPE/TAPE OUT indicator switch, which causes ZC110 pins A10 and Al7 to go negative.

3.38 A similar latch using LA-1C and LA-2C of ZC110, PA-1C of ZC108, and K2 of ZC318 lights the TIGHT TAPE lamp when the TIGHT TAPE switch operates. Tape motion is detected by counting punch drive pulses between operations of the tape puller motor on the punch with an eight stage binary counter. The counter is reset each time the tape puller operates. The tape is not feeding properly if the tape puller does not operate before 161 or 162 drive pulses have been counted.

3.39 The counter **consists of flip-flops D-C, D-D,** D-E. **and** D-F **of** ZC311 **and flip-flops D-B.** D-C. D-E. and D-F **of** ZC309. The **counter is reset to zero by applying a positive pulse through diodes on the same cards to the inverted outputs of all the flip-flops except D-D in** ZC311. **When power is first applied the power on level signal at** ZC313 **pin** A31 **holds the reset bus negative. When** K2 and K3 **of** ZC-418 **operates. both inputs to PA-E of** ZC313 arc negative. **causing this element to generate a positive pulse** at **pin** A27. **resetting the counter flip- flops** (7746WD. Sheet 3).

3.40 When the tape **puller** motor **operates,** 60 **hertz ac is** applied to pin B13 of ZC307. This causes 60 hertz pulses at pin All. The NOR elements LA-2B and LA-1C **of** ZC307 form a latch to store tape **puller motor operations, for** the negative transition of the punch **drive pulse. These cycle** the 725 microsecond delay DY-B in ZC108. This resets the above latch and causes PA-E **of** ZC313 **to generate a positive** pulse and reset the counter **flip-flops.**


TAPE SUPPLY UNWINDER MOTOR
TAPE UNWIND
MECHANISM
END OF
TAPE SWITCH


CHAD BAG
CHAD
BIN
CHAD BIN
SWITCH

3.41 This counter reset causes pin A23 of D-D in ZC311 to go to -6 volts. The next drive pulse will place D-D in the set 1 condition. When pin A23 goes to 0 volt flip-flop D-C of ZC311 is set. This action continues down the counter until all flip-flops are set. The first drive pulse sets the counter to a full count of 255. The next drive pulse resets flip-flop D-D of ZC311 so that the counter holds a count of 254. These counts are determined by assigning values to the counter stages from left to right, 1, 2, 4, 8, 16, 32, 64, and 128. The count in the counter is determined by adding the values of all flip-flops that are set. The next drive pulse sets the first flip-flop again.

3.42 When pin A32 of ZC311 goes to 0 volt, flip-flop D-E of ZC311 is reset, so the count is 253. In the same manner the following pulses decrease the count in the counter by one for each pulse. After 160 pulses the counter will contain a count of 96, with flip-flops D-C and D-E of ZC309 set and all others reset. The next drive pulse sets flip-flop D-C of ZC311, and sets flip-flop D-E which sets flip-flop D-F. This sets flip-flop D-B of ZC309 which resets flip-flop D-C, and resets D-C and D-F of ZC309 which sets D-E. This causes all inputs to LA-1B of ZC307 to be negative, allowing pin A17 to go positive.

3.43 The negative edge of the next drive pulse then resets flip-flop D-D of ZC309. This operates relay K1 on ZC418 to light the TAPE FEED indicator. The tape puller motor normally operates more often than every 161 characters (as mentioned in 3.38). The counter is normally reset before a count of 95 is reached and flip-flop D-D of ZC309 is reset. Pressing the indicator associated with the TIGHT TAPE/TAPE FEED switch resets the TIGHT TAPE latch if it was set, or sets the TAPE FEED flip-flop D-D of ZC309, if it was reset.

3.44 This latter action (described in 3.43) starts with the switch in its normal position, ZC307 pin B27 is at 0 volt and pin B9 is negative. When the switch is operated B9 goes positive to set the flip-flop. The time delay associated with the prime input allows the flip-flop to be set even though the prime input goes negative at the same time the set input goes to 0 volt. The NOR elements LA-1E and LA-1F of ZC110 are connected together to form a seven input gate.

3.45 Normally all inputs are negative, allowing pin B28 to go to 0 volt. This holds pin B9 at a negative voltage, causing the power amplifier to operate relay KC119A. A 0 volt signal at any input of the seven input gate will release the relay to indicate an alarm condition to the associated equipment.

3.46 An alarm condition is also indicated if power to the receiver is turned off, since relay KC119A is also released as a result. The inputs to the seven input gate are BLANK FEED, CHARACTER FEED, BUSY OUT (operator switch), END OF TAPE, TAPE OUT, TIGHT TAPE, and TAPE FEED. The BUSY OUT switch is a push-on, push-off operator control, allowing the operator to remove the receiver from service. The indicator lamps for the BUSY OUT, BLANK FEED, and CHARACTER FEED indicator switches are also shown on 7746WD, Sheet 2.

SERIAL-TO-PARALLEL CONVERTER

3.47 Normal and inverted serial data are applied to sections B and C of the CODE LEVEL switch, respectively. If the switch is in the 8-level position, these signals are applied as primes to element D-B of ZD509. The outputs of this element are inverted by elements LA-1A and LA-1B of ZD507 and applied as primes to element D-C of ZD509. Similarly element D-D of ZD509 is primed from the inverted outputs of element D-C, and element D-E primed from the inverted outputs of D-D (7746WD, Sheet 7 and Sheet 8).

3.48 Elements D-B, D-C, D-E, D-F, and D-D of ZD513 are primed from the preceding elements. The group of flip-flops is arranged as a nine element shift register. When the CODE LEVEL switch is set to the 7-level position a ground is applied to pin A7 and pin A13 of ZD507 to allow the output of both LA-1A and LA-1B to go negative. The outputs of these elements, which are the primes of element D-C, ZD509, are connected to the normal and inverted serial leads through sections B and C of the CODE LEVEL switch. One or the other of the serial data leads will be held at 0 volt by the data. Therefore, element D-B of ZD509 is effectively eliminated from the shift register.

3.49 When the CODE LEVEL switch is set to the 6-level position the ground on A7 and A13 of ZD507 is maintained through diode CR-B of ZD507. A ground is applied to pin A24 and pin A31 of ZD507. At the same time the normal and inverted serial data leads are moved to prime D-D of ZD509, which eliminates D-B and D-C from shifting action. In a similar manner element D-D is eliminated from shifting action when the CODE LEVEL switch is in the 5-level position. The number of active elements in the shift register is always one greater than the number of levels indicated by the CODE LEVEL switch setting.

3.50 An additional element is used to hold the start bit in start-stop operation. Each shift register element except the start element primes a storage flip-flop. For example, element D-B of ZD509 primes element D-B of ZD511. In normal operation data is continuously shifted through the shift register without regard to character boundaries. The synchronizing logic (to be described in 3.73 through 3.78), keeps track of character boundaries, and sets the shift register contents into the storage flip-flops when a complete character is properly positioned in the shift register.

3.51 Normal and inverted storage flip-flop outputs enter the patching circuit card ZD517. This card allows the output circuits to be connected to the data storage flip-flops in any order, and with either normal or inverted polarity. The NOR and INV markings on the terminals of ZD517 (TB243) appear to be backwards with respect to the storage flip-flop output. This is done because the signals will be inverted in NOR gates before being presented to the punch driver and output amplifiers. The LEVEL markings on ZD517 correspond to punch levels and have no relation to the order in which bits are received.

3.52 The outputs from ZD517 for levels 2 through 6 pass through inverters to the punch drive logic, after inversion through output elements to the associated equipment. The R-C networks provided in these output leads are used to prevent fast rise time pulses from leaving the receiver, as an RF noise reduction measure.

3.53 The outputs from ZD517 for levels 1, 7, and 8 are passed through NOR gates controlled by the CODE LEVEL switch. For example, level 8 is applied to input B13 of ZD518. Elements LA-2A and LA-2B of this card are connected together to provide signal isolation and increased load driving capability, the outputs of these two elements are identical. With the CODE LEVEL switch in the 8 level position these elements act as a simple inverter. In the 5, 6, or 7 level position a ground is applied to input B12 of these elements, holding the outputs negative.

UNITS COUNTER

3.54 The units counter determines when a complete character is in the shift register by counting clock pulses. To perform this function the units counter must be properly aligned with respect to character boundaries; it must start counting at the first bit of a character and stop at the last bit, and then reset to the starting position (Sheet 6).

3.55 The synchronizing circuits which align the counter with character boundaries will be described in 3.79 through 3.85. For the present discussion it will be assumed that the counter is properly aligned. In the SYNCHRONOUS operation all received bits are data bits. In the START-STOP operation a character is always preceded by a start unit and may or may not be followed by one or more stop units. In either case clock pulses are supplied continuously, so that a stop element must contain an integral number of units.

3.56 The SIGNAL MODE switch selects SYNCHRONOUS or START-STOP operation. The CHAR. SYNC. switch in the OFF position allows reception of characters which always contain a specified number of units. In the ON position the receiver can accept characters having stop elements containing an unspecified number of units. The SIGNAL MODE switch is equipped with a latching circuit. The NOR element ZD303 pin A9 is at 0 volt and pin A11 is negative in the START- STOP position. These conditions are reversed in the SYNCHRONOUS position.

3.57 The counter is composed of flip-flops D-B, D-C, D-D, and D-E of ZD503. In synchronous operation the starting position of the counter is the element D-B, which is reset while the other elements are set. (Sheet 6, the semicircular symbols with the letter D, are additional Prime and set inputs for the flip-flop.)

3.58 The counter is placed in this position by the last character shift pulse. This resets element D-B directly and fires the 100 microsecond one-shot DY-B pulse of ZD305 to pull counter elements D-C, D-D, and D-E into the set condition. In the starting position of the START-STOP operation of the counter all flip-flops are set. With the counter placed in the condition just described, the element D-B is primed to be set rather than reset.

A. Synchronous Operation, 5 Units Per Character

3.59 The output at pin A10 of ZD303 is held negative by the 0 volt input at pin A6. With the synchronous prime signal also negative, the inverted clock pulses are reinverted by LA-1B of ZD303. This causes counter element D-B to be driven by normal clock pulses. The positive-to-negative clock transition occurs in the center of a data bit. The negative-to-positive transition occurs at the time of data transitions. Therefore, the counter is advanced at the time of data transitions.

3.60

3.60 The first clock pulse sets counter element D-B. As pin B34 of this element goes negative pin A26 of ZD303 goes positive to reset element D-C. The next clock pulse resets element D-B. The third clock pulse sets D-B, which sets D-C, and resets D-D. The fourth clock pulse resets D-B. The fifth clock pulse sets D-B which resets D-C. Table A summarizes the action.

TABLE A

FLIP-FLOP OPERATION, 5 UNITS PER CHARACTER

CLOCK PULSE	D-B	D-C	D-D	D-E
0	Reset	Set	Set	Set
1	Set	Reset	Set	Set
2	Reset	Reset	Set	Set
3	Set	Set	Reset	Set
4	Reset	Set	Reset	Set
5	Set	Reset	Reset	Set

3.61 After the fourth clock pulse, and the UNITS PER CHARACTER INTERVAL switch set at 5 (SYNCHRONOUS), all inputs to element LA-1C of ZD303 were negative allowing the output to go to 0 volt. After the fifth clock pulse, pin A27 of ZD303 goes negative. This causes PA-E of ZD305 to emit a pulse, which triggers DY-B of ZD305. These two signals reset the counter to the condition mentioned above for clock pulse 0.

3.62 The pulse from pin A27 of ZD305 is the character shift pulse, and sets the shift register contents into the storage flip-flops. The pulse from DY-B of ZD305 is inverted by element LA-2A of ZD520. The resulting signal goes positive 100 microseconds after the clock pulse which caused the counter to be reset. Pin A21, LA-1F of ZD518 is at 0 volt in synchronous operation (Sheet 8). Therefore, pin B28 of ZD518 is negative and pin B27 of ZD520 is at 0 volt, priming the 2 millisecond one-shot DY-A of ZD305. This is triggered by the character shift pulse.

3.63 The normal output of the one-shot is made available to external equipment. The one-shot output is inverted by LA-1F of ZD520 to form the sample pulse for the punch driver. This pulse enters pin B7 of ZC112 and causes the character in the storage flip-flops to be punched (Sheet 4). The timing diagram in Figure 5 is of the counter operations described in the preceding paragraphs. To relate the description to the figure, the first clock pulse is represented in Figure 5 as the positive going clock transition following the number 1 data pulse, the second clock pulse follows the number 2 data pulse, and so on.

3.64 This mode of operation is the same as described in the previous paragraphs, except that more clock pulses are received before LA-1C of ZD303 detects the completion of a character (Figure 6). Table B shows the various flip-flop states, the first six are the same as those given previously.

C. Start-Stop Operation, 6 Units Per Character, 5-Level

3.65 In this mode of operation the 5 bits of a character are preceded by a start pulse. With the SIGNAL MODE switch in the START-STOP position pin A9 of ZD303 is at 0 volt, pin A11 is negative. This removes the reset prime from counter element D-B, and applies a set prime, so that the starting position of the counter is that in which all flip-flops are set.

3.66 With the CHAR. SYNC. switch in the OFF position, the established synchronous operation proceeds as described in the 5 unit synchronous operation, except for the starting position of the counter and the method of obtaining the punch sample pulse. Table C shows the various counter states.

3.67 As compared with synchronous operation one additional clock pulse is received before the character shift signal is generated and the counter is reset. Referring to 7746WD, Sheet 8, input A21 of LA-1F, ZD518 is negative in START-STOP operation. When the start pulse is in element D-D of ZD513 input A34 of LA-1F, ZD518 goes to 0 volts because of appropriate strapping on ZD517. This causes pin B27 of ZD520 to go to 0 volt, and primes DY-A of ZD305 to generate the sample pulse as before when the character shift pulse arrives. The timing diagram for this mode of operation is shown in Figure 7.

D. Start-Stop Operation, 7 Units Per Character, 5-Level

3.68 If the data information consisted of a start pulse followed by 6 data bits, then operation is the same as described previously. With the exception that this setting of the UNITS PER CHARACTER INTERVAL switch causes the counter to count one additional pulse before generating the character shift signal. An exceptional case is that in which the start pulse is always spacing and the 5 data bits are followed by a stop pulse which is always marking. In this case the CHAR. SYNC. switch may be operated to the ON position, permitting receipt of characters in which the stop pulse may have a duration of an indefinite number of units.

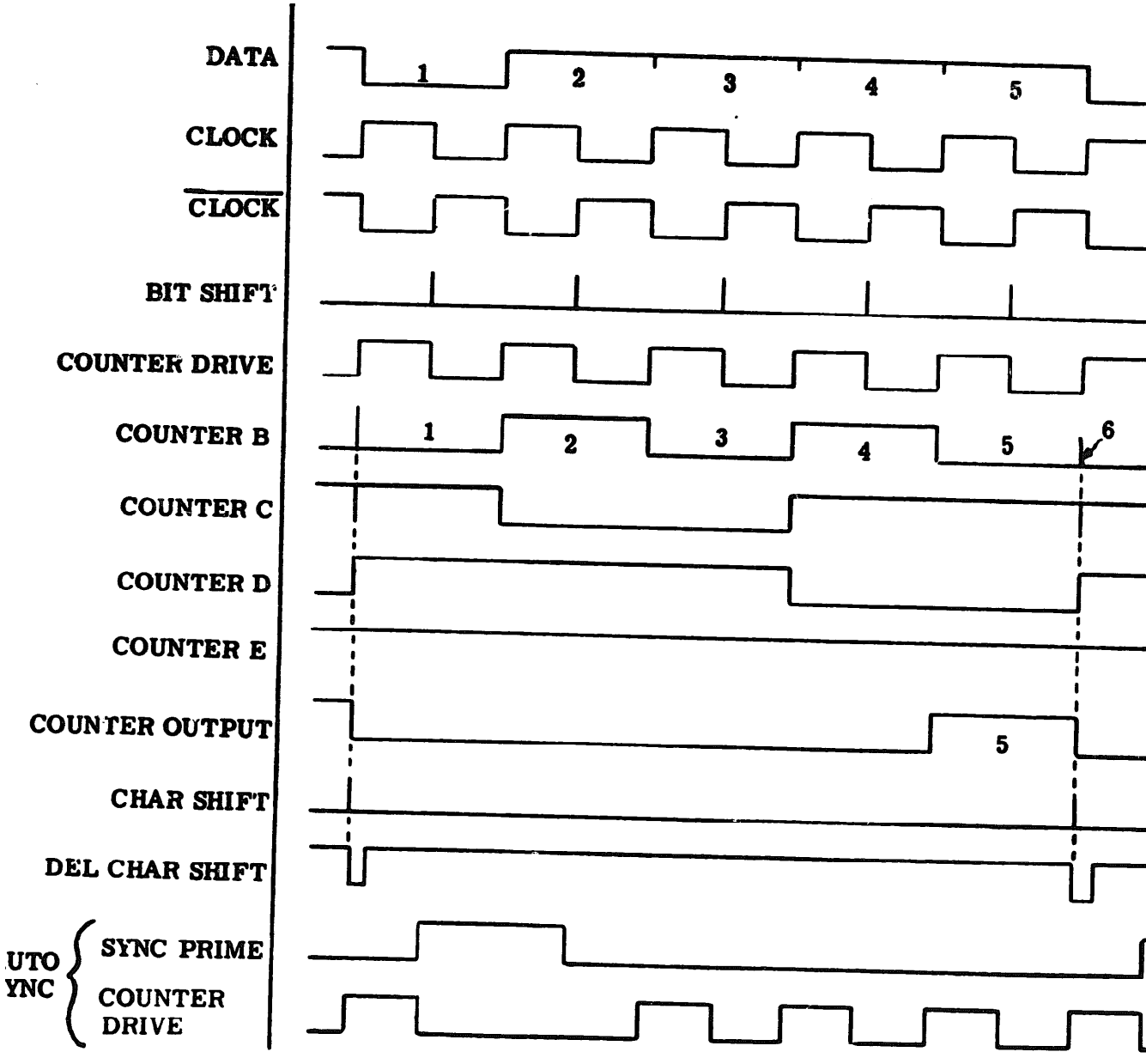


Figure 5- RDL Logic for 5 Unit 5-Level Synchronous operation

TABLE B

FLIP-FLOP OPERATION, 10 UNITS PER CHARACTER

CLOCK PULSE	D-B	D-C	D-D	D-E	REMARKS
0	Reset	Set	Set	Set	
1	Set	Reset	Set	Set	
2	Reset	Reset	Set	Set	
3	Set	Set	Reset	Set	
4	Reset	Set	Reset	Set	
5	Set	Reset	Reset	Set	
6	Reset	Reset	Reset	Set	
7	Set	Set	Set	Reset	
8	Reset	Set	Set	Reset	
9	Set	Reset	Set	Reset	ZD303 pin A27 to 0 volt.
10	Reset	Reset	Set	Reset	Reset to clock pulse 0.

TABLE C

FLIP-FLOP OPERATION, 6 UNITS PER CHARACTER

CLOCK PULSE	D-B	D-C	D-D	D-E	REMARKS
0	Set	Set	Set	Set	
1	Reset	Set	Set	Set	
2	Set	Reset	Set	Set	
3	Reset	Reset	Set	Set	
4	Set	Set	Reset	Set	
5	Reset	Set	Reset	Set	ZD303 pin A27 to 0 volts.
6	Set	Reset	Reset	Set	Reset to clock pulse 0.

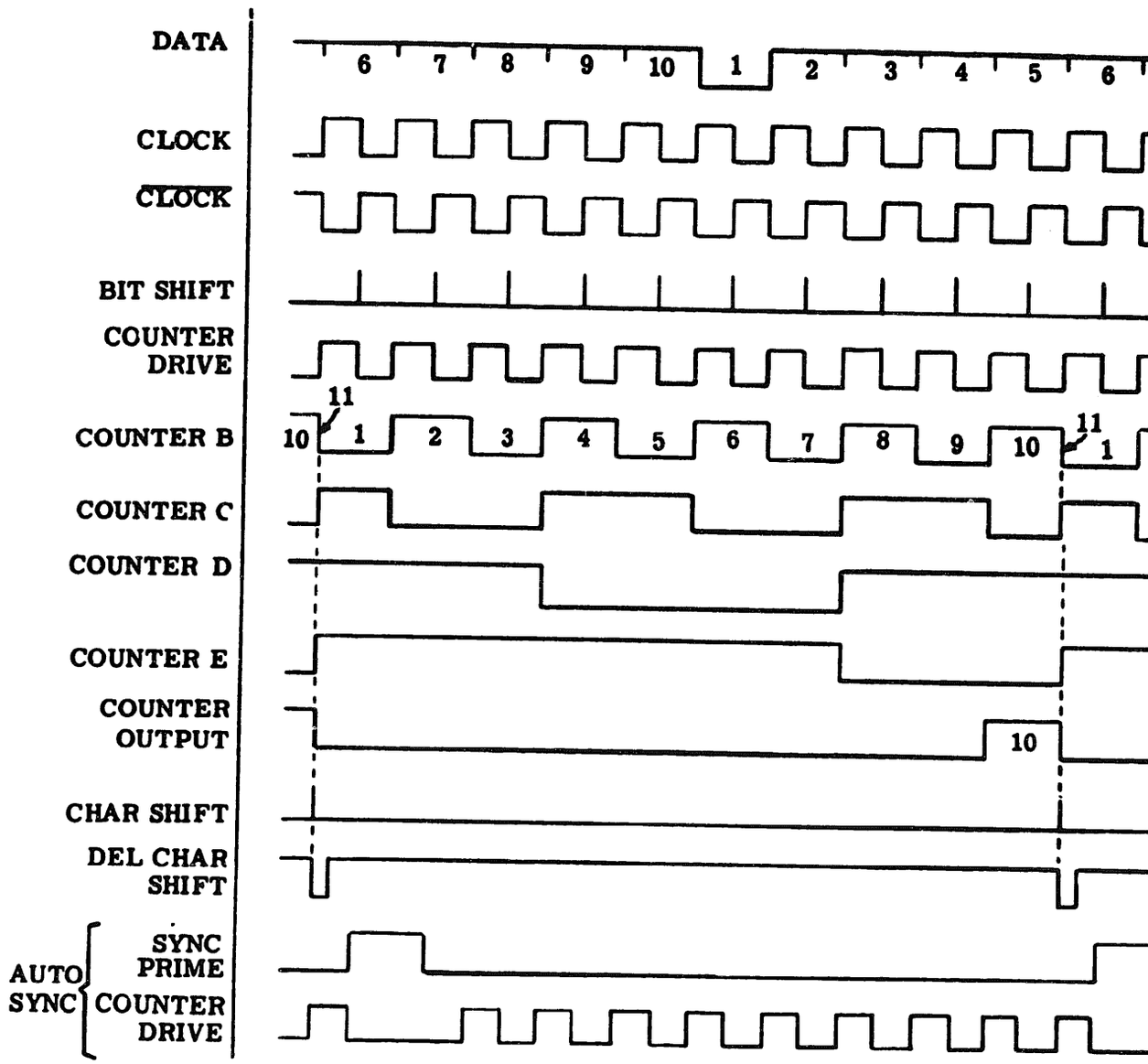


Figure 10 RDL Logic fo 10 Unit 10-Level Synchronous operation

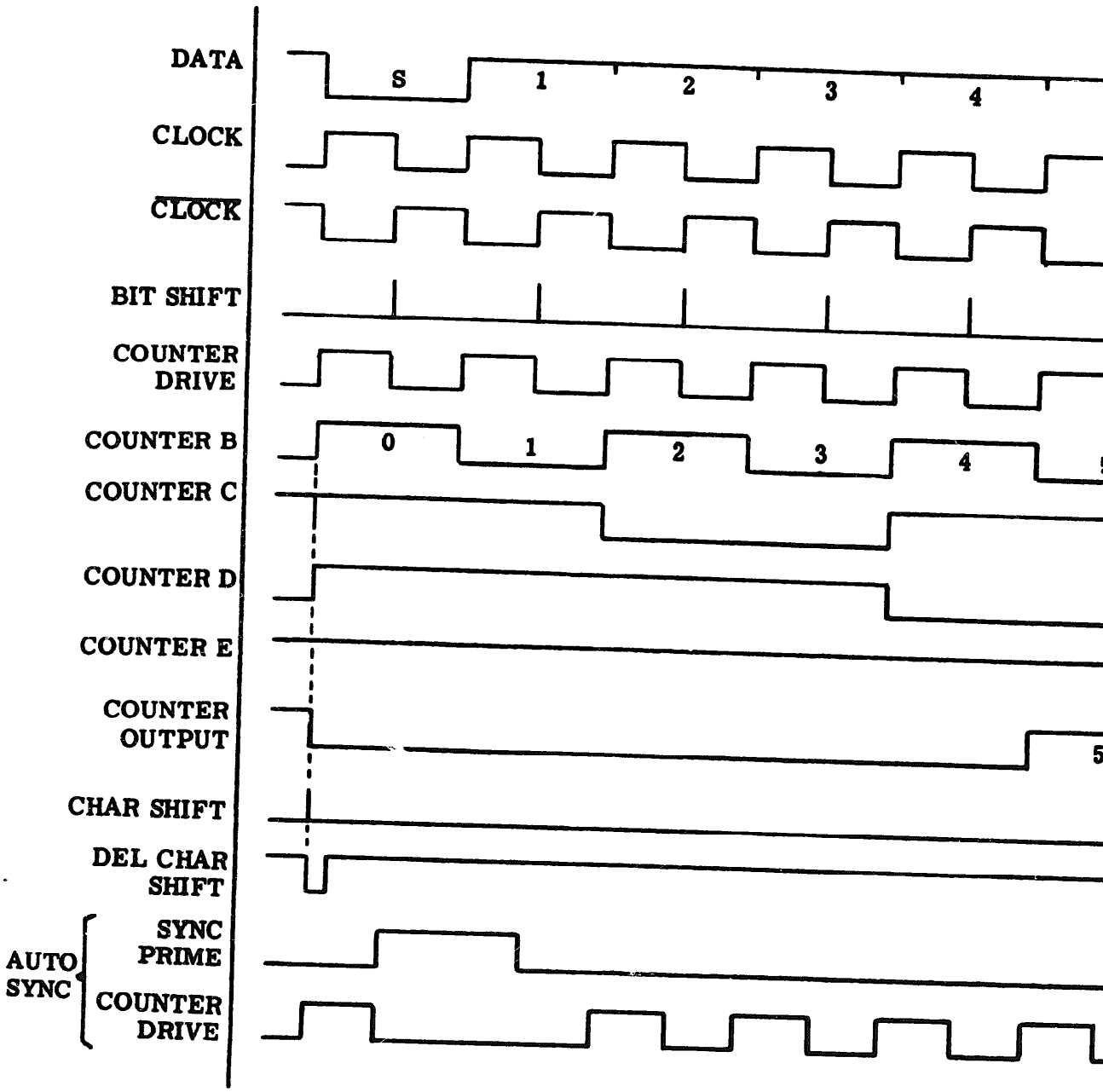


Figure 7 RDL Logic for 6 Unit, 5-Level (Start-Stop)

3.69 In this mode of operation the character synchronous prime signal controls the output of LA-1A, ZD303. When the character synchronous prime signal is 0 volt, pin A10 of ZD303 is negative as before and clock pulses reach the counter. When the character synchronous prime signal is negative pin A10 of ZD303 goes to 0 volt. This holds pin A17 of ZD303 negative at all times so that clock pulses cannot reach the counter. The character synchronous prime signal is controlled by flip-flops D-B and D-C of ZD505. During receipt of a character both of these elements are set, so that the character synchronous prime lead is at 0 volt (Sheet 5).

3.70 When the complete character has been received and transferred into the storage flip-flops, the delayed character shift signal resets element D-B. This occurs 100 miscroseconds after the beginning of the stop pulse. The next bit shift (clock) pulse resets element D-C in the center of the first unit of the stop pulse. With element D-B reset no further clock pulses are counted, so the counter remains in the state corresponding to a number 0 clock pulse.

3.71 No change takes place in the circuit, as long as the incoming data lead remains marking. When the incoming data lead goes spacing, pin A26 of ZD507 goes positive to set element D-B. This allows clock pulses to reach the counter, the first clock pulse also sets element D-C. This element is necessary to delay priming element D-B for one half unit of time, because a slow rise time data input could otherwise cause D-B to be set falsely.

3.72 The timing diagram for this mode of operation is shown in Figure 8. The timing diagram for the 10 unit 5 level start-stop operation is shown in Figure 9, which is the same as that just described except for the different setting of the UNITS PER CHARACTER INTERVAL switch and the greater number of pulses counted.

E. Synchronization

3.73 In the preceding paragraphs it has been assumed that the receiver is properly synchronized, meaning, the counter is reset between characters. It is possible for the receiver not to be synchronized resulting in the character shift pulses not coinciding with character boundaries. This causes each punched character to contain some bits from one data character and some bits from the adjacent character. The circuits to be described perform the function of placing the receiver in synchronism.

3.74 The usual method of synchronizing is suppressing clock pulses from reaching the counter. This is the function of the synchronous prime lead. The 0 volt on this lead holds ZD303 pin A17 negative so that clock pulses are not counted (Sheet 6). A negative voltage on this lead allows the pulses to be counted normally. During synchronizing one clock pulse is deleted during each character interval. This causes the counter to fall behind the data stream. The synchronizing action should stop when the counter falls into the correct position with respect to the data.

3.75 Synchronizm cannot be achieved if any or all of the following conditions are present:

(a) If the UNITS PER CHARACTER INTERVAL switch is not set correctly for the data being received.

(b) If the SIGNAL MODE switch is not set to its proper position.

(c) If the CHAR. SYNC. switch is turned ON when the data stream does not contain proper start-stop pulses.

3.76 With miscellaneous signals being received it is impossible for the receiver to determine whether it is in or out of synchronism. Operating the MANUAL SYNC. indicator switch allows the operator to slip the counter. This process can be repeated until the data being punched appears to be reasonable, as determined by inspecting the tape. The counter slips one position for each operation of the MANUAL SYNC. indicator switch.

3.77 The automatic synchronizing mode causes the receiver to search for a predetermined idle character pattern in the received data. Whenever this character is being received a search for synchronism can be initiated by pressing the AUTOMATIC/MANUAL SYNC MODE indicator switch, unless the receiver is already in synchronism. The AUTOMATIC/MANUAL SYNC MODE switch controls whichever mode is to be used by controlling flip-flop D-D of ZD505. This flip-flop is set for the automatic mode and reset for the manual mode.

3.78 In the automatic mode a negative voltage at pin B22 of ZD505 causes relay K1 of ZD526 to be operated by PA-1D of ZD305. In the manual mode a negative voltage at pin A23 of ZD505 causes PA-2D of ZD305 to operate relay K2 of ZD526. These relays operate the AUTOMATIC SYNC MODE and MANUAL SYNC MODE indicators, respectively. The AUTOMATIC/MANUAL SYNC MODE siwtch operates a latch composed of LA-1D and LA-1E of ZD303. Pin B10 of ZD303 goes to 0 volt when the switch is operated, and pin B34 of ZD303 goes to 0 volt when the switch is released.

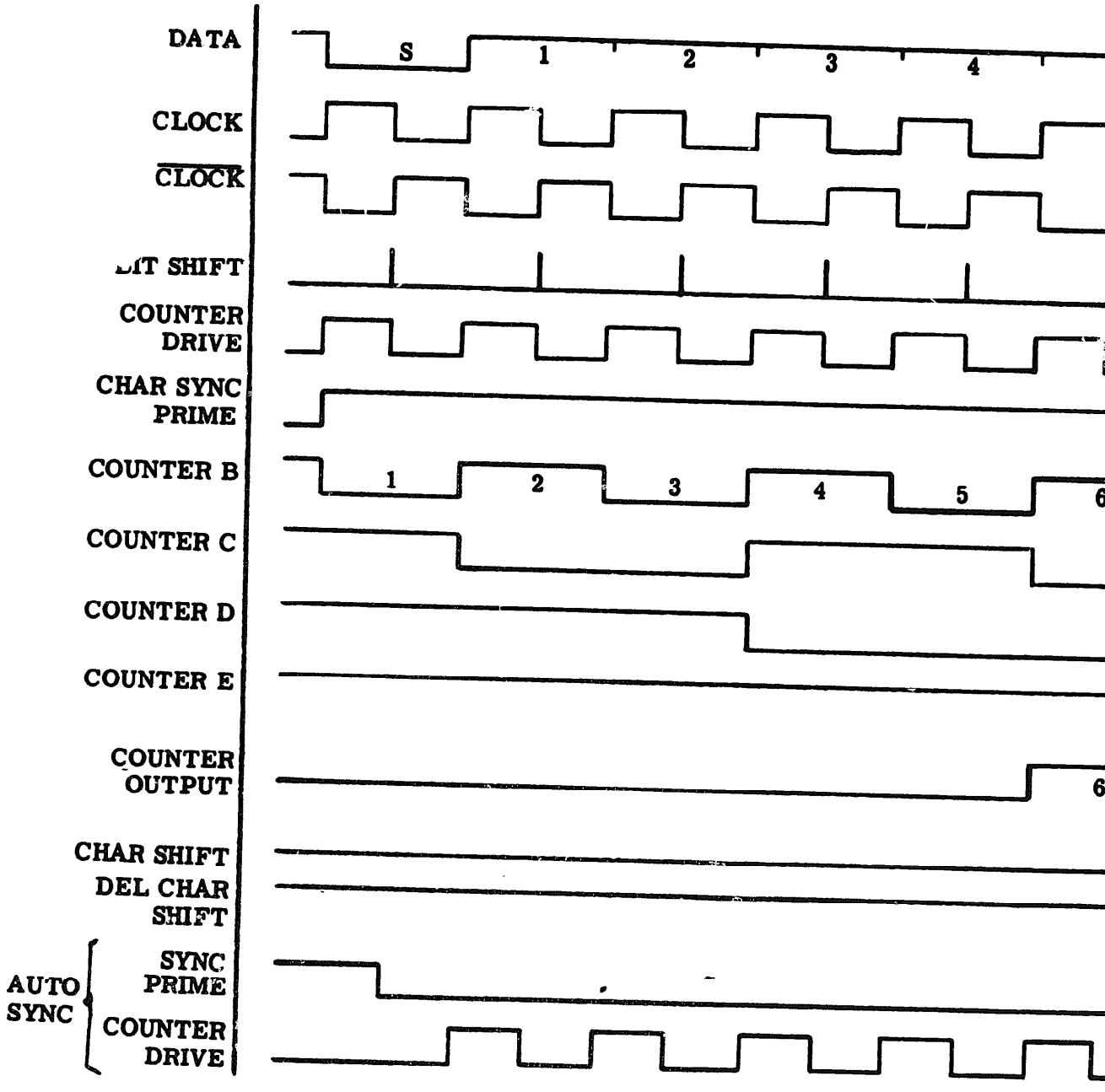


Figure 7 RDL Logic for 7 Unit, 5-Level (Start-Stop)

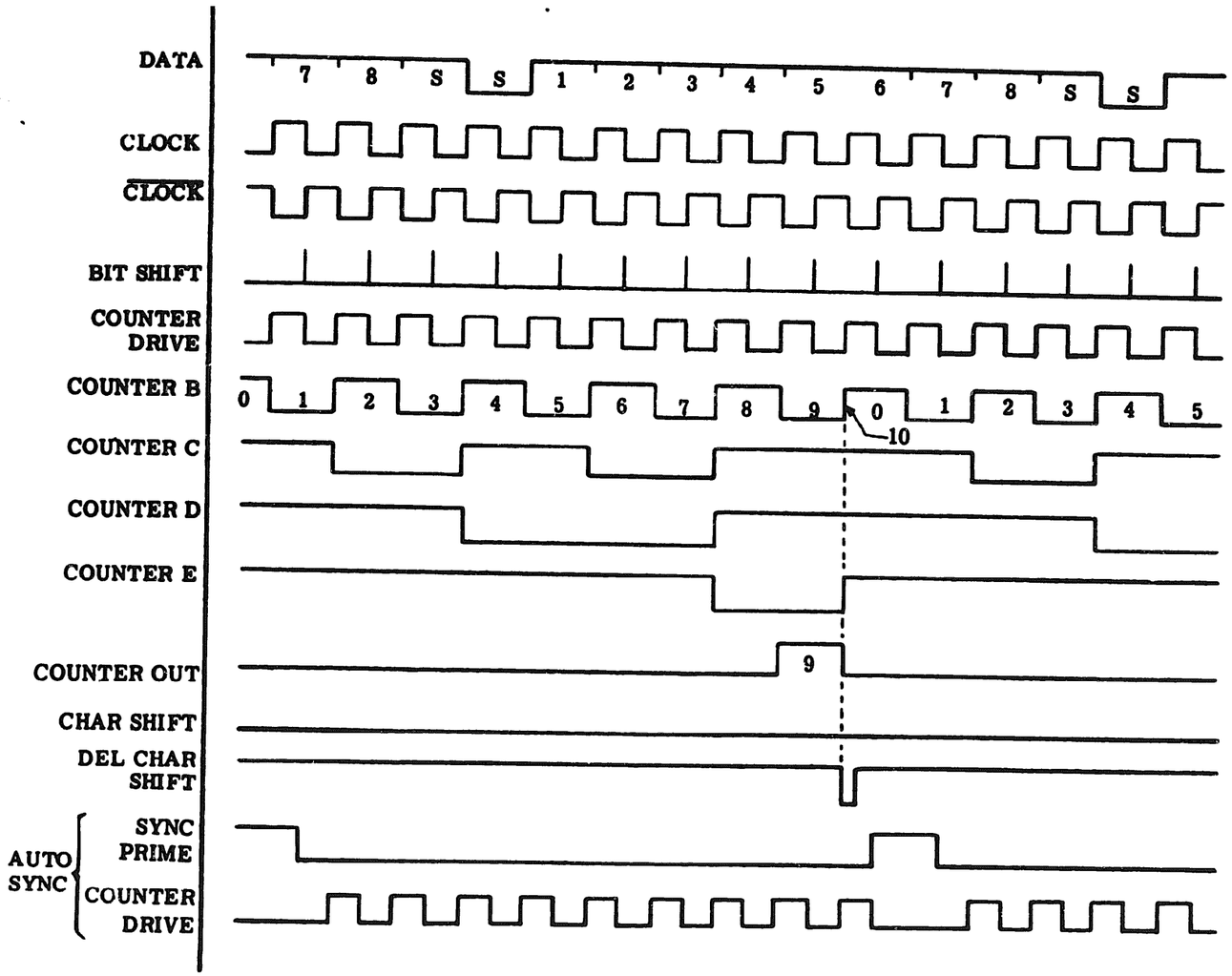


Figure 9 RDL Logic for 10 Unit, 5-Level (Start-Stop)

Automatic Synchronism

3.79 The output of LA-1A, ZD520 is 0 volt when the receiver detects the idle character (Sheet 7). This occurs when all inputs to this NOR element are negative. The outputs of ZD517 indicate negative voltage marking signals. Inputs A7, A6, and B7 of LA-1A are connected to code levels 6, 5, and 4 respectively. Diodes CR-E and CR-F of ZD515 form two additional inputs to the gate for bits 3 and 2, respectively (Sheet 8).

3.80 Elements LA-2C, LA-2D, and LA-2E of ZD520 have their outputs connected in parallel. If any of these gates have both inputs negative, input A5 of LA-1A, ZD520, will be held at 0 volt. Therefore, the in synchronous lead will go to 0 volt, only if levels 2 through 6 after passing through ZD517 are marking, and if each of the gates LA-2C, LA-2D, and LA-2E of ZD520 have at least one input at 0 volt. The latter condition is satisfied if the levels in use, out of group 1, 7, and 8 are marking and the CODE LEVEL switch is set correctly for the number of levels in use. For example, with 7-level operation, the CODE LEVEL switch grounds input B23 of LA-2C so the condition of the eighth level flip-flop is immaterial.

3.81 The elements LA-2D and LA-2E do not have their inputs (B30 and A1) grounded by the CODE LEVEL switch. Therefore, inputs B31 and B1 must be at 0 volt, which is the marking condition, for the in synchronous lead to go to 0 volt. This causes pin A11 of LA-2B, ZD520 to be held negative and prevents flip-flop D-D of ZD505 from being set (Sheet 5). With the preceding conditions available, pin A11 of ZD520 goes to 0 volt to prime flip-flop D-D to be set.

3.82 Operating the AUTOMATIC/MANUAL SYNC MODE switch once, causes B10 of ZD303 to go to 0 volt, setting flip-flop D-D. This primes flip-flop D-E, which is set by the next delayed character shift pulse, at the positive going transition. This causes pin B10 of flip-flop D-E to go to a negative voltage. If the synchronous prime signal is negative pin B27 of LA-2F, ZD507 goes to 0 volt priming flip-flop D-F. The next bit shift pulse sets flip-flop D-F which primes itself to be reset and holds the synchronous prime lead at 0 volt to prevent the next clock pulse from being counted.

3.83 The next bit shift pulse resets element D-F, which then allows clock pulses to reach the counter. When the synchronous prime lead goes negative pin B3 of D-F goes to 0 volt, resetting flip-flop D-E. Therefore, one clock pulse has been inhibited from reaching the counter. If the receiver is still not synchronized, the next delayed character shift sets flip-flop D-E again, causing another pulse to be dropped.

3.84 When synchronism is achieved the in synchronous lead goes to 0 volt on the positive edge of the character shift pulse. This and the inverted character shift, reset flip-flop D-D through the auxiliary input gate. This removes the set prime from flip-flop D-E before the delayed character shift pulse arrives. Therefore, flip-flop D-E is not set and further clock pulses are prevented from reaching the counter by this circuit.

3.85 If synchronism cannot be achieved because there are no characters in the data stream the operator can press the AUTOMATIC/MANUAL SYNC MODE switch again As flip-flop D-D primed itself to be reset, it removed its set prime as it was set, and will reset when the switch is operated. The operator can then try to achieve synchronism with the manual procedure.

Manual Synchronism

3.86 The MANUAL SYNC indicator switch drives a latch composed of LA-1F and LA-2F of ZD303, pin B27 of ZD303 goes to 0 volt when the switch is operated. With flip-flop D-D of ZD505 reset, the auxiliary setting gate of flip-flop D-E is primed. Operating the MANUAL SYNC switch, sets flip-flop D-E, causing a clock pulse to be inhibited from reaching the counter as described previously for automatic synchronizing.

3.87 Because of the ac coupled auxiliary setting gate is is necessary to operate the MANUAL SYNC switch once for each clock pulse to be slipped. Operating this switch the number of times equal to the UNITS PER CHARACTER INTERVAL switch setting, will slip the counter around to its original position. Therefore, to bring the receiver into synchronism, the switch should be operated only the number of times indicated by the UNITS PER CHARACTER INTERVAL switch.

URGENT TRAFFIC

3.88 Urgent traffic, detected by the associated equipment requires immediate operator attention. When urgent traffic is received the associated equipment drives the urgent traffic input lead positive. Inverters LA-1D, and LA-1E of ZD520, insure a sufficiently fast rise time to set flip-flop D-D of ZD515. This causes pin B22 to go to a negative voltage activating PA-2C of ZD305 which operates relay K3 of ZD526. This relay lights the URGENT TRAFFIC indicator (Sheet 5).

3.89 The URGENT TRAFFIC switch drives a latch composed of LA-1B and LA-1C of ZD520. Normally pin A27 is negative and pin A17 is at 0 volt. This primes flip-flop D-D to be reset. Operating the switch causes pin A27 of ZD520 to go to 0 volt, resetting flip-flop D-D and turning off the URGENT TRAFFIC indicator. The time delay, associated with the priming action allows flip-flop D-D to be reset, as the prime input goes negative the reset input goes to 0 volt.

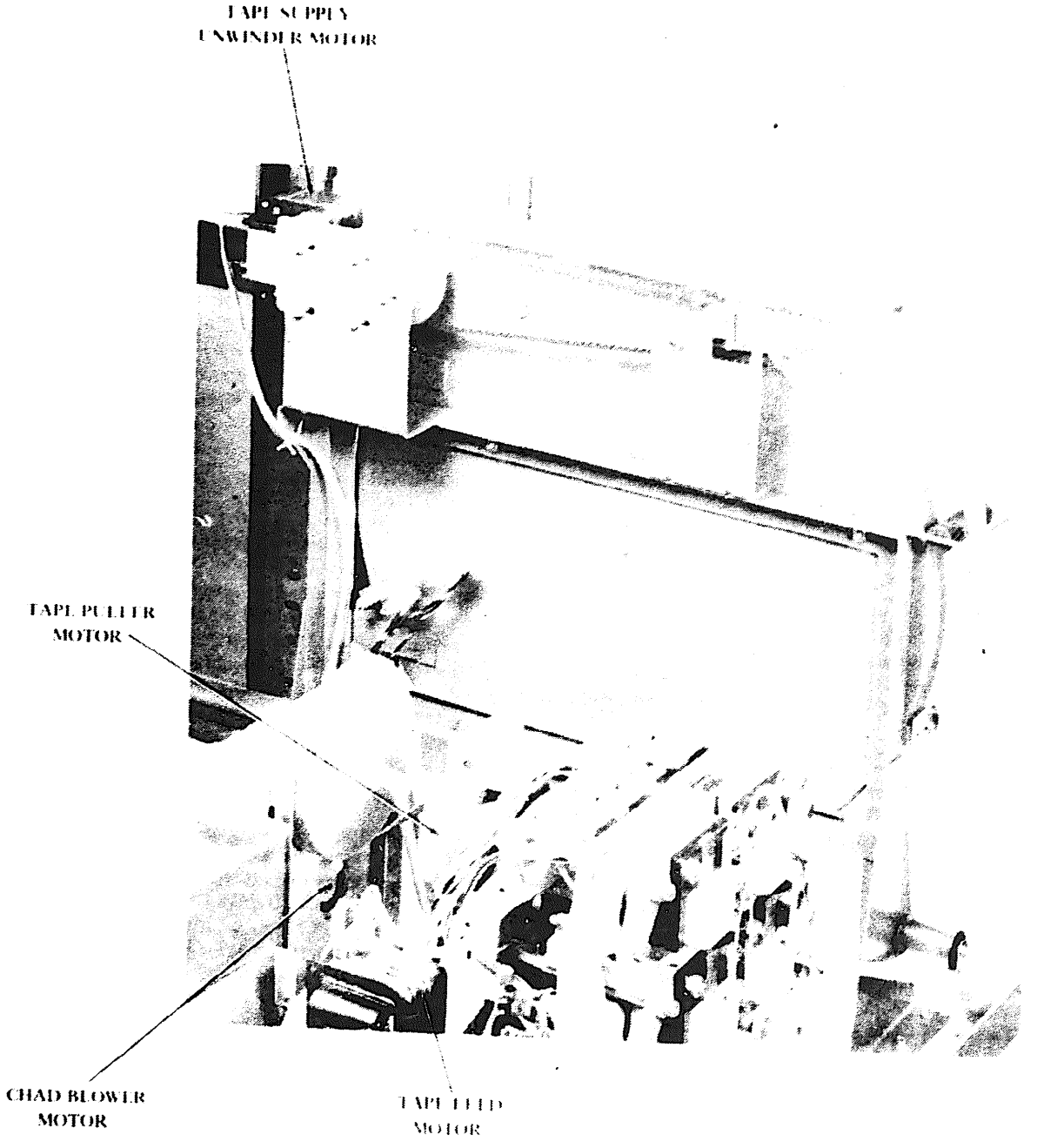


Figure 10 Tape Supply and Chad Blower Mowers

3.90 There are three independent ac input circuits, one for each receiver (upper and lower), and one for the cabinet outlets and fans. Each input is filtered through a 0.47 microfarad bypass capacitor (for rfi purposes) and protected by a 15 ampere circuit breaker. The ac outlets are protected with 5 ampere circuit breakers. Operating either power switch, SW110 or SW210 (upper or lower), activates the three exhaust fans which are protected by a 1 ampere circuit breaker (Figures 2 and 4). The upper reperforator shelf receives its power through the bidirectional silicon switch SST, protected by a 4 ampere circuit breaker (Sheet 9).

3.91 The power supply for the upper receiver is protected by a 5 ampere circuit breaker inside the power supply. The gate circuit for each switch is controlled by a separate pole of the POWER switch, protected by a 1 ampere circuit breaker. A thermal cutout switch removes power to the power supply and reperforator shelf when excessive cabinet temperature is detected. The lower power distribution circuits are similar to those in the upper receiver and will not be described separately.

REPERFORATOR POWER

3.92 Each reperforator shelf includes the following four motors; tape supply unwinder, chad blower, tape puller, and tape feed. The chad blower and tape supply unwinder motors run continuously as long as the POWER switch is on (Figure 10). The tape puller motor is mounted on the tape input side of the punch mechanism. The switch contacts for this motor close when the tape slack in the tape guide loop is used up. This causes the bidirectional silicon switch associated with the tape puller motor to conduct, activating the motor (Sheet 10). The switch contacts for the tape feed motor close whenever the tape feed spring becomes unwound. This causes the bidirectional silicon switch associated with the tape feed motor to conduct, activating the motor.

3.93 The power supply employs a ferroresonant transformer to regulate for line voltage variations. Five separate windings, each with a full-wave rectifier, filter capacitor, and bleeder resistor are used for the outputs of -55 volts, -12 volts, -6 volts, -5 volts, and +6 volts (Sheet 11).

3.94 The -55 volt supply is used by the punch drivers. Each punch driver has a separate 1.7 ampere circuit breaker. The -5 volt supply is used for the punch holding circuits and is protected by a 25 ampere circuit breaker. The -12 volt supply is used by the logic circuits and is protected by a 3.5 ampere circuit breaker. The +6 volt and -6 volt supplies are electronically regulated with the polarity determined by which side is grounded. Except for some resistor values and circuit breakers these two supplies are alike. Due to the fact that both supplies are similar, only one will be described.

3.95 The Q6 emitter follower carries the entire current load of the supply. The base current is supplied through emitter follower Q4. The -12 volt base current comes directly from the power supply through R12. The base current may be diverted from Q4 through Q3 and CR12. The amount of diverted current is controlled by the base current of Q3. This is partly determined by the difference in potential between the CR12 drop and the output voltage at the arm of the variable resistor R16. The voltage across CR12 is a constant 4.7 volts regardless of the current through this diode.

3.96 If the output of the -6 volt supply tends to increase, more current will flow through R17 and the upper portion of R16 into the base of Q3 and through CR12. This will cause an increased current through R12 and Q3, causing the voltage at the collector of Q3 to become more positive. This reduces the base current into Q4, which reduces the base current into Q6. This causes an increased voltage drop across Q6, tending to restore the output of the supply to normal. Similarly, a decrease in output will decrease the base current into Q3, making more base current available to Q4 and therefore to Q6. This reduces the drop across Q6 and tends to increase the output of the supply.

HIGH SPEED TAPE RECEIVER WITH RADIO FREQUENCY INTERFERENCE (RFI) SUPPRESSION FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

INSTALLATION AND CHECKOUT

CONTENTS

1.

1.01 This section contains information necessary to install radio frequency interference (RFI) suppression equipment on standard high speed receivers. It is used with reference to the standard (MAPS) literature as additional information relating to certain modules and components. The operating functions of the high speed tape receivers are unchanged.

1.02 Wiring diagram sections contain pertinent actual and schematic wiring diagrams for rfi circuitry. Reference should be made to the appropriate wiring diagram for specific wiring information.

1.03 All references to right or left, front or rear, up or down, are made from a normal operating position in front of the cabinet. Clearance for service and maintenance is necessary in front, rear, and top of cabinet. Tape handling equipment, tape punch, chad box, tape supply, electronic logic, and power supplies are accessible from the front of the cabinet (Figure 1).

2.

2.01 All equipment is packed for maximum protection during shipment. Caution must be taken when unpacking the rfi modification parts cartons (one carton for master and supplementary cabinets and one carton for receiver cabinet) to prevent damage to the components. Observe all caution labels as well as any special instructions on the cartons. Small bags and loose parts should be kept with their associated components until used in the installation. Refer to appropriate parts literature for identification of components.

3.

DOOR SHIELDING

3.01 Unlatch upper tape punch door and pivot down to its open position (Figure 2). Remove all upper window mounting hardware including door handle and window tape guide hardware. Leave plastic window in place, lay TP333327 screen over window aligning screw holes and tape exit openings. Place the TP333311 frame with flange up over the screen, replace handle, window tape guide hardware with ground strap, and upper window mounting hardware. Place tape punch door in its latched position.

3.02 Unlatch lower tape punch door and pivot down to its open position. Repeat operation in 3.01 using TP333328 screen, and TP333312 frame shield parts, reassemble in the same manner. Place lower tape punch door in its latched position.

3.03 Open tape supply door (to the right), and remove window bracket hardware (four screws and lockwashers). Discard left window bracket. Remove plastic

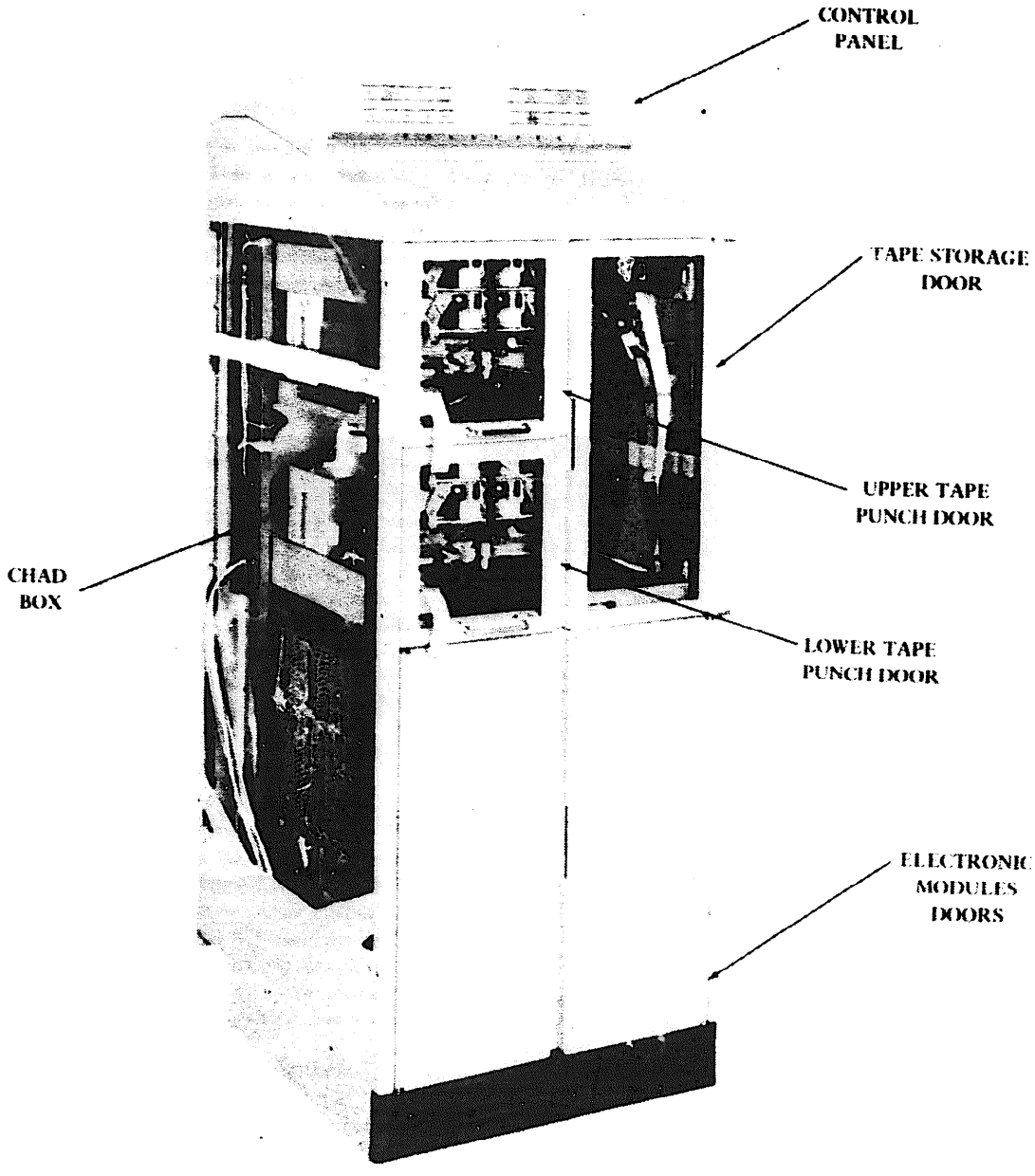


Figure 1 High Speed Tape Receiver Cabinet

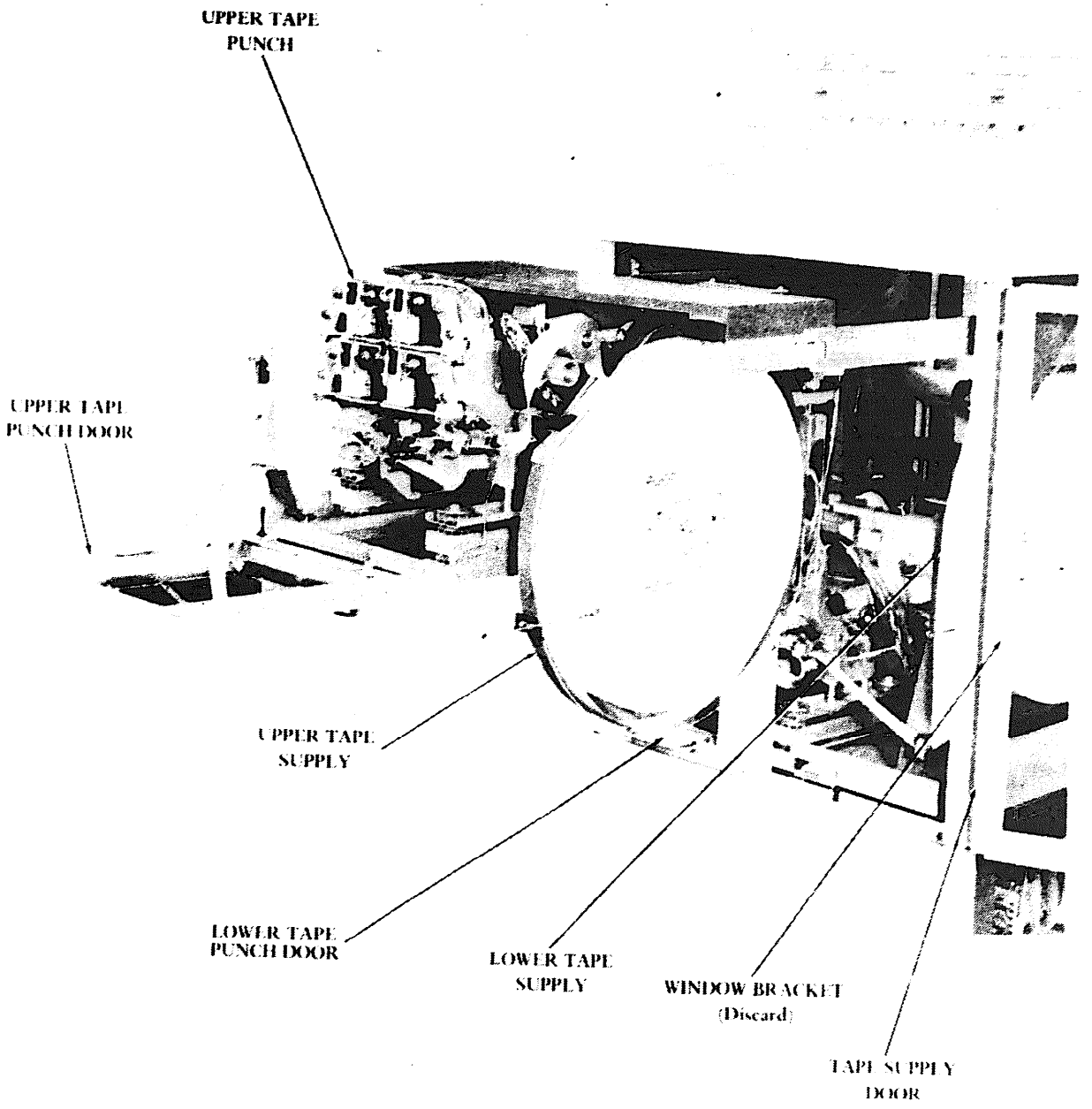


Figure 2 Tape Punch and Punch and Tape Supply Doors

window and pry up stationary metal flange on opposite side of window frame to allow for additional thickness necessary for added screen and frame.

3.04 Replace plastic window and place TP333329 screen on window. Place TP333313 frame on the screen with flange up and against the window. Make sure the frame is under the pried up window flange. Place new TP333318 clip bracket against the TP333313 frame on the opposite side of window frame, secure with hardware removed in disassembly operation. For ease of installation, form edges of screen over flanges of screen frame before installation.

CONDUIT PLATE

3.05 Before installing conduit plate, determine number of 3/4 inch conduits to be used for signal and clock cables. Remove the number of knockouts necessary. If cables have connectors attached, insert the cables and conduit through the appropriate openings before installing the plate (Figure 3).

3.06 Position TP333315 conduit plate on underside of cable opening in the lower rear section of the cabinet. Place flanged side of plate on top of front flange of cable opening, raise rear end of conduit plate to bottom side of cable opening. Place TP333316 bracket support on inside of cabinet above rear end of conduit plate. Secure plate and bracket together with five TP151723 screws and TP3639 lockwashers screwed into conduit plate (Figure 4).

3.07 Connect ground strap between conduit plate and inner frame of cabinet. Attach one end of strap to 6-40 tap hole on the left side of conduit plate with hardware provided. Connect other end of strap to the first hole from the bottom of the inner frame at rear vertical support with hardware furnished, tighten securely. (Place star lockwashers between terminals and mounting surfaces.)

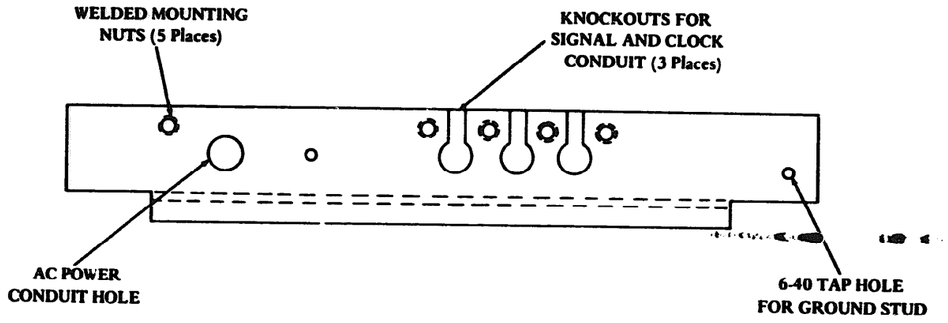


Figure 3 - Conduit Plate

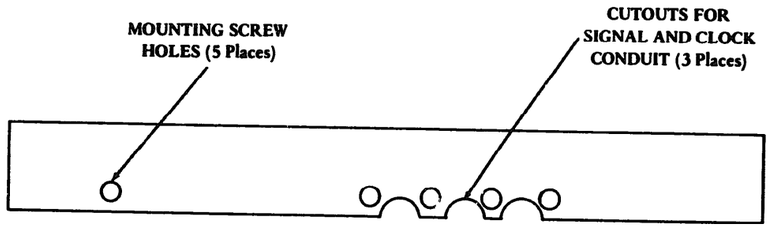


Figure 4 - Bracket Support Plate

JUNCTION BOX

3.08 Place TP333343 junction box assembly over conduit plate and align 3/4 inch hole in box with 3/4 inch hole in conduit plate, on the inside of cabinet (refer to Figure 5). Install 3/4 inch conduit connector into the 3/4 inch opening of conduit plate and junction box. Place connector locknut over thread of connector inside junction box and tighten securely (refer to Figure 6).

3.09 Make TP333336 cable connections at main power terminal board A as shown below:

POWER TERMINAL BOARD A	CAPACITOR CONNECTION	TP333336 CABLE WIRE
A-1	(1)	White
A-2	(2)	Black
A-3	(3)	White
A-4	(4)	Black
A-5	(5)	White
A-6	(6)	Black
Frame Ground	Ground Stud	Green

EXTERNAL ELECTRICAL CONNECTIONS

3.10 To maintain rfi capabilities all electrical inputs and outputs to the cabinet should be routed through solid steel conduit (EMT). Feed ac wires into junction box and make connections to terminal board as shown in 7730WD. After wiring is completed, install cover on junction box using the hardware provided.

INPUT SIGNAL AND CLOCK CONNECTIONS

3.11 Signal and clock cables with connectors installed may be routed through the conduit plate by removing the appropriate number of keyhole knockouts provided for 3/4 inch conduits. After conduit is installed, route the cables inside the cabinet and make wire connections according to information found in Section 592-851-230TC.

MAGNET DRIVER CARDS

Text Remove one of the TP303672 or TP303730 magnet driver cards located at ZC121-123 and ZC319-324, at the rear of module C. Compare the card with

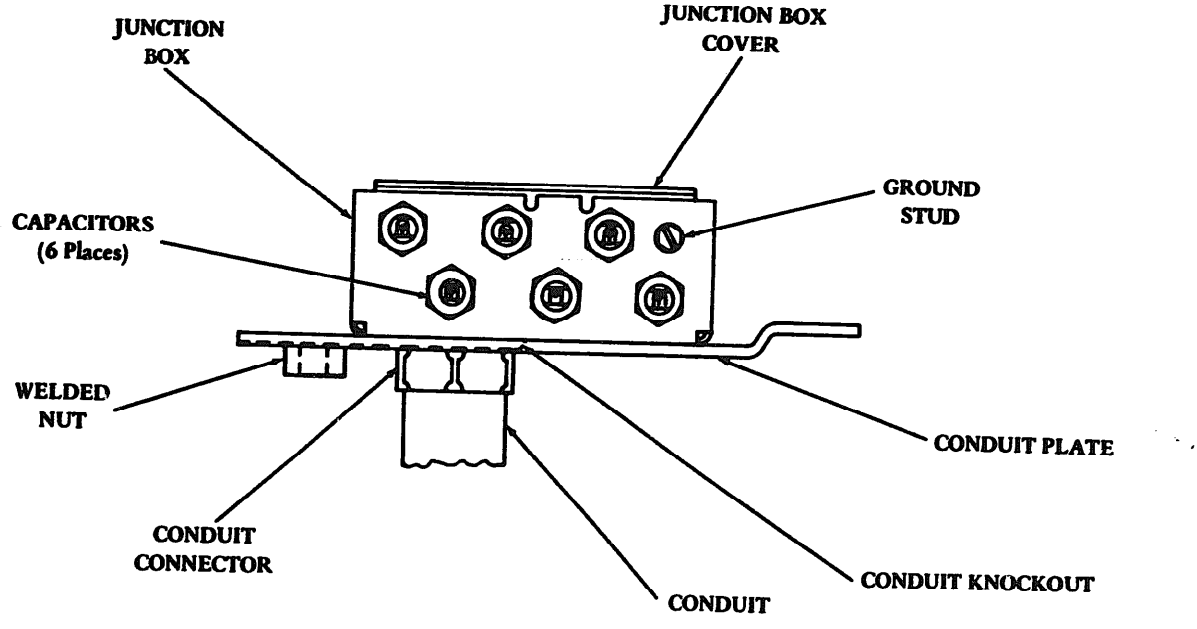


Figure 5 - Junction Box and Conduit Plate Connection

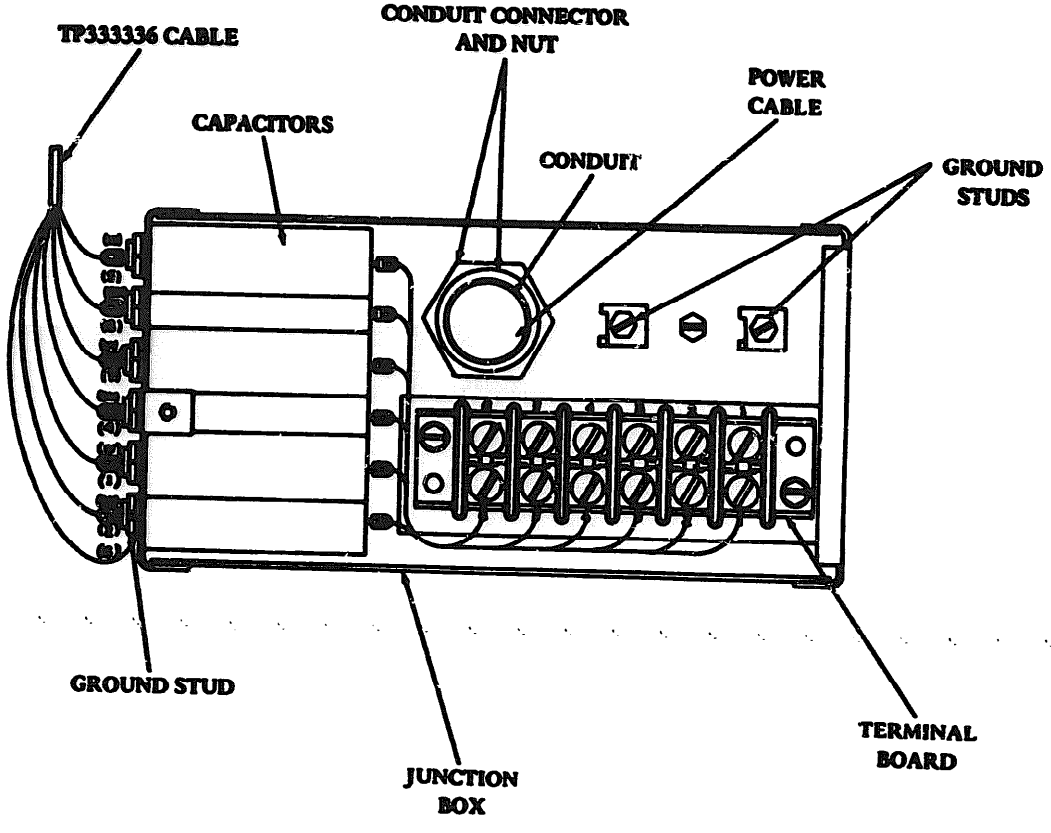


Figure 6 - Junction Box Components

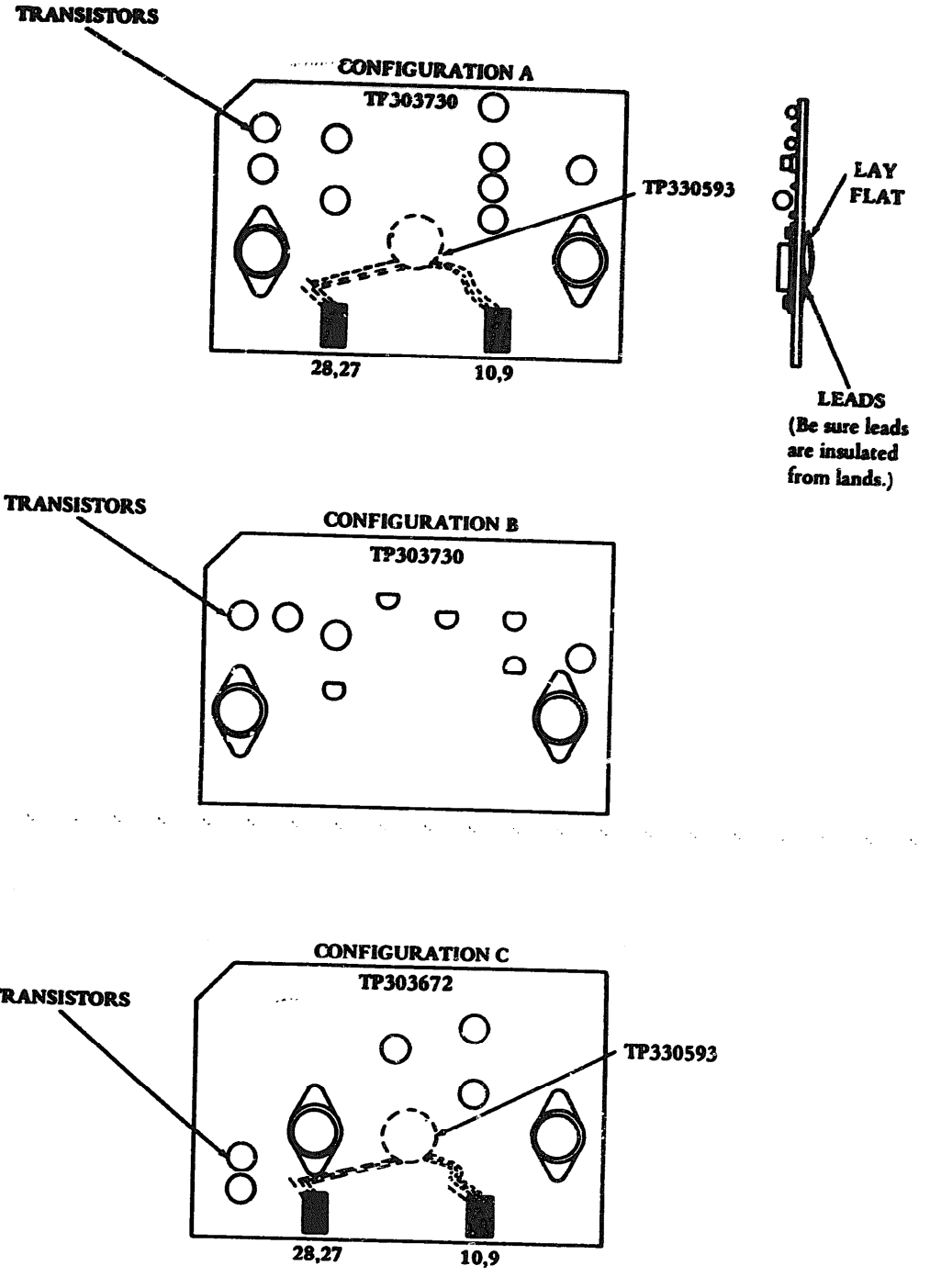


Figure 7 - Magnetic Driver Card Configurations

configurations shown in Figure 7. If the card conforms to configuration B nothing need be done to the card, replace it in the module.

3.13 If the card conforms to configuration A or C, remove nine cards from the locations given (3.12), from each module C. Place plastic tubing over each TP330593 capacitor lead, solder one lead to terminals 9 and 10 and the other lead to terminals 27 and 28 of the card (Figure 7).

4. CHECKOUT PROCEDURE

GENERAL

4.01 Checkout procedures should be made after installation is completed. These checkout tests should also be performed after routine servicing or correcting extensive troubles in the set. A physical inspection should precede all rfi tests to insure that all ground straps and shields are properly installed and all connections properly tightened.

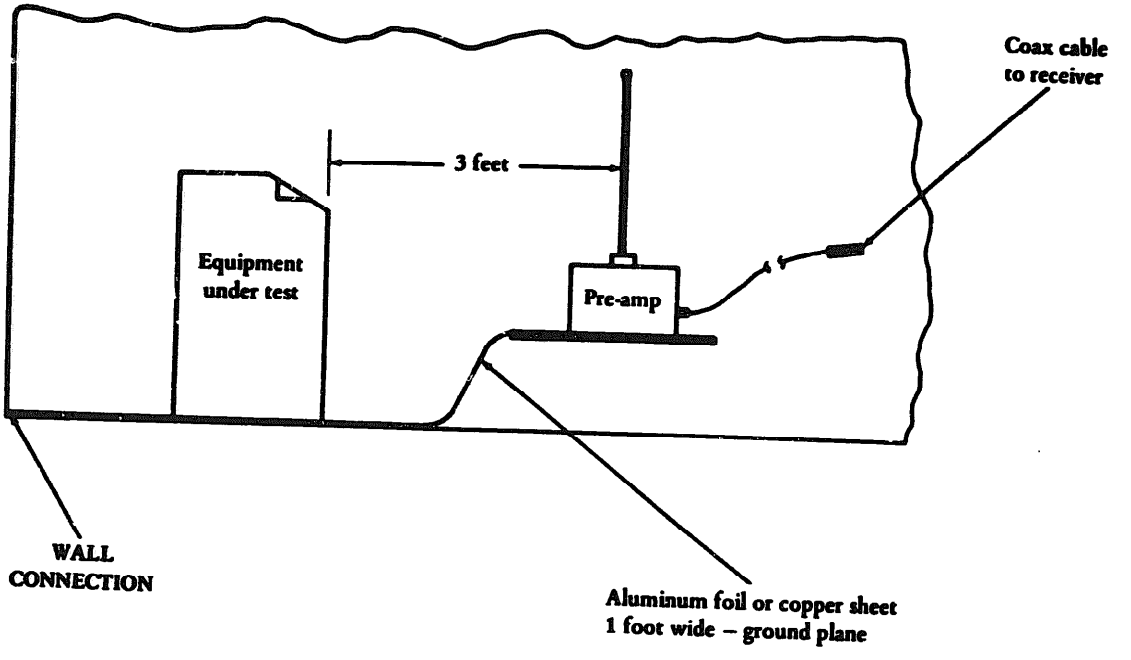


Figure 8- Vertical Rod Antenna Test Setup

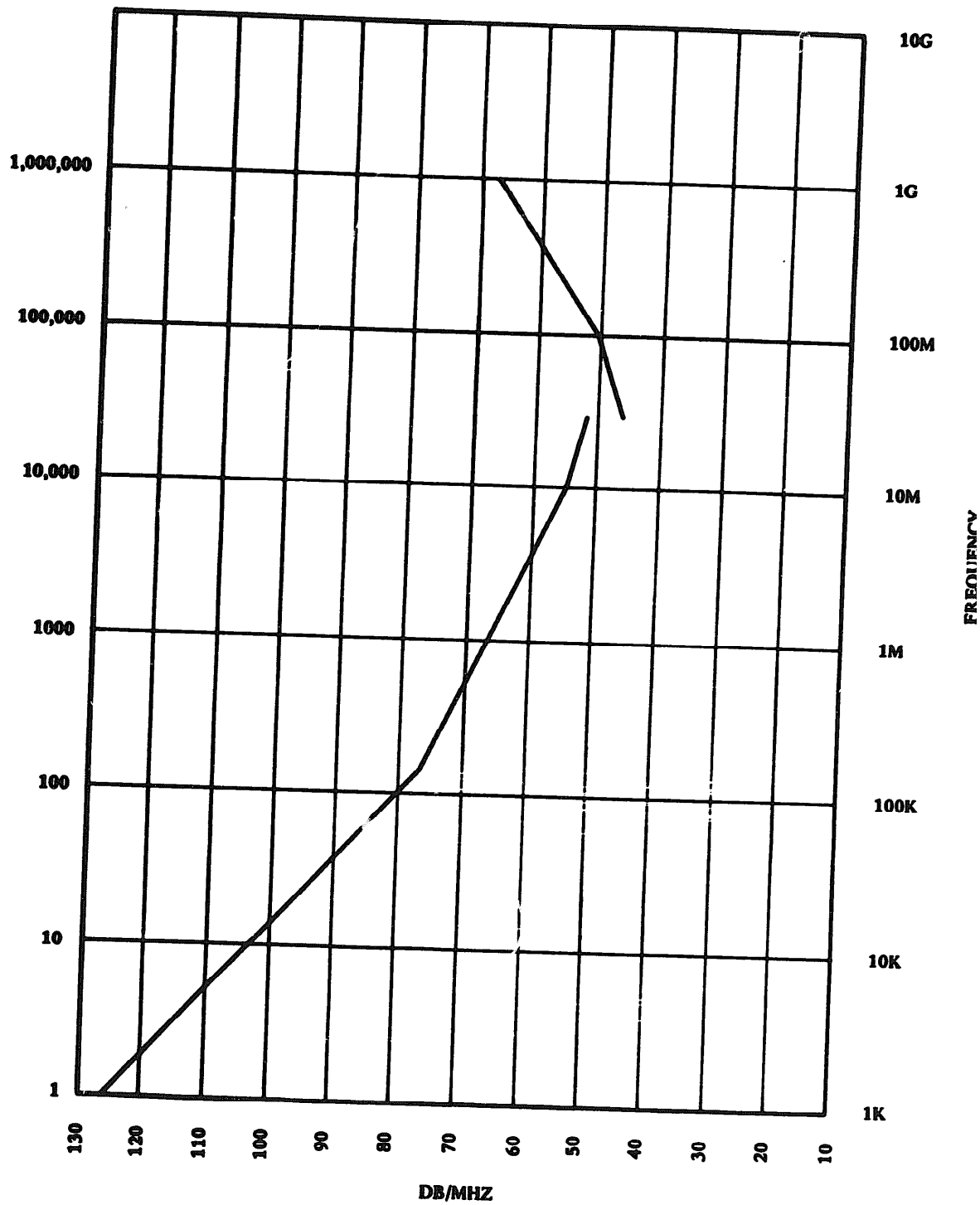


Figure 9 - Electrical Field Limits

4.02 Sets with rfi components installed should be tested by setting up a functional system consisting of a receiver, master, and supplementary transmitter; or a master transmitter and receiver in a rfi shielded room. Primary power and interconnecting signal leads should be enclosed in separate 3/4 inch electrical metal tubing conduit. An rf quiet clock should be used for timing and must be in a shielded enclosure.

4.03 All mechanical adjustments and electrical continuity tests should be completed before rfi testing. To insure good shield connections, shield continuity tests should be made. The screen room should be free of all loose metallic parts, tools, wires, and nonessential test equipment.

4.04

RFI TEST

4.05 Make preliminary tests to assure proper operation of the system. Disconnect tape feed motors before making rfi tests, to prevent triac noise. Test limits apply to data related signals only.

4.06 Place the cabinets in a row facing the antenna approximately 1 foot apart. Center the antenna 3 feet in front of the cabinet group. When making test with a vertical rod antenna setup, mount the cabinets and antenna on a common ground plane (aluminum foil or copper sheet 1 foot wide and appropriate length), connected to the shielded room walls (Figure 8). Electrical field limits are shown in Figure 9.

SUPPLEMENTARY HIGH SPEED TAPE SENDER WITH RADIO FREQUENCY INTERFERENCE (RFI) SUPPRESSION FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

WIRING DIAGRAMS

1. GENERAL

1.01 This section contains wiring diagrams for the supplementary high speed tape sender with radio frequency interference (RFI) suppression, used in the multiple address processing system.

1.02 The following information can be found on each wiring diagram: Physical component layout, wiring symbols, terminal numbers and locations, and wire network lists. Notes are included on wiring diagrams to explain the symbols used and point out special conditions.

1.03 A complete listing of the schematic and actual wiring diagrams is presented in the wiring diagram index found in this section. The location of each diagram, which is attached as part of this publication, is indicated by its position in the index. The index lists the equipment title, wiring diagram number, type of diagram (A for actual, S for schematic), and wiring diagram package number. Wiring diagrams are listed in numerical order.

2. WIRING DIAGRAM INDEX

TITLE	WIRING DIAGRAM NUMBER	TYPE	WIRING DIAGRAM PACKAGE NUMBER
Supplementary Cabinet	7741WD	A	0235
VS268 Transmitter Set	7742WD	S	0235
Module E	7756WD	A	0235
310913 Control Panel	7757WD	A	0235

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SHEET INDEX	A1	1														
NOTES	A2	1														
NOTES	A3	1														
NOTES	A4	1														
NOTES	A5	1														
NETWORK LISTING-INDEX (B SECTION)	ALL	1														
NETWORK LISTING (C SECTION)	ALL	1														

NOTES

1. Wire is part of 336903 Cable Assembly and must be connected to the indicated "From" Terminal.
2. Wire is part of 336903 Cable Assembly and must be connected to indicated "To" Terminal.
3. Wire is part of 336903 Cable Assembly and must be connected to indicated "From" and "To" Terminals.
4. Wire is part of 336903 Cable Assembly and must be connected to indicated "From" and "To" Terminals with 72597RM Terminal connected on the "To" end of the wire.
5. Wire must be connected to indicated "From" and "To" terminals with terminals (TP121533) on both ends of wire.
6. Wire must be connected to indicated "To" Terminal with 72597RM on "To" end of wire.
8. Wire is #14 GA. White (RM31116) or #14 GA. Black (RM31080) as indicated in "color-ga."
9. Wire is 21.5 inches long. Connect to indicated "From" and "To" terminals.
10. Wire is part of twisted pair 31161RM, and must be connected to indicated "From" and "To" Terminal with 121533 Terminal on "To" end of wire.
11. Wire must be connected to indicated "From" and "To" Terminals.
12. Wire is 20 AWG bare wire and must be connected to indicated "From" and "To" Terminals.
13. Wire must be connected to indicated "From" and "To" Terminal. The "To" Terminal being one of the mounting screws for FLF101. The wire should be 21.5 inches long.
14. CF101 and CF102 are each 2 mf capacitors No. 193053. Connect to the indicated "From" and "To" terminals with appropriate tubing on each lead.

7741 WD-A2

REVISIONS

ISSUE	DATE	AUTH. NO.
1	6-5-70	20846-R

WIRING DIAGRAM FOR SUPPLEMENTARY TRANSMITTER CABINET AC395

APPROVALS

D AND R	E OF M

SHUNTER	61,761S
PROD. NO.	7741WD
DATE:	1-05-70
P.D. FILE NO.	38-A2765AA
DRAWN. DO	CHKD.
ENGD. RGR	APPD.

TELETYPE CORPORATION

7741 WD-A2

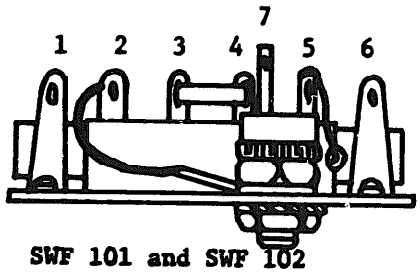
NOTES

7741 WD-A3

REVISIONS

ISSUE	DATE	AUTH. NO.
1	6-8-70	20846-R

15. TERMINAL DESIGNATIONS



310952

SWF 101 and SWF 102

16. Use appropriate tubing on all leads of XKF101.

17. Notes 4, 7, and 9 make up the cabinet wiring.
Notes 5, 6, 8, 10, 11, 12 and 14 make up the surface wiring for the 336916 ESU Panel Assembly.
Notes 1, 2, and 3 are for wiring the 336903 Cable Assembly to the 336916 ESU Panel Assembly.

18. Wire is part of 336903 Cable Assembly and must be connected to indicated "From" and "To" Terminals. The "To" Terminal is one of the mounting screws for TB1.

19. POWER NETWORKS

The following list indicates a terminal common to a particular voltage. The index will provide the individual network number.

VOLTAGE	TERMINAL
115V AC	TBF101 4
115V AC RTN	TBF101 3
Frame	TBF101 1
+6V	JF101 23
-6V	JF101 21
Circuit Common	JF101 37
-12V	JF101 47
Lamp Common	JF101 40

WIRING DIAGRAM FOR SUPPLEMENTARY TRANSMITTER CABINET AC395

APPROVALS

D AND R	E OF M
LBM	

S-NUMBER 61,761S

PROD. NO. 7741WD

DATE: 1-05-70

P.D. FILE NO. 38-A2/65AA

DRAWN. DQ | CHKD.

ENGR. RGS | APPD.

TELETYPE CORPORATION

7741 WD-A3

ST-151401

NOTES

7741 WD-A4

REVISIONS

ISSUE	DATE	AUTH. NO.
→	6-5-70	20846-R

20. This WD consists of three sections:

Section A	Notes and Sheet Index
Section B	Network Listing - Index
Section C	Network Listing

NETWORK LISTING

21. The index lists pins in alpha-numerical order and is a cross reference to the number of the network in which they appear.

22. NETWORK LIST

The Network List is a list of connector pins that are connected together in a common electrical circuit. It lists the pins in from-to-to order. At branching points the first pin of the branch is indented. A second indentation indicates a branch within the first branch. Three indents indicate a third sub branch. If further sub branches are encountered, an indent number is used instead of further indenting.

At a branching point the branching pin is connected to the pin listed on the next line below as well as to the pin at the end of the column of dots extending below the branching pin. If no pins are listed directly below or to the right, the branch ends. There is no direct connection between a pin and one listed below and in a column to its left.

The asterisk in front of the indent number identifies the first pin of a new sub branch.

WIRING DIAGRAM FOR SUPPLEMENTARY TRANSMITTER CABINET AC395

APPROVALS

D AND R	E OF M
LKM	vL

S NUMBER 61.761S

PROD. NO. 7741WD

DATE: 1-05-70

P.D. FILE NO. 38-A2/65AA

DRAWN. DQ	CHKD. MWB
ENGD. RGS	APPD. RMR

TELETYPE CORPORATION

7741 WD-A4

ST-1014021

7741 WD-A5

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	6-5-70	20846-R

SAMPLE NETWORK (Arrows Show Connections)

Net		Component	Pin
0143		JD 4	G 6
0143		XZD314	21
0143		XZD313	20
0143		XZD313	6
0143		XZD312	6
0143		XZD311	6
0143		XZD313	23
0143		XZD313	25
0143		XZD313	31
0143	**04	XZD313	33
0143	04	XZD312	33
0143		XZD312	31
0143		XZD311	31
0143		XZD312	25
0143		XZD311	25
0143		XZD312	23
0143		XZD311	23
0143		XZD312	20
0143		XZD311	20
0144		JD 4	G 7
0144		XZD308	18
0144		XZD309	18
0144		XZD310	18
0144		XZD310	28
0144		XZD313	8
0144		XZD314	31
0144		XZD319	29
0144		XZD328	31
0144		XZD309	28
0144		XZD308	28
0144		XZD310	4
0144		XZD309	4

WIRING DIAGRAM FOR SUPPLEMENTARY TRANSMITTER CABINET AC395

APPROVALS

D and R	E of M
(signature)	(signature)

S-NUMBER 61.761S

PROD. NO. 7741WD

DATE: 1-05-70

RD. FILE NO. 38-A2/65AA

DRAWN DO — CHKD. (signature)

ENGD. RGS — APPD. (signature)

TELETYPE CORPORATION

7741 WD-A5

TITLE
CABINET WIRING OF SUPPLEMENTARY TRANSMITTER 336916

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
7741	1	VS268	1 2 70	B 1	2

COMPONENT	PIN	NET
CBF101	LIN	0075
CBF101	LOA	0074
CBF102	LIN	0079
CBF102	LOA	0078
CBF103	1	0077
CBF103	2	0079
CF101	1	0033
CF101	2	0020
CF102	1	0033
CF102	2	0021
FRAME	F	0023
J		0049
JF101	1	0001
JF101	2	0002
JF101	3	0003
JF101	4	0004
JF101	5	0005
JF101	6	0006
JF101	7	0007
JF101	8	0008
JF101	9	0009
JF101	10	0010
JF101	11	0011
JF101	12	0012
JF101	13	0013
JF101	14	0014
JF101	15	0015
JF101	16	0016
JF101	17	0017
JF101	18	0018
JF101	20	0019
JF101	21	0020
JF101	23	0021
JF101	26	0022
JF101	27	0023
JF101	28	0024
JF101	29	0025
JF101	30	0026
JF101	31	0027
JF101	32	0028
JF101	33	0029
JF101	34	0030
JF101	35	0031
JF101	36	0032
JF101	37	0033
JF101	40	0034
JF101	46	0035
JF101	47	0036
PE128	A 3	0069
PE128	A 7	0061
PF128	A 8	0001
PE128	A 9	0065
PE128	A10	0068

COMPONENT	PIN	NET
PE128	B 1	0035
PE128	B 2	0033
PE128	B 7	0062
PE128	B 8	0002
PE128	B 9	0066
PE128	B10	0067
PE128	C 1	0070
PE128	C 7	0050
PE128	C 8	0043
PE128	C 9	0005
PE128	C10	0004
PE128	D 1	0022
PE128	D 2	0023
PE128	D 7	0008
PE128	D 8	0057
PE128	D 9	0003
PE128	D10	0006
PE128	E 1	0036
PE128	E 3	0071
PE128	E 5	0071
PE128	E 7	0009
PE128	E 8	0058
PE128	E10	0072
PE128	F 7	0010
PE128	F 8	0007
PE128	F 9	0060
PE128	F10	0059
PE128	G 7	0053
PE128	G 8	0054
PE128	G 9	0055
PE128	G10	0056
PE128	H 4	0048
PE128	H 5	0071
PE128	H 6	0073
PE128	H 7	0071
PE128	H 8	0052
PE128	H 9	0064
PE128	H10	0063
PE228	1	0074
PE228	2	0023
PE228	3	0040
PF102	1	0025
PF102	2	0026
PF102	3	0027
PF102	4	0028
PF102	5	0029
PF102	6	0030
PF102	7	0031
PF102	8	0032
PF102	9	0024
PF102	10	0033
PF102	11	0037
PF102	12	0038

COMPONENT	PIN	NET
PF102	14	0039
PF102	17	0040
PF102	20	0041
PF102	21	0041
PF102	25	0042
PF102	26	0043
PF102	27	0042
PF102	32	0023
PF102	34	0011
PF102	35	0012
PF102	36	0013
PF102	37	0014
PF102	38	0015
PF102	39	0016
PF102	40	0017
PF102	41	0018
PF102	43	0033
PF102	44	0044
PF102	45	0045
PF102	47	0046
PF102	50	0047
PF103	1	0048
PF103	2	0041
PF103	3	0049
PF103	4	0041
PF103	5	0050
PF103	7	0051
PF103	8	0041
PF103	9	0034
PF103	10	0034
PF103	11	0034
PF103	12	0034
PF103	13	0034
PF103	14	0034
PF103	15	0034
PF103	16	0023
PF103	17	0033
PF103	18	0052
PF103	19	0053
PF103	20	0054
PF103	21	0055
PF103	22	0056
PF103	23	0019
PF103	24	0057
PF103	25	0058
PF103	26	0059
PF103	27	0060
PF103	28	0061
PF103	29	0062
PF103	30	0063
PF103	31	0064
PF103	32	0065
PF103	33	0066

NETWORK LISTING (TABULAR WIRING DIAGRAM) - INDEX

TITLE
CABINET WIRING OF SUPPLEMENTARY TRANSMITTER 336916

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
7741	1	VS268	1 2 70	B2	2

COMPONENT	PIN	NET
PF103	34	0034
PF103	35	0067
PF103	36	0068
PF104	1	0039
PF104	2	0046
PF104	3	0047
PF104	4	0076
SWF101	2	0078
SWF101	3	0050
SWF101	4	0073
SWF101	7	0047
SWF102	1	0040
SWF102	2	0074
SWF102	3	0051
SWF102	4	0048
SWF102	6	0040
SWF102	7	0079
TB 1	F	0023
TB 1	1	0077
TB 1	2	0040
TB 1	3	0042
TB 1	4	0033
TB 1	6	0072
TB 1	7	0037
TB 1	8	0045
TB 1	9	0038
TB 1	10	0044
TB 2	1	0023
TB 2	2	0076
TB 2	3	0047
TB 2	4	0040
TBF101	1	0023
TBF101	2	0074
TBF101	3	0040
TBF101	4	0075
TBF102	1	0073
TBF102	2	0023
TBF102	3	0023
TBF102	4	0033
TBF102	5	0034
TBF102	6	0034
TBF102	7	0041
TBF102	8	0071
TBF103	1	0021
TBF103	2	0020
TBF104	G	0023
TBF104	W	0040
TBF104	BK	0075
XKF101	1	0020
XKF101	2	0078
XKF101	3	0069
XKF101	6	0021
XKF101	7	0070
XKF101	9	0073
XKF101	10	0040
XKF101	11	0048

OF PINS - 0215

END OF LISTING

COMPONENT	PIN	NET

TITLE: CABINET WIRING OF SUPPLEMENTARY TRANSMITTER 336916

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
7741	1	VS268	1 2 70	C 1 OF 3

NET	COMPONENT	PIN
0001	JF101	1
0001	PE128	A 8
0002	JF101	2
0002	PE128	B 8
0003	JF101	3
0003	PE128	D 9
0004	JF101	4
0004	PE128	C10
0005	JF101	5
0005	PE128	C 9
0006	JF101	6
0006	PE128	D10
0007	JF101	7
0007	PE128	F 8
0008	JF101	8
0008	PE128	D 7
0009	JF101	9
0009	PE128	E 7
0010	JF101	10
0010	PE128	F 7
0011	JF101	11
0011	PF102	34
0012	JF101	12
0012	PF102	35
0013	JF101	13
0013	PF102	36
0014	JF101	14
0014	PF102	37
0015	JF101	15
0015	PF102	38
0016	JF101	16
0016	PF102	39
0017	JF101	17
0017	PF102	40
0018	JF101	18
0018	PF102	41

NET	COMPONENT	PIN
0019	JF101	20
0019	PF103	23
0020	JF101	21
0020	XKF101	1
0020	TBF103	2
0020	CF101	2
0021	JF101	23
0021	XKF101	6
0021	TBF103	1
0021	CF102	2
0022	JF101	26
0022	PE128	D 1
0023	JF101	27
0023	TBF102	3
0023	• • • PE228	2
0023	• • TBF101	1
0023	• • TBF104	G
0023	• TBF102	2
0023	**05	PF103 16
0023	• • • • TB 2	1
0023	• • • FRAME	F
0023	• • TB 1	F
0023	• PF102	32
0023	PE128	D 2
0024	JF101	28
0024	PF102	9
0025	JF101	29
0025	PF102	1
0026	JF101	30
0026	PF102	2
0027	JF101	31
0027	PF102	3
0028	JF101	32
0028	PF102	4
0029	JF101	33
0029	PF102	5
0030	JF101	34
0030	PF102	6
0031	JF101	35
0031	PF102	7

NETWORK LISTING (TABULAR WIRING DIAGRAM

TITLE
CABINET WIRING OF SUPPLEMENTARY TRANSMITTER 336916

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
7741	1	VS268	1 2 70	C 3 OF 3

NET	COMPONENT	PIN
0056	PF103	22
0056	PE128	G10
0057	PF103	24
0057	PE128	D 8
0058	PF103	25
0058	PE128	E 8
0059	PF103	26
0059	PE128	F10
0060	PF103	27
0060	PE128	F 9
0061	PF103	28
0061	PE128	A 7
0062	PF103	29
0062	PE128	B 7
0063	PF103	30
0063	PE128	H10
0064	PF103	31
0064	PE128	H 9
0065	PF103	32
0065	PE128	A 9
0066	PF103	33
0066	PE128	B 9
0067	PF103	35
0067	PE128	B10
0068	PF103	36
0068	PE128	A10
0069	PE128	A 3
0069	XKF101	3
0070	PE128	C 1
0070	XKF101	7
0071	PE128	E 3
0071	TBF102	8
0071	• • PE128	H 5
0071	• PE128	H 7
0071	PF128	E 5
0072	PE128	E10
0072	TB 1	6

NET	COMPONENT	PIN
0073	PE128	H 6
0073	TBF102	1
0073	• SWF101	4
0073	XKF101	9
0074	PE228	1
0074	SWF102	2
0074	TBF101	2
0074	CBF101	LCA
0075	CBF101	LIN
0075	TBF101	4
0075	TBF104	BK
0076	TB 2	2
0076	PF104	4
0077	TB 1	1
0077	CBF103	1
0078	XKF101	2
0078	SWF101	2
0078	CBF102	LCA
0079	SWF102	7
0079	CBF102	LIN
0079	CBF103	2

NUMBER OF WIRES - 0136

END OF LISTING

NO.	NOTES	SUPPORTING INFORMATION	
		CATEGORY	NO.

CONTENTS

TC 482 (1-66)

SEE R&D ROUTINE #5
FOR USE OF THIS FORM

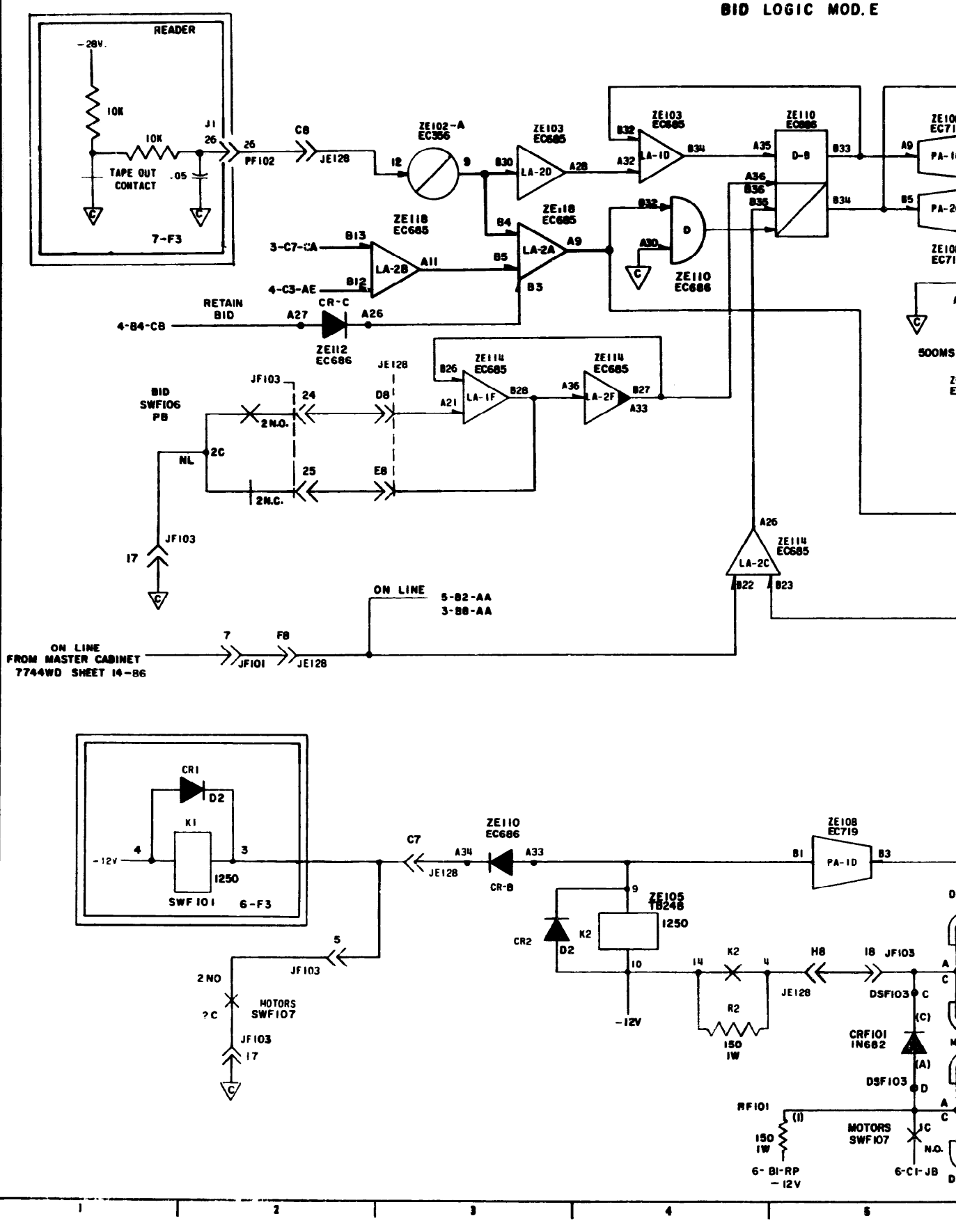
NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ( ) ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
3	ALL RESISTORS 1/2 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
4.	ALL CAPACITANCE VALUES IN MICROFARADS.
5.	COMPONENTS ENCLOSED IN SOLID DOUBLE LINES ARE PRESENTED FOR REFERENCE ONLY A COMPLETE SCHEMATIC OF THESE COMPONENTS IS AVAILABLE AT THE WD OR AREA INDICATED.
6.	DASHED - - - - SINGLE LINE ENCLOSING COMPONENTS INDICATES ONE CARD OR ASSEMBLY LOCATION FOR ALL THE ENCLOSED COMPONENTS.
7.	THE FOLLOWING CIRCUIT CARDS ARE LOCATED IN THE FOLLOWING POSITIONS MODULE-E ZE102 172356 ZE103 303685 ZE105 149248 ZE106 303687 ZE108 303719 ZE110 303686 ZE112 " ZE114 303685 ZE116 " ZE118 " ZE202 303117 ZE426 149242 ZE205 149248
8.	SPARE CIRCUITS AVAILABLE ZE426 K4 ZE205 K1 ZE105 K1, K3 ZE106 DYA, DYB, PAE, PAF ZE110 CR-C, CR-D, CR-F CR-F, ZE112 D-D, D-E, D-F, CR-B, CR-D, CR-E, ZE118 LA-2C, LA-1C, LA-1D, LA-2D, LA-1F, LA-2F ZE102 B, C, D
9.	THE RESISTANCE OF ALL RELAY COILS IS IN OHMS.
10.	REFER TO SPECIFICATION 61761 S OR TELETYPE BULLETIN 592-851-730 FOR TIMING CIRCUIT ADJUSTMENT.
11.	>— INDICATES FEMALE AND —> INDICATES MALE TERMINAL ON CONNECTOR INDICATED.
12.	ALL REVISION INFORMATION IS REFLECTED ON THE ISSUE CONTROL RECORD.
13.	INDUCTANCE VALUE IN MICROHENRIES
14.	FOR ACTUAL WIRING DIAGRAMS REFER TO: MODULE E 7756 WD SUPPLEMENTARY CABINET 7741 WD SUPPLEMENTARY CONTROL PANEL 7757 WD TAPE TRANSPORT 7712 WD DX READER 6532 WD DX DRIVER 6436 WD.
15.	SWITCHES ARE GANGED TOGETHER.
16.	-12VOLTS IS AT THIS POINT WHEN THE MASTER TRANSMITTER POWER IS ON
17	CROSS REFERENCE LEGEND: 5 - B2 A LEAD DESIGNATION WHEN NEEDED CO-ORDINATE LOCATION SHEET NUMBER
18	INDICATES LAMP COMMON INDICATES CIRCUIT COMMON THESE ARE CONNECTED TOGETHER IN THE 310860 POWER SUPPLY (7744 WD SHEET 6)
19.	ONLY THE CONNECTORS ARE INDICATED WHEN THE PLUG HAS THE SAME DESIGNATION EXCEPT THE J___ IS REPLACED WITH A P___. THE PIN NUMBERS REMAIN THE SAME ON BOTH CONNECTORS.

NO.	NOTES
20.	THE HALF ARROWS (⇌) TO A DIGITAL POTTED MODULE CIRCUIT INDICATE THAT CIRCUIT IS SENSITIVE TO A VOLTAGE OR CURRENT LEVEL AT THAT INPUT. THE FULL ARROW (—►) INPUT TO A DIGITAL POTTED MODULE CIRCUIT INDICATES THAT CIRCUIT IS SENSITIVE TO A VOLTAGE CHANGE OR A PULSE AT THAT INPUT.
21.	LAMP COLORS ARE CLEAR UNLESS OTHERWISE INDICATED.
22.	WHEN 15 PIN CARDS ARE USED, TWO ARE PLACED IN ONE 36 PIN CARD CONNECTOR. THE ACTUAL WD INDICATES ONLY ONE LOCATION NUMBER FOR THE ENTIRE 36 PIN CONNECTOR. THIS SCHEMATIC WD DESIGNATES A POSITION FOR EACH CARD EG: ZE103 ON ACTUAL WOULD BE ZE103 AND ZE203 ON SCHEMATIC DEPENDING ON LOCATION. SEE MODULE CO-ORDINATE SYSTEM.
23	CERTAIN LOGIC SYMBOLS USED ON THIS WIRING DIAGRAM DO NOT CONFORM TO TELETYPE DESIGN STANDARDS. THE SYMBOLS ARE EXPLAINED ON THE RESPECTIVE CIRCUIT CARD DRAWINGS.
24	ALL SIGNAL AND VOLTAGE LINES TERMINATING AT JF101 IN THE SUPPLEMENTARY TRANSMITTER CABINET, VS268 ARE CONNECTED TO THE MASTER CABINET, VS267 VIA AN INTERCONNECTING CABLE. THESE SIGNAL AND VOLTAGE LINES ENTER THE MASTER CABINET AT ANY ONE OF FIVE CONNECTORS (JG101, JG102, JG103, JG104, OR JG105). THE CONNECTOR USED IS DEPENDENT UPON THE NUMBER OF SUPPLEMENTARY CABINETS BEING USED WITH THE MASTER CABINET.
25	THE FOLLOWING FROM-TO CONNECTIONS ARE SPARE WIRES PROVIDED IN THE CABINET CABLE

FROM	TO
PF102 - 20	TBF102 - 7
PF103 - 2	TBF102 - 7
PF103 - 4	TBF102 - 7
PF103 - 8	TBF102 - 7
PF102 - 21	TBF102 - 7
PF103 - 3	FOLDED BACK AT SWF 102
PE128 - E3	TBF102 - 8
PE128 - H7	TBF102 - 8
PE128 - H5	TBF102 - 8
PE128 - E5	TBF102 - 8

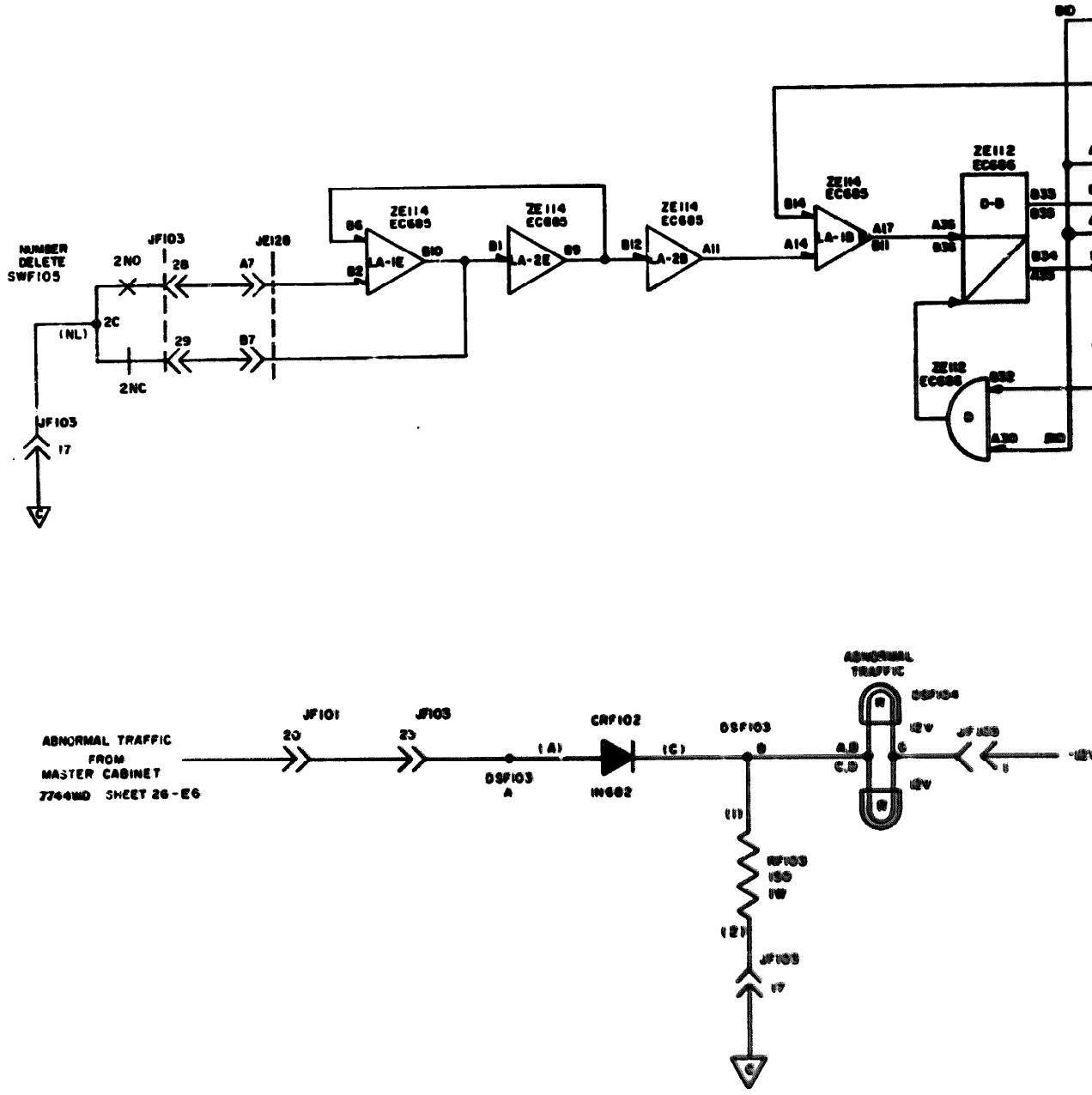
SEE SHEET 1 FOR NOTES.

BID LOGIC MOD. E

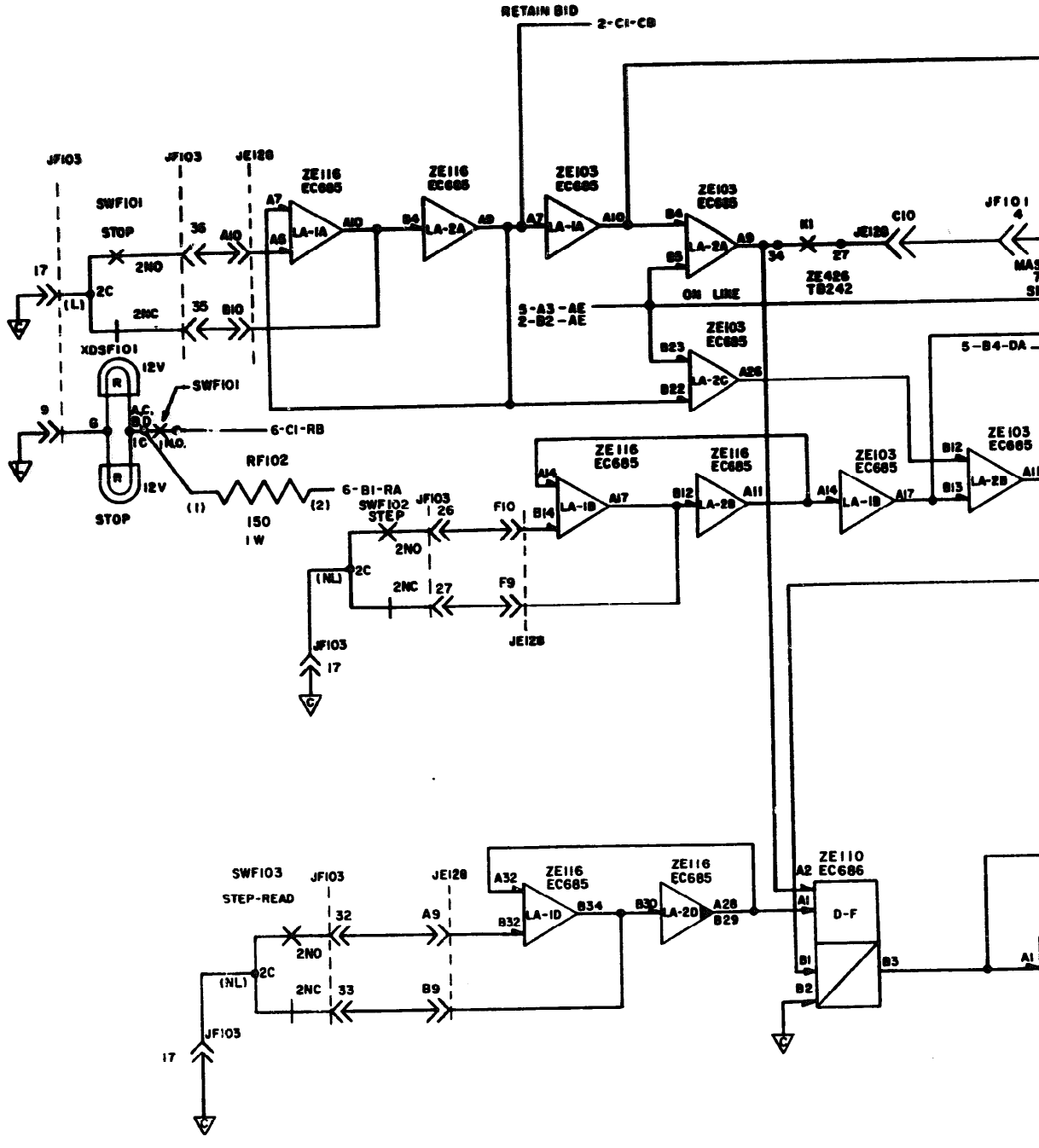


SEE SHEET 1 FOR NOTES

NUMBER DELETE MOD. E

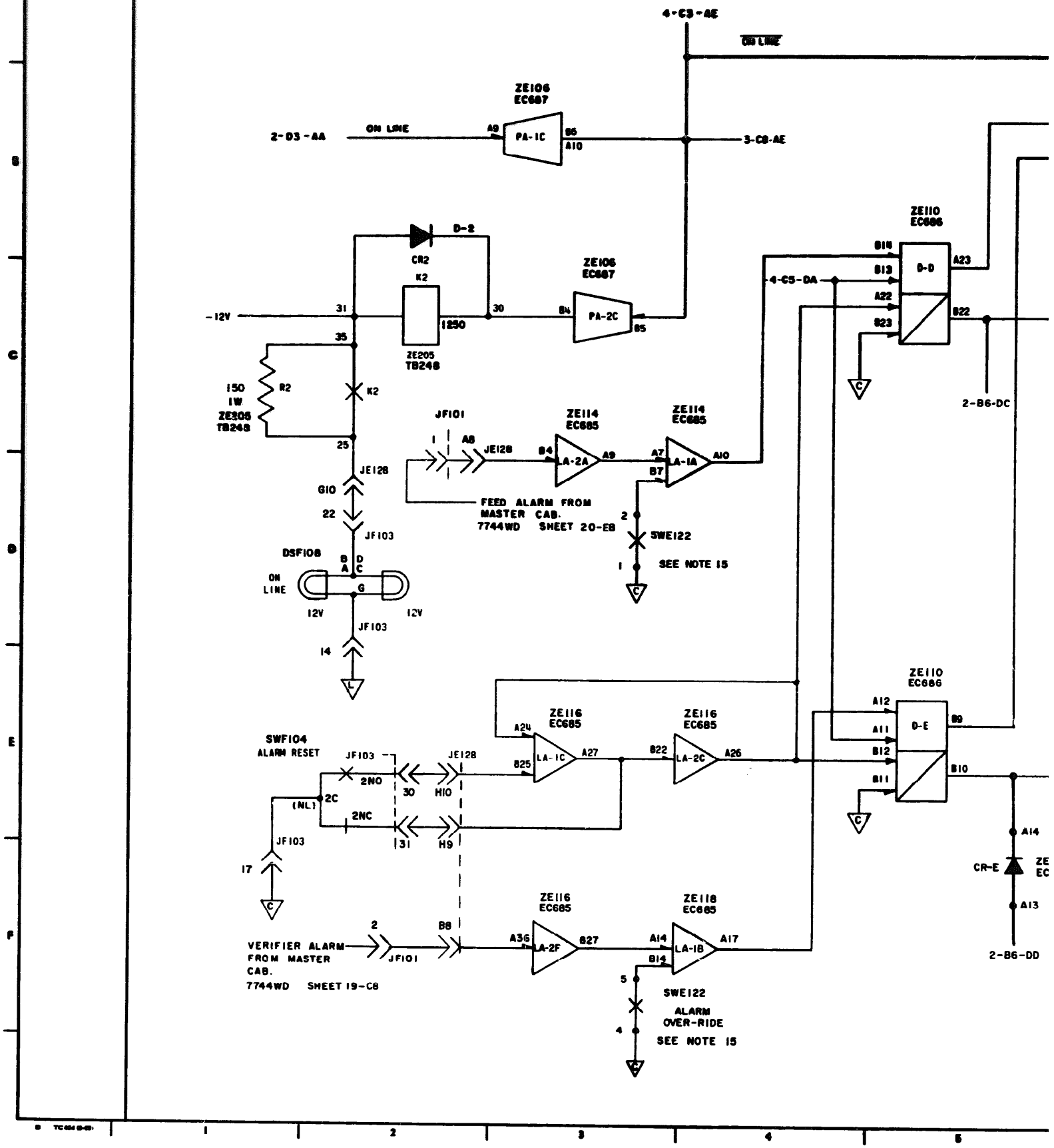


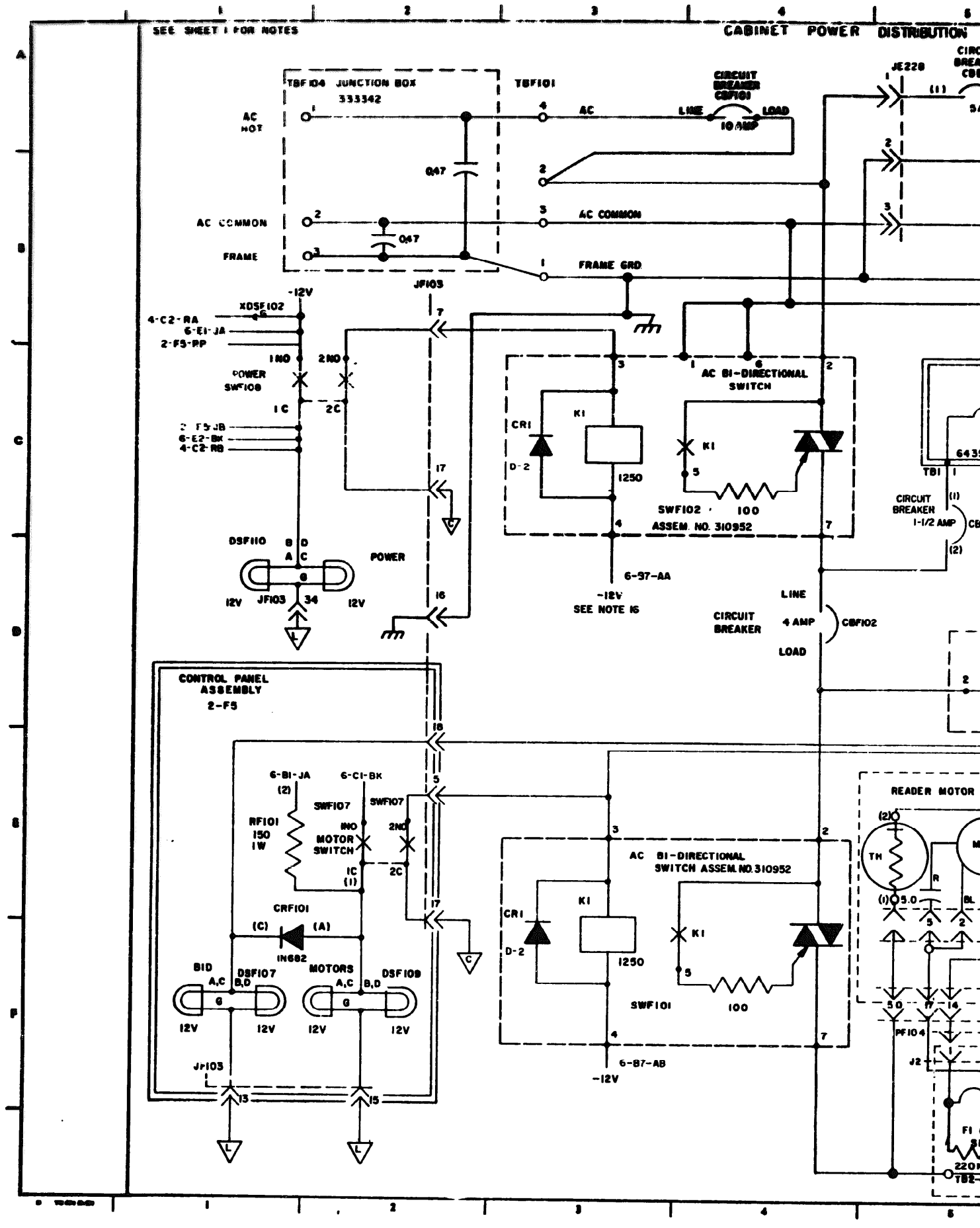
SEE SHEET 1 FOR NOTES



SEE SHEET 1 FOR NOTES.

ALARM LOGIC

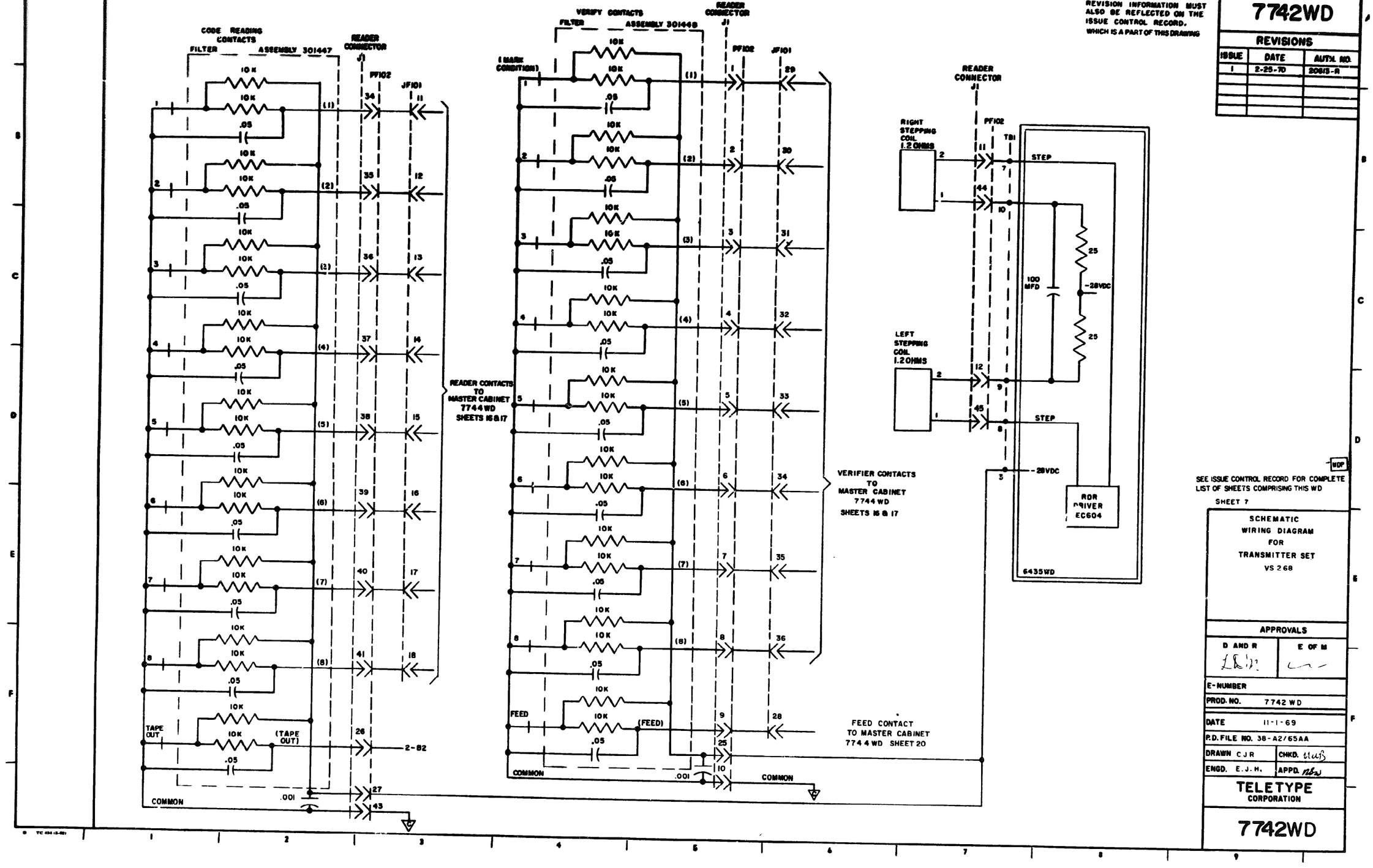



SEE SHEET 1 FOR NOTES
CABINET POWER DISTRIBUTION
TBF104 JUNCTION BOX
333342
TBF101
AC HOT
AC COMMON
FRAME
.047
.047
AC
AC COMMON
FRAME GRD
CIRCUIT BREAKER CBF101
LINE
LOAD
10 AMP
JE228
-12V
XDSF102
4-C2-RA
6-E1-JA
2-F5-PP
1NO
2NO
POWER SWF108
1C
2C
2-F5-JB
6-E2-BK
4-C2-RB
JF103
7
17
16
DSF110
POWER
12V
JF103
34
12V
AC BI-DIRECTIONAL SWITCH
CR1
K1
D-2
1250
SWF102
100
ASSEM. NO. 310952
6-87-AA
-12V
SEE NOTE 16
TB1
CIRCUIT BREAKER
1-1/2 AMP
CB
LINE
CIRCUIT BREAKER
4 AMP
CBF102
LOAD
CONTROL PANEL ASSEMBLY
2-F5
6-B1-JA
6-C1-BK
SWF107
RF101
150
1W
MOTOR SWITCH
IC
2C
CRF101
IN682
BID
DSF107
MOTORS
DSF109
JF103
13
15
AC BI-DIRECTIONAL SWITCH ASSEM. NO. 310952
SWF101
100
6-87-AB
-12V
READER MOTOR
TH
5.0
PF104
J2

SEE SHEET 1 FOR NOTES.

NOTES:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING

7742WD		
REVISIONS		
ISSUE	DATE	AUTH. NO.
1	2-25-70	20815-A



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD

SHEET 7

SCHEMATIC WIRING DIAGRAM FOR TRANSMITTER SET VS 268

APPROVALS	
D AND R	E OF M

E-NUMBER	
PROD. NO.	7742 WD
DATE	11-1-69
P.D. FILE NO.	38-A2/65AA
DRAWN CJR	CHKD.
ENGD. E.J.H.	APPD.

TELETYPE CORPORATION

7742WD

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	SHEET NO.
SHEET INDEX	A1	1																									A1
NOTES	A2	1																									A2
NOTES	A3	1																									A3
NOTES	A4	1																									A4
NETWORK LISTING-INDEX (B SECTION)	ALL	1																									ALL
NETWORK LISTING (C SECTION)	ALL	1																									ALL

SUPPORTING INFORMATION

CATEGORY	NO.
VS268 M.A.P.S. SUPPLEMENTARY TRANSMITTER SET.	WDP0235

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND UPDATED EACH TIME ANY SHEET OF THE DRAWING IS REISSUED OR A NEW SHEET IS ADDED.
3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.

REVISIONS 4 - 1 0 9

ISSUE	DATE	AUTH. NO.
1	6-5-70	20846-R

WIRING DIAGRAM

FOR

MODULE E

336914

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
	RJL	

ENGR. R. G. S.	DSGNR.
DRN. D. Q.	DATE 3-16-70
R & D FILE	38-A2/65AA
S-NUMBER	61.761S

TELETYPE

7756WD A1

TC 639 (3-69)

NOTES

7756 WD-A2

REVISIONS

ISSUE	DATE	AUTH. NO.
2	6-5-70	20546-R

1. This WD consists of three sections:

   Section A — Notes

   Section B — Network Listing - Index

   Section C — Network Listing

2. NETWORK LISTING - INDEX

   The Index lists pins in alpha-numerical order and is a cross reference to the number of the network in which they appear.

3. NETWORK LIST

   The Network List is a list of connector pins that are connected together in a common electrical circuit. It lists the pins in from-to-to order. At branching points the first pin of the branch is indented. A second indentation indicates a branch within the first branch. Three indents indicates a third sub branch. If further sub branches are encountered, an indent number is used instead of further indenting.

   At a branching point the branching pin is connected to the pin listed on the next line below as well as to the pin at the end of the column of dots extending below the branching pin. If no pins are listed directly below or to the right, the branch ends. There is no direct connection between a pin and one listed below and in a column to its left.

   The asterisk in front of the indent number indentifies the first pin of a new sub branch.

4. POWER NETWORKS

   The following list indicates a terminal common to a particular voltage. The index will provide the individual network number.

VOLTAGE	TERMINAL
+6V	JE128 C1
-6V	JE128 A3
Circuit Common	JE128 B2
-12V	JE128 E1

WIRING DIAGRAM FOR MODULE E 336914

APPROVALS

D AND R	E OF M
[illegible]	[illegible]

S-NUMBER	61,761S
PROD. NO.	7756WD
DATE:	1-05-70
P.D. FILE NO.	38-A2765AA
DRAWN. DO	CHKD. [illegible]
ENGD. RGS	APPD. RJR

TELETYPE CORPORATION

7756 WD-A2

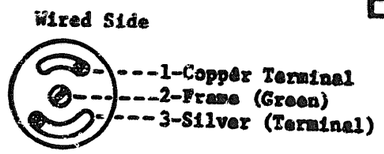
ST-101401

NOTES

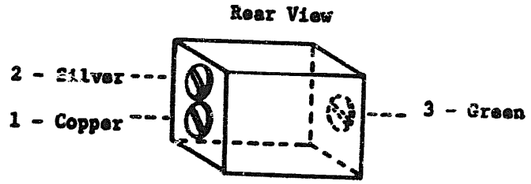
7756WD-A3

REVISIONS		
ISSUE	DATE	AUTH. NO.
[illegible]	5-8-70	20846-R

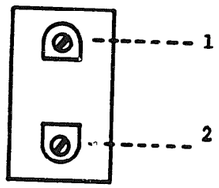
5. A-C Receptacle



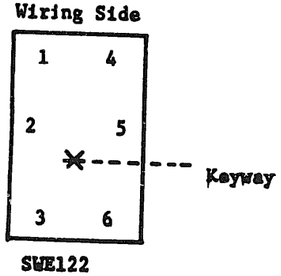
6. Auxiliary outlet on front plate



7. Circuit Breaker



8. Toggle switch terminal locations.



SWE122

WIRING DIAGRAM FOR MODULE E 336914

APPROVALS

D AND R	E OF M
LDM	

S NUMBER 61.7616
PROD. NO. 7756WD

DATE: 1-05-70
RD. FILE NO. 3U-A2765AA
DRAWN DQ CHKD. MWS
ENGR. RCM APPD. RMR

TELETYPE CORPORATION

7756 WD-A3

7756 WD A4

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	6-5-70	20846-R

SAMPLE NETWORK (Arrows Show Connections)

Net	Component	Pin
0143	JD 4	G 6
0143	XZD314	21
0143	XZD313	20
0143	XZD313	6
0143	XZD312	6
0143	XZD311	6
0143	XZD313	23
0143	XZD313	25
0143	XZD313	31
0143	**04 XZD313	33
0143	04 XZD312	33
0143	XZD312	31
0143	XZD311	31
0143	XZD312	25
0143	XZD311	25
0143	XZD312	23
0143	XZD311	23
0143	XZD312	20
0143	XZD311	20
0144	JD 4	G 7
0144	XZD308	18
0144	XZD309	18
0144	XZD310	18
0144	XZD310	28
0144	XZD313	8
0144	XZD314	31
0144	XZD319	29
0144	XZD328	31
0144	XZD309	28
0144	XZD308	28
0144	XZD310	4
0144	XZD309	4

WIRING DIAGRAM FOR MODULE E 336914

APPROVALS	
D AND R	E OF M
LDM	[signature]

S NUMBER 61.761S

PROD. NO. 7756WD

DATE: 1-05-70

RB. FILE NO. 38-A2/65AA

DRAWN DQ	CHKD. [signature]
ENGR. RGS	APPD. [signature]

TELETYPE CORPORATION

7756 WD-A4

NETWORK LISTING (TABULAR WIRING DIAGRAM) - INDEX

TITLE MODULE E WIRING OF SUPPLEMENTARY TRANSMITTER 336914

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE B1 OF 3
7756	1	VS269 #2	1 2 70	

COMPONENT	PIN	NET
CBF 1	1	0104
CBE 1	2	0106
CBE 2	1	0101
CBE 2	2	0103
CBE 3	1	0094
CBE 3	2	0001
CBE 4	1	0093
CBE 4	2	0005
JE 1	1	0106
JE 1	2	0105
JE 1	3	0098
JE128	A 3	0093
JE128	A 7	0074
JE128	A 8	0075
JE128	A 9	0092
JE128	A10	0080
JE128	B 1	0078
JE128	B 2	0002
JE128	B 7	0073
JE128	B 8	0084
JE128	B 9	0091
JE128	B10	0081
JE128	C 1	0094
JE128	C 7	0057
JE128	C 8	0004
JE128	C 9	0095
JE128	C10	0096
JE128	D 1	0097
JE128	D 2	0098
JE128	D 7	0071
JE128	D 8	0070
JE128	D 9	0069
JE128	D10	0100
JE128	E 1	0101
JE128	E 7	0102
JE128	E 8	0072
JE128	E10	0090
JE128	F 7	0079
JE128	F 8	0047
JE128	F 9	0082
JE128	F10	0087
JE128	G 7	0036
JE128	G 8	0042
JE128	G 9	0040
JE128	G10	0043
JE128	H 4	0103
JE128	H 6	0006
JE128	H 8	0038
JE128	H 9	0083
JE128	H10	0088
JE228	1	0104
JE228	2	0098
JE228	3	0105

COMPONENT	PIN	NET
SWE122	1	0002
SWE122	2	0077
SWE122	4	0002
SWE122	5	0106
XZE102	2	0001
XZE102	4	0002
XZE102	9	0003
XZE102	12	0004
XZE102	14	0005
XZE102	15	0006
XZE102	16	0002
XZE102	18	0001
XZE102	20	0005
XZE102	22	0007
XZE102	24	0005
XZE102	26	0006
XZE102	27	0002
XZE102	28	0001
XZE102	29	0008
XZE102	30	0009
XZE102	31	0010
XZE102	32	0011
XZE102	33	0012
XZE102	34	0013
XZE102	35	0014
XZE102	36	0009
XZE103	A 1	0015
XZE103	A 7	0016
XZE103	A 9	0017
XZE103	A10	0018
XZE103	A11	0019
XZE103	A14	0020
XZE103	A16	0002
XZE103	A17	0021
XZE103	A18	0001
XZE103	A20	0005
XZE103	A21	0022
XZE103	A24	0022
XZE103	A26	0023
XZE103	A27	0024
XZE103	A28	0025
XZE103	A32	0025
XZE103	A33	0026
XZE103	A35	0019
XZE103	A36	0027
XZE103	B 1	0028
XZE103	B 4	0018
XZE103	B 5	0029
XZE103	B 6	0030
XZE103	B 9	0031
XZE103	B10	0027
XZE103	B12	0023
XZE103	B13	0021

COMPONENT	PIN	NET
XZE103	B16	0002
XZE103	B17	0027
XZE103	B18	0001
XZE103	B20	0005
XZE103	B21	0024
XZE103	B22	0016
XZE103	B23	0029
XZE103	B25	0032
XZE103	B26	0013
XZE103	B27	0033
XZE103	B28	0026
XZE103	B30	0003
XZE103	B32	0034
XZE103	B34	0035
XZE105	1	0036
XZE105	2	0037
XZE105	4	0038
XZE105	9	0039
XZE105	10	0006
XZE105	11	0006
XZE105	14	0006
XZE105	16	0002
XZE105	18	0001
XZE105	20	0005
XZE105	22	0040
XZE105	23	0041
XZE105	24	0042
XZE105	25	0043
XZE105	30	0044
XZE105	31	0006
XZE105	32	0006
XZE105	33	0006
XZE105	35	0006
XZE105	36	0045
XZE106	A 1	0041
XZE106	A 4	0046
XZE106	A 9	0047
XZE106	A10	0029
XZE106	A16	0002
XZE106	A18	0001
XZE106	A20	0005
XZE106	A25	0001
XZE106	A36	0001
XZE106	B 1	0045
XZE106	B 2	0014
XZE106	B 4	0044
XZE106	B 5	0029
XZE106	B 6	0029
XZE106	B16	0002
XZE106	B18	0001
XZE106	B20	0005
XZE108	A 1	0037
XZE108	A 4	0013

NETWORK LISTING (TABULAR WIRING DIAGRAM) - INDEX

TITLE
MODULE E WIRING OF SUPPLEMENTARY TRANSMITTER 336914

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
7756	1	/S268 #2	1 2 70	B 2	3

COMPONENT	PIN	NET
XZE108	A 9	0034
XZE108	A10	0022
XZE108	A12	0048
XZE108	A16	0002
XZE108	A18	0001
XZE108	A20	0005
XZE108	A22	0049
XZE108	A23	0002
XZE108	A25	0001
XZE108	A27	0049
XZE108	A31	0050
XZE108	A32	0051
XZE108	A33	0002
XZE108	A34	0050
XZE108	A36	0001
XZE108	B 1	0039
XZE108	B 3	0022
XZE108	B 4	0051
XZE108	B 5	0011
XZE108	B 6	0022
XZE108	B 8	0051
XZE108	B 9	0052
XZE108	B10	0052
XZE108	B11	0053
XZE108	B16	0002
XZE108	B18	0001
XZE108	B20	0005
XZE108	B27	0048
XZE110	A 1	0054
XZE110	A 2	0017
XZE110	A11	0027
XZE110	A12	0055
XZE110	A13	0008
XZE110	A14	0046
XZE110	A16	0002
XZE110	A18	0001
XZE110	A20	0005
XZE110	A22	0056
XZE110	A23	0015
XZE110	A24	0051
XZE110	A25	0022
XZE110	A30	0002
XZE110	A33	0039
XZE110	A34	0057
XZE110	A35	0035
XZE110	A36	0058
XZE110	B 1	0059
XZE110	B 2	0002
XZE110	B 3	0012
XZE110	B 9	0028
XZE110	B10	0046
XZE110	B11	0002
XZE110	B12	0056

COMPONENT	PIN	NET
XZE110	B13	0027
XZE110	B14	0060
XZE110	B16	0002
XZE110	B18	0001
XZE110	B20	0005
XZE110	B22	0014
XZE110	B23	0002
XZE110	B24	0053
XZE110	B25	0002
XZE110	B26	0010
XZE110	B27	0061
XZE110	B29	0002
XZE110	B32	0061
XZE110	B33	0034
XZE110	B34	0011
XZE110	B35	0062
XZE110	B36	0053
XZE112	A16	0002
XZE112	A18	0001
XZE112	A20	0005
XZE112	A24	0063
XZE112	A25	0024
XZE112	A26	0064
XZE112	A27	0016
XZE112	A30	0022
XZE112	A31	0047
XZE112	A32	0065
XZE112	A35	0013
XZE112	A36	0066
XZE112	B16	0002
XZE112	B18	0001
XZE112	B20	0005
XZE112	B24	0026
XZE112	B25	0065
XZE112	B26	0063
XZE112	B31	0067
XZE112	B32	0029
XZE112	B33	0032
XZE112	B34	0013
XZE112	B35	0032
XZE112	B36	0066
XZE114	A 7	0068
XZE114	A 9	0068
XZE114	A10	0060
XZE114	A11	0069
XZE114	A14	0069
XZE114	A16	0002
XZE114	A17	0066
XZE114	A18	0001
XZE114	A20	0005
XZE114	A21	0070
XZE114	A24	0022
XZE114	A26	0062

COMPONENT	PIN	NET
XZE114	A27	C071
XZE114	A28	C059
XZE114	A33	0058
XZE114	A36	C072
XZE114	B 1	0073
XZE114	B 2	0074
XZE114	B 4	0075
XZE114	B 6	0076
XZE114	B 7	C077
XZE114	B 9	C076
XZE114	B10	0073
XZE114	B11	0066
XZE114	B12	0076
XZE114	B14	0047
XZE114	B16	0002
XZE114	B18	0001
XZE114	B20	0005
XZE114	B22	C047
XZE114	B23	0022
XZE114	B25	C010
XZE114	B26	0058
XZE114	B27	0058
XZE114	B28	0072
XZE114	B30	0078
XZE114	B32	C063
XZE114	B34	0079
XZE116	A 1	0012
XZE116	A 6	C080
XZE116	A 7	0016
XZE116	A 9	0016
XZE116	A10	0081
XZE116	A11	0020
XZE116	A14	0020
XZE116	A16	0002
XZE116	A17	0082
XZE116	A18	CC01
XZE116	A20	0005
XZE116	A24	0056
XZE116	A26	0056
XZE116	A27	0083
XZE116	A28	0054
XZE116	A32	0054
XZE116	A36	C084
XZE116	B 2	0029
XZE116	B 4	0081
XZE116	B 6	0031
XZE116	B 9	0085
XZE116	B10	0086
XZE116	B12	C082
XZE116	B14	0087
XZE116	B16	0002
XZE116	B18	0001
XZE116	B20	0005

NETWORK LISTING (TABULAR WIRING DIAGRAM) - INDEX

TITLE: MODULE E WIRING OF SUPPLEMENTARY TRANSMITTER 336914

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
7756	1	VS268 ~~02~~	1 2 10	B 3 OF 3

COMPONENT	PIN	NET
XZE116	B22	0093
XZE116	B25	0088
XZE116	B26	0033
XZE116	B27	0094
XZE116	B28	0090
XZE116	B29	0054
XZE116	B30	0091
XZE116	B32	0092
XZE116	B34	0091
XZE118	A 1	0102
XZE118	A 6	0021
XZE118	A 7	0018
XZE118	A 9	0061
XZE118	A10	0097
XZE118	A11	0107
XZE118	A14	0099
XZE118	A16	0002
XZE118	A17	0055
XZE118	A18	0001
XZE118	A20	0005
XZE118	B 3	0064
XZE118	B 4	0003
XZE118	B 5	0107
XZE118	B 6	0100
XZE118	B 7	0029
XZE118	B 9	0067
XZE118	B10	0030
XZE118	B12	0029
XZE118	B13	0065
XZE118	B14	0108
XZE118	B16	0002
XZE118	B17	0067
XZE118	B18	0001
XZE118	B20	0005
XZE326	24	0086
XZE326	25	0085
XZE326	26	0007
XZE326	27	0096
XZE326	30	0007
XZE326	31	0006
XZE326	33	0099
XZE326	34	0017
XZE326	35	0095
XZE326	36	0007

OF PINS = 0362

END OF LISTING

COMPONENT	PIN	NET

COMPONENT	PIN	NET

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE: MODULE E WIRING OF SUPPLEMENTARY TRANSMITTER 336914

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
7756	1	VS268	1 2 70	C1 OF 5

NET	COMPONENT	PIN
0001	XZE103	B18
0001	XZE103	A18
0001	• XZE105	18
0001	• • • XZE106	A25
0001	• • • XZE106	A36
0001	• • XZE108	A25
0001	• • XZE108	A36
0001	• XZE106	A18
0001	• • XZE108	A18
0001	• • • XZE110	A18
0001	• • • • XZE112	A18
0001	**05 XZE114	A18
0001	**06 XZE116	A18
0001	**07 XZE118	A18
0001	**07 XZE118	B18
0001	**06 XZE116	B18
0001	**05 XZE114	B18
0001	• • • • XZE112	B18
0001	• • • XZE110	B18
0001	• • XZE108	B18
0001	• XZE106	B18
0001	XZE102	18
0001	XZE102	2
0001	XZE102	28
0001	CBE 3	2
0002	XZE102	27
0002	XZE102	4
0002	XZE102	16
0002	XZE103	A16
0002	• XZE105	16
0002	• XZE106	A16
0002	• • XZE108	A16
0002	• • • • XZE108	B16
0002	• • • • XZE110	B25
0002	• • • XZE110	A16
0002	**05 XZE110	B16
0002	**05 XZE110	B11
0002	**06 XZE110	B23
0002	**05 XZE110	B 2
0002	• • • • XZE112	A16
0002	**05 XZE114	A16
0002	**06 XZE116	A16
0002	**07 XZE118	A16
0002	**08 XZE118	B16
0002	**07 JE128	B 2
0002	**06 XZE116	B16
0002	**05 XZE114	B16
0002	• • • • XZE112	B16
0002	• • • XZE110	A30
0002	• • • XZE110	B29
0002	• • XZE108	A23
0002	• • XZE108	A33

NET	COMPONENT	PIN
0002	• XZE106	B16
0002	XZE103	B16
0002	SWE122	1
0002	SWE122	4
0003	XZE103	B30
0003	XZE102	9
0003	XZE118	B 4
0004	XZE102	12
0004	JE128	C 8
0005	XZE103	B20
0005	XZE103	A20
0005	• XZE105	20
0005	• XZE106	A20
0005	• • XZE108	A20
0005	• • • XZE110	A20
0005	• • • • XZE112	A20
0005	**05 XZE114	A20
0005	**06 XZE116	A20
0005	**07 XZE118	A20
0005	**07 XZE118	B20
0005	**06 XZE116	B20
0005	**05 XZE114	B20
0005	• • • • XZE112	B20
0005	• • • XZE110	B20
0005	• • XZE108	B20
0005	• XZE106	B20
0005	XZE102	20
0005	XZE102	14
0005	XZE102	24
0005	CBE 4	2
0006	XZE102	15
0006	XZE102	26
0006	XZE105	31
0006	• XZE105	32
0006	• • XZE105	35
0006	• • XZE326	31
0006	• • JE128	H 6
0006	• XZE105	33
0006	XZE105	10
0006	XZE105	11
0006	XZE105	14
0007	XZE102	22
0007	XZE326	26
0007	XZE326	30
0007	XZE326	36
0008	XZE102	29
0008	XZE110	A13

RM 151698 (9-63)

TELETYPE

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE
MODULE E WIRING OF SUPPLEMENTARY TRANSMITTER 336914

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
90 7756	1	VS268	1 2 70	C2OF 5

NET	COMPONENT	PIN
0009	XZE102	30
0009	XZE102	36
0010	XZE102	31
0010	XZE110	B26
0010	XZE114	B25
0011	XZE102	32
0011	XZE108	B 5
0011	XZE110	B34
0012	XZE102	33
0012	XZE110	B 3
0012	XZE116	A 1
0013	XZE102	34
0013	XZE112	B34
0013	XZE112	A35
0013	XZF103	B26
0013	XZE108	A 4
0014	XZE102	35
0014	XZE110	B22
0014	XZE106	B 2
0015	XZE103	A 1
0015	XZE110	A23
0016	XZE103	B22
0016	XZE103	A 7
0016	XZE116	A 7
0016	XZE116	A 9
0016	XZE112	A27
0017	XZE110	A 2
0017	XZE103	A 9
0017	XZE326	34
0018	XZE103	B 4
0018	XZE103	A10
0018	XZE118	A 7
0019	XZE103	A11
0019	XZE103	A35
0020	XZE103	A14
0020	XZE116	A11
0020	XZE116	A14
0021	XZE103	B13
0021	XZE103	A17
0021	XZF118	A 6

NET	COMPONENT	PIN
0022	XZE103	A24
0022	XZE103	A21
0022	XZE108	B 3
0022	XZE108	B 6
0022	XZE108	A10
0022	• XZE114	B23
0022	• XZE114	A24
0022	XZE110	A25
0022	XZE112	A30
0023	XZE103	A26
0023	XZE103	B12
0024	XZE103	B21
0024	XZE103	A27
0024	XZE112	A25
0025	XZE103	A28
0025	XZE103	A32
0026	XZE103	B28
0026	XZE103	A33
0026	XZE112	B24
0027	XZE103	A36
0027	XZE103	B10
0027	• XZE110	A11
0027	• XZE110	B13
0027	XZE103	B17
0028	XZE103	B 1
0028	XZE110	B 9
0029	XZE103	B23
0029	XZE103	B 5
0029	XZE106	B 5
0029	• XZE116	B 2
0029	• XZE118	B 7
0029	• XZE118	B12
0029	• XZE112	B32
0029	XZE106	B 6
0029	XZE106	A10
0030	XZE103	B 6
0030	XZE118	B10
0031	XZE103	B 9
0031	XZE116	B 6
0032	XZE103	B25
0032	XZE112	B35
0032	XZE112	B33

TITLE
MODULE E WIRING OF SUPPLEMENTARY TRANSMITTER 336914

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
00 7756	1	VS268	1 2 70	C3OF 5

NET	COMPONENT	PIN
0033	XZE103	B27
0033	XZE116	B26
0034	XZE103	B32
0034	XZE110	B33
0034	XZE108	A 9
0035	XZE103	B34
0035	XZE110	A35
0036	XZE105	1
0036	JE128	G 7
0037	XZE105	2
0037	XZE108	A 1
0038	XZE105	4
0038	JE128	H 8
0039	XZE105	9
0039	XZE108	B 1
0039	XZE110	A33
0040	XZE105	22
0040	JE128	G 9
0041	XZE105	23
0041	XZE106	A 1
0042	XZE105	24
0042	JE128	G 8
0043	XZE105	25
0043	JE128	G10
0044	XZE105	30
0044	XZE106	B 4
0045	XZE105	36
0045	XZE106	B 1
0046	XZE106	A 4
0046	XZE110	B10
0046	XZE110	A14
0047	XZE106	A 9
0047	XZE114	B14
0047	XZE114	B22
0047	• JE128	F 8
0047	XZE112	A31
0048	XZE108	A12
0048	XZE108	B27
0049	XZE108	A22
0049	XZE108	A27
0050	XZE108	A31
0050	XZE108	A34
0051	XZE108	B 4
0051	XZE108	B 8
0051	XZE108	A32
0051	XZE110	A24
0052	XZE108	B 9
0052	XZE108	B10
0053	XZE108	B11
0053	XZE110	B24
0054	XZE110	A 1
0054	XZE116	A28
0054	• XZE116	B29
0054	XZE116	A32
0055	XZE110	A12
0055	XZE118	A17
0056	XZE110	B12
0056	XZE110	A22
0056	XZE116	A26
0056	XZE116	A24
0057	XZE110	A34
0057	JE128	C 7
0058	XZE110	B36
0058	XZE110	A36
0058	XZE114	A33
0058	XZE114	B27
0058	XZE114	B26
0059	XZE110	B 1
0059	XZE114	A28
0060	XZE110	B14
0060	XZE114	A10
0061	XZE110	B27
0061	XZE110	B32
0061	XZE118	A 9
0062	XZE110	B35
0062	XZE114	A26

NETWORK LISTING (TABLULAR WIRING DIAGRAM)

TITLE
MODULE E WIRING OF SUPPLEMENTARY TRANSMITTER 336914

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
88 7756	1	VS268	1 2 70	C 4OF 5

NET	COMPONENT	PIN
0063	XZE112	A24
0063	XZE112	B26
0063	XZE114	B32
0064	XZE112	A26
0064	XZE118	B 3
0065	XZE112	B25
0065	XZE112	A32
0065	XZE118	B13
0066	XZE112	B36
0066	XZE112	A36
0066	XZE114	A17
0066	XZE114	B11
0067	XZE112	B31
0067	XZE118	B 9
0067	XZE118	B17
0068	XZE114	A 7
0068	XZE114	A 9
0069	XZE114	A11
0069	XZE114	A14
0070	XZE114	A21
0070	JE128	D 8
0071	XZE114	A27
0071	JE128	D 7
0072	XZE114	A36
0072	XZE114	B28
0072	JE128	E 8
0073	XZE114	B10
0073	XZE114	B 1
0073	JE128	B 7
0074	XZE114	B 2
0074	JE128	A 7
0075	XZE114	B 4
0075	JE128	A 8
0076	XZE114	B 6
0076	XZE114	B 9
0076	XZE114	B12
0077	XZE114	B 7
0077	SWE122	2

NET	COMPONENT	PIN
0078	XZE114	B30
0078	JE128	B 1
0079	XZE114	B34
0079	JE128	F 7
0080	XZE116	A 6
0080	JE128	A10
0081	XZE116	B 4
0081	XZE116	A10
0081	JE128	B10
0082	XZE116	A17
0082	XZE116	B12
0082	JE128	F 9
0083	XZE116	A27
0083	XZE116	B22
0083	JE128	H 9
0084	XZE116	A36
0084	JE128	B 8
0085	XZE116	B 9
0085	XZE326	25
0086	XZE116	B10
0086	XZE326	24
0087	XZE116	B14
0087	JE128	F10
0088	XZE116	B25
0088	JE128	H10
0089	XZE116	B27
0089	XZE118	A14
0090	XZE116	B28
0090	JE128	E10
0091	XZE116	B34
0091	XZE116	B30
0091	JE128	B 9
0092	XZE116	B32
0092	JE128	A 9
0093	JE128	A 3
0093	CBE 4	1

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE: MODULE E WIRING OF SUPPLEMENTARY TRANSMITTER 336914

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
00 7756	1	VS268	1 2 70	C5 OF 5

NET	COMPONENT	PIN
0094	JE128	C 1
0094	CBF 3	1
0095	JE128	C 9
0095	XZE326	35
0096	JE128	C10
0096	XZE326	27
0097	JE128	D 1
0097	XZE118	A10
0098	JE128	D 2
0098	JF228	2
0098	JE 1	3
0099	JE128	D 9
0099	XZE326	33
0100	JE128	D10
0100	XZE118	B 6
0101	JE128	E 1
0101	CBE 2	1
0102	JE128	E 7
0102	XZE118	A 1
0103	JE128	H 4
0103	CBE 2	2
0104	JE228	1
0104	CBE 1	1
0105	JE228	3
0105	JE 1	2
0106	CBE 1	2
0106	JE 1	1
0107	XZE118	A11
0107	XZE118	B 5
0108	XZE118	B14
0108	SWE122	5

NUMBER OF WIRES - 0254

NET	COMPONENT	PIN

END OF LISTING

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	SHEET NO.
SHEET INDEX	A1	1																									A1
NOTES	A2	1																									A2
NOTES	A3	1																									A3
NOTES	A4	1																									A4
NOTES	A5	1																									A5
NOTES	A6	1																									A6
NETWORK LISTING-INDEX (B SECTION)	ALL	1																									ALL
NETWORK LISTING (C SECTION)	ALL	1																									ALL

SUPPORTING INFORMATION

CATEGORY	NO.
VS268 M.A.P.S. SUPPLEMENTARY TRANSMITTER SET.	WDP0235

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND UPDATED EACH TIME ANY SHEET OF THE DRAWING IS REISSUED OR A NEW SHEET IS ADDED.
3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.

REVISIONS

ISSUE	DATE	AUTH. NO.
1	6-5-70	20846-R

WIRING DIAGRAM

FOR

SUPPLEMENTARY

CONTROL PANEL

310913

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
	R/R	

ENGR. R.G.S.	DSGNR.
DRN. D.Q.	DATE 3-16-70
R & D FILE	38-A2/65AA
S-NUMBER	61.761S

TELETYPE

7757WD-A1

TC 639 (3-69)

NOTES

1. Connect IN682 Diode (177611) to the indicated "To" Terminals with 60340 RM Tubing on each end of diode.

2. Connect 150 ohm Resistor (310988) to the indicated "To" terminal.

3. Wire must be connected to the indicated "From" and "To" terminals. The "To" end of the wire must have a 72597 RM terminal connected to it. The "To" terminal is a screw on the JF 103 Connector Mount.

4. Use 155754 Tubing on the following pins of JF 103: 5, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, and 36.

5. Use 155752 Tubing on the following pins of JF 103: 1, 3 and 7

6. All white 20 AWG is 31722 RM
   All black 20 AWG is 31721 RM
   All red 20 AWG is 32147 RM
   All green 24 AWG is 31784 RM

7. Switch designations SWF - - - and SF - - - are identical. In the schematic wiring diagram it appears as SWF - - -.

7757 WD-A2

REVISIONS

ISSUE	DATE	AUTH. NO.
1	6-5-70	20846-R

WIRING DIAGRAM FOR SUPPLEMENTARY CONTROL PANEL 310913

APPROVALS

D AND R	E OF M
LCM	

S-NUMBER 61,761S

PROD. NO. 7757WD

DATE: 1-05-70

P.D. FILE NO. 38-A2/65AA

DRAWN. DQ | CHKD. MWB

ENGD. HGS | APPD. RMR

TELETYPE CORPORATION

7757 WD-A2

ST-101401

NOTES

7757 WD-A3

REVISIONS

ISSUE	DATE	AUTH. NO.
→	6-5-70	20846-R

8. This WD consists of three sections:

Section A	Notes
Section B	Network Listing - Index
Section C	Network Listing

9. NETWORK LISTING - INDEX

The Index lists pins in alpha-numerical order and is a cross reference to the number of the network in which they appear.

10. NETWORK LIST

The Network List is a list of connector pins that are connected together in a common electrical circuit. It lists the pins in from-to-to order. At branching points the first pin of the branch is indented. A second indentation indicates a branch within the first branch. Three indents indicate a third sub branch. If further sub branches are encountered, an indent number is used instead of further identing.

At a branching point the branching pin is connected to the pin listed on the next line below as well as to the pin at the end of the column of dots extending below the branching pin. If no pins are listed directly below or to the right, the branch ends. There is no direct connection between a pin and one listed below and in a colmun to its left.

The asterisk in front of the indent number identifies the first pin of a new sub branch.

11. POWER NETWORKS

The following listing indicates a terminal common to a particular voltage. The index will provide the individual network number.

VOLTAGE	TERMINAL
-12V	JF103 1
Lamp Common	JF103 34

67100143
VC202(C-04)

WIRING DIAGRAM FOR SUPPLEMENTARY CONTROL PANEL 310913

APPROVALS

D AND R	E OF M
LEM	

S NUMBER 61,761S

PROD. NO. 7757WD

DATE: 1-05-70

P.D. FILE NO. 38-A2/65AA

DRAWN. DQ	CHKD. MWR
ENGD. RGS	APPD.

TELETYPE CORPORATION

7757 WD-A3

ST-101401

7757WD-A4		
REVISIONS		
ISSUE	DATE	AUTH. NO.
1	6-5-70	20846-R

SAMPLE NETWORK (Arrows Show Connections)

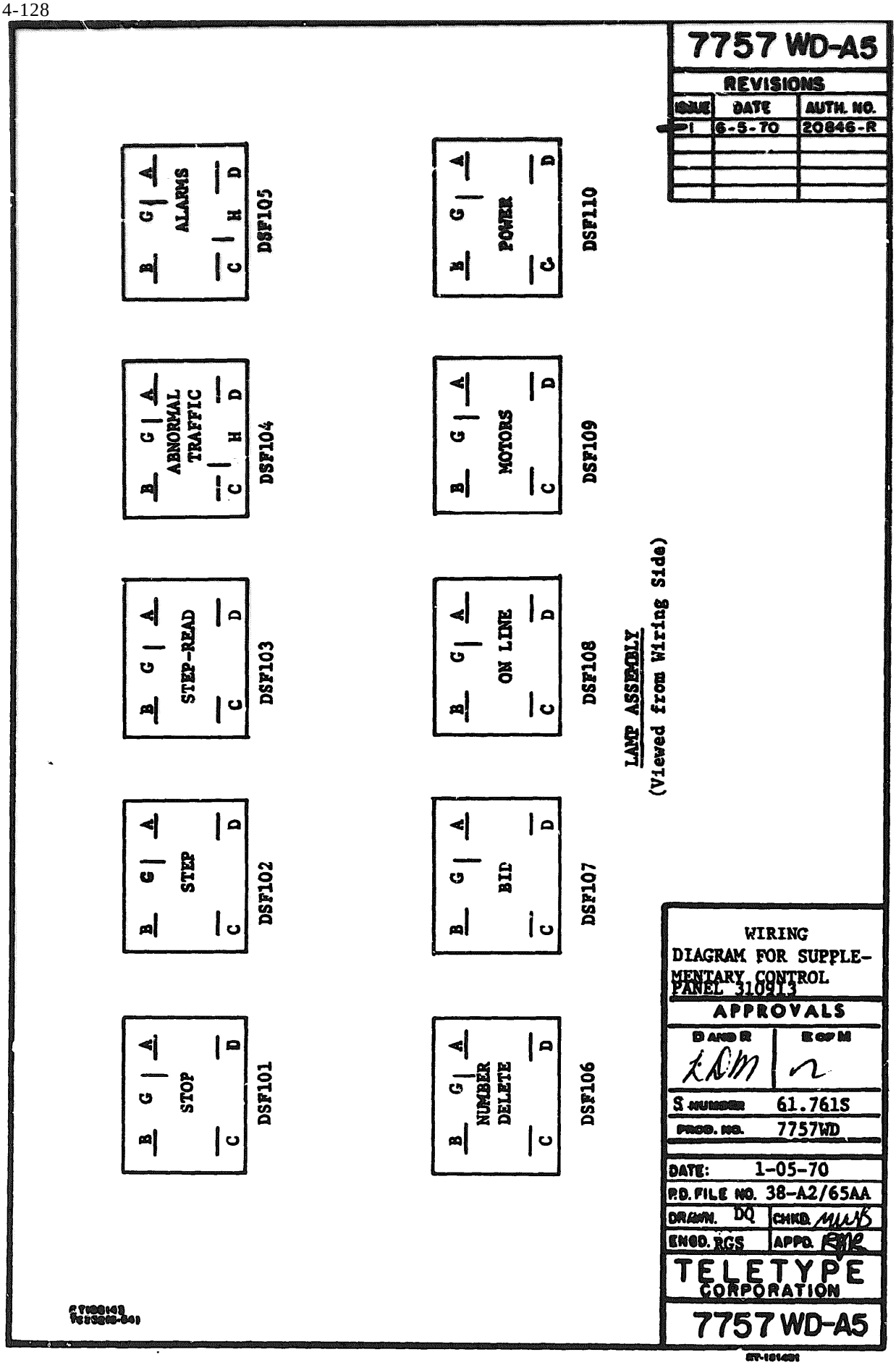
Net	Component	Pin
0143	JD 4	G 6
0143	XZD314	21
0143	XZD313	20
0143	. . XZD313	6
0143	. . XZD312	6
0143	. . XZD311	6
0143	. XZD313	23
0143	. . XZD313	25
0143	. . . XZD313	31
0143	04 . . XZD313	33
0143	04 . . XZD312	33
0143	. . . XZD312	31
0143	. . . XZD311	31
0143	. . XZD312	25
0143	. . XZD311	25
0143	. XZD312	23
0143	. XZD311	23
0143	XZD312	20
0143	XZD311	20
0144	JD 4	G 7
0144	XZD308	18
0144	XZD309	18
0144	XZD310	18
0144	. XZD310	28
0144	. . XZD313	8
0144	. . XZD314	31
0144	. . XZD319	29
0144	. . XZD328	31
0144	. XZD309	28
0144	. XZD308	28
0144	XZD310	4
0144	XZD309	4

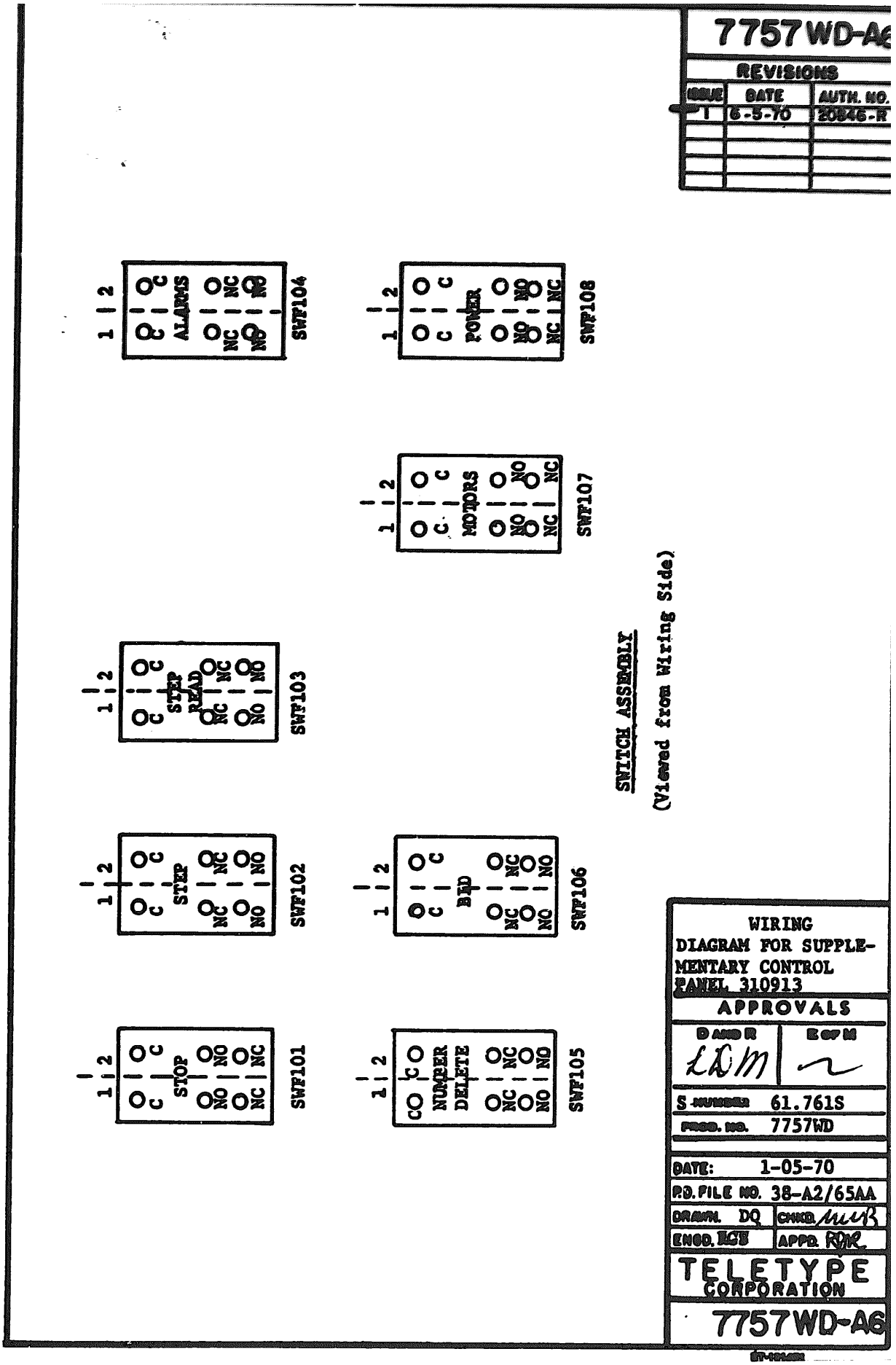
WIRING DIAGRAM FOR SUPPLEMENTARY CONTROL PANEL 310913

APPROVALS	
DRAWN	CHKD
JDM	
S [illegible]	61.761S
PROD. NO.	7757WD
DATE:	1-05-70
RD. FILE NO.	38-A2/65AA
DRAWN DQ	CHKD MWS
ENGR. RGS	APPD RJK

TELETYPE CORPORATION

7757 WD-A4


7757 WD-A5
REVISIONS
ISSUE | DATE | AUTH. NO.
1 | 6-5-70 | 20846-R
B G A
STOP
C D
DSF101
B G A
STEP
C D
DSF102
B G A
STEP-READ
C D
DSF103
B G A
ABNORMAL TRAFFIC
C H D
DSF104
B G A
ALARMS
C H D
DSF105
B G A
NUMBER DELETE
C D
DSF106
B G A
BID
C D
DSF107
B G A
ON LINE
C D
DSF108
B G A
MOTORS
C D
DSF109
B G A
POWER
C D
DSF110
LAMP ASSEMBLY
(Viewed from Wiring Side)
WIRING DIAGRAM FOR SUPPLEMENTARY CONTROL PANEL 310913
APPROVALS
D AND R
E OF M
S NUMBER 61.761S
PROD. NO. 7757WD
DATE: 1-05-70
P.D. FILE NO. 38-A2/65AA
DRAWN. DQ
CHKD. MWB
ENGD. RGS
APPD.
TELETYPE CORPORATION
7757 WD-A5


7757WD-A6
REVISIONS
ISSUE
DATE
AUTH. NO.
1
6-5-70
20846-R
SWF104
ALARMS
SWF108
POWER
SWF107
MOTORS
SWF103
STEP
READ
SWF102
STEP
SWF106
BID
SWF101
STOP
SWF105
NUMBER
DELETE
SWITCH ASSEMBLY
(Viewed from Wiring Side)
WIRING
DIAGRAM FOR SUPPLE-
MENTARY CONTROL
PANEL 310913
APPROVALS
D AND R
E OF M
S NUMBER 61.761S
PROD. NO. 7757WD
DATE: 1-05-70
P.D. FILE NO. 38-A2/65AA
DRAWN. DQ
CHKD.
ENGD. ECS
APPD.
TELETYPE
CORPORATION
7757WD-A6

NETWORK LISTING (TABULAR WIRING DIAGRAM) -INDEX

TITLE
CONTROL PANEL WIRING OF SUPPLEMENTARY TRANSMITTER 210913

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
7757	1	VS269	1 2 70	1 OF 1

COMPONENT	PIN	NET
CRF101	A	0016
CRF101	C	0028
CRF102	A	0033
CRF102	C	0035
FRAME		0027
JF103	1	0018
JF103	5	0017
JF103	7	0019
JF103	9	0020
JF103	10	0021
JF103	11	0022
JF103	12	0023
JF103	13	0024
JF103	14	0025
JF103	15	0026
JF103	16	0027
JF103	17	0003
JF103	18	0028
JF103	19	0029
JF103	20	0030
JF103	21	0031
JF103	22	0032
JF103	23	0033
JF103	24	0014
JF103	25	0015
JF103	26	0006
JF103	27	0007
JF103	28	0012
JF103	29	0013
JF103	30	0010
JF103	31	0011
JF103	32	0008
JF103	33	0009
JF103	34	0034
JF103	35	0005
JF103	36	0004
RF101	1	0016
RF101	2	0018
RF102	1	0001
RF102	2	0018
RF103	1	0035
RF103	2	0003
SF101	1 C	0001
SF101	1NO	0002
SF101	2 C	0003
SF101	2NC	0005
SF101	2NO	0004
SF102	2 C	0003
SF102	2NC	0007
SF102	2NO	0006
SF103	2 C	0003
SF103	2NC	0009
SF103	2NO	0008

COMPONENT	PIN	NET
SF104	2 C	0003
SF104	2NC	0011
SF104	2NO	0010
SF105	2 C	0003
SF105	2NC	0013
SF105	2NO	0012
SF106	2 C	0003
SF106	2NC	0015
SF106	2NO	0014
SF107	1 C	0016
SF107	1NO	0002
SF107	2 C	0003
SF107	2NO	0017
SF108	1 C	0002
SF108	1NO	0018
SF108	2 C	0003
SF108	2NO	0019
XDSF101	A	0001
XDSF101	B	0001
XDSF101	C	0001
XDSF101	D	0001
XDSF101	G	0020
XDSF102	G	0018
XDSF103	A	0033
XDSF103	B	0035
XDSF103	C	0028
XDSF103	D	0016
XDSF104	A	0035
XDSF104	B	0035
XDSF104	C	0035
XDSF104	D	0035
XDSF104	G	0018
XDSF105	A	0031
XDSF105	B	0031
XDSF105	C	0030
XDSF105	D	0030
XDSF105	G	0021
XDSF105	H	0022
XDSF106	A	0029
XDSF106	B	0029
XDSF106	C	0029
XDSF106	D	0029
XDSF106	G	0023
XDSF107	A	0028
XDSF107	B	0028
XDSF107	C	0028
XDSF107	D	0028
XDSF107	G	0024
XDSF108	A	0032
XDSF108	B	0032
XDSF108	C	0032
XDSF108	D	0032
XDSF108	G	0025

COMPONENT	PIN	NET
XDSF109	A	0014
XDSF109	B	0014
XDSF109	C	0014
XDSF109	D	0014
XDSF109	G	0026
XDSF110	A	0002
XDSF110	B	0002
XDSF110	C	0002
XDSF110	D	0002
XDSF110	G	0034

OF PINS - 0116

END OF LISTING

TITLE
CONTROL PANEL WIRING OF SUPPLEMENTARY TRANSMITTER 310913

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
7757	1	VS96A	1 2 70	C1 OF 2

NET	COMPONENT	PIN
0001	XDSF101	A
0001	XDSF101	B
0001	XDSF101	C
0001	XDSF101	D
0001	SF101	1 C
0001	RF102	1
0002	SF101	1NO
0002	SF107	1NO
0002	SF108	1 C
0002	XDSF110	D
0002	XDSF110	C
0002	XDSF110	B
0002	XDSF110	A
0003	SF108	2 C
0003	SF107	2 C
0003	• JF103	17
0003	SF106	2 C
0003	SF105	2 C
0003	SF101	2 C
0003	SF102	2 C
0003	SF103	2 C
0003	SF104	2 C
0003	RF103	2
0004	SF101	2NO
0004	JF103	34
0005	SF101	2NC
0005	JF103	35
0006	SF102	2NC
0006	JF103	26
0007	SF102	2NC
0007	JF103	27
0008	SF103	2NO
0008	JF103	32
0009	SF103	2NC
0009	JF103	33
0010	SF104	2NO
0010	JF103	30
0011	SF104	2NC
0011	JF103	31
0012	SF105	2NC
0012	JF103	28
0013	SF105	2NC
0013	JF103	29
0014	SF106	2NC
0014	JF103	24
0015	SF106	2NC
0015	JF103	25
0016	RF101	A
0016	XDSF103	D
0016	XDSF109	A
0016	XDSF109	B
0016	XDSF109	C
0016	XDSF109	D
0016	SF107	1 C
0016	RF101	1
0017	SF107	2NC
0017	JF103	5
0018	JF103	1
0018	XDSF104	G
0018	SF108	1NO
0018	• XDSF102	G
0018	• RF102	2
0018	RF101	2
0019	SF108	2NO
0019	JF103	7
0020	JF103	9
0020	XDSF101	G
0021	JF103	10
0021	XDSF105	G
0022	JF103	11
0022	XDSF105	H
0023	JF103	12
0023	XDSF104	G
0024	JF103	13
0024	XDSF107	G
0025	JF103	14
0025	XDSF108	G
0026	JF103	15
0026	XDSF109	G
0027	JF103	16

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE
CONTROL PANEL WIRING OF SUPPLEMENTARY TRANSMITTER 21091?

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
7767	1	VS268	1 ? 7?	C? OF 2

NET	COMPONENT	PIN
0027	FRAME	
0028	JF103	1A
0028	XDSF107	D
0028	XDSF107	C
0028	XDSF107	B
0028	XDSF107	A
0028	XDSF103	C
0028	CPF101	C
0029	JF103	1C
0029	XDSF106	D
0029	XDSF106	C
0029	XDSF106	B
0029	XDSF106	A
0030	JF103	20
0030	XDSF105	D
0030	XDSF105	C
0031	JF103	21
0031	XDSF105	B
0031	XDSF105	A
0032	JF103	22
0032	XDSF108	D
0032	XDSF108	C
0032	XDSF108	B
0032	XDSF108	A
0033	JF103	23
0033	XDSF103	A
0033	CPF102	A
0034	JF103	34
0034	XDSF110	C
0035	XDSF104	A
0035	XDSF104	B
0035	XDSF104	C
0035	XDSF104	D
0035	PF103	1
0035	XDSF103	B
0035	CPF102	C

NUMBER OF WIRES - 0080

END OF LISTING

NET	COMPONENT	PIN

HIGH SPEED TAPE RECEIVER WITH RADIO FREQUENCY INTERFERENCE (RFI) SUPPRESSION FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS) WIRING DIAGRAM

1. GENERAL

1.01 **This section contains wiring diagrams and circuit card drawings for the high speed receiver with** radio **frequency interference (RFI) suppression, used in the** Multiple Address Processing System.

1.02 **The following** information can be found on each **wiring diagram: Physical component layout, wiring** symbols, **terminal numbers and locations, and wire network** lists. Not**es are included on wiring diagrams to explain the** symbols used and point out special conditions.

1.03 **Information covered in circuit card drawings, shows physical component layout, wiring symbols, schematic of the circuit card, circuit description, and bill of material. Notes are included on the diagrams to explain the symbols used, or to point out special conditions.**

1.04 **A complete listing of the schematic and actual wiring diagrams is presented in the wiring diagram index found in this section. The index lists the equipment title, wiring diagram number, type of diagram (A for actual, S for schematic, CD for circuit card drawings), and wiring diagram package number. Wiring diagrams are listed in numerical order.**

2. WIRING DIAGRAM INDEX

TITLE	WIRING DIAGRAM NUMBER	TYPE	WIRING DIAGRAM PACKAGE NUMBER
Receiver Cabinet	7745WD	A	0234
VS269 Receiver Set	7746WD	S	0234
Logic	336906	CD	0234
Relay and Contact	336908	CD	0234

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	SHEET NO.
SHEET INDEX	A1	1																									A1
NOTES	A2	1																									A2
CABLE ROUTING	A3	1																									A3
NOTES	A4	1																									A4
NOTES	A5	1																									A5
NETWORK LISTING-INDEX (B SECTION)	ALL	1																									ALL
NETWORK LISTING (C SECTION)	ALL	1																									ALL

SUPPORTING INFORMATION

CATEGORY	NO.
VS269 M.A.P.S. RECEIVER SET.	WDP0234

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND UPDATED EACH TIME ANY SHEET OF THE DRAWING IS REISSUED OR A NEW SHEET IS ADDED.
3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.

REVISIONS

ISSUE	DATE	AUTH. NO.
1	6-5-70	20846-R

WIRING DIAGRAM

FOR

RECEIVER CABINET

336915

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

ENGR. R.G.S.	DSGNR.
DRN. D.Q.	DATE 3-16-70
R & D FILE	38-A2765AA
S-NUMBER	61,762S

TELETYPE

7745WD - A1

TC 639 (3-69)

NOTES

7745 WD-

REVISIONS

ISSUE	DATE	AUTH.
J	6-5-70	2084

1. Wire is part of 310840 Cable Assembly and must be connected to this indicated "From" terminal.

2. Wire is 31044RM Lamp Cord with length given in feet. It must be connected between the indicated "From" and "To" terminals.

3. Wire is part of 310838 Cable Assembly and must be connected to the indicated "From" and "To" terminals.

4. Wire is part of 310841 Cable Assembly and must be connected to the indicated "From" terminal.

5. Wire is part of 310841 Cable Assembly and must be connected to the indicated "To" terminal.

6. Wire is part of 310841 Cable Assembly and must be connected to the indicated "From" and "To" terminals.

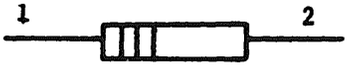
7. Wire is part of 310841 Cable Assembly and are connected between terminals of indicated connectors.

8. Wire is 193479 Strap and must be connected to the indicated "From" and "To" terminals.

9. Wire is 31883RM Green 18 AWG and must be connected to the indicated "From" and "To" terminals.

10. Wire is 31880RM with length given in inches and must be connected to the indicated "From" and "To" terminals.

11. Components are four (4) 137438 Resistors and designated as R1 to R4. Connections must be made to the indicated "From" and "To" terminals.



12. POWER NETWORKS

The following list indicates a terminal common to a particular voltage. The index will provide the individual network number

VOLTAGE	TERMINAL	
115V AC	A	2
115V AC RTN	A	1
Frame	A	FR
+6V	TPC328	C1
-6V	TPC328	A3
Circuit Common	TPC328	B2
-12V	TPC328	E1

(TPC328)
Version(s-04)

WIRING DIAGRAM FOR RECI
CABINET 336815

APPROVAL

D AND R	E OR

S NUMBER	61,762
PROD. NO.	7745WI
DATE:	1-05-7
P.O. FILE NO.	98-A2
DRAWN. RO	CHKD.
ENGD. RGS	APPD.

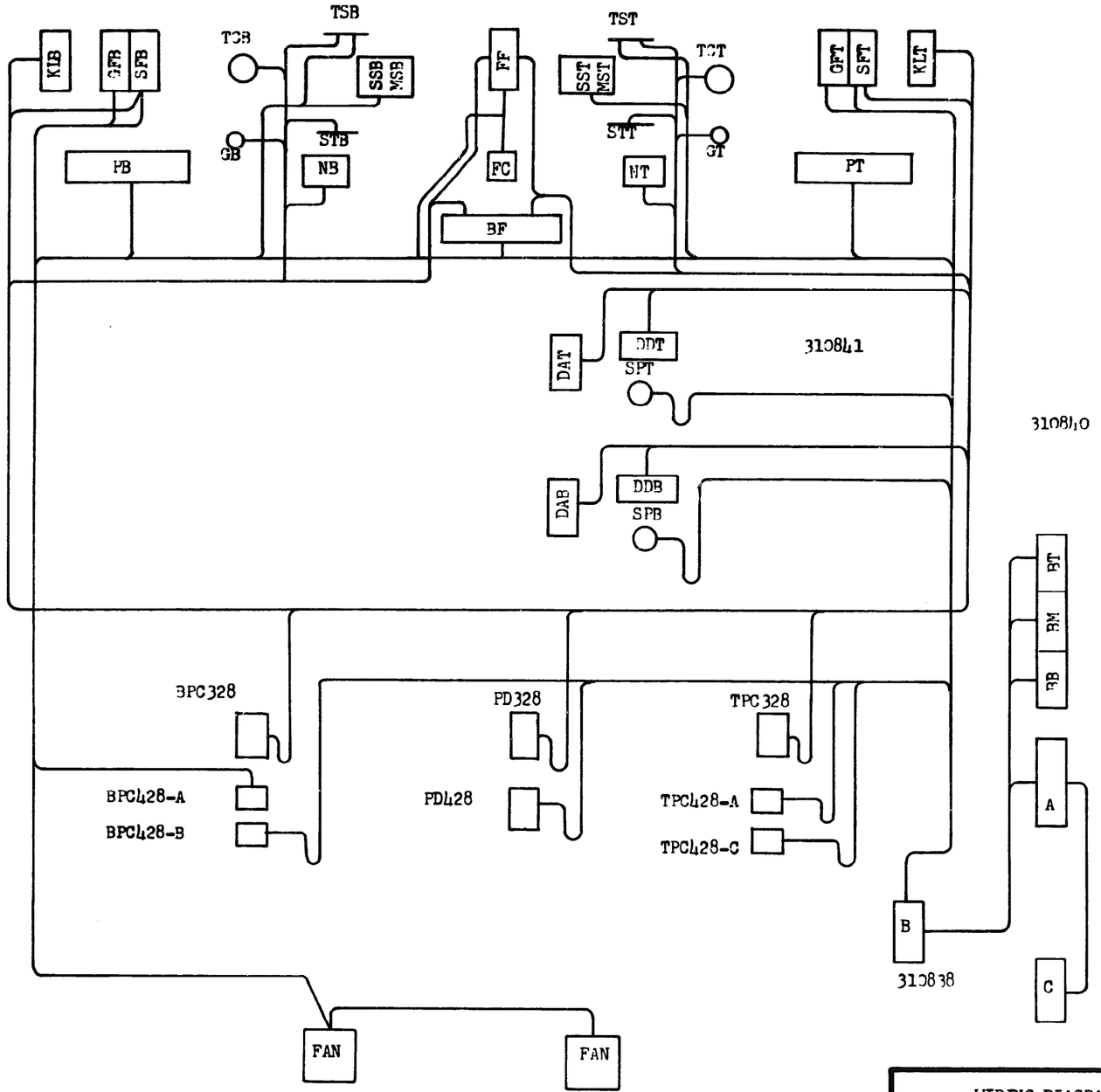
TELETYP
CORPORATIO

7745 WD-

ST-101400

12. Cabling Layout - Rear View

ISSUE



WIRING DIAGRAM FOR
RECEIVER CABINET 336915

TELETYPE

7745 WD-A3

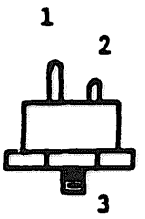
NOTES

7745 WD-A4

REVISIONS

ISSUE	DATE	AUTH. NO.
1	6-5-70	20946-R

13. Bi Directional Switch



14. PAGE NUMBERING

This WD consists of three sections:

Section A	Notes and Cable Routing
Section B	Network Listing - Index
Section C	Network Listing

15. Wire is part of 333336 Cable Assembly on 333343 Junction Box and must be connected to the indicated "To" Terminals.

16. NETWORK LISTING - INDEX

The Index lists pins in alpha-numerical order and is a cross reference to the number of the network in which they appear.

17. NETWORK LIST

The Network List is a list of connector pins that are connected together in a common electrical circuit. It lists the pins in from-to-to order. At branching points the first pin of the branch is indented. A second indentation indicates a branch within the first branch. Three indents indicates a third sub branch. If further sub branches are encountered, an indent number is used instead of further indenting.

At a branching point the branching pin is connected to the pin listed on the next line below as well as to the pin at the end of the column of dots extending below the branching pin. If no pins are listed directly below or to the right, the branch ends. There is no direct connection between a pin and one listed below and in a column to its left.

The asterisk in front of the indent number identifies the first pin of a new sub branch.

WIRING DIAGRAM FOR RECEIVER CABINET 336915

APPROVALS

D AND R	ENGR M
LDM	

S NUMBER 61,762S

PROD. NO. 7745WB

DATE: 1-05-70

P.O. FILE NO. 38-A2/65AA

DRAWN DQ | CHKD. MLJS

ENGD. RGS - | APPD. RGR

TELETYPE CORPORATION

7745 WD-A4

7745 WD-A5

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	6-5-70	20846-R

SAMPLE NETWORK (Arrows Show Connections)

```
Net   Component   Pin

0143  JD  4       G 6
0143  XZD314       21
0143  XZD313       20
0143  .     .      XZD313       6
0143  .     .      XZD312       6
0143  .     .      XZD311       6
0143  .     XZD313       23
0143  .     .     XZD313       25
0143  .     .     .   XZD313       31
0143  .  **04         XZD313       33
0143       04         XZD312       33
0143  .     .     .   XZD312       31
0143  .     .     .   XZD311       31
0143  .     .     XZD312       25
0143  .     .     XZD311       25
0143  .     XZD312       23
0143  .     XZD311       23
0143  XZD312       20
0143  XZD311       20

0144  JD  4       G 7
0144  XZD308       18
0144  XZD309       18
0144  XZD310       18
0144  .     XZD310       28
0144  .     .     XZD313       8
0144  .     .     XZD314       31
0144  .     .     XZD319       29
0144  .     .     XZD328       31
0144  .     XZD309       28
0144  .     XZD308       28
0144  XZD310        4
0144  XZD309        4
```

WIRING
DIAGRAM FOR
RECEIVER 336915

APPROVALS

NUMBER 61,7628
PROD. NO. 7745WD

DATE: 1-05-70
P.D. FILE NO. 38-A2/65AA
DRAWN DO | CHKD. MWB
ENGG. RGS | APPD. RMR

TELETYPE CORPORATION

7745 WD-A5

NETWORK LISTING (TABULAR WIRING DIAGRAM)- INDEX

TITLE
CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
7745	1	VS269	1 2 70	1	4

COMPONENT	PIN	NET
A	1	0013
A	2	0054
A	3	0014
A	4	0055
A	5	0026
A	6	0056
A	FR	0217
B	1	0024
B	2	0013
B	3	0005
B	4	0014
B	5	0025
B	6	0026
B	FR	0012
B B	LIN	0056
B B	LOA	0025
B F	1	0014
B F	2	0014
B F	3	0023
B F	4	0023
B M	LIN	0055
B M	LOA	0005
B T	LIN	0054
B T	LOA	0024
BPC328	A 1	0167
BPC328	A 2	0168
BPC328	A 3	0165
BPC328	A 4	0205
BPC328	A 6	0096
BPC328	A 7	0201
BPC328	A 8	0142
BPC328	A 9	0134
BPC328	A10	0138
BPC328	B 1	0185
BPC328	B 2	0166
BPC328	B 4	0206
BPC328	B 6	0098
BPC328	B 7	0204
BPC328	B 8	0151
BPC328	B 9	0143
BPC328	B10	0147
BPC328	C 1	0192
BPC328	C 3	0186
BPC328	C 4	0207
BPC328	C 6	0100
BPC328	C 7	0190
BPC328	C 8	0196
BPC328	C 9	0135
BPC328	C10	0139
BPC328	D 1	0198
BPC328	D 2	0104
BPC328	D 4	0208
BPC328	D 6	0102

COMPONENT	PIN	NET
BPC328	D 7	0066
BPC328	D 8	0200
BPC328	D 9	0144
BPC328	D10	0148
BPC328	E 1	0202
BPC328	E 2	0110
BPC328	E 5	0159
BPC328	E 7	0088
BPC328	E 8	0203
BPC328	E 9	0136
BPC328	E10	0140
BPC328	F 1	0113
BPC328	F 2	0209
BPC328	F 3	0210
BPC328	F 4	0160
BPC328	F 5	0211
BPC328	F 7	C090
BPC328	F 8	0184
BPC328	F 9	0145
BPC328	F10	0149
BPC328	G 1	0114
BPC328	G 3	0212
BPC328	G 4	0164
BPC328	G 5	0213
BPC328	G 7	0092
BPC328	G 8	0191
BPC328	G 9	0137
BPC328	G1C	0141
BPC328	H 1	0115
BPC328	H 2	0214
BPC328	H 3	0215
BPC328	H 4	0216
BPC328	H 5	0161
BPC328	H 7	0094
BPC328	H 8	0197
BPC328	H 9	0146
BPC328	H10	0150
BPC428	A 1	0018
BPC428	A 2	0027
BPC428	A 3	0026
BPC428	B 1	0005
BPC428	B 2	0012
BPC428	B 3	0014
C	1	0013
C	2	0054
C	3	0014
C	4	0055
C	5	0026
C	6	0056
C	FR	0217
DA B	4	0159
DA B	10	0160
DA B	11	0161

COMPONENT	PIN	NET
DA B	12	0162
DA B	13	0163
DA B	14	0164
DA B	15	0165
DA B	16	0166
DA B	17	0167
DA B	18	0168
DA T	4	0152
DA T	10	0153
DA T	11	0154
DA T	12	0029
DA T	13	0030
DA T	14	0155
DA T	15	0156
DA T	16	0053
DA T	17	0157
DA T	18	0158
DD B	1	0134
DD B	2	0135
DD B	3	0136
DD B	4	0137
DD B	5	0138
DD B	6	0139
DD B	7	0140
DD B	8	0141
DD B	9	0142
DD B	13	0143
DD B	14	0144
DD B	15	0145
DD B	16	0146
DD B	17	0147
DD B	18	0148
DD B	19	0149
DD B	20	0150
DD B	21	0151
DD T	1	0116
DD T	2	0117
DD T	3	0118
DD T	4	0119
DD T	5	0120
DD T	6	0121
DD T	7	0122
DD T	8	0123
DD T	9	0124
DD T	13	0125
DD T	14	0126
DD T	15	0127
DD T	16	0128
DD T	17	0129
DD T	18	0130
DD T	19	0131
DD T	20	0132
DD T	21	0133

NETWORK LISTING (TABULAR WIRING DIAGRAM)- INDEX

TITLE
CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
7745	1	VS269	1 2 70	B2	4

COMPONENT	PIN	NET
FAN 1	1	C014
FAN 1	2	0023
FAN 2	1	0014
FAN 2	2	0023
FC	1	0014
FC	2	0023
FF	LIN	0005
FF	LOA	0006
G B	1	0166
G T	1	0053
GF B	LIN	0003
GF B	LOA	0004
GF T	LIN	0001
GF T	LOA	0002
INNER	FR	0012
KL B	1	0202
KL B	3	0162
KL B	4	0163
KL B	5	0214
KL B	7	0210
KL B	8	0212
KL B	9	0215
KL B	10	0189
KL B	11	0183
KL B	12	0182
KL B	13	0188
KL B	14	0194
KL B	15	0199
KL B	16	0213
KL B	17	0211
KL B	18	0209
KL B	19	0195
KL B	20	0023
KL B	22	0006
KL B	24	0205
KL B	25	0206
KL B	26	0207
KL B	27	0208
KL B	28	0216
KL B	29	0187
KL B	30	0019
KL B	31	C193
KL B	32	0004
KL B	33	0017
KL B	34	0104
KL B	36	0166
KL T	1	0028
KL T	3	0029
KL T	4	0030
KL T	5	0031
KL T	7	0032
KL T	8	0033
KL T	9	0034

COMPONENT	PIN	NET
KL T	10	C035
KL T	11	0036
KL T	12	0037
KL T	13	0038
KL T	14	0039
KL T	15	0040
KL T	16	0041
KL T	17	0042
KL T	18	0043
KL T	19	0044
KL T	20	0023
KL T	22	0006
KL T	24	0045
KL T	25	0046
KL T	26	0047
KL T	27	0048
KL T	28	0049
KL T	29	0050
KL T	30	0016
KL T	31	0051
KL T	32	0002
KL T	33	0015
KL T	34	0052
KL T	36	0053
MS B	1	0018
MS B	2	0020
MS B	3	0003
MS T	1	0011
MS T	2	0218
MS T	3	0001
N B	1	0086
N B	2	0087
N B	3	0088
N B	4	0089
N B	5	0090
N B	6	0091
N B	7	0092
N B	8	0093
N B	9	0094
N B	10	0095
N B	11	0096
N B	12	0097
N B	13	0098
N B	14	0099
N B	15	0100
N B	16	0101
N B	17	0102
N B	18	0103
N B	19	0104
N B	20	0105
N B	21	0106
N B	22	0107
N B	23	0108

COMPONENT	PIN	NET
N B	26	0109
N B	27	0110
N B	28	0111
N B	30	0112
N B	32	0113
N B	34	0114
N B	36	0115
N T	1	0057
N T	2	0058
N T	3	0059
N T	4	0060
N T	5	0061
N T	6	0062
N T	7	0063
N T	8	0064
N T	9	0065
N T	10	0066
N T	11	0067
N T	12	0068
N T	13	0069
N T	14	0070
N T	15	0071
N T	16	0072
N T	17	0073
N T	18	0074
N T	19	0052
N T	20	0075
N T	21	0076
N T	22	0077
N T	23	0078
N T	26	0079
N T	27	0080
N T	28	0081
N T	30	0082
N T	32	0083
N T	34	0084
N T	36	0085
OUTER	FR	0012
P B	1	0010
P B	2	0025
P B	3	0003
P B	4	0026
P B	6	0018
P B	FR	0027
P T	1	0008
P T	2	0024
P T	3	0001
P T	4	0013
P T	6	0011
P T	FR	0012
PD328	A 1	0076
PD328	A 2	0078
PD328	A 3	0156

NETWORK LISTING (TABULAR WIRING DIAGRAM)- INDEX

TITLE
CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
7745	1	VS269	1 2 70	B 3	4

COMPONENT	PIN	NET
PD328	A 4	0037
PD328	A 5	0036
PD328	A 8	0169
PD328	A10	0064
PD328	B 1	0170
PD328	B 2	0171
PD328	B 3	0050
PD328	B 4	0038
PD328	B 5	0035
PD328	B 7	0172
PD328	B 8	0173
PD328	B 9	0074
PD328	B10	0066
PD328	C 1	0174
PD328	C 2	0051
PD328	C 3	0081
PD328	C 4	0039
PD328	C 5	0044
PD328	C 7	0175
PD328	C 8	0176
PD328	C 9	0058
PD328	C10	0068
PD328	D 1	0177
PD328	D 2	0052
PD328	D 4	0040
PD328	D 6	0075
PD328	D 7	0178
PD328	D 8	0179
PD328	D 9	0060
PD328	D10	0070
PD328	E 1	0028
PD328	E 3	0082
PD328	E 5	0079
PD328	E 6	0077
PD328	E 7	0180
PD328	E 8	0181
PD328	E 9	0062
PD328	E10	0072
PD428	A 1	0106
PD428	A 2	0108
PD428	A 3	0165
PD428	A 4	0182
PD428	A 5	0183
PD428	A 8	0184
PD428	A10	0093
PD428	B 1	0185
PD428	B 2	0186
PD428	B 3	0187
PD428	B 4	0188
PD428	B 5	0189
PD428	B 7	0190
PD428	B 8	0191
PD428	B 9	0103

COMPONENT	PIN	NET
PD428	B10	0095
PD428	C 1	0192
PD428	C 2	0193
PD428	C 3	0111
PD428	C 4	0194
PD428	C 5	0195
PD428	C 7	0196
PD428	C 8	0197
PD428	C 9	0087
PD428	C10	0097
PD428	D 1	0198
PD428	D 2	0104
PD428	D 4	C199
PD428	D 6	0105
PD428	D 7	0200
PD428	D 8	0201
PD428	D 9	0089
PD428	D10	0099
PD428	E 1	0202
PD428	E 3	0112
PD428	E 5	0109
PD428	E 6	0107
PD428	E 7	0203
PD428	E 8	0204
PD428	E 9	0091
PD428	E10	0101
R 1	1	0015
R 1	2	0021
R 2	1	0016
R 2	2	0218
R 3	1	0022
R 3	2	0017
R 4	1	0020
R 4	2	0019
SF B	LIN	0009
SF B	LOA	0010
SF T	LIN	0007
SF T	LOA	0008
SP B	1	0010
SP B	2	0027
SP B	3	0026
SP T	1	0008
SP T	2	0012
SP T	3	0013
SS B	1	0009
SS B	2	0022
SS B	3	0003
SS T	1	0007
SS T	2	0021
SS T	3	0001
ST B	1	0166
ST B	2	0104
ST B	3	0165

COMPONENT	PIN	NET
ST B	4	0202
ST T	1	0053
ST T	2	0052
ST T	3	0156
ST T	4	0028
TC B	1	0025
TC B	2	0003
TC T	1	0024
TC T	2	0001
TPC328	A 1	0157
TPC328	A 2	0158
TPC328	A 3	0156
TPC328	A 4	0045
TPC328	A 6	0067
TPC328	A 7	0179
TPC328	A 8	0124
TPC328	A 9	0116
TPC328	A10	0120
TPC328	B 1	0170
TPC328	B 2	0053
TPC328	B 4	0046
TPC328	B 6	0069
TPC328	B 7	0181
TPC328	B 8	0133
TPC328	B 9	0125
TPC328	B10	C129
TPC328	C 1	0174
TPC328	C 3	0171
TPC328	C 4	0047
TPC328	C 6	0071
TPC328	C 7	0172
TPC328	C 8	0175
TPC328	C 9	0117
TPC328	C10	0121
TPC328	D 1	0177
TPC328	D 2	0052
TPC328	D 4	0048
TPC328	D 6	0073
TPC328	D 7	0057
TPC328	D 8	0178
TPC328	D 9	0126
TPC328	D10	0130
TPC328	E 1	0028
TPC328	E 2	0080
TPC328	E 5	0152
TPC328	E 7	0059
TPC328	E 8	0180
TPC328	E 9	0118
TPC328	E10	0122
TPC328	F 1	0083
TPC328	F 2	0043
TPC328	F 3	0032
TPC328	F 4	0153

NETWORK LISTING (TABULAR WIRING DIAGRAM)- INDEX

TITLE
CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE	OF
7745	1	VS269	1 2 70	B4	4

COMPONENT	PIN	NET
TPC328	F 5	0042
TPC328	F 7	0061
TPC328	F 8	0169
TPC328	F 9	0127
TPC328	F10	0131
TPC328	G 1	0084
TPC328	G 3	0033
TPC328	G 4	0155
TPC328	G 5	0041
TPC328	G 7	0063
TPC328	G 8	0173
TPC328	G 9	0119
TPC328	G10	0123
TPC328	H 1	0085
TPC328	H 2	0031
TPC328	H 3	0034
TPC328	H 4	C049
TPC328	H 5	0154
TPC328	H 7	0065
TPC328	H 8	0176
TPC328	H 9	0128
TPC328	H10	0132
TPC428	A 1	0011
TPC428	A 2	0012
TPC428	A 3	0013
TPC428	B 1	0005
TPC428	B 2	0012
TPC428	B 3	0014
TS B	1	0017
TS B	2	0018
TS B	3	0009
TS B	4	0019
TS T	1	0015
TS T	2	0011
TS T	3	0007
TS T	4	0016

OF PINS = 0513

END OF LISTING

COMPONENT	PIN	NET

COMPONENT	PIN	NET

NETWORK LISTING (TABULAR WIRING DIAGRAM)- INDEX

TITLE
CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
7745	1	VS269	1 2 70	C1 OF 7

NET	COMPONENT	PIN
0001	GF	T LIN
0001	P	T 3
0001	• • TC	T 2
0001	• MS	T 3
0001	SS	T 3
0002	GF	T LOA
0002	KL	T 32
0003	GF	B LIN
0003	P	B 3
0003	• • SS	B 3
0003	• TC	B 2
0003	MS	B 3
0004	GF	B LOA
0004	KL	B 32
0005	FF	LIN
0005	B	3
0005	• • BPC428	B 1
0005	• B M	LOA
0005	TPC428	B 1
0006	KL	T 22
0006	FF	LOA
0006	KL	B 22
0007	SF	T LIN
0007	TS	T 3
0007	SS	T 1
0008	SF	T LOA
0008	P	T 1
0008	SP	T 1
0009	SF	B LIN
0009	TS	B 3
0009	SS	B 1
0010	SF	B LOA
0010	P	B 1
0010	SP	B 1
0011	TPC428	A 1
0011	P	T 6
0011	TS	T 2
0011	MS	T 1
0012	TPC428	A 2
0012	P	T FR
0012	• B	FR
0012	• • • •	BPC428 B 2

NET	COMPONENT	PIN
0012	• • •	INNER FR
0012	• •	OUTER FR
0012	•	TPC428 B 2
0012	SP	T 2
0013	TPC428	A 3
0013	P	T 4
0013	• SP	T 3
0013	R	2
0013	A	1
0013	C	1
0014	TPC428	B 3
0014	B	4
0014	• •	BPC428 B 3
0014	• A	3
0014	• C	3
0014	B F	2
0014	B F	1
0014	• • FAN	2 1
0014	• FC	1
0014	FAN 1	1
0015	KL	T 33
0015	TS	T 1
0015	R 1	1
0016	KL	T 30
0016	TS	T 4
0016	R 2	1
0017	R 3	2
0017	TS	B 1
0017	KL	B 33
0018	MS	B 1
0018	TS	B 2
0018	P	B 6
0018	BPC428	A 1
0019	R 4	2
0019	TS	B 4
0019	KL	B 30
0020	MS	B 2
0020	R 4	1
0021	SS	T 2
0021	R 1	2
0022	SS	B 2
0022	R 3	1

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE
CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
90 7745	1	VS269	1 2 70	C 2 OF 7

NET	COMPONENT	PIN
0023	FAN 1	2
0023	B F	4
0023	. . B F	3
0023	. . . KL B	20
0023	. . KL T	20
0023	. FC	2
0023	FAN 2	2
0024	TC T	1
0024	P T	2
0024	B	1
0024	B T	LOA
0025	TC B	1
0025	P B	2
0025	B	5
0025	B B	LOA
0026	BPC428	A 3
0026	P B	4
0026	. SP B	3
0026	B	6
0026	A	5
0026	C	5
0027	BPC428	A 2
0027	P B	FR
0027	SP B	2
0028	KL T	1
0028	ST T	4
0028	. TPC328	E 1
0028	PD328	E 1
0029	KL T	3
0029	DA T	12
0030	KL T	4
0030	DA T	13
0031	KL T	5
0031	TPC328	H 2
0032	KL T	7
0032	TPC328	F 3
0033	KL T	8
0033	TPC328	G 3
0034	KL T	9
0034	TPC328	H 3
0035	KL T	10

NET	COMPONENT	PIN
0035	PD328 .	B 5
0036	KL T	11
0036	PD328	A 5
0037	KL T	12
0037	PD328	A 4
0038	KL T	13
0038	PD328	B 4
0039	KL T	14
0039	PD328	C 4
0040	KL T	15
0040	PD328	D 4
0041	KL T	16
0041	TPC328	G 5
0042	KL T	17
0042	TPC328	F 5
0043	KL T	18
0043	TPC328	F 2
0044	KL T	19
0044	PD328	C 5
0045	KL T	24
0045	TPC328	A 4
0046	KL T	25
0046	TPC328	B 4
0047	KL T	26
0047	TPC328	C 4
0048	KL T	27
0048	TPC328	D 4
0049	KL T	28
0049	TPC328	H 4
0050	KL T	29
0050	PD328	B 3
0051	KL T	31
0051	PD328	C 2
0052	KL T	34
0052	ST T	2
0052	. . PD328	D 2

TITLE CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
80 7745	1	VS269	1 2 70	C3 OF 7

NET	COMPONENT	PIN
0052	• TPC328	C 7
0052	N T	19
0053	KL T	36
0053	ST T	1
0053	• • TPC328	B 2
0053	• G T	1
0053	DA T	16
0054	R T	LIN
0054	A	2
0054	C	2
0055	B M	LIN
0055	A	4
0055	C	4
0056	B R	LIN
0056	A	6
0056	C	6
0057	N T	1
0057	TPC328	D 7
0058	N T	2
0058	PD328	C 9
0059	N T	3
0059	TPC328	E 7
0060	N T	4
0060	PD328	D 9
0061	N T	5
0061	TPC328	F 7
0062	N T	6
0062	PD328	E 9
0063	N T	7
0063	TPC328	G 7
0064	N T	8
0064	PD328	A10
0065	N T	9
0065	TPC328	H 7
0066	N T	10
0066	PD328	B10
0067	N T	11
0067	TPC328	A 6
0068	N T	12
0068	PD328	C10
0069	N T	13
0069	TPC328	B 6
0070	N T	14
0070	PD328	D10
0071	N T	15
0071	TPC328	C 6
0072	N T	16
0072	PD328	E10
0073	N T	17
0073	TPC328	D 6
0074	N T	18
0074	PD328	B 9
0075	N T	20
0075	PD328	D 6
0076	N T	21
0076	PD328	A 1
0077	N T	22
0077	PD328	E 6
0078	N T	23
0078	PD328	A 2
0079	N T	26
0079	PD328	E 5
0080	N T	27
0080	TPC328	E 2
0081	N T	28
0081	PD328	C 3
0082	N T	30
0082	PD328	E 3
0083	N T	32
0083	TPC328	F 1
0084	N T	34
0084	TPC328	G 1
0085	N T	36

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE
CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
00 7745	1	VS269	1 2 70	C 4 OF 7

NET	COMPONENT	PIN
0085	TPC328	H 1
0086	N B	1
0086	BPC328	D 7
0087	N B	2
0087	PD428	C 9
0088	N B	3
0088	BPC328	E 7
0089	N B	4
0089	PD428	D 9
0090	N B	5
0090	BPC328	F 7
0091	N B	6
0091	PD428	E 9
0092	N B	7
0092	BPC328	G 7
0093	N B	8
0093	PD428	A10
0094	N B	9
0094	BPC328	H 7
0095	N B	10
0095	PD428	B10
0096	N B	11
0096	BPC328	A 6
0097	N B	12
0097	PD428	C10
0098	N B	13
0098	BPC328	B 6
0099	N B	14
0099	PD428	D10
0100	N B	15
0100	BPC328	C 6
0101	N B	16
0101	PD428	E10
0102	N B	17
0102	BPC328	D 6

NET	COMPONENT	PIN
0103	N B	18
0103	PD428	B 9
0104	N B	19
0104	ST B	3
0104	• • BPC328	B 2
0104	• KL B	[illegible]
0104	PD428	B 2
0105	N B	20
0105	PD428	D 6
0106	N B	21
0106	PD428	A 1
0107	N B	22
0107	PD428	E 6
0108	N B	23
0108	PD428	A 2
0109	N B	26
0109	PD428	E 5
0110	N B	27
0110	BPC328	E 2
0111	N B	28
0111	PD428	C 3
0112	N B	30
0112	PD428	E 3
0113	N B	32
0113	BPC328	F 1
0114	N B	34
0114	BPC328	G 1
0115	N B	36
0115	BPC328	H 1
0116	DD T	1
0116	TPC328	A 9
0117	DD T	2
0117	TPC328	C 9
0118	DD T	3
0118	TPC328	E 9
0119	DD T	4
0119	TPC328	G 9

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
7745	1	VS269	1 ? 70	C 5OF 7

NET	COMPONENT	PIN
0120	DD T	5
0120	TPC328	A10
0121	DD T	6
0121	TPC328	C10
0122	DD T	7
0122	TPC328	E10
0123	DD T	8
0123	TPC328	G10
0124	DD T	9
0124	TPC328	A 8
0125	DD T	13
0125	TPC328	B 9
0126	DD T	14
0126	TPC328	D 9
0127	DD T	15
0127	TPC328	F 9
0128	DD T	16
0128	TPC328	H 9
0129	DD T	17
0129	TPC328	B10
0130	DD T	18
0130	TPC328	D10
0131	DD T	19
0131	TPC328	F10
0132	DD T	20
0132	TPC328	H10
0133	DD T	21
0133	TPC328	B 8
0134	DD B	1
0134	BPC328	A 9
0135	DD B	2
0135	BPC328	C 9
0136	DD B	3
0136	BPC328	E 9
0137	DD B	4

NET	COMPONENT	PIN
0137	BPC328	G 9
0138	DD B	5
0138	BPC328	A10
0139	DD B	6
0139	BPC328	C10
0140	DD B	7
0140	BPC328	E10
0141	DD B	8
0141	BPC328	G10
0142	DD B	9
0142	BPC328	A 8
0143	DD B	13
0143	BPC328	B 9
0144	DD B	14
0144	BPC328	D 9
0145	DD B	15
0145	BPC328	F 9
0146	DD B	16
0146	BPC328	H 9
0147	DD B	17
0147	BPC328	B10
0148	DD B	18
0148	BPC328	D10
0149	DD B	19
0149	BPC328	F10
0150	DD B	20
0150	BPC328	H10
0151	DD B	21
0151	BPC328	B 8
0152	DA T	4
0152	TPC328	E 5
0153	DA T	10
0153	TPC328	F 4
0154	DA T	11
0154	TPC328	H 5

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE
CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE	PAGE
01 7745	1	VS269	1 2 70	C 6 OF 7

NET	COMPONENT	PIN
0155	DA T	14
0155	TPC328	G 4
0156	DA T	15
0156	ST T	3
0156	• TPC328	A 3
0156	PD328	A 3
0157	DA T	17
0157	TPC328	A 1
0158	DA T	18
0158	TPC328	A 2
0159	DA B	4
0159	BPC328	E 5
0160	DA B	10
0160	BPC328	F 4
0161	DA B	11
0161	BPC328	H 5
0162	DA B	12
0162	KL B	3
0163	DA B	13
0163	KL B	4
0164	DA B	14
0164	BPC328	G 4
0165	DA B	15
0165	ST B	3
0165	• BPC328	A 3
0165	PD428	A 3
0166	DA B	16
0166	ST B	1
0166	• • KL B	36
0166	• G B	1
0166	BPC328	B 2
0167	DA B	17
0167	BPC328	A 1
0168	DA B	18
0168	BPC328	A 2
0169	PD328	A 8
0169	TPC328	F 8
0170	PC328	B 1

NET	COMPONENT	PIN
0170	TPC328	B 1
0171	PD328	B 2
0171	TPC328	C 3
0172	PD328	B 7
0172	TPC328	C 7
0173	PD328	B 8
0173	TPC328	G 8
0174	PD328	C 1
0174	TPC328	C 1
0175	PD328	C 7
0175	TPC328	C 8
0176	PD328	C 8
0176	TPC328	H 8
0177	PD328	D 1
0177	TPC328	D 1
0178	PD328	D 7
0178	TPC328	D 8
0179	PD328	D 8
0179	TPC328	A 7
0180	PD328	E 7
0180	TPC328	E 8
0181	PD328	E 8
0181	TPC328	B 7
0182	PD428	A 4
0182	KL B	12
0183	PD428	A 5
0183	KL B	11
0184	PD428	A 8
0184	BPC328	F 8
0185	PD428	B 1
0185	BPC328	B 1
0186	PD428	B 2
0186	BPC328	C 3
0187	PD428	B 3
0187	KL B	29

NETWORK LISTING (TABULAR WIRING DIAGRAM)

TITLE
CABINET WIRING OF RECEIVER 336915

WIRING DIAGRAM	ISSUE	USED ON	DATE		
7745	1	VS269	1 2 70	PAGE	C 7 OF 7

NET	COMPONENT	PIN
0188	PD428	A 4
0188	KL A	13
0189	PD428	A 5
0189	KL A	10
0190	PD428	B 7
0190	BPC328	C 7
0191	PD428	A 8
0191	BPC328	G 8
0192	PD428	C 1
0192	BPC328	C 1
0193	PD428	C 2
0193	KL B	31
0194	PD428	C 4
0194	KL B	14
0195	PD428	C 5
0195	KL B	19
0196	PD428	C 7
0196	BPC328	C 8
0197	PD428	C 8
0197	BPC328	H 8
0198	PD428	D 1
0198	BPC328	D 1
0199	PD428	D 4
0199	KL A	15
0200	PD428	D 7
0200	BPC328	D 8
0201	PD428	D 8
0201	BPC328	A 7
0202	PD428	F 1
0202	ST A	4
0202	• KL B	1
0202	BPC328	E 1
0203	PD428	E 7
0203	BPC328	E 8
0204	PD428	E 8
0204	BPC328	B 7

NET	COMPONENT	PIN
0205	BPC328	A 4
0205	KL B	24
0206	BPC328	B 4
0206	KL B	25
0207	BPC328	C 4
0207	KL B	26
0208	BPC328	D 4
0208	KL B	27
0209	BPC328	F 2
0209	KL B	18
0210	BPC328	F 3
0210	KL B	7
0211	BPC328	F 5
0211	KL B	17
0212	BPC328	G 3
0212	KL B	8
0213	BPC328	G 5
0213	KL B	16
0214	BPC328	H 2
0214	KL B	5
0215	BPC328	H 3
0215	KL B	9
0216	BPC328	H 4
0216	KL B	28
0217	A	FR
0217	C	FR
0218	R 2	2
0218	MS T	2

NUMBER OF WIRES - 0293

END OF LISTING

NO.	NOTES

SUPPORTING INFORMATION	
CATEGORY	NO.

CONTENTS	SHEET NO.
NOTES	1
ALARM LOGIC	2
REPERFORATOR CONTROL	3
PUNCH DRIVER	4
RECEIVER CONTROL LOGIC	5
UNITS COUNTER	6
SERIAL TO PARALLEL CONVERTER	7
SERIAL TO PARALLEL CONVERTER	8
CABINET POWER	9
REPERFORATOR SHELF POWER	10
POWER SUPPLY	11

ISSUE CONTROL RECORD

SHEET NO.	ISSUE 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1	X																	
2																		
3																		
4																		
5																		
6																		
7																		
8																		
9																		
10																		
11																		

7746WD

REVISIONS APPLYING TO THIS CONTROL RECORD

ISSUE	DATE	AUTH. NO.
1	2-24-70	20615-R
2	6-4-70	585

WDP

ISSUE CONTROL SHEET 1 OF 1

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER SET
VS269

WD NUMBER	7746 WD
DRAWN DG	CHKD. [illegible]
ENGD. [illegible]	APPD. [signature]

TELETYPE
CORPORATION

7746WD

TC 482 8-65 SEE R&D ROUTINE #5 FOR USE OF THIS FORM

1. ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED

2. TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ( ) ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT

3. ALL RESISTORS 1/2 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.

4. ALL CAPACITANCE VALUES IN MICROFARADS, UNLESS OTHERWISE SPECIFIED

5. COMPONENTS ENCLOSED IN SOLID DOUBLE LINE ARE PRESENTED FOR REFERENCE ONLY. A COMPLETE SCHEMATIC OF THESE COMPONENTS IS AVAILABLE AT THE WD OR AREA INDICATED.

6. DASHED---SINGLE LINE ENCLOSING COMPONENTS INDICATES ONE CARD OR ASSEMBLY LOCATION FOR ALL THE ENCLOSED COMPONENTS.

7. THE FOLLOWING CIRCUIT CARDS ARE LOCATED IN THE FOLLOWING POSITIONS:

MODULE-C

ZC121 THRU ZC123, ZC319 THRU ZC324	303730
ZC110, ZC112, ZC116, ZC307, ZC316	303685
ZC309, ZC311	303686
ZC108	303629
ZC114, ZC115, ZC315	303688
ZC120	336906
ZC313	303626
ZC418	336908
ZC318	149248
ZC608	149254
ZC107, ZC207	149261

MODULE-D

ZD107, ZD118, ZD120, ZD303, ZD313, ZD507, ZD518, ZD520	303685
ZD103, ZD105, ZD109, ZD111, ZD113, ZD115, ZD503, ZD505, ZD509, ZD511, ZD513, ZD515	303686
ZD307, ZD317	303688
ZD122, THRU ZD124, ZD322 THRU ZD324	303689
ZD305, ZD315	303627
ZD117, ZD517	149243
ZD125, ZD525	149244
ZD226, ZD626	149248
ZD127, ZD527	149252
ZD227, ZD627	149253
ZD126, ZD526	177530
ZD308, ZD318	149261

8. SPARE CIRCUITS AVAILABLE:

MODULE C

ZC108-DYA, PAE
ZC313-PAF
ZC307-LA-ID, IE, IF
ZC316-KI
ZC107-A, C

(SEE NOTE 28 FOR MODULE D)

9. THE RESISTANCE OF ALL RELAY COILS IS IN OHMS UNLESS OTHERWISE SPECIFIED.

10. KC119-A IN MODULE C CONTAINS A 304147 RELAY.

11. ZC127 OF MODULE C CONTAINS 9 148640 POWER RESISTORS.

12. ZC128 OF MODULE C CONTAINS 9 148643 POWER DIODES.

13. FOR ADDITIONAL WIRING INFORMATION ON TAPE REPERFORATOR REFER TO DR' 7751 WD. SCHEMATIC

14.

15. ➢ INDICATES FEMALE AND ➢ INDICATES MALE TERMINAL ON CONNECTORS

16. ALL REVISION INFORMATION IS REFLECTED ON THE ISSUE CONTROL RECORD.

17. LAMP COLORS ARE CLEAR UNLESS OTHERWISE SPECIFIED.

THE SYMBOLS ON THE FOLLOWING PAGES HAVE DESIGNATIONS THAT MAKE REFERENCE TO THE BOTTOM REPERFORATOR. THE FOLLOWING TABLE GIVES THE CORRESPONDING DESIGNATIONS FOR THE UPPER REPERFORATOR.:

MODULE D

BOTTOM REPERF.	TOP REPERF.
ZD503	ZD103
ZD505	ZD105
ZD507	ZD107
ZD509	ZD109
ZD511	ZD111
ZD513	ZD113
ZD515	ZD115
ZD517	ZD117
ZD518	ZD118
ZD520	ZD120
ZD522	ZD122
ZD523	ZD123
ZD524	ZD124
ZD525	ZD125
ZD526	ZD126
ZD626	ZD226
ZD527	ZD127
ZD627	ZD227
ZD303	ZD313
ZD305	ZD315
ZD307	ZD317
ZD308	ZD318
SWD5	SWD1
SWD7	SWD3
SWD8	SWD4
SWD6	SWD2
JD428	JD328

MODULE C

18. THERE IS ONE MODULE C FOR EACH REPERFORATOR; THEREFORE, THE DESIGNATIONS FOR EACH MODULE ARE IDENTICAL.

CONTROL PANEL

BOTTOM REPERF.	TOP REPERF.
DS101	DS201
DS102	DS202
DS103	DS203
DS104	DS204
DS105	DS205
DS106	DS206
DS107	DS207
DS108	DS208
DS109	DS209
DS110	DS210
SWI01	SW201
SWI02	SW202
SWI03	SW203
SWI05	SW205
SWI06	SW206
SWI07	SW207
SWI08	SW208
SWI09	SW209
SWI10	SW210
R1	R7
R2	R8
R3	R9
R4	R10
R5	R11
R6	R12

CABINET CONNECTORS

BOTTOM REPERF.	TOP REPERF.
KLB	KLT
NB	NT
DAB	DAT
DDB	DDT
SPB	SPT
BPC328	TPC328
PD428	PD328
BPC428-A	TPC428-A
BPC428-B	TPC428-B

19. THE TERMINALS INDICATED AS "LEVEL" ON THE 149243 CIRCUIT CARD ARE "STRAPPED TO THE "INVERTED" OR "NORMAL" TERMINALS DEPENDING ON THE APPLICATION. THIS CARD MUST BE IDENTICALLY WIRED IN BOTH THE TRANSMITTER AND THE RECEIVER.

20. THE R C NETWORKS ON EACH CIRCUIT CARD ARE IDENTICAL; HOWEVER THE VALUES PER CARD ARE DEPENDENT ON THE DESIRED WAVESHAPE.

21. INDUCTANCE VALUE IN MICROHENRIES.

22. FOR ACTUAL WIRING DIAGRAMS REFER TO:

MODULE C	7731 WD
MODULE D	7732WD
VS269 CABINET	7745 WD
REPERF. SHELF	7734WD
KEY & LAMP PANEL	7735WD
MODULE C POWER SUPPLY	7736WD

REFERENCE WIRING DIAGRAMS:

ACTUAL	DRPE 811	7750WD
SCHEMATIC	DRPE 811	7751WD

23. ONLY ONE CONNECTOR IS INDICATED IN THE CASES WHERE PLUG AND RECEPTACLE ARE THE SAME OR THEY ONLY DIFFER BY A J & P. THE PIN NUMBERS ON PLUG AND RECEPTACLE ARE THE SAME

24. THE HALF ARROWS (⇀) INPUT TO A DIGITAL POTTED MODULE CIRCUIT INDICATES THAT CIRCUIT IS SENSITIVE TO A VOLTAGE OR CURRENT LEVEL AT THAT INPUT.
THE FULL ARROW (⟶) INPUT TO A DIGITAL POTTED MODULE CIRCUIT INDICATES THAT CIRCUIT IS SENSITIVE TO A VOLTAGE CHANGE OR PULSE AT THAT INPUT.

25. WHEN 15 PIN CARDS ARE USED, TWO ARE PLACED IN ONE 36 PIN CARD CONNECTOR. THE ACTUAL WD INDICATES ONLY ONE LOCATION NUMBER FOR THE ENTIRE 36 PIN CONNECTOR. THIS SCHEMATIC WD DESIGNATES A POSITION NUMBER FOR EACH CARD. EG: ZE103 ON ACTUAL WOULD BE ZE103 AND ZE203 ON SCHEMATIC DEPENDING ON LOCATION. SEE MODULE CO-ORDINATE SYSTEM.

26. CROSS REFERENCE LEGEND:
5-B2-AA
- 5 — SHEET NUMBER
- B2 — CO-ORDINATE SYSTEM
- AA — LEGEND DESIGNATION WHEN NEEDED

27. ▽ INDICATES CIRCUIT COMMON.
▽ INDICATES LAMP AND SWITCH COMMON.
THESE ARE CONNECTED TOGETHER IN MODULE C (336912)

28. SPARE CIRCUITS AVAILABLE:

MODULE D

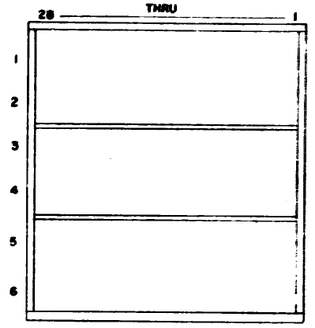
ZD103-D-F, CR-B
ZD503-D-F, CR-B
ZD105-CR-B, CR-C, CR-E, CR-F
ZD505-CR-B, CR-C, CR-E, CR-F
ZD109-D-F, CR-F
ZD509-D-F, CR-F
ZD111-D-F, CR-B, CR-C, CR-E, CR-F
ZD511-D-F, CR-B, CR-C, CR-E, CR-F
ZD113-CR-B, CR-C, CR-E, CR-F
ZD513-CR-B, CR-C, CR-E, CR-F
ZD115-CR-B, CR-C,
ZD515-CR-B, CR-C,
ZD125-10
ZD525-10
ZD126-3
ZD526-3
ZD226-K4
ZD626-K4

29. CERTAIN LOGIC SYMBOLS USED ON THIS WIRING DIAGRAM DO NOT CONFORM TO TELETYPE DESIGN STANDARDS. THE SYMBOLS ARE EXPLAINED ON THE RESPECTIVE CIRCUIT CARD DRAWINGS.

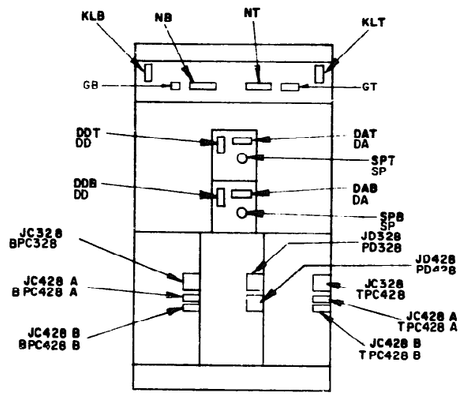
30. WIRING TO PUSHBUTTON LIGHT SOCKETS HAS BEEN PROVIDED.

31. THE FOLLOWING FROM TO CONNECTIONS ARE SPARE WIRES PROVIDED IN THE CABINET CABLE.

FROM		TO		
BPC328	A1	DA	B	17
BPC328	A2	DA	B	18
BPC328	B1	PD428		B1
BPC328	D1	PD428		D1
BPC328	E2	N	B	27
BPC328	F2	KL	B	18
PD428	A1	N	B	21
PD428	A2	N	B	23



COORDINATE SYSTEM
VIEWED FROM WIRING SIDE



CONNECTOR LOCATION IN RECEIVER CABINET
VIEWED FROM REAR
VS 269

7746WD		
REVISIONS		
ISSUE	DATE	AUTH
	2-24-70	20613-R

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD

SHEET 1

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER SET
VS 269

APPROVALS

D AND R	E OF M

E-NUMBER	
PROD. NO.	7746 WD
DATE	11-1-69
P.D. FILE NO.	38-A2/65AA
DRAWN DQ	CHKD.
ENGD. EJH	APPD.

TELETYPE CORPORATION

7746WD

TC 484-5-69

"SEE SHEET 1 FOR NOTES."

ALARM LOGIC - MOD. C

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD. WHICH IS A PART OF THIS DRAWING

7746WD		
REVISIONS		
ISSUE	DATE	AUTH. NO.
1	2-24-70	2083-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD

SHEET 2

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER SET
VS 269

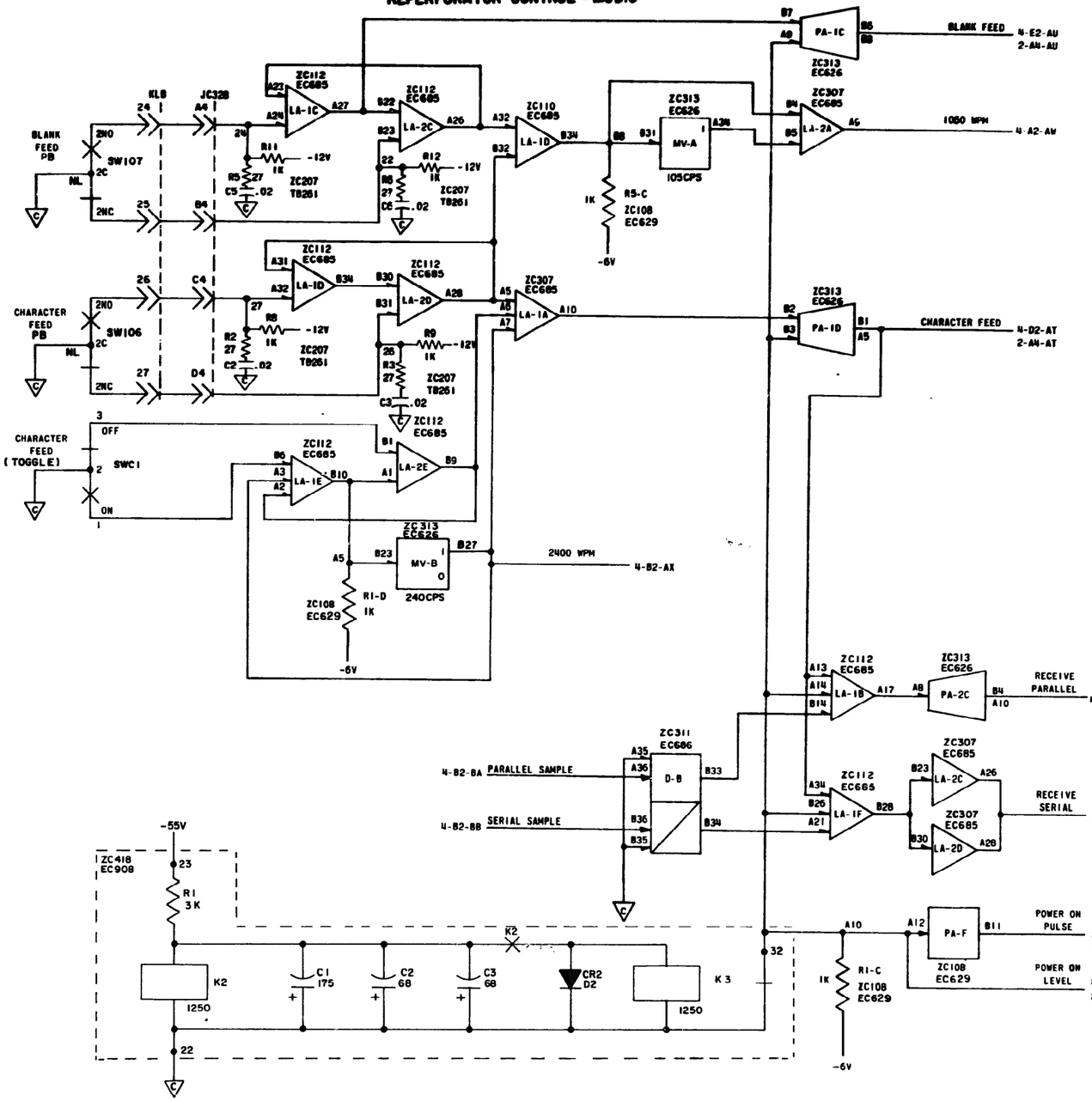
APPROVALS	
D AND R	E OF M
E-NUMBER	
PROD. NO. 7746 WD	
DATE 11-1-69	
P.D. FILE NO. 38-A2/65AA	
DRAWN D Q	CHKD.
ENGD. E J H	APPD.

TELETYPE CORPORATION

7746WD

SEE SHEET 1 FOR NOTES.

REPERFORATOR CONTROL - MOD.C



7746WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	2-24-70	20613-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD SHEET 3

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER SET
VS 269

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 7746 WD

DATE 11-1-69

P.D. FILE NO. 38-A2/65AA

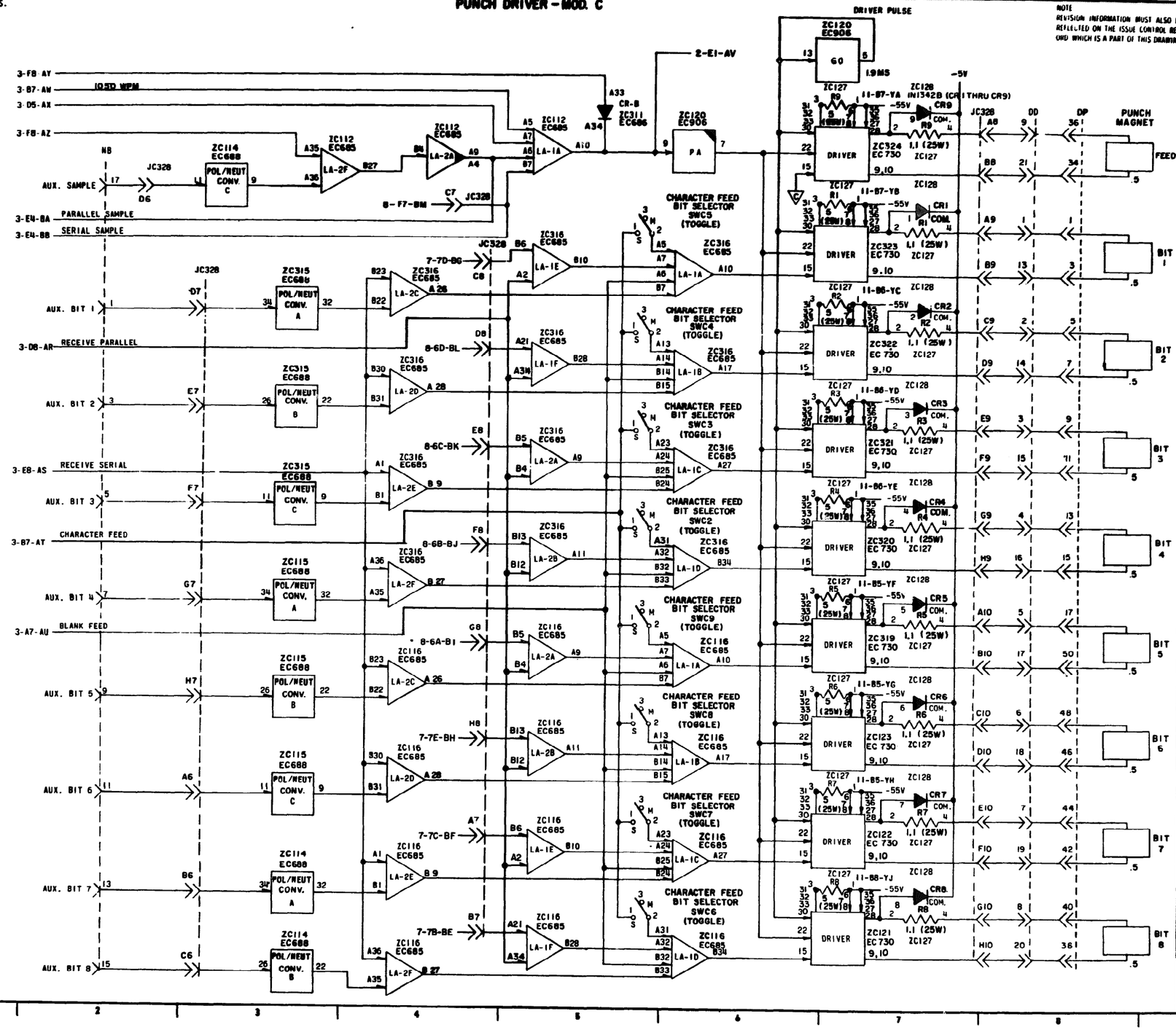
DRAWN DQ	CHKD.
ENGD. EJH	APPD.

TELETYPE CORPORATION

7746WD

SEE SHEET 1 FOR NOTES.

PUNCH DRIVER - MOD. C



NOTE
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD WHICH IS A PART OF THIS DRAWING

7746WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	2-24-70	2985-R

WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD SHEET 4

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER SET
VS 269

APPROVALS

D AND R	E OF M
LDM	

E-NUMBER	
PROD. NO.	7746 WD
DATE	11-1-69
P.D. FILE NO.	38-A2/65AA
DRAWN DQ	CHKD.
ENGD. EJH	APPD.

TELETYPE CORPORATION

7746WD

SEE SHEET 1 FOR NOTES.

RECEIVER CONTROL LOGIC - MOD. D

NOTE : REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD. WHICH IS A PART OF THIS DRAWING

7746WD		
REVISIONS		
ISSUE	DATE	AUTH. NO.
1	2-24-70	20613-R

CLOCK — NB — 20 — JD428 D6 — ZD307 EC688 POL/NEUT CONV. A — 34 — 32 — ZD507 EC685 LA-2A — B4 — A9 — ZD807 EC685 LA-28 — B12 — A11 — ZD305 EC627 PA-F — A12 — B11 — BIT SHIFT — 7-AN-AC

6-B8-AH — CLOCK

DATA IN — 22 — E6 — ZD307 EC688 POL/NEUT CONV. B — 26 — 22 — ZD507 EC685 LA-2C — B23 — A26 — B21

7-FI-AB

7-EI-AA — ZD507 EC685 LA-2D — A28 — B30

ZD505 EC686 D-B — A35 — A36 — B35 — B33 — B34

ZD505 EC686 D-C — A24 — B24 — A25 — B25 — B26

CHARACTER SYNC. PRIME — 6-A5-AG

6-EI-AE — DELAYED CHARACTER SHIFT

6-B7-AF — SYNC. PRIME

ZD505 EC686 D — B6 — A8

ZD505 EC686 D-E — A12 — A11 — B12 — B11 — B9 — B10

ZD507 EC685 LA-2F — A36 — A35 — B27

ZD505 EC686 U-F — A2 — A1 — B1 — B2 — A10 — B3

ZD303 EC685 LA-1F — A34 — A21 — B28

ZD303 EC685 LA-2F — A36 — A35 — B27 — A33

KLB — 14 — C4 — 2NO — 2C — NL — 2NC — MANUAL SYNC. PB — SW108

15 — D4

R6 27 — C6 .02 — ZD308 TB261 — R2 1K — -12V

R5 27 — C5 .02 — R1 1K — -12V

MANUAL SYNC. DS108 — NOTE 30 — R3 150 1W — SW108 — 1C — 1NO — NL — -12V

ZD520 EC685 LA-2B — B12 — B13 — A11 — IN SYNC. 7-E8-AI

ZD505 EC686 D-D — B14 — B13 — A23 — A22 — B23 — B22

ZD505 EC686 D — B28 — A28

ZD303 EC685 LA-1D — A31 — A32 — B34

ZD303 EC685 LA-1E — A2 — B10 — B6 — B17

AUTO.-MAN. SYNC. MODE PB — SW109 — 2NO — 2C — NL — 2NC — 12 — A4 — 13 — B4

R10 1K — J4 27 — C4 .02 — ZD308 TB261 — -12V

JD428 — 5 — R3 27 — C3 .02 — R8 1K — ZD308 TB261 — -12V

6-FI-AP — CHAR. SHIFT — A1

ZD507 EC685 LA-2E — B17 — B9

ZD307 EC688 POL/NEUT CONV. C — URGENT TRAFFIC — NB — 26 — E5 — JD428 — 11 — 9 — A31 — B34

ZD520 EC685 LA-1D — A31 — B34 — A2 — B10

ZD520 EC685 LA-1E — A2 — B10

ZD308 TB261 — R8 1K — -12V

KLB — 31 — C2 — JD428 — 2NC — 2C — NL — SW105 — URGENT TRAFFIC PB — 2NO — 29 — B3

R2 27 — C2 .02 — ZD308 TB261 — 6 — -12V

ZD520 EC685 LA-1B — A14 — A13 — A17

ZD520 EC685 LA-1C — A24 — A23 — A27

R7 1K — R2 27 — C1 .02 — ZD308 TB261 — -12V

ZD515 EC686 D-D — B14 — B13 — A22 — B23 — B22

ZD305 EC627 PA-1D — B2 — B1

ZD305 EC627 PA-2D — A3 — A1

ZD305 EC627 PA-2C — A8 — B4

ZD626 TB248 CR1 D2 — K1 — 1250 — 26 — 31 — R1 220 1W — 27 K1 34 — -12V

CR2 D2 — K2 — 1250 — 30 — 31 — R2 220 1W — 25 K2 35 — -12V

CR3 D2 — K3 — 1250 — 36 — 31 — R3 220 1W — 24 K3 33 — -12V

JD428 — A5 — 11 — KLB — B5 — 10 — C5 — 19

AUTOMATIC SYNC. MODE DS109 — C — D — G — L

MANUAL SYNC. MODE DS109 — A — B — G — L

URGENT TRAFFIC DS105 — R — B — D — G — L

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD

SHEET 5

SCHEMATIC WIRING DIAGRAM FOR RECEIVER SET VS 269

APPROVALS	
D AND R	E OF M
E-NUMBER	
PROD. NO. 7746 WD	
DATE 11-1-69	
P.D. FILE NO. 38-A2/65AA	
DRAWN D Q	CHKD.
ENGD. E J H	APPD.

TELETYPE CORPORATION

7746WD

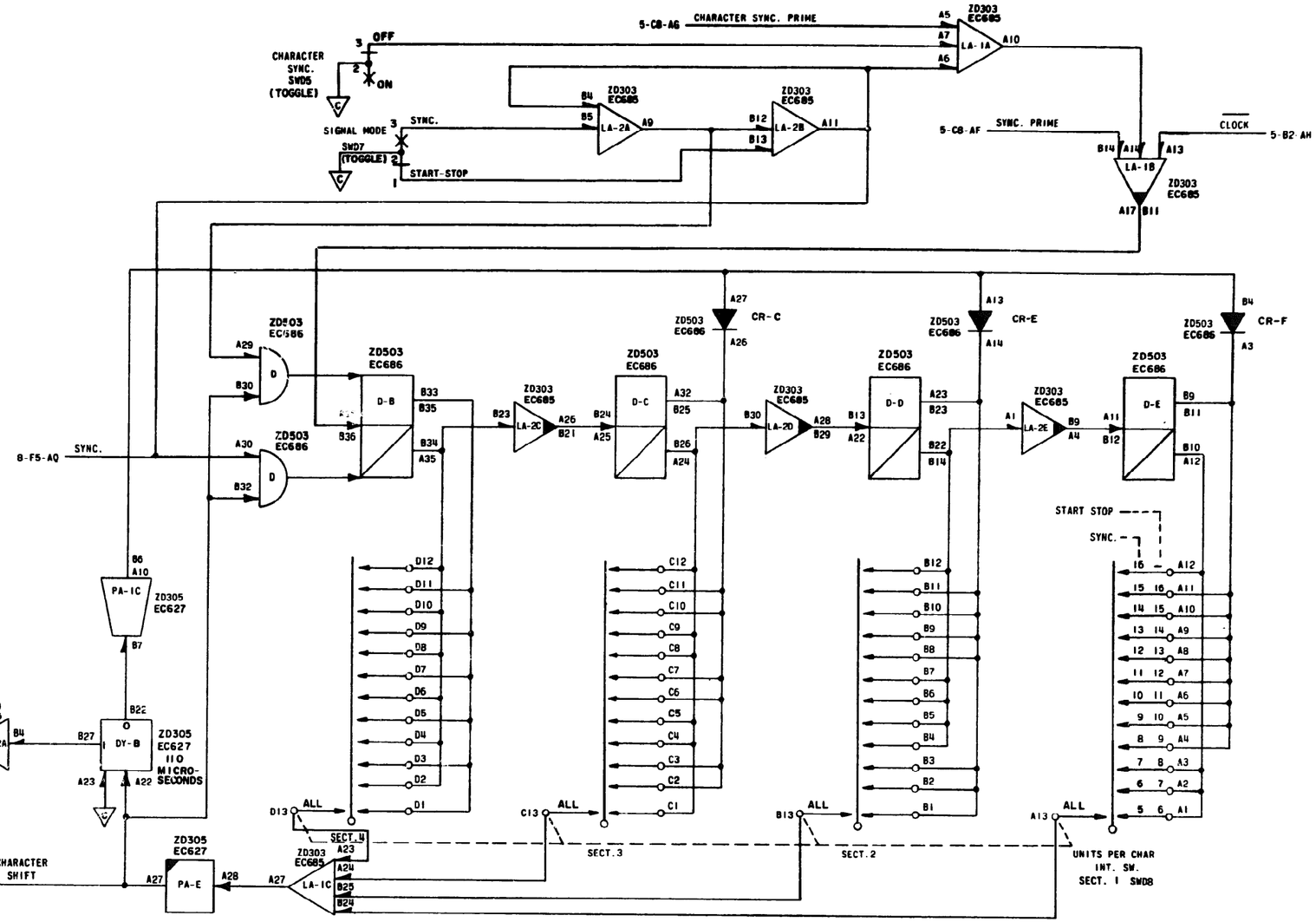
SEE SHEET 1 FOR NOTES.

UNITS COUNTER - MOD. D

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD WHICH IS A PART OF THIS DRAWING

7746WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	2-24-70	20613-R



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD
SHEET 6

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER SET
VS 269

APPROVALS	
D AND R	E OF M
LEM	

E-NUMBER	
PROD. NO.	7746 WD
DATE	11 - 1 - 69
R.D. FILE NO.	38-A2/65AA
DRAWN D Q	CHKD.
ENGD. E J H	APPD.

TELETYPE CORPORATION

7746WD

SEE SHEET 1 FOR NOTES.

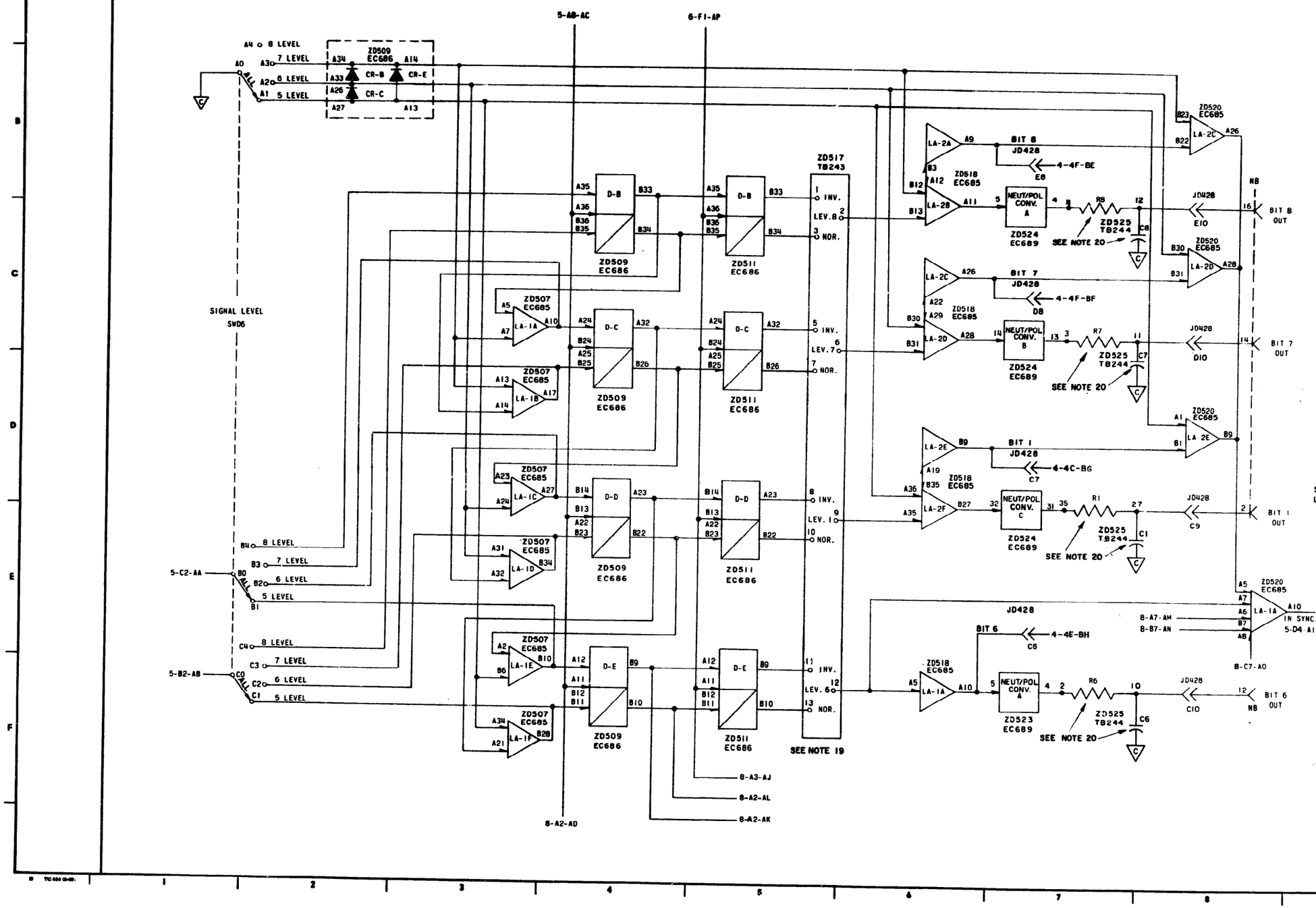
SERIAL TO PARALLEL CONVERTER - MOD. D

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD WHICH IS A PART OF THIS DRAWING

7746WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	2-24-70	2065-R



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD

SHEET 7

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER SET
VS 269

APPROVALS

D AND R	E OF M
LDm	

E-NUMBER	
PROD. NO.	7746 WD
DATE	11 - 1 - 69
P.D. FILE NO.	38-A2/65AA
DRAWN D Q	CHKD.
ENGD. E J H	APPD.

TELETYPE CORPORATION

7746WD

SEE SHEET 1 FOR NOTES.

SERIAL TO PARALLEL CONVERTER-MOD. D

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD WHICH IS A PART OF THIS DRAWING

7746WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	2-24-70	20613-A

7-F5-AJ

7-F5-AK
7-F4 AD
7-F5-AL

ZD513 EC686 D-B
ZD515 EC686 D-B
ZD517 TB243
22 INV.
23 LEV.5
24 NOR.

ZD518 EC685 LA-1B
ZD523 EC689 NEUT/POL CONV. B
BIT 5
JD428 4-4E-B1
SEE NOTE 20
ZD525 TB244 C5
JD428 B10 BIT 5 OUT NB 10

7-E8-AN

ZD513 EC686 D-C
ZD515 EC686 D-C
25 INV.
26 LEV.4
27 NOR.
ZD518 EC685 LA-1C
ZD523 EC689 NEUT/POL CONV. C
BIT 4
JD428 4-4D-BJ A8
SEE NOTE 20
ZD525 TB244 C4
A10 BIT 4 OUT 8

ZD513 EC686 D-E
ZD515 EC686 D-E
28 INV.
29 LEV.3
30 NOR.
ZD518 EC685 LA-1D
ZD522 EC689 NEUT/POL CONV. A
BIT 3
JD428 4-4D-BK E7
SEE NOTE 20
ZD525 TB244 C3
E9 BIT 3 OUT 6

ZD515 EC686 CR-E
7-E8-AO
ZD515 EC686 CR-F
JD428 4-4C-BL D7
BIT 2

ZD513 EC686 D-F
ZD515 EC686 D-F
31 INV.
32 LEV.2
33 NOR
ZD518 EC685 LA-1E
ZD522 EC689 NEUT/POL CONV. B
SEE NOTE 20
ZD525 TB244 C2
D9 BIT 2 OUT 4

ZD513 EC686 D-D
34 INV.
35 START
36 NOR.
SEE NOTE 19

ZD520 EC685 LA-1F
JD428 4-4B-BM B7
SERIAL SAMPLE

ZD518 EC685 LA-1F
ZD520 EC685 LA-2F
ZD305 EC627 DY-A
2 MILLISECONDS
SYNC.
6-D2-AQ

ZD522 EC689 NEUT/POL CONV. C
SEE NOTE 20
ZD525 TB244 C9
B9 CHARACTER AVAILABLE 18

ZD527 TB252
ZD627 TB253
-6V
+6V
ALL CAP. 5 100 V.
ALL CAP. 175 15 V.

JD428 E1 -12V.

ZD526 EC530 FILTER
+6V
-6V
+6V EXTERNAL
-6V EXTERNAL
NB 28
30
ZD307-14
ZD307-24
CKT. GRD. B2
FR. GRD. D2

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD
SHEET 8

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER SET
VS 269

APPROVALS

D AND R	E OF M
LDM	

E-NUMBER
PROD. NO. 7746 WD
DATE 11-1-69
P.D. FILE NO. 38-A2/65AA
DRAWN DQ CHKD
ENGD. EJH APPD.

TELETYPE CORPORATION

7746WD

SEE SHEET 1 FOR NOTES.

CABINET POWER

NOTE:
REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD WHICH IS A PART OF THIS DRAWING

7746WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	2-24-70	20613-R

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD
SHEET 9

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER SET
VS 269

APPROVALS

D AND R	E OF M
LDM	

E-NUMBER

PROD. NO. 7746 WD

DATE 11-1-69

P.D. FILE NO. 38-A2/65AA

DRAWN DQ | CHKD

ENGD. EJH | APPD.

TELETYPE
CORPORATION

7746WD

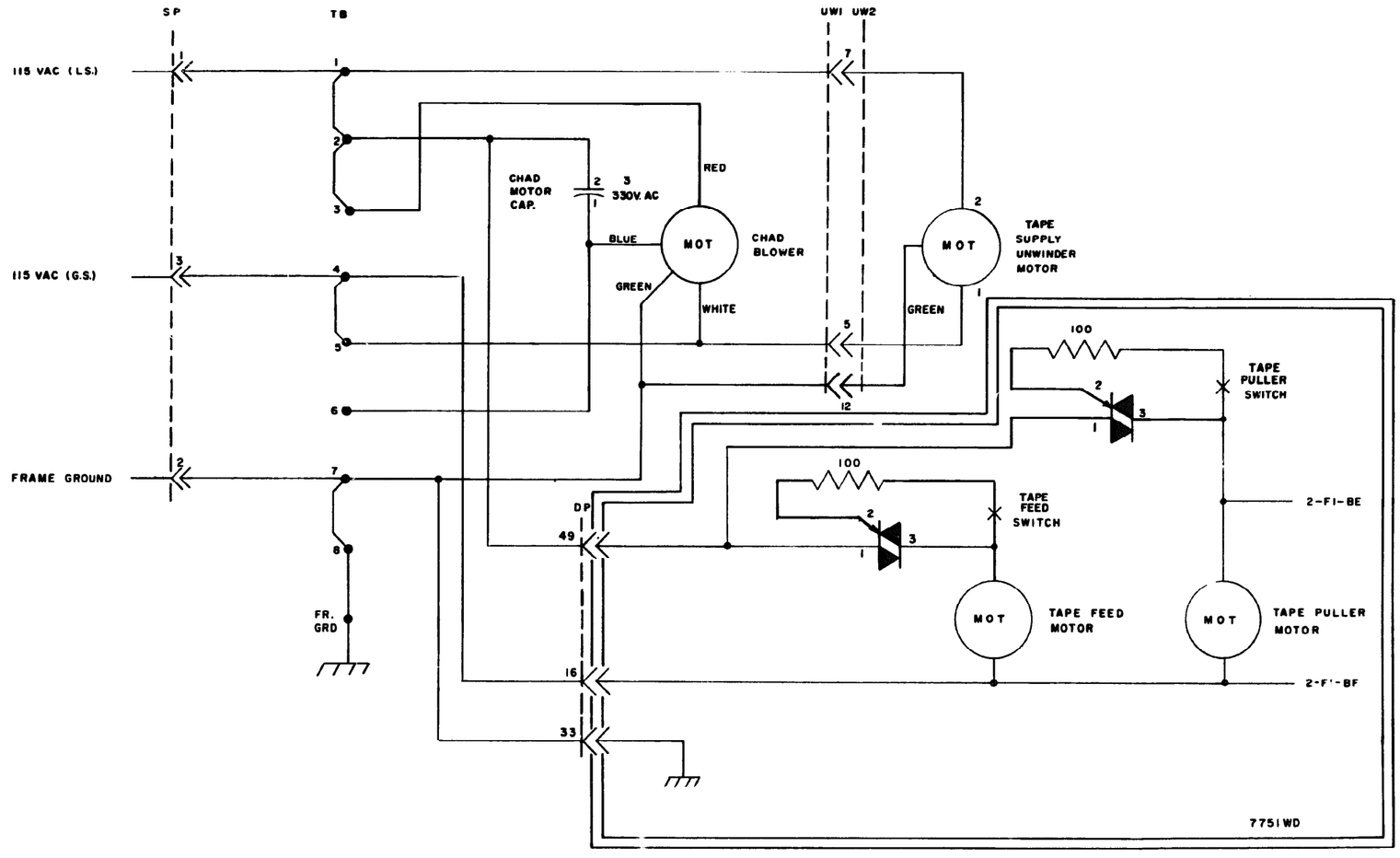
SEE SHEET 1 FOR NOTES

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD WHICH IS A PART OF THIS DRAWING

7746WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	2-24-70	20613-R

REPERFORATOR SHELF POWER.



SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS W D

SHEET 10 WDP

SCHEMATIC
WIRING DIAGRAM
FOR
RECEIVER S:
VS 269

APPROVALS	
D AND R	E OF M
LDM	~

E-NUMBER

PROD. NO. 7746 WD

DATE 11-1-69

P.D. FILE NO. 38-A2/65AA

DRAWN	CHKD.
D Q	
ENGD.	APPD.
E J H	

TELETYPE CORPORATION

7746WD

TC 454.1E-69

SEE SHEET 1 FOR NOTES.

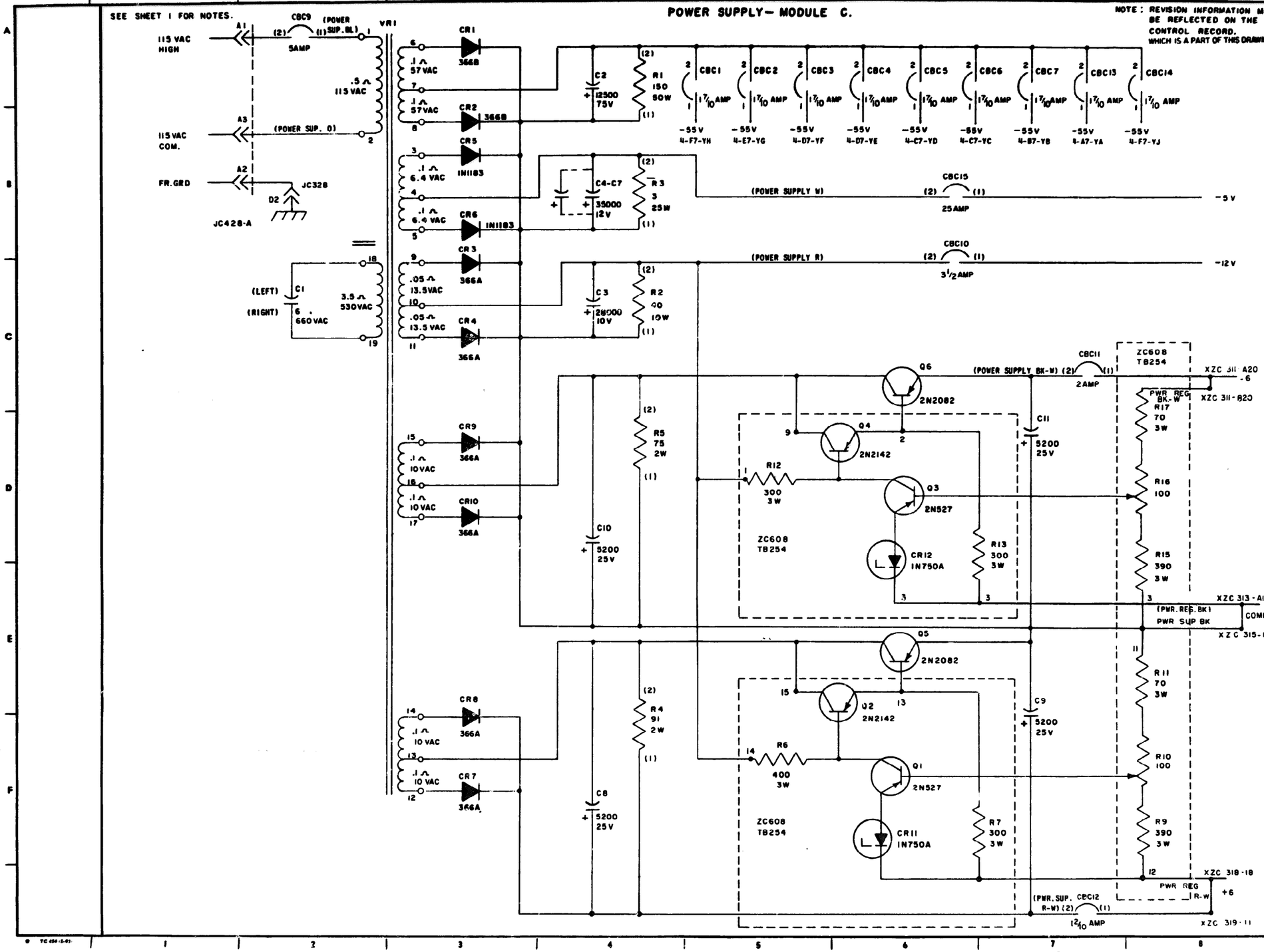
POWER SUPPLY— MODULE C.

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD, WHICH IS A PART OF THIS DRAWING

7746WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	2-24-70	20815-R



WDP

SEE ISSUE CONTROL RECORD FOR COMPLETE LIST OF SHEETS COMPRISING THIS WD

SHEET 11

SCHEMATIC WIRING DIAGRAM FOR RECEIVER SET VS 269

APPROVALS

D AND R	E OF M
LRM	

E-NUMBER	
PROD. NO.	7746 WD
DATE	11-1-69
P.D. FILE NO.	38-A2/65AA
DRAWN DQ	CHKD.
ENGD. EJH	APPD.

TELETYPE CORPORATION

7746WD

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	2-11-70	20668-A

CIRCUIT CARD SPECIFICATION

TEMPERATURE RANGE OPERATION— 40°F TO 150°F STORAGE— -50°F TO 185°F NO AIR FLOW REQUIRED

HUMIDITY RANGE - 0 TO 95 REL HUM

SUPPLY VOLTAGES

VOLTAGE	PIN	MIN.	MAX	MAX CURRENT	MAX RIPPLE	COMMENTS
-6V	3	-5.4V	-6.6V	10 MA	2%	
+6V	11	+5.4	+6.6	20 MA	2%	
-12V	26	-11.2V	-12.8V	40 MA	2%	
GRD.	36	-0.1V	+0.1V	100 MA		

INPUTS

NAME	PIN	V_{T-0}	V_{T+0}	T_{RISE}	T_{FALL}	WIDTH	RELATIONSHIP TO INPUTS	INPUT IMPEDANCE	WHEN NOT USED	REPETITION RATE	COMMENTS
POWER AMPLIFIER	9	-4.0V TO -6.5V	-0.5V TO 0.0V	< 1μs	< 10μs	>10μs	DRPE APPLICATION: GOES HIGH UP TO 10μS BEFORE PIN 13 GOES LOW.	1 K OHMS TO - 6V	WITH INPUT OPEN, OUTPUT REMAINS LOW	4.17 MS MAX.	
GATED OSCILLATOR	13	-0.5V TO +1.0V	-4.0V TO -6.5V	< 1μs	< 10μs	NOTE 2	DRPE APPLICATION: GOES LOW UP TO 10μS AFTER PIN 9 GOES HIGH.	10 K OHMS TO GRD	WITH INPUT OPEN, OUTPUT REMAINS LOW.	4.17 MS MAX.	THE GATED OSCILLATOR INPUT IS NORMALLY SUPPLIED BY THE OUTPUT, PIN 30, OF THE MAGNET DRIVER CARD 303730. THIS OUTPUT IS - 12 VOLTS THROUGH A 3900 OHM RESISTOR, AS A RESULT THE VOLTAGE AT THE INPUT IS AS SHOWN.

OUTPUTS

NAME	PIN	V_{T-0}	V_{T+0}	T_{RISE}	T_{FALL}	WIDTH	RELATIONSHIP TO INPUTS/OUTPUTS	LOADING	WHEN NOT USED	COMMENTS
POWER AMPLIFIER	7	-4.9V TO -6.1V	-0.5V TO 0.0V	< 1μs	<10μs	>10μs	PROVIDES A NON-INVERTED OUTPUT WITH RESPECT TO THE INPUT, PIN 9	22 K OHMS TO GRD.		CAPABLE OF SUPPLYING 80 MA MAX. WHEN Q4 IS CONDUCTING. HELD AT GROUND FOR APPROXIMATELY 40 M.S. ON POWER TURN ON.
GATED OSCILLATOR	5	-0.5V TO +1.0V	-4.0V TO -6.5V	< 1μs	<10μs	NOTE 2	REFER TO NOTE 2	3K OHMS TO - 12V		CAPABLE OF SUPPLYING 100 MA MAX. WHEN Q3 IS CONDUCTING

NOTES

1. DEFINITIONS:
   - V_{T-0} - THE VOLTAGE BEFORE ACTIVATION.
   - V_{T+0} - THE VOLTAGE AFTER ACTIVATION.
   - < - LESS THAN
   - > - GREATER THAN
   - T_{RISE} - TIME REQUIRED FOR THE INSTANTANEOUS AMPLITUDE TO GO FROM 10% TO 90% OF THE MAXIMUM VALUE.
   - T_{FALL} - TIME REQUIRED FOR THE INSTANTANEOUS AMPLITUDE TO GO FROM 90% TO 10% OF THE MAXIMUM VALUE.
   - WIDTH - TIME REQUIRED FOR THE INSTANTANEOUS AMPLITUDE TO GO FROM THE 50% POINT OF THE LEADING EDGE THROUGH THE MAXIMUM VALUE AND RETURN TO THE 50% LEVEL OF THE TRAILING EDGE.
2. INPUT, PIN 13, IS CONNECTED TO OUTPUT, PIN 5, AND THE OSCILLATOR IS ADJUSTED TO GIVE A PULSE WIDTH OF 1.9MS ± 0.05 MS (DRPE APPLICATION)

ISSUE CONTROL

CONTENTS	SHEET NO	ISSUE NO 1	2	3	4	5	6	7	8	9	10	11	12
CIRCUIT CARD SPECIFICATION	1												
CIRCUIT CARD ASSEMBLY	2												

EC906
336906
LOGIC
CARD

APPROVALS		
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

ENGR. EJH DSGNR. R M S

DRN. E. Q. DATE 10-28-69

R&D FILE 38 A2/65AA

S-NUMBER

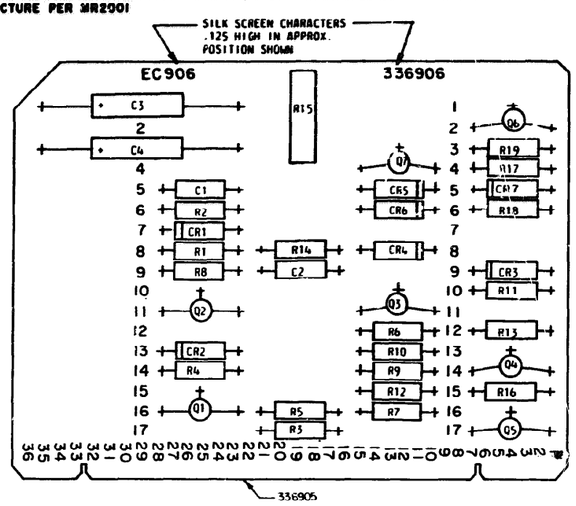
TELETYPE

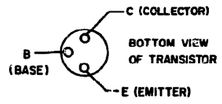
336906 (1)

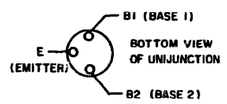
TC 434 (3-69)

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
R1	143669	1	RESISTOR 360 OHMS
R2	118180	2	RESISTOR 10K OHMS
R3			SAME AS R2
R4	137441	3	RESISTOR 1200 OHMS
R5	118153	2	RESISTOR 33K OHMS
R6			SAME AS R4
R7			SAME AS R4
R8	137602	1	RESISTOR 470 OHMS
R9	143667	1	RESISTOR 3900 OHMS
R10	118151	1	RESISTOR 18K OHMS
R11			SAME AS R5
R12	118177	1	RESISTOR 22K OHMS
R13	137440	3	RESISTOR 1K OHMS
R14	118154	1	RESISTOR 47K OHMS
R15	148836	1	POTENTIOMETER 20K OHMS
R16			SAME AS R13
R17			SAME AS R13
R18	118727	1	RESISTOR 47 OHMS
R19	118724	1	RESISTOR 220 OHMS
C1	148833	1	CAPACITOR .1 MFD.
C2	137311	1	CAPACITOR .02 MFD.
C3	146736	2	CAPACITOR 175 MFD. 15VDC
C4			SAME AS C3
CR1	177404	1	DIODE ZENER 1N965A 15V
CR2	177611	5	DIODE SILICON 1N682
CR3			SAME AS CR2
CR4			SAME AS CR2
CR5			SAME AS CR2
CR6			SAME AS CR2
CR7	181667	1	DIODE ZENER 4.7V
Q1	177105	6	TRANSISTOR P22
Q2	177610	1	TRANSISTOR 2N1671
Q3			SAME AS Q1
Q4			SAME AS Q1
Q5			SAME AS Q1
Q6			SAME AS Q1
Q7			SAME AS Q1
	144495	7	TRANSISTOR PADS
	300116	2	TRANSISTOR CAPS Q6,Q7
	336905	1	ETCHED CARD

NOTE: MANUFACTURE PER MR2001







THE POWER AMPLIFIER PROVIDES A NON-INVERTED NOMINAL OUTPUT OF 0 V AND -5.45V AMPLITUDE. IT IS CAPABLE OF SUPPLYING 80 MA WHEN Q4 IS ON.

WITH 0V APPLIED TO PIN 9, Q3 CUTS-OFF. THIS CAUSES Q4 TO CONDUCT, WHICH PLACES THE OUTPUT PIN 7 AT 0V. WITH -6V APPLIED TO PIN 9,Q3 CONDUCTS. THIS HOLDS Q4 CUT-OFF, WHICH CAUSES THE OUTPUT TO BE-5.45V.

THE OUTPUT IS -5.45V. BECAUSE OF THE AMPLITUDE LIMITING RESISTOR R13, WHICH ALLOWS CURRENT TO FLOW THROUGH R7 EVEN THOUGH Q4 IS CUT-OFF.

THE GATED OSCILLATOR PROVIDES SWITCHING OF THE OUTPUT TRANSISTOR (Q5) ACCORDING TO A SET TIME CONSTANT (DETERMINED BY THE SETTING OF R15).

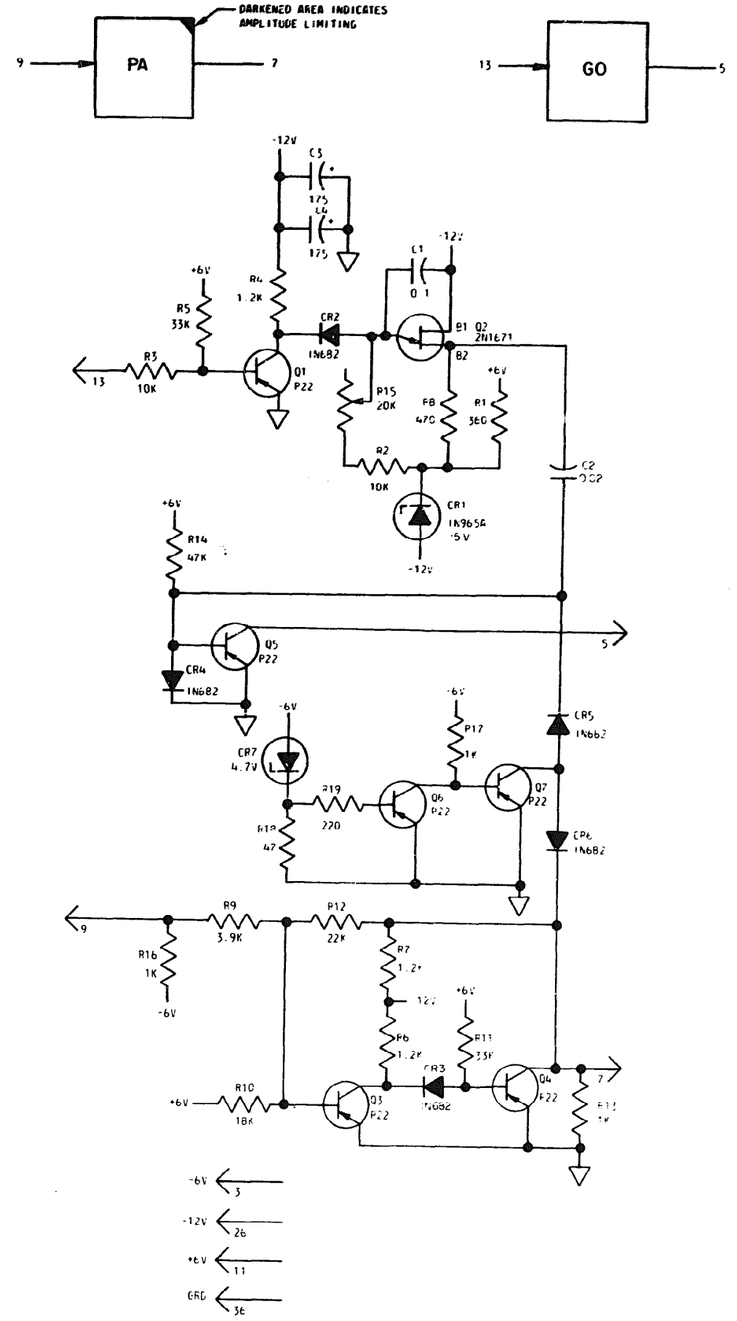
WHEN PIN 13 IS AT 0V.,Q1 IS CUT-OFF. CR2 IS THUS FOFWARD BIASED. THIS HOLDS THE EMITTER OF Q2 AT A CONSTANT -12V.C1 CANNOT CHARGE. THUS, Q5 IS NOT CONDUCTING.

WHEN PIN 13 IS AT -6V.,Q1 IS CONDUCTING,CR2 IS REVERSE BIASED,C1 CAN NOW CHARGE THROUGH R15,R2,R1. WHEN THE VOLTAGE ACROSS C1 REACHES A CERTAIN VALUE, Q2 WILL CONDUCT. A NEGATIVE PULSE APPEARS AT THE BASE OF Q5 CAUSING Q5 TO CONDUCT EVERY TIME THIS PULSE OCCURS. WHEN THIS PULSE IS NO LONGER PRESENT, Q5 CUTS-OFF.

THE EC906 CIRCUIT CARD WAS DESIGNED TO OPERATE IN CONJUNCTION WITH THE EC672 OR EC730 MAGNET DRIVER CIRCUIT CARDS. THE POWER AMPLIFIER SECTION SUPPLIES A CHARACTER SAMPLE PULSE TO PIN 22 OF THE MAGNET DRIVER CARD. THE GATED OSCILLATOR SECTION SUPPLIES A TIMED RESET PULSE TO PIN 30 OF THE MAGNET DRIVER CARD 1.9 MS AFTER RECEIVING A NEGATIVE GOING INDICATION FROM THE SAME PIN (I.E. THE OUTPUT, PIN 5, OF THE GATED OSCILLATOR IS CONNECTED TO ITS OUTPUT,PIN 13) REFER TO SHEET 2 FOR A DETAILED DESCRIPTION OF CIRCUIT CHARACTERISTICS.

Q6 AND Q7 CONSTITUTE A POWER ON RESET CIRCUIT. AS THE 6 VOLT SUPPLY BUILDS UP AFTER POWER TURN ON, Q7 CONDUCTS, ITS COLLECTOR IS AT GROUND POTENTIAL AND THE PA AND GO OUTPUT ARE HELD AT 0V. WHEN THE -6 VOLT SUPPLY REACHES THE BREAKDOWN VOLTAGE OF CR7 (4.7V) Q6 BECOMES CONDUCTIVE AND CUTS OFF Q7. CONTROL OF THE PA AND GO OUTPUT IS RELEASED TO THEIR RESPECTIVE INPUTS.

SIMILAR TO: 303690



REVISIONS		
ISSUE	DATE	AUTH NO.
1	2-11-70	20566-R

CIRCUIT CARD
EC 906
336906
LOGIC
CARD

APPROVALS		
PROJ SUPV.	PROJ DIR	MFG. REL. COMPL.
ENGR F. J. H	DSGNR. R. M. S.	
DRN. E. S	DATE	
E-NUMBER		
SD-CD NO		
R&D FILE 38-A2/650A		

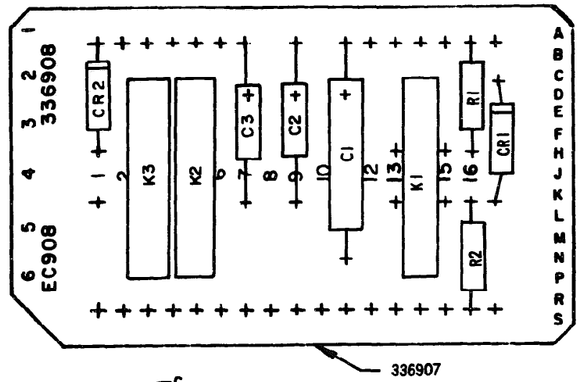
TELETYPE

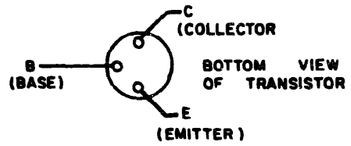
336906(2 OF 2)

TC 637 (3-69)

EC908

336908





NOTE:
REFER TO 5016 WD FOR MARKING IMFORMATION.

ALPHA NUMERIC CONVERSION CHART

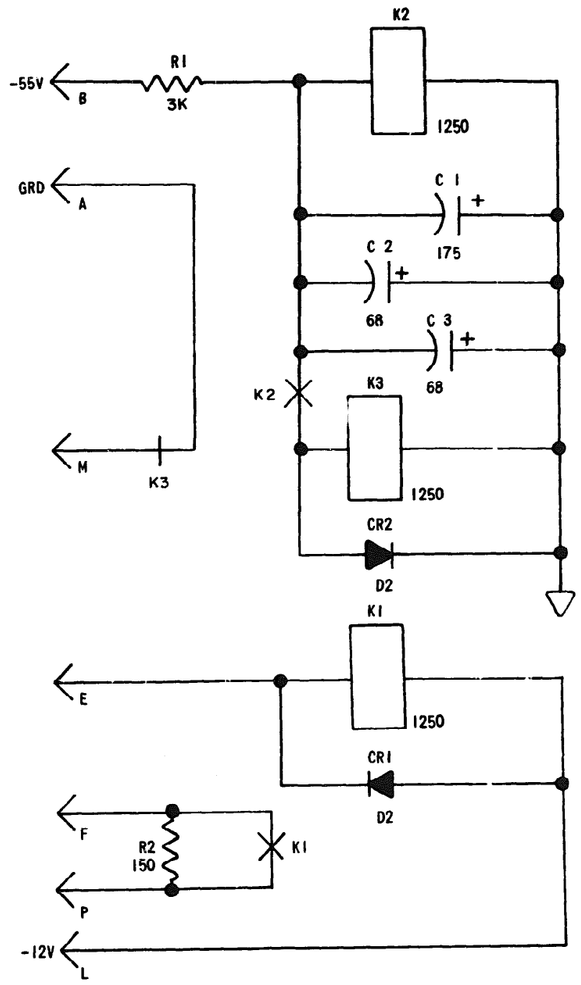
STAMPING ON CIRCUIT BOARD	NUMERICAL CONVERSION FOR 15 PT. CARDS WHEN USED WITH 36 PT. CONNECTOR	
	WHEN INSERTED IN UPPER HALF OF CONNECTOR	WHEN INSERTED IN LOWER HALF OF CONNECTOR
A	1	22
B	2	23
C	3	24
D	4	25
E	5	26
F	6	27
H	7	28
J	8	29
K	9	30
L	10	31
M	11	32
N	12	33
P	13	34
R	14	35
S	15	36

REF. DESIGN.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
K1	306843	2	RELAY, REED MAKE 12 VOLT	
K2			SAME AS K1	
K3	306844	1	RELAY, REED BREAK 12 VOLT	
CR1	177108	2	DIODE D2	
CR2			SAME AS CR1	
R1	171588	1	RESISTOR, FIXED 3K OHMS 1/2 WATT.	
R2	310988	1	RESISTOR, FIXED 150 OHMS 1 WATT.	
C1	146736	1	CAPACITOR, 175 MFD 15 VOLT	
C2	306088	2	CAPACITOR, 68 MFD 15 VOLT	
C3			SAME AS C2	
EC	336907	1	ETCHED CIRCUIT BOARD	

TC-473 (6-66)

CIRCUIT BOARD EC908

SYMBOLS



NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS.

336908

REVISIONS

ISSUE	DATE	AUTH. NO.
1	2-11-70	20566-R

APPROVALS

R AND D	E OF M
LDM	

E-NUMBER.

PROD. NO. 336908

DATE 11-1-69

FILE NO. 38-A2/65AA

DRAWN. D.Q. CHKD.

ENGD. E.J.H. APPD.

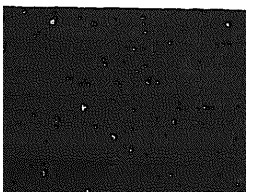
TELETYPE CORPORATION

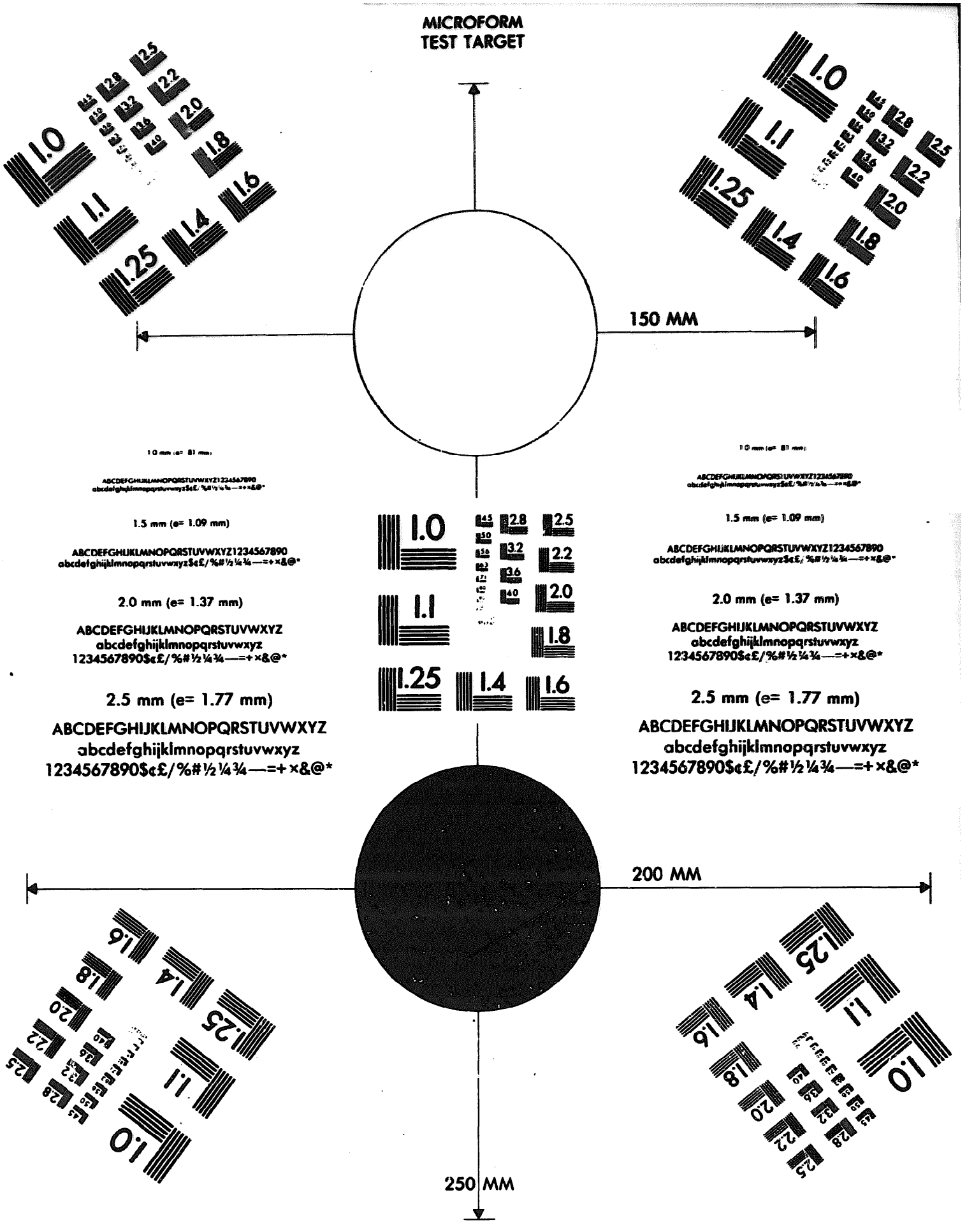
336908

END

11-19-82

DATE




MICROFORM
TEST TARGET
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1.5 mm (e= 1.09 mm)
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2.0 mm (e= 1.37 mm)
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*
2.5 mm (e= 1.77 mm)
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*
200 MM
250 MM