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BULLETIN 302B
VOL 1 OF 3

TECHNICAL MANUAL
MASTER AND SUPPLEMENTARY HIGH SPEED TAPE SENDER, AND HIGH SPEED TAPE RECEIVER FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

(A MODEL)

This publication *replaces* all previously dated Army and Navy manuals, and the Air Force TO 31W4-2FG-1351 Vol 4 of 6 In part.

TELETYPE®
CORPORATION
5555 TOUHY AVENUE, SKOKIE, ILLINOIS

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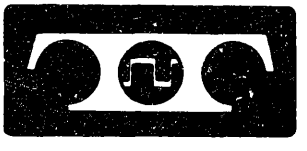
READER PLEASE NOTE: As of 8 September 1971, this BULLETIN consists of five volumes.



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MARCH 1972

INTRODUCTION

Bulletin 302B is a technical manual for the Master and Supplementary High Speed Tape Sender, and High Seed Tape Receiver used in the Multiple **Address** Processing System (MAPS).

This bulletin now consists of three volumes. Volume 1 contains the Master, Supplementary, and Receiver sections, which provide description and theory of operation, installation, troubleshooting, adjustments, removal and replacement of components, and lubrication. Volume 1 must be used in conjunction with Bulletins 279B Technical Manual High Speed Tape Punch (DRPE), and 301B High Speed Tape Reader (DX Type).

Volume 2 contains the master sender wiring diagrams, (actuals, circuit cards, and schematics). Volume 3 contains the supplementary sender, and receiver cabinet wiring diagrams, (actuals, circuit cards, and schematics).

Eachvolume is made up of a group of individualsections. The sections are separately identified by title and section number, and the pages are numbered consecutively, independent of other sections. The identifying nine-digit number appears on each page of the section in the upper right-hand corner of right-hand pages, and in the upper left-comer of left-hand pages.

To locate specific information, refer to the table of contents on the following page. Look for the name of the equipment involved in the heft-handcolumn, the associated section title is found in the next column, and the identifying section number is found in the right-hand column.

The sections are arranged in the bulletin, in the order shown in the table of contents. Turn to page one of the indicated section where the table of contents will be found (except where a section is small and does not require a listing of contents).

NOTE: For parts ordering information refer to Bulletin 1208B.

TABLE OF CONTENTS

*Indicates changes.
**Indicates a new section added to this bulletin.

Note 1: This bulletin now consists of three volumes. Sections originally in Bulletin 302B have been revised. New sections have been added in each volume.

Note 2: Circuit Description information formerly in Section 592-851-430TC is now contained in Section 592-851-130TC. Section 592-951-420TC contains schematic drawings and will be found in Volume 2. Lubrication information formerly in Section 592-851-730TC can be found in Section 592-851-731TC.

Note 3: Circuit Description information formerly in Section 592-852-430TC is now contain in Section 592-852-130TC. Section 592-852-430TC contains schematic drawings and will be found in Volume 2. Lubrication information formerly in Section 592-852-790TC can be found in Section 592-852-791TC.

TELETYPE CORPORATION
Skokie, Illinois, U.S.A.

MASTER AND SUPPLEMENTARY HIGH SPEED TAPE SENDER

FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

DESCRIPTION AND THEORY OF OPERATION

CONTENTS PAGE

CONTENTS PAGE

1. GENERAL

1.01 This section provides description and theory of operation for the master and supplementary high speed tape senders. It is reissued to include the latest engineering information, remove the preliminary designation, and change this section to the standard format. Circuit description information formerly contained m Section 592-851-430TC can now be found in this section under theory of operation. The changes include certain pushbutton circuit breakers in place of toggle type, an added circuit ground terminal strip and an added tape reader motor switch and fuse. Since this is a general revision. marginal arrows that indicate changes have been omitted.

1.02 The master and supplementary tape senders can send messages at rates up to 240 characters per second (2400 words a minute) The tape senders can read all standard paper tape including one inch width (5. 6, 7, and 8 level). Each **tape** sender is contained in US own separate cabinet incorporating a high speed reader (DX2) with a 600 foot tape supply container and tape wind-up facilities (Figure 1 and Figure 2)

2. DESCRIPTION

2.01 The master tape sender controls up to five supplementary tape senders and consists of a cabinet, cape reader, tape transport, and logic modules A and B. Logic circuitry includes reader control. drive circuits, message numbering, reader contact verification, feed verification. parallel to serial converter, and reader sequencing logic for controlling operations of the master and supplementary tape

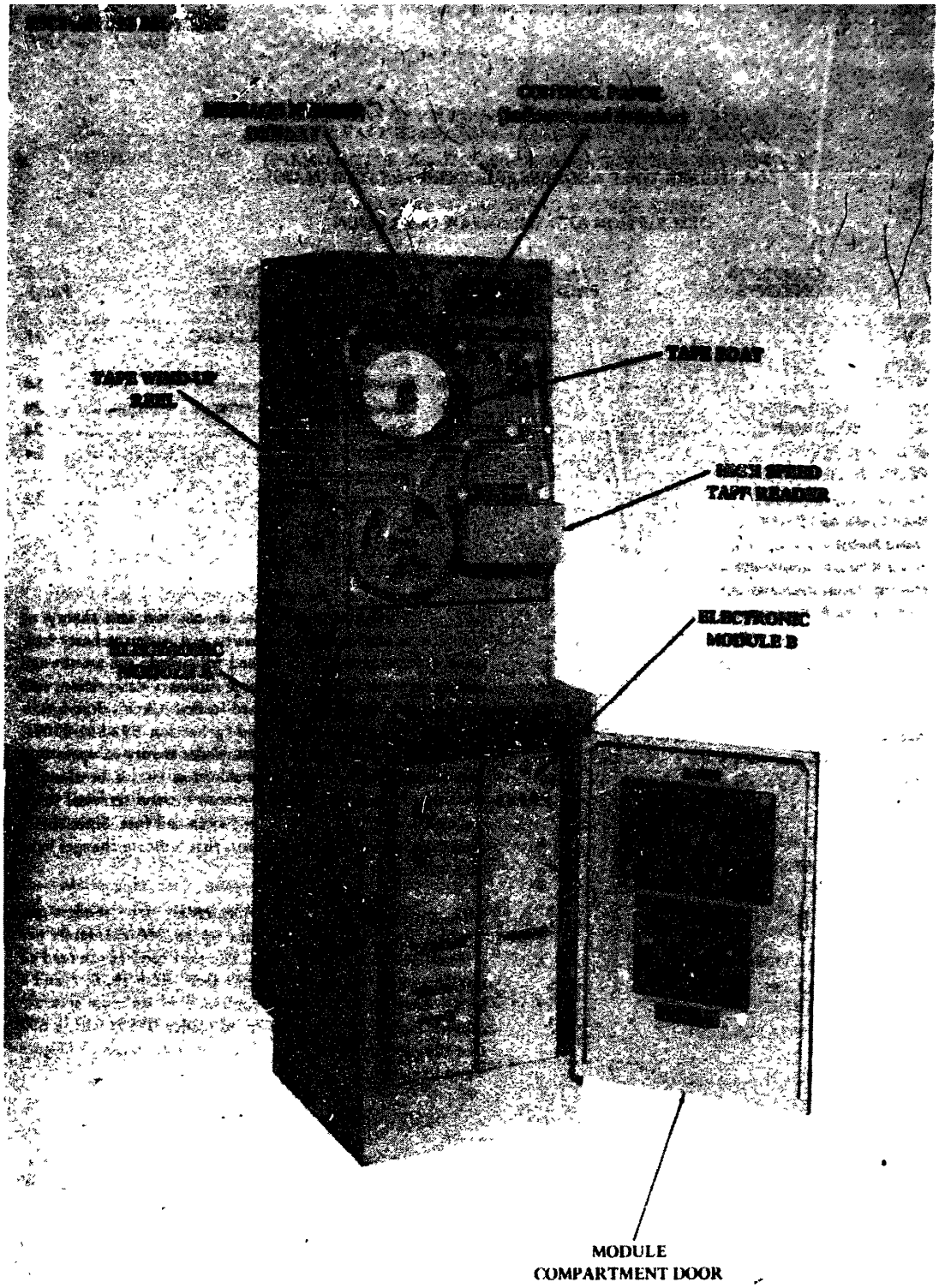

Figure 1. Master High Speed Tape Sender

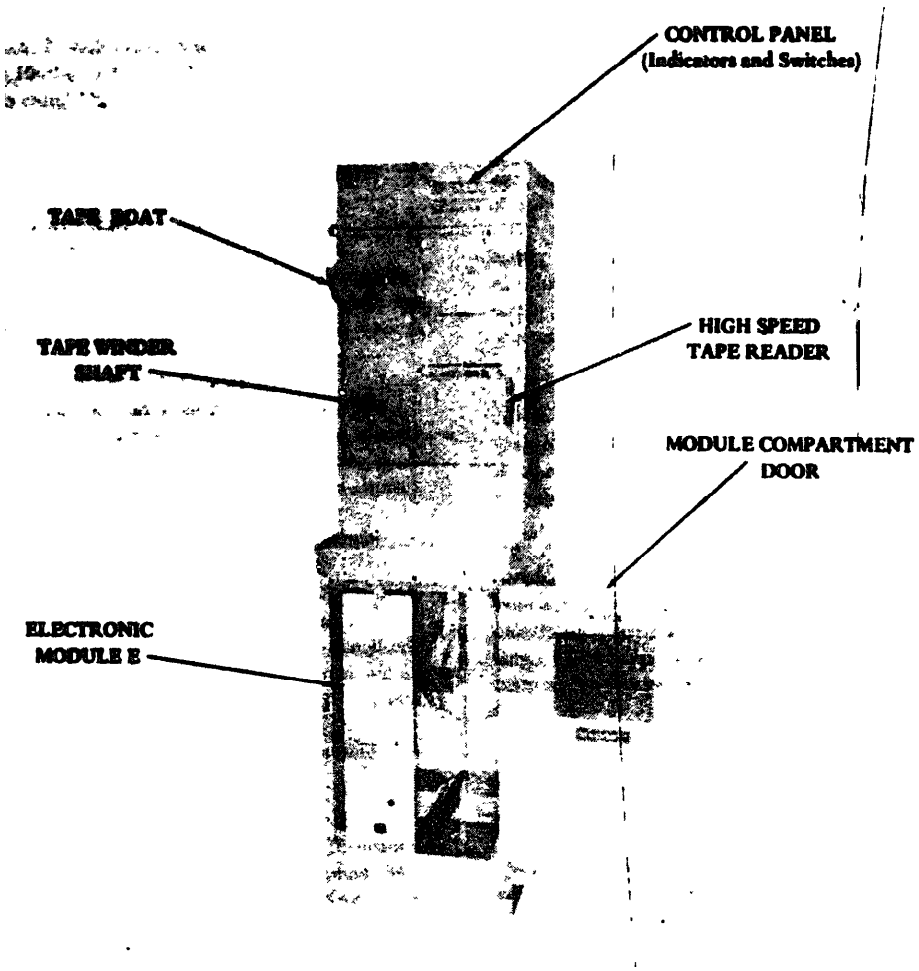

Figure 2- Supplementary High Speed Tape Sender

senders. The reader sequence logic circuitry permits each sender to transmit in turn one at a time, before any one sender can transmit a second time (Figure 1).

2.02 The supplementary tape sender contains the reader control and drive circuits for its associated tape sender. All other necessary logic circuitry is contained and controlled in the master tape sender cabinet. The reader sequence logic permits readers with tape to transmit in turn, permitting each reader to send before any one reader is given a second opportunity to send (Figure 2).

2.03 Each character is read and verified by the high speed reader, then sent by bit to external equipment Reader verification detects reading errors to assure that data is delivered correctly to the parallel to serial converter

A message numbering circuit automatically inserts a message number sequence ahead of each transmission.

2.04 The master transmitter and supplementary tape senders are mounted in separate cabinets. Each cabinet is 16 inch wide 23 inches deep, and 60 inches high. Tape readers. tape handling mechanism, electronic logic, and power supplies are accessible from the front of the cabinet. Component connections and some maintenance can be performed through the rear cabinet doors.

2.05 All controls and message numbering display (on master cabinet panel) are located on the control panel at the top of each cabinet The logic circuits are mounted on removeable plug-m type etched circuit cards, for case in replacing components and maintenance

ASSOCIATED EQUIPMENT

2.06 **The master and supplementary cabinets contain a tape transport and tape reading equipment. After the tape is taken up through the tape transport system to a power driven tape reel. Tape is read in one direction only.**

2.07 Reading is controlled by introducing drive pulses to the high speed. tape reader, which results in feeding the tape one character for each drive pulse. Drive pulses and output signals must conform to the specifications outlined in Section 592-804-500TC.

2.08 Sender operation begins by replacing a tape in the reading head of the master or supplementary reader and operating the BID switch. When no other sender is transmitting, the message numbering sequence to immediately sent and the reader starts operating

2.09 The data information is delivered by the reader to the parallel-to-serial converter of the master sender in parallel wire form. It is converted to a serial pulse stream and delivered to external equipment at appropriate signal levels. Data information may be delivered **to** external equipment directly in parallel form.

TECHNICAL DATA

A. Temperature and Power Specifications

2.10 Operating temperature fop all cabinets and equipment is between 40 degrees to 110 degrees fahrenheit ambient room temperature. Humidity ranges are between 5 percent and 95 percent for best operating efficiency. The power supply. located in the master sender cabinet, furnishes voltages for logic circuitry in the supplementary sender cabinet as well as the master sender. Reader stepping power is supplied by each individual cabinet. Power requirements for the master and supplementary cabinets are as follows.

(2) 117 volts ac **±10%,** 58.5 to 61.5 hertz, single phase.

(b) The master cabinet uses 287 watts without any supplementary cabinets connected; and 362 watts with five supplementary cabinets connected, transmitting a test message.

(c) Each **supplementary** cabinet uses 208 watts transmitting **at** 2400 words per minute.

B Input Signal Requirements

2.11 Input signal voltages are nominally positive and negative 6 volts ±1 volt. The minimum input impedance for all signals is mote than 5000 ohms. Input **signal capacitance is less than 0.0025 microfarads, and maximum input operating current of 0.0001 amperes. Input circuit switching occurs between the limits of ±0.5 volts or less.**

C. Input Signal Characteristics

2.12 Input signals from a binary timing clock controls the transmitting bit rate. This square wave signal with +6 volts and -6 volts has a bit rate exactly twice the data bit rate. The positive leading edge of each clock pulse occurs in time with the beginning of each binary data bit.

2.13 An abnormal traffic input to the master tape sender. controls a red warning indicator on the control panels of the master and supplementary tape senders. A -6 volt signal will operate the indicators and +6 volts will turn them off.

D. Output Signal Requirements

2.14 The output voltage of all signals is +6 volts ±1 volt or -6 volts ±1 volt, and the source impedance of the signals should not exceed 100 ohms. The maximum short circuit current delivered to the Interface should be 0.1 ampere.

E Output Signal Characteristics

2.15 The serial data output is a positive and negative 6 volt binary stream, The character rate is under control of the incoming clock signal and should not exceed 240 characters per second. Each character incorporates from 5 to 16 bits for synchronous operation, or from 6 to 16 bits for start-stop operation. The start bit of every start-stop character is generated at the same polarity (+6 volts or -6 volts), this is used to maintain character synchronization by the external equipment.

2.16 The next bats of each character (5, 6, 7, or 8 depending on mode of operation) carries the variable message information, while the remaining unused bits are transmitted marking (+6 volts). The synchronous signal contains no synchronizing information during data transmission because it contains no start bit. With no data being sent, a synchronizing pattern is generated under control of the timing clock input. This pattern is used by external equipment to achieve character register. any unused bus are always transmitted marking (+6 volts).

2.17 **A** parallel wire output IS available for 5, 6, 7, and 8 levels, corresponding to the 5, 6, 7, or 8 channels of the input tape. The signal output corresponding to the punch in the tape should be +6 volts; with no punch in the tape, the signal output should be -6 volts. Signals present for the entire character duration, less 200 microseconds at the end of the character.

2-18 The additional signal clock output defines the characters. When no signal is present it is -6 volts and rises to +6 volts at the beginning of each new character, it recycles to negative approximately two milliseconds later When operating five, six, or seven level, the parallel outputs at the unused levels will be dependent upon the size of the tape used. Operating with five level tape (11/16 inch), levels six, seven, and eight will be marking. Operating with six level tape (7/8 inch), levels seven and eight will be marking. When operating with seven level tape (1 inch), level eight will be spacing.

MASTER TAPE SENDER LOGIC

A. Modules

2-19 The electronic logic circuits required to control and operate the equipment are housed in modules located in the bottom of each cabinet. Two modules (A and B) are used in the master tape sender cabinet and one module (E) is used in the supplementary cabinet. Each module is 21 inches high, 6 inches wide, and 19-3/4 inches deep. It consists of a steel frame with a front panel for mounting controls and a rear panel for mounting receptacles (Figure 3).

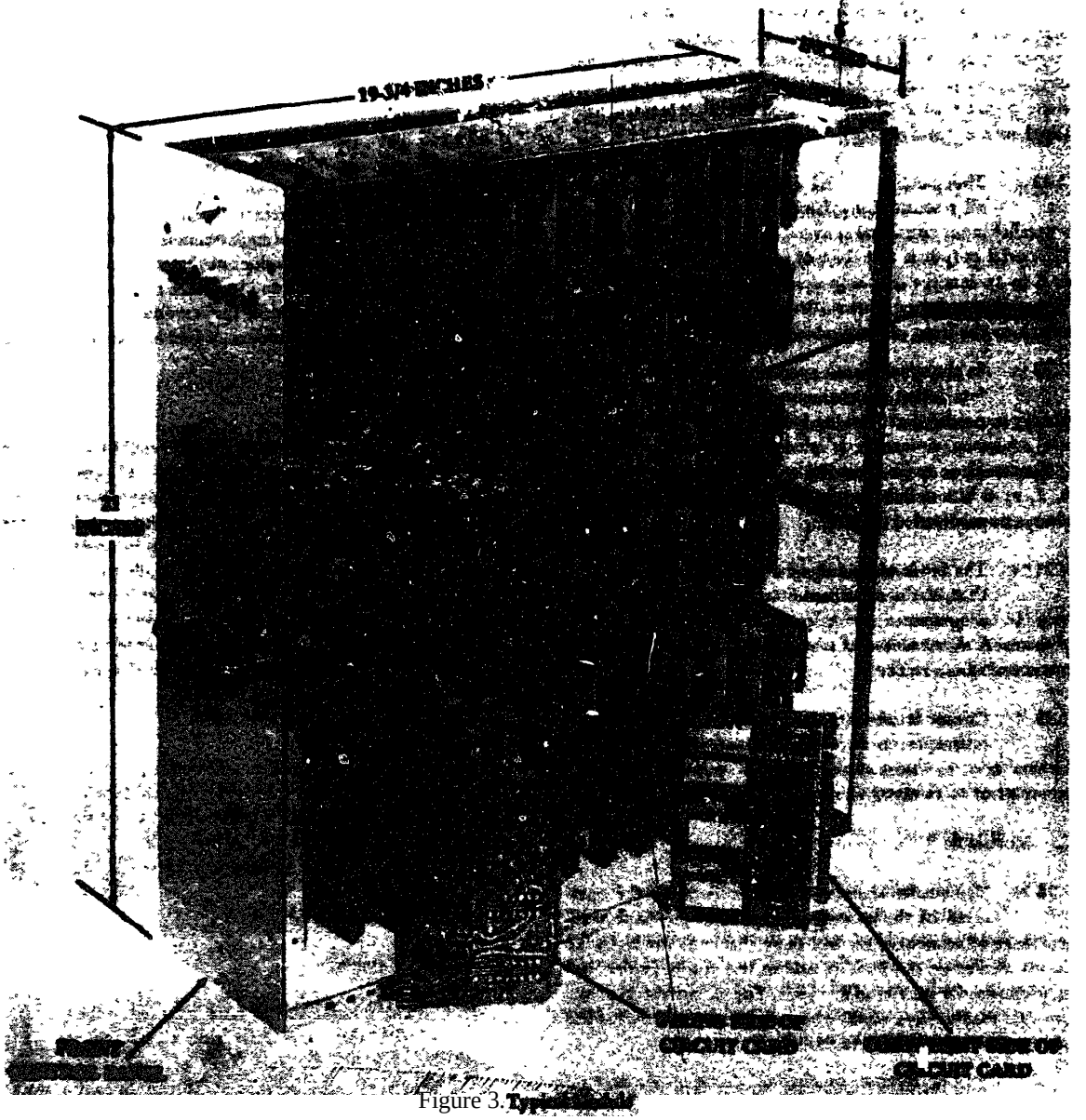

Figure 3. Typical Module

2.20 The electronic components are mounted on etched circuit plug-m cards. Each module can be fully extended or removed from the cabinet for ease of testing and maintenance. The converting cables at the rear of the modules provide enough slack to permit module removal without disrupting service.

B. Modules A and E

2.21 Reader control and drive circuits contained in both modules A and E, includes circuits that will accept low level reader drive signals from the sequencing logic, and converts them to high power pulses to drive the reader. There circuits also perform miscellaneous alarm and control function peculiar to each cabinet, and are incorporated in all supplementary and master cabinets.

2.22 The parallel to serial converter circuit (shared by all associated supplementary tape senders) accepts a parallel input signal and converts it to a serial signal output. The serial output is 5 to 16 bits for synchronous operation, or 6 to 16 bits for start-stop operation to define a character. The mode is selected by the SYNCHRONOUS START-STOP switch on the front of the module.

2.23 In the synchronous operation, the first 5, 6, 7, or 8 bits define the character and the remaining bits are always transmitted as marking bits (+6 volts). The fat bit in the start-stop operation is always transmitted the same (either mark or space according to the program), the next 5, 6, 7, or 8 bits define the character. The remaining bits are always transmitted as marking.

2.24 The bit levels and signal sensing are programmed in that, the signal sensed by the reader in one channel may be programmed for transmission in a different bit position. **A** signal sensed as a space, may be programmed for transmission as a mark.

2.25 Circuit breakers are provided at the power supply output for over load protection. Should a circuit breaker trip, the normal procedure of turning off cabinet power prior to resetting circuit breakers should be observed.

C. Module B

2.26 The ruder sequencing circuit controls the operation of the master and supplementary tape senders. Since all associated readers share this common logic, the circuit direct reader drive signals to the proper reader, and only one reader may send at **a** time. The circuit also prevents any one reader from sending a second time until all readers have had the opportunity to send first.

2.27 The message numbering circuit is a visually displayed control circuit on the master cabinet control panel. This message numbering device is capable of operating with supplementary as well as with master senders. **The visually displayed numbers during message transmission, or during idle time, is the next number to be sent.**

2.28 Each reader transmission is preceded by thirteen characters. These consist of: seven programmed identifying characters, one operator programmed character, one figures character, three numeric characters, and a letters character in that order (example: ZCZCABCX/999/). The three numeric character **increase one count after each** transmission. The counter can be manually reset to any count **including zero. The operator has the option of deleting** complete sequence by use of the NUMBERS DELETE switch. The message rate is limited to the maximum recycling rate of the counter (five times per second).

2.29 The reader contact verification circuit (shared by all readers) compares information presented to the parallel to serial converter with the actual character punched **in the tape.** Each character is read by two functionally independent contact reading assemblies, and the outputs compared. If one output does not match the other output, **a** reading failure is assumed to have taken place and the verifier alarm circuit is energized. Tape motion is verified by a sensing contact, which reads each feed hole as the tape passes over the tape feed wheel.

D. Alarms

2.30 When a condition occurs requiring immediate attention, the specific cause of each alarm is indicated by illuminating the affected control switch in red on the control panel of the appropriate supplementary cabinet and master cabinet. An alarm will be activated if the verifier detects an error or if a reader fails to feed. Alarm indicators must be reset manually, even when the alarm condition corrects itself. When an alarm is activated, a transfer contact (common to all alarms) in the master cabinet operates and is made available to the external apparatus.

TAPE TRANSPORT MECHANISM

2.31 The tape transport mechanism provides tape handling facilities for the high speed tape reader. The mechanism mounts in the supplementary or master cabinet, the dimensions are, 14-3/4 inches wide, 18 inches high, 19-1/2 inches deep, and the weight is 31 pounds. Tape supply is approximately 700 feet and tape winder capacity is approximately 900 feet (Figure 4).

TAPE THREADING

2.32 The message roll of tape is placed in the tape boat with the three hole side closest to the panel. Unwind approximately five feet of tape for threading through the tape transport system. Thread the tape along the path indicated on the label located on the plastic cover of the tape boat. Wrap approximately two turns around the wind-up reel hub to insure a nonslip start (Figure 4).

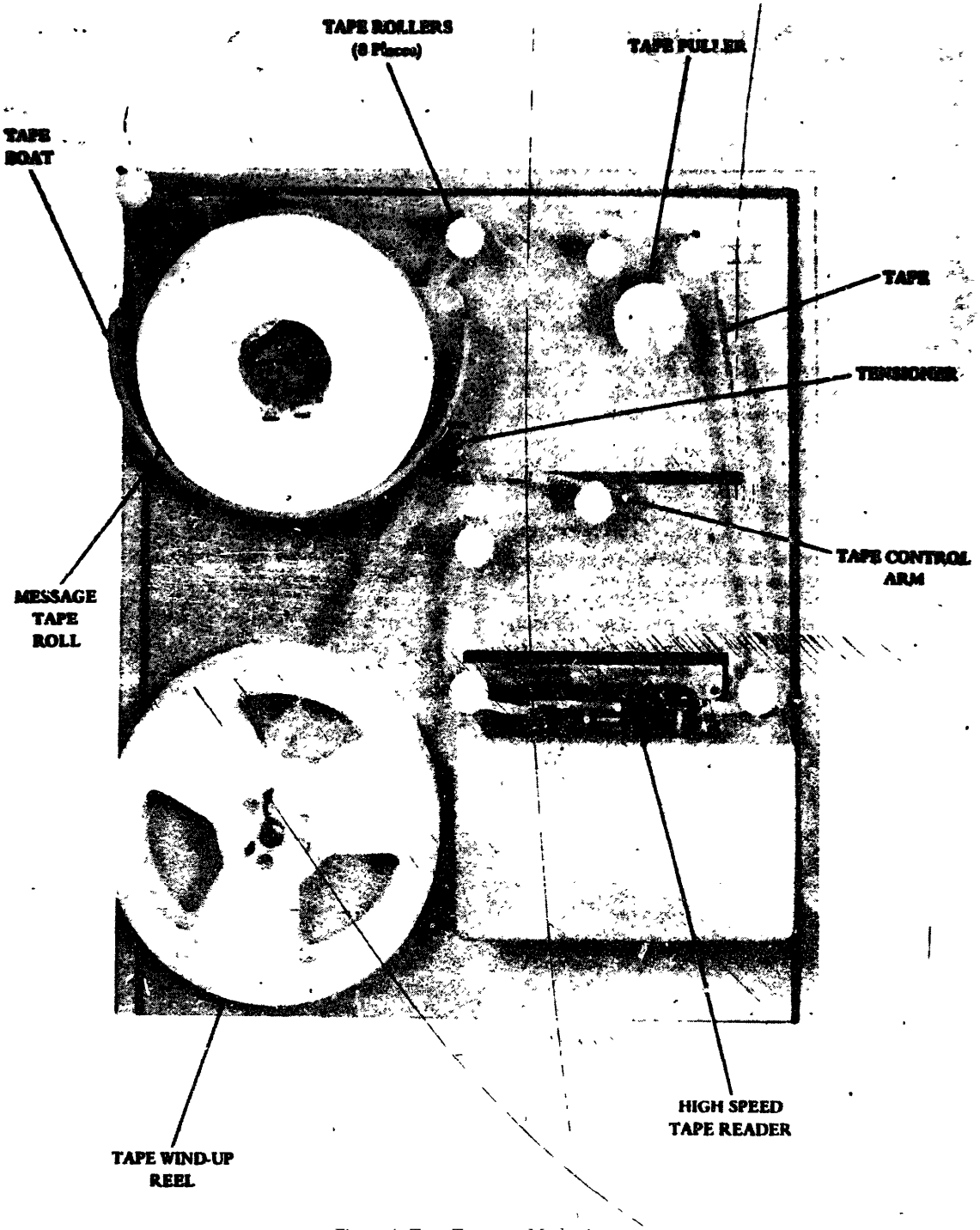

Figure 4- Tape Transport Mechanism

2-33 If the loose end of the tape roll is on the left side of the tape boat, run the tape over the left tape roller. Run the tape over the right tape roller if the tape end is on the right side. Pull the tape over the roller to the left tape puller roller, place the tape over the puller roller and under the tape puller and then over the right tape puller roller. The tape puller rotates continuously, but only contacts the tape when it is tightened around the puller from tension created by the high speed reader (DX). The tape then runs down the right side of the panel and under the right hand tape roller on the high speed tape reader cover. Place the tape in the reading head.

2.34

threading from left to right and around the tape control arm roller. Follow a horizontal path with the tape to the bottom tape tensioner, bring the tape up the left side and over the right side of the top tape tensioner, then run the tape to the windup reel.

2.55 When the tape becomes slack between the reader and the tensioner, the control arm moves toward the right. Through a system of levers, the belt clutch is tightened and the excess tape is wound up, the control arm moves to the left and loosens the belt clutch.

2.56 The high speed tape reader (DX) driver and power supply provides -24 volts and +6 volts operating voltages for a dual stepper driver card assembly. The dual stepper driver changes the low level stepping pulses to a power level adequate for energizing the reader stepping coils. Refer to Section 592-804-100TC, for high speed tape reader information.

3. THEORY OF OPLRATION

CONTROLS AND INDICATORS

3.01 Operator controls and indicators are located on the control panel at the top of each cabinet. The master and supplementary control panels are identical except for the message numbering indicator on the left side of the master control panel. Additional controls are located on the front panels of the electronic modules in the lower half of each cabinet behind protective doors. Parallel to the converter programming facilities are located within the transmitter logic module (Figures 5, 6 and 7).

3.02 The VERIFIER/TAPE FEED (Figures 5 and 6) split alarm and pushbutton switch indicates the alarm in red, with the reset switch common to both alarms. External equipment alarms are accepted through contacts common to both alarms, providing the alarm signal contacts.

3.03 The ABNORMAL TRAFFIC indicator lights when an abnormal traffic input signal is received from the external equipment.

3.04 When the reader is in the STOP condition, the STEP READ switch can be used to step the reader through a tape message, one character length (0.1 inch) for each operation of the switch. The operator may use the STEP switch to manually step the reader at times when there is as normally supplied step pulses.

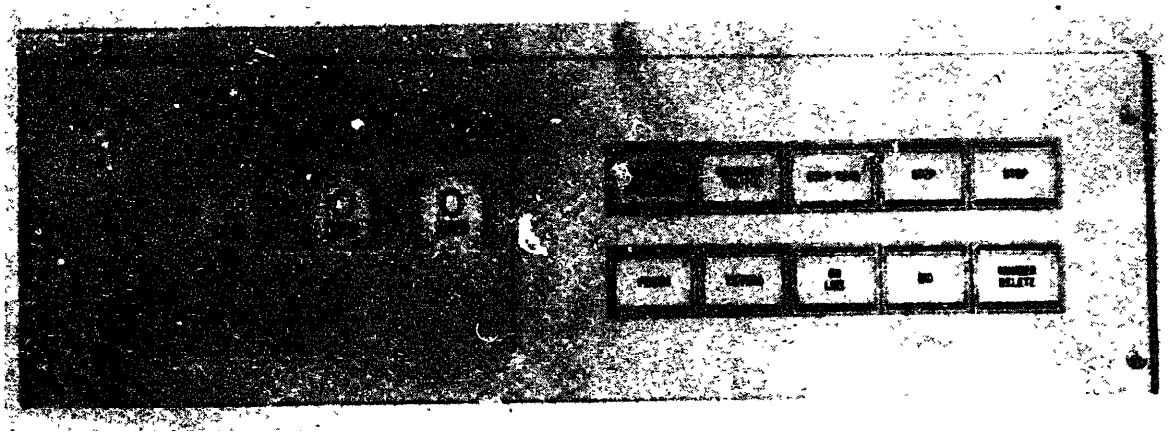

Figure 5-Master Control Panel

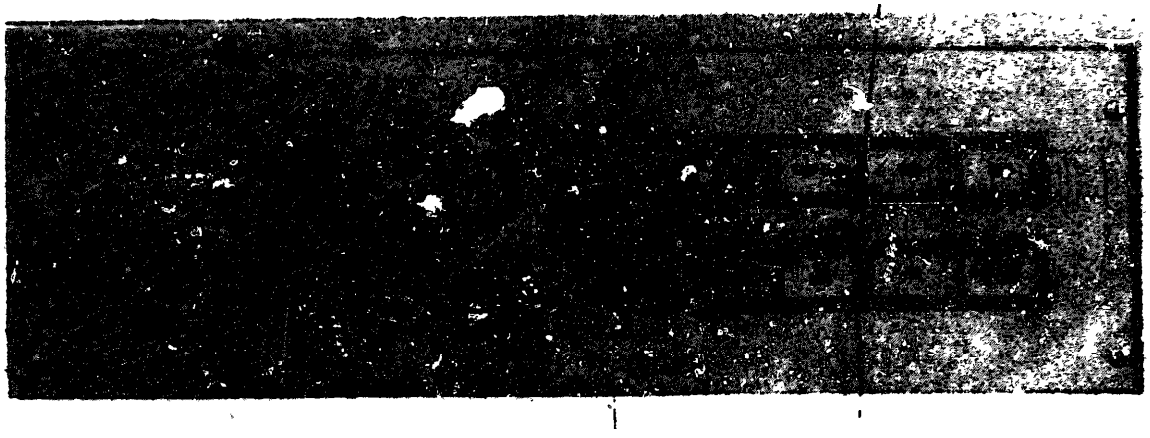

Figure 6- Supplementary Control Panel

3.05 Operating the STOP switch, illuminates the switch indicator and stops the reader during transmission. No other associated reader may used at this time. Operating the switch a second time, puts out the switch light, and restarts the reader and tape reading system.

3.06 When the POWER switch is operated, the switch indicator is illuminated and the switch actuates electric power to the tape transport motor, tape reader motor, and electronic circuits.

3.07 When a bid to transmit has not been initiated, operate the MOTORS switch, which illuminates the indicator and permits manual operation of the reader and tape winder motors.

3.08 The ON LINE indicator is illuminated when the reader has authorization to transmit.

3.09 The BID switch indicator is illuminated when operated and generates a bid to transmit when tape is in the reader.

3.10 When the NUMBER DELETE switch is operated and illuminated, the start of message sequence is not transmitted ahead of each transmission. At the end of each transmission the switch automatically resets to the normal (send number) mode and the indicator light is turned off.

3.11 Circuit breakers are provided on the front panel of the power supply module for overload protection. Should a circuit breaker trip to its off position, the normal procedure of turning off cabinet power before resetting the breaker should be observed.

3.12 The additional controls found on the front panels of the electronic modules in the lower half of the cabinet are as follows:

(1) Module A – CODE LEVEL selector switch (5, 6, 7, and 8 levels). UNITS PER CHARACTER INTERVAL selector switch indicates synchronous or start-stop level numerals; SIGNAL MODE toggle switch indicates either START-STOP or SYNCHRONOUS operation

(2) Module B – The SOM CHARACTER toggle switches (2, 3, 4, 5, and 6) one for each character bit, are operated in MARK or SPACE position to determine the eighth character in the start of message sequence.

(3) Module E – The module control panel contains some logic circuitry and logic voltage circuit breakers, all other controls are contained in modules A and B in the master cabinet.

CIRCUIT DESCRIPTION

3.13 The 0 volt, and -5 volts on some internal leads, are identified by a shaded corner in the logic symbol from which they originate. The dc coupled inputs to logic elements are shown as half arrow heads. Full arrow heads indicate ac coupled (pulse) inputs.

3.14 The commonly used NOR logic element is identified by the designation LA within the element symbol. The output of the element is negative when any input is 0 volt. The output is 0 volt only if all inputs are negative. A special input, identified by an arrow entering a corner of the symbol, allows the addition of extra logic

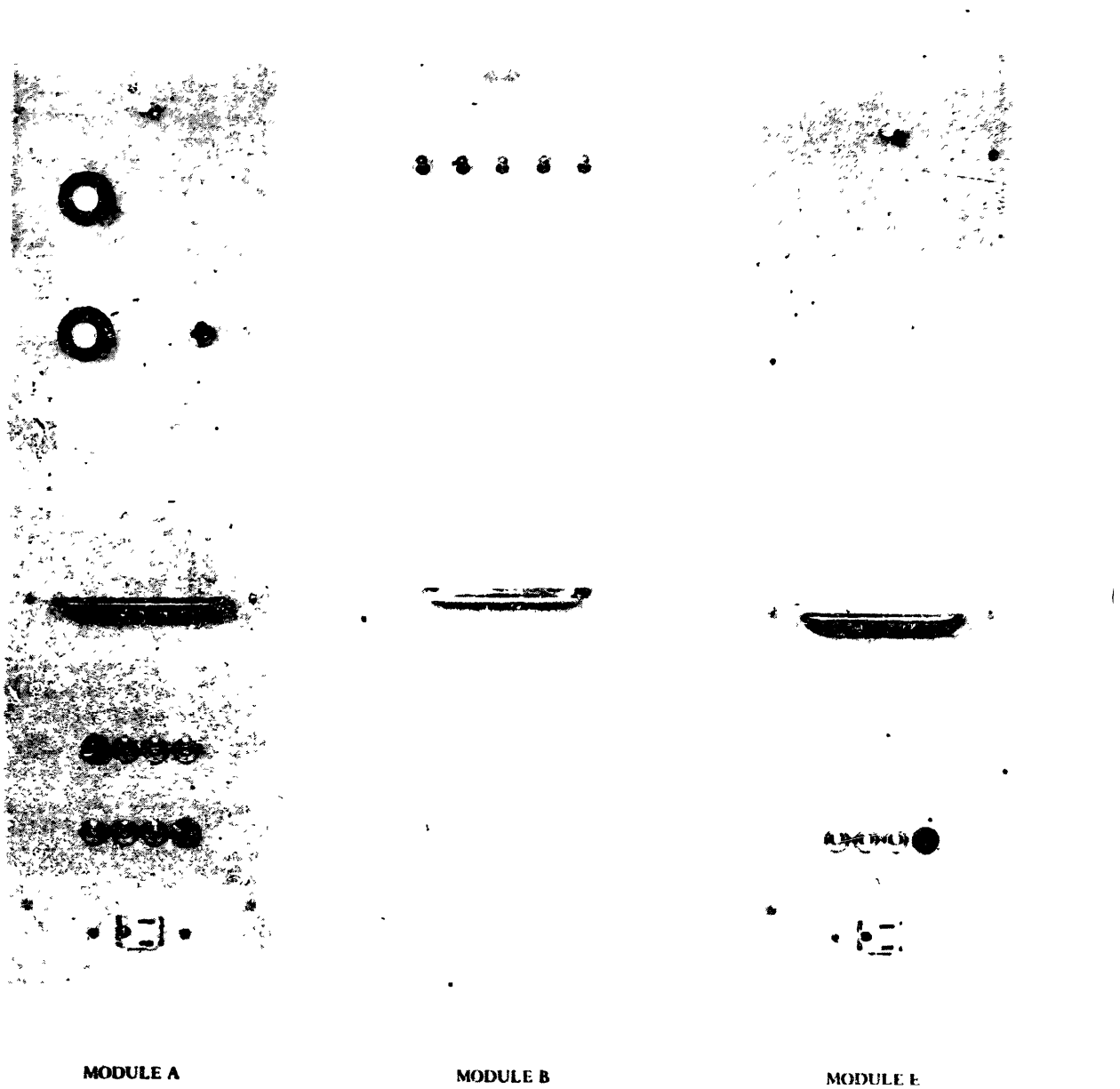

Figure 7- Master and Supplementary Modules

inputs to the element, or connecting two or more elements together to obtain more inputs and greater load driving capability.

3.15 The flip-flop element is designated by a rectangular box with a diagonal line across the lower half. The priming voltage inputs are shown as half arrows, and the setting voltage inputs by full arrows. Prime one input arrows enter the upper half of the symbol, and prime 0 volt and set 0 signals enter the lower half of the symbol. An arrow entering the center of the symbol designates the set 1 and set 0 inputs are connected together.

3.16 If no priming inputs are shown, the prime 1 input is connected to the inverted output (lower half of the symbol) and prime 0 input is connected to the normal output (upper half of symbol). Each input pulse reverses the condition of the voltages on the normal and inverted outputs.

3.17 The pulse amplifier element is identified by a square box with the letters PA in the symbol. A full arrow head indicates the input. This element produces a pulse approximately two microseconds in duration whenever the input goes negative. When both inputs are used, a pulse is produced only when both inputs go negative.

3.18 A trapezoid with the letters PA within the symbol represents the power amplifier element. This element has two inputs and can perform the NOR element function with approximately three times the load driving capability of an ordinary NOR (LA) element.

3.19 The delay element can be used either as a one shot or a free-running multivibrator, and is identified by a square box with the letters DY within the symbol. Delay elements used as one shots have the pulse duration indicated, when used as a free-running multivibrator, the frequency is indicated.

3.20 An input element translates input polar signals (+6 volts and -6 volts) to neutral signals (0 volt and -6 volts) used internally. It is identified by a rectangular box with INPUT printed within the symbol.

3.21 An output element translates neutral signals (0 volt and -6 volts) to output polar signals (+6 volts and -6 volts). It is identified by a rectangular box with OUTPUT printed within the symbol.

SUPPLEMENTARY READER LOGIC

3.22 The electronic logic circuits contained in module E are divided into the following four functional groups: bid circuitry, start of message delete circuitry, step and read circuitry, and alarm circuitry.

A. Bid circuitry

3.23 Insert the punched paper tape in the reading head. The normally closed tape-out contact moves to its open position which is connected to pin C8 of JE128. This action initiates the bid circuitry of the reader logic. Refer to 7711WD, Sheet 2, and Figure 8.

3.24 Pin C8 of JE128 assumes a negative voltage allowing the inverter ZE102 to saturate. The 0 volt output at the inverter (pin 9) is applied to the input pin B30, LA-2D, ZE103, and pin B4 of LA-2A, ZE118. AT LA-2D it is inverted, and applied to pin A32, LA-1D, ZE103 together with the input at pin B32. When both inputs are negative, the output on pin B34 is driven to 0 volt which acts as a prime voltage for setting the flip-flop D-B of ZE110 into the set one state. (Pin B33 is at 0 volt and pin B34 at a minus voltage.)

3.25 The BID indicator witch may now k operated to provide a transition at the input, pins A36, and B36 of flip-flop D-B of ZE110. The voltage transition switches the flip-flop to the set one state. The two LA networks connected between the BID switch and the complementary input are connected as a dc (direct current) flip-flop, to prevent switch contact bounce from affecting the set input of the flip-flop.

3.26 With flip-flop D-B of ZE110 in the set one state. pin B34 is driven negative and pin B33 is driven to 0 volt. The 0 volt is inverted by PA-1C of ZE108 and applied to PA-ID of ZE108. The output, pin B1 of PA-1D of ZE108 is driven to 0 volt, energizing relay K2 and the motor start relay K1 through an isolating diode CR3 of ZE110.

3.27 The diode presents relay K2 from king energized when the MOTORS indicator switch (SF107) located on the control panel, is operated Refer to 7710WD, Sheet 6 for the motor circuit. When energized, the motor start relay K1 starts the reader and tape winder motors. Energizing relay K2 lights the bid indicator lamp and motor indicator lamp. The diode connected between the bid lamp and motor lamp prevents the bid lamp from lighting when the MOTORS switch is activated.

3.28 The negative voltage at pin B34 on flip-flop D-B of ZE110 is inverted to 0 volt by PA-2C of ZE108 and applied to the input pin A32 on DY-A of ZE108 for a 500 millisecond one shot. The output pin A34 is driven to 0 volt and remains there for a period of 500 milliseconds, at this time it returns to a negative voltage. This negative transition is applied at the input pin A31 on PA-E of ZE108 and provides a positive pulse at the output, pin A27.

3.29 This pulse is again delayed by an identical delay-pulse amplifier network. The results are a total delay of one second from the time a negative transition was obtained at pin B34 on flip-flop D-B of ZE110 until a pulse is

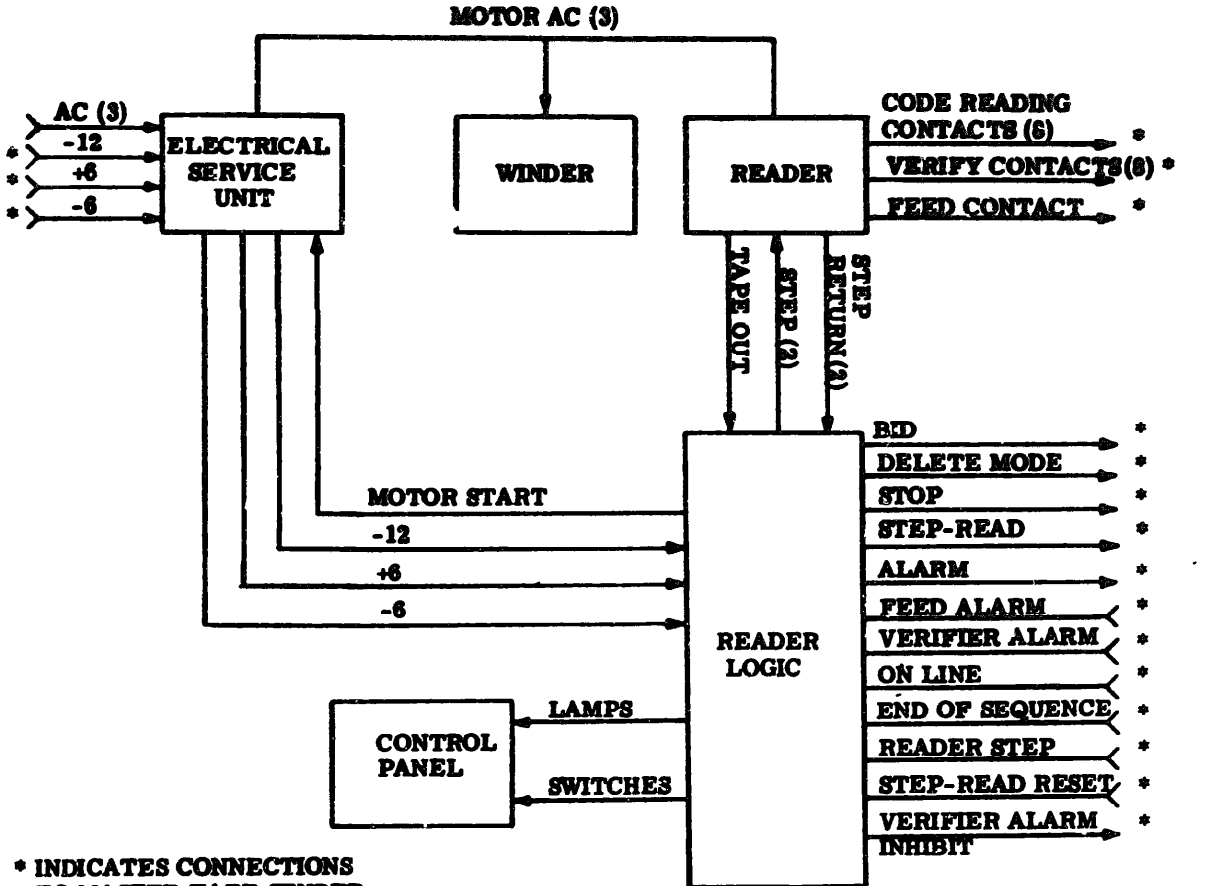

Figure 8- Block Diagram for Supplementary High Speed Tape Sender

provided at pin B24 on flip&p D-C of ZE110. The associated prime input pin A24 on flip-flop D-C of ZE110 was driven to 0 volt at the time flip-flop D-B of ZE110 was initially switched by the BID indicator switch. The flip-flop D-C of ZE110 is switched, driving the inverted output pin B26, negative. This output is applied to the input, pin B25 on LA-1C of ZE114.

3.30 The second input of this element, pin A24, is supplied by the output on PA-1C of ZE108 which **samples the normal output pin B33 on flip-flop D-B of ZE110. The normal output of flip-flop D-B, having been driven to 0 volt at the time the BID switch was activated, allows PA-1C section of ZE108 to provide a -5 volts to pin A24 on LA-1C of ZE114. With both inputs on LA-1C of ZE114 at a negative voltage, the output pin A27 is driven to 0 volt. This 0 volt is supplied as a BID request signal to sequence control logic in the master transmitter cabinet.**

3.31 The effect of inserting tape in the reader and **operating the BID switch is to immediately start** the reader and winder motors, and one second later provide **a** BID request signal.

3.32 After operating the BID indicator switch, the operator may cancel the bid request provided action is taken prior to the receipt of the on-line signal from the sequence control logic. This reset action is accomplished by operating the BID indicator switch a second time to obtain a positive transition at the complementary input pin A36 and B36 on flip-flop D-B of ZE110. The prime 0 volt input at pin B35 of ZE110 is at 0 volt due to the input pins B22 and B23 on LA-2C of ZE114, both being negative. The input pin B23 was driven negative through PA-1C of ZE108 at the time flip-flop D-B first set.

3.33 The second input to LA-2C of ZE114 samples the on-line signal from the sequence control logic. As long as the on-line signal remains negative the flip-flop D-B of ZE110 is primed to be reset. When the on-line signal goes to 0 volt, the prime 0 volt input, pin B35 is driven negative and the option for resetting the flip-flop D-B with the BID indicator switch is removed.

3.34 Flip-flop D-B can now be reset only by a tape-out indication from the reader. This tape-out indication is a positive transition at the input pin 12 of inverter ZE102 where it is inverted and applied to pin B4 on LA-2A, ZE118. If pin B5 on LA-2A is negative at this time a positive transition will be applied at pin B32 and pin B27 on supplementary gates of ZE110, resetting flip-flops D-B and D-C of ZE110. When these flip-flops are reset the reader and winder motors are turned off and the bid request to the sequence control logic is removed.

3.35 The negative input at pin B5 on ZE118 is a result of LA-2B on ZE118 sampling either an off-line condition or an end of sequence. If neither of these conditions exist the input at pin B5 will be at 0 volt and the tape-out indication will be prevented from resetting the above mentioned flip-flops. This logic prevents an incomplete start of message sequence to be transmitted when the tape lid is released during the sequence.

3.36 The power on reset circuit at position ZE202 is used to provide a collector set pulse to flip-flop D-B and D-C of ZE110, a predetermined time after power is turned on. This action insures that the bid circuitry is not bidding for the line when the equipment is initially turned on/ The 150 ohm, 1 watt resistors shown across the various relay contacts driving indicator lamps, are used to keep a small amount of voltage across the filament of the lamp. This reduces the initial current surge and extends the life of the lamp.

B. Start of Message Delete Circuitry

3.37 The number delete circuitry provides the operator with the option of deleting the number sequence which normally precedes each message tape. Prior to operating the BID indicator switch, the operator determines if the message tape requires a number sequence. If the number sequence is not necessary the NUMBER DELETE indicator switch is operated. This switch provides a positive transition at the input pin A36 and B36 on flip-flop D-B, ZE112, provided the on-line signal applied at pin B14 on LA-1B, ZE114 is negative. If this on-line signal is at 0 volt, indicating the associated transmitter is on-line, the indication from the NUMBER DELETE indicator switch is held at LA-1B of ZE114 and does not switch flip-flop D-B of ZE112. Refer to 7710WD, Sheet 3.

3.38 Assume the on-line signal applied at pin B14 on LA-1B of ZE114 is negative and the signal from the NUMBER DELETE indicator switch is presented to input pin A36 and B36 on flip-flop D-B of ZE112. This flip-flop will be switched to the one state, diving the output pin B34, negative. The signal is applied to input pin A4, PA-2D of ZE-108, driving the output pin A1 to 0 volt, which energizes relay K4 and lights the number delete lamp though the K4 relay contact.

3.39 The negative voltage at pin B34 of flip-flop ZE112-B is also applied to pm B26 on LA-1F of ZE103. This element is held at this time due to 0 volt being supplied to pin A21 from the output B6 on PA-1C of ZE108 (refer to 7710WD. Sheet 2). When the BID indicator switch is operated, flip-flop D-B of ZE110 is switched as described in 3.25. A 0 to -5 volt transition is applied to pin A24 on LA-1C and pin A21 on LA-1F of ZE103.

3.40 The output pin A27 of LA-K, ZE103 is held at -5 volts due to the 0 volt present at input pin B25 and output pin B28 on LA-IF of ZE103 goes to 0 volt. The resulting positive transition at the output of LA-IF is used to set flip-flop DC of ZE112 into the one state, driving the output pin B26, negative. This voltage level is inverted by LA-1D of ZE114 and applied to the sequence control logic in the master cabinet as a delete mode signal.

3.41 At the completion of the message tape, a tape-out indication is received from the tape-out contact at the reader. This indication resets the bid circuitry as described in 3.34, and provides a negative to 0 volt transition at pin B6 on PA-1C of ZE108, (refer to 7710WD. Sheet 2). This transition IS applied to pin B32 of supplementary Bate ZE112, resetting flip-flop D-B of ZE112. With the reset of flip-flop D-B, the NUMBER DELETE indicator lamp is extinguished. On later sets, the reset signal for flip-flop D-B of ZE112 is obtained at pin B6 and A10 of power amplifier PA-1C of ZE106.

3.42 During normal operation (not in the delete mode) the output pin B33, on flip-flop D-B of ZE112, is at -5, volts. This is applied to the input pin B25 on LA-1C of ZE103, and permits the negative bid signal transition at pin A24 as described in 3.40. The inverted signal is passed to flip-flop D-C ZE112 as a set zero signal. This provides a -5 volt indication at the delete mode output pin F7 of JE128.

3.43 At the completion of the start of message sequence a negative going transition is received from the master logic at JE128, pin E7. The signal is inverted by LA-2E, of ZE118, and applied to pm B31 of the supplementary gate ZE112 as a reset signal for flip-flop Q-C of ZE112. This reset signal is allowed to pass, provided an on-line signal is present at the prune input pin A31 of the supplementary gate. When flip-flop D-C of ZE112 IS reset, the delete mode indication to the master logic is changed to 0

volt. This permits the step pulses in the master logic to be diverted from the start of message generator to the associated reader.

C. Step and Read Circuitry

3.44 During reader operation, the operator has the option of stopping the reader and stepping it manually with the STEP READ indicator switch. When the STOP switch is operated, the associated STOP indicator lamp is lit and a voltage level change from 0 to -5 volts is obtained at pin B4 on LA-2A, ZE103. The switch output is fed through a dc flip-flop configuration, similar to the circuit described in 3.25 to remove contact bounce. (Refer to 7710WD, Sheet 4.)

3.45 When the reader is operating, the on-line signal input at pin B5 of LA-2A, ZE103 is -5 volts. As a result of the negative level being applied to pin B5 of LA-2A, ZE103 and the level change from 0 volt to -5 volts at pin B4 due to the STOP switch, the output pin A9 is driven to 0 volt. The 0 volt is used as a reader stop signal to the master logic and as a prime voltage to flip-flop D-F of ZE110.

3.46 In the master logic this signal is used to inhibit the stop pulses to the start of message (SOM) generator or the reader, thereby stopping operation. The prime voltage applied at pin A2 of flip-flop D-F permits the positive transition appearing at the set input pin A1, to switch the flip-flop, driving the output pin B3, to -5 volts. The positive transition at the input, pin A1, is a result of operating the STEP READ switch.

3.47 The output pin B3 of flip-flop D-F on ZE110 is inverted by LA-2E on ZE116 and supplied to the master logic as a step-read pulse. This pulse allows the reader to be stepped one character, and read by the reader to be transmitted on line, provided the stop switch is in the stop position. When the STOP switch is operated again, returning it to its normal position, the reader is stepped automatically by the incoming step pulse rate.

3.48 The reader may be manually stepped (off-line) during periods when the reader is not normally being stepped by the incoming step pulse rate. The STEP indicator switch output is fed to a dc connected flip-flop configuration, consisting of LA-1B, and LA-2B on ZE116. When the STEP switch is operated, a positive transition is obtained at the output pin A11 of this flip-flop and applied to LA-1B, ZE103 for inversion prior to being applied to the input pin B13 of LA-2B, ZE103.

3.49 If the second input pin B12 of LA-2B is negative at this time, the input at pin B13 will be inverted and appear at the output pin A11. The input level at pin B12 is 0 volt only when the STOP switch is in its normal position and at the time the on-line signal input at pin B23 of LA-2C, ZE103 is -5 volts. When this condition is met it is assumed the reader is normally being stepped by incoming step pulses and the manual step indications are held.

3.50 The result is, the STEP switch is available for manually stepping the reader at times when it is not reading tape and being stepped by pulses received at pin D10 on JE128. Assuming the input pin B12 of LA-2B, ZE103 is at -5 volts, the manual step pulses at pin B13 appear inverted at the output pin A11. Then the pulses are inverted twice by LA-2F, ZE103 and LA-1F on ZE116.

3.51 At the output, manual step pulses appear as positive transitions which are applied to the driver assembly. The driver assembly, located in the tape transport assembly, functions to change the low-level stepping pulses to a power level adequate for energizing the reader stepping coils. These pulses are delivered to the driver assembly from two sources, one from the STEP switch described in 3.50, and the other from the sequence control circuitry in the master logic. They are applied to pin D10 on JE128.

3.52 The LA-1A of ZE118 performs the function of preventing an alarm indication from occuring when the reader is restarted after it has been stopped and manually stepped with the STEP switch. This is required due to the characteristics of the verify logic explained in the following paragraphs.

3.53 Input pin A7 of LA-1A, ZE118 samples the condition of the STOP switch. When the STOP switch is in the stop condition, the input is -5 volts. Pin B7 of LA-1A, ZE118 samples the online signal, -5 volts, which is on at this point. The third input pin, A6 of LA-1A, ZE118 samples the STEP switch output at pin A17 of LA-1B, ZE103. When the switch operated, pin A6 of LA-1A, ZE118 is driven negative, with all three inputs of LA-1A, ZE118 at -5 volts. The output pin A10 is driven to 0 volt. This positive transition is applied to the master cabinet logic where it is used to prevent an alarm on reader start-up when the contacts are sampled again.

3.54 When power is turned off at the supplementary cabinet, relays K1 and K2 provide an open circuit at the stop signal output, pin C10 of JE128, and the step-read signal output, pin C9 of JE128. When power is turned on, the relays are prevented from energizing for a period of 80 milliseconds, after being energized, the contacts close. At this time the two outputs have had time to stabilize at -5 volts and any transitions are prevented from being applied to the master logic.

D. Alarm Circuitry

3.55 Two types of alarms are contained in the reader logic circuitry: A verify error alarm and a reader feed error alarm. When either one of these errors occur, an indication is received at pin A8 or B8 of JE128, setting an associated flip-flop D-D or D-E of ZE110. The flip-flops are primed by the presence of an on-line indication from the master logic. When either of the two flip-flops is set, an

associated alarm lamp is lighted and a 0 volt indication is applied at pin A1 or B1 of A-2E, ZE103. The output pin B9 of LA-2E, ZE103 is inverted by [illegible] and supplied to the verifier in the master logic as a 0 volt alarm signal. (Refer to 7716WD, Sheet 5.)

3.56 If the alarm flip-flops were to come up in the alarm condition when power is turned on, an output of the alarm circuit is required as LA-1C, ZE116. This prevents an alarm indication to the master logic. Since an alarm at any one sender prevents operation at any other sender, this condition could interrupt the step pulses to an operating sender.

3.57 Press the VERIFIER/TAPE FEED indicator switch (ALARM RESET on schematic) to reset alarm flip-flops and extinguish the alarm lamp or lamps. The ON-LINE indicator lamp is lighted when the on-line signal is received. The indicator lamp is a signal to the operator when a particular reader is allowed to transmit after a line bid has been entered. Relay K3 performs the same function at the output of the alarm circuitry as relays K1 and K2 performed in the step and read circuitry described in 3.54.

3.58 The master transmitter cabinet contains one DX type reader with the necessary tape handling equipment. The electronic logic and power supply is contained in two removable modules located in the lower part of the cabinet.

3.59 The electronic logic circuits in modules A and B are similar to the reader logic in module E and performs the same functions described in 2.21 through 2.29. The controlling logic circuits contained in modules A and B are divided into five functional logic systems. They are arranged for controlling up to five external supplementary tape senders plus the associated master transmitter. Refer to Figure 9 for a block diagram. The logic circuitry consists of the following logic systems: reader logic, parallel to serial converter, sequence control, verifier, and start of message generator (SOM).

A. Reader Logic

Bid Circuitry

3.60 Insert the punched paper tape in the reading head. The normally closed tape-out contact moves to its open position which is connected to pin C8 of JA128. This action initiates the bid circuitry of the reader logic. Refer to Figure 9 and 7716WD, Sheet 2.

3.61 Pin C8 of JA128 assumes a negative voltage allowing the inverter ZA301 to saturate. The 0 volt output at the inverter (pin 9) is applied to the input pin B30 of LA-2D, ZA103 and pin A5 of LA-1A, ZA305. At LA-2D it is inverted, and applied at pin A32 of LA-1D, ZA103 together with the input at pin B32. When both inputs are negative, the output on pin B34 is driven to 0 volt which acts as a prime for the inputs at pins A36, and B36 for setting flip-flop D-B of ZA110.

3.62 The BID indicator switch may now be operated to provide a transition at the input pins A36, and B36, of flip-flop D-B, switching to the set one state. The two RA elements connected between the BID switch and the flip-flop set input are connected as a dc (direct current) flip-flop to eliminate contact bounce.

3.63 With flip-flop D-B in the set state, pin B34 is driven negative and pin B33 is at 0 volt. This 0 volt is inverted by PA-1C of ZA108 and applied to PA-1D of ZA108. The output pin B1, of ZA108 is driven to 0 volt energizing relay K2, and the motor start relay K1 through an isolating diode, ZA110. This diode prevents relay K2 from being energized when the MOTORS indicator switch is operated. With the motor start relay K1 energized the reader and tape winder motors start. When relay K2 is energized the BID and MOTORS lamps are lighted. The diode (CRG101) connected between the BID and MOTORS lamps prevents the BID lamp from being energized when the MOTORS indicator switch is operated.

3.64 The negative voltage transition at pin B34 on flip-flop D-B, of ZA110 is inverted by PA-2C of ZA108 and applied at the input pin A32 of delay DY-A of ZA108. The output pin A34 is driven to 0 volt and remains at 0 volt for a period of 500 milliseconds, when it returns to a negative voltage. This negative transition is applied at the input pin A31, of PA-E on ZA108, and provides a positive pulse at the output pin A27. This pulse is again delayed by an identical delay circuit, the pulse amplifier network. This results in a total delay of one second from the time a negative transition was obtained pm B34. on D-B of ZA110 until a pulse is provided at the set input pin B24, on D-C of ZA110.

3.65 The associated prime prime pin A24, was driven to 0 volt at the rime flip-flop D-B was initially set by the BID indicator switch. The D-C flip-flop is switched driving the inverted output pin B26, to -5 volts. This output is applied to the input Z25, of LA-1C, ZA-114.

3.66 The second input of LA-1C. pm A24 is supplied by the output of PA-1C on ZA108 which samples the normal output of D-B. The normal output pin B33, of D-B in driven to 0 volt at the time the BID switch is activated and allows PA-1C of ZA108 to provide -3 volts to the input pin A24 of LA-1C on ZA114. With both inputs of LA-1C, ZA114 negative, the output pin A27 is driven to 0 volt. This 0 volt is supplied to the sequence control logic as a bid request.

3.67 **The effect of inserting tape in** the reader and operating the BID switch, is to immediately start the reader and winder motors and one second later provide a bid request to the sequence control logic.

3.68 **After operating the BID switch, the operator may cancel the bid request by operating the BID switch a second time before receipt of the on-line signal from the sequence control logic. This reset action obtains a positive transition at the complementary input pins, A36 and B36 of flip-flop D-B on ZA110. At this time the prime one input pin, A35, is at -5 volts because the output pin, B33 on D-B, is at 0 volt. This 0 voltage is applied to the input pin, B32 of LA-1D, ZA103 driving the output of this element to -5 volts.**

3.69 **At the same time, the prime 0 input pin, B35, is at 0 volt because the input pins, B22 and B23 of LA-2C, ZA114 are both negative. The input pin, B23 was driven to -5 volts through PA-1C of ZA108 at the time flip-flop D-B was first switched to the bid condition. The second input to LA-2C, ZA114 is the on-line signal from the sequence control logic. As long as the on-line signal remains negative, D-B is primed to reset. When the on-line signal goes to 0 volt the prime 0 input pin B35 is driven to -5 volts and** the ability to reset with the BID switch is removed.

7.70 Flip-flop D-B can now be reset only by a **reader** tape-out indication in the form of a positive transition at the input pin 12, of inverter ZA-301 where it is inverted and applied to pin A5 of LA-1A, ZA305. If pin B7 of LA-1A is negative, at this time a positive transition will be applied at pins B32 and B37 of supplementary gates in ZA110 resetting flip-flop D-B and D-C. When D-B and D-C are reset the reader and winder motors are turned off and the **bid request to the sequence control logic is removed.**

3.71 The negative input at pin B7 of ZA305 is a result of LA-1C, ZA321 sampling either an off-line **condition or an end of sequence. If neither of these conditions exist, the input at pin B7 will be at 0 volt and the tape-out indication will be prevented from resetting flip-flops D-B and D-C. This logic prevents an incomplete start of message sequence to be transmitted when the tape lid is released during the sequence.**

3.72 **The power on, reset circuit at ZA401, is used to provide a collector set pulse to flip-flop D-B and D-C, a predetermined time after power is turned on. The** action insures that the bid circuitry is not bidding for the line when the equipment is turned on.

Start of Message Delete Circuitry

3.73 **The number delete circuitry provides the operator** with the option of deleting the number sequence which normally precedes each message tape. Prior to operating the BID switch the operator determines if the message tape requires a number sequence. If not, the operator presses the NUMBER DELETE switch, providing **a** positive transition at the input pins A36 and B36 of flip-flop D-B on ZA112, if the on line signal applied at pin B14 of LA-1B, ZA114 is negative. If this on-line signal is at 0 volt, indicating the associated transmitter is on-line, the signal from the NUMBER DELETE switch is held at LA-1B ZA114 and does not switch D-B of ZA112 Refer to 7716WD, Sheet 3.

3.74 **With the -5 volts on-line signal applied to pin B14 of LA-1B, ZA114 the indication from the NUMBER DELETE switch is presented to pins A36 and B36 of flip-flop D-B on ZA112. The D-B will be switched to the one state driving the output pin B34 negative. This -5 volts is applied to the input pin A4 of PA-2D on ZA108, driving the output pin A1 to 0 volt, which energizes relay K4 and lights the NUMBER DELETE lamp through K4 contacts.**

3.75 **The negative voltage at pin B34 of flip-flop D-B is also applied as a prime at pin B26 of LA-1F, ZA103. The LA-1C, ZA103 is inhibited at this time due to the 0 volt supplied at pin B25 from pin B33 on D-B. When the BID switch is operated and D-B of ZA110 is switched as described in 3.62, a 0 to -5 volt transition is applied to pin A24 of LA-1C and pin A21 of LA-1F, ZA103. The output pin A27, of LA-1C, ZA103 is held at -5 volts due to the 0 volt present at input pin B25.**

3.76 **The output pin B28 of LA-1F, ZA103 is allowed to go to 0 volt due to -5 volts present at its other input pin, B26. The resulting positive transition at the output of LA-1F, ZA103 is used to set flip-flop D-C of ZA112 into the one state driving pin B26 to -5 volts. This level is inverted by LA-1D, ZA114 and applied to the sequence control logic as a number delete signal.**

3.77 **At the completion of a message the tape-out indication is received from the tape-out contact at the reader. This signal resets the bid circuitry as described in 3.70 and provides a -5 volt to 0 volt transition at pin B6 of PA-1C, on ZA108. This transition is applied to pin B32 of supplementary gate ZA112 providing a reset signal for flip-flop D-B. With the reset of D-B, ZA112 the NUMBER DELETE lamp is extinguished. On later sets, the reset signal** for D-B of ZA112 is obtained at pin B6, A10 of PA-1C on ZA106. Refer to 7716WD, Sheet 2.

3.78 During normal operation (not in the delete mode) pin B33 of flip-flop D-B is at -5 volts. This is applied to the input pin B25 of LA-1C, ZA103 and permits a **negative transition at pin A24 (3.75) to be inverted and passed to the flip-flop D-C as a reset signal. This provides -5 volts indication at the delete mode output, pin F7 of JA128.**

3.79 **A negative going transition, is received from the start of message (referred to as SOM – module B panel) sequence generator at pin E7 on JA128, upon completion of the SOM sequence. The signal is inverted by LA-2C, ZA305 and applied to pin B31 of supplementary gate ZA112 as a reset signal for flip-flop D-C. This reset signal is allowed to pass provided an on-line signal is present at the prime input pin A31, of supplementary D gate. When D-C is reset, the delete mode indication to the sequence control circuitry is changed to 0 volt. This permits the step pulses in the sequence control to be diverted from the SOM generator to the associated reader.**

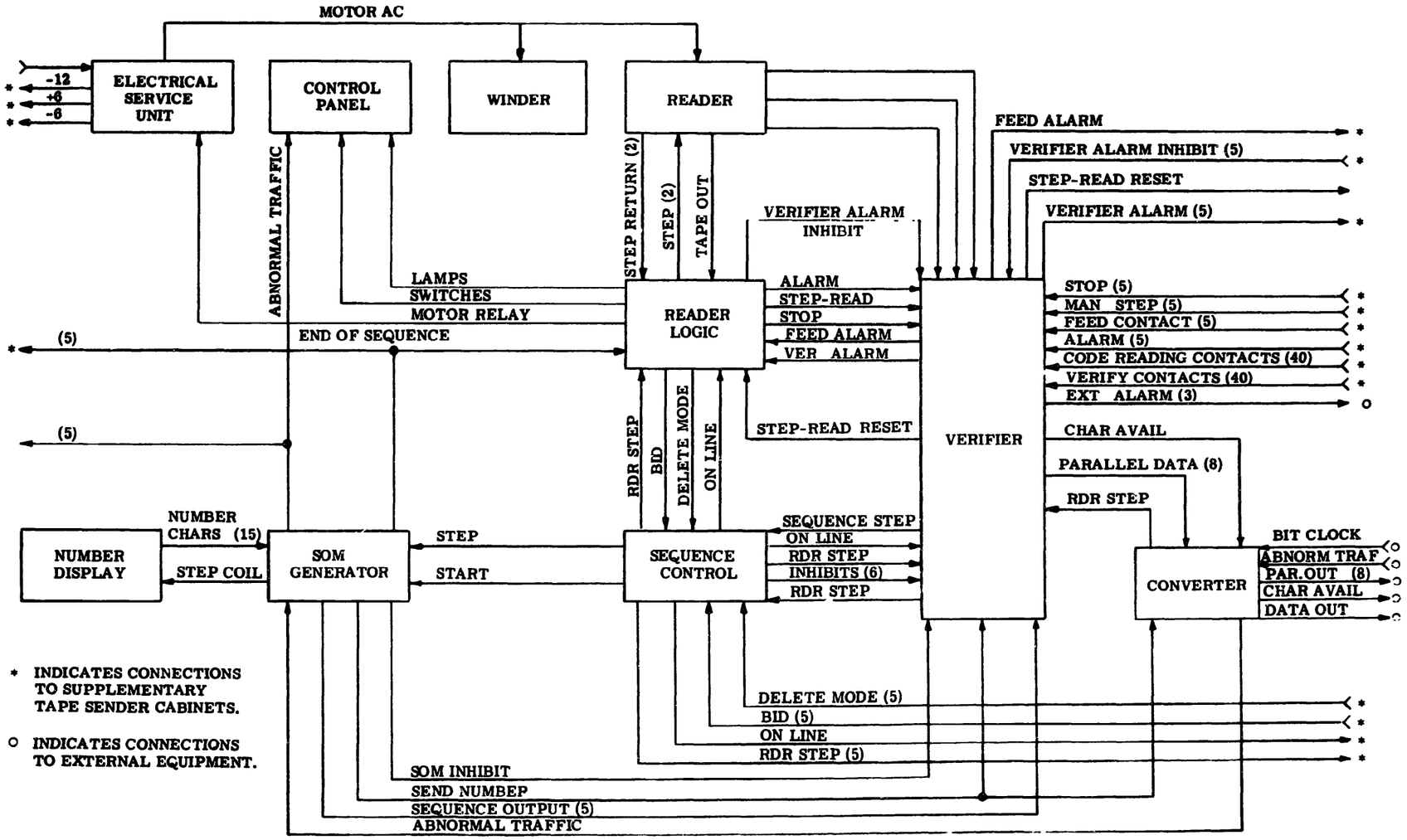

Figure 9- Block Diagram For Master High Speed Tape Sender

Step and Read Circuitry

3.80 During the reading operation, the operator has the option of stopping the reader and stepping it manually with the STEP READ switch. This circuit starts functioning when the STOP switch is operated and the associated STOP lamp is lighted. A level change from 0 to -5 volts is obtained at pin B4 of LA-2A, ZA103. Here again the output of a switch is fed through a dc (direct current) flip-flop configuration to remove contact bounce. Refer to 7716WD, Sheet 4.

3.81 When the reader is operating, the on-line signal input at pin B5 of LA-2A, ZA103 is -5 volts. As a result of the negative level being applied to pin B5 of LA-2A, ZA103 and the level change from 0 to -5 volts at pin B4, due to the STOP switch output, pin A9 is driven to 0 volt. This 0 volt is used as a reader stop signal and as a prime to flip-flop D-F of ZA110. The signal is used to inhibit the pulse to the SOM generator or the reader, thereby stopping operation.

3.82 The prime voltage applied at pin A2 of flip-flop D-F permits the positive transition, appearing at the set input, pin A1, to switch the flip-flop, driving the output pin, B3 to -5 volts. The positive transition at the input pin A1 is a result of operating the STEP READ switch. The output pin B3, of flip-flop D-F on ZA110, is inverted by LA-2E, ZA116 and supplied as a step read pulse. This pulse allows the reader to be stepped one character, and the character read by the reader to be transmitted on-line. To allow the reader to be stepped automatically by the incoming step pulse rate again, the operator presses the STOP switch returning it to the normal condition.

3.83 The reader may also be manually stepped off-line during periods when the reader is not normally being stepped by the incoming pulse rate. The STEP switch output is fed to a dc connected flip-flop configuration consisting of LA-1B, and LA-2B on ZA116. when the STEP switch is operated, a positive transition is obtained at the output pin A11, on the dc flip-flop. This transition is applied to LA-1B, ZA103, for inversion prior to being applied to the input pin B13, of LA-2B, ZA103.

3.84 If the second input pin, B12 of LA-2B is negative at this time, the input at pin B13 will be inverted and appear at the output pin, A11. The input level at pin B12 is 0 volt only when the STOP switch is in its normal position and at the time the on-line signal input is at pin B23 of LA-2C, ZA103 -5 volts. When this condition is met it is assumed the reader is normally being stepped by the incoming pulse rate, the manual step indications must be held.

3.85 The STEP switch is available for stepping the reader manually except when the reader is normally reading tape and stepped by the incoming step pulse rate received at pin D10 of JA128.

3.86 Assuming the input pin B12 of LA-2B, ZA103 is at -5 volts, the manual step indications at input pin B13 appear inverted at the output pin, A11. Then they are inverted twice by LA-2F, ZA103 and LA-1F, ZA116. At the output the manual step indications appear as positive transitions which are applied to the driver assembly..

3.87 The driver assembly is located in the tape transport assembly and functions to change the low-level stepping pulses to a power level adequate for energizing the reader stepping coils. The stepping pulses delivered to the driver assembly come from two sources, one is the STEP switch described in 3.83, and the other is the sequence control circuitry in the master logic. which are applied to pin D10, JA128.

3.88 The LA-1A of ZA321 perform the function of preventing an alarm indication from occuring when the reader is restarted after it has been stopped and manually stepped by means of the STEP switch. This circuit IS required due to the characteristics of the verify logic.

3.89 The description of the following circuit is the same as described in 3.88. Input pin A7 of W-IA. ZA321 samples the condition of the STOP switch. With the STOP switch in the stop condition, this input is -5 volts. Pin B7 of LA-1A, ZA321 samples the on-line signal, which is -5 volts and on at this point. The third input pin. A6 of LA-IA, ZA321 samples the STEP switch output at pin A17 of LA-1B, ZA103. When the STOP switch is operated again. pm A6 of LA-1A, ZA321 is at -5 volts. and the output pin A10 is driven to o volt. This positive transition is applied to the verifier logic where it is used to prevent an alarm on reader start-up when the contacts are again sampled.

Alarm Circuitry

3.90 There are two types of alarms provided in the reader logic. a VERIFIER alarm and a TAPE FEED alarm If either of these two errors occurs, an indication is received at pin A8 or B8 of JA128, setting an associated flip-flop D-D or DE of ZA110. There flip-flops are primed by the presence of an on-line indication. When either of the two flip-flops is set, an associated alarm lamp is lighted and a 0 volt indication is applied at either pin A1 or B1 of LA-2E, ZA103. The output pin B9 of LA-2E, ZA103 as inverted by LA-1E, ZA116 and supplied to the verifier as a 0 volt alarm signal. Refer to 7716WD. Sheet 5.

3.91 To reset the alarm flip-flops and extinguish the alarm indicator lamp or lamps. the operator presses the affected alarm switch. An on-line indicator lamp is lighted when the on-line signal is received. This indicator lamp informs the operator when a particular reader is allowed to transmit after a bid for the line has been entered.

B. Parallel to Serial Converter

3.92 **The primary functions of the parallel to serial converter are as follows: (Refer to 7716WD, Sheets 8 and 9, and Figure 10 for block diagram).**

(a) Accepts an eight-level parallel signal, 0 volt for mark and -5 volts for a space, and converts this signal into a serialized signal output, +6 volts for mark, and -6 volts for space.

(b) Accepts a clock pulse input at the bit rate which determines the speed of operation.

(c) Provides a reader step pulse output at character rate.

(d) Capability of working five through eight-level operation, start-stop or synchronous.

(e) Optional parallel signal output is provided.

3.93 The parallel to serial converter, hereafter referred to as converter, includes a four stage binary counter which is capable of a maximum count of 16. It is also capable of being reset at a specific count by the UNITS PER CHARACTER INTERVAL switch, hereafter referred to as UPCI switch (module A), which will be explained later.

3.94 The counter is reset by a positive pulse coupled through diodes to the 1 side of flip-flops D-B, D-C, D-E, and D-F of ZA307. The positive pulse coupled to flip-flop D-B is first fed through the SIGNAL MODE switch (module A). When the SIGNAL MODE switch is in the START-STOP position, the 1 side of flip-flop D-B is reset to 0 volt by the reset pulse. When the SIGNAL MODE switch is in the SYNCHRONOUS position, the 0 side of flip-flop D-B is set to 0 volt by the reset pulse.

3.95 clock pulses, +6 volts to -6 volts, are fed to input circuit ZA302-A, pin B4. The input circuit converts the polar clock from 0 to -6 volts signal, 0 volt corresponding to a +6 volt input, while -6 volts corresponds to a -6 volt input. This neutral clock is inverted by LA-2D, ZA305 and fed to the input of the binary counter. The output of LA-2D on ZA305 also feeds LA-2B on ZA305. Since the clock has been inverted by LA-2D, ZA305 the counter counts at the negative going clock transitions. The outputs of all stages in the binary counter are fed to power amplifier which in turn feed the UPCI switch. Refer to 7716WD, Sheet 10.

3.96 NOR gates LA-1A, LA-1B, LA-1C, LA-1D, LA-1E, and LA-IF of ZA314 and LA-1B, LA-1D, and LA-1E of ZA305 and their associated OR gates ZA313-22, 21, 20, 19, 18, 17, 16, 15, and 14 detect the count in the counter. When the counter is reset in the start-stop mode, pins A32, B33 of LA-1D on ZA305, and pins A13 and B13 of OR gate ZA313-14 are at -6 volts. The output of 1A-1D, ZA305 is then dependent upon the other input pin B32.

3.97 **LA-1D, ZA305 samples the contents of flip-flop D-E of ZA319 when the counter is at the reset state. When there is a count of one in the counter, the output of LA-1E, ZA305 is dependent upon the input at pin B6 which samples flip-flop D-D of ZA319. Flip-flops D-F of ZA319, D-C, D-F, D-E, and D-D of ZA317; D-B, D-C, D-D, and D-E of ZA319 are sequentially sampled, each for the duration of the bit clock period. When the SIGNAL MODE switch is in the SYNCHRONOUS position, flip-flop D-E of ZA319 is not sampled.**

3.98 **The flip-flops mentioned in 3.97 stores information supplied from the verifier. If the one prime is at 0 volts, the flip-flop will store a mark when a complementary input is supplied a positive pulse. If the 0 prime is at 0 volt, the flip-flop will store a space. The primes for the storage flip-flops determine whether a mark or space is stored in a particular level. At the time a positive pulse is** applied to the converter for **reset, a character shift pulse is** also applied to the complementary **inputs of the storage flip-flops.**

3.99 **The output of the storage flip-flops are fed to program board ZA316 where the customer has the option of either sampling the 1 or 0 sides of the flip-flops. When the 1 side is sampled, a mark at the input will be sampled as a mark at the output. If the 0 side is sampled, a mark at the input will be sampled as a space.**

3.100 The output of NOR gates LA-1A, LA-1B, LA-1C, LA-1D. LA-1E and LA-1F of ZA314, and LA-1B, and LA-1E of ZA-305 are fed to LA-1F, ZA305. The output of LA-1D, ZA305 is fed to NOR gate LA-1F, ZA305 only when the SIGNAL MODE switch is in the START-STOP position. The output of LA-1F, ZZA305 is the serial output. A 0 volt output of LA-1F, ZA305 represents a mark while a -6 volt level represents a space.

3.101 The counter can accept up to sixteen clock pulses before recycling. The number is dependent upon the position of the UPCI switch. If the switch is positioned so the counter counts above eight, each subsequent clock pulse will generate a mark or stop condition, until the counter is reset and again samples the storage flip-flops.

3.102 Levels eight, seven, and one from the verifier are fed through NOR gates 1-F, 1-D, and 2-D of ZA321, respectively. The outputs of these gates are fed to the converter. Levels six, five, four, three and two from the verifier are fed directly to the converter. The character available signal from the verifier also feeds the converter.

3.103 The CODE LEVEL switch (module A), determines the number of code levels that are transmitted. When the switch is in the five-level position a 0 volt level is fed to NOR gate 1-F, 1-D, and 2-D of ZA321 which inhibits these gates. When the switch is in the six-level position, NOR

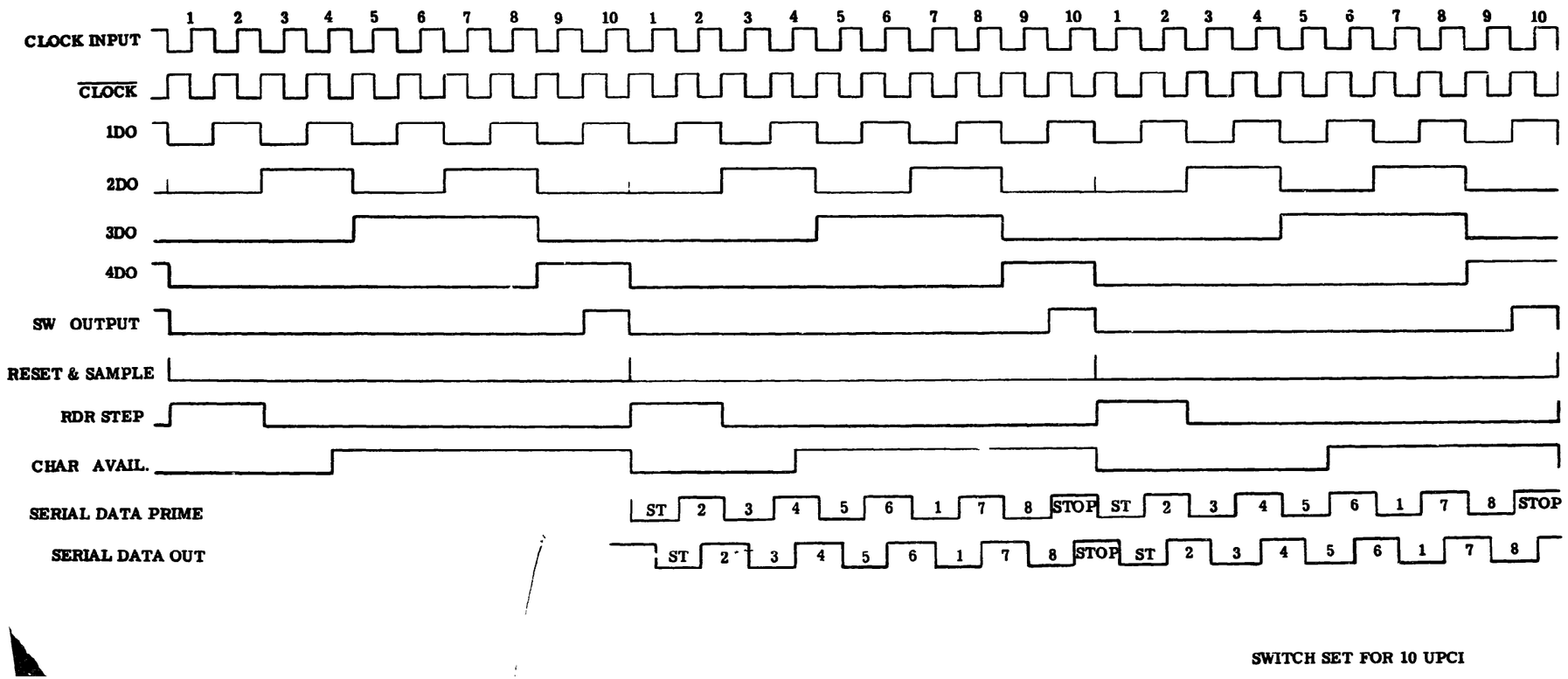

Figure 10- Timing Diagram for Parallel to Send Converter

gates 1-F and 1-D are held and so on through seven and eight levels. When a level is held in this manner, a mark is generated when the storage flip-flop which stores that particular level is sampled.

3.104 The parallel signal output from the verifier is also passed through output circuits ZA323-S, ZA324-B, ZA325-A, ZA325-B, ZA324-A, ZA325-C, ZA324-C, and ZA323-C. The output circuit converts its neutral input, 0 to -6 volts, to a polar output +6 to -6 volts respectively. The output circuits drive integrators, and time constants are determined by the customer. The outputs of the integrators are optional parallel signal outputs.

3.105 The character available signal from the verifier is also fed to the set input two millisecond delay ZA311-A whose prime is permanently grounded. The normal output is fed to output circuit ZA326-A, and the auxiliary character available output is a two millisecond wide positive pulse.

3.106 The UPCI switch is a four section switch which samples the outputs of the binary counter. The four poles of this switch are fed to NOR gate 1A of ZA303. Pin A8 of this gate is fed from OR gates ZA313-13 and 12 which sample the send number lead from the SOM generator. The send number is strapped to either JA128-G4, H4, G3, or H3. During the SOM sequence, the send number lead is a 0 volt which inhibits LA-1A of ZA303, and disables the UPCI switch.

3.107 The output of LA-1A, ZA303 primes pin B4 of LA-2A, ZA303 for its other input pin B5. The latter gate thus samples the combined outputs of NOR gates 1-F, 1-D, 1-B and 1-C, of ZA303. Depending upon where the send number lead is strapped, one of the above named NOR gates will be primed while the others will be inhibited during the SOM sequence. The other inputs of these gates sample the outputs of the binary counter.

3.108 If the send number lead were strapped to JA-128-H3, a count of nine in the counter will place a -6 volts at all the inputs of LA-1C, ZA303 which drives the output to 0 volt. This 0 volt level is fed to already primed LA-2A on ZA303 which inverts the signal and feeds -6 volts to the converter. This -6 volt level is then inverted again by NOR gate LA-2A and LA-2C of ZA314 and appears as a 0 volt level for a count of nine in the counter.

3.109 The outputs of NOR gates LA-2A and LA-2C of ZA314 are fed to PA-F and PA-E of ZA311. When the next clock pulse steps the counter, the output of LA-1C of ZA303 drops to -6 volts. Consequently a negative transition appears at the input of PA-F, and PA-E of ZA311. The positive pulse resulting from the negative transition resets the counter to either 0000 or 0001 depending upon mode of operation.

3.110 The positive pulse at the output of PA-E, ZA311 is fed to the complementary inputs of the storage flip-flops. It is at this time that the information from the verifier is fed into storage and becomes the next character to be transmitted. The positive pulse is also fed to the set one input of flip-flop D-B of ZA317. Refer to 7716WD, Sheet 10.

3.111 At the end of the SOM sequence, the send number lead goes to -6 volts and holds LA-1C of ZA303 placing a -6 volt level at pin A8 of ZA303. NOR gate LA-1A, of ZA303 now samples the UPCI switch. Depending on the position of this switch the counter is either reset on the sixth through sixteenth clock pulse (START-STOP) or fifth through sixteenth (SYNCHRONOUS).

3.112 Flip-flop D-B, ZA317 is reset when the counter steps to a count of two. The normal output of flip-flop D-B is fed to LA-2E of ZA303. At the output of this gate there are negative pulses whose duration is either one or two clock pulses, depending upon the mode of operation. The interval between leading edges is determined by the UPCI switch or send number strap connections (during the SOM sequence). This is the character interval. The output of NOR gate LA-2E of ZA303, the reader step lead, is fed to the verifier where it is used to generate various timing sequences.

3.113 The serial data output from LA-1F of ZA305 primes flip-flop D-D of ZA307. LA-1E of ZA303 inverts the serial data input applied to the prime 0 of the flip-flop in such a way that if the 0 side is primed, the one side prime is at -6 volts or the sequence may be reversed. The bit sample from the converter (which is at clock pulse time) is fed to the complementary input of flip-flop D-D, ZA307.

3.114 Previously it was stated that the counter was stepped by the inverted clock, with the bit sample at clock pulse time. Thus, flip-flop D-D is primed a half of a bit time before bit sample occurs. The output of flip-flop D-D is fed to output circuit ZA323-B where a +6 volt output represents a mark while -6 volt output represents a space.

3.115 A polar (±6 volts) abnormal traffic indication signal on input connector JA128 pin C4 is fed by external equipment to input circuit card ZA302-B. The output of this input card is fed to PA-1C of ZB1315, input pin A9. The output load of this power amplifier is from the coil of relay KB501-B.

3.116 With the abnormal traffic input positive, relay KB501-B is de-energized and the associated contacts are open. Driving the abnormal traffic input negative energizes relay KB501-B. The relay contacts close providing a ground return for the abnormal traffic indicator lamp on the master and supplementary reader cabinets.

C. Sequence Control

3.117 **The sequence control logic assures that only one reader out of the six is capable of supplying signals to the verifier at any one time. (Refer to 7716WD, Sheets 13 and 14.) The circuitry shown on Sheet 13 provides for bid request inputs from up to six readers. Since the logic for each reader is identical, the sequence of operation will be described for reader number three only.**

3.118 **When a bid request (0 volt) is received at pin G2 of JB128 it is inverted twice by LA-2C, ZB520 and LA-2F, ZB505. An inverted signal is taken from pin A26 of ZB520 to be applied to pin B25 of the flip-flop ZB516, D-C as a reset prime. The bid request input therefore primes the flip-flop at pin A24 in preparation for a set one input at pin B24. This pin receives a zero transition from the output of LA-1C, ZB520 at a time when all inputs of this gate go to a -5 volt level. Three of the inputs to this gate sample the output collectors of a three stage counter composed of flip-flops D-F, D-C and D-E, ZB518.**

3.119 The one side of the first stage is sampled at pin B24, the one side of the second stage is sampled at pin B25, and the zero side of the third stage is sampled at pin A24. The fourth gate input is a character clock signal. The third step pulse input to the counter, along with the character clock input at pin A32 of LA-1C ZB520, results in an output at pin A27 of ZA520 as shown in Figure 11. The bid signal input primes pin A24 of flip-flop DC, ZB516 at this time, as shown on Figure 11. The output of ZB520, pin A27 when applied to pin B24 of flip-flop DC, causes it to go to the set condition (Figure 11).

3.120 The resulting 0 volt at pin A32 of flip-flop D-C is also applied to NOR gate LA-1E, ZB522 where it is used as au inhibit signal for subsequent step pulses arriving at pin A2 of this gate. (Figure 11, shows these step pulses being inhibited.) The inverted output of flip-flop d-D, pin B26, which was driven to -5 volts when the flip-flop was set, drives PA-1C, ZB508 into saturation.

3.121 The output pin B16 of the power amplifier provides a 0 volt on line signal to the reader logic. This signal is also applied to pin B5 of PA-2C, ZB508 driving the output pin B4 to -12 volts, de-energizing relay K-3. This opens the associated contacts and removes the ground normally supplied to the verifier logic, permitting the contacts of the associated reader to k sampled.

3.122 The inverted output side of flip-flop D-C, ZB516 also supplies a negative on-line signal to the sequence control logic. The timing diagram, Figure 11, shows the sequence of operation when reader three is given the on-line signal as described in the preceding paragraphs. When transmission for reader three is completed, reader four is given the on-line signal. The step clock gating circuitry, **shown on 7716WD, Sheet 15, performs the function of directing the step pulses to the start of message generator or to any one of six readers. The gate network for all readers are identical so the operation for only reader one will be described.**

3.123 **Whether the step pulses are to be initially directed toward the start of message generator (normal condition) or the reader drive circuitry (delete mode) is dependent upon the delete prime input voltage from the reader logic. When in the normal condition (a start of message sequence is to proceed the message tape) this input voltage is negative. The negative voltage is applied at pin A7 of LA-1A, ZB524 and acts as a prime. It is inverted by LA-2E, ZB524 and applied as an inhibit signal to pin B14 of LA-1B, ZB524.**

3.124 A second input to LA-1A, ZB524 is the negative on-line signal (assuming reader one has the clear line to send) which is applied at pin B7 and also to pin B15 of NOR gate LA-1B, ZB524 as a prime voltage. Two of the three inputs to LA-1A, ZB524 are now primed. The third input, pin A6 receives negative read pulses from the output of LA-2B, ZB524, and LA-1B, ZB-524 receives negative step pulses at pin A13. Since one input of LA-1B, ZB524 is at 0 volt, the output pin A17, remain, at a negative voltage while the output pin A16 of LA-1A, ZB524 supplies positive pubes to the input pin B31 of LA-2D, ZB526.

3.125 The result is a negative pulse output at pin A28 which is supplied as a step pulse to the start of message generator. At the end of the thirteenth character start of message sequence the delete prime input from the reader logic changes to 00volt. This drives the output of LA-1A, ZB524 to -5 volts and primes LA-1B, ZB524. The negative pulses appearing at pin A13 of this gate ate inverted and appear at the output pin A17, as positive step pulses to reader sue. These pulses are also fed to the verifier for alarm purpose.

D. Verifier

3.126 This logic accepts a step pulse from the parallel to serial converter at the character sate. The functions performed are listed in the three following groups:

(a) Inhibiting the step pulse in alarm conditions, and in the stop mode.

(b) Allow a step pulse to k passed when manually stepping the reader.

(c) Generate time slots within the character period, and reference the step pulse for reader contact sampling and verifying.

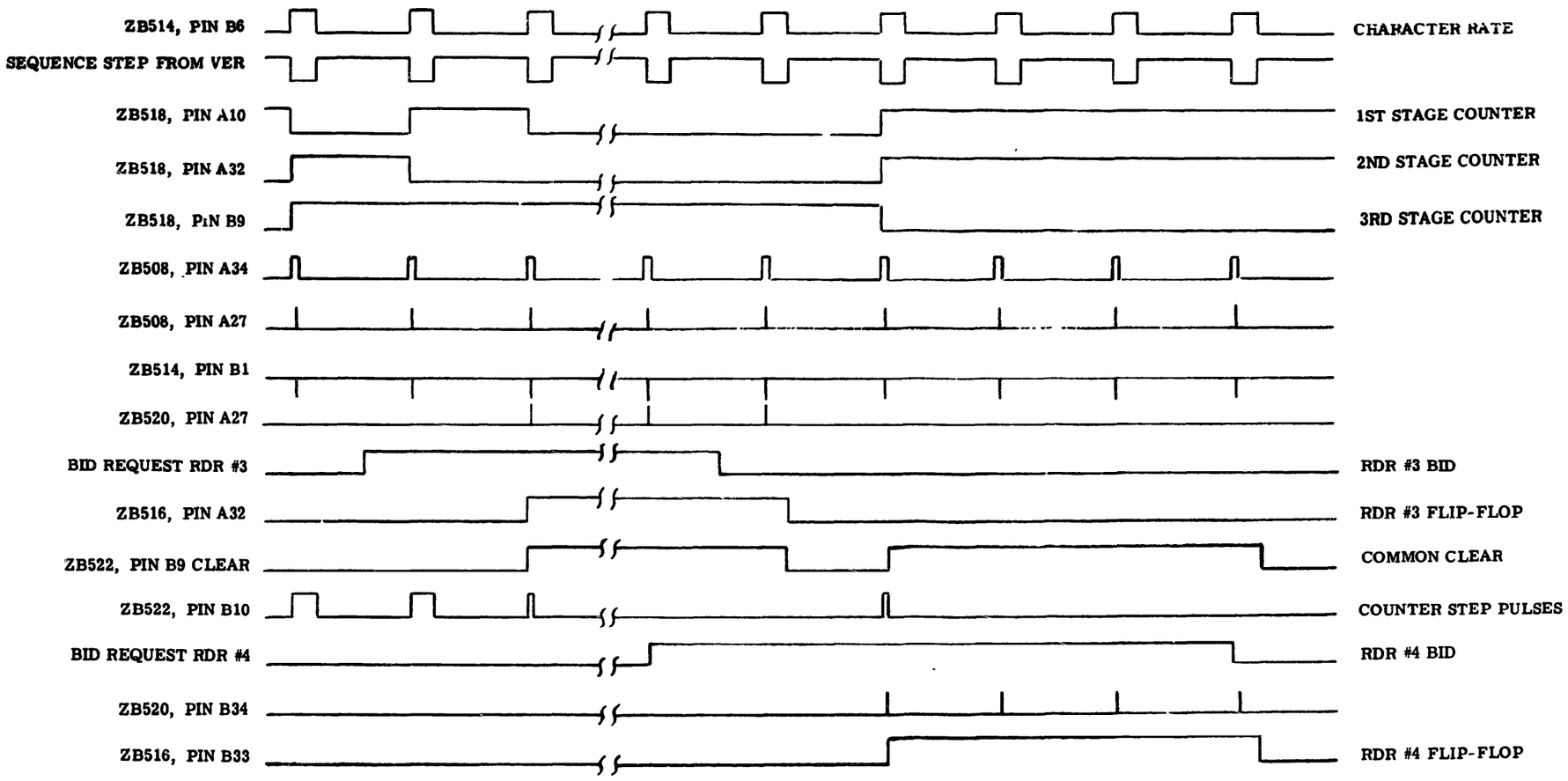

Figure 11- Timing Diagram For Sequence Control

3.127 **The reader stop input is applied at pin C2 of JB128 as a negative pulse (Figure 12). This pulse is inverted by PA-2D, ZB514 and is used to trigger a 50 microsecond delay (DY-A, ZB319). The 50 microsecond delay is used to delay the application of the step pulse at the input, pin A3 of PA-2D, ZB319 until after a reader stop signal has had time to be applied to one of the six inputs to LA-1C, ZB324. The reader stop signal may be applied at any time during reader operation or at the time a reader is given the on-line signal.**

2.128 **In the latter case the on-line to the reader logic occurs at reader step time. Therefore the reader stop signal will be applied at one of the six inputs to LA-1C, ZB324 at the reader step time, causing the input pin A4 of PA-2D, ZB319 to be driven to zero, disabling the input at pin A3. Fifty microseconds later the delayed step pulse will be applied at pin A3. This action permits the operator to bid for the line with the reader logic in the stop mode. Then manually step through the start-of-message sequence or the message tape when in the number delete mode.**

3.129 Pulse amplifier PA-E, ZB319 provides **a** positive pulse at the trailing edge (negative transition) of the 50 microsecond delay (Figure 12). The pulse is inverted by LA-2C, ZB324 and applied to pin A3 of PA-2D, ZB319. If a 0 volt (reader stop), **signal** is not present at any one of the six inputs of LA-1C, ZB324 a positive level will appear at the **output pin, A27. this level under normal conditions will be** inverted by LA-2B, ZB522 and applied as a negative input at pin A4 of PA-2D, ZB319. The pulse appearing at pin A3 is then allowed to pass to the output pin A1, as **a** positive pulse. Here it is used as a prime at pin A4 of PA-2D, ZB319.

3.130 If a 0 volt (reader stop) signal is present at one of the inputs to OR gate LA-1C, ZB324 (Figure 12). the output pin A27, is driven negative. This prevents the passage of step pulses at PA-2D, ZB319, pin A3 by the presence of 0 volt at pin A1. The following paragraphs explain how a single step pulse is developed after a reader stop signal has been received.

3.131 A positive manual step signal is applied at one of the **six inputs to** LA-1A, ZB324 (Figure 12). It is inverted twice and used as a prime one pulse at pin B14 of flip-flop D-D, ZB322 which is then set by the next step pulse. Flip-flop D-D and D-C, are normally in the reset state (pins B22 an B26 at 0 volt). When power is turned on, the flip-flops do not assume this state, the normal flow of step pulses **at** pins A22 and A25 will cause the flip-flops to be **driven into this state.**

3.132 When flip-flop D-D is set the output pm A22, is driven to -5 volts. Both inputs to LA-2C, ZB522 are now at -5 volts, allowing the output pm A26 to go to 0 volt which is used as **a** prime one input, for flip-flop D-C, ZB322. On arrival of the next step pulse at pm A25 this flip-flop is driven to the set one state, allowing the output pm A32 to go to 0 volt (Figure 12). This 0 volt is applied at pin B12 of LA-2B, ZB522 and drives the output pin All. negative.

3.133 The negative voltage at pin A11 is used as a prime at pin A4 of PA-2D, ZB319. Fifty microseconds later a negative pulse is applied at the second input pin A3 of this gate causing a positive pulse output at pin A1 (Figure 12). This pulse has the same time reference and is used to perform the same functions as the normal step pulse stream, **but** only one pulse is generated for each application of **a** manual step pulse.

3.134 After flip-flop D-C of ZB322 bar been set. it primes itself and flip-flop D-D, ZB322 for reset. The output pin A32, is 0 volt at this time. This 0 volt as applied at pin B22 of LA-2C, ZB522 and removes the prime one voltage at pin A24 of ZB322. Pin B23 of flip-flop D-D and pin B25 of flip-flop D-C are primed for the following reader step pulse which resets both flip-flops.

3.135 The step pulses are passed though PA-2D, ZB319. The second input pin A4. of this element is -5 volts at this tune. If there is no alarm indication from any one of the six readers as sampled by NOR gate LA-1E, ZB324 (7716WD. Sheet 19). and no voltage supplied to pin B25 of LA-1C, ZB324 the voltage at pin A4 of PA-2D will remain at -5 volts.

3.136 When an alarm indication is received, the voltage at pm A4 of the power amplifier is driven to 0 volt. This prevents step pulses appearing at pin A3 to be passed to the output pin A1, thereby stopping reader operation. This 0 volt IS also applied at the input pm B33 of PA-1D, ZB319 (Sheet 19) which de-energizes the alarm relay KB-501-A. When KB-501-A de-energizes. the transfer contact at pins B1. C1, and D1 of JB326 changes state. This indication of an alarm IS supplied to external equipment.

3.137 During normal operating conditions reader step pulses are present at the output of PA-2D. ZB319. pm Al. From here the pulses arc fed to the sequence control **logic** for stepping either the start of message generator or the reader. The step pulses are also applied to the input pm A22 of the 800 microsecond delay DY-B. ZB317. The output IS taken from the normal side, B27 and is an 800 microsecond positive pulse. At the trailing edge of this pulse. a positive pulse is developed by PA-F. ZB512. pin B11 (Figure 12). where it IS inverted by PA-2C. ZB319 and applied as a negative reset pulse to the verifier logic.

3.138 This reset pulse IS the first of four time slots which are referenced to the step pulse and arc developed within each character period These time slots arc used for reading and verifying the reader contact information. The reset pulse IS used to reset the contact sampling circuit prior to reading a new character

3.139 The second time slot is developed by 1.6 millisecond delay, DY-A, ZB317 and PA-F, ZB317. The output pin B11 of ZB317 is inverted by PA-2C, ZB317 and is applied as a negative verifier sample pulse to the verifier logic. This pulse is used to sample the reader verifying contacts, and occurs 1.6 milliseconds after the reset pulse or 2.4 milliseconds after the step pulse (Figure 12).

3.140 The third time slot is developed by 110 microsecond delay DY-B, ZB315 and PA-E, ZB317. This pulse is used to set the verifier alarm flip-flop D-B, ZB322 if a verifier error indication is present. The positive pulse output of pin A27, ZB317 (Figure 12) is inverted by LA-2D, ZB324 and applied to pin B5 of NOR gate LA-2A, ZB324. If the second input of this gate is -5 volts at this time, the pulse will be applied at the set one input pin A36, of flip-flop D-B, sampling the prime **at** pin A35 (refer to 7716WD. Sheet 19).

3.141 Pin B4 of LA-2A, ZB324 receives its voltage from the inverted output, pin B10 of flip-flop D-E, ZE322 (refer to 7716WD. **Sheet** 18). This flip-flop is normally reset, making **the output** 0 volt, due to the reset pulse being fed to the 50 microsecond delay, DY-B, ZB319. A pulse is also generated by PA-E, ZB512 and applied to the reset input pin B12 of ZB322. The output pin B19, is not driven to -5 volts until an on-line and not send number signal is present at the prime one input pin A12, and a set pulse is applied at pin A11.

3.142 This set puke on pin A11 is developed by the 110 microsecond delay DY-A, ZB315, and PA-E, ZB315. It is the fourth and last time slot developed during the character period, and determines the time that the character being read by the reader contacts is places in the verifier storage. This is the pulse that sets flip-flop D-E, driving pin B10 to -5 volts. Pin B4 of LA-2A, ZB324 (refer to 7716WD, Sheet 19) will not be printed until the first read pulse has occurred after an on-line is present. Therefore, the first verifier alarm sample pulse is inhibited.

3.143 The prime for the verifier alarm flip-flop D-B, ZB322 is applied at pin A35 and is supplied by the **output of NOR gate LA-1B, ZB324. If all inputs of this gate are -5 volts the output is 0 volt (error condition). Input B15 is supplied by the start of message generator and is driven to 0 volt when this circuit is generating a sequence. This input inhibits a verifier alarm during the start of message sequence.**

3.144 During normal reader stepping B15 of LA-1B, is it -5 volts and the second input pin A14, is at 0 volts until an error is detected. When an error is detected, input A14 is driven negative causing the output pin A17 to go to 0 volt, priming flip-flop D-B for the next alarm sample puke.

3.145 When the verifier alarm flip-flops D-B is set, pin B33 goes from -5 volts to 0 volt, which is inverted by PA-1C, ZB319 and supplied as a negative alarm indication to the reader logic. The alarm flip-flop is reset by by the follo**wing** reader step pulse applied at pin B36.

3.146 **Flip-flop** D-F, ZB322 **(refer to 7716WD, Sheet 18) is used to provide a character available signal to the parallel to serial converter and the signal gating. The flip-flop is normally reset by the delayed alarm sample pulse input at pin B1. When an on-line signal is received at the prime input pin A2, the next read pulse applied at pin A1 will set the flip-flop and pavovide a character available signal. It remains in this state until the next step pulse at pin B1, causes the flip-flop to reset.**

3.147 **If an on-line signal is still present for the next character, the following read pulse will again set the flip-flop to the character available state. This action continues until the on-line is removed or an alarm condition inhibits the read pulses causing the flip-flop to remain in the reset state.**

3.148 **The verifier logic performs the function of sampling the code reading and verifier contacts of the operating reader, placing the code reading information in storage and later clearing the storage with the verifier information. The outputs of the storage register, supply an alarm condition at the alarm sample time, if all levels of the register are not properly cleared by the verifier information prior to this sample time.**

3.149 Input provisions are made for 6 readers with 17 contacts per reader: 8 reading, 8 verify and 1 feed. Since the logic for all levels is identical, only level number one will be described.

3.150 Assuming reader number one is operating, the code reading contact indication is applied at pin A10 of JB228 (refer to 7716WD. Sheet 16). The verifier contact **indication is applied at pin G10 of JE228. The contact configuration for each input is as shown in the reference block. When the contact is detecting a hole (mark) it is closed to ground. When the contact is detecting no hole (space) it is open.**

3.151 **The code reading contact signal at pin A10 of JB228 is applied to pin B26 of NAND gate, ZB124-A. It will be permitted to pass to the output pin A29, provided the inhibited input appearing at pin B6 of the gate has been opened. The other five inhibit inputs from the sequence control are held at ground at this time permitting only the contact signals from reader number one to be capable of supplying an output at pin A29.**

3.152 **When the contact detects a hole (mark) the output pin A29 of the gate goes to -5 volts. When a no hole (space) is detected the output is driven to 0 volt. These levels are inverted by LA-1D, ZB118 resulting in 0 volt for a mark and -5 volts for a space at the output pin B34. This output is applied to LA-2D, ZB118 which is connected in conjunction with LA-1F, ZB118 to function as a dc flip-flop.**

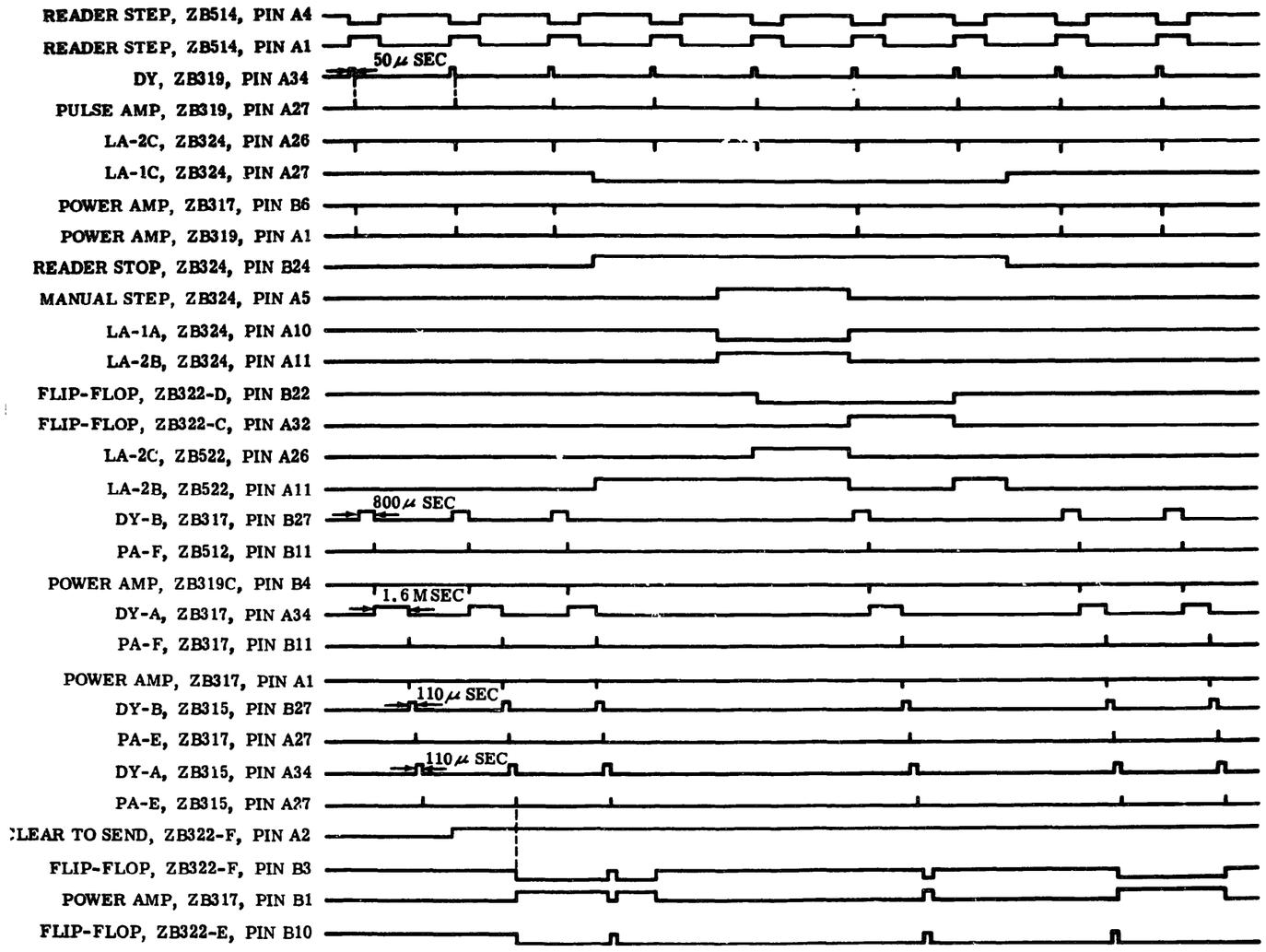

Figure 12- Timing Diagram for Verifier

3.153 With a mark being read by the contact, 0 volt is applied at pin B31 of LA-2D driving pin A28 to -5 volts. This -5 volts is applied to pin B36, of LA-1F. With the second input of this gate at -5 volts the output pin B28 is driven to 0 volts which is fed back to LA-2D at pin B30 clamping the network into the mark condition. The 0 volt present at the output of LA-1F is also applied to pin A29 of supplementary D gate ZB108 where it is used as a prime for the read sample pulse applied to pin B30.

3.154 The output of LA-2D which is -5 volts at this time is applied at pin A30 of supplementary flip-flop ZB108 inhibiting the read sample pulse applied to pin B32. Flip-flop D-B, ZB108 is now primed to be set on the arrival of a read sample pulse, which will drive pin B33 to 0 volt. This mark condition will remain in storage until the next character.

3.155 At the beginning of the next character period, the reader is supplied a step pulse, 800 microseconds later a reset pulse is generated and supplied as a positive pulse to pin A34 of LA-1F, ZB118. At this time the reader has stepped and is now reading the next character due to the step command of the previous character. Assuming the character now being read is a space, the voltage applied at pin B31 of LA-2D is -5 volts.

3.156 When the reset pulse is applied to LA-1F, pin B28 is driven to -5 volts which is fed back to pin B30 of LA-2D. This results in pin A28 going to 0 volt and holding the output of LA-1F at -5 volts. The dc flip-flop has thereby been reset by the application of the reset pulse and is reset because the reader output is spacing.

3.157 The next pulse occurring after the reset pulse is the verify sample pulse. This negative pulse is applied at pin A7 of LA-1A, ZB110 and is used to sample the output of the dc flip-flop network consisting of LA-2C and LA-2D, ZB118. This output is applied to pin A6 of LA-1A.

3.158 The gated NAND, ZB124-B is now sampling the readers verify contact, which at this time should be reading the bit previously under the read contact. Since that bit was a mark, the voltage at the gated output pin A31, is -5 volts. This -5 volts is inverted by LA-1C, ZB118 and applied to the input pin B23, of LA-2C, ZB118 driving the output to -5 volts. This voltage is sampled by the verify sample pulse.

3.159 When it is -5 volts, a positive pulse is developed at the output pin A10, LA-1A of ZB110 which is applied to complimentary input pin A36, of flip-flop D-B. This pulse resets the flip-flop (which was set previously) driving pin B33 to -5 volts to remove the alarm indication.

3.160 The next tune slot in the character period is the alarm sample pulse. This occurs 110 microseconds after the verify sample pulse. If the 0 volt at pin B33 of flip-flop D-B has not been removed by the verify sample pulse, the alarm sample pulse causes an alarm. If the code reading contact had supplied a space indication instead of a mark, flip-flop D-B would have been reset at the time of the read sample pulse.

3.161 One character after the read sample puke. the verify contact would have indicated a space. which would have resulted in the inhibit voltage at the input of LA-1A. This presents the verify sample pulse from reaching the complementary input pm A%. of flip-flop D-B. The flip-flop remains in the reset state (pm B33 at -5 volts) and no alarm condition is detected by the alarm sample pulse which occurs 110 microseconds later.

3.162 All eight levels are treated in the same manner When **a** mark is detected by the code reading contact, the storage flip-flop is set at the read sample tune. If a space IS detected the storage flip-flop is not set. One character later, if **a** mark is detected by the verify contact. **a** complementing input pulse is applied to the flip-flop. If a space is detected the complementing input pulse is inhibited and the flip-flop is not switched.

3.163 Logic identical to that described in the preceding paragraph pertaining to levels 5, 6, 7, and 8 appears on Sheet 17 (7716WD). The logic appearing on Sheet 20 is used fur sampling and detecting a reader feed error. Gated NAND ZB120-A. samples the feed contact from up to six readers and supplied an output at pm A29. The six inhibit inputs from the sequence control logic determine which feed contact input will control the output. Only one is permitted to do to **at** any one time.

3.164 If any one of the six readers is receiving step pukes these step pulses will be gated and averted at NOR gate LA-1F, ZB522. A step pulse will be developed by PA-F. ZB510 and applied as **a** step pulse to the four stage **counter.** The state of the four flip-flops is sampled by LA-1D, ZB324. If the counter is reset and then allowed to receive 15 step pulses, LA-1D, ZB324 will supply **a** 0 volt output at pin B34. This 0 volt level will be inverted by lA-1F. ZB324 and PA-X, ZB514 and be supplied as a 0 volt feed alarm indication to the reader logic.

3.165 Normally pin A29 of ZB120-A is at -5 volts (feed contact closed). When the reader steps, the paper tape move forcing the feed contact to open until the next feed hole is sensed by the contact, and will close again. The contact remains closed until the reader is stepped again and the contact will be forced open as before.

3.166 As **a** result of stepping the reader. a transition is obtained at pin A29 of ZB120-A. This positive transition is inverted by LA-2F. ZB110 and applied to PA-F.

ZB514. The positive pulse output of PA-F is applied as a reset pulse to the four stage counter.

3.167 The alarm indication is inhibited if the feed indication has been received prior to 15 step pulses. Had a feed indication not been received, the counter would not have been reset and an alarm indication would have been generated.

Signal Gating

3.168 The logic appearing on Sheet 12 (7716WD) performs the function of presenting to the parallel to serial converter one of the three following signals:

(a) The output from the reader via the verifier register.

(b) The output of the start of message generator (SOM).

(c) The no character available signal (all levels marking).

3.169 In the no character available condition, -5 volts is applied to pin A8 of PA-2C, ZB317. The output pin B4 is driven to 0 volt which is applied to eight second-level gates, driving the outputs to -5 volts. These -5 volt outputs are inverted by eight inverters and supplied to the parallel to serial converter as 0 volt mark signals.

3.170 When the SOM generator is operating, the send number indication from the SOM generator is 0 volt. This is applied to all eight first level gates driving the outputs to -5 volts. This inhibits the reader information which is being sampled at the verifier storage.

3.171 The -5 volt outputs from the first level gates are applied to the inputs of the second level gates to act as primes at each gate. A second input to each second level gate is a character available indication which is -5 volts at this time.

3.172 The two inputs of each second level NOR gate servicing code levels 1, 7, and 8 have all been supplied with -5 volts resulting in a 0 volt output from each gate. This is inverted and supplied as a -5 volt space indication to the parallel to serial converter. Since the start of message generator sequence is 5-level code only, the space indications on these remaining three levels are required to inhibit perforating these levels at the receiving set.

3.173 The output from the start of message generator is supplied to each of the five, three input second level gates, associated with code levels 2, 3, 4, 5, and 6. The 0 volt designates a mark and -5 volts designates a space. With the other two inputs primed as explained in the previous paragraph, the mark-space indication is inverted at the output of the NOR gates and again at the inverters resulting in 0 volt for a mark and -5 volts for a space. This information is supplied to the parallel to serial converter.

3.174 In the case where the reader is supplying information to the parallel to serial converter, this information is supplied at one of the inputs to each of the first level gates (0 volt is a space, -5 volts is a mark). The second input to the gates is supplied by the send number signal from the SOM generator which is -5 volts at this time. The data input is therefore inverted by the first level gates, and applied to the input of each of the second level gates.

3.175 A second input to each second level gate is the character available signal which is -5 volts at this time, as in the SOM generator output. At the output of the second level gates the reader information is 0 volt for space and -5 volts for mark. This is inverted by the inverters and applied to the parallel to serial converter as a 0 volt for mark and a -5 volts for space.

E. Start of Message Generator (SOM)

3.176 The start of message generator, referred to as the SOM generator, is explained in 2.28. The 13 character sequence is capable of being distributed at 2400 WPM, utilizing the five level Baudot code. The number display assembly (master control panel), gives a visual indication of the next number to be generated.

3.177 The SOM generator uses a four stage counter made up of flip-flops D-B, D-C, D-E, and D-F, ZB307 (7716WD, Sheet 22). A detect network consisting of NOR gates LA-1A, LA-1B, LA-1C, LA-1D, LA-1E, LA-1F, of ZB311, LA-1A, LA-1B, LA-1C, LA-1D, LA-1E, LA-1F, of ZB309 and LA-1A, LA-1D of ZB305 which detects the count in the counter as the counter steps. The outputs of the above named gates are numbered one through thirteen corresponding to the count which each gate detects. The numbered output also indicates the gates driven (Sheet 25).

3.178 The NOR gate LA-1D, ZB305 detects the reset condition of the counter. The collectors of the flip-flops in the counter, feed NOR gates, which in turn feed the detect network. The purpose of these in between gates is to reduce the loading on each flip-flop in the counter.

3.179 When the counter leaves the reset condition there is at least one input of NOR gate LA-1D, ZB305 that is at 0 volt. For the duration of the SOM sequence the output of this gate is a -6 volts, this negative level is fed to PA-1D and PA-2D, ZB313. Power amplifier PA-2D energizes relay KB501-C which energizes the stepping magnets located in the number display.

3.180 Relay KB501-C stays energized for the entire SOM sequence. When the counter resets, PA-2D deenergizes KB501-C and the stepping magnets. The number

display steps one character. Therefore at reset, the number display steps and indicates the next message number to be sent.

3.181 The -6 volt level at pin B3 of PA-1D, ZB313 during the SOM sequence is inverted by this power amplifier, and fed to LA-1B of ZB324 where it inhibits the verifier alarm during the SOM sequence. The output of PA-1D on ZB313 is also fed to the verifier, (Sheet 12, 7716WD). During the SOM sequence, this output also inhibits the gates that sample the output of the reader.

3.183 The output of PA-1C, feeds three points:

(1) NOR gate LA-2F, ZB302 (7716WD, Sheet 25).

(2) Set input of DY-B, ZB512.

(3) Power amplifier PA-2C, ZB313.

During the SOM sequence, the -6 volt level appearing at the input of NOR gate LA-2F, ZB302 is inverted and fed to the parallel to serial converter (Sheet 10) where it inhibits the UPCI switch (module A) for the duration of the SOM sequence.

3.183 The output of NOR gate LA-2F also feeds PA-1D, ZB315. During the SOM sequence, the -6 volt level at the output of this power amplifier primes the output gates of the SOM generator. At the end of the SOM sequence, the output of NOR gate LA-2F, drops to -6 volts, which enables the UPCI switch to perform its function. The output of PA-1D deprimes the output gates of the SOM generator.

3.184 Upon reset of the SOM counter, a positive transition appears at the output of PA-1C, ZA313, (Sheet 22, 7716WD). This triggers DY-B, ZB512 since its prime is permanently at 0 volt. The normal output is fed to NOR gate LA-1C, ZB305 where it acts as a prime for the SOM pulses which originate in the sequence control. When triggered, the delay times out for 225 milliseconds, depriming NOR gate LA-1C.

3.185 The purpose of applying 0 volt at pin A24, of this gate during this period, is to prevent the counter from being retriggered. The delay is required due to the stepping mechanism which drives the number display. Since it takes a positive transition to trigger the delay, the delay will only be triggered when the counter reaches reset.

3.186 The output of NOR gate LA-1C, ZB305 is fed through diode CR-C of ZB108 to the direct base input of NOR gate LA-1D, ZB305. The positive SOM step pulses at this point prevent possible unwanted switching transients to appear at the output of NOR gate LA-1D, ZB305.

3.187 Upon receipt of the first SOM step pulse the counter steps off reset. The first gate in the detect network, LA-1A. ZB311 detects the first count (all of its inputs are negative) and drives its output to 0 volt. During the first character interval. the other NOR gates in the detect network all have at least one 0 volt input, therefore the outputs of these gates are negative at this time.

3.188 For the first character it has been shown that the output of NOR gate LA-1A. ZB311 is 0 volt. This output is fed to NOR gates LA-1A and LA-1E, ZB302 (Sheet 25, 7716WD), where it is inverted and applied to the already primed gates LA-2E and LA-2A, ZB302 producing a 0 volt level at the output of these gates. levels six and two respectively.

3.189 Since the inputs of gates LA-1B. LA-1C, and LA-1D. ZB302 are at -6 volts during the first character, the outputs of these gates are at 0 volt. This level is inverted by output gates LA-2B. LA-2C. and LA-2D, ZB302 producing -6 volts at the outputs of these gates. For the first character levels two and six are marking. while levels three, four and five are spacing. representing the letter Z.

3.190 The second SOM step pulse steps the counter which drives the outputs of LA-1A. ZB311 to -6 volts and LA-1B. ZB311 to 0 volt. indicating a count of two in the counter. The 0 volt level at the output of LA-1B, ZB311 is fed to LA-1B. and LA-1D. ZB302 and OR gate ZB304-8. The 0 volt input to OR gate ZB304-8 drives its output to 0 volt which in turn drives the output of LA-1C, ZB302 to -6 volts. Therefore the second character levels, three, four and five are marking while levels two. and six are spacing, generating the letter C for the second character in the SOM (refer to Sheets 23 and 25. 7716WD).

3.191 The third through seventh step pulses generate the appropriate characters The eighth step pulse drives the output of LA-1B. ZB309 to 0 volt. which is inverted by LA-1F, ZB302 (Sheet 25. 7716WD) and reinverted by PA-2C, ZB315. The five switches on the front panel of module B permit the operator to feed this 0 volt level at the output of PA-2C, ZB315 to OR gates ZB304-22, 16, 7, 3, and 10 for levels six, five, four. three and two respectively. This 0 volt level applied to these OR gates supplies a mark signal to these particular levels.

3.192 The ninth SOM generator step pulse generates a figures character During the tenth step period the output of NOR gate LA-1D, ZB309 is 0 volt which is inverted by NOR gates LA-1E and LA-2E, ZB503 (Sheet 24, 7716WD). The -6 volt level appearing at the outputs of the gates mentioned above, primes NOR gates LA-1A, LA-2A, LA-1B, and LA-1C, of ZB503. The outputs of these gates are therefore dependent upon their other inputs on pins A6, B4, B15, B12, and B25.

3.193 The inputs for the above named gates are supplied by the Baudot coded switch assembly located in the number display assembly. The outputs of these gates are fed to their number identifying inputs of OR gates ZB304-22, 11, 17, 20, and 21, and NOR gates LA-1B, LA-1C, LA-1D, and LA-1E on ZB302. Therefore, a -6 volt level at an input of NOR gates LA-1A, LA-2A, LA-1B, LA-2B, and LA-1C of ZB503 generates a mark in their respective level.

3.194 The next two numerical characters are generated by the same means, utilizing different levels of the Baudot coded switch. The 13 SOM step pulse generates a letters character during that interval. At this time the output of PA-2C, ZB315 goes to -6 volts. The output of this power amplifier is fed to the reader logic (Sheet 3, 7716WD). This -6 volt step is inverted and sets flip-flop D-C of ZA112. The output of this flip-flop is fed to step clock gating (module B) Sheet 15 where it prevents subsequent SOM step pulses from reaching the SOM counter and now permits the next reader step pulse to be fed to the reader logic on Sheet 4.

3.195 The 14 SOM step pulse causes the output of NOR gate LA-1A, ZB305 to go to -6 volts. This negative transition is fed to PA-E, ZB313 (Sheet 22, 7716WD) causing a positive pulse at its output. This pulse is coupled through diodes to the normal outputs of the flip-flops in the SOM counter, driving them to 0 volt, or the reset condition.

Master Transmitter Power Distribution

3.196 Alternating current (ac) is connected to the cabinet at TBG101 (Sheet 7, 7716WD), and passes through the main circuit breaker CBG101 (15 ampere). From this circuit breaker (CBG101) power is distributed to various components and assemblies throughout the cabinet. Power receptacle is provided and protected by its own 5 ampere circuit breaker. The POWER indicator switch controls power to all equipment in the cabinet by operating a silicon bidirectional switch SWG102. This switch provides power to the reader driver assembly, the power supply (protected by a 3 ampere circuit breaker), and to silicon bidirectional switch SWG101.

3.197 The SWG101 switch is controlled by relay K1 and controls power to the reader and winder motors. Relay K1 is controlled by the MOTORS indicator switch, which controls the indicator lamp. Power amplifier PA-1D, ZA108 can turn on the motors even if the MOTORS switch is off by energizing K1 through CR-B, ZA110. This power amplifier also operates relay K2 which energizes the BID lamp and, through a diode, the MOTORS lamp. The diodes prevent a bid from being indicated when the MOTORS switch is turned on. The power amplifier input is shown on Sheet 2 (7716WD).

Supplementary Power Distribution

3.198 The ac portions of this circuit (Sheet 6, 7716WD) are exactly the same as those described in 3.196 and 3.197 except for component designations and the addition of relay KF100. This relay operates when power is applied to the silicon bidirectional switch controlling the motors through the 4 ampere circuit breaker CBF102. When KF101 operates it connects the supplementary station equipment to the -12 volt, -6 volt, and +6 volt power supply leads. Each of these voltages is individually protected by a circuit breaker. PA-1D, ZE180 drives bid relay K2 as shown on Sheet 2.

Power Supply

3.199 The power supply (Sheet 6, 7716WD) produces outputs of 28 volts, 48 volts, -12 volts, -6 volts, and +6 volts. Each of these outputs is associated with a separate winding on transformer VR1, and each output circuit has its own full-wave rectifier, filter capacitor, and bleeder resistor. VR1 is a ferroresonent transformer which compensates for power line voltage variations. The -6 volt and +6 volt outputs are electronically regulated. In the -6 volt regulator, transistors Q5 and Q6 are in parallel and connected in series with the load. The 0.1 ohm resistors in the emitter circuits help to divide the load current equally between the two transistors. The Q5 and Q6 receive their base current through emitter-follower transistor Q2.

3.200 Transistor Q2 receives base current through R6 from the -12 volt supply. Some of this base current is diverted to ground through Q1 and CR11. Resistor R7 provides a drain for the leakage currents of Q5 and Q6. The CR11 maintains a constant voltage of -4.7 at the emitter of Q1 regardless of the current through Q1. Base current to Q1 is supplied from the output terminal through the voltage divider composed of R11, R10, and R9. If the output of the supply should go more negative the base of Q1 would go more negative while the voltage at the emitter of Q1 would not change.

3.201 The negative change would increase the base current of Q1, therefore increasing the collector current. This would make less current available for the base of Q2, causing a reduced current into the bases of Q5 and Q6 reducing the load voltage, correcting for the change. Similarly, if the load voltage should go less negative the base current of Q1 would be reduced, making more base current available for Q2. This would allow more current to flow through Q5 and Q6 returning the output voltage to its correct value. The +6 volt regulator operation is exactly the same as that of the -6 volt regulator except that only one series pass transistor is used.

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MASTER AND SUPPLEMENTARY HIGH SPEED TAPE SENDERS FOR MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS) INSTALLATION

CONTENTS PAGE

1. GENERAL

1.01 This section covers the installation of the master and supplementary high speed tape sender. it is reissued to provide the latest engineering changes, remove preliminary from the title and male this a standard publication. Since this is a general revision, marginal arrows that indicate changes have been omitted.

1.02 Each master and supplementary transmitter set incorporates a high speed tape reader (DX) with a 600-foot tape supply container and tape wind-up mechanism. **The sets are packaged in separate cabinets and interconnected with appropriate cabling.**

1.03 **Tape reader, tape handling, tape supply, electronic logic, power supplies, and most maintenance duties are accessible from the front of the cabinets. Terminal board and power cable connections are made at the rear of the cabinets. Controls and message numbering displays are located in the control panel on top of the cabinet (Figure 1 and Figure 2).**

1.04 **All references to left or right, front or rear, up or down are made from a normal operating position in front of the cabinet.**

2. TECHNICAL DATA

2.01 A 15 ampere, three-wire power cable is required for each tender cabinet. A master or supplementary transmitter set requires a voltage of 117 vac ±10%, and a single phase frequency of 58.5 to 61.5 hertz. Power consumption measurements for both types of senders operating on 117 vac, 60 hertz power are listed in **Table** A. **All** figures were obtained with a matter or supplementary sender transmitting an eight-level message at a speed of 2400 words per minute.

2.02 The dc power required by a supplementary sender is obtained from a master sender. The first line of measurements in Table A were taken on the master sender without any supplementary senders connected to the master sender. The second line of measurements were taken with five supplementary senders turned on and connected to a master sender. The third line of measurements is for a single supplementary sender connected to a master sender.

TABLE A

CONSUMPTION POWER MEASUREMENTS

UNIT	RUNNING CURRENT (AMPERES)	APPARENT (VOLT-AMPERES)	ACTUAL (WATTS)	POWER FACTOR (LAG-GING)
MASTER SENDER	2.85	333	287	0.86
MASTER SENDER	3.45	405	362	0.89
SUPPLE-MENTARY SENDER	2.20	258	208	0.81

2.03 The ambient room temperature should be within +40 degrees fahrenheit to 110 degrees fahreheit range. For reliable system operation, sufficient air space is necessary for each cabinet to prevent recirculation of room air in excess of 110 degrees fahrenheit. Operating humidity

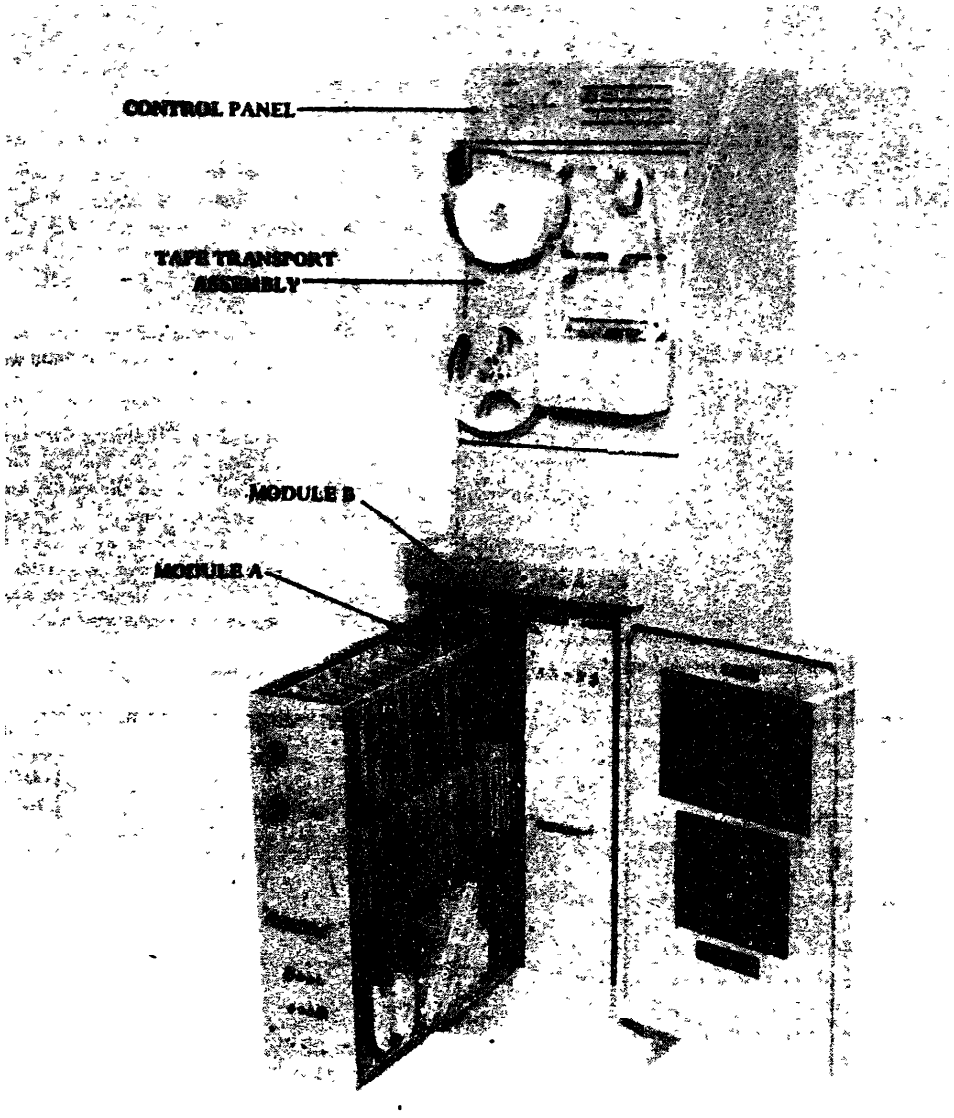


Figure 1- Master High Speed Tape Sender

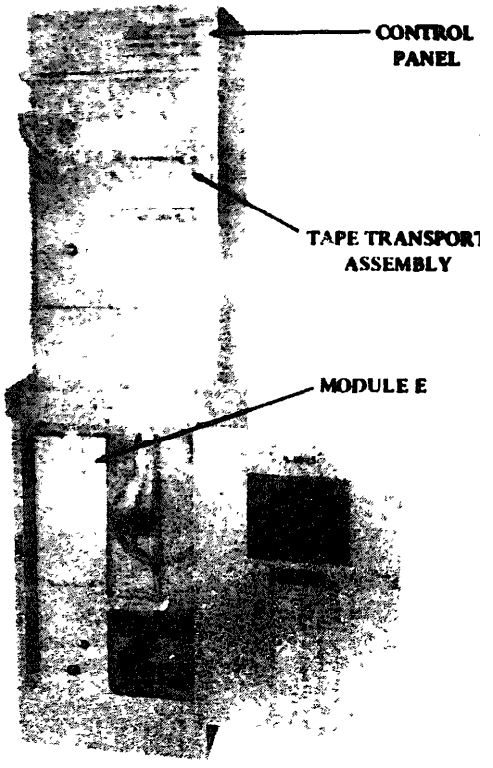


Figure 2- Supplementary High Speed Tape Sender

tolerance is between 5 percent and 95 percent. The master cabinet weighs 270 pounds and the supplementary cabinet weighs 190 pounds. These weights include all appropriate assemblies and modules.

2.04 Outside dimensions for master and supplementary cabinets are as follows:

(a) Base, 16 inches wide, 18 inches deep.

(b) Cabinet, 16 inches wide, 23 inches deep, and 60 inches high.

(c) Cabinet, with front doors open and modules fully extended, front to rear is 42 inches.

2.05 Service and maintenance clearances, front and back, are necessary for maintenance personnel accessibility. The tape transport shelf extends seven inches out beyond the front lower portion of the cabinet. The electronic module extends 19 inches beyond the lower front portion of the cabinet, no clearance is required for sides and top of cabinet. There are no provisions for side to side mounting installations. Floor mounting information can be found in Figure 3.

2.06 Overhead conduit accessibility can be made through a suitable hole cut in the top or rear of the control panel cover. This will permit access to the receptacles and connections through the cable opening in the cabinet top (Figure 4).

Note The equipment is packed for maximum protection. Exercise care when unpacking and handling units to prevent damage. Observe all caution labels and instructions.

3. INSTALLATION

CABINETS

3.01 The modules and tape transport assemblies are fastened during shipment with special shipping bolts and brackets. Use the following procedure when removing the shipping bolts and brackets (Figure 6).

(a) Loosen the screw at the top center of the cabinet back panel. Tilt the back panel outward and lift it out of the bottom channel.

(b) Remove the shipping bolts and brackets (approximately at center of cabinet back) holding the tape transport assembly to the cabinet frame. Slide tape transport assembly forward, and remove shipping blocks under the tape reader vibration mounts.

Note: Check all cable routing, tying, and clamping with the tape transport and electronic modules in their extended and closed positions. The cables should not bind or restrict the movement of mechanisms or slide-out assemblies.

(c) Remove the shipping screws in back of each module (one at the top, and one at the bottom). There are two electronic modules in the master cabinet and one in the supplementary cabinet (Figure 5 and Figure 7).

(d) The module is now held in place by its regular latching device, located at the top center of the front module panel. Rotate the module latch to its horizontal position by turning the locking screw counterclockwise a quarter of a turn. This disengages the module latch from the tab on the module guide (Figure 8 and Figure 9).

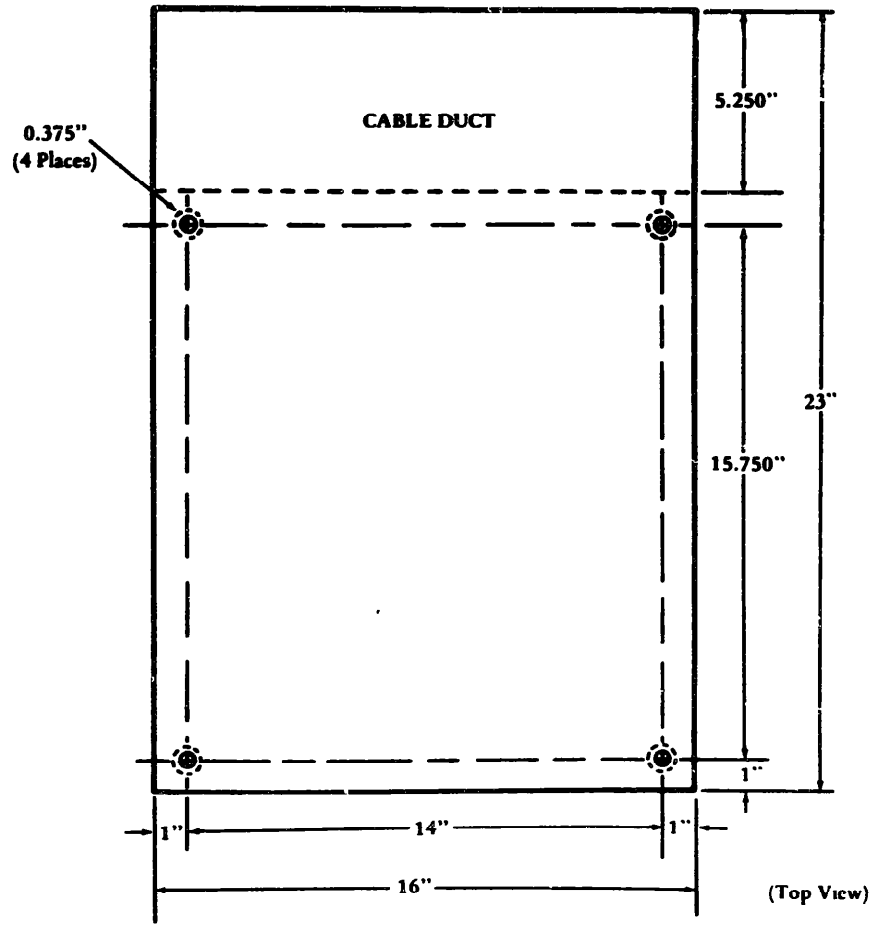


Figure 3- Cabinet Mounting Hole Locations

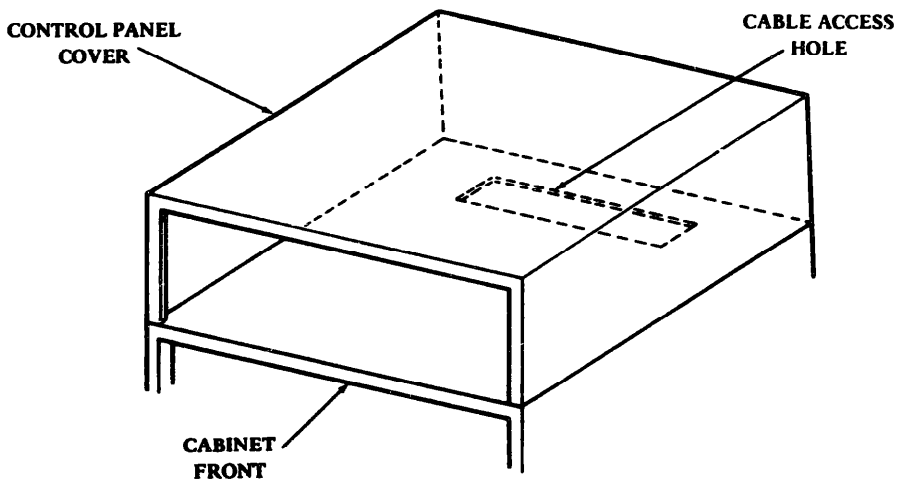


Figure 4- Cable Access Hole

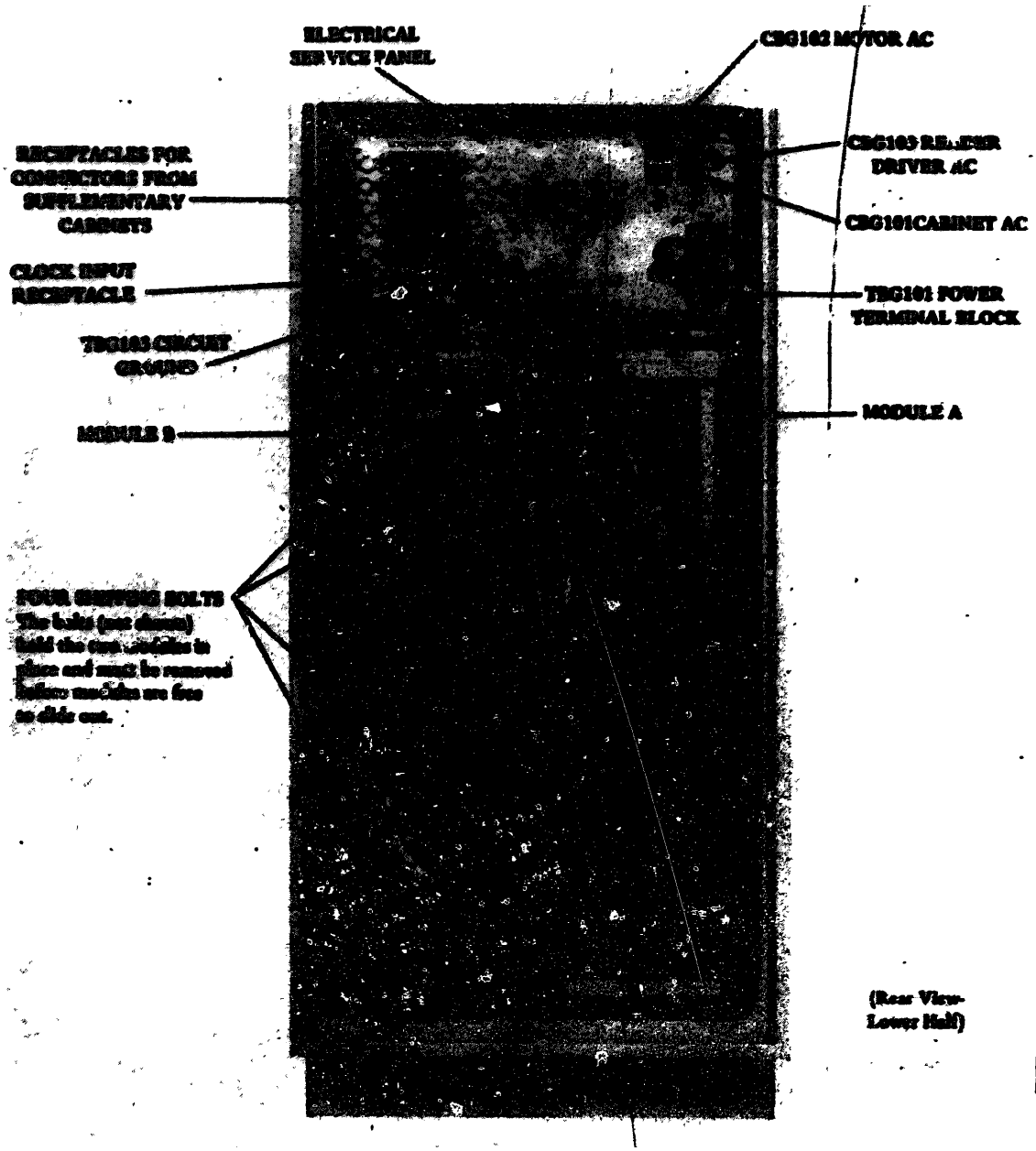


Figure 5- Master High Speed Tape Sender

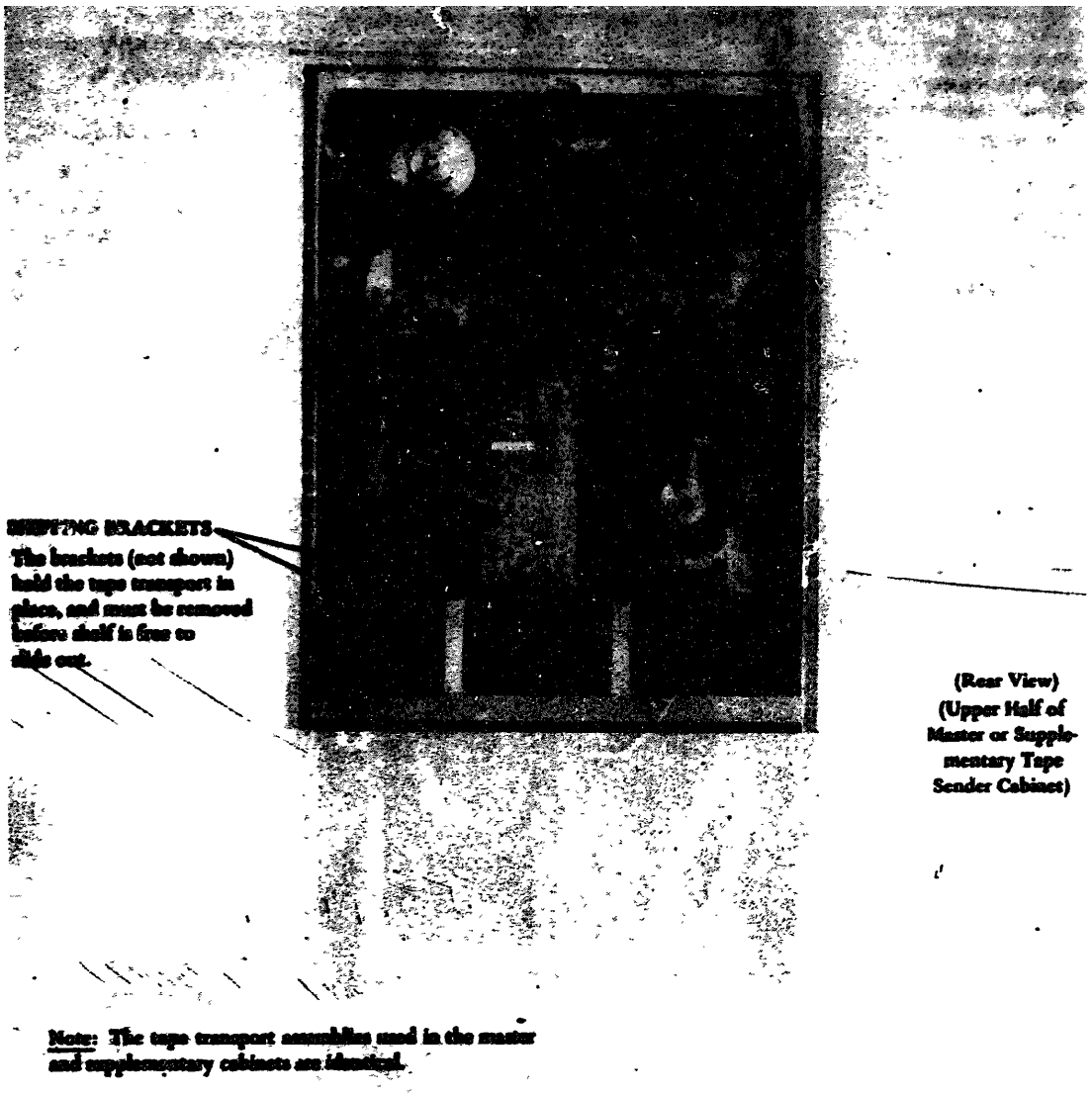


Figure 6- Tape Transport Assembly

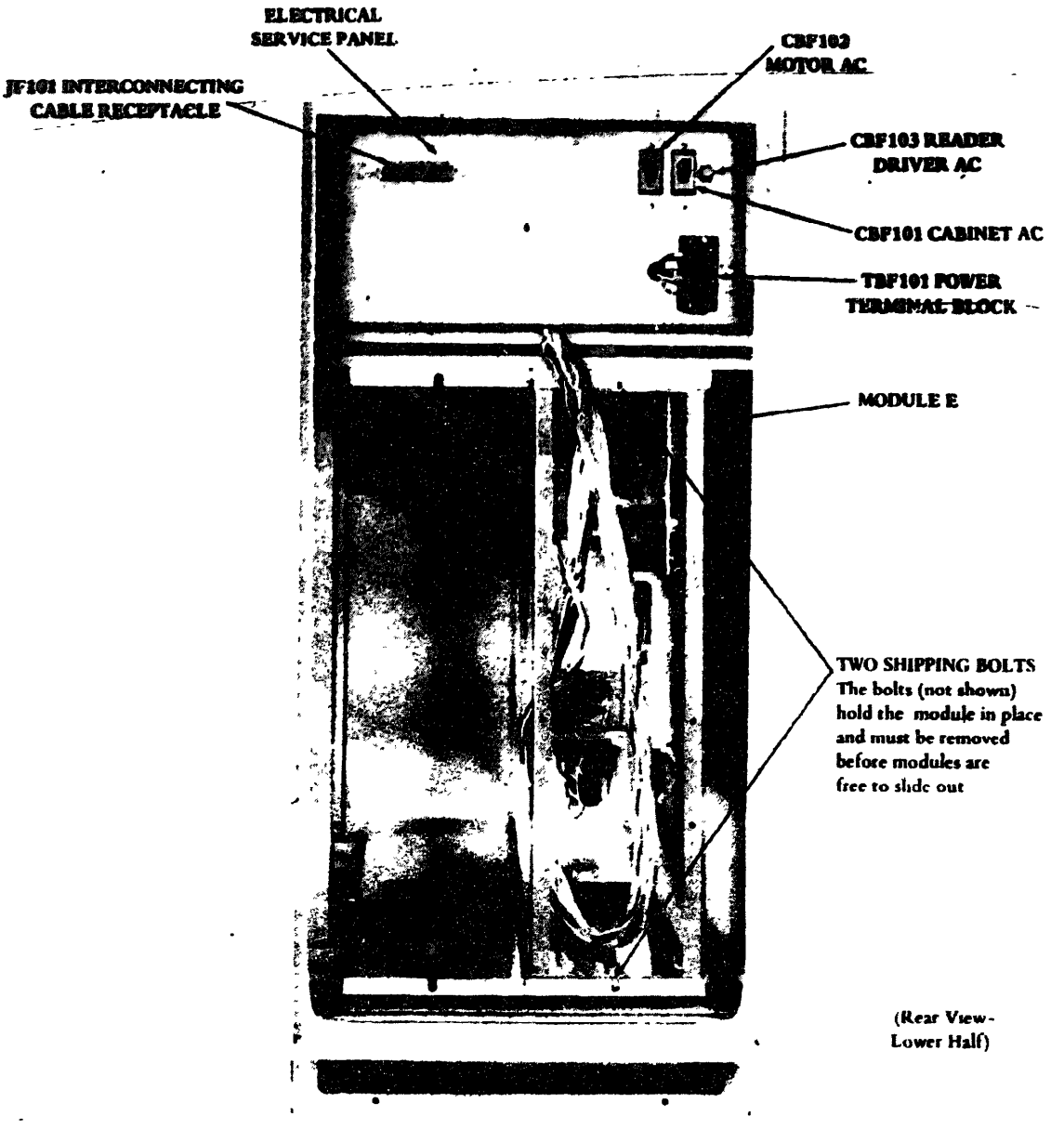


Figure 7- Supplementary High Speed Tape Sender

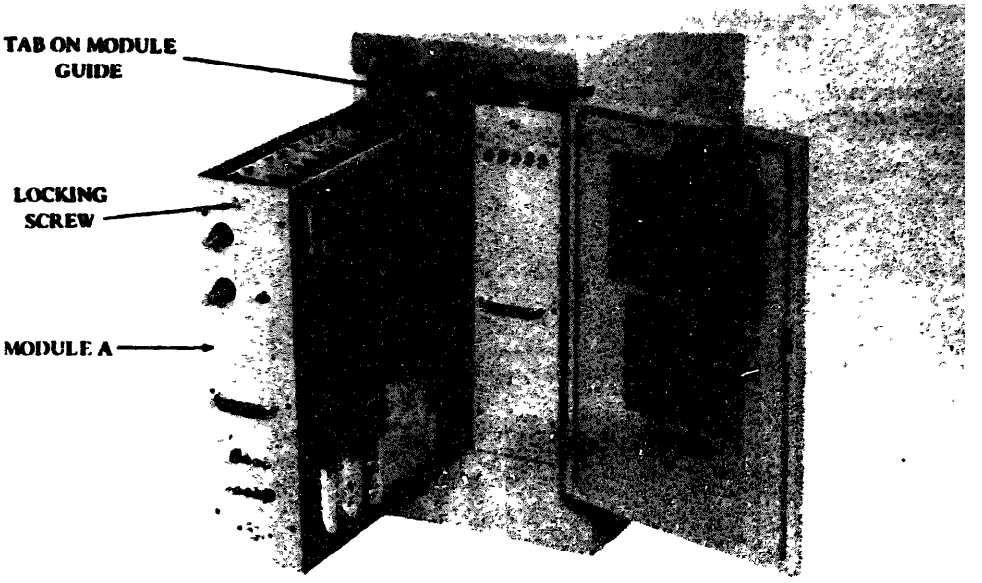


Figure 8- Module Removal

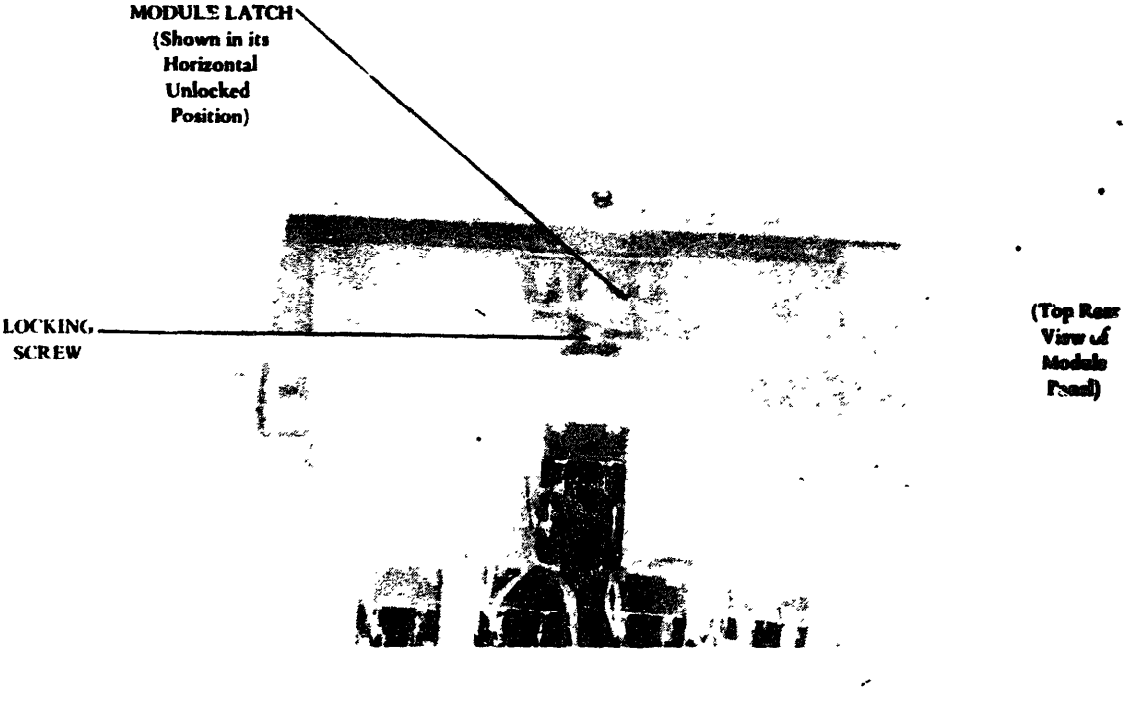


Figure 9- Module Hatch Detail

(e) Slide the module out to its fully extended position (the module is stopped from coming completely out of the cabinet by the tab at the front of the module guide). Examine all circuit cards for damage and proper seating in their receptacles. Check other components and exposed wiring for damage.

(f) To remove a module and set it out in front of the cabinet on the floor, pull the module out to its fully extended position. Tilt the front of the module upward while moving the bottom outward and lower slightly, until the rear of the module frame is clear of the tab on the upper module guide.

(g) The cables connected to the rear of the modules should have sufficient length to accomplish the procedure above (f), without disconnecting or carrying any of the cables to bind or strain. Reverse the procedure ((f) through (d)) to replace the module in the cabinet.

CABLE ROUTING

3.02 The interconnecting power and input cables may be routed from the top of the cabinet down along both sides to the electrical service panel located to the rear and center of the cabinet (Figure 4).

3.03 Route interconnecting cables from the supplementary cabinets to any one of the receptacles (JG101 through JG105) located on the master cabinet electrical service panel. Circuit ground connections are made at TBG103 (Figure 5).

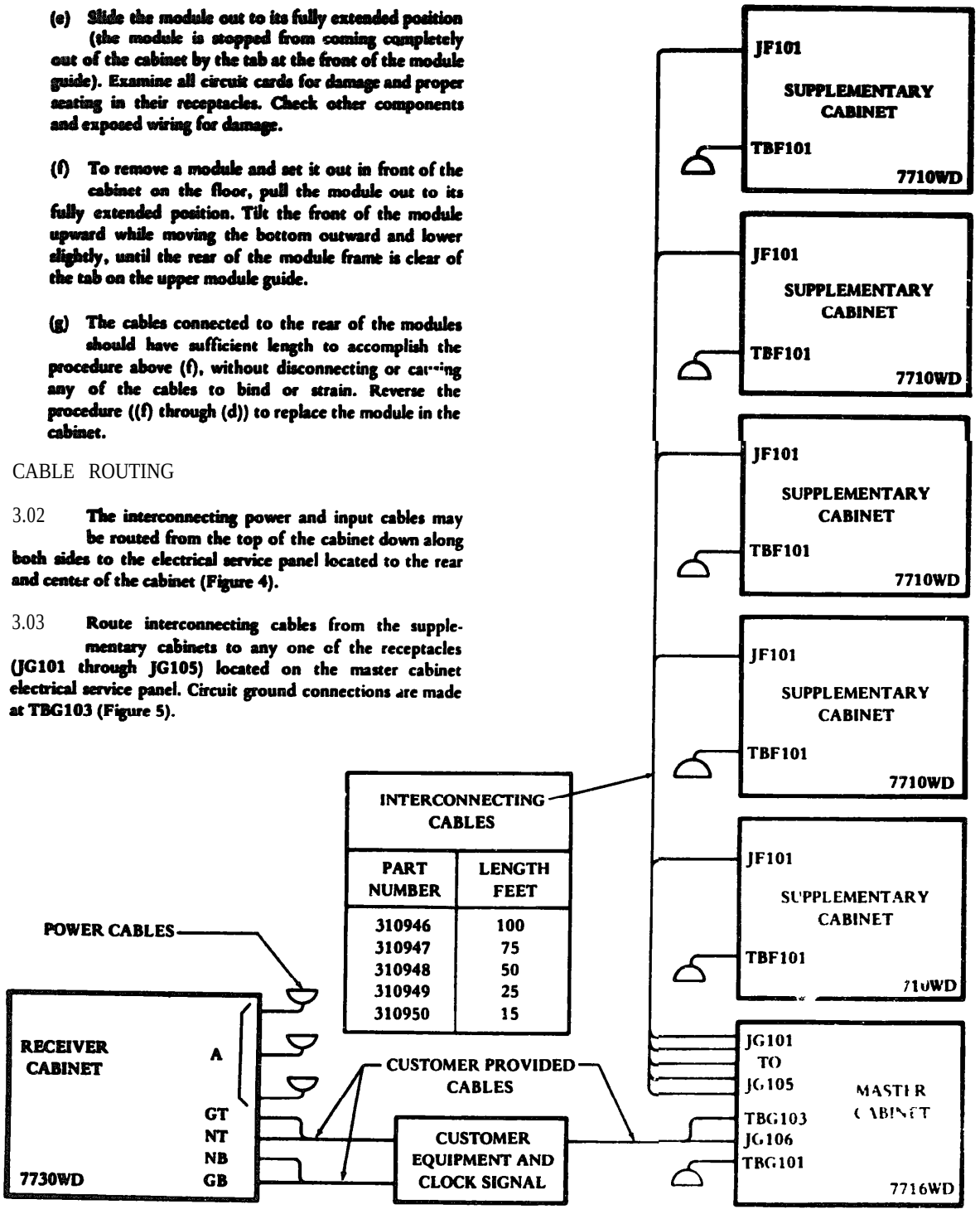


Figure 10- Interconnecting Cabling Diagram

3.04 **Up to five different interconnecting cables may be connected to the master cabinet. There are five different transmitter interconnecting cable lengths available (selection should be based on physical layout of cabinets). Cable lengths may be determined from the information found in Figure 10.**

3.05 **Typical tape sender system arrangement (Figure 10) with power, signal cable starting, termination points and wiring diagram references.**

3.06 **Wiring connections with starting and termination reference points can be found in Table B Supplementary Transmitter Connections, and Table C Master Transmitter Connections. The location code refers to schematic wiring diagram sheet number, horizontal, and vertical coordinates respectively.**

TABLE B

SUPPLEMENTARY TRANSMITTER CONNECTIONS

DESIGNATION	CONNECTOR JF101	LOCATION 7710WD
Feed Alarm	1	5-D-2
Verifier Alarm	2	5-F-2
Reader Alarm	3	5-A-8
Reader Stop	4	4-B-5
Step-Read	5	4-E-7
Reader Step	6	4-C-7
On Line	7	2-D-2
Bid	8	2-C-8
End of Sequence	9	3-C-8
Delete Number	10	3-C-8
Code Reading Contact – Bit 1	11	7-B-3
Code Reading Contact – Bit 2	12	7-B-3
Code Reading Contact – Bit 3	13	7-C-3
Code Reading Contact – Bit 4	14	7-C-3
Code Reading Contact – Bit 5	15	7-D-3
Code Reading Contact – Bit 6	16	7-E-3
Code Reading Contact – Bit 7	17	7-E-3
Code Reading Contact – Bit 8	18	7-F-3
Abnormal Traffic	20	3-E-2
-6 Volts	21	6-C-7
+6 Volts	23	6-C-7
Verifier Alarm Inhibit	26	4-B-7
Frame Ground	27	6-B-7
Feed Contact	28	7-F-6
Verifier Contact – Bit 1	29	7-B-6
Verifier Contact – Bit 2	30	7-B-6
Verifier Contact – Bit 3	31	7-C-6
Verifier Contact – Bit 4	32	7-C-6
Verifier Contact – Bit 5	33	7-D-6
Verifier Contact – Bit 6	34	7-D-6
Verifier Contact – Bit 7	35	7-E-6

TABLE B

SUPPLEMENTARY TRANSMITTER CONNECTIONS
(Continued)

DESIGNATION	CONNECTOR JF101	LOCATION 7710WD
Verifier Contact – Bit 8	36	7-F-6
Circuit Common	37	6-C-7
Lamp Common	40	6-B-7
Step-Read Reset	46	4-D-7
12 Volts	47	6-B-7

DESIGNATION	TBF101 TERMINAL	LOCATION 7710WD
Frame Ground	1	6-B-3
Common ac	3	6-B-3
Power ac	4	6-A-3

TABLE C

MASTER TRANSMITTER CONNECTIONS

DESIGNATION	CONNECTOR JG106	LOCATION 7716WD
Parallel Data Out – Bit 1	1	11-F-5
Parallel Data Out – Bit 2	3	11-F-2
Parallel Data Out – Bit 3	5	11-F-3
Parallel Data Out – Bit 4	7	11-F-3
Parallel Data Out – Bit 5	9	11-F-4
Parallel Data Out – Bit 6	11	11-F-4
Parallel Data Out – Bit 7	13	11-F-5
Parallel Data Out – Bit 8	15	11-F-6
Character Available	17	11-F-8
Frame Ground	19	11-F-7
Clock Input	20	8-B-1
Serial Data Out	22	9-F-6
Abnormal Traffic	26	26-C-2
External +6 Volts	28	26-E-2
External -6 Volts	30	26-E-3
Alarm Contact (Normally Open)	32	19-F-2
Alarm Contact (Common)	34	19-F-2
Alarm Contact (Normally Closed)	36	19-F-2

TABLE C

MASTER TRANSMITTER CONNECTIONS
(Continued)

DESIGNATION	TBG103 TERMINAL	LOCATION 7716WD
Circuit Common	1	11-F-1
DESIGNATION	**CONNECTORS JG101 THROUGH JG105**	**LOCATION 7716WD**
Feed Alarm	1	20-E-8
Verifier Alarm	2	19-C-8
Reader Alarm	3	19-E-2
Reader Stop	4	18-A-5
Step-Read	5	18-C-2
Reader Step	6	15-C-8
On Line	7	14-B-6
Bid	8	13-C-2
End of Sequence	9	22-E-5
Delete Number	10	15-F-2
Code Reading Contact – Bit 1	11	16-A-2
Code Reading Contact – Bit 2	12	16-B-2
Code Reading Contact – Bit 3	13	16-E-2
Code Reading Contact – Bit 4	14	16-F-2
Code Reading Contact – Bit 5	15	17-A-2
Code Reading Contact – Bit 6	16	17-C-2
Code Reading Contact – Bit 7	17	17-E-2
Code Reading Contact – Bit 8	18	17-F-2
Abnormal Traffic	20	26-E-6
-6 Volts	21	7-C-8
+6 Volts	23	7-C-8
Verifier Alarm Inhibit	26	18-F-8
Frame Ground	27	7-B-8
Feed Contact	28	20-D-2
Verifier Contact – Bit 1	29	16-B-2
Verifier Contact – Bit 2	30	16-C-2
Verifier Contact – Bit 3	31	16-E-2
Verifier Contact – Bit 4	32	16-F-2
Verifier Contact – Bit 5	33	17-B-2
Verifier Contact – Bit 6	34	17-C-2
Verifier Contact – Bit 7	35	17-E-2
Verifier Contact – Bit 8	36	17-F-2
Circuit Common	37	7-B-8
Lamp Common	40	7-B-8
Step-Read Reset	46	18-A 7
-12 Volts	47	7-C-8

TABLE C

MASTER TRANSMITTER CONNECTIONS
(Continued)

DESIGNATION	TBG101 TERMINAL	LOCATION 7716WD
Frame Ground	1	7-B-3
Common ac	3	7-B-3
Power ac	4	7-B-3

INITIATING OPERATION

3.07 A preliminary power check should be made on the master tape sender as follows.

(a) Operate circuit breakers CBG101, CBG102, and CBG103 (upper position for toggle type, push in for button type) located at the left side of the electrical service panel (Figure 5)

(b) Operate the eight circuit breakers on the lower front panel of module A (Figure 11).

(c) Press the POWER switch on the master control panel on top of the cabinet. The switch indicator will light when pressed and the switch transfers power to the modules and mechanisms in the cabinet. When the switch is pressed a second time, the switch indicator will go off and power is removed (Figure 13)

3.08 Make a preliminary power check on the supplementary tape sender as follows

(a) Operate circuit breakers CBF101, CBF102, and CBF103 (upper position for toggle type, push in for button type) located on the left side of the electrical service panel (Figure 7).

(b) Operate the four circuit breakers on the front panel of module E (Figure 12).

(c) Press the POWER switch on the control panel on top of the cabinet. (Same action occurs as described in paragraph 3.07(c), Figure 14)

4. CHECKOUT PROCEDURE

4.01 After installation of both master and supplementary high speed tape senders, the procedure should be checked out for proper operation of the sets (see Chart). The procedure is arranged in chart form with each step designed to be followed in sequence. A visual verification corresponds to each test

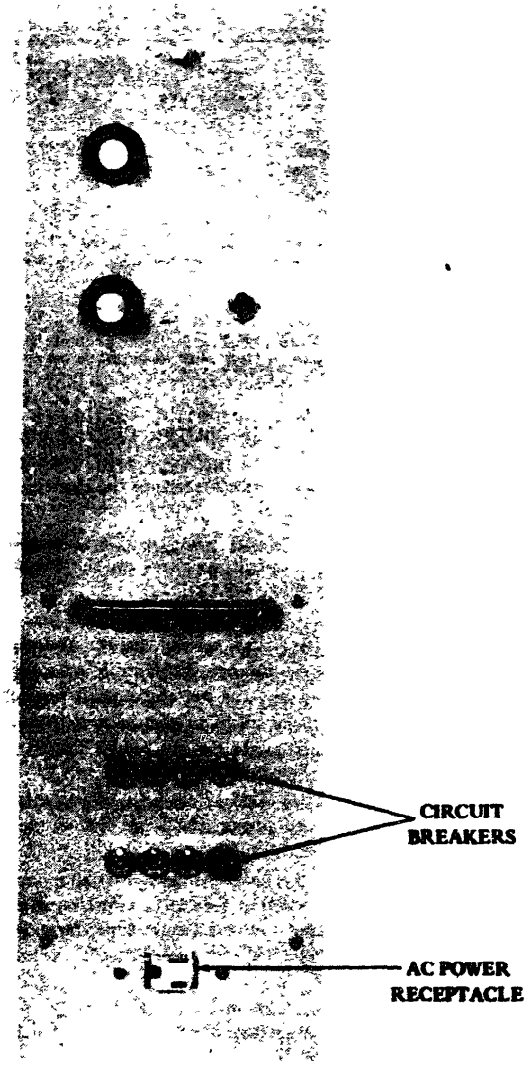


Figure 11- Module A Control Pane;

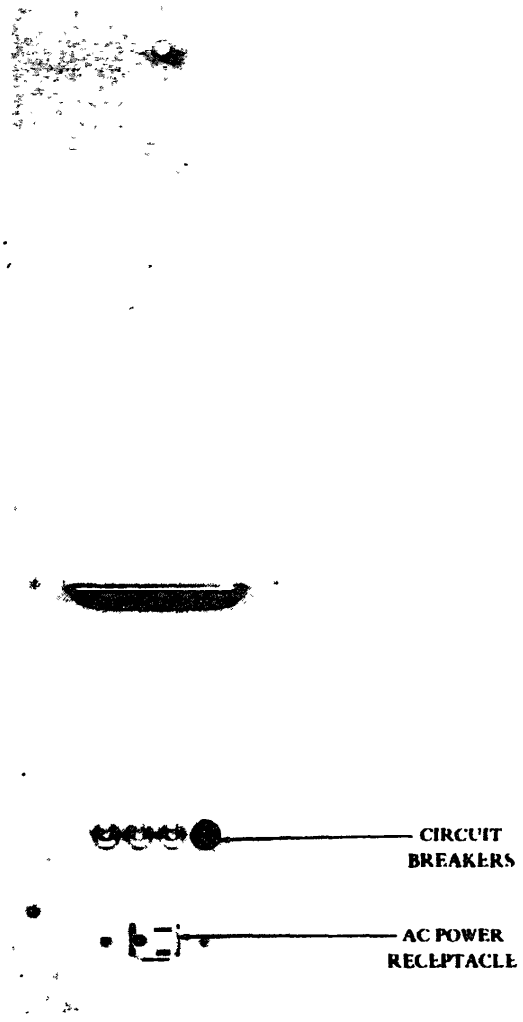


Figure 12- Module E **Control** Panel

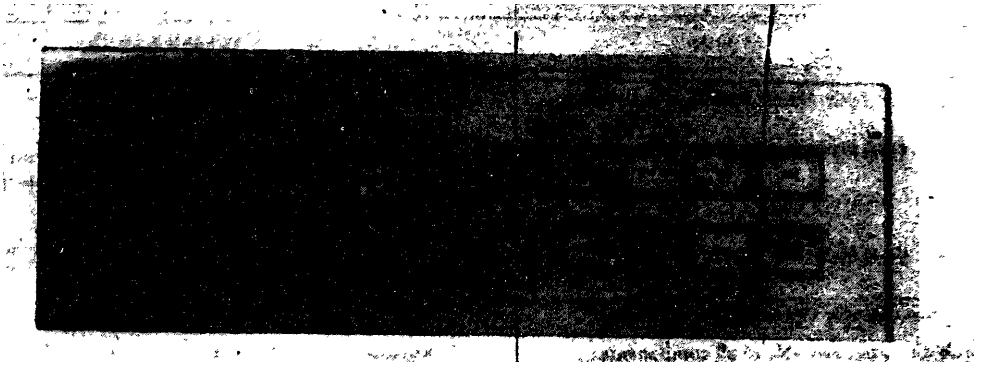


Figure 13- [redacted]

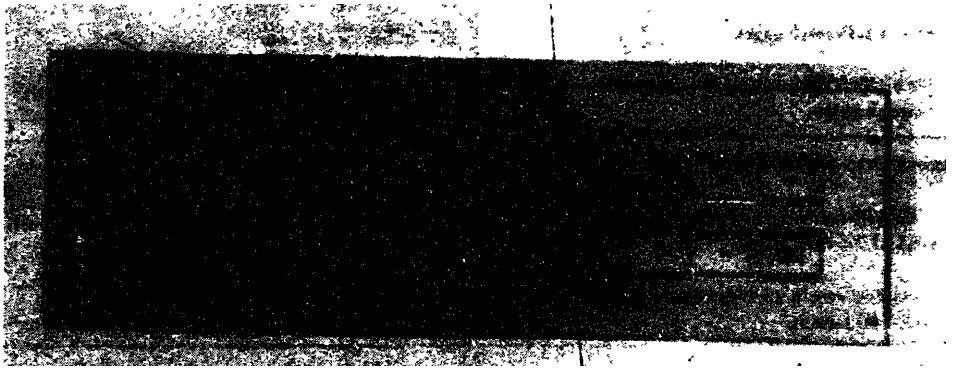


Figure 14- [redacted]

CHART

CHECKOUT PROCEDURE CHART FOR MASTER AND SUPPLEMENTARY SENDER CABINETS

STEP	ACTION	VERIFICATION
1	Power Switch, Master Sender	
	(a) Press POWER switch.	POWER indicator lights. Power is available for motors, modules, and electrical receptacle (JA1) on the front panel of module A.
	(b) Press MOTORS switch.	MOTORS indicator lights. Reader and tape winder motors operate.
2	Power Supply Operation, Master Sender	
	With power available to all components.	Correct voltages should be present, refer to adjustment Section 592-851-730TC for voltage test points.
3	Bid Request, Master Sender	
	(a) With no tape in reader, press BID switch.	BID indicator does not light.
	(b) With tape in reader, press BID switch.	BID indicator lights.
	(c) Remove tape from reader.	BID indicator goes out.
	(d) Repeat step (b).	BID indicator lights.
	(e) Press BID switch again.	BID indicator goes out.
	(f) With MOTORS switch off, press BID switch twice	MOTORS indicator and motors go on and off with BID switch and indicator.
4	Number Delete, Master Sender	
	(a) With BID indicator off, press NUMBER DELETE switch twice.	NUMBER DELETE indicator goes on and then off.
	(b) Press BID switch and then NUMBER DELETE switch.	With BID switch on and indicator lit, NUMBER DELETE switch has no effect.
5	STEP Switch, Master Sender	
	With tape in the reader, press STEP switch and release.	Tape will advance one character position. Character on tape will not be read.
6	Transmitter Operation, Master Sender	
	The following test requires that the set be connected to an external clock pulse source.	
	(a) With tape in the reader, press the BID switch.	ON LINE indicator lights, tape reader starts, and message number generator advances.
	(b) Press STOP switch.	STOP switch indicator goes on and reader stops.
	(c) Press STEP switch.	Reader advances one character.

CHART

CHECKOUT PROCEDURE CHART FOR MASTER AND SUPPLEMENTARY SENDER CABINETS
(Continued)

STEP	ACTION	VERIFICATION
	(d) Press STEP-READ switch.	Reader advances one character and transmits.
	(e) Press STOP switch.	STOP switch indicator goes out and reader starts.
	(f) Allow end of tape to pass through reader.	Reader stops.
7	Alarms, Master Sender	
	(a) With tape reader stepping, hold back on tape so tape does not feed.	TAPE FEED indicator lights, and alarm transfer contact output operates.
	(b) Release tape until normal feeding is resumed. Press TAPE FEED switch.	TAPE FEED indicator goes out. Alarm contact output returns to normal.
	(c) Block reader contacts with a piece of paper without blocking verifier contacts. Start reader with BID switch.	VERIFIER indicator lights.
	(d) Remove piece of paper. Press VERIFIER switch.	VERIFIER indicator light goes out.
8	Supplementary Transmitters	
	(a) Connect one or more supplementary transmitters to the master sender. With the master sender power on, perform the preceding tests on the supplementary transmitters.	All test requirements should be made
	(b) Load torn tapes into two or more transmitters (including master sender). Press BID switches on all senders.	The readers operate in turn, each reader starting as the preceding reader reaches the end of its tape
9	Transmission Quality	
	(a) Make this test with the Master Sender. Connect with a tape receiver or other means of monitoring a serial output. Transmit in synchronous and start-stop operation with all combinations of units per character interval, and code levels.	Signals should be received correctly Receiver should synchronize properly when receiving all transmitting modes. Proper data should be received from the start of message (SOM) generator, including the eighth character selected by the SOM CHARACTER toggle switches Check parallel outputs (Figure 15).
	(b) Make test transmissions in 8 level code from each supplementary transmitter connected to each supplementary input in turn	Check each supplementary input in sequence Signals should be received correctly

CHART

CHECKOUT PROCEDURE FOR MASTER SUPPLEMENTARY SENDER CABINETS
(Continued)

STEP	ACTION	VERIFICATION
10	Abnormal Traffic Indicator (a) Apply -6 volts to the abnormal traffic input lead (JA128-C4). (b) Apply +6 volts to the abnormal traffic input lead (JA128-C4).	 ABNORMAL TRAFFIC indicators light on master and all supplementary senders. All ABNORMAL TRAFFIC indicators go out.

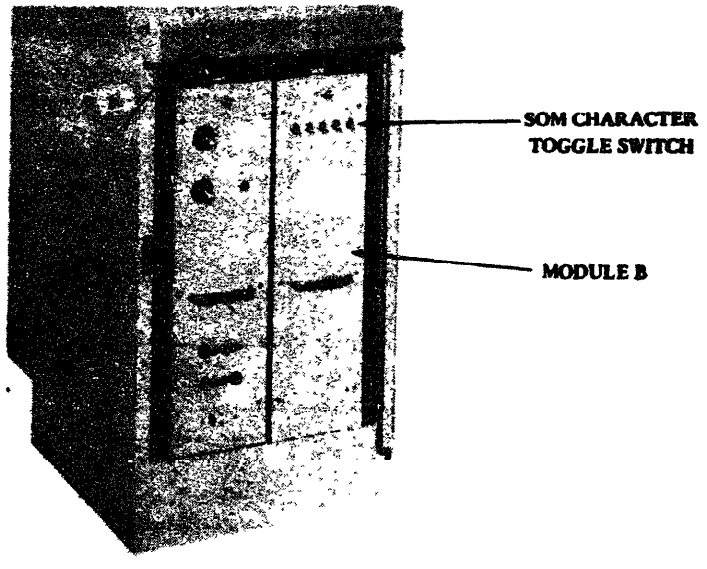


Figure 15- SOM CHARACTER Switches

TELETYPE CORPORATION
Skokie, Illinois, U.S.A.

MASTER AND SUPPLEMENTARY HIGH SPEED TAPE SENDERS

FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

TROUBLESHOOTING

CONTENTS PAGE

1. GENERAL

1.01 **This section provides troubleshooting procedures for the master and supplementary high speed tape senders, used in the Multiple Address Processing System. It is reissued to include the latest engineering information, change** the title, remove the preliminary designation, and change, and this section to the standard format. Since this is a general revision, marginal arrows that indicate changes and additions ate omitted.

1.02 The troubleshooting tables in this section are designed to be used as an aid in locating trouble within the equipment. Testing and replacing components should be performed by persons familiar with transistor circuits.

Note: After performing maintenance of trouble-shooting duties, make certain all screws and electrical connections are secure.

1.03 The following test equipment and took are recommended to be used in troubleshooting:

(a) Tektronix 516 series oscilloscope or equivalent.

(b) Multimeter (volt&n-ma) 20,000 ohms/volts.

(c) Adjusting tool information for the high speed reader can be found in Section 592-804-700TC.

2. TROUBLESHOOTING

2.01 If the tape sender fails to operate, the trouble should be analyzed to recognize the source of the problem Pinpoint the exact area or cause of trouble rather than giving a general description. For example, it would be more informative to say, '"The CR3 diode does not energize day K1 when the MOTORS switch is operated." instead of The MOTORS switch does not operate."

2.02 Readjustments should not be made to correct trouble that is not fully understood. This can result in inserting more trouble into a malfunctioning mechanism or circuit.

2.03 When trouble indicates that a circuit card or cards should be replaced. the procedure to follow, if possible, would be to replace all the indicated cards. Then one by one replace the new cards with the old cards, until the malfunction reappears. The faulty card should be replaced with a new card and the remaining old cards plugged back into the equipment.

Note: If at anytime a power circuit breaker trips or the power is turned off on the cabinet during troubleshooting, the sequence must be started over again with operating the POWER switch.

2.04 The information in the troubleshooting tables is based on the fact that input data to the equipment is not faulty. A table is not included for the alarm circuits due to the simplicity of their operation

TABLE A

MASTER CABINET POWER FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate POWER switch. POWER indicator lights	POWER indicator does not light.	Check for defective -12 volt ac circuit breakers in module A. Refer to 7716WD, Sheet 7.
		Check POWER indicator lamp.
Turn power off and reset circuit breakers		Check ac switch SWG102. Refer to 7716WD, Sheet 4.
		Check ac circuit breaker CBG101.
		Check input power source.
Restore power to cabinet		Check ac outlet and circuit breaker on module A. Refer to 7716WD, Sheet 7.
		Check -12 volts at control panel. Refer to 7716WD, Sheet 6.
		Check connectors, wiring and power supply.
		Check POWER switch and wiring.
		Check +6, -6, -48, -28 volts at the power supply in module A. Refer to 7716WD, Sheet 6.
Operate MOTORS switch. MOTORS indicator lights	MOTORS indicator lamp does not light.	Check indicator lamp. Refer to 7716WD, Sheet 2. Check MOTORS switch and wiring.
		Check reader and winder motors.
		Check ac circuit breaker CBG102. Refer to 7716WD, Sheet 7.
		Check ac switch SWG101.
		Check connectors, wiring, and motors.

TABLE B

SUPPLEMENTARY CABINET POWER FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate POWER switch. POWER indicator lights.	POWER indicator does not light.	Check POWER indicator lamp.
		Check POWER switch and wiring. . . 7710WD, Sheet 6.
Turn off power and reset circuit breakers.		Check -12 volt ac circuit breakers in module E.
		Check ac circuit breaker CBF101.
		Check ac switch SWF102. Check input power source.
Restore power to cabinet.		Check ac outlet and circuit breaker on module E.
		Check -12 volts at JF101-19 on electrical service panel.
		Inspect connections and -12 volt output from master cabinet.
		Check -12 volts at control panel. Refer to 7710WD, Sheet 6. Check relay KF101.
		Check -6 volts at ZA314-A20 and +6 volts at ZA314-A18. Check -6 volt and +6 volt circuit breakers on module panel.
		Check -6 volts and +6 volts at JF101-21 and 23 respectively. Recheck relay KF101. Check voltage output from master cabinet.
Operate MOTORS switch. MOTORS indicator should light.	MOTORS indicator is not lit.	Check indicator lamp and operate switch again. Refer to 7710WD, Sheet 2.
		Check MOTORS switch, wiring and connections, 7710WD, Sheet 6.

TABLE B

SUPPLEMENTARY POWER FAILURE (Continued)

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
		Check reader and winder motors.
		Check ac circuit breaker CBF102.
		Check ac switch SWF101.
		Check connectors, wiring, and motors.

TABLE C

MASTER CABINET READER STEP FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate POWER switch. POWER indicator lights.	Reader steps.	Check ZA401. Refer to 7716WD, Sheet 2.
Operate STOP switch. STOP indicator lights.	Indicator does not light.	Check lamp, connections, and wiring.
	Reader steps.	Check ZA116, ZA103, ZB321, ZB324, and ZA110. If reader still steps, check manual step and read from the supplementary transmitter, or the supplementary reader step failure. Refer to 7716WD, Sheets 2, 3, and 4.
	Reader steps.	Check ZB522, ZB322, ZB317, and ZA114. Check associated wiring, connectors and voltages on the reader, and reader driver. Refer to 7716WD, Sheets 2, 3, 12, 13, and 18.
Operate STOP switch. Reader should not step.	STOP lamp does not light.	Check STOP lamp, -12 volts, and associated wiring.
Reader does not step after STOP switch is operated.	BID and ON LINE lamps light.	Release BID indication by removing tape from the reader. This turns off ON LINE indication through bid sequence failure.

TABLE C

MASTER CABINET READER STEP FAILURE (Continued)

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate STOP switch to the off position.	Reader steps.	Check ZB524 and ZB526. Check associated wiring, connectors, voltages, reader driver, and reader. Refer to 7716WD, Sheet 15.
If reader does not step after operating STOP switch, operate STEP switch.	STEP indicator lights. Reader does not step.	Check ZA116, ZA103, ZB524, and ZB526. Check associated wiring connectors, voltages, reader driver, and reader. Refer to 7716WD, Sheets 2, 3, and 15.
Operate STEP switch. Reader steps. Operate STOP and NUMBER DELETE switches. The indicators are lit. Secure ON LINE condition by initiating BID sequence.	BID sequence fails. BID and ON LINE indicators will not light. Reader does not step with ON LINE condition.	Check delete mode output of reader logic. Refer to 7716WD, Sheets 2, 3, 4, 12, 13, 15, and 18.
Start with STOP switch sequence again. Operate STEP READ switch.	Reader does not step.	Check cards ZB524, ZB526, ZA116, ZA110, ZB321, ZB324, ZB322, ZB522, ZB319, ZA114, and ZB317. Check for failure in SOM sequence.
Start with STOP and NUMBER DELETE switch sequence again. Reader steps when STEP READ switch is operated. Operate STOP switch to the off position, indicator goes out.	Reader does not step.	Check ZA116, ZA103, ZB321, and ZB324. Check associated wiring, connectors, and voltages. Refer to 7716WD, Sheets 2, 3, and 4.
Reader steps. Failure is not in step-read circuitry.	Tape readout is wrong	Check for errors in transmission.

TABLE D

SUPPLEMENTARY CABINET READER STEP FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate POWER switch. The POWER indicator lights.	Reader steps.	Check ZE202. and relays K1 and K2 on ZE426. Refer to 7710WD, Sheets 2 and 4.
Operate STOP switch to the on position. The STOP indicator should light.	Indicator does not light, check lamp.	Check wiring and connections. Refer to 7710WD. Sheet 4.
	Reader steps.	Check ZE116. ZE103. ZE110, and relay K1 on ZE426. Check associated voltages. connectors, wiring connections, reader driver, reader and interconnecting cable to the master cabinet. Refer to 7710WD. Sheet 4.
With STOP switch on and reader not stepping, BID and ON LINE indicator lamps should be off.	Indicator lamps are on.	Release BID indication by removing tape from reader. This turns off the ON LINE indication through bid sequence failure.
Operate STOP switch to the off position. STOP indicator goes off.	Reader steps.	Check ZB524 and ZB526 in master cabinet. Check associated connectors, wiring connections, voltages, reader, and reader driver. Refer to 7716WD, Sheets 2 and 3.
Operate STEP switch, STEP indicator should light and reader steps.	Reader does not step.	Check ZE116 and ZE103. Check associated wiring connections, connectors, voltages, reader, and reader driver. Refer to 7710WD, Sheet 4.
Reader steps when STEP switch is operated. Operate STOP and NUMBER DELETE switches. Associated indicators light. Secure ON LINE condition by initiating BID sequence.	BID sequence fails. BID and ON LINE indicators will not light.	Check indicator lamps, and initiate STOP through STEP switch sequence.
Operate STEP READ switch	Reader does not step.	If reader does not step correctly, check delete mode output of reader logic. Refer to 7710WD, Sheet 4. Check cards ZE116, ZE110, ZE114, and relay K2 on ZE426. Check ZB324 and ZB321 in master cabinet. Refer to 7716WD, Sheet 4.

TABLE D

SUPPLEMENTARY CABINET READER STEP FAILURE (Continued)

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
	Reader still does not step.	Check for failure in SOM sequence.
Proceed with STOP and NUMBER DELETE switch sequence again. Reader steps when STEP READ switch is operated. Operate STOP switch to the off position. Indicator goes out.	Reader does not step.	Check ZE116 and ZE103. Check ZB321 and ZB324 in master cabinet. Refer to 7716WD, Sheet 4. Check associated wiring connections and voltages
If reader steps, failure is not in step-read circuitry.	Tape readout is inaccurate.	Check for errors in transmission.

TABLE E

TRANSMISSION OF GARBLED DATA

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Check indicators on SIGNAL MODE, UNITS PER CHARACTER INTERVAL switches and strapping on ZA316 (TB243).	Clock pulses are below standard.	Check clock pulses at ZA303-34 Check clock circuitry. Restore clock pulses and recheck failure Refer to 7716WD, Sheets 8, 9, and 10.
Compare clock pulses between ZA305-B30, and reader step pulses at ZA311-A27, with the setting on the UNITS PER CHARACTER INTERVAL switch.	Pulses are defective.	Check cards ZA307, ZA309, ZA311, and ZA303. Recheck failure Refer to 7716WD, Sheets 8 and 9.
If pulses are good, check all transmitters for garbled data.	Tape readout is inaccurate.	Check contacts on the failing readers at ZB120, ZB121, ZB122, ZB123, and ZB124. Refer to 7716WD, Sheets 16 and 17
Check all code levels for garbled data.	All levels are defective	Check cards ZA323, ZA307, and ZA305. Refer to 7716WD, Sheets 8 and 9

TABLE E

TRANSMISSION OF GARBLED DATA **(Continued)**

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
	Some code levels have garbled data.	**Check for trouble on cards ZA305, ZA313, ZA314, ZA317, ZA321, ZB102 through ZB108, and ZB120 through ZB124. Refer to 7716WD, Sheets 12, 16, 17, 18, 19, 20, and 23.**

TABLE F

MASTER AND SUPPLEMENTARY CABINETS VERIFIER ALARM

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Reset VERIFIER indicator alarm at the ON LINE transmitter.	**ON LINE transmitter constantly goes into VERIFIER alarm.**	**Reset alarm and check cards ZB322, ZB324, ZB512, ZB321, ZB108, ZB106, ZB110, ZB120, ZB116, and ZB118. Check reader contacts. Check through procedures in Table C and Table D. Refer to 7716WD, Sheets 4, 16, 17, and 20.**
	Alarm cannot be reset.	**Check master cabinet cards ZA110, ZA106, ZA205, and ZA116. Refer to 7716WD, Sheets 2, 4, and 5.**
	Alarm still cannot be reset.	**Check supplementary cabinet cards ZE110, ZE106, ZE205, and ZE116. Refer to 7710WD, Sheets 2, 4, and 5.**

TABLE G

MASTER AND SUPPLEMENTARY CABINET FEED ALARM

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Reset TAPE FEED alarm at ON LINE transmitter.	ON LINE transmitter constantly goes into TAPE FEED alarm.	Reset alarm and check cards ZB120, ZB110, ZB514, ZB522, and ZB305. - Check reader contacts, and check through procedures in Table C and Table D. Refer to 7716WD, Sheets 13, 17, 20, 22, and 23.
	Alarm cannot be reset.	Check master cabinet cards ZA110, ZA106, ZA205, and ZA116. Refer to 7716WD, Sheets 2, 4, and 5.
	Alarm still cannot be reset.	Check supplementary cabinet cards ZE110, ZE106, ZE205, and ZE116. Refer to 7710WD, Sheets 2, 4, and 5.

TABLE H

MASTER CABINET BID SEQUENCE FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate POWER switch, POWER indicator lights.	ON LINE indicator lights.	Check ZA401, bid logic module A. If ON LINE indicator is still lit, check cards ZA301, ZA103, ZA110, ZA114, ZA108, and relay K2 on ZA105. Refer to 7716WD, Sheet 2.
Insert tape in reader and operate BID switch.	BID indicator does not light.	Check BID lamp, associated wiring and connections. If lamp is not defective, check circuit cards listed above.
Check motors.	Motors are not running.	Check through Table A.
The motors are running and the ON LINE indicator is lit. Failure is not in the bid sequence.	The ON LINE indicator is not lit.	Check associated circuit cards ZA110, ZA114, ZA108, ZB520, ZB505, ZB522, and ZB524. Refer to 7716WD, Sheets 2, 13, and 24.

TABLE H

MASER CABINET AND SEQUENCE FAILURE (Continued)

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate BID switch. Check ZA114-A27 for bid signal one second after BID switch is operated. Check clear to send signal at ZA106-A9.	Signal is present.	Check through ZA106 and relay K2 on ZA205. Check associated wiring, connectors, voltages, and the ON LINE lamp. Refer to 7716WD, Sheets 2 and 5.
Check sequence step at ZB514-A9.	Signal is inaccurate.	Check ZB520, ZB505, ZB522, and ZB524.
	Sequence step is not good.	Check through ZB516, ZB518, ZB514, ZB512, ZB508, ZB510, ZA106, and relay K2 on ZA205. Refer to 7716WD, Sheets 2, 5, 13, and 14.
	Clear to send signal is inaccurate.	Check clock input at ZA302-34. If signal is still bad, restore clock signal. Refer to 7716WD, Sheet 8.
		Check clock signal at ZA302, ZA305, ZA307; ZA309, ZA311, ZA303, ZA314, ZA317, ZB517, and ZA313. Check associated wiring, connections and voltages. Refer to Sheets 8, 9, and 10.

TABLE I

SUPPLEMENTARY CABINET BID SEQUENCE FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Insert tape in reader. Operate POWER switch, POWER indicator should light. Operate BID switch, BID indicator should light.	The BID indicator does not light.	Check lamp and cards ZE102, ZE103 and relay K2 on ZE105, ZE108, ZE110, ZE114, and ZE202. Refer to 7710WD, Sheet 2.
Check reader and tape winder motors.	Motors are off.	Check through Table B.
Motors are on and ON LINE indicator is lit. Failure is not in bid sequence.	Indicator is not lit.	Check indicator lamp and ZE108, ZE110, and ZE114. Refer to 7710WD, Sheet 2.
Operate BID switch. Check at ZA114-A27 for bid signal one second after BID switch is operated.	Bid signal does not appear.	Operate BID switch again. Refer to 7716WD, Sheet 2.
Check for clear to send signal at ZA106-A9.	Signal is not present or signal is inaccurate.	Check interconnecting cables and connections to master cabinet. Check through Table H. Refer to 7716WD, Sheet 5.
Clear to send signal is present.	Check ZE106 and relay K2 on ZE205.	Check associated wiring, connectors, voltages and ON LINE lamp. Refer to 7716WD, Sheet 5.

TABLE J

MASTER CABINET START OF MESSAGE (SOM) FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Secure on line signal by initiating bid sequence with BID switch.	The ON LINE indicator lamp is not lit.	Check indicator lamp, and check through Table H.
The ON LINE indicator lamp is lit, and the SOM is transmitted.	SOM is not transmitted.	Check cards ZB305, ZB526, ZB307, ZB524, ZB313, ZA112, ZA103, and ZA114. Refer to 7716WD, Sheets 2, 3, 15, 17, 20, and 22.
After the 13 SOM character, the reader steps	Reader does not step.	Check cards ZA305, ZA114, ZB313, ZB524, ZA112, and ZA526. If reader does not step, check through Table C. Refer to 7716WD, Sheets 2, 3, 8, 13, 15, and 17.
The SOM is transmitted.	Tape does not transmit correctly.	Check for errors in transmission. Check through Table E.
Reader is transmitting correctly.	SOM is transmitted incorrectly.	Check cards ZB311, ZB309, ZB305, ZB313, ZB302, ZB315, ZB304, ZB503, ZB505, ZB307, ZB512, SB1 through SB5, and KB501-C. Check number display assembly, associated wiring, connections, and voltages. Refer to 7716WD, Sheets 14, 17, 19, 20, 22, 23, 24, and 25.
SOM is transmitted correctly. Release ON LINE indication by removing tape from the reader. Operate NUMBER DELETE switch, and start bid sequence over again.	SOM is transmitted and reader fails to step.	Check ZA112, ZA114, and ZA103. Check through Table C. Check associated wiring connections and voltages. Refer to 7716WD, Sheets 2 and 3.
If reader steps, failure is not in SOM circuit.		

TABLE K

SUPPLEMENTARY CABINET START OF MESSAGE (SOM) FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Secure on line signal and start bid sequence by operating BID switch.	The ON LINE indicator is not lit.	Check indicator lamp. Refer to Table I.
The ON LINE indicator lamp is lit and the SOM is transmitted.	SOM is not transmitted.	Check ZE112, ZE114, ZE118, and ZE103. Refer to 7710WD, Sheets 2 and 3.
	SOM is still not transmitted.	Operate STOP switch, (on position) and start bid sequence by operating BID switch. Measure voltage at ZE114-B34. Refer to Table J.
After the 13th SOM character the reader steps.	Reader does not step.	Check ZE118, ZE112, and ZE114. In the master cabinet check ZB524 and ZB526. If the reader does not step, check Table D. Refer to 7710WD, Sheets 2 and 3, and 7716WD, Sheets 13 and 15.
SOM is transmitted correctly. Release the ON LINE indication by removing tape from the reader. Operate NUMBER DELETE switch, and start bid sequence over again.	SOM is transmitted and reader fails to step.	Check ZE114, ZE112, and ZE103. Check through Table D. Check associated wiring, connections and voltages. Refer to 7710WD, Sheets 2 and 3.
If reader steps, failure is not in SOM circuit.		

MASTER AND SUPPLEMENTARY HIGH SPEED TAPE *SENDER* **FOR** THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS), ADJUSTMENTS, AND REMOVAL AND REPLACEMENT **OF** COMPONENTS

CONTENTS PAGE

1. GENERAL

1.01 This section covers adjustments, and removal and replacement of components. It is reissued to change the title, add minor engineering changes, remove the preliminary designation, and make this a standard publication. Lubrication information removed from this section can be found in Section 592-851-731TC. Since this is a general revision, marginal arrows that indicate changes have been omitted.

CIRCUIT CARD IDENTIFICATION

1.02 Circuit card and pin designation references made in the following electronic adjustments are explained below and referenced in **Figure** 1 showing the wiring side of a typical module.

1.03 The numbering and lettering system is the same on all modules. For example, assume a reference has been made to circuit card ZA102.

Z - signifies an electronic circuit card.

A - designates module A.

1 - corresponds to the horizontal row in which the circuit card is found in the module.- (The single numbers on the vertical side of the frame).

0 2 - corresponds to the specific position in that row (directly under the two-digit numbers across the top of the frame and duplicated on the lower part of the frame).

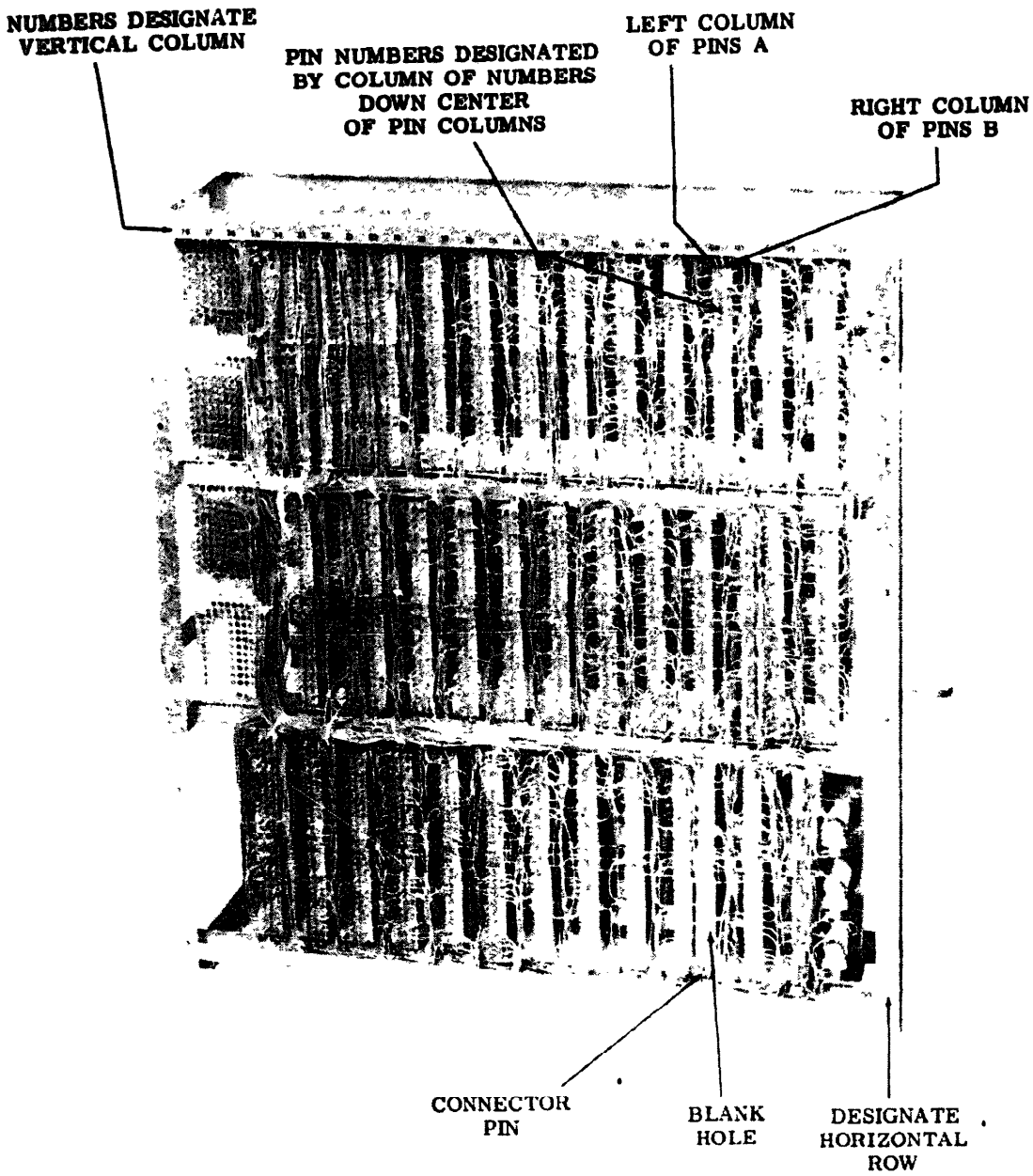


Figure 1- Wiring Side of Typical Module

1.04 Once the card is located, the pin numbers are easily identified. Pin numbers starting with A are in the left column of pins, and B in the right column (viewed from the wiring side of the circuit card connector). The numbers running down the center identify the pins. For example, pin B6 would be the sixth pin down on the right-hand column.

1.05 In some instances, pins are referred to only by number and not preceded by *A* or B. In these case, only one pin exists at each level (shown in lower portion of (Figure 1).

1.06 Each connector will accommodate two sizes of cards (large and small). The large card occupies the entire connector, with the odd numbers on the vertical frame designating the horizontal rows. Therefore, ZA102 would be in the first (top) row, ZA302 would be in the second (middle) row, and ZA502 would be in the third (bottom) row.

1.07 The small card occupies half the connector using all the numbers (1 through 6) on the vertical frame to designate the *row.*

1.08 The actual electronic adjustments are made on the card side of the modules, with the same numbering system described in 1.06.

1.09 Use the following equipment to make the necessary electrical, and electronic adjustments:

Voltmeter - ac-dc.

Oscilloscope - with dual trace inputs and dc amplifiers, such as Tektronix 516, 561, 540 series. or equivalent.

CAUTION: REMOVE ELECTRIC POWER FROM CABINET WHEN REMOVING OR REPLACING CIRCUIT CARDS, AND WHEN MAKING MECHANICAL ADJUSTMENTS.

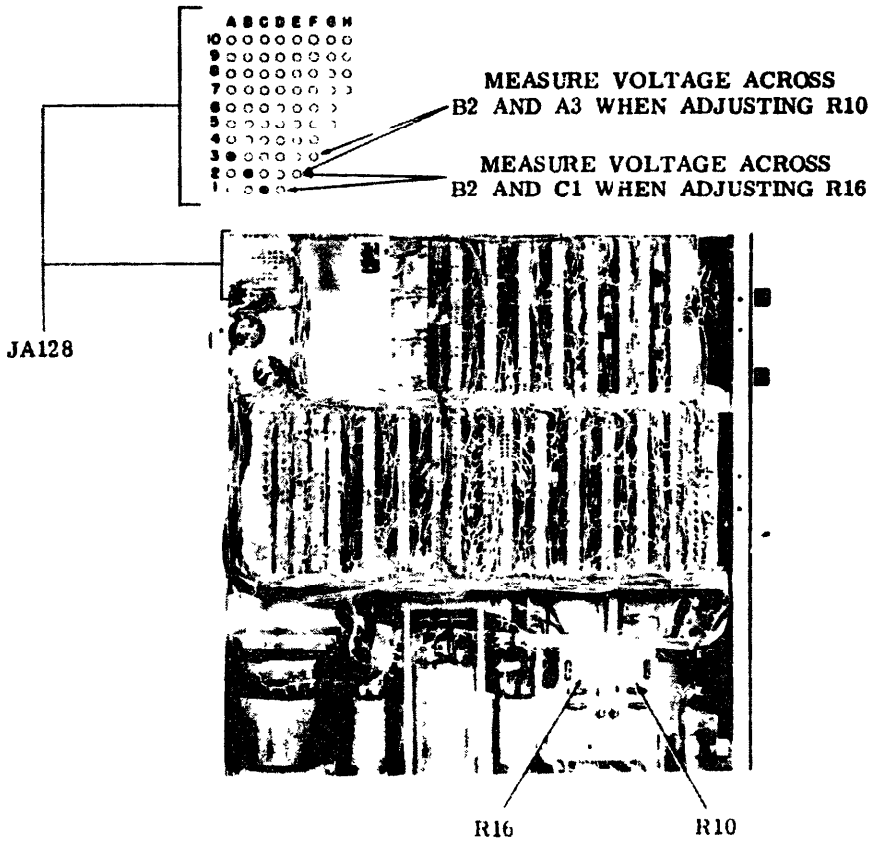


Figure 2- Module A, DC Voltage Adjustment

2. ADJUSTMENTS

ELECTRICAL (AC AND DC)

2.01 With Rower applied to themaster sender cabinet, the ac voltage reading at terminal board TBG101 (terminals 3 and 4) should be between 105 and 130 volts.

2.02 To check the -6 volt output of the power supply, place a dc voltmeter between pins B2 and A3 on connector JA128. Make adjustment, if necessary, at resistor R10 on power supply regulator card (bottom of module A) until meter reading is -6 volts ±5% (Figure 2).

2.03 To check +6 volt output of the power supply - place a dc voltmeter between pins B2 and Cl on connector JA128. Make adjustment, if necessary, at resistor R16 on power supply regulator card until meter reading is +6 volts ±5%.

2.04 Although the remaining power supply voltages are not adjustable, the voltage readings should be within the following tolerance limits.

(a) -12 volts ±5% - take reading between pins B2 and A2 on JA128.

(b) -28 volts ±5% - take reading between pins B2 and F2 on JA128.

(c) -48 volts ±5% - take reading between pins A2 and A1 on JA128.

ELECTRONIC

2.05 Disconnect all external equipment from the tape sender cabinet before adjusting the following delay circuits using the 100 hertz multivibrator on EC626 card in position ZA106 located in module A. Connect a strap, for testing purposes, from pin B31 of ZA106 to pin B20 of ZA106. Remove this test strap after adjustments are completed.

2.06 Delay Circuits

DELAY ZB319-A 50 MICROSECONDS

(a) Remove cards ZB322, ZB324 and ZB514

(b) Strap pin A34 of ZA106 in module A to pm A32 of ZB319 in module B.

(c) With the scope probe on pin A34 of ZB319, a positive pulse should appear on the screen.

(d) Adjust resistor R101 of ZB319 until positive pulse lasts 50 microseconds.

(e) Replace cards ZB322, ZB324, ZB514 and disconnect one end of strap from pin A32 of ZB319.

DELAY ZB317-B 800 MICROSECONDS

(a) Remove cards ZB524 and ZB526.

(b) Strap pin A34 of ZB106 to pin A22 of ZB317.

(c) A positive pulse should appear on the scope screen when the scope probe is on pin B27 of ZB317.

(d) Adjust R102 on ZB317, until positive pulse lasts 800 microseconds.

(e) Replace cards ZB524, ZB526 and remove strap from pm A22 of ZB317.

DELAY ZB317-A 1.6 MILLISECONDS.

(a) Remove card ZB319 and strap pin A34 of ZA106 to pin A32 of ZB317.

(b) With the scope probe on pin A34 of ZB317, a positive pulse should appear on the scope screen.

(c) Adjust R101 of ZB317 until the positive pulse lasts 1.6 milliseconds.

(d) Replacecard ZB319 and remove strap from pm A32 of ZB317.

DELAY ZB315-B 110 MICROSECONDS

(a) Remove card ZB317 and strap pin A34 of ZA106 to pin A22 of ZB315

(b) With the scope probe on pm B27 of ZB315, a positive pulse should appear on the scope screen.

(c) Adjust R102 of ZB315 until the positive pulse lasts 110 microseconds.

(d) Replace card ZB317 and remove strap from pm A22 of ZB315.

2.07 Delay Circuits (continued)

DELAY ZB315-A 110 MICROSECONDS

(a) Remove cards ZB324 and ZB319, and strap pin A34 of ZA106 to pin A32 of ZB315.

(b) with the scope probe on pin A34 of ZB315, a positive pulse should appear on the scope screen.

(c) **Adjust R101 on ZB315 until the positive pulse lasts 110 microseconds.**

(d) Replace cards **ZB319 and ZB324, and remove strap from pin A32 of ZB315.**

DELAY ZB319-B 50 MICROSECONDS

(a) Remove cards ZB315 and ZB324, and strap pin A34 of ZA106 to pin A22 of ZB319.

(d) With the scope probe on **pin B22 of ZB319,** a negative pulse should appear on the scope screen.

(c) Adjust R102 **on ZB319** until the negative *pulse lasts 50* microseconds.

(d) Replace cards *ZB315 and ZB324, and re-*move strap *from* pin A22 of ZB319.

DELAY ZB512-B 225 MILLISECONDS

(a) Attach scope scope to pin B27 of ZB512.

(b) Connect one end of a strap to pin A16 of ZB512 and momentarily touch pin A22 of ZB512 with the other end.

(c) A positive pulse should appear on the scope screen.

(d) Adjust R102 on ZB512 until a positive pulse lasts for 225 milliseconds.

(e) Remove strap from pin A16 of ZB512.

DELAY *ZB508-A 25* MICROSECONDS

(a) Remove cards ZB319, ZB322, ZB514, and strap pin A34 of ZA106 to pin A32 of ZB508.

(b) With scope probe on pin A34 of ZB508, a positive pulse should appear on the screen.

(c) Adjust R101 of ZA311 until positive pulse lasts for 25 microseconds.

(d) Remove strap from pins A34 and A32. Replace cards ZB319, ZB322, and ZB514.

DELAY ZB510-A 2.2 MILLISECONDS

(a) Remove cards *ZB319, ZB522, and* strap pin A33 of ZB510 to ground.

(b) Strap pin A34 of ZA106 to pin A32 of ZB510 and attach scopeprobe to pin A34 of ZB510.

(c) Adjust **R101** of ZB510 until positive pulse on scope screen lasts for 2.2 milliseconds.

(d) Remove the strap from pin A33 to ground and from pin A34 to pin **A32.**

(e) Replace cards ZB319 and ZB522.

DELAY ZA108-A 0.5-SECOND

(a) Connect one end of a strap to pin A16 of ZA108.

(b) With the scope probe on pin A34 of ZA108, momentarily touch pin **A32** of ZA108 with the other end of the strap connected to pin A16.

(c) A positive pulse should appear on the scope screen.

(d) Adjust R101 of ZA108, until the positive pulse lasts for 0.5 second.

(e) Do not remove strap connected to pin A16 of ZA108.

DELAY ZA108-B OS-SECOND

(a) With the scope probe on pin B27 of ZA108, momentarily touch pin A22 of ZA108 with the other end of the strap connected to pin A16 of ZA108.

(b) A positive pulse should appear on the scope screen.

(c) Adjust R102 on ZA108 until the positive pulse lasts for 0.5-second.

(d) Remove strap connected to pin A16 of ZA108.

DE LAY ZA311-A 2 MILLISECONDS

(a) Remove cards ZA319, ZA321, and ZA317, and strap pm A34 of ZA106 to pin *A32* of ZA311.

(b) With the scope probe on pm A34 of ZB311, a positive pulse should appear on the scope screen.

2.08 Delay Circuits (continued)

(c) Adjust R101 of ZA311 until the pulse lasts for 2 milliseconds.

(d) Remove the strap from pin A34 to pin A32, and replace cards ZA321, ZA319, and ZB317.

DELAY ZE108-A AND ZE108-B 0.5-SECOND
(Supplementary Cabinet)

Follow identical procedure used for 0.5-second delays in position ZA108-A and ZA108-B.

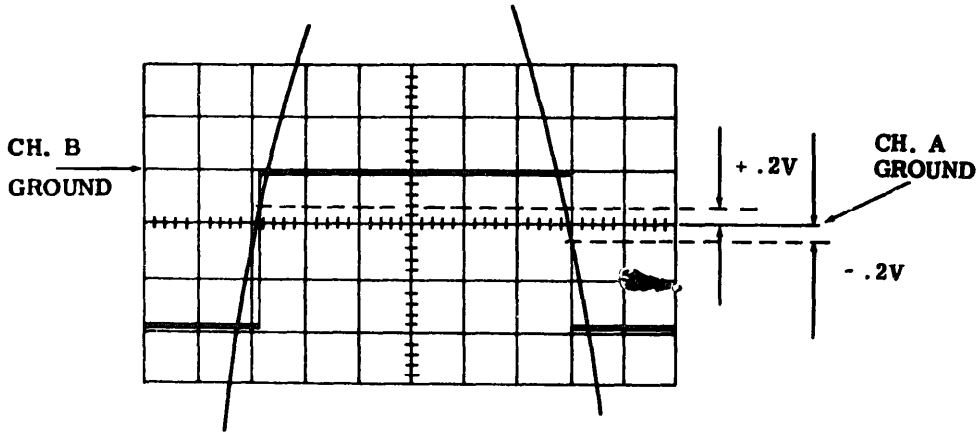


Figure 3- Input ZA302-A and ZA302-B Adjustment

INPUT CARDS ZA302-A AND ZA302-B

(a) Remove all external equipment connected to the tape sender.

(b) Connect one side of the secondary winding of a 6.3 volt filament transformer (customer provided 6.3 volt ac source) to pm 20 of ZA302, and the other side of the secondary winding to pin 34 of ZA302.

(c) Connect primary winding to 117 volts ac.

(d) Use the following oscilloscope set up:

1. Set the trigger slope to "+ line" and the trigger mode to "auto" position.
2. get time base at one millisecond per centimeter and input mode switch to "chopped" position.
3. Adjust channel A trace (0 volt input) to center of the grid, and set input attenuator selector to 0.1 volt per division.
4. Adjust channel B trace (0 volt input), two divisions from the top of the grid, and set input attenuator selector to 0.2 volts per division.
5. Phasing of the transformer may have to be reversed, or, use the "- line" (minus line) on the scope trigger input to obtain the proper waveform.

(e) Place channel A scope probe Xl (times 1) on pin 34 of ZA302-A, and channel B scope probe X10 (times 10) on pin 32 of ZA302-A.

(f) Adjust R7 of ZA302-A, until output at pin 32 switches with a symmetrical input sig- between +0.05 volts, and +0.5 volts at pin 34, with respect to ground (Figure 3).

(g) Move the clip lead of the 6.3 volt transformer from pm 34 of ZA302-A to pin 26 of ZA302-B. Movechannel A scope probe from pin 34 of ZA302-A to pm 26 of ZA302-B, and move channel B scope probe from pin 32 of ZA302-A to pin 22 of ZA302-B.

(h) Adjust R8 of ZA302-B until the output at pin 22 switches with a symmetrical input signal, between +0.2 volts and +0.5 volts at pin 26 with respect to ground.

MECHANICAL

2.09 Tape Transport Mechanism

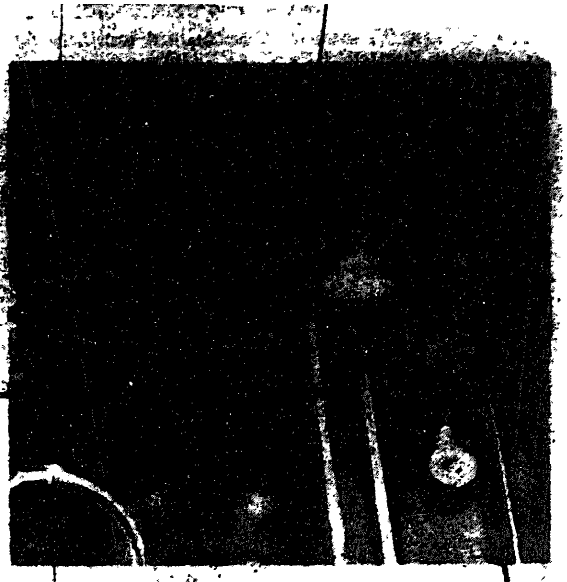
TAPE PULLER SHAFT

Requirement
The tape puller shaft should pass horizontally through the approximate center of its clearance hole in the front panel.

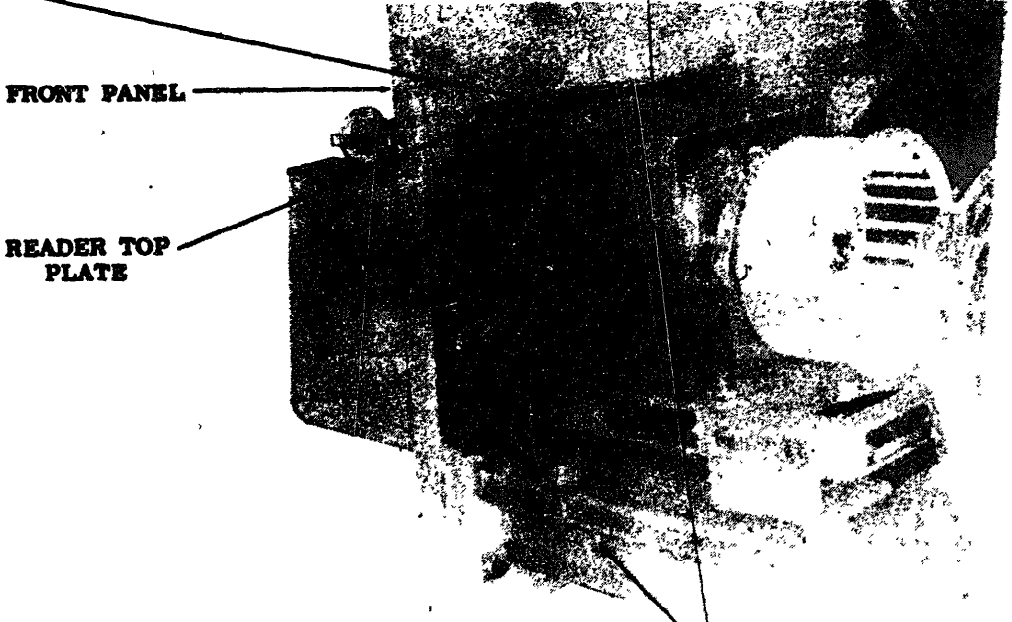
To Adjust
Loosen four screws on the upper crossbar mounting bracket, and position the crossbar until the shaft is centered in the panel hole. Tighten screws.

LOWER CROSSBAR

Requirement
The lower crossbar mounting bracket should be horizontal and positioned vertically to allow clearance between the tape reader top plate and the front panel access hole.



UPPER CROSSBAR MOUNTING SCREWS (2 Each Side)



To Adjust
Loosen the four lower crossbar mounting screws and position the crossbar to meet the requirement above. Tighten screws.

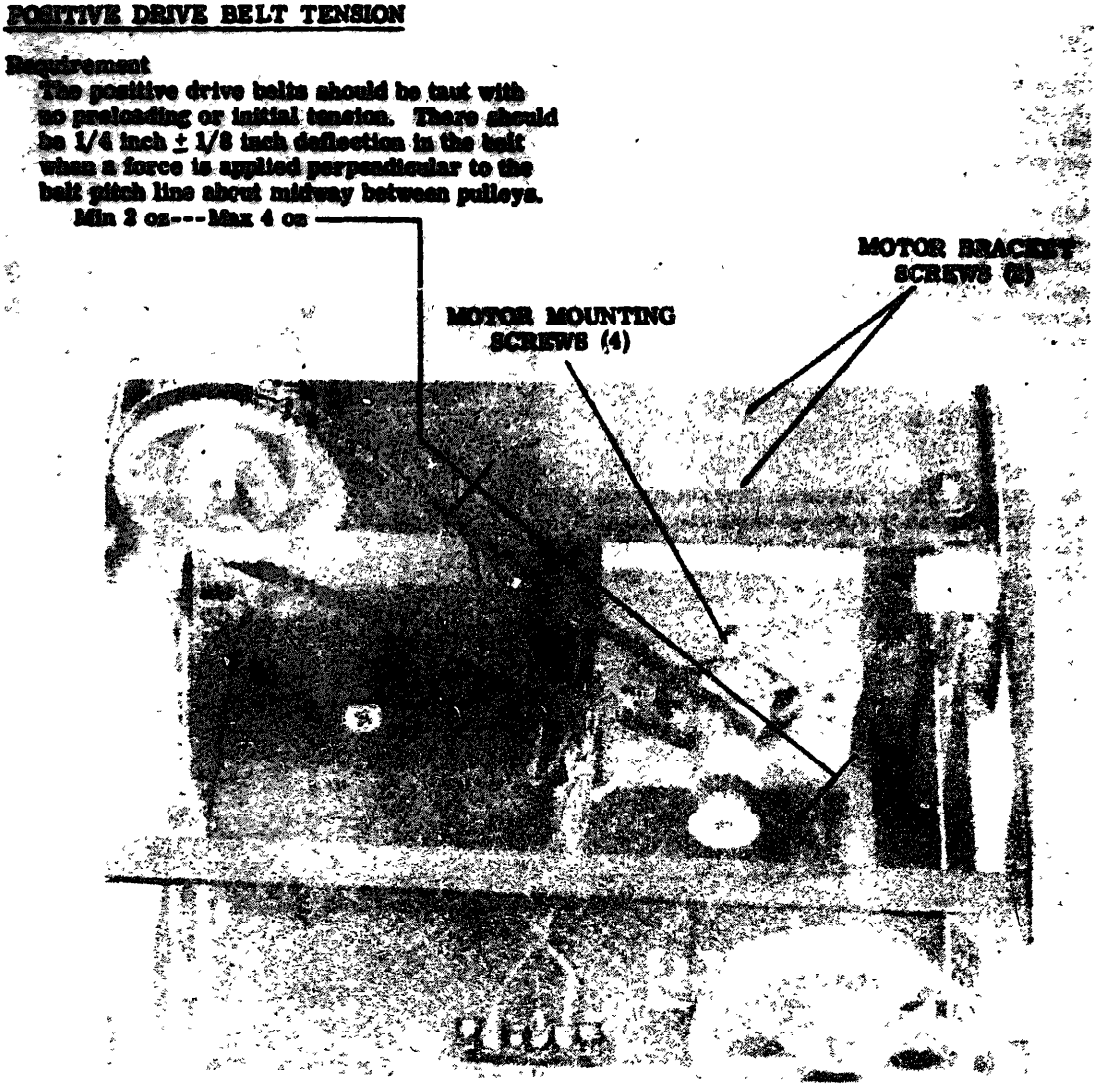
LOWER CROSSBAR MOUNTING SCREWS (2 Each Side)

2.10 Tape Transport Mechanism (continued)

POSITIVE DRIVE BELT TENSION

Requirement

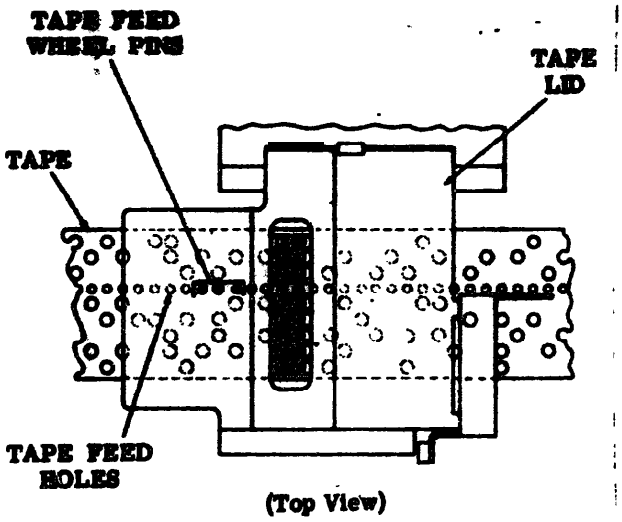
The positive drive belts should be taut with no preloading or initial tension. There should be 1/4 inch ± 1/8 inch deflection in the belt when a force is applied perpendicular to the belt pitch line about midway between pulleys. Min 2 oz---Max 4 oz



To Adjust

Loosen the six screws mounting the motor and motor bracket, position the motor and bracket until the above requirement is met. Tighten screws.

2.11 Tape Transport Mechanism (continued)



(Top View)

HIGH SPEED TAPE READER

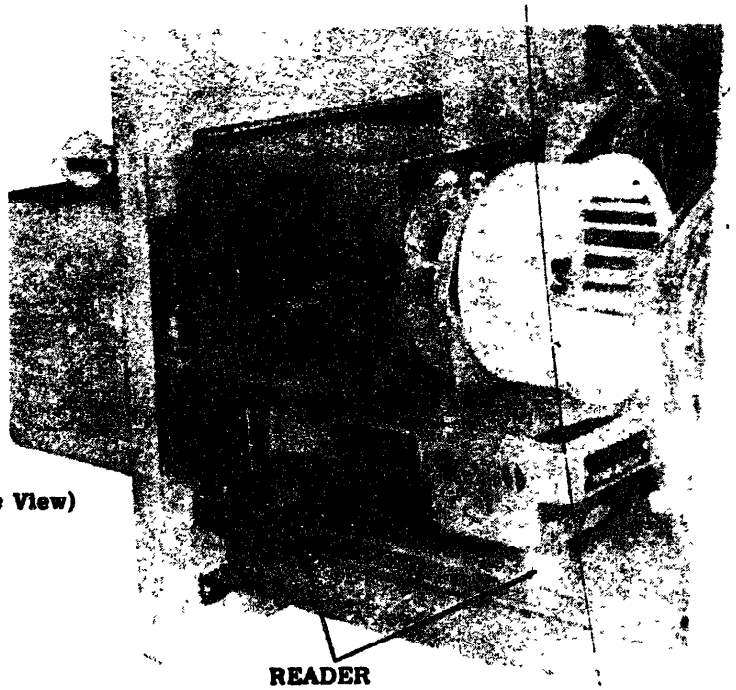
Requirement

The reader tape feed wheel should be aligned in the same plane as the tape feed holes.

To Adjust

Loosen the four mounting screws holding the tape reader assembly to the horizontal mounting panel. With tape threaded through the tape transport and the reading head, lift the reader tape lid and slide the reader forward or backward until tape and feed wheel are aligned.

Note: Further adjustments and list of special tools for DX2 high speed tape reader can be found in Section 592-804-700TC.



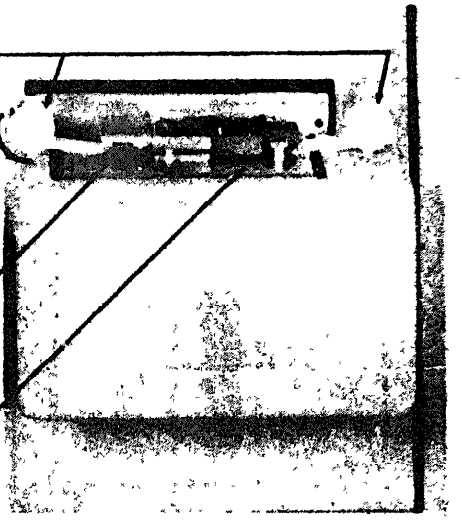
(Right Side View)

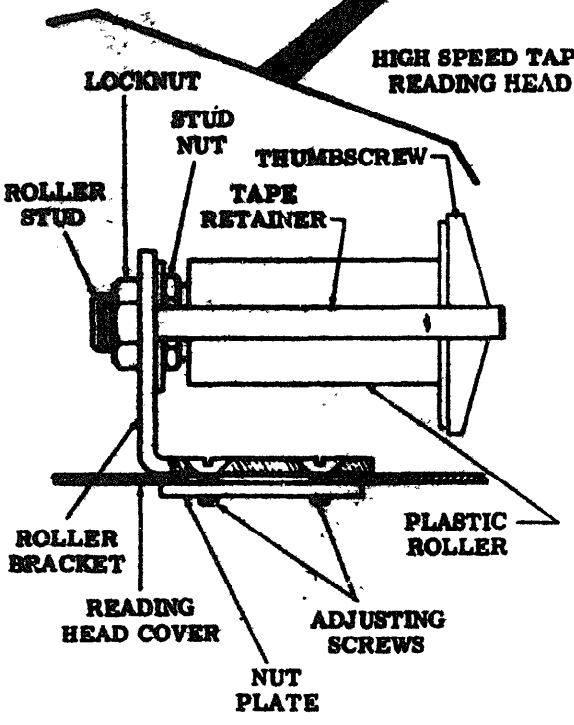
2.12 Tape Transport Mechanism (continued)

READING HEAD TAPE ROLLERS

Requirement

Position the guiding surface of the reading head tape rollers with the feed wheel and tape path through the tape reading head.





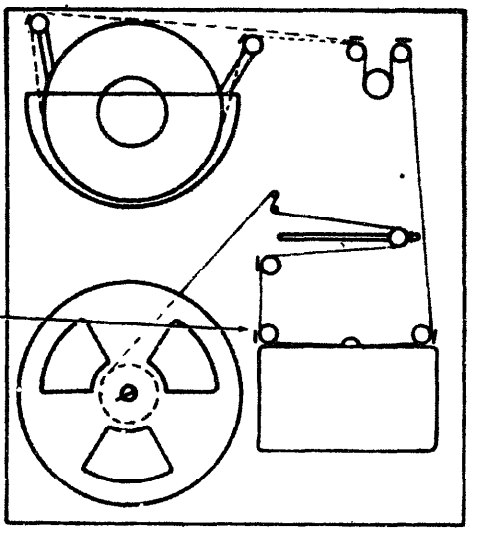
To Adjust

Loosen the knurled thumbscrews on the reading head tape rollers (2), remove screws, and plastic tape roller guide. Loosen the two flat head adjusting screws on each bracket and replace rollers. Thread tape through tape transport system and position rollers until requirement is met. Tighten adjusting screws and thumbscrews on each tape roller.

TAPE RETAINERS

Requirement

Tape retainers should be positioned as illustrated. (Gauge position of tape retainers by eye.)



To Adjust

Loosen roller stud nuts and position tape retainers to meet requirement above. Tighten roller stud nuts while holding retainer in place

2.13 Tape Transport Mechanism (continued)

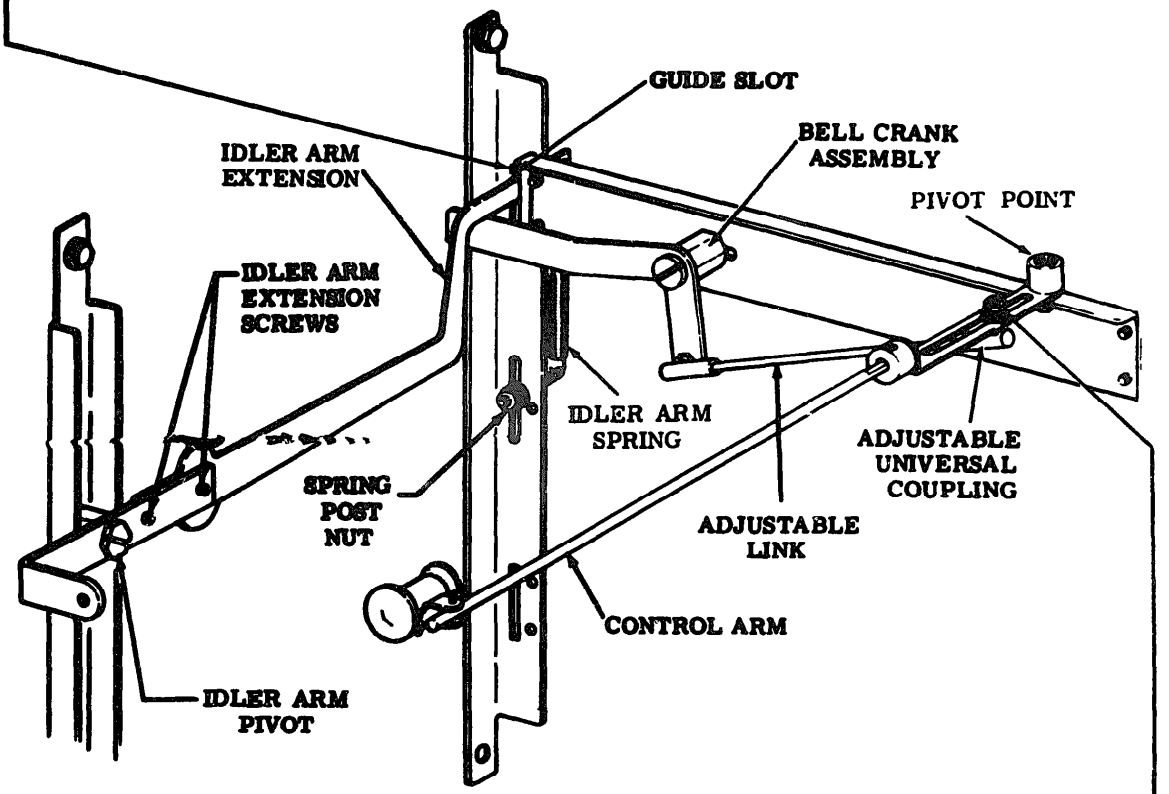
TAPE TENSION

Requirement

When the control arm moves to the extremes of its travel, the end of the idler arm extension should move a minimum of 75 percent through the length of its guide slot.

To Adjust

(1) Loosen locknuts on adjustable link and extend the length (between universals) to approximately 4-3/4 inches. Tighten locknuts.



(2) Position the adjustable universal coupling and the control arm pivot point at a distance of approximately 1-1/4 inches from each other. Loosen the bell crank assembly.

(3) With the control arm at the extreme right and the idler arm extension at the bottom of the guide slot, adjust the bell crank assembly to come in contact with the idler arm extension. Tighten the bell crank assembly.

To Check

If a satisfactory adjustment cannot be made at first, position the adjustable universal coupling, and bell crank assembly, until the requirement can be obtained.

2.14 Tape Transport Mechanism (continued)

V BELT CLUTCH

(1) Requirement

As the idler arm extension travels through 75 percent of its guide slot, the V belt should change from fully engaged to disengaged (slipping).

(1) To Adjust

Loosen the idler arm pivot screw and slide the idler arm up or down until it is parallel to the winder shaft with the belt fitting firmly on its pulleys. Tighten the idler arm pivot screw.

(2) To Adjust

Loosen the two idler arm extension screws and position the idler arm sections to provide a tight fit on the belt and pulley when the end of the idler arm extension is about 1/8 inch from the bottom of its guide slot. Tighten the idler arm extension screws.

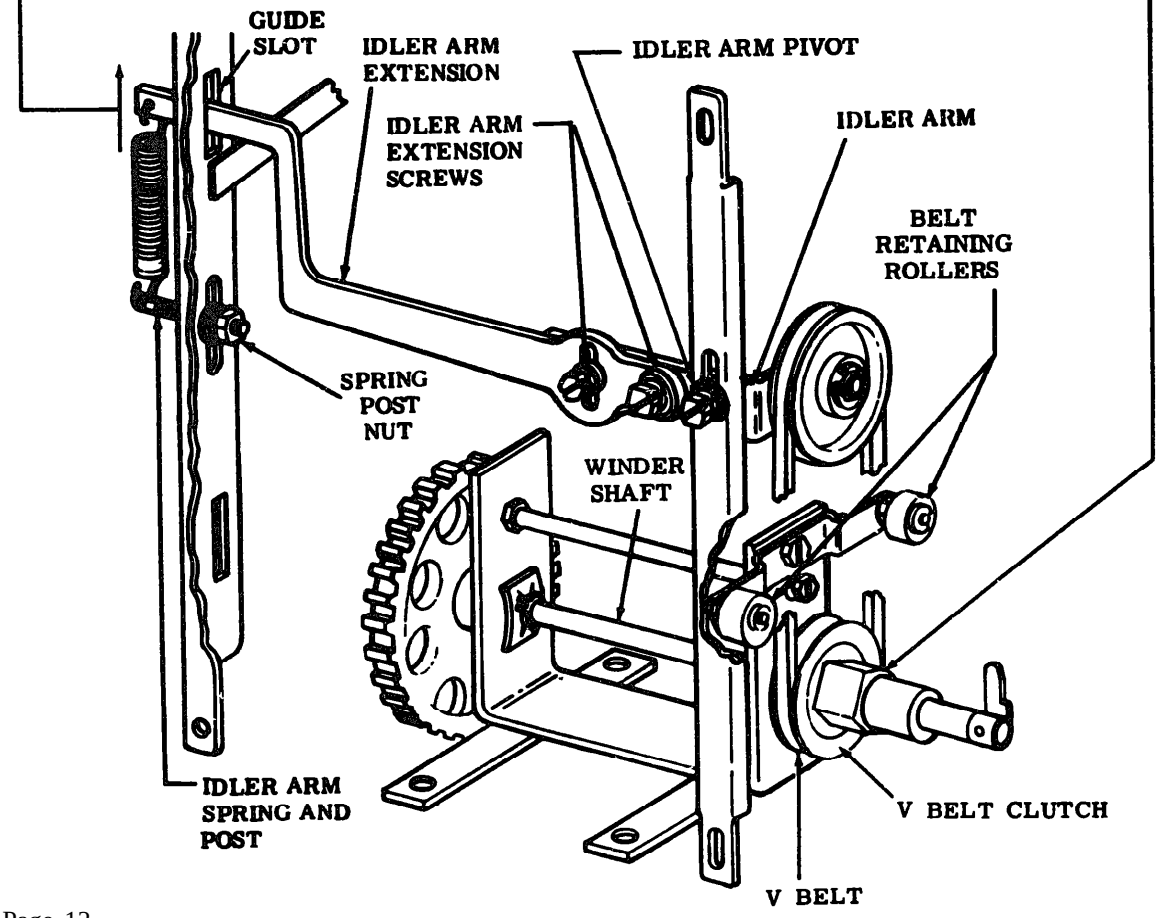
(2) Requirement

To bring the spring end of the idler arm extension to the top of its guide slot, it should require an upward pull of

Min 16 oz---Max 22 oz

To Adjust

With the control arm (2.13) to the right (free position), loosen the spring post nut below the end of the idler arm extension. Position the spring post and check pull with an ounce gauge until requirement is met. Tighten spring post nut.



3. REMOVAL AND REPLACEMENT OF COMPONENTS

MODULE REMOVAL

3.01 Turn the locking screw (located at the top front of each module panel) counter-clockwise, freeing the fastener from the tab on the inner cabinet frame (Figure 4).

3.02 Slide the module out to its fully extended position (stopped by the same tab at the front of the inner cabinet frame), tilt the front of the module upward (pull out bottom and lower slightly) until lip of module frame is clear of tab on inner cabinet frame. Lower module to the floor (Figure 4).

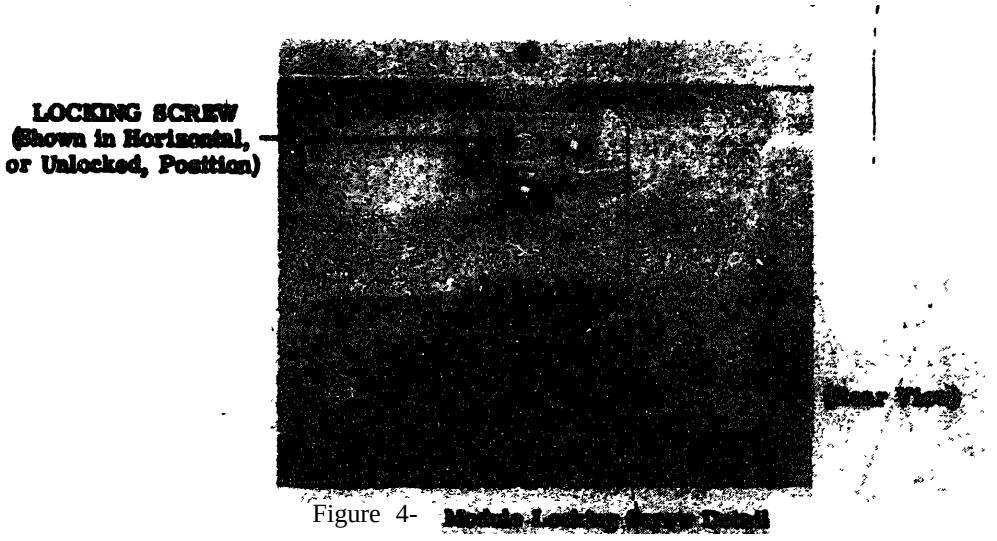


Figure 4- Module Locking Screw Detail

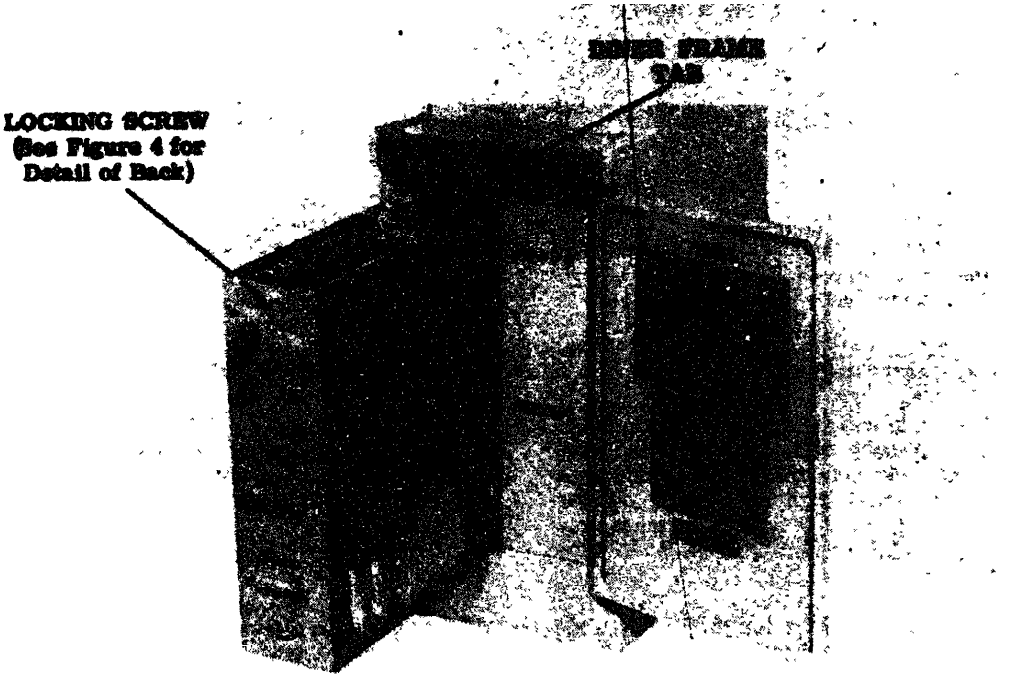


Figure 5- Module Removal

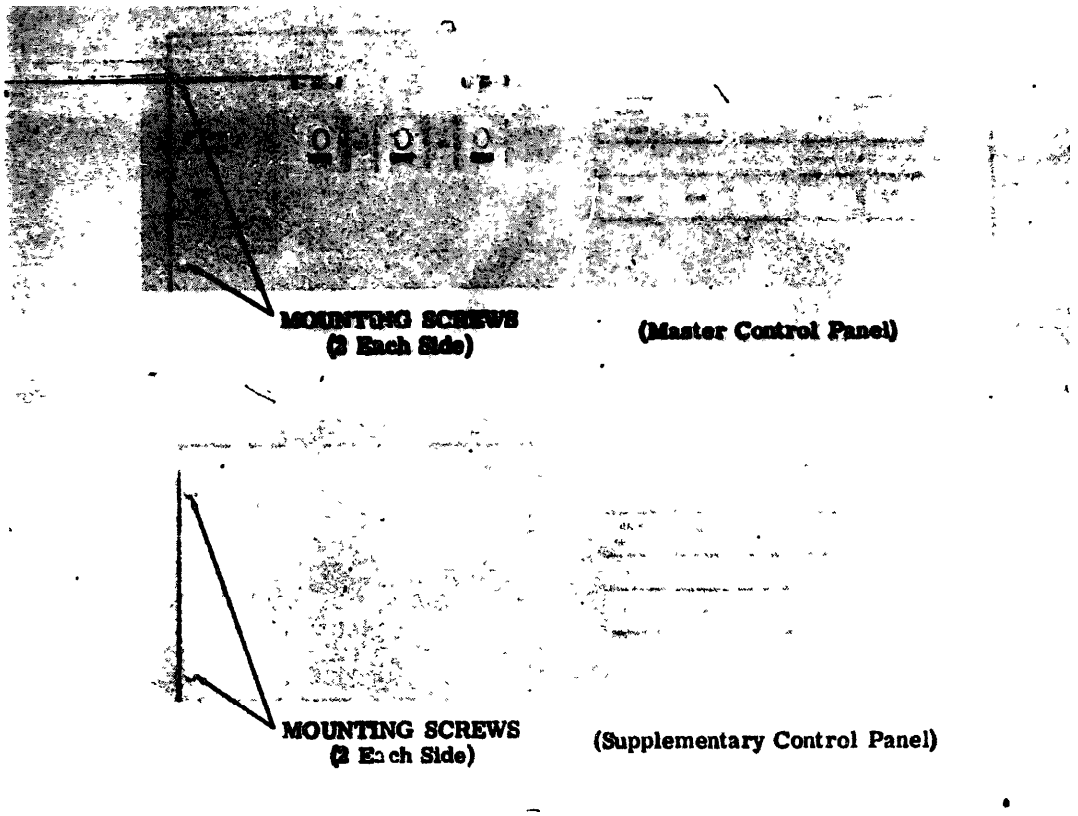


Figure 6- Master and Supplementary Control Panels

3.03 Connecting cables at the rear of the module can be disconnected if necessary. *Reverse the procedure in 3.01* **and 3.02** to replace module-in cabinet.

TAPE TRANSPORT REMOVAL

3.04 When removing tape transport panel from cabinet, remove all wires from TB1, TB2, and ground wires from ground connections. Disconnect high sped tape reader connector and tape *reader* motor fuse connector. Remove cable clamps holding cable to tape transport **frame.**

3.05 Slide tape **transport forward** until slide stops are engaged, tilt bottom of panel up and out disengaging slides from stops. Re**verse** procedure to reassemble panel in cabinet (Figures 7 and 8).

Note: Tape transport slides should be aligned symmetrically with cabinet slides to eliminate binds when sliding transport in and out of cabinet.

CONTROL PANEL REMOVAL

3.06 Remove the four front panel mounting screws, pull control panel forward and disconnect panel connector. Reverse procedure for reassembling control panel to cabinet.

TAPE READER REMOVAL

3.07 Lift the tape lid to remove tape from reading head, Close the tape lid after tape removal. Slide out tape transport assembly to extended position and disconnect the 50-pin connector from rear of tape reader.

3.08 **Remove the four screws mounting the tape reader to the lower crossbar bracket and slide out tape reader from the tape transport assembly. Tilt the rear of tape reader assembly up while sliding reading head from front panel. (Avoid contact with tape transport frame when removing the tape reader from right side of transport assembly.)**

3.09 **Complete disassembly and reassembly information for the high speed tape reader can be found in Section 592-804-702TC.**

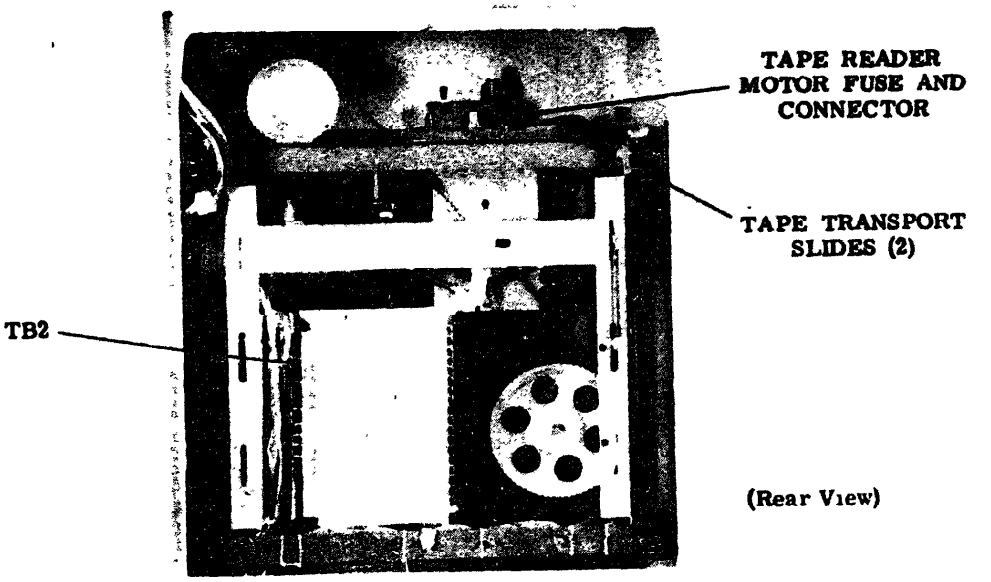


Figure 7- Tape Transport

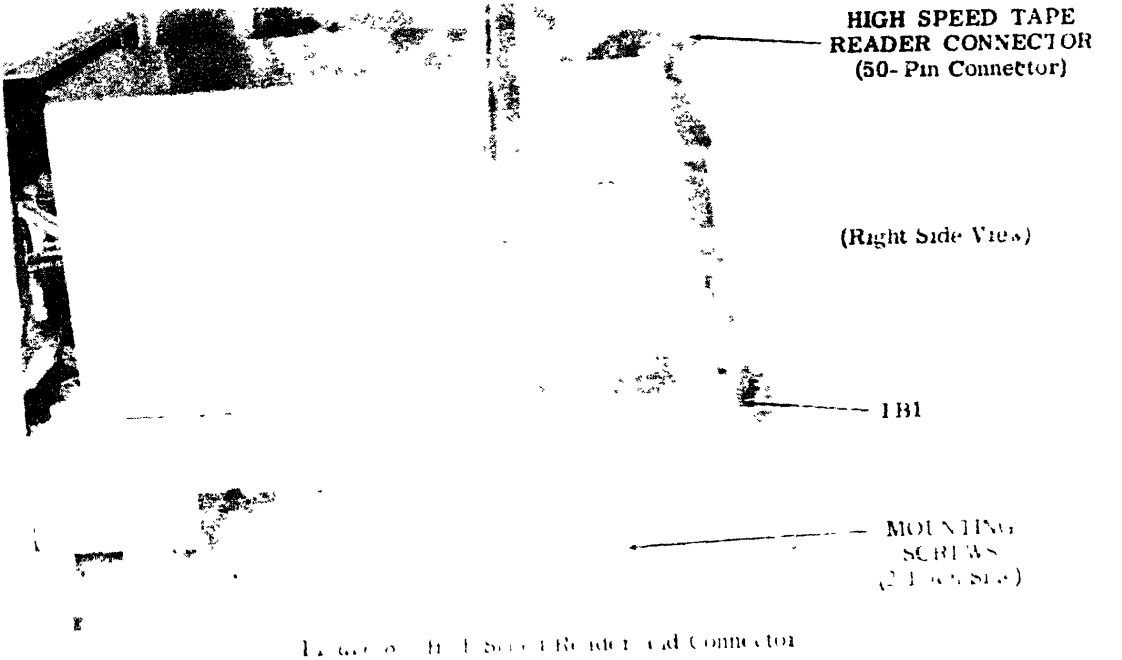


Figure 8- High Speed Reader and Connector

TELETYPE CORPORATION
Skokie, Illinois, U.S.A.

SECTION 592-851-731TC
Issue 1, March 1969

MASTER AND SUPPLEMENTARY HIGH SPEED

TAPE SENDER FOR THE MULTIPLE ADDRESS

PROCESSING SYSTEM (MAPS)

LUBRICATION

CONTENTS **PAGE**

1. GENERAL

1.01 This section provides lubrication information for the master and supplementary tape sender sets. It is issued as a separate section for the first time and includes the latest engineering information. This information was formerly included as a part of Section 592-851-730TC.

CAUTION: REMOVE POWER FROM THE CABINET BEFORE LUBRICATING.

1.02 Lubricate the unit prior to placing in **service. After a few weeks** of service, relubricate to make certain all points receive lubrication. Thereafter the regular lubrication interval should be as follows:

SPEED	*OPERATING HOURS	*TIME
100 wpm	2,000	6 months
1200 wpm	**1,000**	**4 months**

***Whichever occurs first.**

CAUTION: OVERLUBRICATION WHICH ALLOWS OIL OR GREASE TO DRIP OR BE THROW ON ELECTRICAL CONTACTS OR ELECTRONIC ASSEMBLIES SHOULD BE **AVOIDED.**

1.04 The photographs and illustrations indicate points to he lubricated, specific instructions, and type of lubrication.

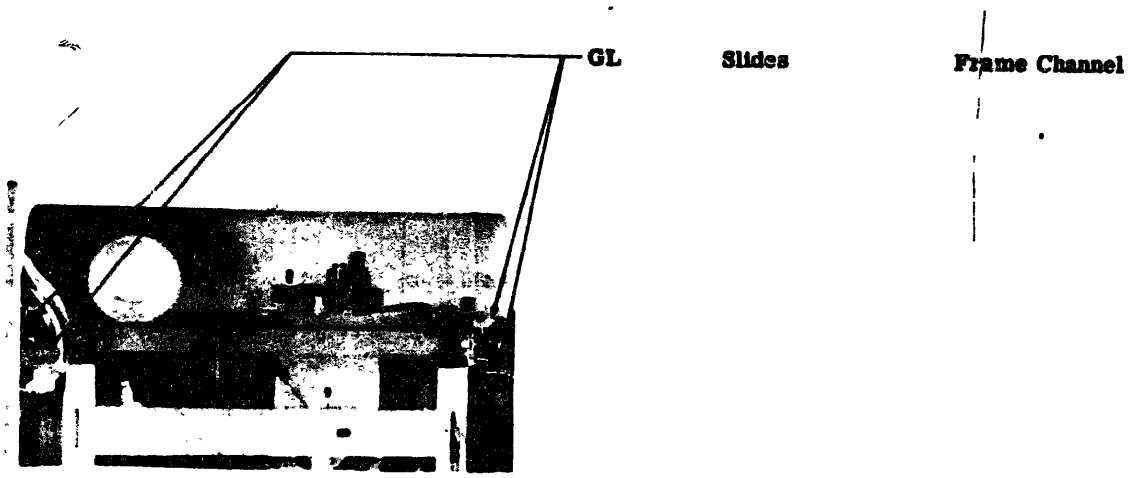
1.05 Lubrication symbols and directions are indicated as follows:

01 Apply 1 drop of oil
02 Apply 2 drops of oil
G Apply thin film of grease.
GL Apply thin film of grease, Lubriplate #105

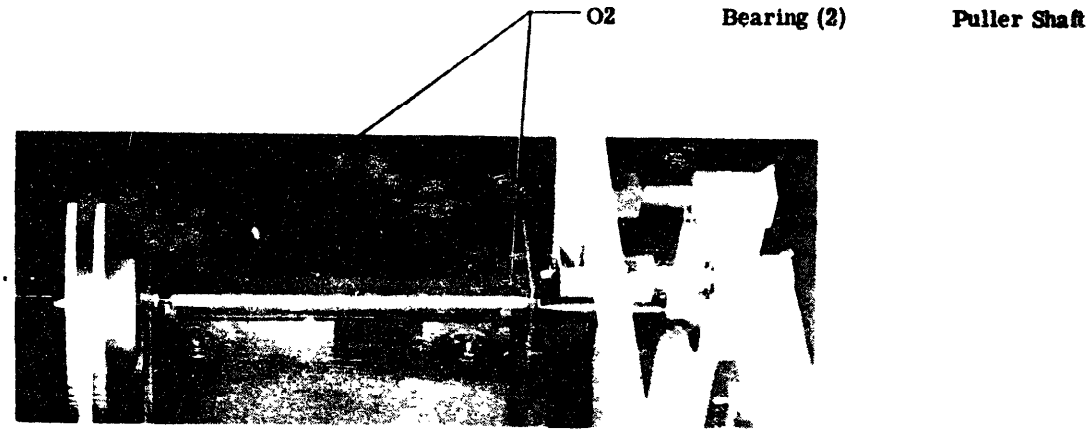
1.06 Use KS7470 oil on points indicating oil, KS7471 grease where grease is indicated, and TP108805 Lubriplate #105 Where Lubriplate is indicated. (Except on components where a referenced lubrication section is recommended.)

2. LUBRICATION

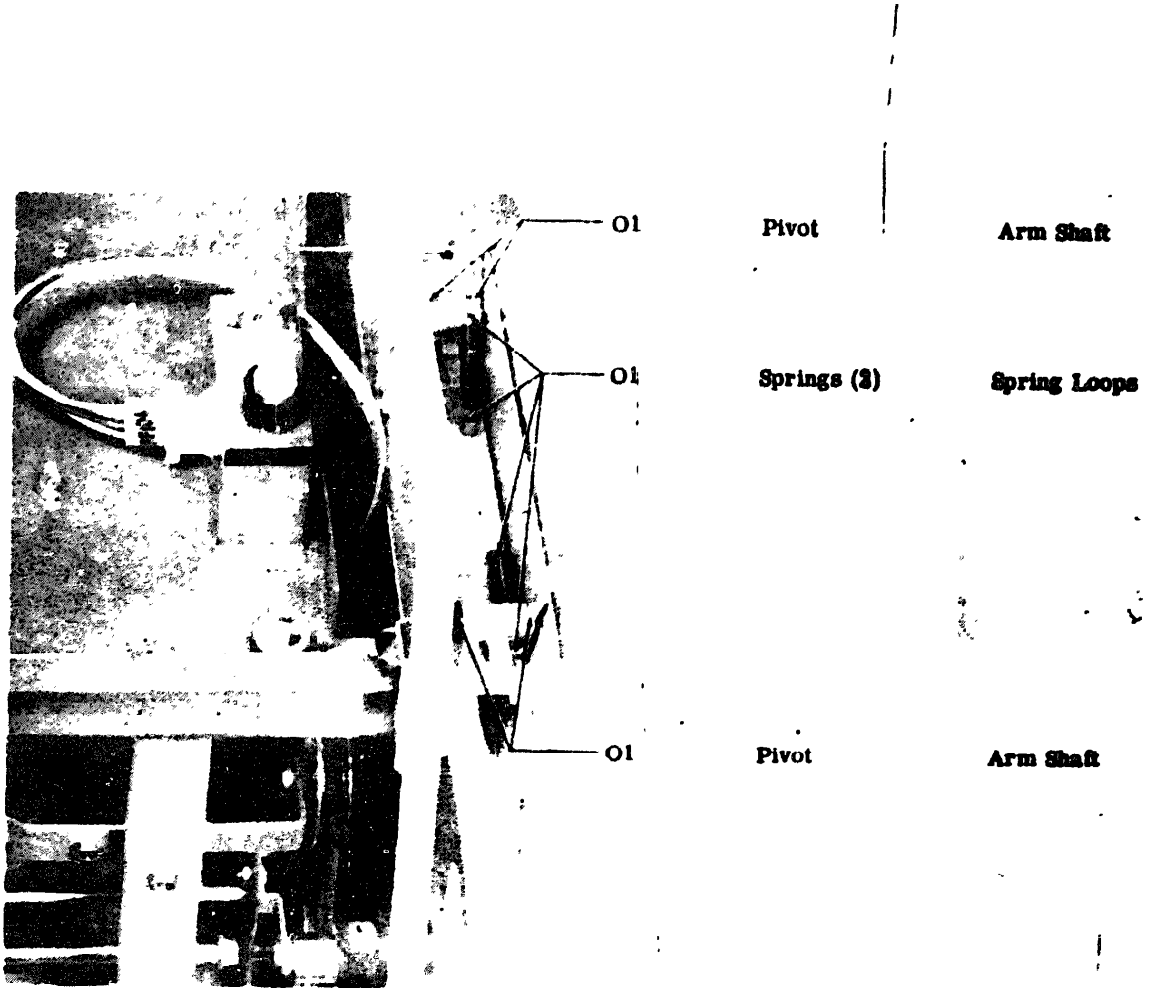
2.01 Tape Transport Slides



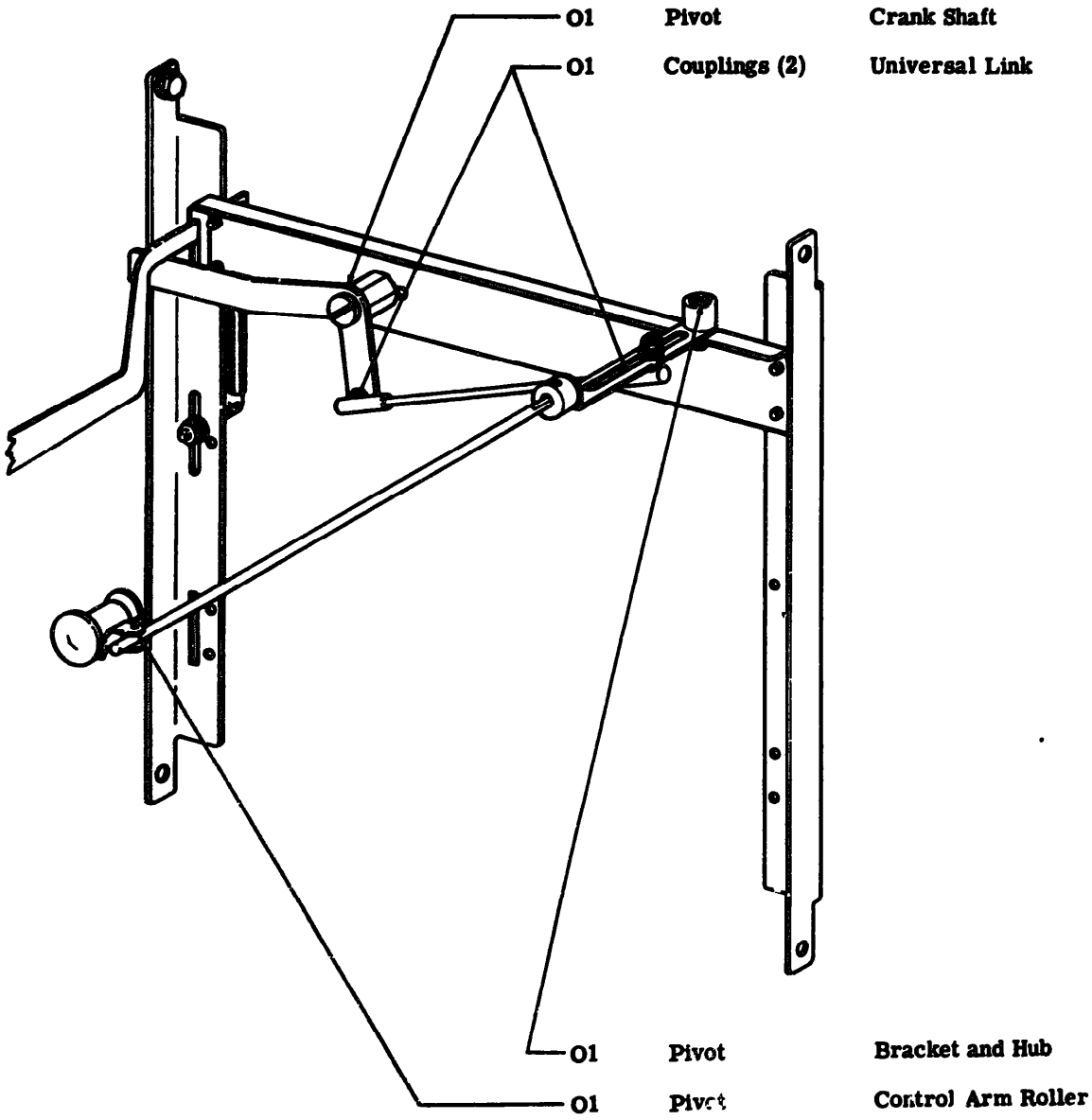
2.02 Tape Puller



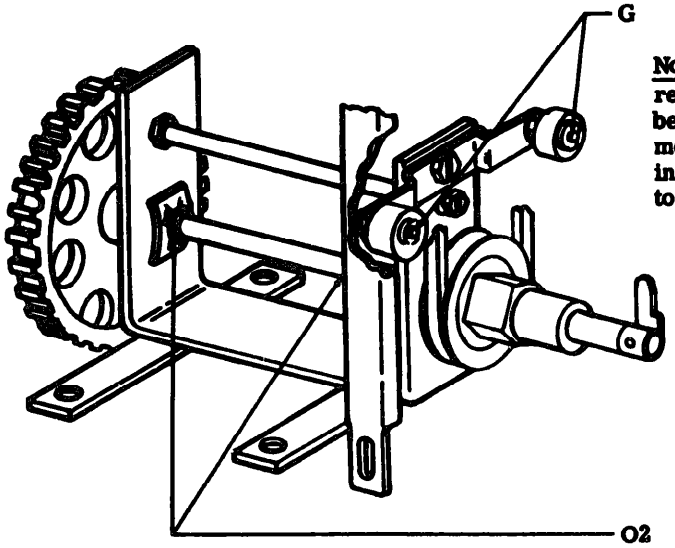
2.03 Tape Yield Arms



2.04 Bell Crank and Control Arm



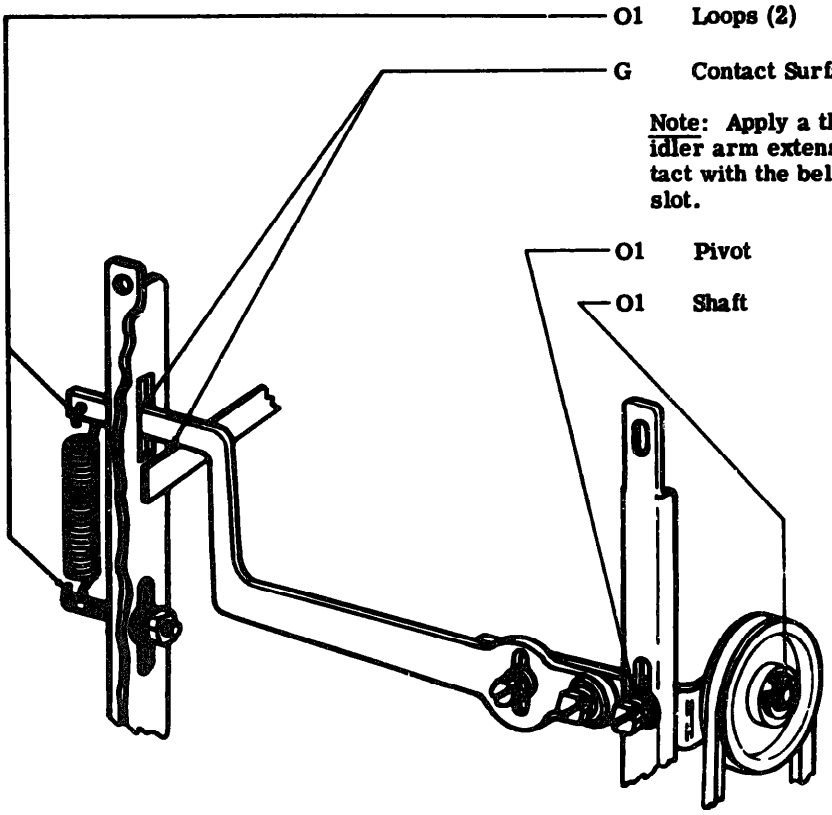
2.05 Tape Winder Mechanism



G	Shafts	Retaining Roller
O2	Bearings (2)	Winder Shaft

Note: Apply a thin film of grease to the retaining roller shafts, which guides the "V" belt between the idler and split pulley. Remove expansion rings holding roller guides in place and remove rollers, apply grease to shafts and replace rollers and rings.

2.06 Idler Arm Mechanism



O1	Loops (2)	Spring
G	Contact Surface	Arm Contact and Slot
O1	Pivot	Drive Arm
O1	Shaft	Pulley

Note: Apply a thin film of grease to the idler arm extension where it comes in contact with the bell crank assembly and guide slot.

TELETYPE CORPORATION
Skokie, Illinois, U.S.A.

HIGH SPEED TAPE RECEIVER FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

DESCRIPTION AND THEORY OF OPERATION

CONTENTS PAGE

1. GENERAL

1.01 **This section provides description, principles of operation, and circuit description for the high speed tape receiver. It is reissued to change the title, add the circuit description information (formerly covered in Section 592-852-430TC), remove preliminary designation and to place this section in standard format. It is also reissued to include the latest engineering changes covering tape punch door latches, door tape chutes, pushbutton circuit breakers, and relocated exhaust fans. Since this is a general revision, marginal arrows that indicate changes and additions are omitted.**

1.02 **The high speed tape receiver is part of the multiple address processing system (MAPS). It can receive messages at speeds up to 240 characters per second. It contains two high speed paper tape punches, each with its own 3000 foot tape supply, power supply, serial-to-parallel converter, punch drive logic, and verifier logic. As the receivers are independent and electrically identical, only one will be described in detail (Figure 1).**

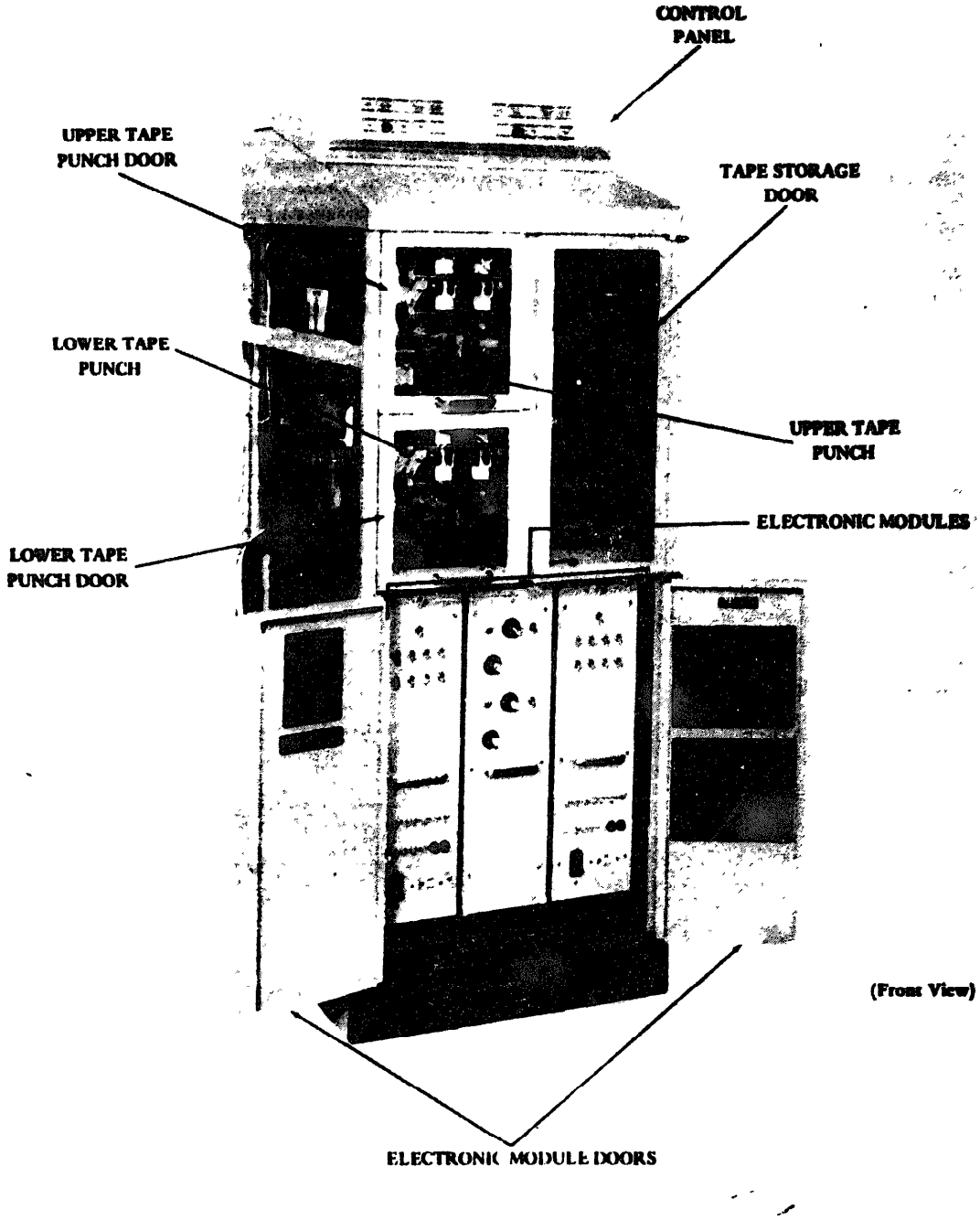


Figure 1 Receiver Cabinet

2. DESCRIPTION

2.01 Each system receives serial or parallel data at speeds up to 2400 words per minute. The data is recoded in the form of punched paper tape, 11/16, 7/8, or 1 inch in width. It is delivered to the operators through a tape chute in the front door of each set, no tape windup facilities are provided. When a tape size is changed, the tape supply bin, punch tape chute guide, punch block guide, and programmed feed-out character switches must be properly set.

2.02 Data is received as a serial pulse stream. It is changed to a parallel wire signal by the serial-to-parallel converter and delivered to the punch drive. Alternately, data may be received directly by the punch drive in parallel form. The parallel signal output of the serial-to-parallel converter is available to external equipment.

2.03 The parallel output of the serial-to-parallel converter (or directly from a parallel input) is converted to high power pulses by the punch drive circuits. The output is delivered with proper timing to drive the high speed tape punch, which punches the information presented to it.

2.04 The cabinet is 22 inches wide, 26 inches deep, and 60 inches high. Front access to tape punches, electronic logic, power supplies, and module control panels is through the front cabinet doors. Rear access is provided through two rear doors for maintenance purposes and connecting components and modules (Figure 2).

TECHNICAL DATA

A. Input Signal Requirements

2.05 All input signal voltages are nominally positive or negative 6 volts ±1 volt. The minimum input impedance for all signals is over 5000 ohms, and an input capacitance of less than 0.0025 microfarads. Input circuit switching occurs between the limits of ±0.5 volt or less.

B. Input Signal Characteristics

2.06 The serial data input is a +6 volts and -6 volts binary stream, with a character rate not exceeding 240 characters per second. The serial input is capable of incorporating 5 to 16 bits per character for synchronous operation, or 6 to 16 bits per character for start-stop operation. The start-stop signal always carries the first bit at the same polarity (either +6 volts or -6 volts) which the serial-to-parallel converter uses for character synchronization.

2.07 The synchronous signal carries no synchronizing information during data transmission. Character register is achieved during idle periods when a synchronizing pattern is present. In the start-stop operation, up to 15 bits per character are variable, while in the synchronous operation all bits are variable. The high speed reperforator punches up to 8-levels per character. The first 5, 6, 7, or 8 information bits of each character are detected and punched. The remaining bits are not detected by the system.

2.08 A binary timing clock input defines the receiving bit rate. This is a square wave signal with levels of +6 volts and -6 volts, and a bit time exactly twice the data bit rate. The positive going edge of the timing clock signal occurs in time with the beginning of each binary data bit. The negative going edge occurs at the center of the data bit.

2.09 The system optionally accepts a parallel signal input of 5 to 8 levels plus the character clock signal. Signal voltages are +6 volts for mark (punch), and -6 volts fir space (no punch). Signal inputs are present during the entire character, and a character clock signal defines character duration. Each positive going character clock puke occurs in time with the beginning of a character cycle and each negative edge occurs at the middle of a cycle. The idle state of the signal levels is +6 volts and of the character clock is -6 volts.

2.10 When operating with a parallel signal input, all 8 levels are active and independent of the portion of the level switch. If a spacing or no-hole condition as required at the reperforator on the unused levels of the tape. -6 volts must he supplied or strapped to the input of these particular levels of the input connector or the associated polar to neutral converter cards.

CAUTION: OPERATING THE RECEIVER WITH 11/16 INCH (5-LEVEL) TAPE WITHOUT STRAPPING (2.10) WILL RESULT IN MYTH EDGES OF THE TAPE BEING PERFORATED DUE TO THE MARKING CONDITION ON THE UNUSED LEVELS.

2.11 An urgent traffic input signal indicates the importance of an incoming message. The idle state of this signal is -6 volts. A pulse to +6 volts lights the URGENT TRAFFIC lamp on the control panel. External voltage sources (+6 volts and -6 volts) are accepted for possible use as power to the clock, data, and urgent traffic input circuits. If these sources are used, a strapping option IS required, and 2.05 does, not apply.

C. Output Signal Requirements

2.12 The open circuit output voltage of all signals is positive and negative 6 volts ±1 volt, and is balanced to within ±10 percent. The source impedance does not exceed 100 ohms, and the maximum short circuit current delivered to the interface is 0.1 amperes. The rise and fall times (wave shaping) of each output signal is greater than 5 percent of the unit interval duration.

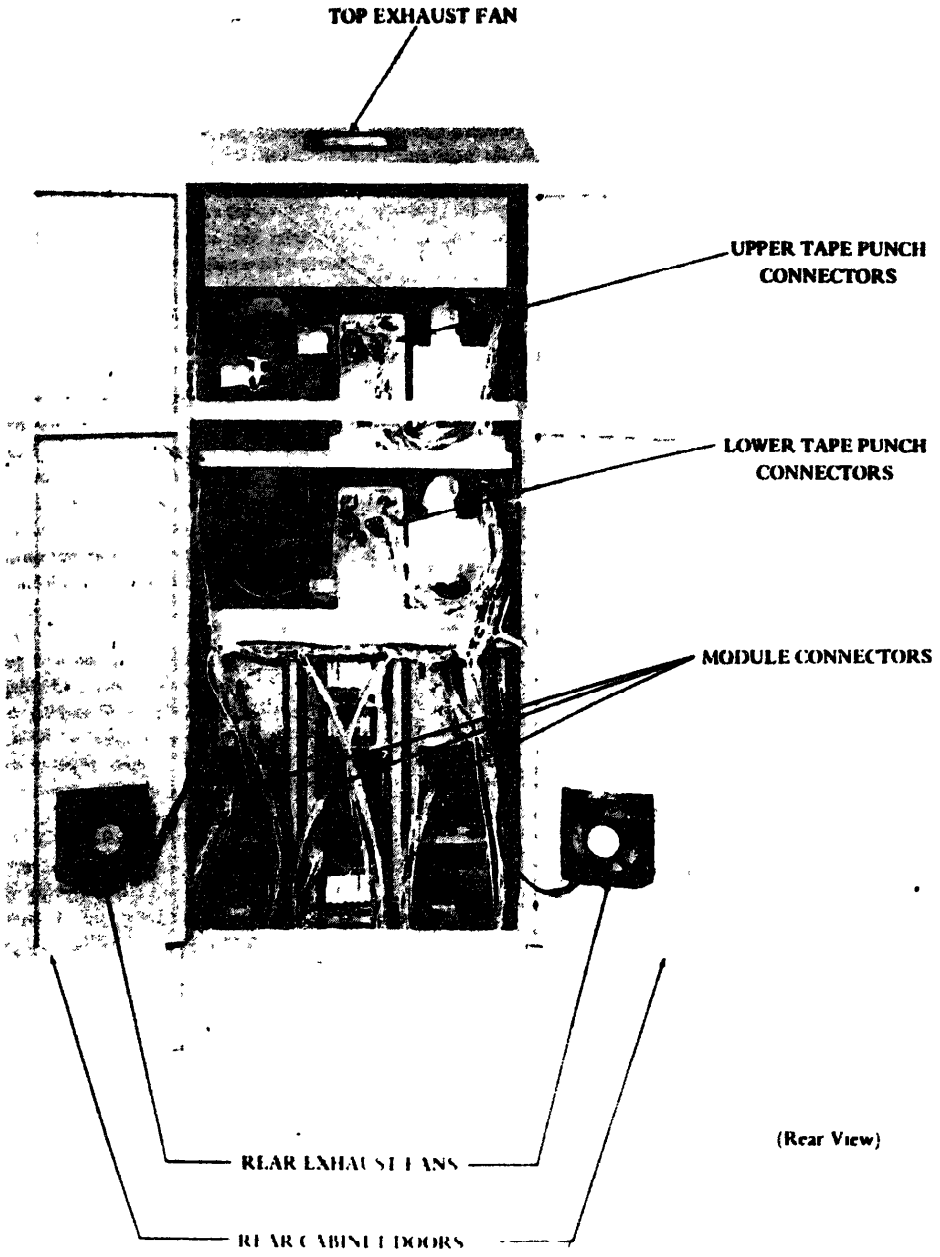


Figure 2 Receiver Cabinet

D. Output Signal Characteristics

2.13 **The output signal system delivers a parallel wire signal to external equipment. This signal, corresponding to the 5-, 6-, 7- or 8-level signal delivered to the punch, is available for the entire character duration. Positive 6 volts corresponds to a mark (punch) and negative 6 volts is a space (no punch). The 6, 7, and 8 bits, or unused levels for 5-level operation, are always -6 volts irrespective of the signal received. The idle state of these signals will be that of the last character received or that of the idle puttern.**

2.14 **A character timing pulse is provided with a positive going edge at the beginning of each character, and a negative going edge approximately two milliseconds later. The idle state of this signal is -6 volts. An urgent alarm transfer contact is provided to indicate that the associated punch cannot receive additional traffic.**

E. Serial-To-Parallel Distributor

2.15 **The serial-to-parallel distributor accepts a serial pulse stream and converts it to a parallel wire signal. The serial input may be 5 to 16 bits synchronous or 6 to 16 bits stop-start to define a character. The signal mode is selected by the operator with the appropriate switches.**

2.16 For synchronous transmission the first 5, 6, 7, or 8 bits are detected depending upon the code level selected. The remaining bits are ignored. For start-stop operation, the first bit of each character is always spacing and is used to identify the beginning of a character. The next 5, 6, 7, or 8 bits are detected and the remaining bits ignored.

2.17 The serial-to-parallel converter is programmed with respect to bit levels and signal sensing. For example, the bit level received as the second bit of a character may be programmed to be punched in the fifth tape channel. Also, a bit level received as a space may be programmed to be detected as a mark. This feature provides the flexibility of connecting any bit level to any punch level and of reversing the mark-space polarity of any bit level.

2.18 The output is a parallel 8-level signal. When in the 5, 6, or 7-level mode, the unused levels are delivered to the punch drive and to external outputs as spacing signals, regardless of the program arrangement.

2.19 The punch drive supplies power and punch commands required by the DRPE (tape punch) to reperforate a character. Parallel wire data is received from the serial-to-parallel converter. or directly from an external source.

F. Alarms

2.20 There are two types of alarms. urgent and advisory. An urgent alarm indicates that a condition has occurred requiring immediate operator attendance. The **specific cause of each urgent alarm is shown on the control panel by a red indicator, and the operation of a dry transfer contact common to all urgent alarms. This contact assembly is made available to external apparatus.**

2.21 The urgent alarms are latching type. Which means, if an alarm occurs and then occurs itself, the alarm indication will continue until reset manually by an operator. The urgent alarms are: TAPE OUT (at reperforator), END OF TAPE (supply), TIGHT TAPE (supply), and TAPE FEED (failure).

2.22 Advisory alarms are shown by a white indicator on the control panel. The alarm indication restores automatically when the condition is corrected. The advisory alarms are: LOW TAPE (apply), and CHAD BIN (full).

G. Controls and Indicators

2.23 All operator control switches and indicators are located on the front panel new the top of the high speed tape receiver cabinet. Control witches are the pushbutton type.

2.24 Additional controls are located on the front panels of the electronic modules behind the lower front cabinet doors. The following list of operator controls and indicators are bated on the top control panel. There are two sets of duplicated controls, the set to the left for the upper high speed tape punch, and the set to the right for the lower high speed tape punch (Figure 3).

2.25 The URGENT TRAFFIC indicator is operated by a positive pulse from external equipment, and is cleared by operating the associated reset switch.

2.26 The BUSY OUT switch closes the urgent alarm transfer contact and lights the indicator in red.

2.27 **The POWER switch controls power to the high speed tape punch motors and electronic modules.** The switch indicator lights when the POWER switch is activated and power is applied to each individual reperforator unit and is electronic modules.

2.28 The AUTOMATIC SYNC MODE and MANUAL SYNC MODE indicator and switch is a two-position split switch used with synchronous or start-stop operation. In the automatic position the synchronizing circuit is energized and tape receiver is phased with the incoming signal pattern. The associated indicator lights when the equipment is synchronized, The switch automatically returns to the manual mode, lighting its indicator and extinguishing the automatic indicator.

Figure 3-

2.29 When the MANUAL [illegible] is operated, it causes the loss of one clock pulse to the counter for each operation. This changes the reading and punching relative phase relationship. Once a channel and component synchronism is achieved. The clock switch is open when the associated indicator is lit.

2.30 Operating the [illegible] causes tape to be fed out at 100 characters per second with all spacing (no punches). This is an [illegible] which automatically operates the figure shift character. The punch cannot receive additional inputs at this time.

2.31 Operating the CHARACTER FEED switch causes tape to be fed out of the associated punch at 100 characters per second. The feed-out character is programmed on the front panel of the associated electronic module C. Since this is also an interfering feed-out, any incoming message character signal is canceled. This switch should be operated first after the power is on to eliminate the possibility of having a blank character (caused by power off-on) directly precede the first message.

Note: The remaining tape handling alarm indications are explained in 2.20 through 2.22.

H. Service Controls

2.32 The following additional controls are located on the front panels of the electronic modules behind the lower cabinet doors (Figure 1 and Figure 4).

(a) CODE LEVEL selector switch (module D)-sets the modules to accept 5-, 6-, 7-, or 8-level operation.

(b) UNITS PER CHARACTER INTERVAL switch (module D)-used to select the bit interval (5 to 16 synchronous, 6 to 16 start-stop).

(c) SIGNAL MODE switch [illegible]

3. OPERATOR MAINTENANCE

3.01 To extend the high speed punch and tape supply shelf, open the upper right hand tape storage door (held in the closed position by a magnetic latch). Pull out straight forward on either (upper or lower) handle on the left-hand tape punch station, a slight pull will release the shelf (also held in place by a magnetic latch) (Figure 5).

3.02 Slide the shelf out to its fully extended locked position. Open the small left-hand tape punch door by releasing the latch at the upper inside left-hand corner.

CAUTION: [illegible]

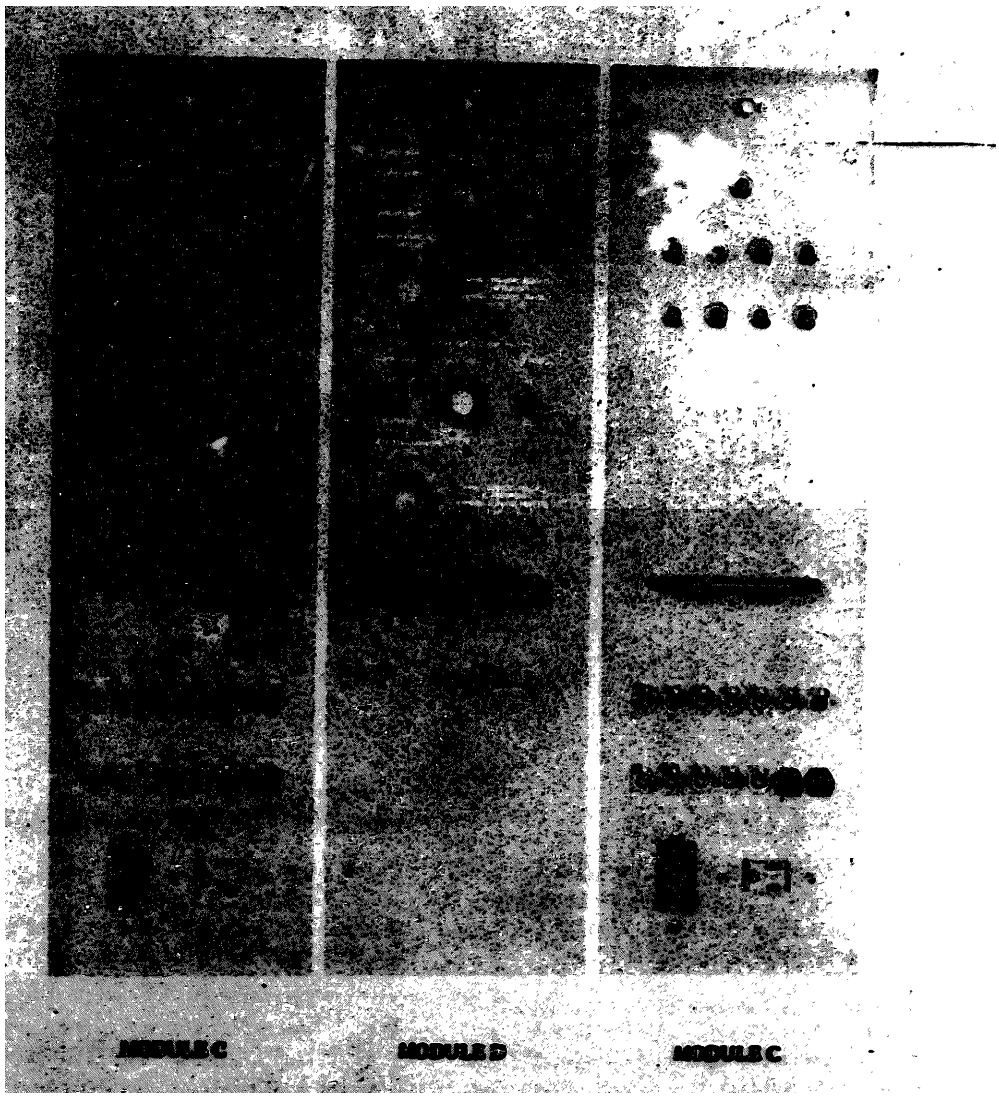


Figure 4-

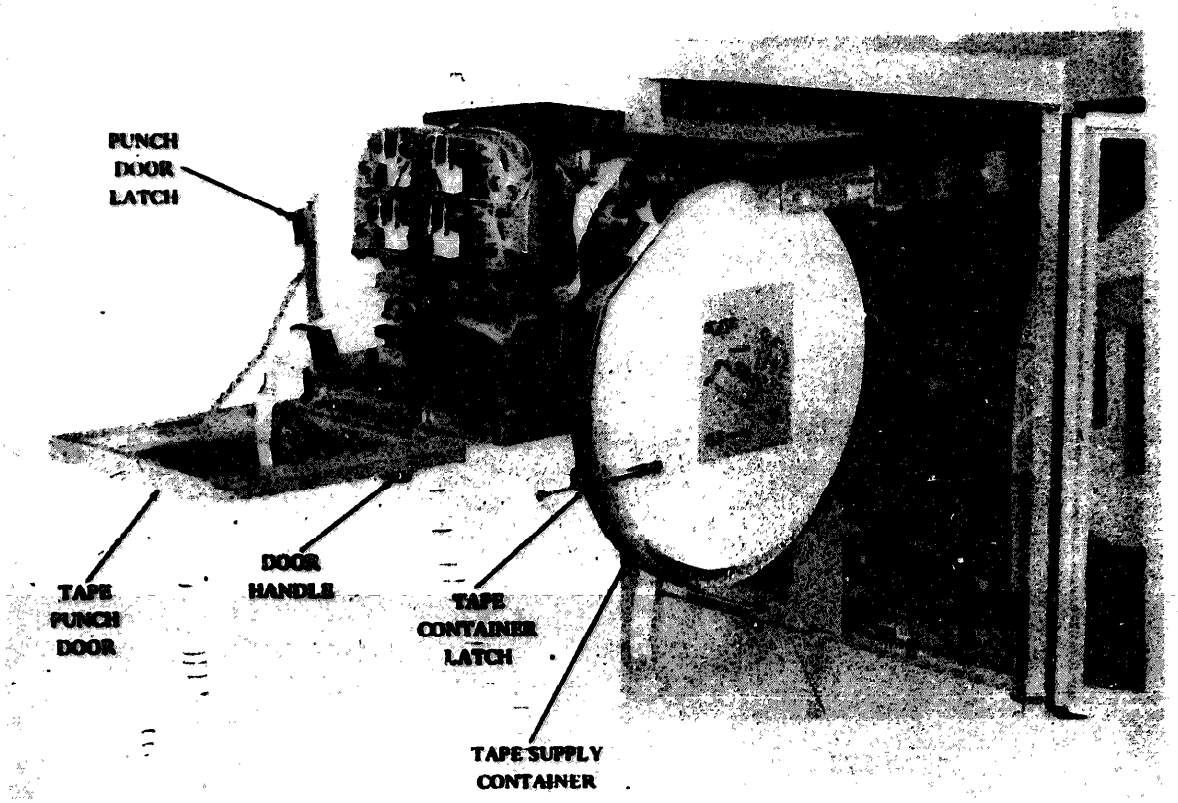


Figure 5- High Speed Punch Shelf

EMPTYING CHAD BIN

3.03 When the CHAD BIN indicator on the control panel lights, the chad bin is full and should be emptied as soon as possible. Slide the appropriate shelf out, in accordance with the procedure in 3.01 and 3.02.

3.04 Remove the end of the chad bag from the end of the chad chute located at the left rear of the shelf. Lift the chad box out of the cradle by its handle. Slide the chad box latch back and open hinged cover. contents can now be easily emptied (Figure 6).

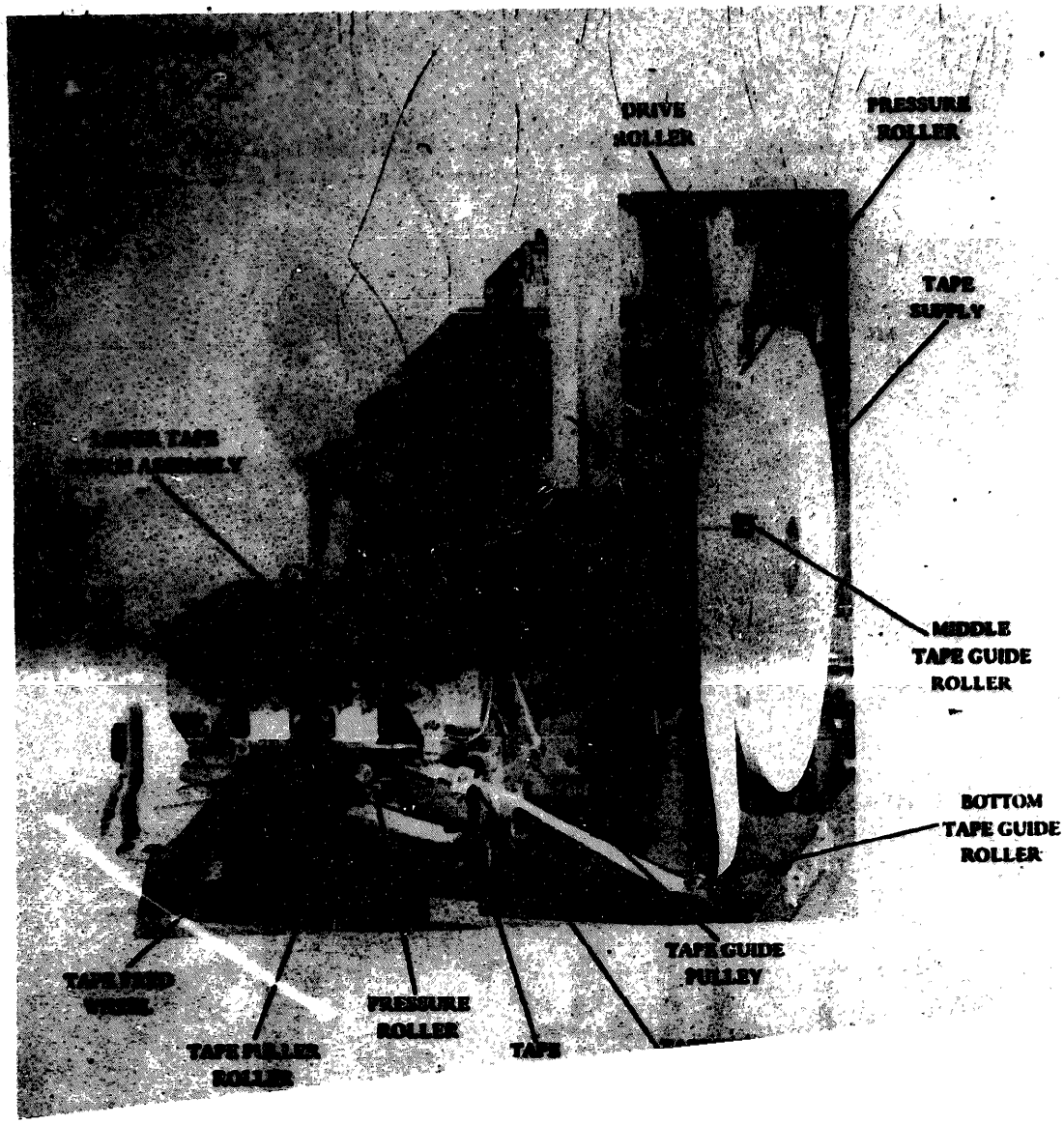
3.05 Replace chad box by reversing the procedure in 3.04, make sure elastic opening of chad bag is securely attached to the chad chute. To slide the shelf back into the cabinet, bring the left-hand tape punch door (upper or lower) up to its locking position. Press the locking latch on the side of each shelf slide and push inward. The shelf can now be pushed back into the cabinet to its closed position.

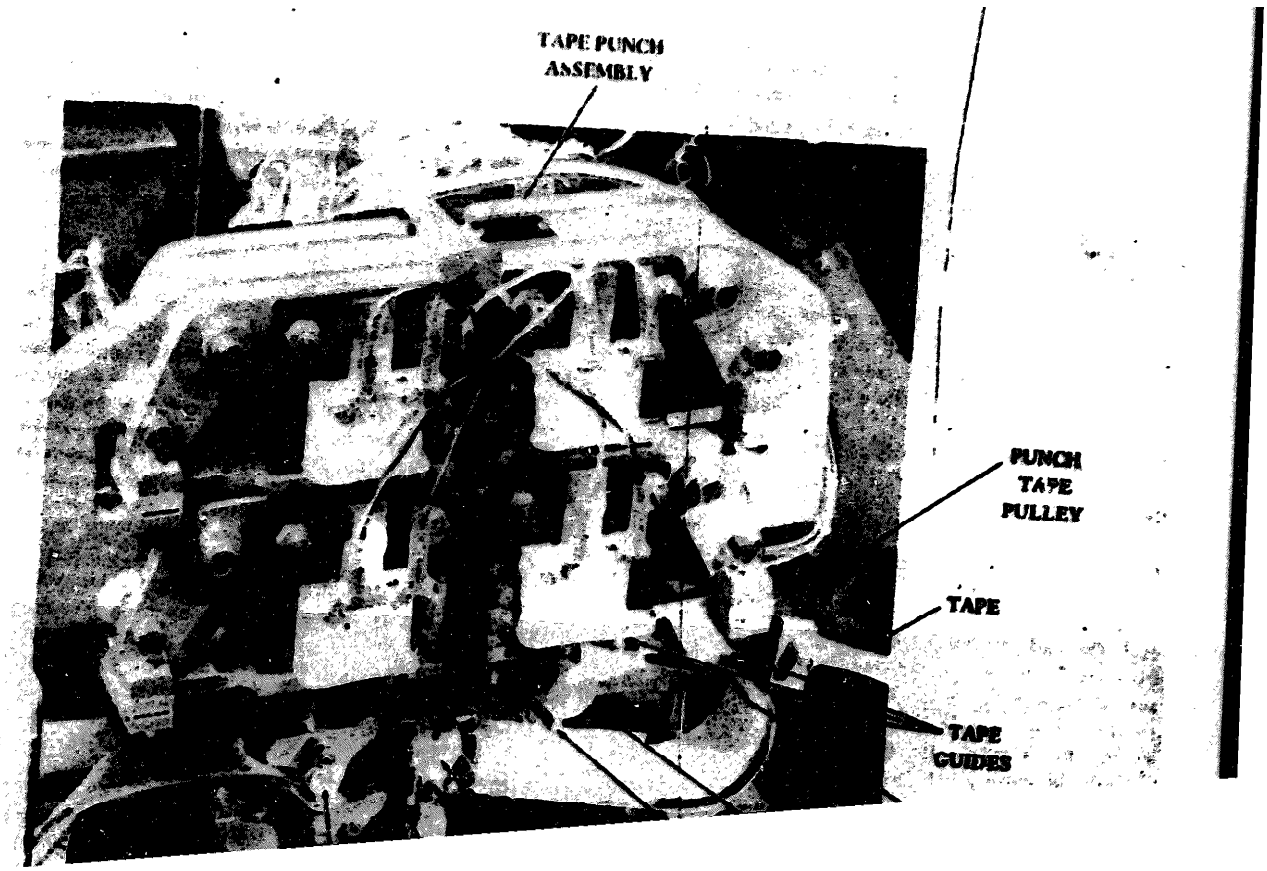
REPLACING TAPE SUPPLY AND THREADING TAPE

3.06 When the LOW TAPE indicator on the control panel lights, the tape supply is empty and should be replaced as soon as possible. Slide the appropriate shelf out, in accordance with the procedure in 3.01 and 3.02.

3.07 Lift the latch at the right front edge of the tape supply container, and swing the door open. Remove the used tape core, and any tape that may still be threaded through the punch (Figure 5).

3.08 Raise the low tape arm (restarting on the used tape core) and place the new tape roll on the tape container hub, with the loose end of the tape at the bottom. Bring the loose end of the tape forward and up, run the tape straight up and out of the tape container at the opening. Run the ape under the tape guide lever and over the driver roller (Figure 7).


DRIVE ROLLER
PRESSURE ROLLER
TAPE SUPPLY
MIDDLE TAPE GUIDE ROLLER
BOTTOM TAPE GUIDE ROLLER
TAPE GUIDE PULLEY
PRESSURE ROLLER
TAPE


TAPE PUNCH
ASSEMBLY
PUNCH
TAPE
PULLEY
TAPE
TAPE
GUIDES

3.12 Then pass the tape to the left along the upper surface of the **tape** guide to pass between the die plate and punch block. All punches must be clear of the tape path in the punch block (reed armatures pulled up), before the new tape can be inserted. The tape is then fed between the tape feed wheel and a manually releasable spring-loaded tape guide directly under the feed wheel. Press down the tape guide handle to facilitate tape insertion under the feed wheel (Figure 9).

3.13 From the feed wheel it arches over, clear of the adjustable guide stop post, then over the tape guide post at the extreme left. The tape chute then makes a half loop around and down to the front tape door slot (Figure 9).

4. THEORY OF OPERATION

GENERAL

4.01 **A detailed** description of each circuit card is included in the drawing covering the card. The number of the drawings is the same as the part number of the card The card part number and drawing number is obtained from the EC number of the card by deleting the prefix EC and adding a prefix of 172 fur EC300 through EC499, 177 for EC500 through EC599, and 303 for EC600 through **EC699.** For example, the drawing number for EC359 is 172359, the drawing number for EC690 is 303690. Terminal board cards **have** the prefix TB, part numbers and drawing numbers for these cards are obtained by deleting TB and adding the prefix 149. For example, the drawing number for TB172 is 149172.

4.02 The equipment voltage levels are of three types:

(a) +6 volts, -6 volts on input and output leads

(b) 0 volt. -6 volts internally

(c) 0 volt, -5 volts on tome internal leads. these ***leads*** are identified by a shaded corner in **the logic** symbol from which they originate.

The dc coupled inputs to logic elements are shown as half arrow heads. Fug arrow heads are reserved for ac coupled (pulse) input

4.03 The most commonly used logic elements is the NOR elements. identified by the designation LA within the logic symbol. The output of this elements IS negative if any input is at 0 volt. The output is ***0*** volt only if all inputs are negative. **A** special input **to** a NOR elements, identified by **an** arrow entering a corner of the symbol, allows the addition of extra logical inputs to the elements. The same results can be obtained by connecting two or more elements together **to** obtain more inputs plus greater load-driving capability.

4.04 The flip-flop element is symbolized by a rectangular box with a diagonal line across the lower half. The operation of this element is similar to that of a standard flip-flop, for example EC671, which contains priming inputs (half arrows) and setting inputs (full arrows). Arrows entering the upper half of the symbol prime 1 inputs, and arrows entering the lower half of the symbol designate prime **0 and set 0 signals.**

4.05 An arrow entering the center of the symbol implies that the set 1 and **set** 0 inputs are connected together. If no printing inputs are shown this indicates that the prime 1 input is connected **to** the inverted output (lower half of symbol). This also indicates the prune 0 input is connected to the normal output (upper half of symbol). A flip-flop connected **this** way is caped a complementing flip-flop or binary counter. Each input pulse reverses the condition of voltages on the normal and inverted outputs.

4.06 A puke amplifier logic elements is identified by a square box with the letters **PA** and a full arrow head input symbol. This element produces a puke of approximately 2 microseconds duration whenever the input goes negative. When both inputs to this elements are used, a pulse is produced only when both inputs are negative.

4.07 A power amplifier element is shown as a trapezoid symbol with the letters PA. This element has two inputs and can perform the NOR function. **It** has about three times the load-driving capability of an ordinary NOR (LA) element.

4.08 The delay elements is symbolized by a square box with the letters DY. This elements can he used as either a one-shot or a free running multivibrator. Those used at one-shot delay elements have the pulse duration **indicated.** Those used as free-running multivibrators have the operating frequency indicated.

4.09 The input elements **translates** the input polar signals (+6 volts and -6 volts) to the neutral **(0** and -6 volt) signals used internally. The output element translates neutral signals to polar signals. The punch driver elements are described in Section **592-803-100TC.**

4.10 The receiver is designed to accept both serial and parallel input signals. Serial signals may he synchronous or start-stop. and may represent 5-, 6-. 7-. or 8-level codes. They may contain from 5 to 16 units (bit times) per character interval. The signals may be received with one or more of the information bus inverted or interchanged in time **sequence.**

4.11 The CODE LEVEL and UNITS PER CHARACTER INTERVAL switches allow selection of the number of code levels to be used and the number of units per *character*. A strapping card controls the selection of bit inversion and bit sequence. When more than 9 units are received per character, the units over nine are ignored by the receiver.

4.12 The interconnecting cable between the receiver and us external signal source contours the following leads

(a) Auxiliary data input (8 leads-parallel)

(b) Auxiliary sample input (parallel)

(c) Data input (serial)

(d) Clock input (serial)

(e) Urgent traffic input

(f) Bit output (8 leads-parallel)

(g) Character available output

(h) Circuit ground, +6 volts and -6 volts

(I) Frame ground

(j) Alarm output (3 leads)

CIRCUIT DESCRIPTION

4.13 A block diagram of the receiver is shown in Figure 10. The counter recognizes character boundaries in incoming serial data by counting the number of units in a character interval. The counter control permits selection of the number of units per character interval and provides for synchronizing the counter with the data. The serial-to-parallel converter stores incoming data bits until a complete character has been received. it includes storage for one character in addition to the character currently being received.

4.14 The punch drive circuits select the data to be punched and control the operation of the punch The tape handling and alarm logic detect trouble, and alarm conditions, such as-low tape, end of tape, tight tape, no tape, and full chad bin. The control panel (Figure 3) contains the various controls used by the operator, and the indicators advise the operator as to the condition of the equipment. The reperforator, power supply, and circuits which distribute ac power to the various components of the set are not shown in Figure 10.

4.15 All indicator lamps in the equipment are controlled by relay contacts or by switches. The controlling contacts are shunted by 150 ohm resistors. These resistors allow a small amount of voltage across the lamp filaments keeping them warm but not enough to allow the lamp to light visibly. This decreases the initial surge of current, which increase the life of the lamps and the controlling contacts.

4.16 All relay windings are shunted by diodes which prevent voltage spikes from being generated when the relays are de-energized. The operator control switches are momentary in action, except BUSY OUT and POWER which are alternate action. push on, push off.

PUNCH DRIVER

4.17 The punch driver mechanisms and electrical components are described in detail in Section 592-803-100TC The operation of the punch driver circuits are described in the following paragraphs Refer to 7730WD, Sheet 4.

4.18 The input stage of a driver element is through a flip-flop. Pin 15 is a priming input and pin 22 is a setting input. Pm 30 corresponds to the inverted output brought out through a diode. The feed level IS controlled by ZC324 so that a feed hole is punched whenever a punch command pulse appears on the common input to pm 22 of all driver cards. A level change occurs on the common pm 30 line when a hole IS punched in any level. including the feed level This level change allows the gated oscillator ZC120 to run

4.19 The first pulse from ZC120 resets all drivers that were set and turns off its own turn-on signal. The circuit remains in this condition until another set pulse arrives The four inputs to the punch driver prunes are, data received serially, data received in parallel. blank feed out character, and feed out characters programmed into the switches on the front of the driver module As levels 1 through 8 operate identically, only level 1 will be described in detail

4.20 The output of ZC316, pm A10 will be 0 volt. conditioning EC323 to punch the l-level. if all inputs to the NOR gate are negative Any positive input to the NOR gate may be viewed as inhibiting punching level 1 The blank feed bus connected to ZC316 pm A6 is negative unless blank feeding is in progress The character feed bus connected to ZC316 pm A5 through switch SWC5 is negative unless character feeding is in progress Opening switch SWC5 has the same effect as if EC316 pin A5 were connected permanently to -6 volts With the SWC5 switch open the character feed bus is unable to inhibit punching

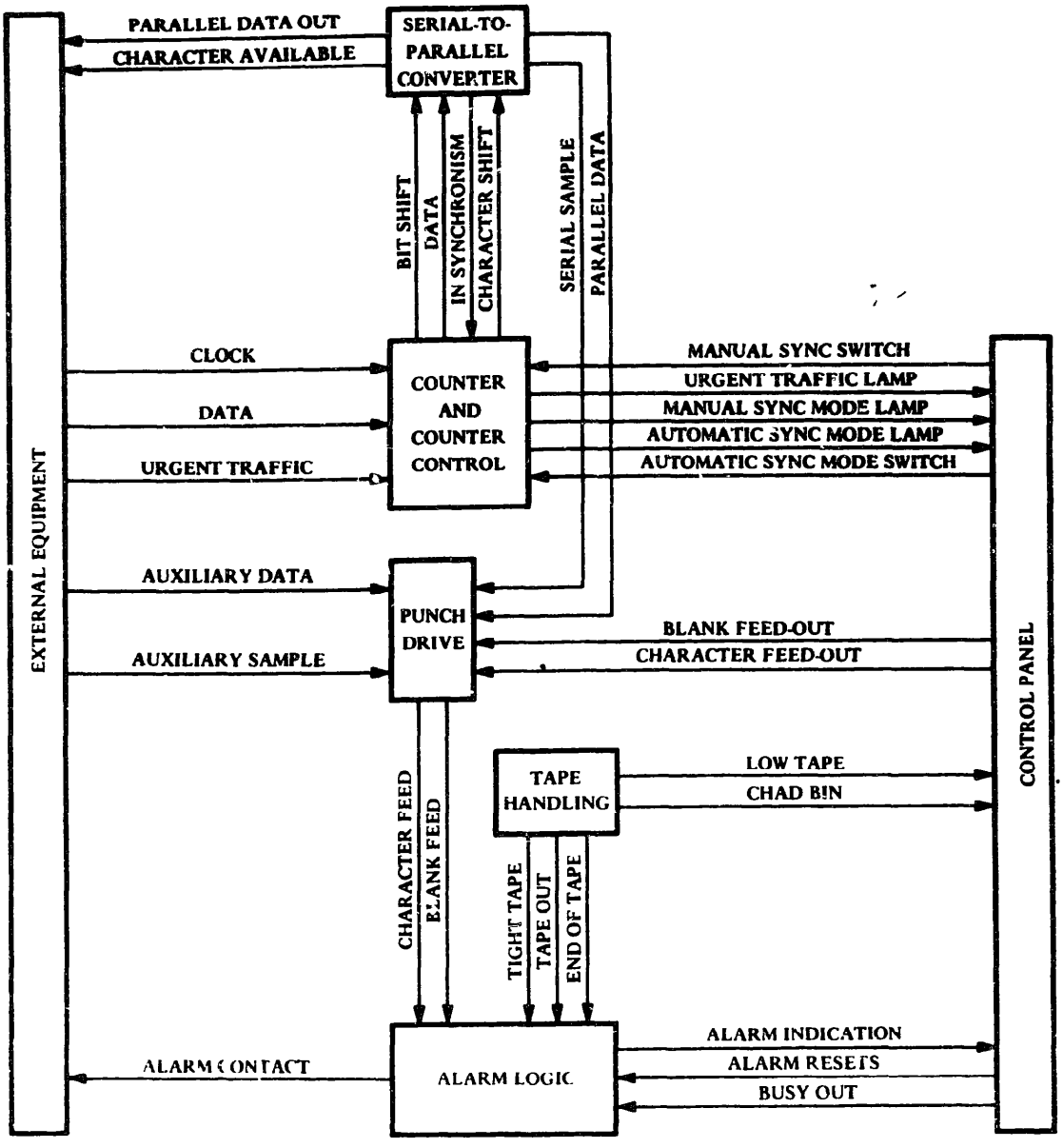


Figure 10- Block Diagram of Receiver

4.21 The receive parallel bus is at 0 volt only when parallel data is received. The receive serial bus is at **0 volt only when serial data is received. When the receive serial bus is at 0 volt and the other three feed busses are negative, ZC316 pin A26 is held negative. At this time ZC316 pin B10 is allowed to go positive if the level 1 input from the receiving distributor storage at JC328 pin C8 is negative, indicating a spacing bit. Therefore, punching in level 1 is inhibited. If the input from the receiving distributor storage is positive, ZC316 pin B10 is held negative so that level 1 is permitted to punch. When the receive parallel bus is at 0 volt and the other three feed busses are negative ZC316 pin B10 is held negative.**

4.22 The output of ZC316 pin A26 goes to 0 volt if the auxiliary bit one input is negative, or to -6 volts if the input is positive. Therefore, punching is controlled by the auxiliary bit input signals. A pulse from ZC120 pin 7 causes a character to be punched, when pin 9 of this element goes positive. When power is first applied, relay K4 of ZC418 does not operate immediately because its winding is with an R-C delay network (7730WD, Sheet 3). Before K4 operates ZC108 pin A12; pin A12 and ZC112 pin A35 (Sheet 4) are held at 0 volt. Therefore ZC112 pin B27 is negative, pin A9 is at 0 volt, and pin A10 is negative.

4.23 A 0 volt on ZC313 pin A9 holds the blank feed bus negative and 0 volt on ZC313 pin B3 holds the character feed bus negative. With 0 volt on ZC112 pin A14. pin A17 is held negative, holding the receive parallel bus at 0 volt. The 0 volt on ZC112 pin B26 holds pin B28 negative, holding the receive serial bus positive. These conditions hold all punch level inhibit sign& off (negative).

4.24 When K4 is operated ZC108 pm B11 (Sheet 3) immediately produces a positive pulse. This acts through diode CR-B of ZC311 to drive ZC120 pin 9 positive, producing a pulse at ZC120 pin 7 punching a **delete** (rub-out) character. This is done because the punch pins may have partially perforated the tape when power was turned off. This would cause the punch to jam if a delete character were not punched over the partial perforations. Because of the inherent delay in the priming circuits, the delete character will be punched even if the punch prune leads go negative when K4 operates.

FEEDOUT CIRCUITS

4.25 With no traffic and K4 operated, ZC120 pm 9 is negative. A circuit consisting of two NOR elements is connected to the BLANK FEED switch (7730WD, Sheet 3), This circuit, sometimes, called a latch, is used frequently in connection with switches to eliminate the effects of contact arcing. With the BLANK FEED switch released, a ground at ZC112 pin B23 holds pins A26 and A23 negative. The open at pin A24 allows pin A27 to go to 0 volt, while holding pin A26 negative. If the ground were removed from pin B23, the outputs of the two NOR gates would he unchanged.

4.26 Operating the BLANK FEED switch, grounds pm A24, while holding pin A27 and pin B22 negative. Pin A26 is at 0 volt with pin B23 open. If the ground were removed from pin A24 the state of the circuit would not change. Pin A26 goes to 0 volt as soon as the switch is operated and remains at that voltage, regardless of the contacts arcing, until the switch is released. The latch circuits composed of ZC112, LA-ID and LA-20 are connected to the CHARACTER FEED switch.

4.27 Operating either the CHARACTER FEED switch or the BLANK FEED switch, holds ZC110 pm B34 negative, allowing the multivibrator (MV-A) of ZC313 to run **at a** frequency of 105 hertz. Square waves from this elements appear inverted at ZC307 pin A9, the 1050 wpm lead. At the same time the blank feed or character feed bus goes positive, because of the negative voltages at both inputs of the selected power amplifier element. The blank feed bus or the character feed bus controls priming of the punch drivers as described in 4.18 through 4.24.

4.28 The character feed bus enters ZC112, pm A13 and pin A34 to hold the receive parallel bus and receive serial bus at 0 volt during character feeding. This prevents parallel and serial input data from reaching the punch and interferring with character feeding. Incoming pubes on the 1050 wpm lead enter at ZC112 pm A5 (Sheet 4). Because all other inputs to this element are negative, the 1050 wpm pulses appear inverted at ZC112 pm A10. These pubes drive the punch drive power amplifier of ZC120 and cause the appropriate characters to be punched at a rate of 1050 per second.

4.29 A thud character feed circuit is controlled by the CHARACTER FEED toggle switch on the front of the appropriate module C punch driver. This switch is connected to a modified version of the latch circuit described in 4.25 Operating the switch causes ZC112 pm B10 to go negative and pm B9 goes to 0 volt This 0 volt from pm B9 drivers ZC307 pm A10 negative, causing the character feed bus (ZC313 pm B1) to go positive. Negative voltage from pm B10 of ZC112 allows the 240 hertz multivibrator (MV-B) of ZC313 to run, producing pulses on the 2400 wpm lead These pubes enter ZC112 pm A7 to cause the punch to operate as described previously.

PARALLEL RECEIVING

4.30 After relay K4 of **ZC418** (7730WD. Sheet 3) has operated **at** the time of power turn-on both inputs to LA-2F of **ZC112** are normally negative. This causes **ZC112** pin B27 to be at 0 volt and pin 9 to be negative. When parallel data is to be received the auxiliary sample lead goes positive, **driving ZC112** pin A9 (the parallel **sample** lead) **positive. This sets** flip-flop **D-B of** ZC311, placing pm B33 at **0** volt. **Pm A17** of ZC112 **is driven negative,** causing the receive parallel bus to go to 0 volt. At the same tune all inputs to **LA-1F** of ZC112 art negative, causing pm B28 to go to 0 volt and holding the receive **serial** bus negative.

4.31 Under these conditions (4.30) the punch drives art pruned from the auxiliary bit input lea& described previously (4.22). When the auxiliary sample lead goes negative ZC112 pm A9 goes negative, allowing ZC112 pin A10 to go to 0 volt. The power amplifier ZC120 then emits a pulse which **causes** the character present on the auxiliary bit leads to be punched. For additional characters the auxiliary sample lead continues to be pulsed, and each negative going transistors causes a character to be punched. When no more characters art to be punched the auxiliary sample lead remains negative.

SERIAL RECEIVING

4.32 Serial data is received and converted to parallel circuits to be described later When a character **is** assembled and ready for punching, a 0 volt pulse appears at ZC112 pin B7 which was negative This pulse ***drives*** ZC112 pin A10 negative and also resets flip-flop D-B of ZC311 With **ZC311** pin B34 **at** 0 **volt and** pin B33 negative, the **receive parallel** bus IS held negative and the receive serial bus IS held at 0 volt.

4.33 The previous conditions prevent parallel data on the auxiliary bit leads from reaching the punch. and allow data from the serial-to-parallel converter circuits to reach the punch. For example, the first bit of a character received received is applied to ZC316 pin B6 and appears inverted at pin B10 because the receive parallel bus IS negative. If the bit in question is marking ZC316 pin B6 will bit at 0 volt, pin B10 will be negative, and pin A10 will be at 0 volt to prune the punch **driver**

4.34 At the end of the serial sample pulse (ZC112 pin **B**7). pin A10 **of** ZC112 will go positive causing the character far which the drivers are pruned to be punched **Further serial sample** pulses cause the punching of an **additional character at** the end of each pulse. When no more characters are to be punched the serial sample pulse lead remains negative.

ALARM CIRCUITS

4.35 The LOW TAPE and END OF TAPE mercury switches are mounted on an arm attached to the tape supply reel holder. The END OF TAPE switch is adjusted to close when the tape supply has been used beyond the point at which the LOW TAPE switch operates. The LOW TAPE switch does nothing more than light the LOW TAPE indicator to advise the operator that the tape supply is used up. The END OF TAPE switch cuts off the associated equipment chat sends messages to the receiver (Figure 11).

4.36 The TAPE OUT switch arm **is** mounted on the tape feed chute of the punch and **close** if there is no cape in the rapt path. The TIGHT TAPE contact is actuated by the punch tape supply tension lever when the tape loop in the punch **because** abnormally short (Figure 9). The CHAD BIN switch **closes** when the chad bin **become** full. as determined by weight (Figure 12). Like the LOW TAPE switch, this switch only lights an indicator when it operates (Figure 3).

4.37 The NOR elements **LA-IA** and **LA-2A** of **ZC110** form a latch circuit. When the END OF TAPE switch **closes ZC110** pm A9 goes negative and pin **A10 goes** to 0 volt. Power amplifier PA-1D of ZC108 operates K4 of ZC318 to light the END OF TAPE lamp. An identical latch circuit involving LA-1B and LA-2B of **ZC110, PA-2C of** ZC108, and K3 of ZC318 controls the TAPE OUT lamp. Both of these latches are reset by **pressing the associated** END OF TAPE/TAPE OUT indicator switch, which causes **ZC110** pins A10 and A17 to go negative.

4.38 A similar latch using LA-1C and LA-2C of ZC110, P4-1C of ZC108, and K2 of ZC318 lights the TIGHT TAPE lamp when **the** TIGHT TAPE switch operates. Tape motion is detected by counting punch drive pulses between operations of the tape puller motor on the punch with an eight stage binary counter. The counter is reset each time the tape puller operates. The tape is not feeding properly if the tape puller does not operate before 161 **or 162** drive pulses have been counted.

4.39 The counter consists of flip-flops D-C. D-D, D-E. and D-F of ZC311 and flip-flops D-B. D-C. D-E, and D-F of ZC309 The counter **IS** reset to zero by applying a positive pulse through **diodes** on the same cards to the inverted outputs of all the flip-flops except D-D in ZC311 When power is first applied **the** power on level signal at ZC313 pin A31 holds the reset bus negative. When K4 of ZC418 operates, both inputs to PA-E of ZC313 are negative. causing this elements to generate a positive pulse at pin A27, resetting the counter flip-flops (7730WD. Sheet 3).

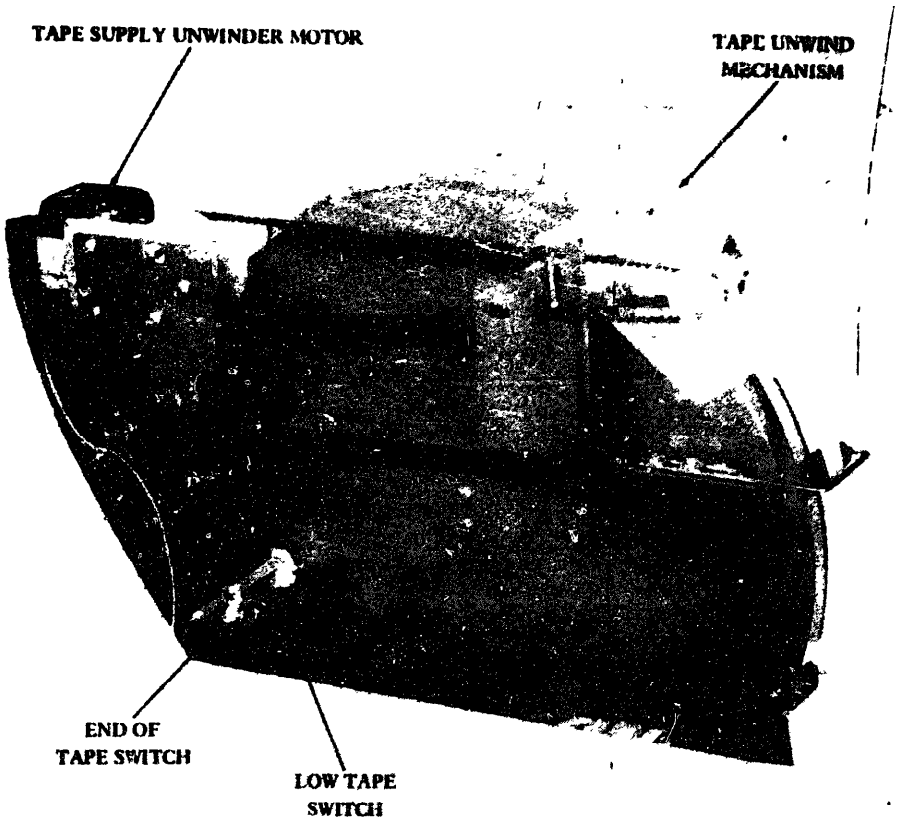


Figure 11- Tape Alarm Switches.

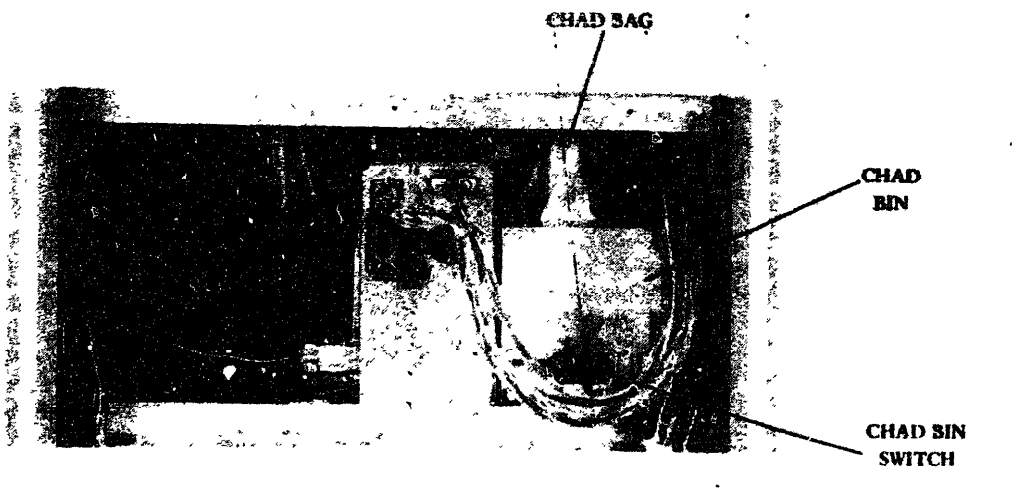


Figure 12- Chad Bin and Switch

4.40 When the tape puller motor operates, 60 hertz ac is applied to pin B13 of ZC307. This causes 60 hertz pulses at pin A11. The NOR elements LA-2B and LA-1C of ZC307 form a latch to store tape puller motor operations, for the negative transition of the punch drive pulse. These cycle the 725 microsecond delay DY-B in ZC108. This resets the above latch and causes PA-E of ZC313 to generate a positive pulse and reset the counter flip-flops.

4.41 This counter reset causes pin A23 of D-D in ZC311 to go to -6 volts. The next drive pulse will place D-D in the set 1 condition. When pin A23 goes to 0 volt flip-flop D-C of ZC311 is set. This action continues down the counter until all flip-flops are set. The first drive pulse sets the counter to a full count of 255. The next drive pulse resets flip-flop D-D of ZC311 so that the counter holds a count of 254. These counts are determined by assigning values to the counter stages from left to right, 1, 2, 4, 8, 16, 32, 64, and 128. The count in the counter is determined by adding the values of all flip-flops that are set. The next drive pulse sets the first flip-flop again.

4.42 When pin A32 of ZC311 goes to 0 volt, flip-flop D-E of ZC311 is reset, so the count is 253. In the same manner the following pulses decrease the count in the counter by on for each pulse. After 160 pulse the counter will contain a count of 96, with flip-flop D-C and D-E of ZC309 set and all others reset. The next drive pulse sets flip-flop D-C of ZC311, and sets flip-slop D-E which sets flip-flop D-F. This sets slip-flop D-B of ZC309 which resets flip-flop D-C, and resets D-C and D-F of ZC309 which sets D-E. This causes all inputs to LA-1B of ZC307 to be negative, allowing pin A17 to go positive.

4.43 The negative edge of the next drive pulse then resets flip-flop D-D of ZC309. This operates relay K1 on ZC418 to light the TAPE FEED indicator. The tape puller motor normally operates more often than every 161 characters (as mentioned in 4.38). The counter is normally reset before a count of 95 is reached and flip-flop D-D of ZC309 is reset. Pressing the indicator associated with the TIGHT TAPE/TAPE FEED switch resets the TIGHT TAPE latch if it was set, or sets the TAPE FEED flip-flop D-D of ZC309. if it was reset.

4.44 This latter action (described in 4.43) stats with the switch in its normal position, ZC307 pin B27 at 0 volt and pin B9 is negative. When the switch is operated B9 goes positive to set the flip-flop. The time delay associated with the prime input allows the flip-flop to be set even though the prime input goes negative at the same time the set input goes to 0 volt. The NOR elements LA-1E and LA-1F of ZC110 are connected together to form a seven input gate.

4.45 Normally all inputs are negative, allowing pin B28 to go to 0 volt. This holds pin B9 at a negative voltage, causing the power amplifier to operate relay KC119A. A 0 volt signal at any input of the seven input gate will release the relay to indicate an alarm condition to the associated equipment.

4.46 An alarm condition is also indicated if power to the receiver is turned off, since relay KC119A is also released as a result. The inputs to the seven input gate are BLANK FEED, CHARACTER FEED, BUSY OUT (operator switch), END OF TAPE, TAPE OUT, TIGHT TAPE, and FEED. The BUSY OUT switch is a push-on, push-off operator control, allowing the operator to remove the receiver from service. The indicator lamps for the BUSY OUT, BLANK FEED, and CHARACTER FEED indicator switch are also shown on 7730WD Sheet 2.

SERIAL-TO-PARALLEL CONVERTER

4.47 Normal and inverted serial data are applied to section B and C of the CODE LEVEL switch, respectively (Figure 4). If the switch is in the 8-level position, there signal are applied as primes to elements D-B of ZD509. The outputs of this element are inverted by elements LA-1A and LA-1B of ZD507 and applied as primes to elements D-C of ZD509. Similarly element D-D of ZD509 is primed from the inverted outputs of element D-C, and element D-E primed from the inverted outputs of D-D (7730WD, sheet 7 and Sheet 8).

4.48 Elements D-B, DC, D-E, D-F, and D-D of ZD513 are primed from the preceding elements. The group of flip-flops is arranged as a nine elements shift register. When the CODE LEVEL switch is set to the 7-level position a ground is applied to pin A7 and pin A13 of ZD507 to allow the output of both LA-1A and LA-1B to go negative. The outputs of these elements, which are the primes of elements D-C, ZD509, are connected to the normal and inverted serial leads through sections B and C of the CODE LEVEL witch. One or the other of the serial data leads will be held at 0 volt by the data. Therefore, elements D-B of ZD509 is effectively eliminated from the shift register.

4.49 When the CODE LEVEL switch is set to the 6-level position the ground on A7 and A13 of ZD507 is maintained through diode CR-B of ZD507. A ground is applied to pin A24 and pin A31 of ZD507. At the same time the normal and inverted serial data leads are moved to prime D-D of ZD509, which eliminates D-B and D-C from shifting action. In a similar manner element D-D is eliminated from shifting action when the CODE LEVEL switch is in the 5-level position. The number of active elements in the shift register is always one greater than the number of levels indicated by the CODE LEVEL switch setting.

4.50 An additional element is used to hold the start bit in start-stop operation. Each shift register element except the start element primes a storage flip-flop. For example, elements D-B of ZD509 primes elements D-B of ZD511. In normal operation data is continuously shifted though the shift register without regard to character boundaries. The synchronizing logic (to be described in 4.73 through 4.78). keeps track of character boundaries, and sets the shift register contents into the storage flip-flop when a complete character is properly positioned in the shift register.

4.51 Normal and inverted storage flip-flop outputs enter the patching circuit card ZD517. This card allows the output circuits to be connected to the data storage flip-flop in any order, and with either normal or inverted polarity. The NOR and INV markings on the terminals of ZD517 (TB243) **appear to be backwards** with respect to the storage flip-flop output. this is done because the signals will be inverted in NOR gates before being presented to the punch driver and output amplifiers. The LEVEL markings on ZD517 correspond to punch levels and have no relation to the order in which bits are received.

4.52 The outputs from AD517 for levels 2 through 6 pass through inverts to the punch drive logic, after inversion through output elements to the associated equipment. The R-C networks provided in these output leads are wed to prevent fast rise time pulses from leaving the receiver, as an RF noise reduction measure.

4.53 The outputs from ZD517 for levels 1, 7, and 8 are pasted through **NOR** gates controlled by the CODE LEVEL switch. For example, level 8 is applied to input B13 of ZD518. Elements LA-2A and LA-2B of this card arc connected together to provide signal isolation and increased lead driving capability, the outputs of these two elements are identical. with the CODE LEVEL switch in the 8 level position these elements act as a simple inverter. In the 5, 6, or 7 level position a pound is applied to input B12 of these elements, holding the outputs negative.

UNITS COUNTER

4.54 The units counter determines when a complete character is in the shift register by counting clock pulses. To perform this function the units counter must be properly aligned with respect to character boundaries; it must start counting at the first bit of a character and stop at the last bit, and then reset to the staring position (Sheet 6).

4.55 The synchronizing circuits which align the counter with character boundaries will be described in 4.79 through 4.85. For the present discussion it will be assumed that the counter is properly aligned.. In the SYNCHRONOUS operation all received bits are data bits in the START-STOP operation a character is always preceded by a start unit and may or may not be followed by one or more stop units. In either case clock pukes are supplied continuously, so that a stop element must contain an integral number of units.

4.56 The SIGNAL MODE switch selects SYNCHRONOUS or START-STOP operation. The CHAR. SYNC. switch in the OFF position allows reception of characters which always contain **a** specified number of units. In the ON position the receiver can accept characters having stop elements containing an unspecified number of units. The SIGNAL MODE switch is equipped with a latching circuit. The NOR elements ZD303 pin A9 is at 0 volt and pin A11 is negative in the START-STOP position. There conditions are reversed in the SYNCHRONOUS position.

4.57 The counter is composed of flip-flops D-B, D-C. D-D, and DE of ZD503 In synchronous operation the staring position of the counter IS the element D-B, which is reset while the other elements are set (Sheet 6, the semicircular symbols with the letter D, are additional Prime and set inputs for the flip-flop.)

4.58 The counter is placed in this position by the last character shift pulse This resets element D-B directly and fires the 100 microsecond one-shot DY-B pulse of ZD305 to pull counter elements PC. D-D, and D-E into the set condition. In the staring position of the START-STOP operation of thee counter all flip-flops are set With the counter placed in the condition just described, the element D-B, IS pruned to be set rather than reset

A. Synchronous Operations, 5 Units Per Character

4.59 The output at pm A10 of ZD303 is held negative by the 0 volt input at pm A6. With the synchronous prune signal also negative. the inverted clock pulses are reinverted by LA-1B of ZD303 This causes counter element D-B to be driven by normal clock pulses The positive-to-negative clock transition occurs in the center of a data bit The negative-to-positive transition occurs at the time of data transitions Therefore. the counter **IS** advanced at the time of data transitions

4.60 The first clock pulse sets counter element D-B As pm B34 of this clement goes negative pm A26 of ZD303 goes positive to reset element DC The next clock pulse resets element D-B The third clock pulse sets D-B, which sets DC. and resets D D The fourth clock pulse resets D-B The fifth clock pulse sets D-B which resets DC Table A summarizes the action

TABLE A

FLIP-FLOP OPERATION, 5 UNITS PER CHARACTER

CLOCK PULSE	D-B	D-C	D-D	D-E
0	Reset	Set	Set	Set
1	Set	Reset	Set	Set
2	Reset	Reset	Set	Set
3	Set	Set	Reset	Set
4	Reset	Set	Reset	Set
5	Set	Reset	Reset	Set

4.61 After the fourth clock pulse, and the UNITS PER CHARACTER INTERVAL switch set at 5 (SYNCHRONOUS), all inputs to element LA-1C of ZD303 were negative allowing the output to go to 0 volt. After the fifth clock pulse, pin A27 of ZD303 goes negative. This causes PA-E of ZD305 to emit a pulse. which triggers DY-B of ZD305. These two signals reset the counter to the condition mentioned above for clock pulse 0.

4.62 The pulse from pm A27 of ZD305 is the character shift pulse. and sets the shift register contents into the storage flip-flops. The pulse from DY-B of ZD305 is inverted by element LA-2A of ZD520. The resulting signal goes positive 100 microseconds after the clock pulse which caused the counter to be reset. Pm A21, LA-1F of ZD518 is at 0 volt in synchronous operation (Sheet 8). Therefore. pin B28 of ZD518 is negative and pin B27 of ZD320 is at 0 volt, pruning the 2 millisecond one-shot DY-B of ZD305. This is triggered by the character shift pulse.

4.63 The normal output of the one-shot is made available to external equipment. The one-shot output is inverted by LA-IF of ZD520 to form the sample pulse for the punch driver. This pulse enters pm B7 of ZC112 and causes the character in the storage flip-flops to be punched (Sheet 4). The timing diagram in Figure 13 is of the counter operations described in the preceding paragraphs. To relate the description to the figure, the first clock pulse is represented in Figure 13 as the positive going clock transition following the number 1 data puke, the second clock pulse follows the number 2 data pulse, and so on.

B. Synchronous Operation, 10 Units Per Character

4.64 **This mode of operation is the same as described in the previous paragraphs, except that more clock** pulses are received before LA-1C of ZD303 detects the completion of a character (Figure 14). Table B shows the various flip-flop states, the first six are the same as those given previously.

C. Start-Stop Operation, 6 Units Per Character, 5-Level

4.65 In this mode of operation the 5 bits of a character are preceded by a start pulse. With the SIGNAL MODE switch in the START-STOP position pin A9 of ZD303 is at 0 volt, pin A11 is negative. This removes the reset prime from counter element D-B, and applies a set prime, so that the starting position the counter is that in which all flip-flops are set.

4.66 With the CHAR. SYNC. switch in the OFF position, the established synchronous operation proceeds as described in the 5 unit synchronous operation, except for the staring position of the counter and the method of obtaining the punch sample pulse. Table C shows the various counter states.

4.67 As compared with synchronous operation one additional clock pulse is received before the character shift signal is generated and the counter is reset. Referring to 7730WD. Sheet 8, input A21 of LA-1F, ZD518 is negative in START-STOP operation. When the start pulse is in element D-D of ZD513 input A34 of LA-1F, ZD518 goes to 0 volt because of appropriate strapping on ZD517. This causes pin B27 of ZD520 to go to 0 volt, and primes DY-A of ZD305 to generate the sample pulse as before when the character shift pulse arrives. The timing diagram for this mode of operation is shown in Figure 15.

D. Start-Stop Operation, 7 Units Per Character, 5-Level

4.68 If the data information consisted of a start pulse followed by 6 data bits, then operation is the same as described preciously. With the exception that this setting of the UNITS PER CHARACTER INTERVAL switch causes the counter to count one additional pulse before generating the character shift signal. An exceptional case is that in which the start pulse is always spacing and the 5 data bits are followed by a stop pulse which is always marking. In this case the CHAR. SYNC. switch may be operated **to the ON** positions, permitting receipt of characters in which the stop pulse may have a duration of an indefinite number of units.

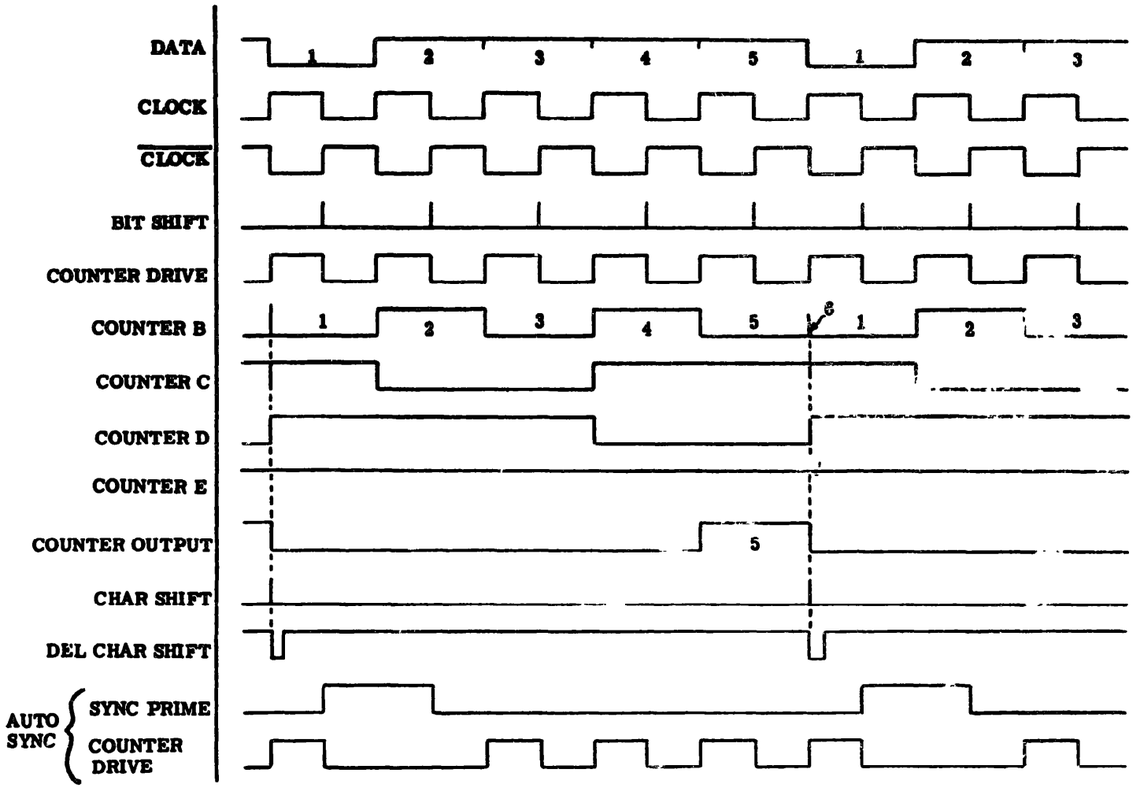


Figure 13- RD Logic for 5 Units, 5-Level Synchronize Operations

TABLE B

FLIP-FLOP OPERATION, 10 UNITS PER CHARACTER

CLOCK PULSE	D-B	D-C	D-D	D-E	REMARKS
0	Reset	Set	Set	Set	
1	Set	Reset	Set	Set	
2	Reset	Reset	Set	Set	
3	Set	Set	Reset	Set	
4	Reset	Set	Reset	Set	
5	Set	Reset	Reset	Set	
6	Reset	Reset	Reset	Set	
7	Set	Set	Set	Reset	
8	Reset	Set	Set	Reset	
9	Set	Reset	Set	Reset	ZD303 pin A27 to 0 volt.
10	Reset	Reset	Set	Reset	Reset to clock pulse 0.

TABLE C

FLIP-FLOP OPERATION, 5 UNITS PER CHARACTER

CLOCK PULSE	D-B	D-C	D-D	D-E	REMARKS
0	Set	Set	Set	Set	
1	Reset	Set	Set	Set	
2	Set	Reset	Set	Set	
3	Reset	Reset	Set	Set	
4	Set	Set	Reset	Set	
5	Reset	Set	Reset	Set	ZD303 pin A27 to 0 volts.
6	Set	Reset	Reset	Set	Reset to clock pulse 0.

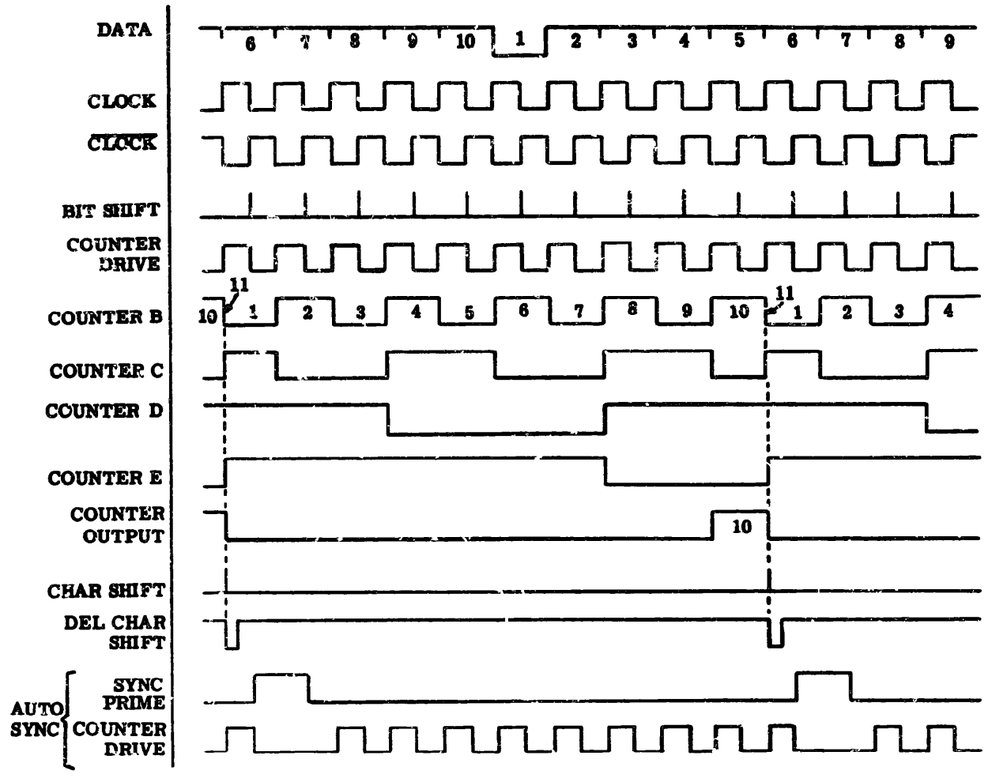


Figure 14- RD Logic for 10 Units, 5-Level Synchronize Operation

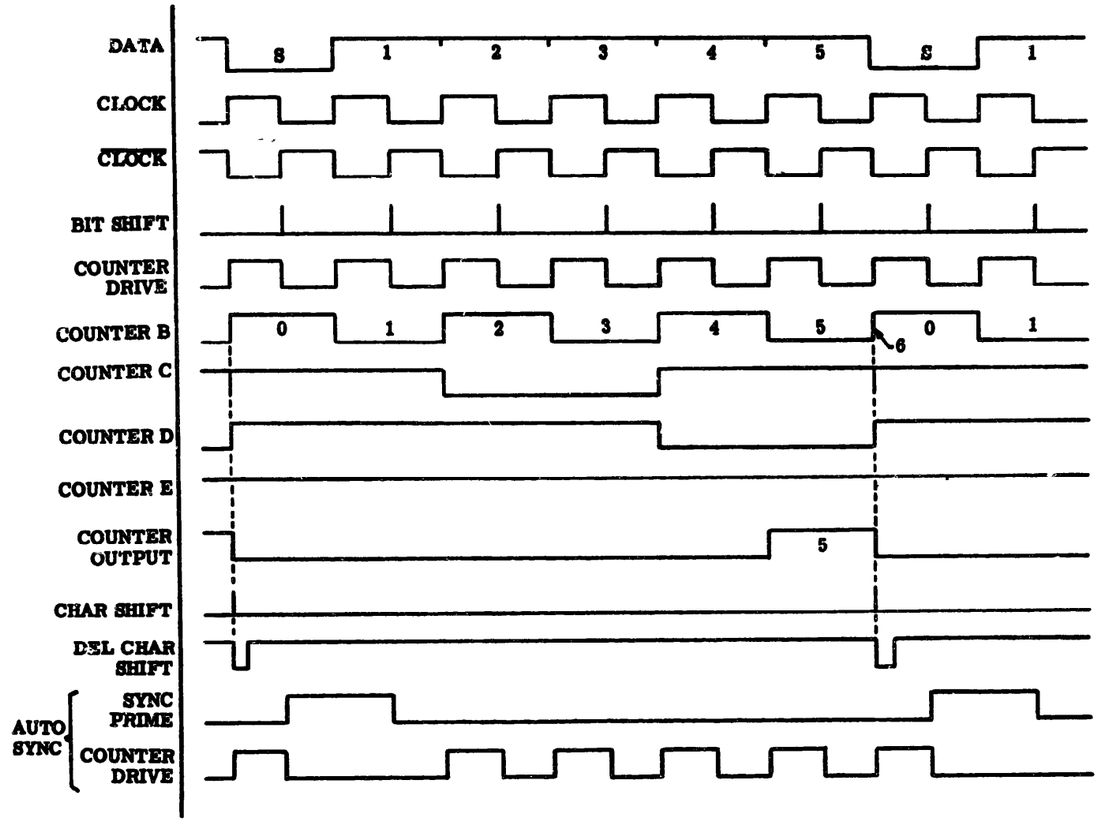


Figure 15- RD Logic for 6 Units, 5-Level (Start-Stop)

4.69 In this mode of operation the character synchronous prime signal controls the output of LA-1A, ZD303. When the character synchronous prime signal is 0 volt, pin A10 of ZD303 is negative as before and clock pulses reach the counter. When the character synchronous prime signal is negative pin A10 of ZD303 goes to 0 volt. This holds pin A17 of ZD303 negative at all times so that clock pulses cannot reach the counter. The character synchronous prime signal is controlled by flip-flops D-B and D-C of ZD505. During receipt of a character both of these elements are set, so that the character synchronous prime lead is at 0 volt (Sheet 5).

4.70 When the complete character had been received and transferred into the storage flip-flops, the delayed character shift signal resets element D-B. This occurs 100 microseconds after the beginning of the stop pulse. The next bit shift (clock) pulse resets elements D-C in the center of the first unit of the stop pulse. With element D-B reset no further clock pulses are counted, so the counter remains in the state corresponding to a nuder 0 clock pulse.

4.71 No change takes place in the circuit, as long as the incoming data lead remains marking. When the incoming data lead goes spacing, pin A26 of ZD507 goes positive to set element D-B. This allows clock pukes to reach the counter, the first clock pulse also sets element D-C. This element is necessary to delay pruning element D-B for one half unit of time, because a slow rise time data input could otherwise cause D-B to be set falsely.

4.72 The timing diagram for this mode of operation is shown in Figure 16. The timing diagram for the 10 unit 5 level start-stop operation is shown in Figure 17, which is the same as that just described except for the different setting of the UNITS PER CHARACTER INTERVAL switch and the greater number of pulses counted.

E. Synchronization

4.73 In the preceding paragraphs it has been assumed that the receiver is properly synchronized, meaning, the counter is reset between characters. It is possible for the receiver not to be synchronized resulting in the character shift pulses not coinciding with character boundaries. This causes each punched character to contain some bits from one data character and some bits from the adjacent character. The circuits to be described perform the function of placing the receiver in synchronism.

4.74 The usual method of synchronizing is suppressing clock pulses from reaching the counter. This is the function of the synchronous prime lead. The 0 volt on this lead holds ZD303 pin A17 negative so that clock pulses are not counted (Sheet 6). A negative voltage on this lead allows the pukes to be counted normally. During synchronizing one clock pulse is deleted during each character interval. This causes the counter to fall behind the data stream. The synchronizing action should stop when the counter falls into the correct position with respect to the data.

4.75 Synchromizm cannot be achieved if any or all of the following conditions are present:

(a) If the UNITS PER CHARACTER INTERVAL switch is not set correctly for the data being received.

(b) If the SIGNAL MODE switch is not set to its proper position.

(c) If the CHAR. SYNC. switch is turned ON when the data stream does not contain proper start-stop pulses.

4.76 with miscellaneous signals being received it is impossible for the receiver to determine whether it is in or out of synchronism. Operating the MANUAL SYNC. indicator switch allows the operator to slip the counter. This process an k repeated until the data being punched appears to k reasonable, as determined by inspecting the tape. The counter slips one position for each operation of the MANUAL SYNC. indicator switch.

4.77 The automatic synchronizing mode causes the receiver to search for a predetermined idle character pattern in the received data. Whenever this character is being received a search for synchronism can be initiated by pressing the AUTOMATIC/MANUAL SYNC MODE indicator switch, unless the receiver is already in synchronism. The AUTOMATIC/MANUAL SYNC MODE switch controls whichever mode is to be used by controlling flip-flop D-D of ZD505. This flip-flop is set for the automatic mode and reset for the manual mode.

4.78 In the automatic mode a negative ***voltage*** at pin B22 of ZD505 causes relay K1 of ZD526 to be operated by PA-1D of ZD305. In the manual mode ***a*** negative voltage at pin A23 of ZD505 causes PA-2D of ZD305 to operate relay K2 of ZD526. These relays operate the AUTOMATIC SYNC MODE and MANUAL SYNC MODE indicators, respectively. The AUTOMATIC/MANUAL SYNC MODE switch operates a latch composed of LA-1D and LA-1E of ZD303. Pin B10 of ZD303 goes to 0 volt when the switch is operated. and pin B34 of ZD303 goes to 0 volt when the switch is released.

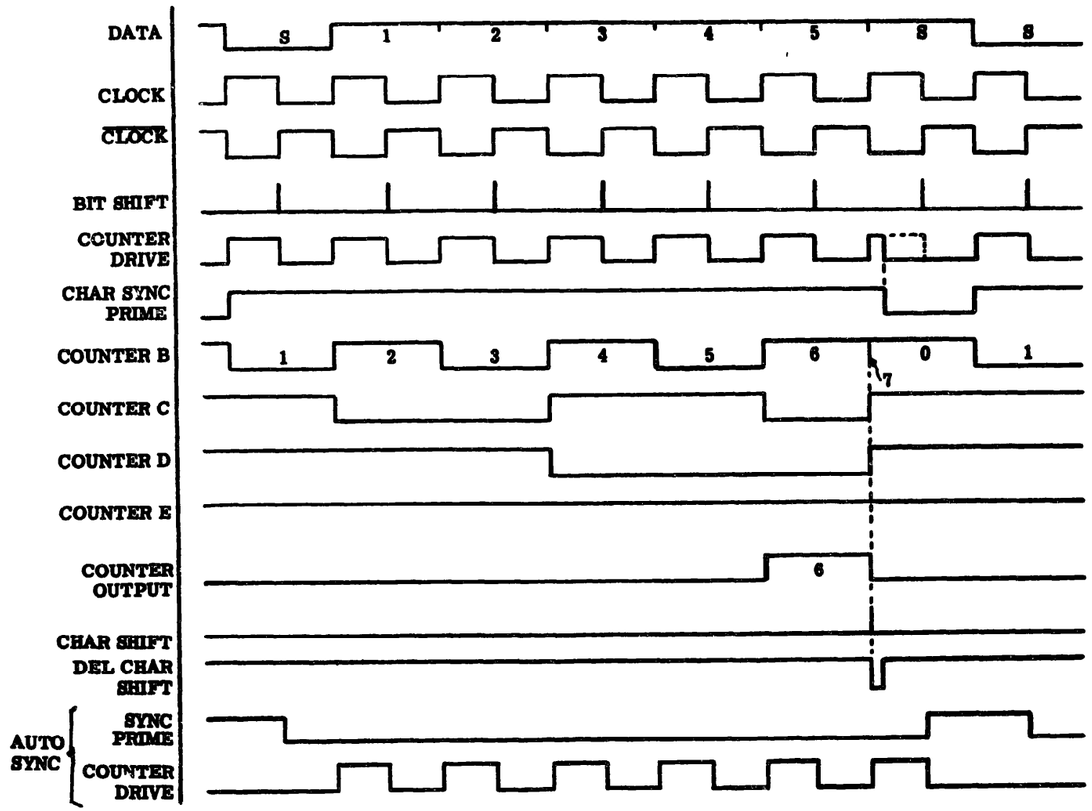


Figure 16- RD Logic for 7 Units, 5-Level (Start-Stop)

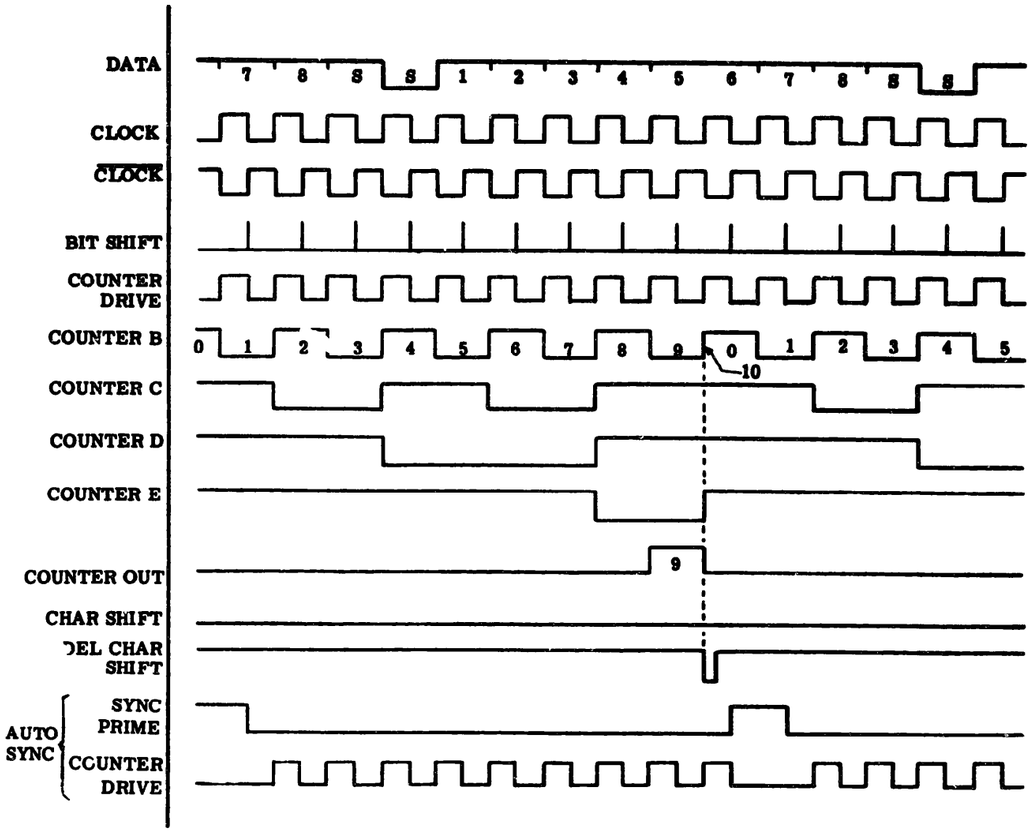


Figure 17- RD Logic for 10 Units, 5-Level (Start-Stop)

Automatic Synchronism

4.79 The output of LA-1A, ZD520 is 0 volt when the receiver detects the idle character (Sheet 7). This occurs when all inputs to this NOR element are negative. The outputs of ZD517 indicate negative voltage marking signals. Inputs A7, A6, and B7 of LA-1A are connected to code levels 6, 5, and 4 respectively. Diodes CR-E and CR-F of ZD515 form two additional inputs to the gate for bits 3 and 2, respectively (Sheet 8).

4.80 Elements LA-2C, LA-2D, and LA-2E of ZD520 have their outputs connected in parallel. If any of these gates have both inputs negative, input A5 of LA-1A, ZD520, will be held at 0 volt. Therefore, the in synchronous lead will go to 0 volt, only if levels 2 through 6 after passing through ZD517 are marking, and if each of the gates LA-2C, LA-2D, and LA-2E of ZD520 have at least one input at 0 volt. The latter condition is satisfied if the levels in use, out of group 1, 7, and 8 are marking and the CODE LEVEL switch is set correctly for the number of levels in use. For example, with 7-level operation, the CODE LEVEL switch grounds input B23 of LA-2C so the condition of the eighth level flip-flop is immaterial.

4.81 The elements LA-2D and LA-2E do not have their inputs (B30 and A1) grounded by the CODE LEVEL switch. Therefore, inputs B31 and B1 must be at 0 volt, which is the marking condition, for the in synchronous lead to go to 0 volt. This causes pin A11 of LA-2B, ZD520 to be held negative and prevents flip-flop D-D of ZD505 from being set (Sheet 5). With the preceding conditions available, pin A11 of ZD520 goes to 0 volt to prime flip-flop D-D to be set.

4.82 Operating the AUTOMATIC/MANUAL SYNC MODE switch once, causes B10 of ZD303 to go to 0 volt, setting flip-flop D-D. This primes flip-flop D-E, which is set by the next delayed character shift pulse, at the positive going transition. This causes pin B10 of flip-flop D-E to go to a negative voltage. If the synchronous prime signal is negative pin B27 of LA-2F, ZD507 goes to 0 volt priming flip-flop D-F. The next bit shift pulse sets flip-flop D-F which primes itself to be reset and holds the synchronous prime lead at 0 volt to prevent the next clock pulse from being counted.

4.83 The next bit shift pulse resets element D-F, which then allows clock pulses to reach the counter. When the synchronous prime lead goes negative pin B3 of D-F goes to 0 volt, resetting flip-flop D-E. Therefore, one clock pulse has been inhibited from reaching the counter. If the receiver is still not synchronized, the next delayed character shift sets flip-flop D-E again, causing another pulse to be dropped.

4.84 When synchronism is achieved the in synchronous lead goes to 0 volt on the positive edge of the character shift pulse. This and the inverted character shift, reset flip-flop D-D through the auxiliary input gate. This removes the set prime from flip-flop D-E before the delayed character shift pulse arrives. Therefore, flip-flop D-E is not set and further clock pulses are prevented from reaching the counter by this circuit.

4.85 If synchronism cannot be achieved because there are no characters in the data stream the operator can press the AUTOMATIC/MANUAL SYNC MODE switch again. As flip-flop D-D primed itself to be reset, it removed its set prime as it was set, and will reset when the switch is operated. The operator can then try to achieve synchronism with the manual procedure.

Manual Synchronism

4.86 The MANUAL SYNC indicator switch drives a latch composed of LA-1F and LA-2F of ZD303, pin B27 of ZD303 goes to 0 volt when the switch is operated. With flip-flop D-D of ZD505 reset, the auxiliary setting gate of flip-flop D-E is primed. Operating the MANUAL SYNC switch, sets flip-flop D-E, causing a clock pulse to be inhibited from reaching the counter as described previously for automatic synchronizing.

4.87 Because of the ac coupled auxiliary setting gate is is necessary to operate the MANUAL SYNC switch once for each clock pulse to be slipped. Operating this switch the number of times equal to the UNITS PER CHARACTER INTERVAL switch setting, will slip the counter around to its original position. Therefore, to bring the receiver into synchronism, the switch should be operated only the number of times indicated by the UNITS PER CHARACTER INTERVAL switch.

URGENT TRAFFIC

4.88 Urgent traffic, detected by the associated equipment requires immediate operator attention. When urgent traffic is received the associated equipment drives the urgent traffic input lead positive. Inverters LA-1D, and LA-1E of ZD520, insure a sufficiently fast rise time to set flip-flop D-D of ZD515. This causes pin B22 to go to a negative voltage activating PA-2C of ZD305 which operates relay K3 of ZD526. This relay lights the URGENT TRAFFIC indicator (Sheet 5).

4.89 The URGENT TRAFFIC switch drives a latch composed of LA-1B and LA-1C of ZD520. Normally pin A27 is negative and pin A17 is at 0 volt. This primes flip-flop D-D to be reset. Operating the switch causes pin A27 of ZD520 to go to 0 volt, resetting flip-flop D-D and turning off the URGENT TRAFFIC indicator. The time delay, associated with the priming action allows flip-flop D-D to be reset, as the prime input goes negative the reset input goes to 0 volt.

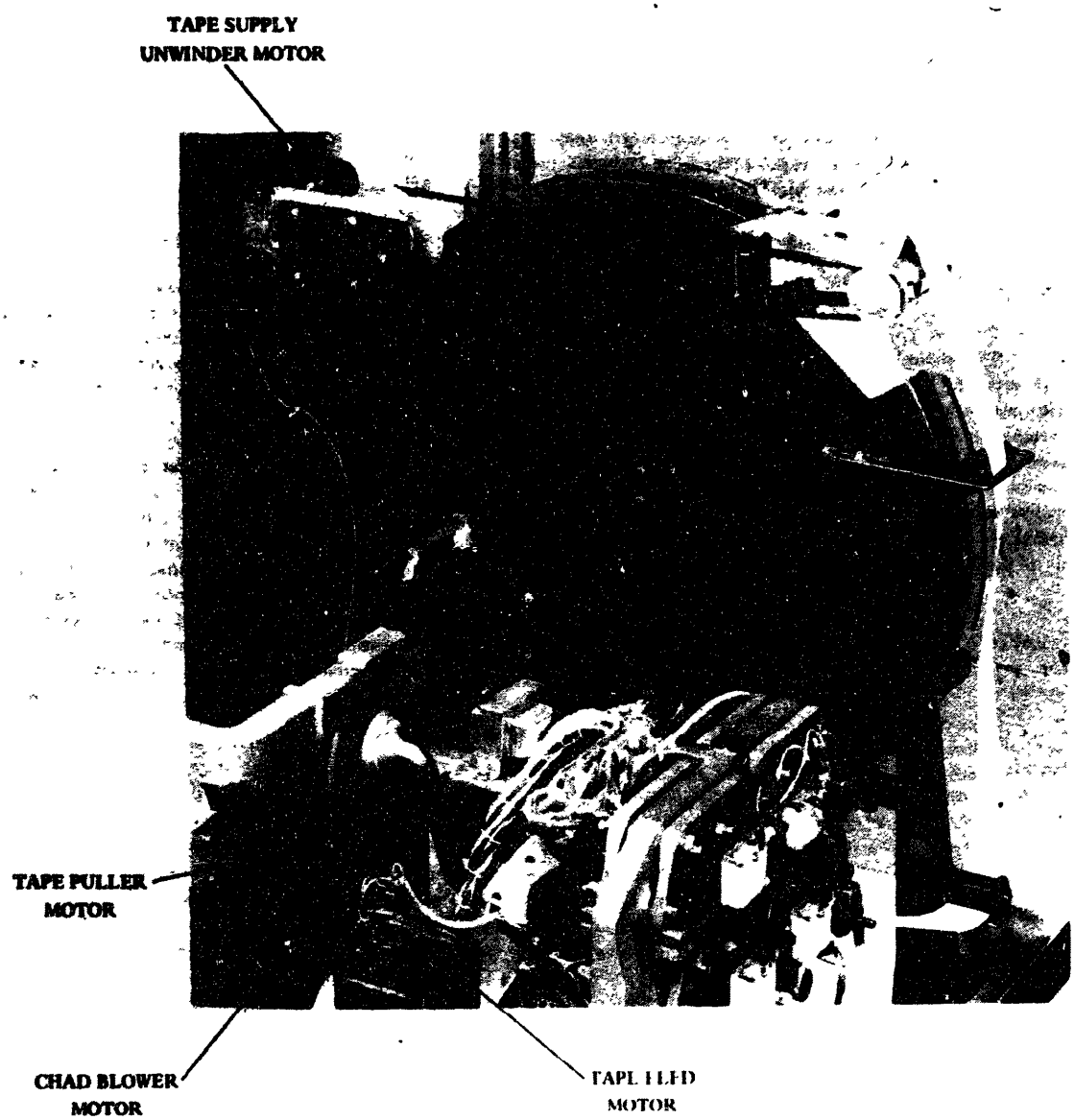


Figure 18- Tape Supply and Chad Blower Motors

POWER DISTRIBUTION

4.90 There are three independent ac input circuits, one for each receiver (upper and lower), and one for the cabinet outlets and fans. Each input is filtered, and protected by a 15 ampere circuit breaker. The ac outlets are protected with 5 ampere circuit breakers. Operating either power switch, SW110 or SW210 (upper or lower), activates the three exhaust fans which are protected by a 1 ampere circuit breaker (Figures 2 and 4). The upper reperforator shelf receives its power through the bidirectional silicon switch SST, protected by a 4 ampere circuit breaker (Sheet 9).

4.91 The power supply for the upper receiver is protected by a 5 ampere circuit breaker inside the power supply. The gate circuit for each switch is controlled by a separate pole of the POWER switch, protected by a 1 ampere circuit breaker. A thermal cutout switch removes power to the power supply and reperforator shelf when excessive cabinet temperature is detected. The lower power distribution circuits are similar to those in the upper receiver and will not be described separately.

REPERFORATOR POWER

4.92 Each reperforator shelf includes the following four motors; tape supply unwinder, chad blower, tape puller, and tape feed. The chad blower and tape supply unwinder motors run continuously as long as the POWER switch is on (Figure. 18). The tape puller motor is mounted on the tape input side of the punch mechanism. The switch contacts for this motor close when the tape slack in the tape guide loop is used up. This causes the bidirectional silicon switch associated with the tape puller motor to conduct, activating the motor (Sheet 10). The switch contacts for the tape feed motor close whenever the tape feed spring becomes unwound. This causes the bidirectional silicon switch associated with the tape feed motor to conduct, activating the motor.

DC POWER SUPPLY

4.93 The power supply employs a ferroresonant transformer to regulate for line voltage variations. Five separate windings, each with a full-wave rectifier, filter capacitor, and bleeder resistor are used for the outputs of -55 volts, -12 volts, -6 volts, -5 volts, and +6 volts (Sheet 11).

4.94 The -55 volt supply is used by the punch drivers. Each punch driver has a separate 1.7 ampere circuit breaker. The -5 volt supply is used for the punch holding circuits and is protected by a 25 ampere circuit breaker. The -12 volt supply is used by the logic circuits and is protected by a 3.5 ampere circuit breaker. The +6 volt and -6 volt supplies are electronically regulated with the polarity determined by which side is grounded. Except for some resistor values and circuit breakers these two supplies are alike. Due to the fact that both supplies are similar, only one will be described.

4.95 The Q6 emitter follower carries the entire current load of the supply. The base current is supplied through emitter follower Q4. The -12 volt base current comes directly from the power supply through R12. The base current may be diverted from Q4 through Q3 and CR12. The amount of diverted current is controlled by the base current of Q3. This is partly determined by the difference in potential between the CR12 drop and the output voltage at the arm of the variable resistor R16. The voltage across CR12 is a constant 4.7 volts regardless of the current through this diode.

4.96 If the output of the -6 volt supply tends to increase, more current will flow through R17 and the upper portion of R16 into the base of Q3 and through CR12. This will cause an increased current through R12 and Q3, causing the voltage at the collector of Q3 to become more positive. This reduces the base current into Q4, which reduces the base current into Q6. This causes an increased voltage drop across Q6, tending to restore the output of the supply to normal. Similarly, a decrease in output will decrease the base current into Q3, making more base current available to Q4 and therefore to Q6. This reduces the drop across Q6 and tends to increase the output of the supply.

TELETYPE CORPORATION
Skokie, Illinois, U.S.A.

HIGH SPEED TAPE RECEIVER FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS) INSTALLATION

CONTENTS PAGE

1. GENERAL

1.01 **This section provides installation information for the high speed tape receiver and is reissued to provide the latest engineering changes, remove preliminary from the title and make this section a standard publication. The changes include tape punch door latches, tape chutes, pushbutton circuit breakers, and relocated exhaust fans. Since this is a general revision, marginal arrows that indicate changes have been omitted.**

1.02 **The tape receiver is contained in one cabinet and incorporates two high speed paper tape punches (DRPE). Each has its own 3000 foot tape supply, serial to parallel converter, punch drive logic, and power supply. These are separate systems and function independently of each other (see Figure 1).**

1.03 **Paper tape punches (DRPE), tape handling mechanisms, electronic logic, and power supplies are accessible by pulling the assemblies or modules out from the front of the cabinet. Terminal board and power cable connections are made at the rear of the cabinet. Control display is located in the control panel on top of the cabinet.**

1.04 **All references to left or right, front or rear, up or down are made from a normal operating position in front of the tape receiver cabinet.**

2. TECHNICAL DATA

2.01 **Three 15 ampere, three-wire power cables are required for each receiver cabinet. An appropriately rated single power cable can be used if the three separate ac input terminals are properly strapped in parallel. A receiver set requires a voltage of 117 v ac ±10%, and a single phase frequency of 58.5 to 61.5 hertz.**

2.02 **Ambient room temperature should be within +40 degrees fahrenheit to 110 degrees fahrenheit range. Operating humidity tolerance is between 5 percent to 95 percent.**

2.03 **The receiver cabinet weighs 496 pounds with all assemblies and modules installed. Outside cabinet dimensions are, 22 inches wide, 26 inches deep and 60 inches high. Figure 2 shows cabinet base and floor mounting dimensions.**

2.04 **Power consumption measurements for the receiver operating on 117 v ac, 60 hertz are listed in Table A. The measurements were obtained with both punches perforating eight-level messages at a speed of 2400 words per minute.**

2.05 **For proper cabinet ventilation, sufficient air space is necessary to prevent recirculation of room air in excess of 110 degrees fahrenheit. Service and maintenance clearance is necessary in front, back, and top of cabinet. The electrical distribution panel, access in the top of the cabinet, requires a minimum of 10 inches clearance for the control cover to be raised. The amount of air passing through each exhaust fan is approximately 85 cubic feet per minute (CFM).**

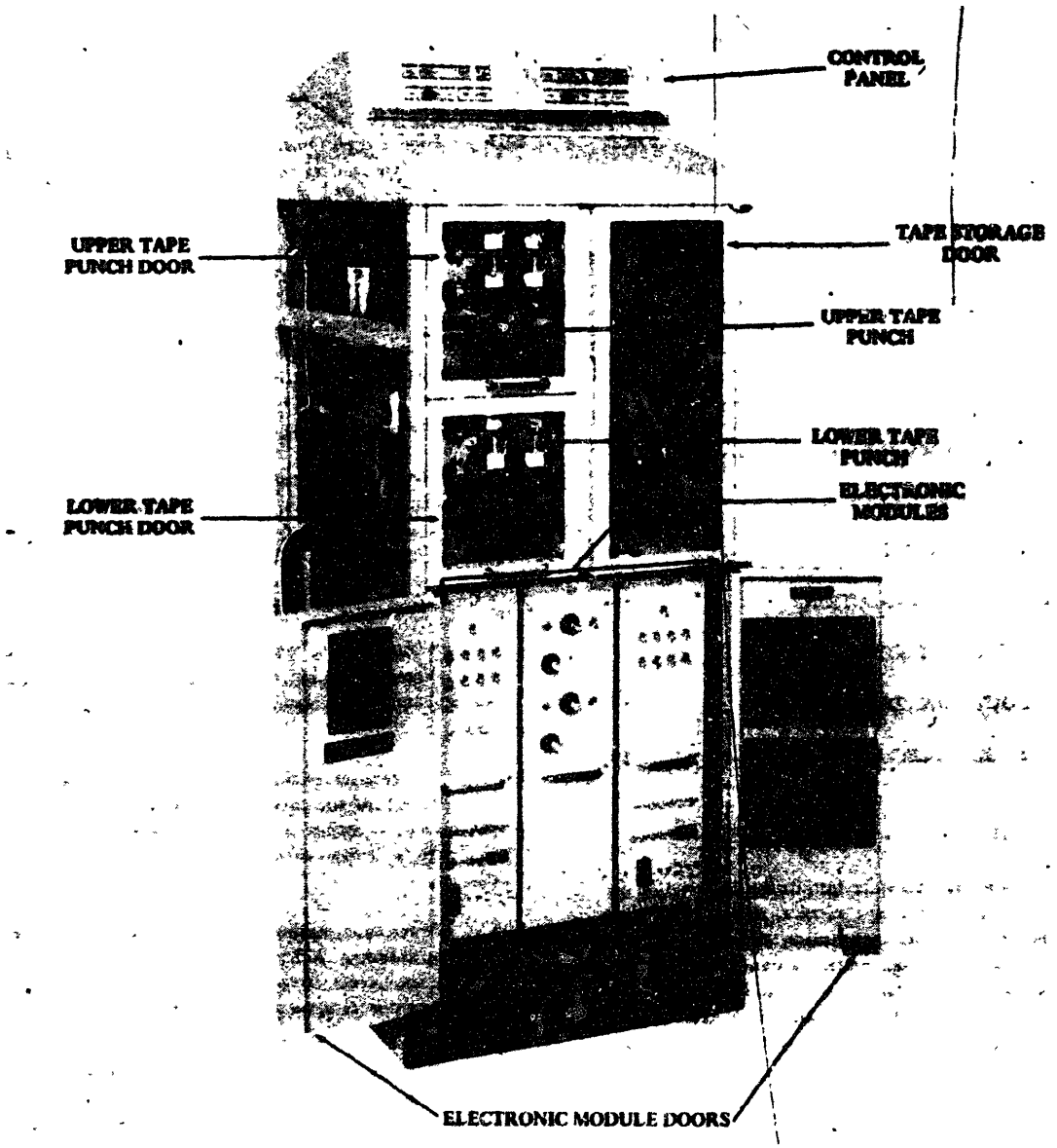


Figure 1- High Speed Tape Receiver Cabinet

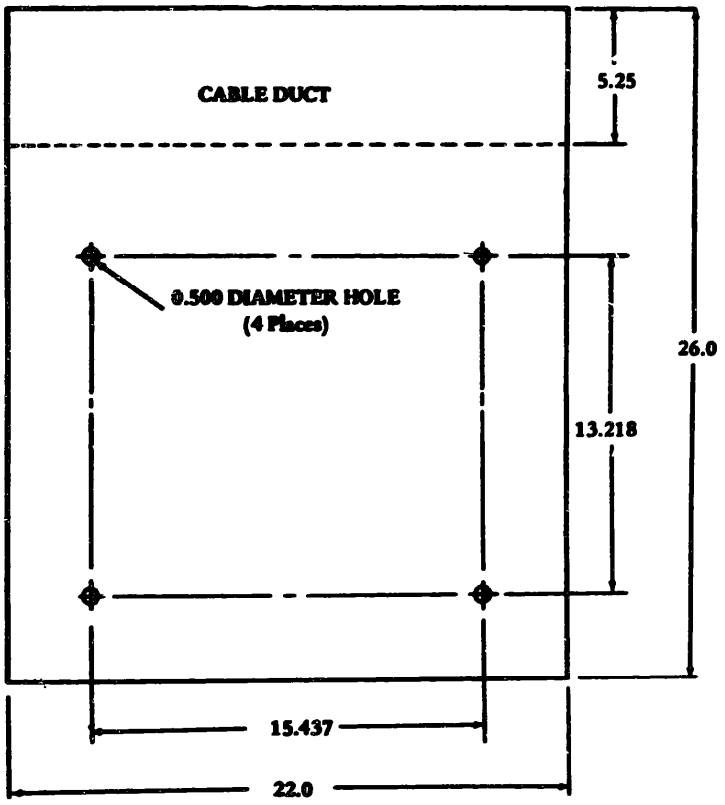


Figure 2- Mounting Hole Locations

TABLE A

POWER MEASUREMENTS

RUNNING CURRENT (AMPERES)	APPARENT (VOLT-AMPERES)	ACTUAL (WATTS)	POWER FACTOR (LAGGING)
9.2	1077	950	0.88

2.06 Access to the rear of cabinet is necessary for cable connectors. Rear doors fully opened swing out 11 inches maximum. Tape punch shelves extend 21 inches, and electronic modules extend 18 inches from the front of the cabinet. The lower cabinet front doors must open 180 degrees to allow the electronic modules to be pulled out.

2.07 The receiver cabinet has four 0.875 inch diameter conduit knock-out holes located on top of the cabinet, in back of the control panel cover. More conduit holes may be added, if necessary, or existing holes enlarged for 1.00 inch conduit (see Figure 3).

CAUTION: DO NOT CONNECT POWER TO CABINET BEFORE ALL ASSEMBLY MECHANISMS AND MODULES ARE INSTALLED AND READY FOR OPERATION.

3. INSTALLATION

CABINET

3.01 Carefully unpack the cabinet and all associated containers, observing all caution labels and instructions. The modules and tape punch (DRPE) units are shipped in separate containers.

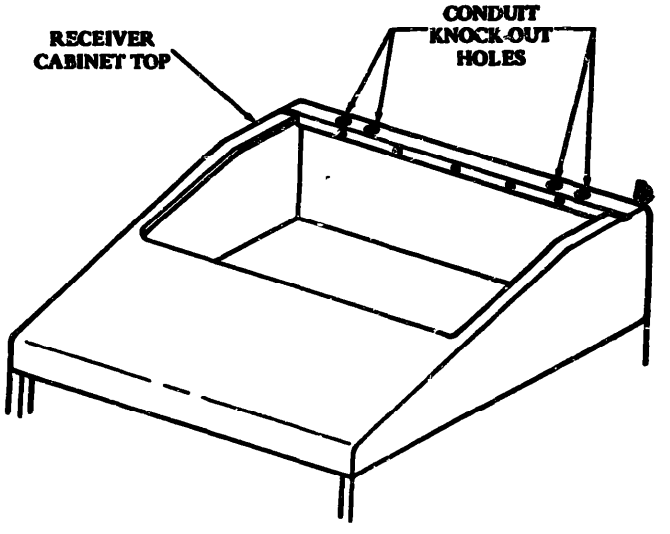


Figure 3- Conduit Accessibility

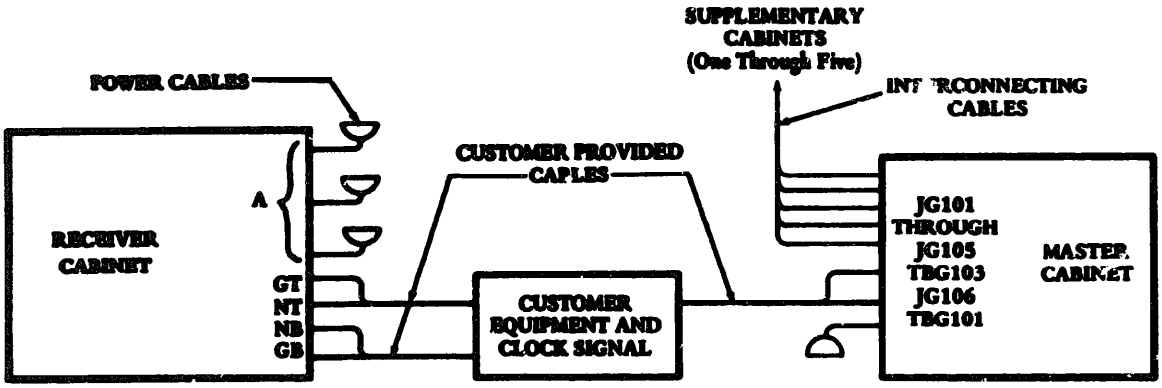


Figure 4- Cabinets and Cable Layout

3.02 **Modification kit, TP310824, provides left and right end enclosures for single and "bank" (side to side) installation of the high speed tape receiver cabinet (see Figure 5).**

3.03 **Remove the four shipping bolts, nuts and spacers, two of each on both sides of the cabinet (see Figure 5). Mount the TP310844 coverplate on the outer frame; the TP310845 duct channel, and TP310804 duct plate. Use the appropriate screws and nuts furnished with the loose parts carton secured to the inner frame. The screws may be installed either from the front or rear depending on the accessibility to the cabinet. Mount the TP310802 duct covers to the TP310804 duct plate using the appropriate screws and nuts.**

3.04 **For single cabinet installation secure the TP310755 right-side panel and TP310756 left-side panel in the mounting holes shown in Figure 5.**

MODULES

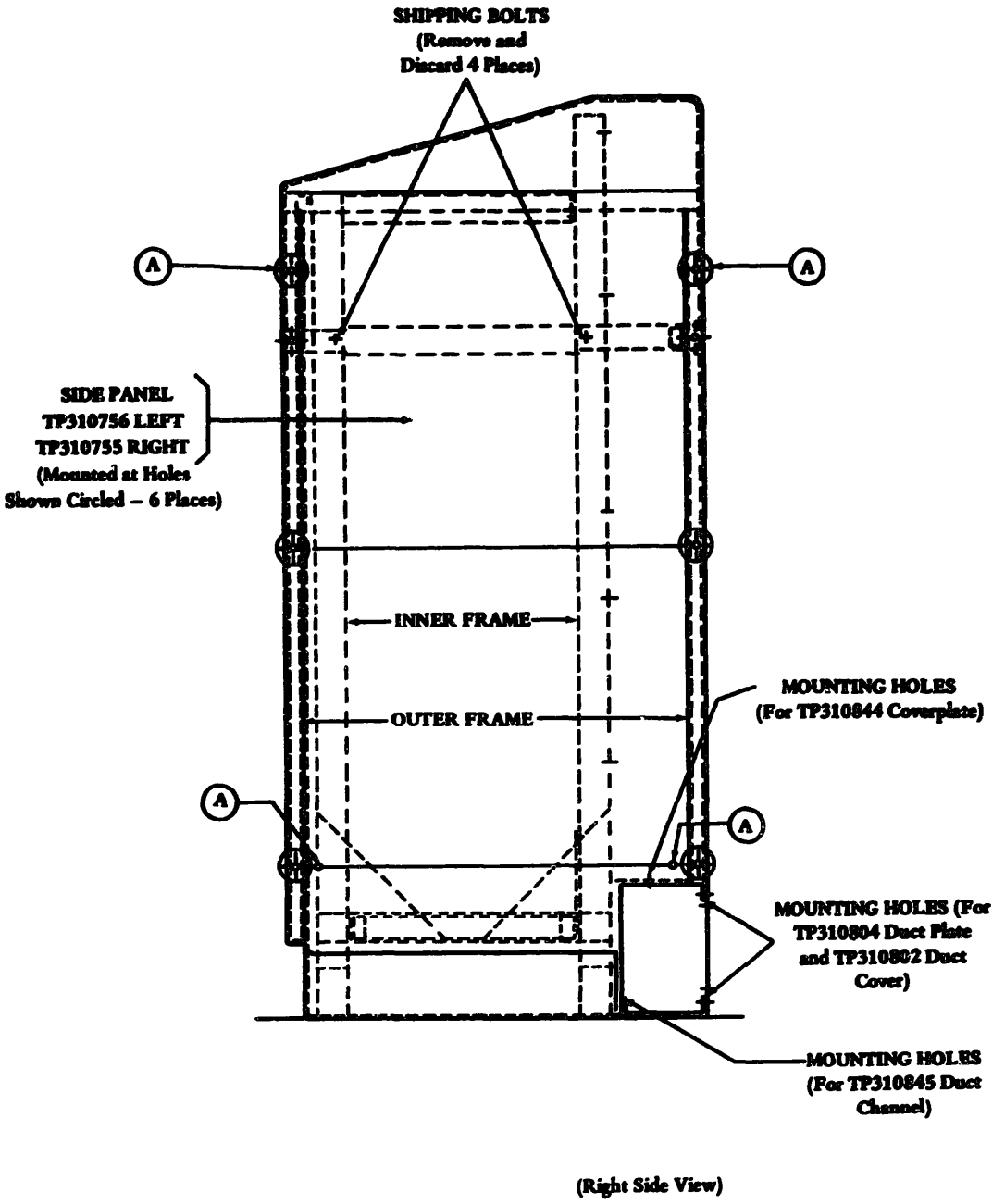
CAUTION:: **MODULE C (CONTAINING THE POWER SUPPLY) IS CONSIDERABLY HEAVIER THAN MODULE D. TO AVOID EXTENSIVE PARTS DAMAGE OR PERSONAL INJURY, HANDLE MODULE C CAREFULLY WHEN INSTALLING OR REMOVING FROM CABINET.**

3.05 **Install C and D modules in front lower section of receiver cabinet using the following procedure:**

(a) Before mounting module D (TP310903 in the center guide of the cabinet) set the module on the floor in front of the open cabinet. Attach the two associated cable connectors from the rear of the cabinet. Connect PD328 connector to upper receptacle JD328 on the module. Connect PD428 connector to lower receptacle JD428, tighten locking screws on all connectors (see Figure 6).

(b) Install the module in the cabinet by slipping the top edge of the module under and behind the metal tab on the top edge of the module guide frame. Slide the bottom of the module on to its guide, and slide the module all the way back into the cabinet.

(c) Lock the module in place by rotating the locking screw (top center of module panel) about a quarter of a turn in a clockwise direction to its locking position



Note: For "bank" installation, use holes marked A (4 places).

Figure 5- Frame Mounting Applications

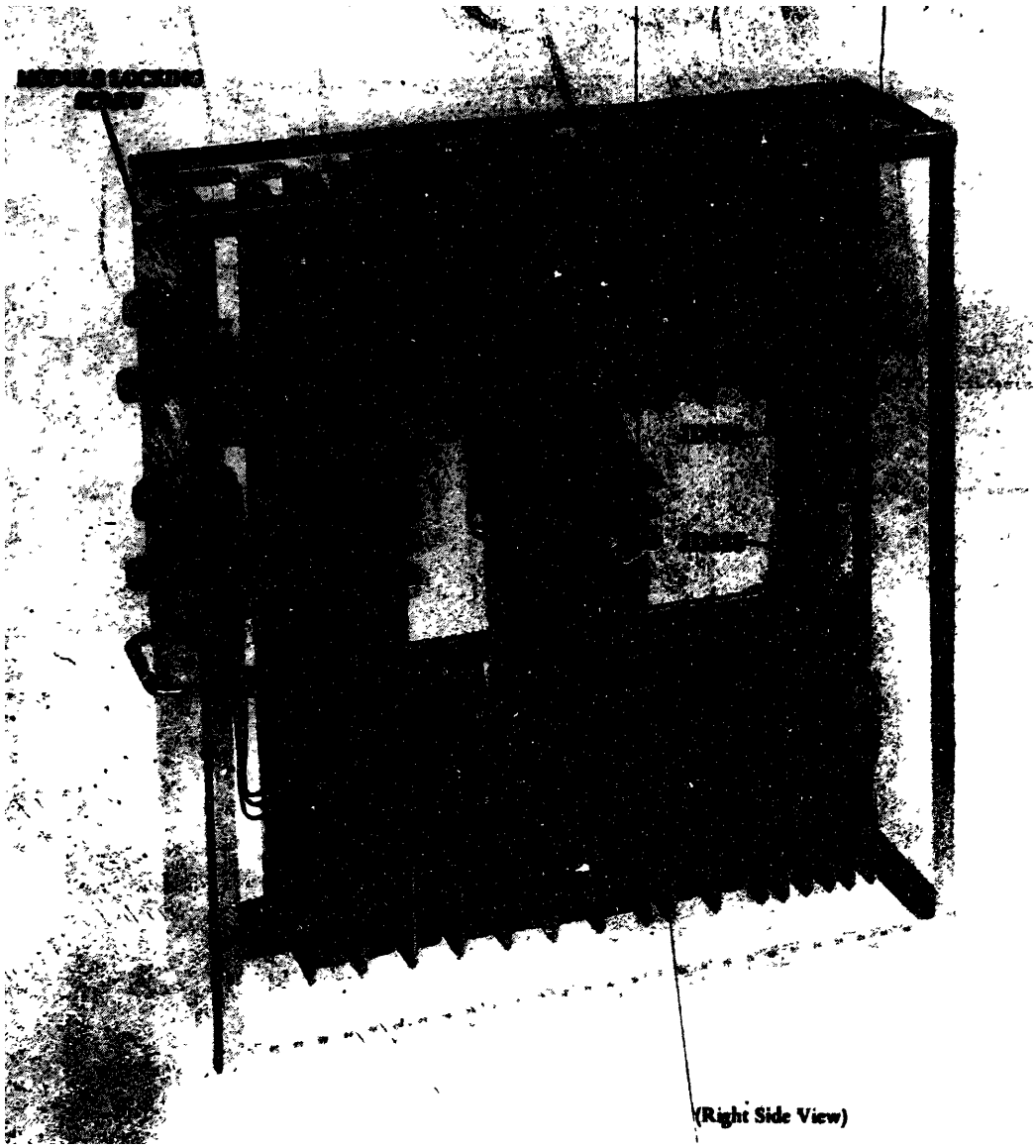


Figure 6- Module D Circuit Card Side

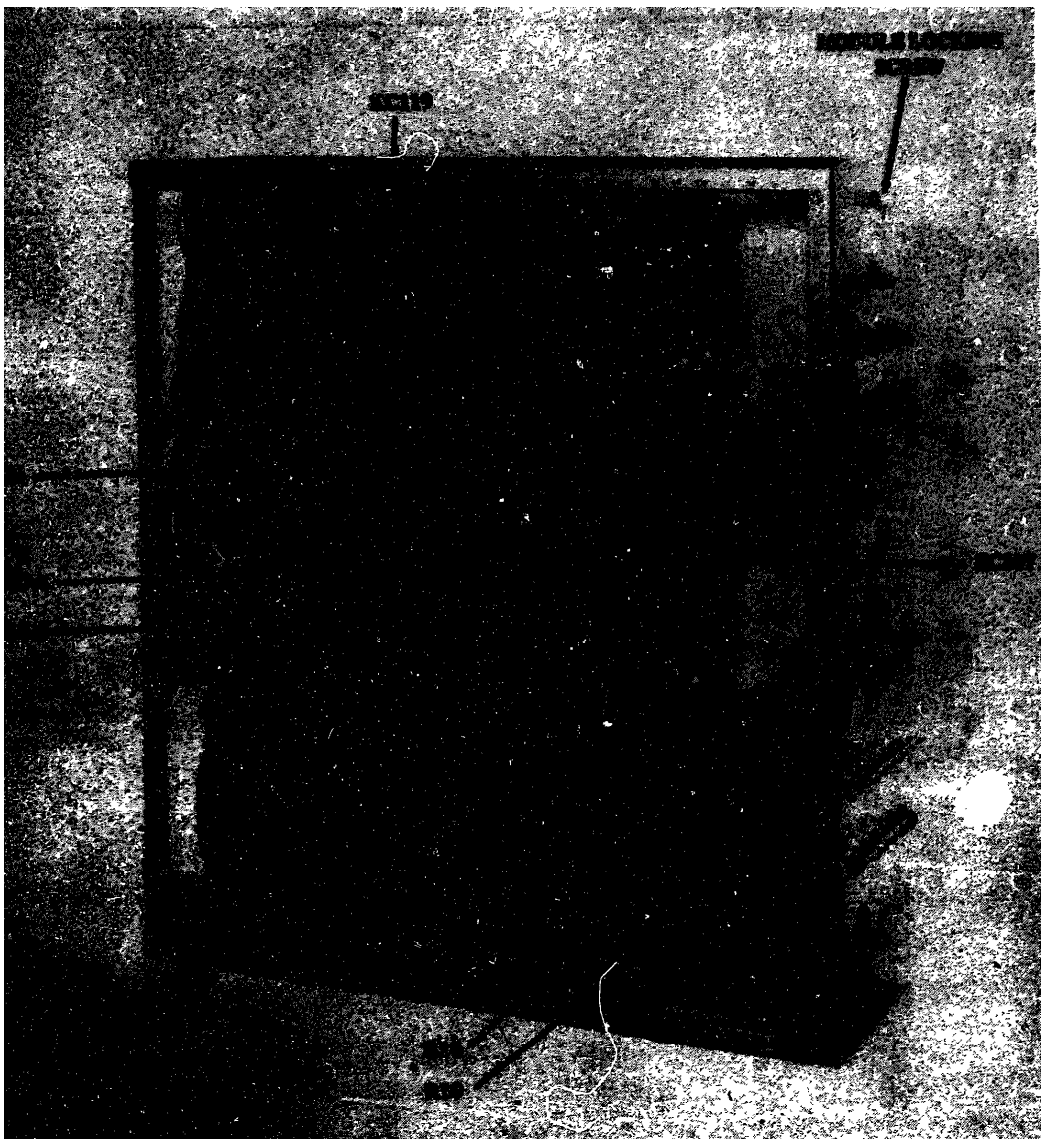


Figure 7- Model C Wiring Slide

(d) Set a module C (both TP310903 modules are identical) on the floor in front of the left guide. Attach the three associated cable connectors from the rear of the cabinet. Connect the TPC328 connector to the upper receptacle JC328 on the module, tighten locking screws on connector. Connect TPC-A connector to middle receptacle JC428-A and BPC-B to lower receptacle JC428-B, insert the connectors and turn a quarter turn clockwise to lock in place (a quarter turn counterclockwise to release) (see Figure 7). Install module in cabinet in the same manner as described in (b) and (c).

(e) Set the other module C (TP310903) on the floor in front of the right guide. Attach the three associated cable connectors from the rear of the cabinet. Connect the BPC328 connector to the upper receptacle JC328 on the module, tighten locking screws on connector. Connect BPC-A connector to middle receptacle JC428-A and TPC-B to lower receptacle JC428-B, insert the connectors and lock in place (see Figure 7). Install module in cabinet in the same manner as described in (b) and (c).

HIGH SPEED TAPE PUNCH

3.07 Before installing the tape punch (DRPE), (both units are identical, use same procedure for each unit), open the right hand upper door and slide out the appropriate shelf by pulling straight forward on the handle (upper or lower) of the left door. A slight pull will release the shelf held in place by a magnetic latch.

3.08 Slide the shelf out to its fully extended locking position. Open the small tape punch door on the left front side of the shelf, by releasing the door latch at the upper inside left hand corner. Place the rear of the tape punch base plate on the shelf at the appropriate mounting location. Slide the base plate back to the shelf stop, and place the positioning hole of the base plate over the locating stud at the front of the shelf.

3.09 Slip the plastic chad tube (attached to the shelf metal chad chute) over the tape punch chad tube, located under the tape punch. Attach the shelf connector "DP" to the tape punch receptacle, and tighten connector locking screws (see Figure 8 and Figure 9).

3.10 To slide the shelf back into the cabinet, bring the left hand tape punch door (upper or lower) up to its locking position. Press the locking latch on the side of each slide and push inward. The shelf can now be pushed back into the cabinet to its closed position.

TAPE CONTAINER DOOR

3.11 The tape container plastic door is hinged at the rear by brackets and a removable rod. The door is latched at the front by a straight wire spring which fits into the notch of the latch plate (see Figure 10).

3.12 The door can be positioned to use 11/16 or 1 inch tape by removing the retaining rings from the rod and sliding the rod downward out of the bracket holes. Insert the rod in the appropriate bracket holes according to the type of tape used. Loosen the latch plate and move the plate to its outer position for 1 inch tape or the inner position for 11/16 inch tape.

POWER CONNECTIONS

3.13 Use the hookup in Table B when connecting power cables to the power terminal board located in the rear left side of the cabinet (see Figure 11 and Table D).

TABLE B

POWER HOOKUP

POWER LINE	WIRE	TERMINAL NUMBER
1	WH BK GN	T1 T2 GND
2	WH BK GN	T3 T4 GND
3	WH BK GN	T5 T6 GND

SIGNAL INPUT CONNECTIONS

3.14 The top cover over the distribution panel can be raised by loosening the cover locking screw located inside the cabinet directly under the top control panel, front and center (see Figure 12).

3.15 Route signal input cables to the front side of electrical distribution panel, connect cables to the signal input connectors NT and NB. The signal input ground connections are made at GT and GB ground terminals shown in Figure 12. A typical cabinet and cable layout is shown in Figure 4.

3.16 Table C consists of wiring information for the signal cables. The table shows wire designations, connectors, pin numbers, and wiring diagram references. The wiring location code refers to wiring diagram sheet numbers with horizontal and vertical coordinates respectively. Refer to Section 592-852-400TC for wiring diagrams and Section 592-852-130TC for circuit description.

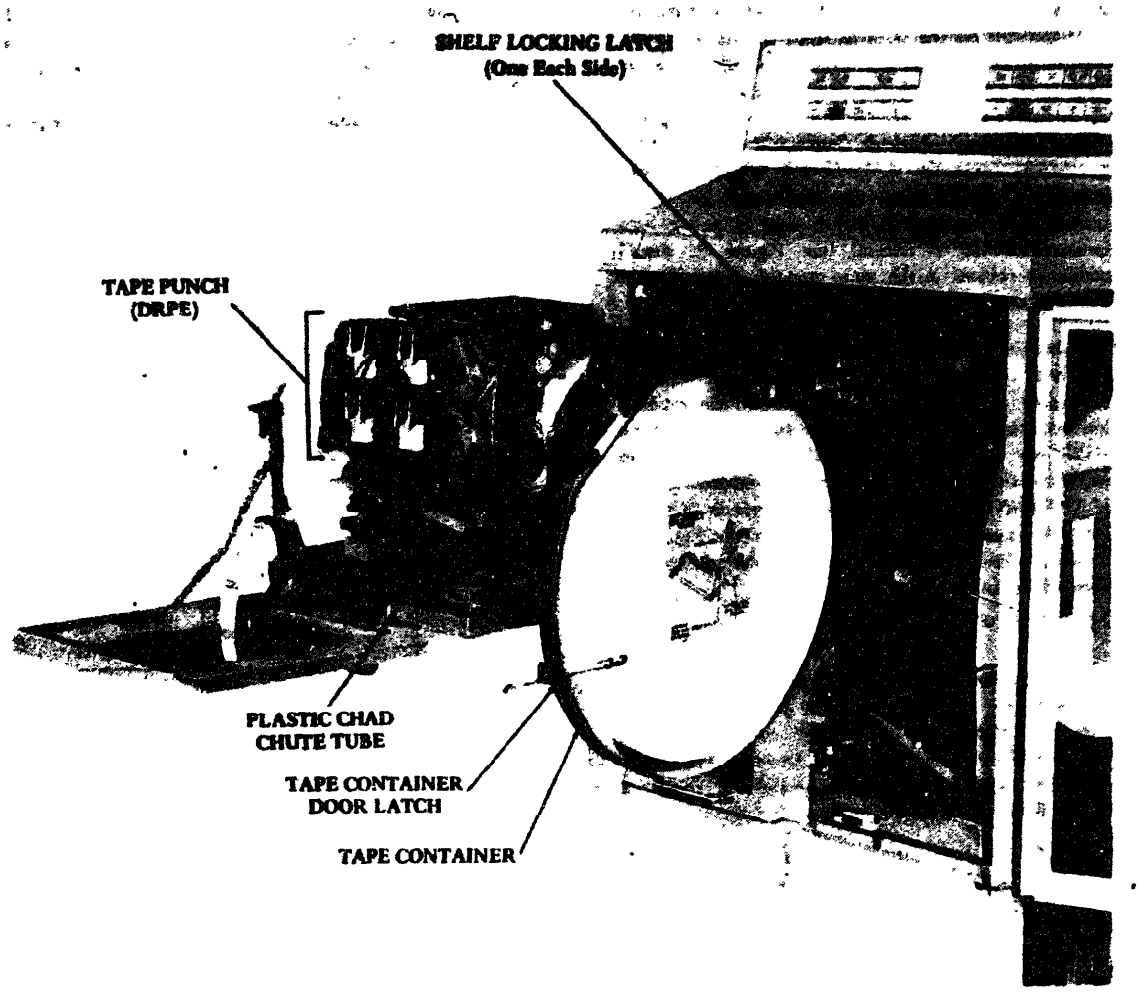


Figure 8- Top Tape Punch and Tape Container

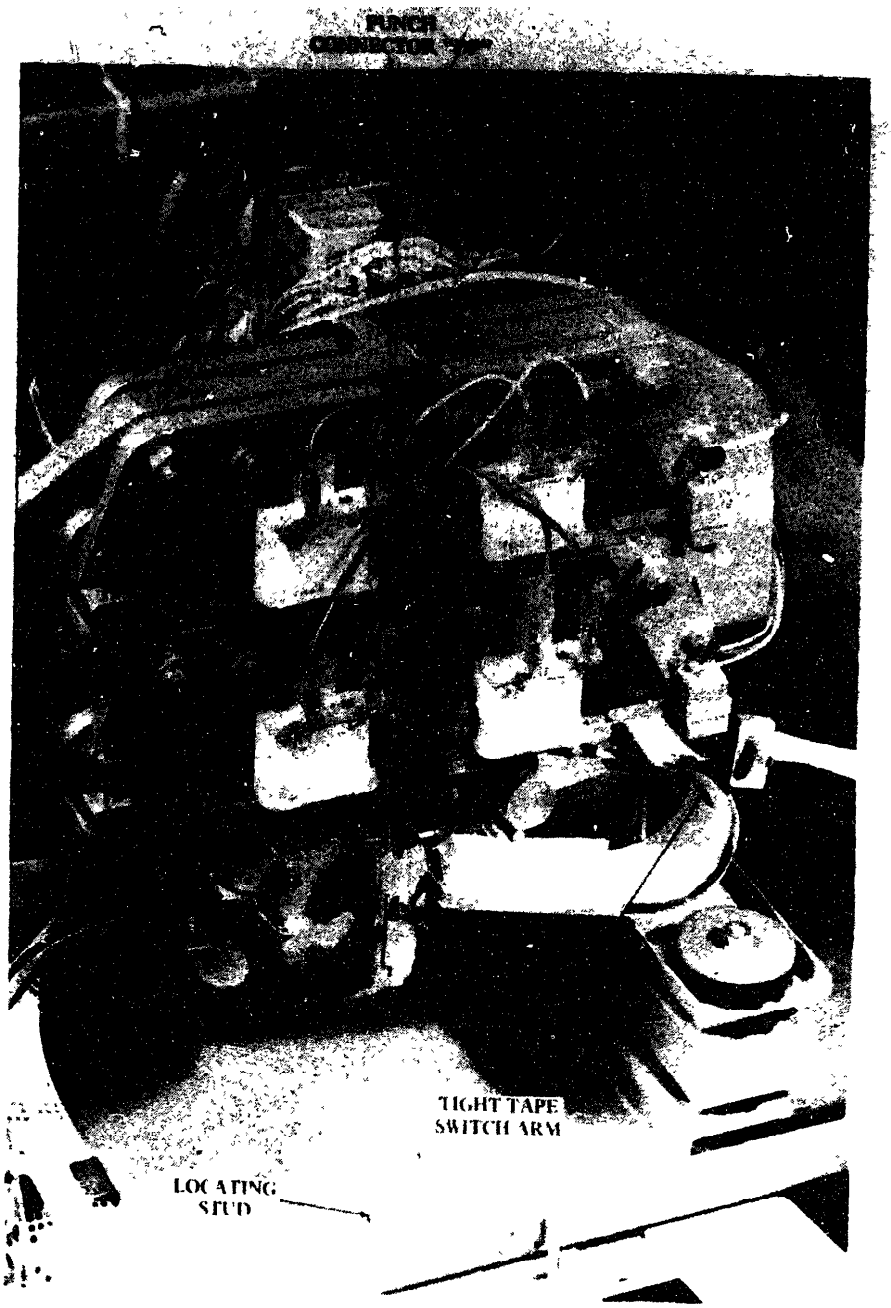


Figure 9 Tape Punch Locating Stud

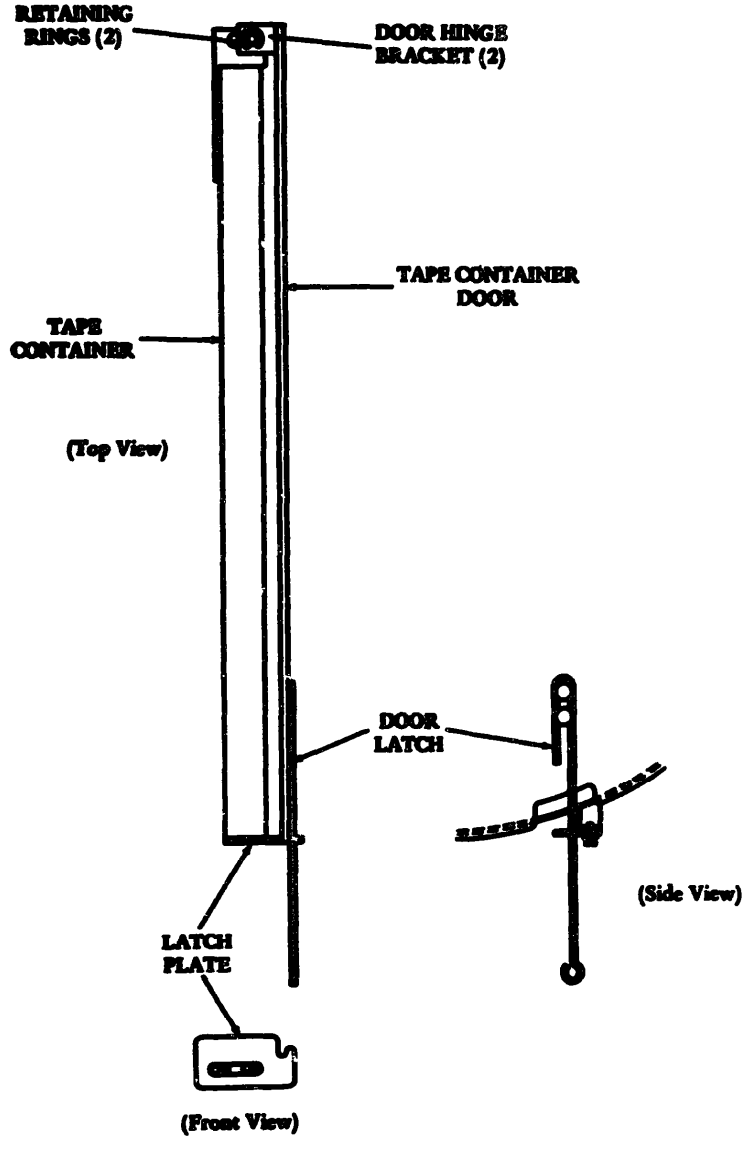


Figure 10- Tape Container Door

Figure 11- Main Power Connections

TABLE C

RECEIVER CABINET CONNECTIONS

DESIGNATION	SIGNAL CONNECTORS NB AND NT	7730 WD LOCATION
Aux Bit 1 In	1	4-C-2
Bit 1 Out	2	7-D-8
Aux Bit 2 In	3	4-C-2
Bit 2 Out	4	8-E-8
Aux Bit 3 In	5	4-D-2
Bit 3 Out	6	8-D-8
Aux Bit 4 In	7	4-D-2
Bit 4 Out	8	8-C-8
Aux Bit 5 In	9	4-E-2
Bit 5 In	10	8-A-8
Aux Bit 6 In	11	4-F-2
Bit 6 Out	12	7-F-8
Aux Bit 7 In	13	4-F-2
Bit 7 Out	14	7-C-8
Aux Bit 8 In	15	4-F-2
Bit 8 Out	16	7-B-8

DESIGNATION	SIGNAL CONNECTORS NB AND NT	7730 WD LOCATION
Aux Sample	17	4-B-2
Character Available	18	8-F-8
Frame Ground	19	9-F-5
Clock Input	20	5-A-3
Serial Data In	22	5-B-3
Urgent Traffic	26	5-F-1
External + 6 Volts	28	8-E-1
External - 6 Volts	30	8-E-1

TABLE D

RECEIVER CABINET CONNECTIONS

DESIGNATION	SIGNAL CONNECTORS NB AND NT	7730 WD LOCATION
Alarm Contact (Common)	32	2-B-8
Alarm Contact (Normally Open)	34	2-A-8
Alarm Contact (Normally Closed)	36	2-B-8
Circuit Common Terminal GB	Terminal 1	9-F-5
Circuit Common Terminal GT	Terminal 1	9-F-8

DESIGNATION	AC POWER TERMINAL BLOCK A	7730 WD LOCATION
AC Common	1	9-C-2
AC Hot	2	9-C-2
AC Common	3	9-C-2
AC Hot	4	9-C-2
AC Common	5	9-C-2
AC Hot	6	9-D-2
Frame Ground	Two Tapped Holes Above Terminal Block A	9-D-2

3.17 [redacted]

3.18 [redacted]

3.19 [redacted]

3.20 Press both POWER switches on the cabinet control panel. The POWER switch indicators will light when pressed, activating power to the cabinet mechanisms and modules. When the switch is pressed a second time, the switch indicator light will turn off and power is deactivated (see Figure 14).

4. CHECKOUT PROCEDURE

4.01 [redacted]

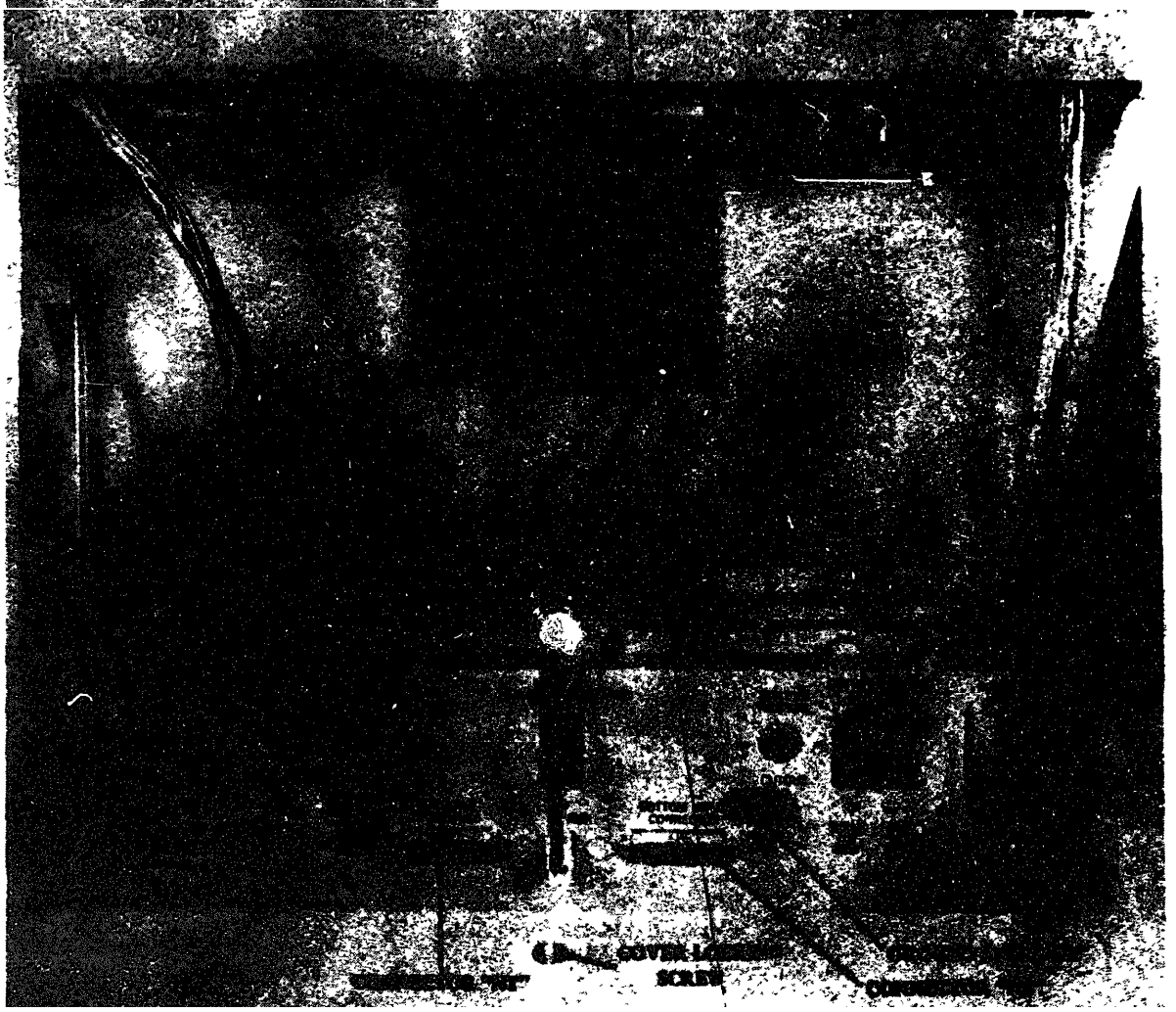


Figure 12- Electrical Distribution Panel

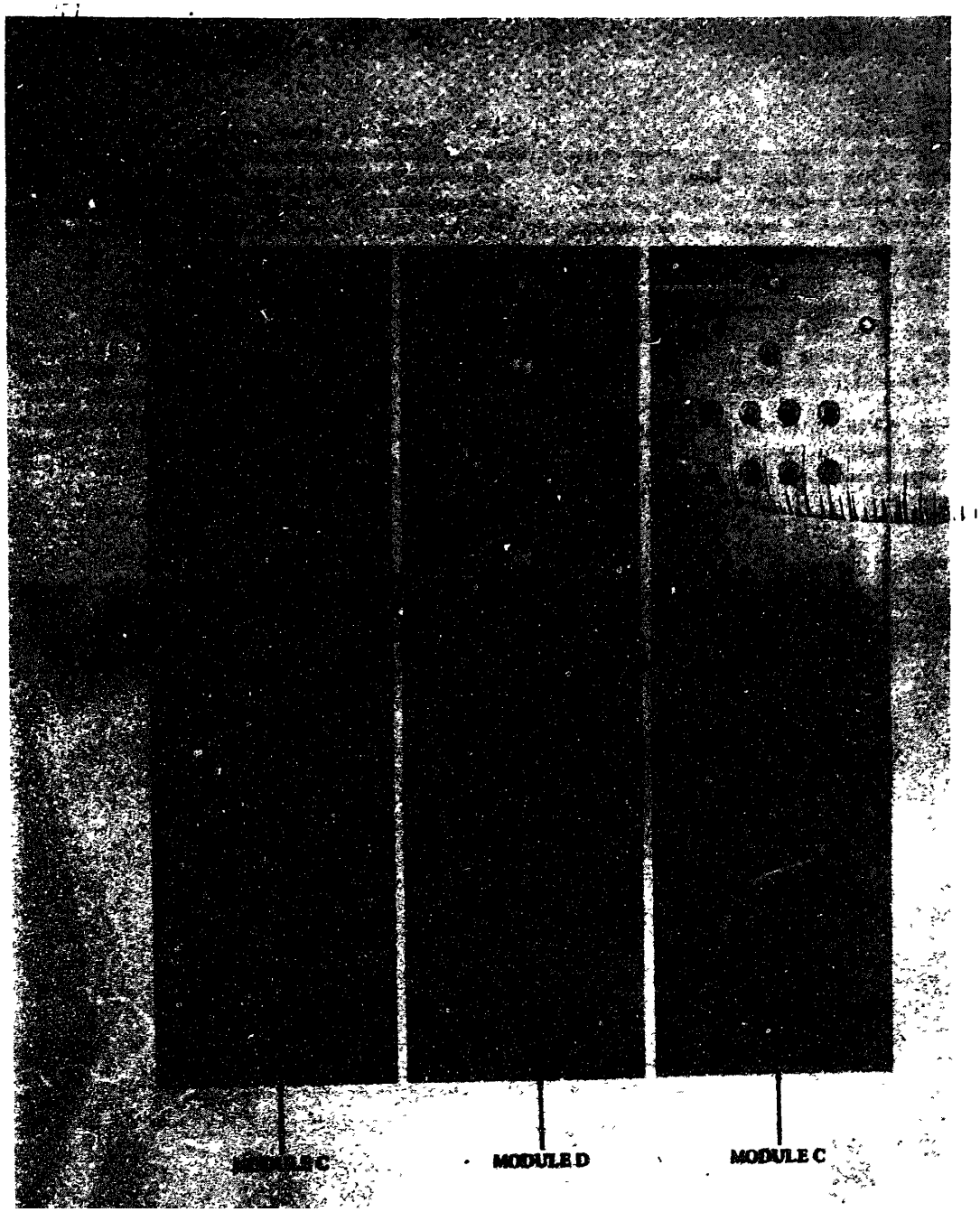


Figure 13- Module Configuration

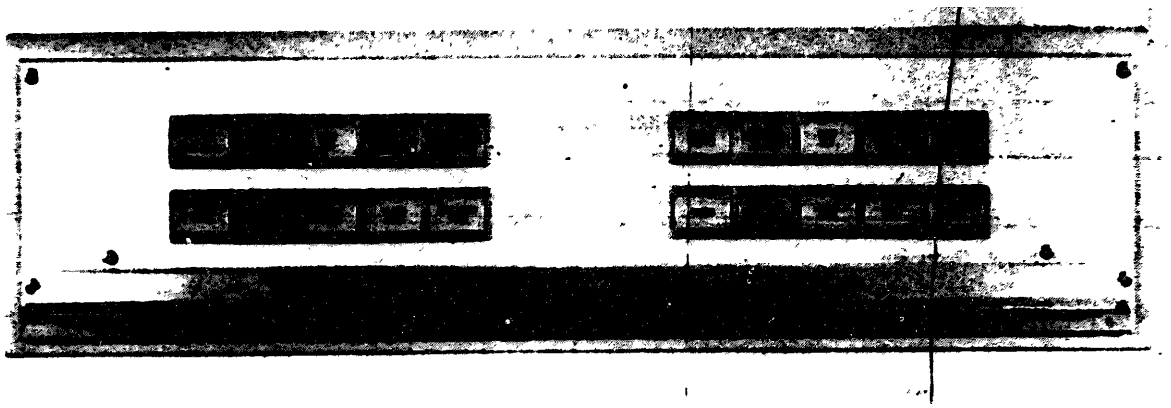


Figure 14- Receive Cabinet Control Panel

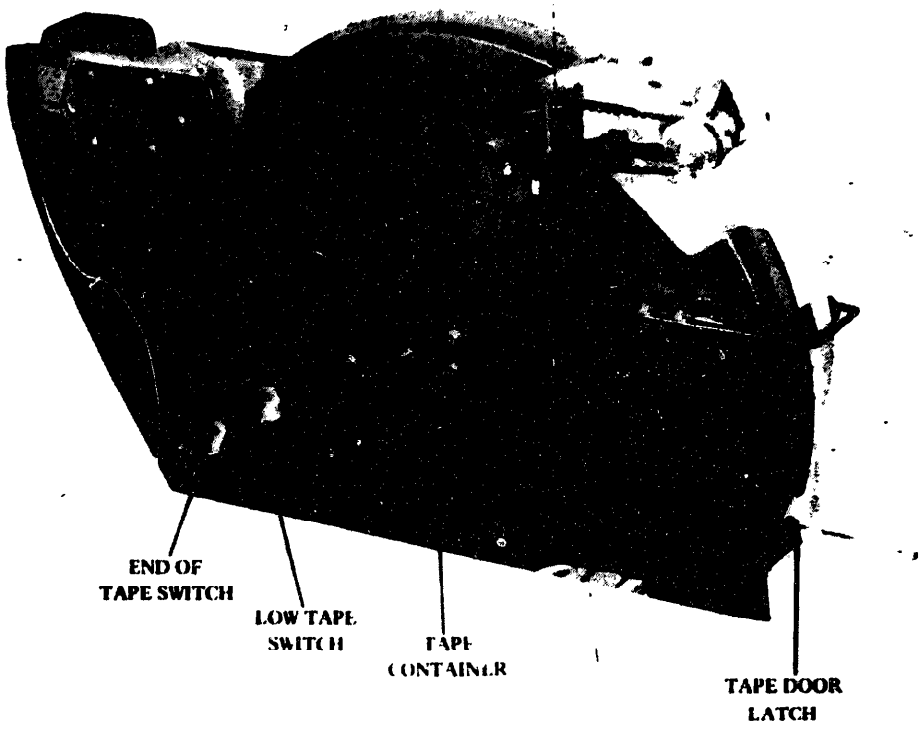


Figure 15- Low Tape and End of Tape Switches

HIGH SPEED RECEIVER CHECKOUT

ACTION	VERIFICATION
(1) Power Supply Operation	
(a) Press POWER switch	Power indicator should light, unwinder motor should run, and exhaust fans (3) should run.
(b) With power applied.	All voltages should be present.
(2) Punch Operation	
(a) Press BLANK FEED switches.	Tape punches should perforate blank characters at 105 characters per second.
(b) Press CHARACTER FEED switches.	Tape punches should perforate the character programmed on the front of the corresponding drive module (C). Check both mark and space of each bit. Check the 105 characters per second and 240 characters per second with both CHARACTER FEED switches.
(c) Remove power for approximately one minute. Reoperate POWER switches. A minimum of 5 seconds should be observed before reoperating POWER switches.	Punches should perforate one delete (Rub-out) character after power is reapplied.
(3) Alarm Operation	
(a) Operate chad bin switch. Press on chad box or tray with one hand until switch activates indicator (see Figure 11).	CHAD BIN indicator on control panel should light.
(b) Operate low tape switch. Without tape in tape container, move tape arm about one inch above the center post (Figure 15).	LOW TAPE indicator on control panel should light.
(c) With no alarms present.	Relay KC119-A should be operated. (Located in C modules, Figure 7).
(d) Operate end of tape switch. Without tape in tape container, tape arm should be resting on center post.	END OF TAPE indicator should light on control panel, and KC119-A should release.
(e) Operate END OF TAPE/TAPE OUT indicator switch with end of tape condition cleared.	END OF TAPE indication should clear and KC119-A should operate.
(f) Operate tape-out switch.	TAPE-OUT indicator should light and KC119-A should release.
(g) Operate END OF TAPE/TAPE-OUT indicator switch with tape out condition cleared.	TAPE-OUT indication should clear and KC119-A should operate

HIGH SPEED RECEIVER CHECKOUT (Continued)

ACTION	VERIFICATION
(h) Operate tight tape switch. Move tight tape switch arm to the left (Figure 9).	TIGHT TAPE indicator should light and KC119-A should release.
(i) Operate TIGHT TAPE/TAPE FEED indicator switch with tight tape condition cleared.	TIGHT TAPE indication should clear and KC119-A should operate.
(j) Hold tape in supply chute of punch and operate a feed-out switch.	TAPE FEED indicator should light and KC119-A should release.
(k) Refeed tape through the punch to permit proper operation of the feedout switches. Operate TIGHT TAPE/TAPE FEED indicator switch.	TAPE FEED indicator should clear and KC119-A should operate.
(l) Momentarily operate each of the following switches: BLANK FEED, CHARACTER FEED, and BUSY OUT.	The associated switch indicators should light and release KC119 A while each switch is operated.
(4) Auxiliary Parallel Input	
Operate auxiliary parallel input with a suitable test message.	The punch should reperforate the test message properly.
(5) Counter Operation	
The following checks require an input clock signal, with CHAR. SYNC. switch (module D) in the OFF position, and the receiver in the MANUAL SYNC. MODE (control panel).	
(a) Place the SIGNAL MODE switch in the SYNCHRONOUS position. Vary the UNITS PER CHARACTER INTERVAL switch from 5 through 16 (D module).	The number of clock pulses (ZD507-A11) indicated by the UPCI switch should occur between character shift pulses (ZD305-A27).
(b) Place the SIGNAL MODE switch in the START-STOP position. Vary the UNITS PER CHARACTER INVERVAL switch from 6 through 16.	The number of clock pulses (ZD507-A11) indicated by the UPCI switch should occur between character shift pulses (ZD305-A27).
(6) Synchronizing Circuit Operation	
(a) Operate MANUAL SYNC switch (control panel).	When the switch is operated, the MANUAL SYNC indicator should light and pin ZD505-B6 should be at circuit ground. When the switch is released the indicator should go out and the voltage reading should be -5 volts.
(b) With pin ZD520-A5 at circuit ground, operate the MANUAL SYNC switch (control panel).	The MANUAL SYNC MODE and AUTOMATIC SYNC MODE indicators should light alternately with each operation of the indicator switch.

HIGH SPEED RECEIVER CHECKOUT (Continued)

ACTION	VERIFICATION
(c) With an input clock signal provided, operate the MANUAL SYNC switch.	Pin ZD505-A10 should have a circuit ground potential for one clock pulse (between two adjacent bit shifts) for each operation of the MANUAL SYNC switch.
(d) With an input clock signal provided, connect circuit ground to pin ZD520-A5 and operate the receiver AUTOMATIC SYNC MODE indicator switch.	Pin ZD505-A10 should have a circuit ground potential for one clock pulse (between two adjacent bit shifts) following each character shift pulse.
(e) Remove the circuit ground from pin ZD520-A5.	
(7) Serial to Parallel Converter Operation	
The following checks require an input clock signal and serial data should be provided. The strapping on the program board (ZD517) should agree with the input data. The UNITS PER CHARACTER INTERVAL switch should be properly selected, and the CHAR. SYNC. switch should be in the OFF position.	
(a) Place the SIGNAL MODE switch in the SYNCHRONOUS position. Synchronize the receiver to the sending device, and send a test message.	The punch should accurately reproduce the test message.
(b) With the same conditions as (a) above, vary the CODE LEVEL switch from 8 through 5.	The punch should accurately reproduce the test message with unselected data levels spacing.
(c) Place the SIGNAL MODE switch in the START-STOP position. Synchronize the receiver to the sending device, and send a test message.	The punch should accurately reproduce the message.
(8) Character Synchronization Operation	
The following check requires an input clock signal and serial data with no inverted bits and with more than one stop bit. The strapping on the program board (ZD517) should agree with the input data. Place the SIGNAL MODE switch in the START-STOP position, and the CHAR SYNC switch in the ON position.	
Place the CODE LEVEL switch in the correct level position. Place the UNITS PER CHARACTER INTERVAL switch two positions higher in relation to the CODE LEVEL switch.	The punch should accurately reproduce the test message.
(9) Urgent Traffic Operation	
(a) Place a positive (-6 volts to +6 volts) pulse on the urgent traffic input.	The URGENT TRAFFIC indicator should light.
(b) Operate the URGENT TRAFFIC indicator switch.	The URGENT TRAFFIC indicator should go out.

TELETYPE CORPORATION
Skokie, Illinois, U.S.A.

HIGH SPEED TAPE RECEIVER FOR THE MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS) TROUBLESHOOTING

CONTENTS PAGE

1. GENERAL

1.01 This section provides troubleshooting procedures for the high speed tape receiver, used in the Multiple Address Processing System. It is reissued to include the latest engineering information, change the title, remove the preliminary designation, and change this section to the standard format. Since this is a general revision, marginal arrows that indicate changes and additions are omitted.

1.02 The troubleshooting tables in this section are designed to be used as an aid in locating trouble within the equipment. Testing and replacing components should be performed by persons familiar with transistor circuits.

Note: After performing troubleshooting duties, make certain all screws and electrical connections are secure.

1.03 The following test equipment and tools are recommended to be used in troubleshooting this equipment:

(a) Tektronix 516 series oscilloscope or equivalent.

(b) Multimeter (volt-ohm-ma) 20,000 ohms/volts.

(c) Adjustments and adjusting tool information for the high speed punch can be found in Section 592-803-700TC.

2. TROUBLESHOOTING

2.01 The trouble should be analyzed to recognize the source of the problem. The cause of trouble should be pinpointed to the exact area rather than giving a general description. For example, it would be more informative to say, "The command pulse failed to appear at input pin A22 on ZC324." instead of, "The tape punch fails to operate." Readjustments should not be made to correct trouble that is not fully understood. This can result in creating more trouble in the malfunctioning mechanism or circuit.

2.02 When trouble indicates that a circuit card or cards should be replaced the procedure to follow, if possible, would be to replace all the indicated cards. Then one by one replace the new cards with the old cards, until the trouble reappears. The faulty card should be replaced with a new card and the remaining old cards plugged back into the equipment.

2.03 The troubleshooting information in the tables is based on the fact that input data to the equipment is not faulty. A table is not included for the alarm circuits due to the simplicity of their operation.

2.04 Before removing or replacing circuit cards or reperforators during the troubleshooting procedure, make certain the cabinet POWER switch is in the off condition. Removing or replacing components with the power on can result in serious injury to personnel or can damage equipment.

TABLE A

POWER FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate POWER switch. POWER indicator should light.	POWER indicator does not light.	Check power circuit breakers. Refer to 7730WD, Sheet 9.
		Check power source. Check -12 volt circuit breakers. Refer to 7730WD, Sheet 9.
		Check POWER indicator lamp. Refer to 7730WD, Sheet 9.
If the tape unwinder motor is running, the fault is not in the power supply.	Tape unwinder motor is not running.	Check shelf bi-directional switch.
		Check module bi-directional switch.
		Check ac wiring for open circuit.
		Check -12 volt power supply voltage, and connections before circuit breaker.

TABLE B

COMPLETE PUNCH FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate CHARACTER FEED switch.	Punch fails to operate.	Check Table A, Power Failure.
Operate CHARACTER FEED switch.	CHARACTER FEED switch fails to operate punch.	Replace circuit cards ZC112 and ZC313.
Operate BLANK FEED switch.	BLANK FEED switch fails to operate punch.	Replace ZC120, ZC307, ZC114, ZC314, ZC110. Refer to 7730WD, Sheets 2, 3, and 4.
When the CHARACTER FEED switch is operated, the parallel input signal should operate.	Parallel input not operating.	Replace ZC114 and ZC112.
Check serial input.	Serial input not operating.	Replace ZC311. Recheck failure. Refer to 7730WD, Sheet 2.

TABLE B

COMPLETE PUNCH FAILURE (Continued)

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Check reperforator switch positions on module D.	Punch not operating.	Check reperforator switch positions and strapping on ZD517. Strapping on ZD517 must be the same as strapping on the transmitter. Refer to 7730WD, Sheet 8.
With the switches and strapping correct, check clock input signal.	Clock input is not present at bit shift ZD305-B11.	Replace ZD305, ZD507, and ZD307. Refer to 7730WD, Sheet 5.
Check character shift at ZD305-A27.	Character shift is not present.	Check counter drive at ZD303-A17. If counter drive is not present, replace ZD303.
	Check for failure in character synchronous circuit.	Recheck troubleshooting sequence from serial input. Refer to 7730WD, Sheet 5.
Check counter output at ZD303-A27.	Counter output present.	Replace ZD305.
	Counter output not present.	Replace ZD303 and ZD503.
Check sample pulse at ZC520-B28.	Sample pulse not present.	Place SIGNAL MODE switch in the SYNCHRONOUS position. Recheck for sample pulse.
	Sample pulse still not present.	Replace ZD520, ZD305, and ZD518.
Sample pulse is present at ZC520. Place SIGNAL MODE switch in START-STOP position. Synchronize receiver.	Sample pulse not present.	Replace ZD513. Refer to 7730WD, Sheets 5, 7 and 8.
Receiver should be copying data.	Punch is not operating. Sample pulse not reaching module C.	Check wiring for open circuits.

TABLE C

GARBLED DATA

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Operate CHARACTER FEED switch.	Receiver is getting garbled data.	Check reperforator switch positions on module D. Check receiver synchronization, and make sure receiver is getting data from only one source (serial or parallel).
	Trouble in mark or space bit information.	Exchange driver cards with another level. If the fault follows the exchanged card, replace with a new card.
	The fault stays in the bit information.	Replace ZC316 and ZC116. Refer to 7730WD, Sheet 4.
Bit information is good. Operate parallel input with an appropriate test tape.	Parallel input is garbled.	Replace ZC114, ZC115, ZC315, ZC316, and ZC116.
Parallel input is good. Operate serial input with an appropriate test tape.	Serial input is garbled.	Replace ZC316 and ZC116. Refer to 7730WD, Sheet 4.
Compare character shift at ZD305-A27 with bit shift at ZD305-B11 to check the units per character interval.	Character shift, or bit shift information is bad.	Check position of UNITS PER CHARACTER INTERVAL switch. Replace ZD303 and ZD503. Recheck failure. Refer to 7730WD, Sheets 5 and 6.
Units per character interval are good. Check for the last element of the shift register at ZD513-A23.	Input data is not present.	Check polar input data at ZD307-A26. Check for defective wiring or external equipment failure. Refer to 7730WD, Sheets 5 and 8.
Input data is good. Check input data at ZD507-A28.	Input data not present.	Replace ZD507 and ZD307. Refer to 7730WD, Sheets 5, 7, and 8.
	Input data is present.	Replace ZD507, ZD509, and ZD513.
Input data present at shift register.	Garbled data still present.	Replace ZD511, ZD515, and ZD518.

TABLE D

AUTOMATIC SYNC MODE OR MANUAL SYNC MODE FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Check positions of reperforator switches and strapping on ZD517. Operate serial input with the proper idle test pattern. Operate the MANUAL SYNC switch.	Input signal at ZD505-B6 is not present.	Replace ZD303. Recheck failure. Refer to 7730WD, Sheets 5 and 7.
If correct input level is present, operate the MANUAL SYNC MODE switch. One clock period should occur for each operation of the MANUAL SYNC switch.	Positive pulse is not present at ZD505-A10.	Replace ZD505, and ZD507.
If the positive pulse is present, check ZD303-A17 for one clock pulse to be omitted after each operation of the MANUAL SYNC switch.	Pulse is not omitted.	Replace ZD303. Recheck failure. Refer to 7730WD. Sheets 5 and 6.
Operate the AUTOMATIC SYNC MODE (assuming the receiver is not synchronized).	The receiver will not synchronize with transmitter.	Replace ZD303, ZD520, and ZD505.
If receiver synchronizes, check for delayed character shift at ZD505-A11.	Character shift is not present.	Replace ZD520, ZD305, ZD303, and ZD503
After each delayed character shift, a positive pulse should occur for one clock period at ZD505-A10. If a positive pulse is present, the logic is functioning properly.	Pulse does not occur.	Replace ZD505. Refer to 7730WD, Sheets 5 and 6.

TABLE E

CHARACTER SYNCHRONISM FAILURE

PROCEDURE AND NORMAL INDICATION	TROUBLE INDICATION	ISOLATING TROUBLE AND CORRECTIVE ACTION
Check reperforator switch positions on module D.	Input data not present.	Replace ZD307, ZD507, and recheck failure. Refer to 7730WD, Sheet 5.
Operate aerial input with appropriate test message. Check for input data at ZD507-A27. Check for input data at ZD507-A27.	Character synchronism fails with input data present.	Replace ZD303, and ZD505. Repeat last troubleshooting procedure. Refer to 7730WD, Sheets 5 and 6.

HIGH SPEED TAPE RECEIVER MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS), ADJUSTMENTS, AND REMOVAL AND REPLACEMENT OF COMPONENTS

CONTENTS PAGE

1. GENERAL

1.01 This section covers adjustments, and removal and replacement of components. It is reissued to provided the latest changes, engineering information, and to remove preliminary from the title. The lubrication information is removed fro this section and can be found in Section 592-852-731TC. Since this is a general revision, marginal arrows that indicate changes have been omitted.

CIRCUIT CARD IDENTIFICATION

1.02 Circuit card and pin designation references made in the following electronic adjustments are explained below and referenced in Figure 1, showing the wiring side of a typical module. The numbering and lettering system is the same on all modules. For example, assume a reference has been made to circuit card ZC102.

Z - signifies an electronic circuit card.

C - designates module C.

1 - corresponds to the horizontal row in which the circuit card is found in the module. (The single numbers on the vertical side of the fram .)

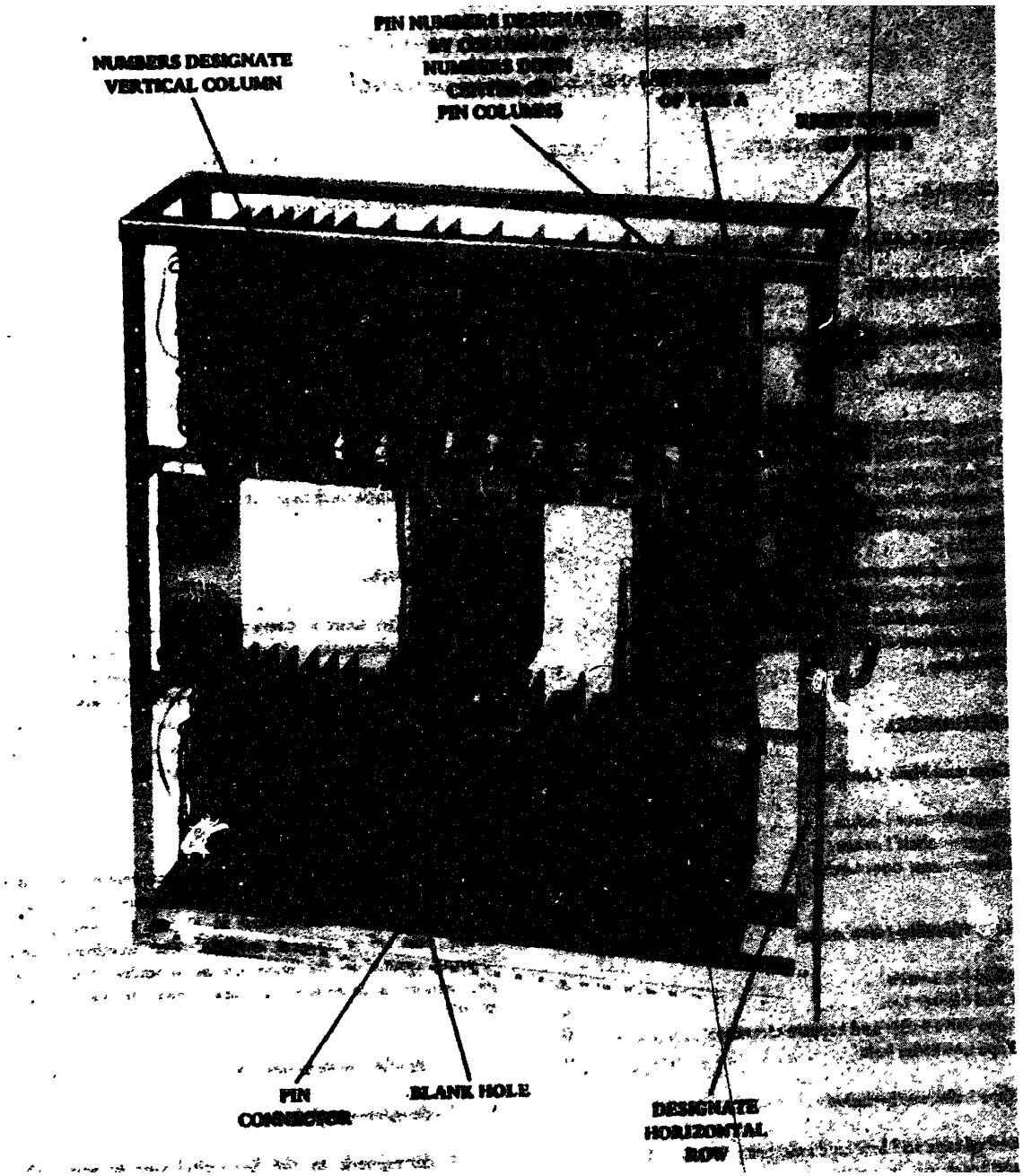


Figure 1- Wiring Side of Typical Module

02 - corresponds to the specific position in that row (directly under the two-digit numbers across the top of the frame and duplicated on the lower part of the frame).

1.03 **Once the card is located, the pin numbers are easily identified. Pin numbers starting with A are in the left column and those starting with B are in the right column (viewed from the wiring side of the circuit card connector). The numbers running down the center identify the pins. For example, pin B6 would be the sixth pin down on the right-hand column.**

1.04 **In some instances, pins are referred to only by number and not preceded by A or B. In these cases, only one pin exists at each level (shown in lower portion of Figure 1).**

1.05 **Each connector will accommodate two sizes of cards (large and small). The large card occupies the entire connector, with the odd numbers on the vertical frame designating the horizontal rows. Therefore, ZC102 would be in the first (top) row, ZC302 would be in the second (middle) row, and ZC502 would be in the third (bottom) row.**

1.06 **The small card occupies half of the connector using all the numbers (1 through 6) on the vertical frame to designate the horizontal row.**

1.07 **The actual electronic adjustments are made on the card side of the modules, with the same numbering system described above.**

1.08 **Use the following equipment to make the necessary electrical, electronic, and mechanical adjustments:**

AC-DC Voltmeter

Oscilloscope with dual trace inputs and dc amplifiers, such a TEKTRONIX 516, 561, or 540 series, or equivalent.

TP315783 tool kit for HIGH SPEED TAPE punch (DRPE)

Note: The following adjustments apply to both receiver assemblies contained in the cabinet. Since both independent assemblies are identical, only one is discussed.

CAUTION: **REMOVE ELECTRIC POWER FROM CABINET BEFORE MAKING MECHANICAL ADJUSTMENTS AND BEFORE REMOVING OR REPLACING CIRCUIT CARDS OR COMPONENTS.**

2. ADJUSTMENTS

ELECTRICAL (AC AND DC)

2.01 **With ac power applied to the receiver cabinet, the** input should be between 103 and **127 volts** measured at terminals 1 and 2, 3, and 4, 5, and 6 on the input terminal board..

2.02 **When checking and adjusting +6 and -6 volts power supply output, place the dc voltmeter leads on pins 16 and 18 on circuit card connector ZC307 and adjust resistor R10 on the power supply regulator card until meter reading is +6 volts ±5% (Figure 2).**

2.03 Place meter leads on pins 16 and 20 on circuit card **connector ZC307 and adjust resistor R16 on the** power supply regulator card until meter reading is -6 volts ±5‰.

2.04 Although the remaining power supply voltages are not adjustable, their readings **should be** within **the following** tolerance **limits:**

(a) Voltage between pins 22 and 31 on circuit card connector ZC118 should read -12 volts ±5%.

(b) Voltage between pins 22 and 23 on circuit card connector ZC418 should read -55 volts ±5%.

(c) Voltage between pins 1 and 5 on circuit card connectors ZC121, ZC122. ZC123, ZC319, ZC320, ZC321. ZC322. ZC323. and ZC324 should **read -5 volts ±5%.**

ELECTRONIC

2.05 Circuit Cards

Note: Check calibration of oscilloscope before making the following adjustments.

MULTIVIBRATOR ZC313, 105 HERTZ and 240 **HERTZ**

(a) Remove circuit card **ZC114.**

(b) Depress "BLANK FEED" or "CHARACTER FEED" momentary switches on control panel. Attach scope lead to pin A34 of ZC313.

(c) Adjust **R101** on circuit card ZC313 until one hertz of the square wave (seen on scope screen) is 9.5 milliseconds ±5% (105 Hz).

(d) Operate toggle switch **CHARACTER FEED OUT** to the ON position (module C). Attach scope lead **to** pin **B27** of ZC313.

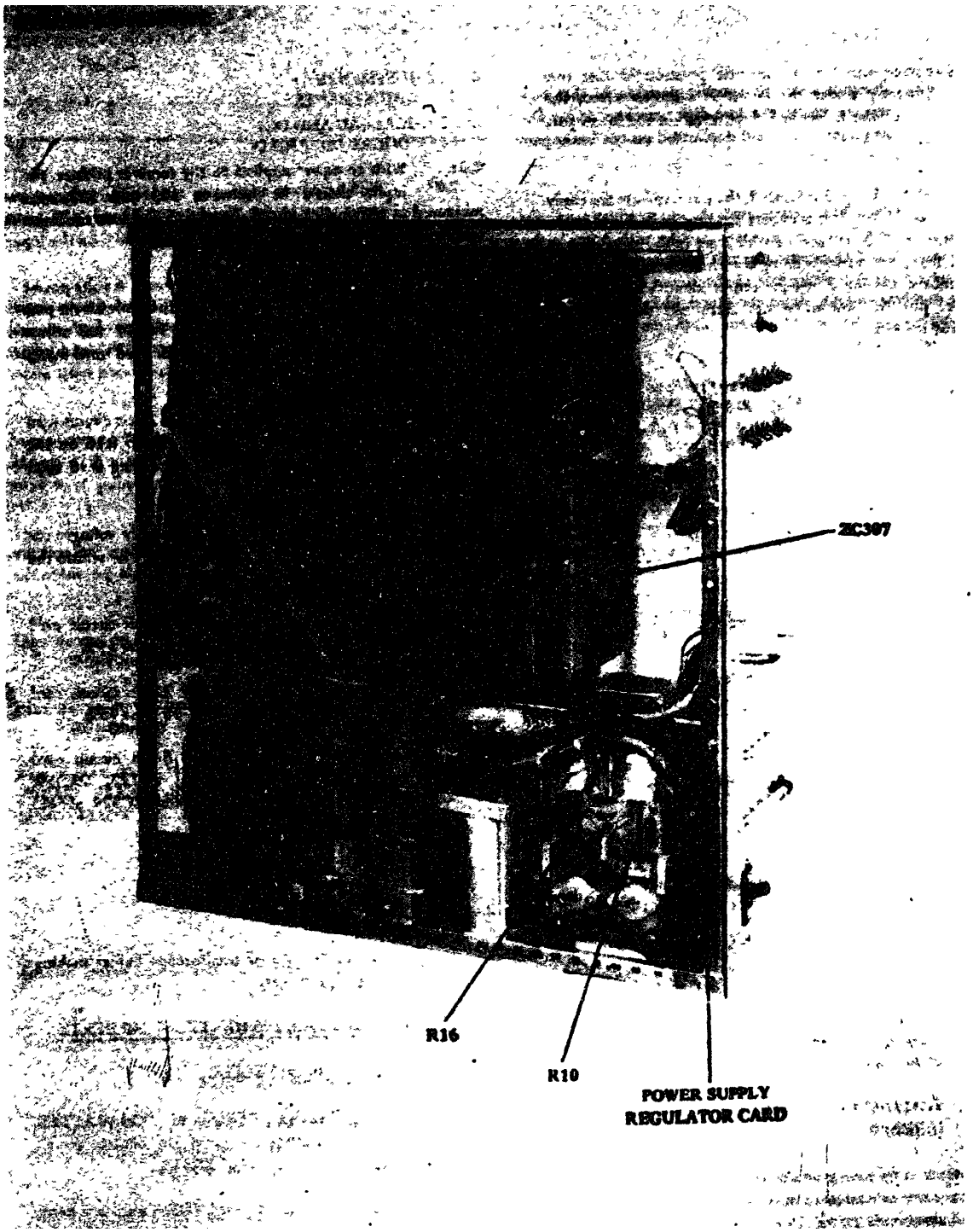


Figure 2 - Module C DC Voltage Adjustment

2.06 **Circuit Cards (continued)**

(e) Adjust R102 on circuit card ZC313 until one hertz of the square wave (viewed on scope screen) is 4.17 milliseconds ±10% (240 Hz).

(f) Replace circuit card ZC114.

GATED OSCILLATOR, ZC120

(a) Before proceeding, set up oscilloscope control switches as follows:

(1) DC couple scope

(2) Vertical - 5 V/CM

(3) Horizontal - 0.2 MS/CM

(4) Trigger - internal, negative

(b) Remove circuit card ZC114.

(c) Operate CHARACTER FEED toggle switch to the ON position (module C). Attach scope lead to pin 13 of ZC120.

(d) Adjust R15 on circuit card ZC120 until negative portion of waveform (viewed on scope screen) is 1.9 milliseconds ±0.05‰. Replace ZC114 circuit card.

MAGNET DRIVER CARDS ZC324, ZC323, ZC322, ZC321, ZC320, ZC319, ZC123, ZC122, and ZC121

Note 1: The new magnet driver cards (TP303730) in module C cannot be adjusted. Use the following adjustments for magnet cards (TP303672) used in earlier modules.

CAUTION: **CHECK ADJUSTMENTS AFTER REPLACING REPERFORATOR OR CIRCUIT CARDS. TURN ALL POTENTIOMETERS TO THEIR FULLY COUNTERCLOCKWISE POSITION, THEN 5 TURNS CLOCKWISE.**

(a) Before proceeding, set up oscilloscope control switches as follows:

(1) AC couple scope

(2) Vertical 5 V/CM

(3) Horizontal -0.2 MS/CM

(4) Trigger-external, positive, on pin 13 of **gated oscillator (ZC120).**

Note 2: When making the following adjustments, ground reference for the scope should be pin 1 or pin 2 on the card being adjusted.

(b) Remove circuit card ZC114. Operate CHARACTER FEED OUT toggle switch to the ON position (module C). Attach scope lead to **pin 32** when adjusting each individual card.

(c) Adjust the potentiometer provided on each card until the output waveform (on scope screen) is 14 volts ±10%..

(d) This peak should fall between the limits of 1.0 and 1.4 milliseconds. shown in Figure 3. Make adjustments with 5 reeds operating. Measure **voltage between the peak and** the **steady voltage** after the peak.

(e) If the waveform does not fall within the limits shown, check gap and bumper adjustments in **Section 592-803-700TC.**

(f) Use the same adjust procedure on each of the remaining circuit cards Replace ZC114.

INPUT CARDS ZD307, ZC114. ZC115, and ZC315

CAUTION: DISCONNECT ALL **EXTERNAL EQUIPMENT FROM RECEIVER CABINET AND REMOVE PAPER** TAPE FROM PUNCH (DRPE).

(a) Move the tape tension arm (on the punch) to the left until the tape puller motor is energized. Devise a method of holding the tape tension arm in this position during the adjustment sequence.

(b) This action provides a 6.3 v ac sine wave **signal above a -6 v dc reference which should** be strapped to the input of each input card.

(c) Adjust each card to provide a circuit switching level symmetrical to a zero volt signal reference (Figure 4).

(d) The circuit under test should switch for input levels of ±0.05 volt to ±0.5 volt.

(e) Use ok connections found in CHART 1 to **make adjustments.**

Note: Use a dual trace input oscilloscope to view the input and **output** signals simultaneously.

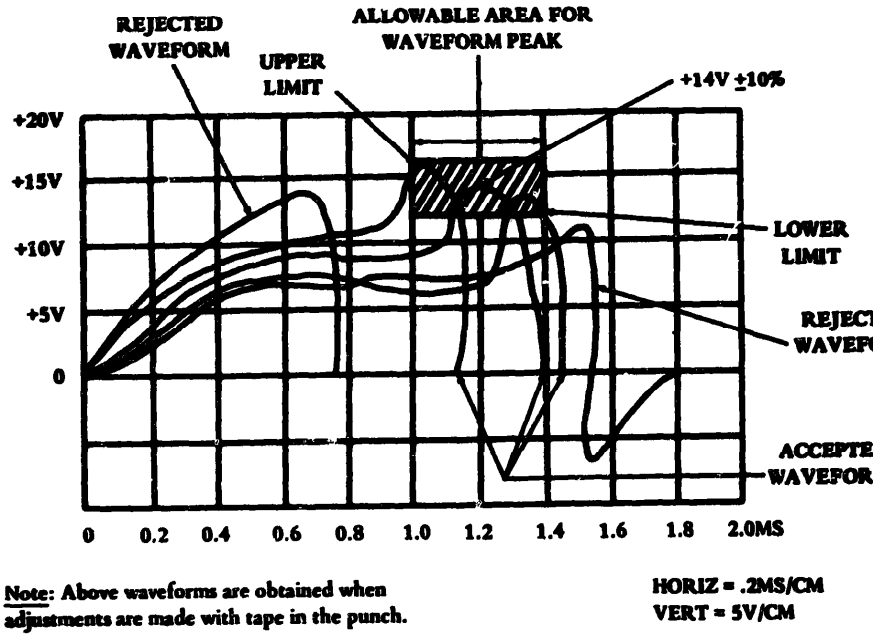


Figure 3- Punch Driver Output Waveform

CHART 1

OSCILLOSCOPE CONNECTIONS

STRAP B13 OF ZC307 TO	TRACE A OF SCOPE ON INPUT PIN	TRACE B OF SCOPE ON OUTPUT PIN	ADJUST POT.	FUNCTION OF INPUT CARD
ZD307-34	ZD307-34	ZD307-32	Lower (R7)	Clock
ZD307-26	ZD307-26	ZD307-22	Middle (R8)	Data
ZD307-11	ZD307-11	ZD307-9	Upper (R9)	Urgent Traffic
ZC114-11	ZC114-11	ZC114-9	Upper (R9)	Aux Sample
ZC315-34	ZC315-34	ZC315-32	Lower (R7)	Aux Bit 1
ZC315-26	ZC315-26	ZC315-22	Middle (R8)	Aux Bit 2
ZC315-11	ZC315-11	ZC315-9	Upper (R9)	Aux Bit 3
ZC115-34	ZC115-34	ZC115-32	Lower (R7)	Aux Bit 4
ZC115-26	ZC115-26	ZC115-22	Middle (R8)	Aux Bit 5
ZC115-11	ZC115-11	ZC115-9	Upper (R9)	Aux Bit 6
ZC114-34	ZC114-34	ZC114-32	Lower (R7)	Aux Bit 7
ZC114-26	ZC114-26	ZC114-22	Middle (R8)	Aux Bit 8

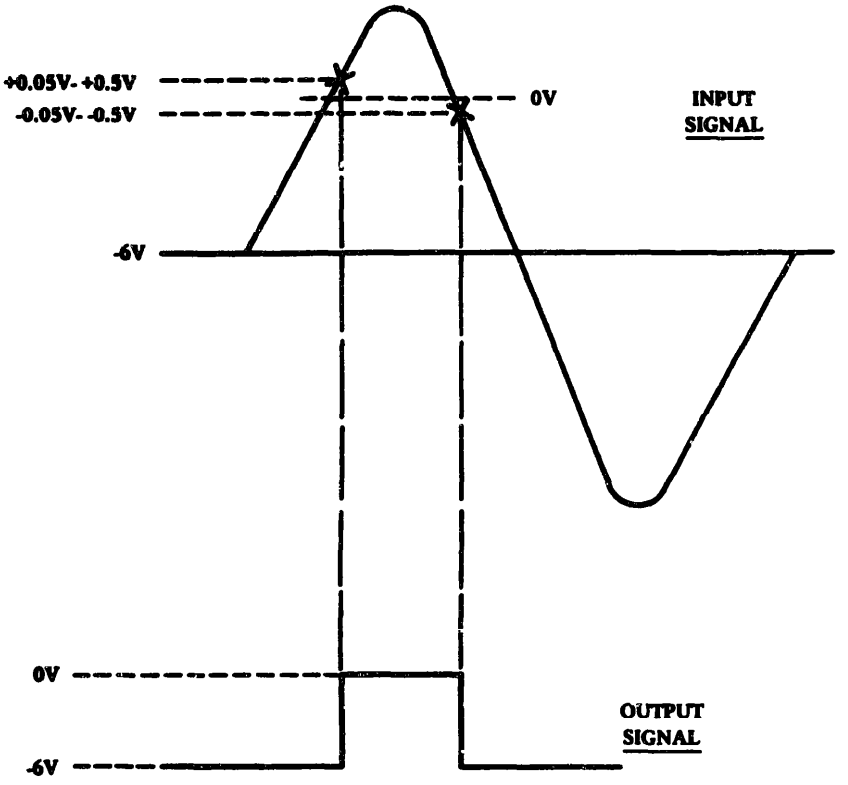


Figure 4- Adjustment of Input Circuit Cards with Sine **Wave** Input Signal

2.07 Circuit Cards (continued)

DELAY ZD305, 110 MICROSECONDS

(8) Remove circuit cards ZD503 and ZC114. Strap pin B27 of ZC313 to pin A24 of ZD303.

(b) Operate CHARACTER FEED OUT toggle switch to ON position (module C).

(c) **Adjust potentiometer** R102 located on ZD305 **until positive** portion of waveform on pin B27 is **110 microseconds.**

(d) Replace circuit cards ZD503 and ZC114 if not **continuing with next adjustment.**

DELAY ZD305, 2 MILLISECONDS

(a) Use same test set up described above. Operate SIGNAL MODE toggle switch to the SYNCHRONOUS position.

(b) Adjust potentiometer R101 located on ZD305 until the positive portion of the output waveform at pin A34 is 2 milliseconds.

(c) Replace circuit cards ZD503, ZC114 and remove strap.

DELAY ZC108, 725 MICROSECONDS

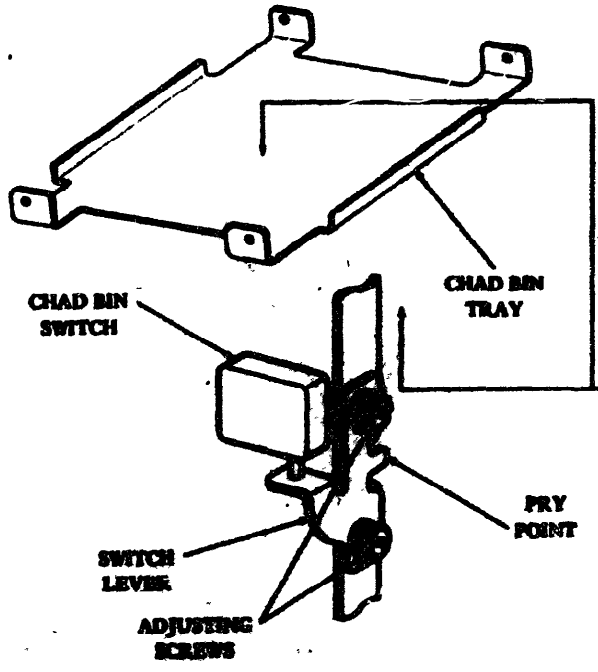
(a) Remove circuit card ZC114. Strap pin A23 to pin A16 on ZC108. Operate CHARACTER FEED out toggle switch to ON position.

(b) Adjust potentiometer R102 located on ZC108 until positive portion of the output waveform on pin B27 is 725 microseconds.

(c) Remove strap and replace circuit card ZC114.

MECHANICAL

2.08 Tape Handling Mechanism



CHAD BIN SWITCH

To Check

Remove chad box from tray. Connect test lamp or meter to terminals of chad level switch. Place push end of 64 ounce scale in center of the tray, push scale down until operation is indicated by the test light or meter.

Requirement

The switch should operate when pressure is applied to the center of the tray.
— Min 36 oz - - - Max 40 oz

To Adjust

Loosen adjusting clampscrews on the switch lever friction tight. Use screwdriver to adjust switch lever to meet requirement. Tighten clampscrews.

CHAD BLOWER BELT

To Check

Visually inspect motor drive belt.

Requirement

The motor drive pulley and the driven chad blower pulley should be vertically aligned.

To Adjust

Loosen the blower mounting plate screws and position blower assembly to meet requirement. Tighten mounting screws.

To Check

Remove belt guard. Use the push end of a 32 ounce scale to apply pressure at right angles to the belt midway between pulleys. Measure belt deflection.

Requirement

Approximately ¼ inch deflection should be measured when 6 ounces of force is applied to the belt.

To Adjust

Loosen the blower mounting bracket screws and position blower to meet requirement. Tighten bracket screws.

2.09 Tape Handling Mechanism (continued)

TAPE UNWINDING BELT

To Check

Apply pressure perpendicularly to the unwinder belt, midway between pulleys using the push end of a eight ounce scale. Measure belt deflection.

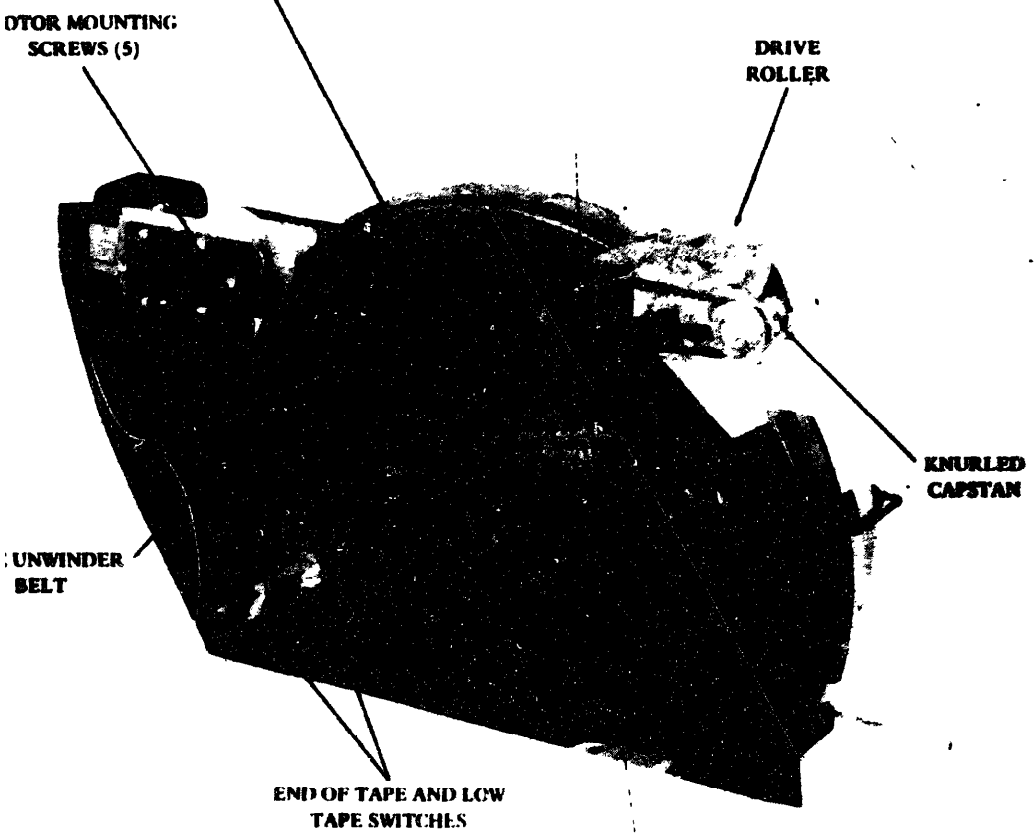
Requirement

With 4-ounces of pressure applied to the drive belt between the two pulleys, the deflection should be

Min ½ inch · · · Max 1 inch

To Adjust

Loosen tape unwind motor mounting screws and position motor to meet requirement. Tighten screws.



2.10 Tape Handling Mechanism (continued)

TAPE DRIVE ROLLER AND CAPSTAN CLEARANCE

Requirement

With drive lever against its eccentric stop, the gap between the drive roller sleeve and knurled capstan should be

Min 0.04 inch to Max 0.08 inch

To Adjust

Loosen eccentric stop locknut and rotate eccentric stop until requirement is met.
Tighten locknut.

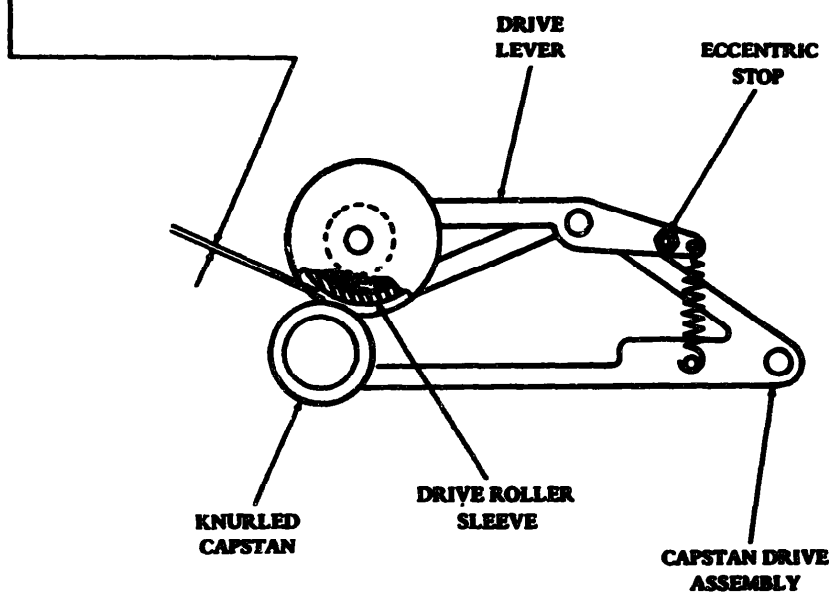


Figure 5- Magnetic Shelf Latch Adjustments

2.12 Door and Shelf Latches (continued)

MAGNETIC DOOR LATCHES

Requirement
All doors should be flush with the outside of the cabinet frame (Figure 5 and 6).

To Adjust
Loosen magnet latch mounting screws friction tight, position latch to meet requirement.
Tighten screws.

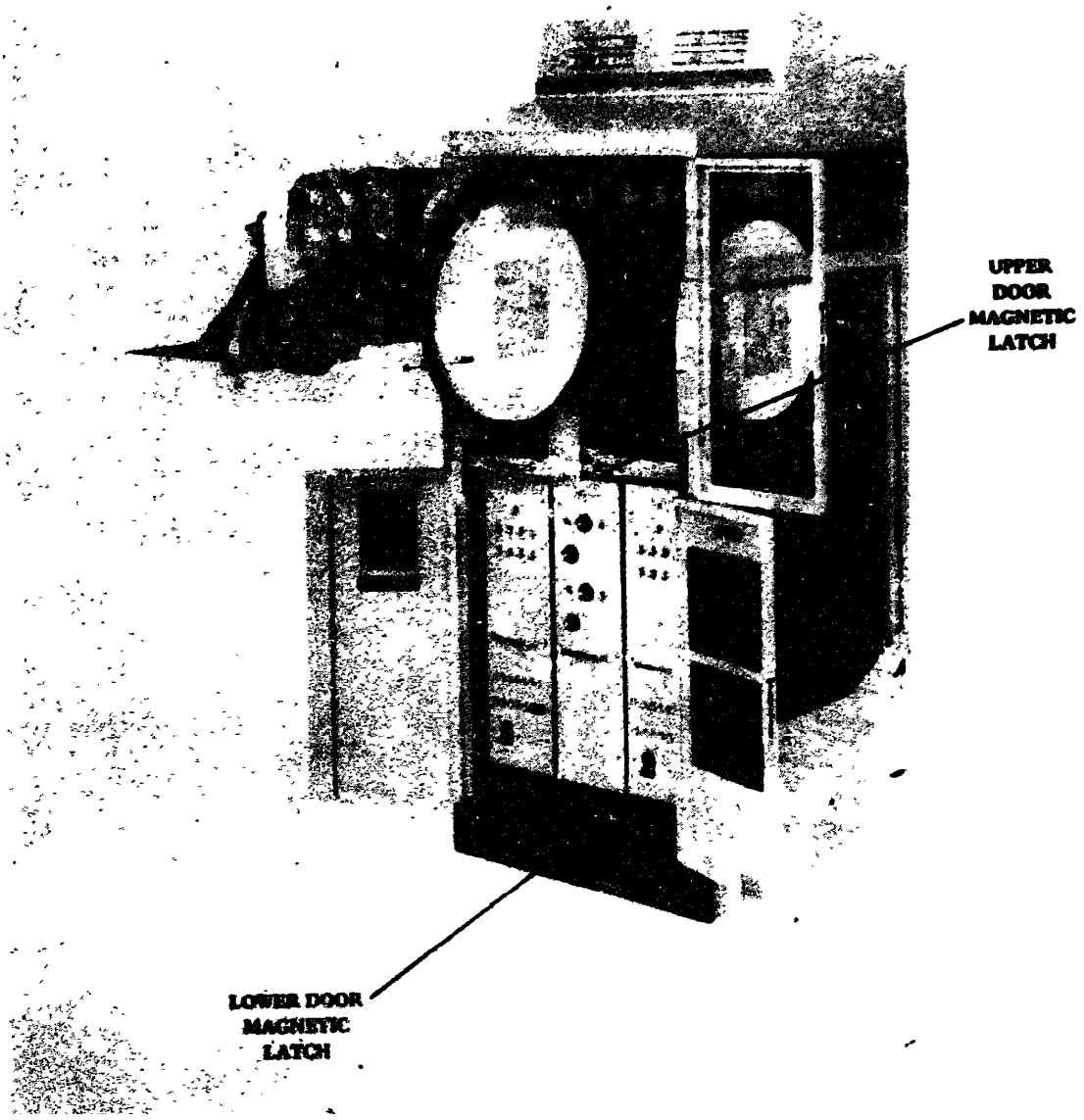


Figure 6- Door Magnetic Latches

2.13 Door and Shelf Latches (continued)

REPERFORATOR DOOR LATCH

To Check

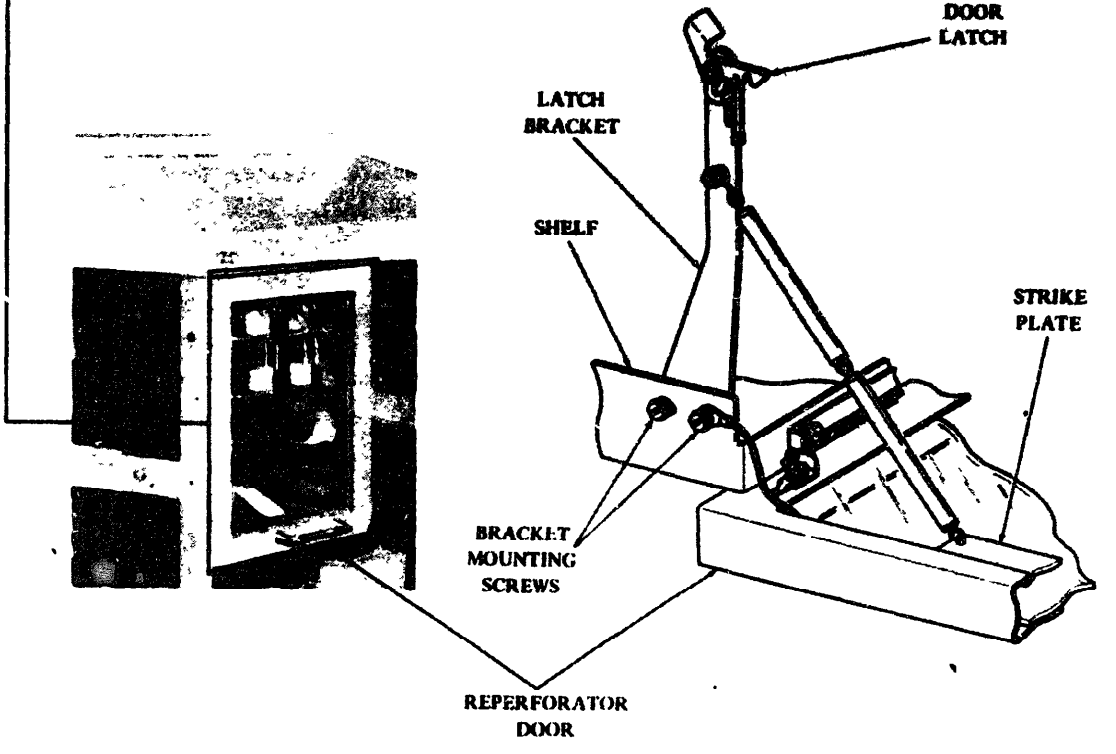
Before adjusting, check back of reperforator shelves to be sure they are against their back stops and held in place by the magnetic shelf latches.

Requirement

Reperforator assembly doors should be flush with the outside of the cabinet frame.

To Adjust

Loosen latch bracket mounting screws (2) friction tight and position bracket to meet requirement. Tighten mounting screws.



2.14 Tape Indicator Switches

END OF TAPE AND LOW TAPE SWITCHES AND BRACKET

Note 1: The switch brackets are mounted differently on the upper and lower shelves because of mechanical interferences on the upper shelf. The lower shelf switch bracket is mounted to the tape container at one end, with the low tape switch clamped to the opposite end and the end of tape switch clamped at the center hole.

Note 2: The upper shelf switch bracket is mounted to the tape container at the center hole of the bracket. The low tape switch is clamped at the same end of the bracket as described in Note 1. The end of tape switch is clamped at the opposite end of the bracket as shown in Figure 7. In both cases, the bracket should be mounted in a horizontal position as gauged by eye with the tape arm resting on the center core in the tape container.

To Check

Remove tape from container. Operate tape arm and visually check position at which mercury moves to closing side of switch. If a more accurate adjustment is necessary, disconnect the associated 14-pin connector and connect a meter or test light to the proper pins on the connector.

Requirement

This requirement may t varied for different applications. When the low tape switch is operated, the low tape indicating light on the control panel should light. A normal operating low tape thickness of 1 inch of tape on the spool is recommended. When the tape-out switch operates, the tape-out indicating light on the control panel should light and the associated tape punch (DRPE) turns off. The normal operating tape thickness for this switch is 1/8 inch from the spool.

To Adjust

Loosen the clampscrews holding switches in place, and position clamps until requirements for both switches are met. Tighten screws.

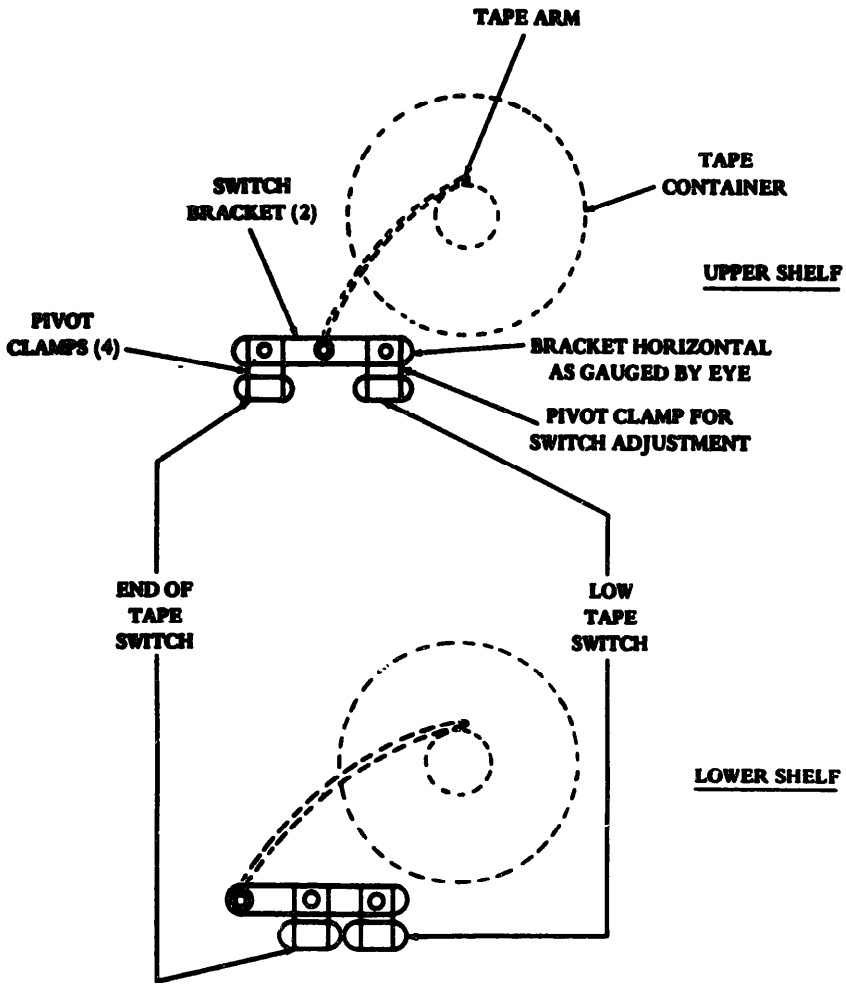


Figure 7- Low **Tape and** End of **Tape** Switch Adjustments

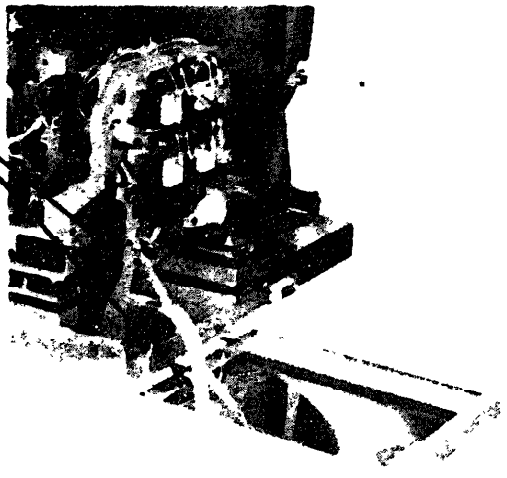
2.15 Tape Indicator Switches (continued)

TAPE CHUTE ALIGNMENT

Requirement
The tape should not bind when passing through the inner and outer tape chutes.

To Adjust
(a) Loosen the tape chute mounting screws at the front of the tape punch, adjust tape chute and tighten screws.

(b) Loosen the tape chute mounting screws on the shelf door and position door tape chute to align with shelf tape chute. Tighten screws.



SPRING TENSIONS

2.16 Tape Unwinder Mechanism

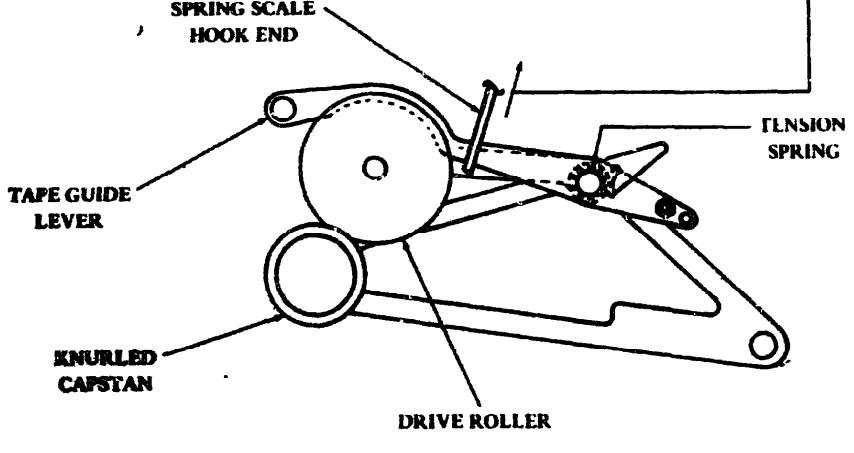
TAPE GUIDE LEVER

To Check
Attach the hook end of an eight ounce spring scale under the lever and pull at right angles.

Note: If springs do not meet their tension requirements they should be replaced.

Requirement
To lift the tape guide lever away from the drive roller it should require
Min 1-1/2 oz - - - Max 2-1/2 oz

To Adjust
Unhook one end of the tension spring and wind or unwind the spring to meet requirement

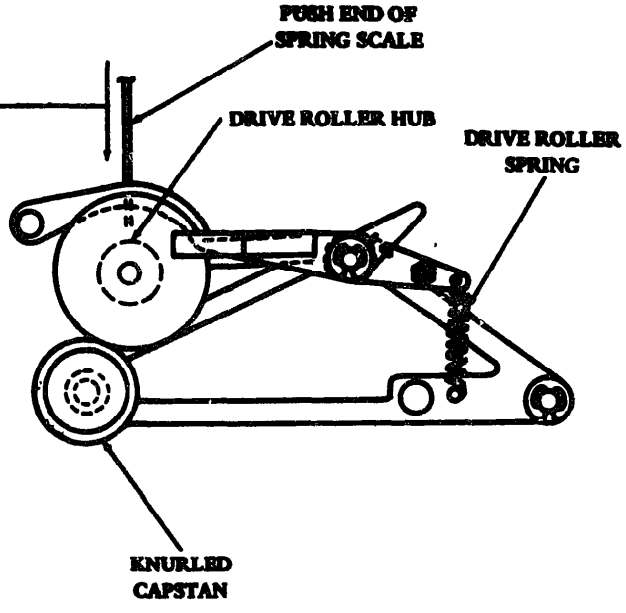


2.17 Tape Unwinder Mechanism (continued)

TAPE DRIVE ROLLER SPRING

Requirement
To engage the drive roller with the knurled capstan it should require a downward pressure of
Min 3 oz - - - Max 5 oz

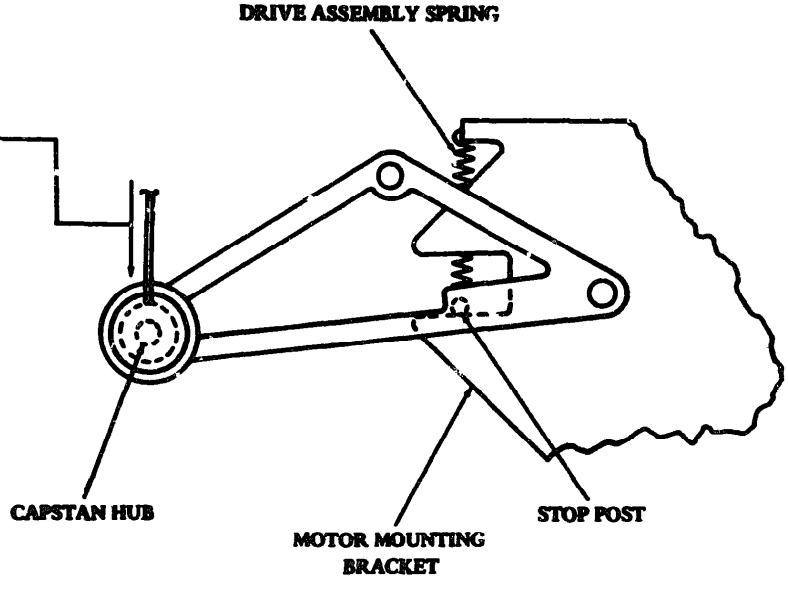
To Measure
Apply the push end of the eight ounce spring scale on the hub of the roller shaft, and push in a line with the tension spring travel.



CAPSTAN DRIVE ASSEMBLY SPRING

Requirement
For the capstan drive assembly to touch the lower limit stop, it should require a downward pressure of
Min 25 oz - - - Max 34 oz

To Measure
Apply the push end of a 64 ounce spring scale to the knurled capstan hub, and push in a line with the tension spring travel.



3. REMOVAL AND REPLACEMENT OF COMPONENTS

Note: Reverse installation procedure when removing components covered in appropriate installation section.

TAPE PUNCH SHELF REMOVAL

3.01 Before removing either tape punch shelf, first disconnect the 3 connectors from the rear of each shelf and open the upper right hand door to its fully open position (Figure 8).

3.02 Pull the shelf to its fully extended position, depress the two locking latches on the inner track of the slides and pull the shelf from the slides while firmly holding the shelf with both hands.

CONTROL PANEL REMOVAL

3.03 Remove the four corner mounting screws, (Figure 9) pull control panel forward, and disconnect both control panel connectors on distribution panel. Reverse procedure for reassembling the control panel to cabinet.

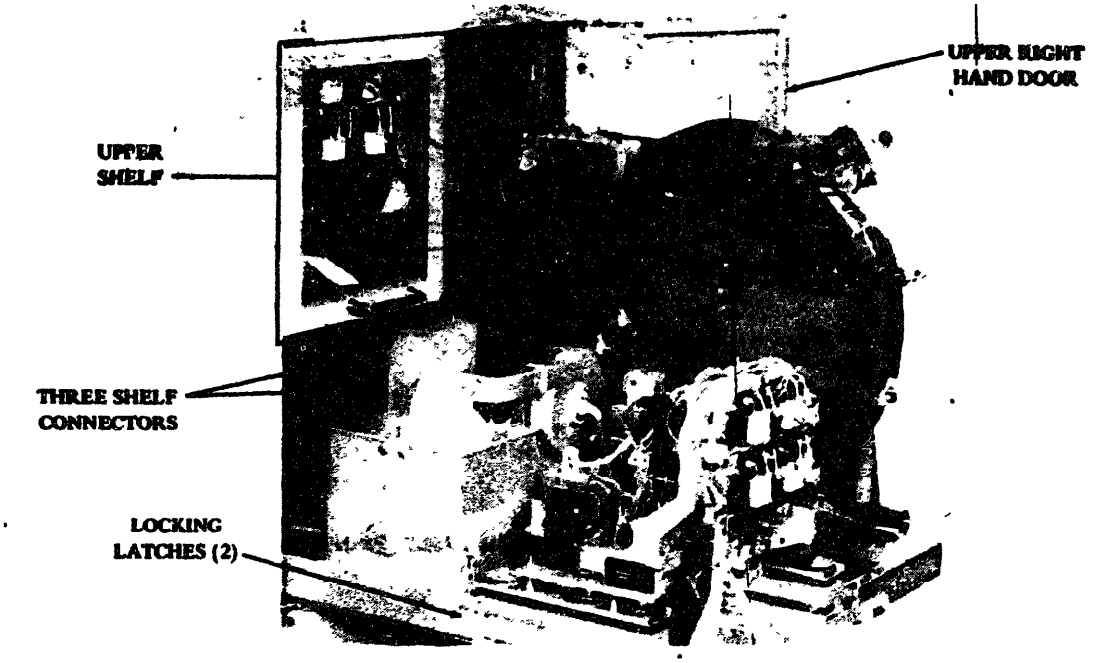


Figure 8- Lower Shelf Fully Extended

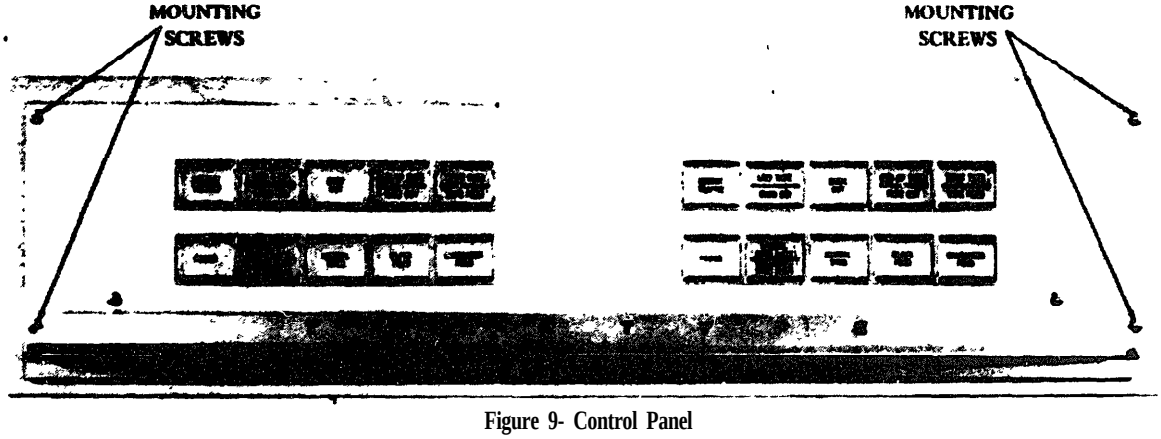


Figure 9- Control Panel

TELETYPE CORPORATION
Skokie, Illinois, U.S.A.

HIGH SPEED TAPE RECEIVER FOR MULTIPLE ADDRESS PROCESSING SYSTEM (MAPS)

LUBRICATION

CONTENTS PAGE

1. GENERAL

1.01 This section provides lubrication information for the high speed tape receiver. It is issued as a separate section for the first time, and includes the latest engineering **information. Previously, the lubrication information** *was issued as* **a** *part of Section 595-852-730TC.*

CAUTION: REMOVE POWER FROM THE CABINET BEFORE LUBRICATING.

1.02 Lubricate the unit prior to placing in **service. After a** *few weeks of service, relubricate to make* **certain** *that all points* **receive lubrication. Thereafter, the regular lubrication interval should be followed.**

1.02 Refer **to Section 592-803-701TC, for high speed tape punch lubricating information, which is used in this receiver cabinet. All spring wicks and felt oilers should be saturated with oil, and friction surfaces** *of all moving parts should be adequately* **lubricated.**

CAUTION: OVERLUBRICATION **WHICH** ALLOWS OIL OR GREASE TO DRIP OR TO **BE THROWN** ON ELECTRICAL **CONTACTS** OR ELECTRICAL **MAGNET MECHANISMS SHOULD BE AVOIDED.**

1.04 The photograph show paragraph numbers *referring to* particular *parts and* **mechanisms on the unit. The illustrations indicate** points to be lubricated, specific instructions, **and type of** lubrications.

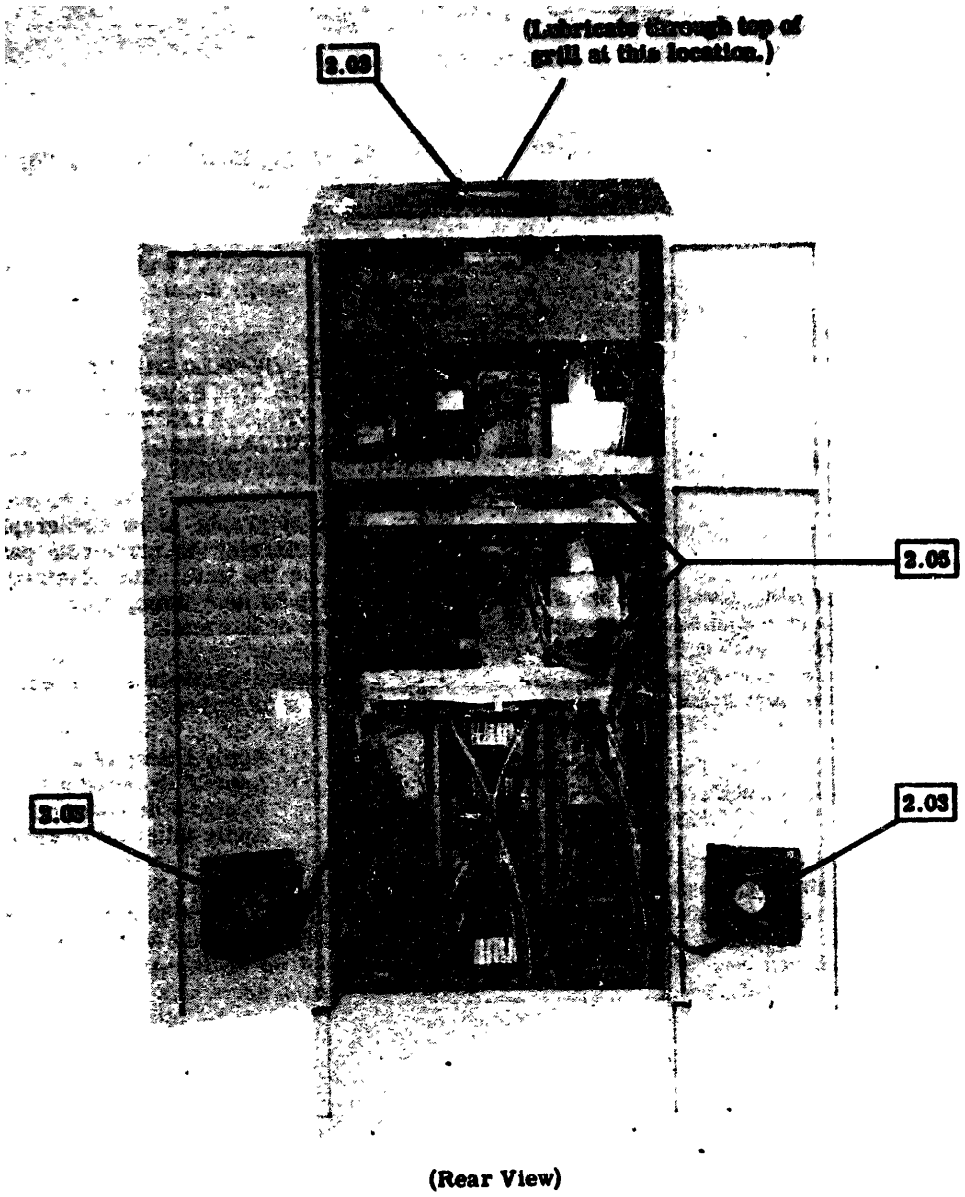
1.05 Lubrication symbols and directions are indicated as follows:

01	Apply **1** drop of oil
02	Apply 2 drops of oil
20	Apply 20 drops *of* oil
G	Apply **thin film** of grease
1/8"	Amount of oil **from injector**

1.05 Use KS7470 oil on points indicating oil, and KS7471 grease where grease is indicated (except on components where a referenced lubrication section is recommended).

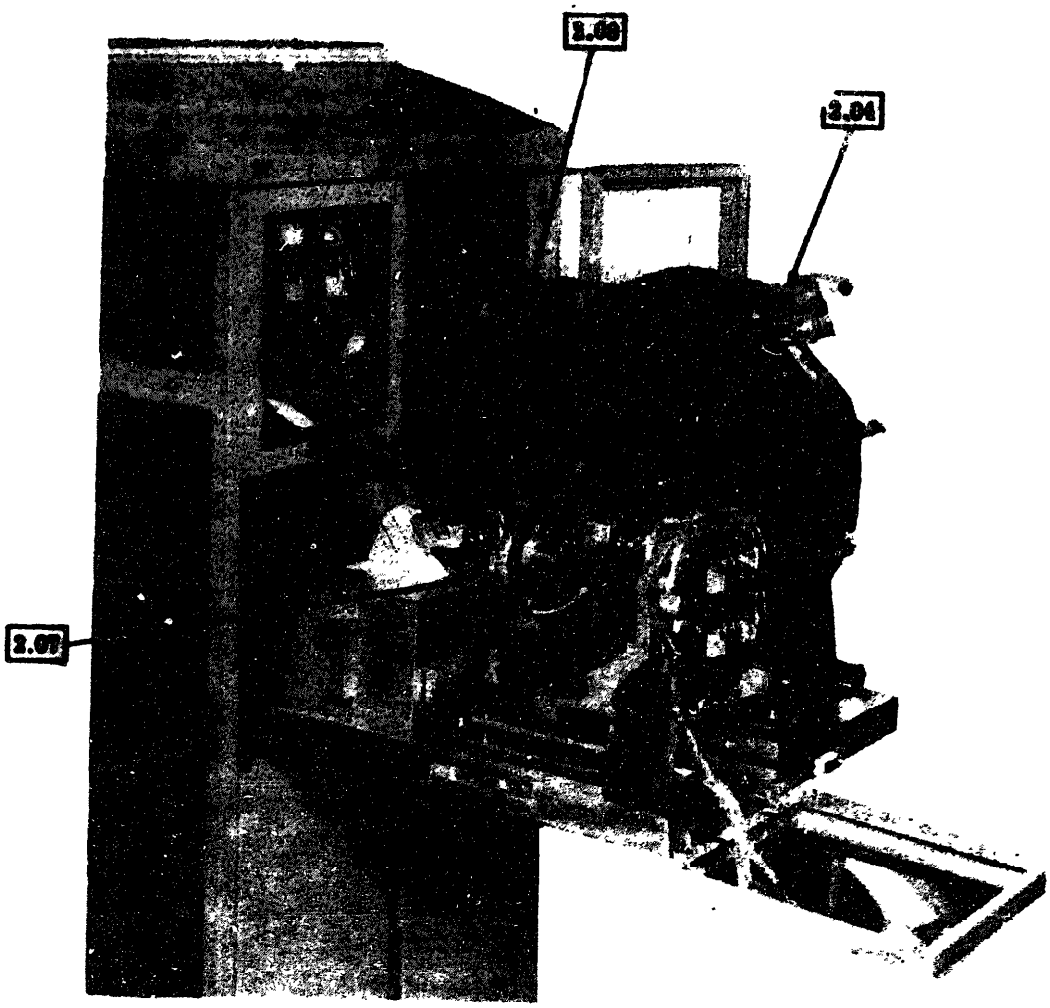
2. LUBRICATION

2.01 Receiver Cabinet



(Rear View)

2.02 Lower Shelf



(Left Front View)

2.03 Cabinet Blower and Exhaust Fans

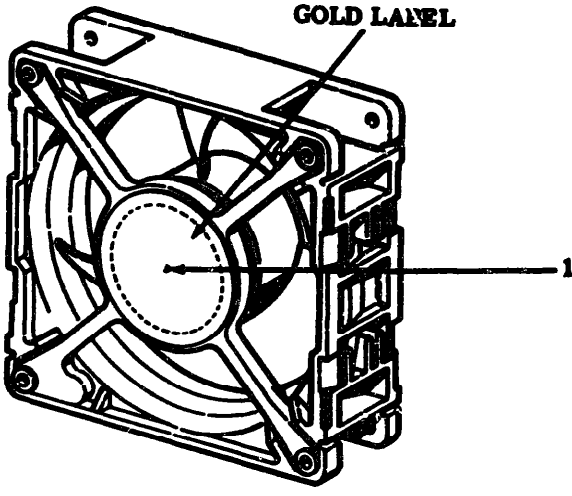
Note: Lubricate cabinet blower and exhaust fans once a year with TP194853 oil injector kit (not furnished, order separately) as follows:

(a) Remove cap from end of oil injector.

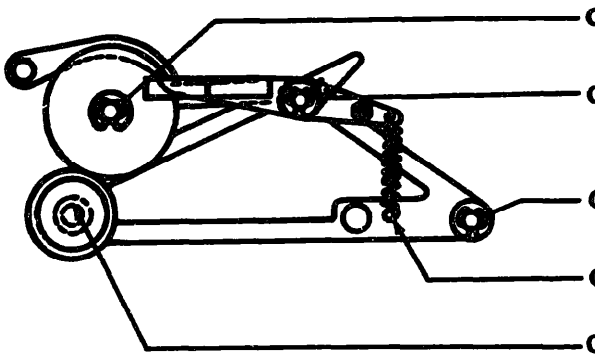
(b) Place injector needle at the center of circle marked on the gold label attached to the fan.

(c) Position needle at a 45 degree angle to the surface of the label. Pierce the circle and the self-sealing rubber seal located under the circle.

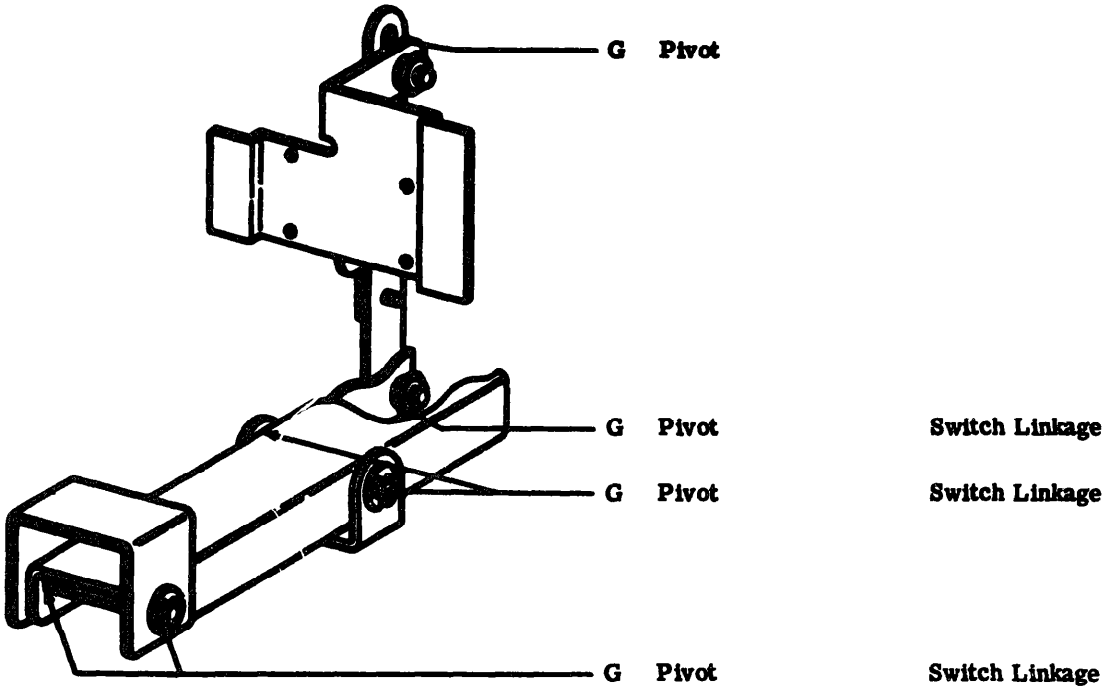
(d) Slowly depress the oil injector plunger, inject approximately 1/8 inch of oil (estimate by eye).



2.04 Tape Unmind Mechanism



2.05 Chad Bin Switch Linkage



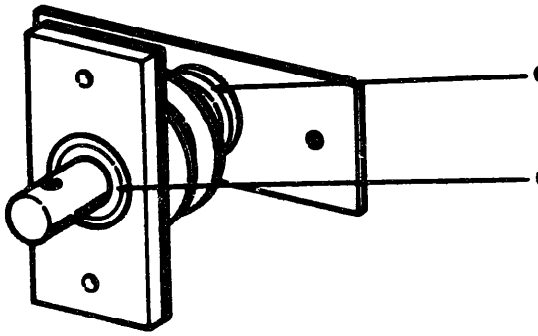
2.06 Maintenance intervals for the above lubrication points are as follows:

SPEED OF OPERATION	*OPERATING HOURS	*TIME
100 wpm	2,000	6 mo
1200 wpm	1,000	4 mo

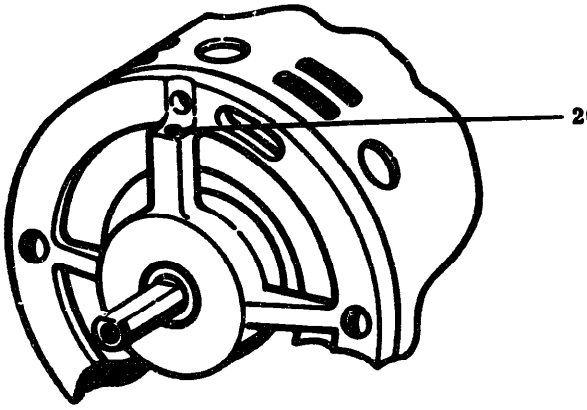
*Whichever occurs first.

2.07 Chad Blower Mechanism

Note: Maintenance interval for the blower mechanism should be 750 operating hours or three months, whichever occurs first.



2.08 Blower Motor

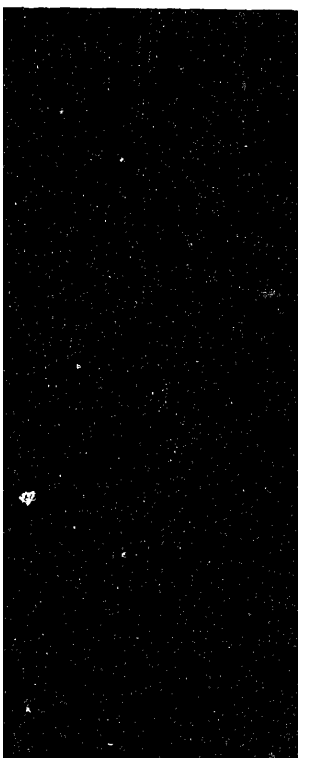


Note: Maintenance interval is the same as indicated in the note in 2.07.

END

11-19-82

DATE



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