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4408 CD

CIRCUIT DESCRIPTION OF THE 419408 COMMUNICATION INTERFACE UNIT CARD ASSEMBLY

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CIRCUIT DESCRIPTION OF THE 410408

COMMUNICATION INTERFACE UNIT CARD ASSEMBLY

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CIRCUIT DESCRIPTION OF THE 410408

COMMUNICATION INTERFACE UNIT CARD ASSEMBLY

Section I - User Information

1. General Description

1.1 The 410408 Communication Interface Unit (CIU) card assembly is an I/O device for the 40C400 Controller that provides an interface to various modems. Operation of the associated modem in either a character and bit synchronous, character and bit asynchronous or character asynchronous, bit synchronous (isochronous) mode is accommodated by means of switch options in the CIU.

1.2 To interface the 40C400 Controller to a data set, the CIU converts data and control information from the line discipline and TTL signal levels of the Telebus to an EIA-RS-232C compatible interface. The exchange of information is accomplished by the operating program in the controller reading or writing data into registers located on the CIU card assembly.

The parallel to serial conversion of the data to be transmitted is performed by the Transmit Buffer. This register indicates its empty/not empty state by a bit in the Status Register (see below) and is double buffered to allow the operating program a full character time for servicing.

The Receive Buffer similarly performs the serial to parallel conversion of incoming data characters. If enabled, an interrupt occurs when a new character has been assembled. Double buffering of the received data allows the program a full character time to service this interrupt.

Send and receive baud rates are the same and are determined by a clock from the data set in synchronous and isochronous operation while one of two crystal oscillators in the CIU is selected under program control to provide either 110 or 1200 baud operation in the asynchronous mode.

The Status Register is interrogated by the operating program for all status information from the CIU. Included in this is the parity of the assembled character and the state of various data set leads. Several internal states of the CIU are also reflected in the bits of this register.

Writing into the Control Register allows the program to control several data set leads directly and set or clear certain internal states of the CIU.

Testing of the CIU from the Telebus interface by an operating program in the Controller is facilitated by providing a data loopback capability.

1.3 Register Programming Information

Although the Telebus has a 16 bit data/address bus, only the lower byte of this 16 bit word is used by the CIU. Address bits A_4-A_7 are switch programmable on the CIU card assembly. To provide additional addressing

1.3 (Continued)

capability, a DEVICE A ENABLE and DEVICE B ENABLE leads are supplied on the Telebus. The CIU is activated for address decoding by a DEVICE A ENABLE only. The addresses and interrupt vectors of the registers are assigned as follows:

REGISTER	ADDRESS (binary)	INTERRUPT VECTOR (binary)
Receive Buffer	A_7 A_6 A_5 A_4 0000	0 A_7 A_6 A_5 A_4 000
Status Register	A_7 A_6 A_5 A_4 0100	None
Transmit Buffer	A_7 A_6 A_5 A_4 1000	None
Control Register	A_7 A_6 A_5 A_4 1010	None

where A_N = Bit N of the device address

As can be seen from the above table, bits 3 to 6 of the interrupt vector are identical to bits 4 to 7 of the CIU address.

2. Features

2.1 Operational Features

(1) Interface to modem is EIA-RS-232C Compatible.
(2) Data rates:
Synchronous or Isochronous: Up to 9600 Baud
Asynchronous: 110 or 1200 Baud under program control
(3) Program interrupt on receive character available.
(4) Double buffering of receive and transmit data.
(5) Parity check and overrun bits provided for receive data.
(6) Data Loopback and Analog Test capability under program control.

2.2 Features Controlled by Switch Options

(1) Synchronous/Asynchronous/Isochronous operation
(2) Half duplex/full duplex operation
(3) Character length of 5,6,7 or 8 bits (synchronous operation with 8 bit characters only)
(4) One or two STOP bits per character (asynchronous and isochronous modes only)
(5) The "Request to Send" lead to the modem maybe permanently enabled or remain under program control.
(6) The "Carrier Detect" lead from the modem may be permanently enabled in the CIU to facilitate interfacing with modems not provided with this lead.
(7) Four switches for address encoding. (Address of the CIU for operation with the 40C400 Controller.)

3. Switch Options

3.1 The following convention is used in the schematic wiring diagram and the circuit description to give a unique designation to each switch.

SPA5-SW4

SP - Refers to switch pack
A5 - Refers to package A5, a unique designation for that package which describes its location on the card assembly.
SW4 - Refers to the fourth switch of package A5

3.2 Detailed description of switch options. (Switch 1 is always oriented towards top of card, irrespective of numbering on switch pack)

ON = SWITCH CLOSED
OFF= SWITCH OPEN

DESIGNATION	FUNCTION	SWITCH STATE (To Enable Function)
SPA5-SW1	Character and bit synchronous systems	OFF
SPA5-SW2 SPA5-SW3 SPA5-SW4	Receiver word length selection	5 Bits: SW2 ON, SW3 OFF, SW4 ON 6 Bits: SW2 ON, SW3 ON, SW4 ON 7 Bits: SW2 OFF, SW3 ON, SW4 ON 8 Bits: SW2 ON, SW3 ON, SW4 OFF
SPA5-SW5 SPA5-SW6 SPA5-SW7 SPA5-SW8	These switches program bits 4 to 7 of the CIU address	SW5 A4, SW6 A5, SW7 A6, SW8 A7 ON = Logic "0"
SPB13-SW1 SPB13-SW2 SPB13-SW3 SPB13-SW4 SPB13-SW5	Factory Test Switches - When opened, these switches isolate MOS outputs MLA8 26,30 and MLA10 11,13,14 from TTL inputs to facilitate factory testing of card.	ON ON ON ON ON These switches must be closed for proper card operation
SPB15-SW1 SPB15-SW2	Transmitter word length selection	5 Bits: SW1 ON, SW2 ON 6 Bits: SW1 ON, SW2 OFF 7 Bits: SW1 OFF, SW2 ON 8 Bits: SW1 OFF, SW2 OFF
SPB15-SW3	2 Stop bits per character (1.5 Stop bits for 5 level Code)	OFF

3.2 Switch Options - continued

DESIGNATION	FUNCTION	SWITCH STATE (To Enable Function)
SPB15-SW4	Character asynchronous systems	OFF
SPB15-SW5	Half duplex operation (blinds receive data when sending)	ON
SPB15-SW6	"Request to Send" to modem strapped permanently ON	ON
SPB15-SW7	"Data Carrier Detect" from modem strapped permanently ON	ON
SPD20-SW1	Factory Test Switch - When switch is open, LOCAL CLOCK on card is isolated from logic for factory test purposes.	ON } This switch must be closed for proper card operation

		SW2	SW3	SW4	SW5	SW6
SPD20-SW2	Character & Bit Asynch.	ON	OFF	OFF	ON	ON
SPD20-SW3	(sets low speed to 110 baud)					
SPD20-SW4						
SPD20-SW5	Synchronous & Isoch.	OFF	ON	OFF	OFF	OFF
SPD20-SW6	(sets loopback test baud rate to 8.448K baud)					

4. Synchronous Communication Interface Unit

4.1 The Synchronous Communication Interface Unit provides the interface between the 40C400 Controller and a modem operating in a character and bit synchronous mode. An 8 bit character consisting of seven ASCII information bits and a parity bit is used. Character synchronization of received data and automatic insertion of SYN characters into transmitted data ("Sync Stuffing") is performed by the CIU under program control.

To unburden the program, automatic control of the "Request to Send" lead (to the modem) by the CIU is provided. This lead is activated by the CIU whenever data or SYN characters are transmitted.

The Communication Interface Unit is addressable in the lower byte of a word only. Address bits A_4-A_7 are switch programmable on the CIU circuit card assembly.

4.2 Status Register - (READ ONLY)

ADDRESS A_7 A_6 A_5 A_4 0 1 0 0

The bits of the Status Register are READ ONLY and are set and cleared by the CIU. Initialization will clear these bits.

Bit	Description
Ø	Receive Character Available - This bit is set by the CIU when the Receive Buffer contains an assembled character. An interrupt request is generated by the CIU at this time if the Interrupt Enable bit is set. This bit is cleared by the CIU when the Receive Buffer is read.
1	Character Parity - This bit indicates the parity of the assembled character contained in the Receive Buffer and is updated by the CIU whenever the Receive Character Available bit is set. A "one" indicates "even" character parity and a "zero" indicates "odd" character parity. This bit is cleared by the CIU when the Receive Buffer is read.
2	Overrun - This bit is set by the CIU when two or more successive characters have been transferred into the Receive Buffer without an intervening sampling of the buffer. This bit is cleared when the Receive Buffer is read.
3	In Sync - This bit is set by the CIU when two consecutive SYN characters have been detected. Synchronism is then established and the Receive Character Available bit is subsequently set for every assembled character. This bit is cleared by the CIU when the New Sync bit in the Control Register is set by the program.
4	Transmit Buffer Available - This bit is set by the CIU when the Data Set Ready lead from the modem is ON and the Transmit Buffer is empty. Transmit Buffer Available is reset by the CIU when the Transmit Buffer is loaded with a character by the program.

4.2 Status Register (READ ONLY) - continued

Bit	Description
5	Carrier - This bit reflects the condition of the Carrier Detect lead from the modem. A "one" indicates a carrier ON state.
6	Ring - This bit reflects the condition of the Ring lead from the modem. A "one" indicates a Ring ON state.
7	Not used

4.3 Receive Buffer - (READ ONLY)

ADDRESS A_7 A_6 A_5 A_4 0 0 0 0

The bits of the Receive Buffer are READ ONLY and are updated by the CIU when a new character has been assembled.

Bit	Description
Ø-7	Receive Data Bits - Data bits 1-8 (MARK is a "1", SPACE is a "0")

4.4 Transmit Buffer - (WRITE ONLY)

ADDRESS A_7 A_6 A_5 A_4 1 0 0 0

The bits of the Transmit Buffer are WRITE ONLY and are set and cleared by the program when a new character is to be transmitted.

Bit	Description
Ø-7	Transmit Data Leads - Data bits 1-8 (MARK is a "1", SPACE is "0")

4.5 Control Register - (WRITE ONLY)

ADDRESS A_7 A_6 A_5 A_4 1 0 1 0

The bits of the Control Register are WRITE ONLY and are set and cleared by the program.

Initialization will clear these bits.

4.5 Control Register - (WRITE ONLY) - continued

Bit	Description
Ø	Interrupt Enable - When set, this bit allows an interrupt by the CIU when the Receive Character Available bit is set.
1	Transmit Sync - When this bit is set, ASCII SYN characters are automatically generated by the CIU to prevent idle intervals between transmitted characters. At the beginning of a "Request to Send"/"Clear to Send" handshaking sequence with the modem, setting this bit causes "Request to Send' (to the modem) to be activated but does not immediately result in the transmission of SYN characters. This "Sync Stuffing" does not begin until the first character has been loaded by the program.
2	Data Terminal Ready - When set, this bit provides a Data Terminal Ready signal to the modem.
3	Loopback - When this bit is set, serial data from the transmitter output is sent to the receiver input of the CIU at 8.448K baud. The CIU is blinded to the Receive Data lead from the modem while the Transmit Data and Request to Send leads to the modem are held at MARK and OFF respectively.
4	Analog Test - When set, this bit activates the Analog Test lead to the modem. If provided with this feature, the modem will then perform an analog loopback of transmitted data to the receiver input. The modem must activate all the appropriate control leads (Clear to Send, Data Set Ready, Carrier Detect) for proper data transfer to occur.
5	Program must clear this bit (Not used in synchronous system).
6	Program must clear this bit (Not used in synchronous system).
7	New Sync - This bit is set by the program to cause the CIU to drop synchronization. The New Sync bit is reset by the CIU when this action has been performed.

4.6 CIU/Modem Interface Lead Description

Signal levels on the CIU/MODEM interface are compatible with the EIA-RS-232C standard.

4.6.1 Transmitted Data

Direction: From Communication Interface Unit

Synchronous serial data from the Communication Interface Unit (CIU) is transferred to the modem on this lead. Data bit transitions will be presented in phase with the positive transitions of the timing signal from the modem. The CIU will hold this lead in a MARKING condition when no data is being transmitted.

4.6.2 Received Data

Direction: To Communication Interface Unit

Synchronous serial data from the modem is transferred to the CIU on this lead. Data bit transitions must be presented in phase with the positive transitions of the timing signal from the modem. The Receive Data lead should be held in the MARKING condition when the Carrier Detect Lead is in the OFF condition.

4.6.3 Transmitter Signal Element Timing (SCT)

Direction: To Communication Interface Unit

This interface lead provides the CIU with signal element timing information for the transmission of data from the CIU. This timing information should be present whenever the modem is in a POWER ON condition.

4.6.4 Receiver Signal Element Timing (SCR)

Direction: To Communication Interface Unit

This interface lead provides the CIU with signal element timing information for sampling of the received data from the modem and should be held ON when the Carrier Detect lead is in the OFF condition.

4.6.5 Control to Modem

Direction: From Communication Interface Unit

4.6.5.1 Data Terminal Ready - The ON condition of this lead indicates that the CIU is ready to transmit or receive data.

4.6.5.2 Request to Send - This lead is turned ON to condition the modem for data transmission.

4.6.5.3 Analog Test - The ON condition of this lead causes the modem to disconnect the transmitter and receiver from the channel and loopback the transmitter output to the receiver input. The modem must activate all the appropriate control leads (Clear to Send, Data Set Ready, Carrier Detect) for proper data transfer to occur.

4.6.6 Control from Modem

Direction: To Communication Interface Unit

4.6.6.1 Data Set Ready - This lead reflects the status of the modem. When ON, this lead indicates that the modem is powered and not in test, talk, or dial mode. The OFF condition is an indication to the CIU to disregard all data from the modem with the exception of the Ring Indicator lead.

4.6.6.2 Clear to Send - This lead indicates to the CIU that the modem is ready to transmit data. When ON, this lead indicates to the CIU that signals presented on the Transmitted Data lead will be sent to the communication channel. The OFF condition is an indication to the CIU that it should not transfer data across the Transmitted Data lead.

4.6.6.3 Carrier Detect - When ON, this lead indicates to the CIU the presence of line signals at the modem receiver. The OFF condition of this lead indicates that no signal is being received or that the received signal is unsuitable for demodulation. With this lead OFF, the CIU will blind the Received Data from the Modem.

4.6.6.4 Ring Indicator- When ON, this lead indicates that a ringing signal is being received by the modem. The OFF condition indicates that no ringing signal is being received on the communication channel.

5. Asynchronous/Isochronous Communication Interface Unit

5.1 The Asynchronous Communication Interface Unit provides the interface between the 40C400 Controller and a modem operating in a character and bit asynchronous or a character asynchronous, bit synchronous mode (isochronous). Character lengths of 5,6,7 or 8 bits with one or two stop bits are accommodated. Operating speeds of either 110 or 1200 Baud may be selected under program control.

To unburden the program, automatic control of the "Request to Send" lead (to the modem) by the CIU is provided. This lead is activated by the CIU whenever data is transmitted.

Send and receive line breaks are accommodated to provide compatibility with low speed systems.

The Communication Interface Unit is addressable in the lower byte of a word only. Address bits A_4-A_7 are switch programmable on the CIU circuit card assembly.

5.2 Status Register (READ ONLY)

ADDRESS A_7 A_6 A_5 A_4 0 1 0 0

The bits of the Status Register are READ ONLY and are set and cleared by the CIU. Initialization will clear these bits.

5.2 Status Register (READ ONLY) - continued

Bit	Description
Ø	Receive Character Available - This bit is set by the CIU when the Receive Buffer contains an assembled character. An interrupt request is generated by the CIU at this time if the Interrupt Enable bit is set. This bit is cleared by the CIU when the Receive Buffer is read.
1	Character Parity - This bit indicates the parity of the assembled character contained in the Receive Buffer and is updated by the CIU whenever the Receive Character Available bit is set. A "one" indicates "even" character parity and a "zero" indicates "odd" parity. This bit is cleared by the CIU when the Receive Buffer is read.
2	Overrun - This bit is set by the CIU when two or more successive characters have been transferred into the Receive Buffer without an intervening sampling of the buffer. This bit is cleared when the Receive Buffer is read.
3	Framing Error - This bit is set by the CIU when the character in the Receive Buffer did not have a valid (i.e. MARKING) STOP bit and is updated by the CIU when the Receive Character Available bit is set. This bit is cleared when the Receive Buffer is read.
4	Transmit Buffer Available - This bit is set by the CIU when the Data Set Ready lead from the modem is ON and the Transmit Buffer is empty. Transmit Buffer Available is reset by the CIU when the Transmit Buffer is loaded with a character by the program.
5	Carrier - This bit reflects the condition of the Carrier Detect lead from the modem. A "one" indicates a carrier ON state.
6	Ring/Receive Break - This bit is set when the Ring lead from the modem is ON or when 16 consecutive bits of SPACING receive line are detected.
7	Supervisory Receive Data - This bit reflects the state of the Supervisory Receive Data lead from suitable modems. When this lead from the modem is ON, the bit is set to a "one".

5.3 Receive Buffer - (READ ONLY)

ADDRESS A_7 A_6 A_5 A_4 0 0 0 0

The bits of the Receive Buffer are READ ONLY and are updated by the CIU when a new character has been assembled.

Bit	Description
Ø-7	Receive Data Bits - Data Bits 1-8 (MARK is a "1", SPACE is a "0")

5.4 Transmit Buffer - (WRITE ONLY)

ADDRESS A_7 A_6 A_5 A_4 1 0 0 0

The bits of the Transmit Buffer are WRITE ONLY and are set and cleared by the program when a new character is to be transmitted.

Bit	Description
Ø-7	Transmit Data Leads - Data Bits 1-8 (MARK is a "1", SPACE is a "0")

5.5 Control Register (WRITE ONLY)

ADDRESS A_7 A_6 A_5 A_4 1 0 1 0

The bits of the Control Register are WRITE ONLY and are set and cleared by the program. Initialization will clear these bits.

Bits	Description
Ø	Interrupt Enable - When set, this bit allows an interrupt to be initiated by the CIU when the Receive Character Available bit is set.
1	Request to Send - When set, this bit activates the Request to Send lead to the modem, indicating that the program has data to transmit. Setting this bit is not required for data transmission. Loading a character into the Transmit Buffer will also initiate a Request to Send for the time interval required to transmit that character.
2	Data Terminal Ready - When set, this bit provides a Data Terminal Ready signal to the modem.
3	Loopback - When this bit is set, serial data from the transmitter output is sent to the receiver input of the CIU. The CIU is blinded to the Receive Data lead from the modem while the Transmit Data and Request to Send leads to the modem are held at MARK and OFF respectively. The loopback baud rate is as follows:

5.5 Control Register (WRITE ONLY) - continued

Bits	Description
	(1) Asynchronous - Loopback testing occurs at the baud rate selected by bit 7 of the Control Register. Baud Rate = 110 or 1200 baud. (2) Isochronous - Loopback testing occurs at 8.448K baud.
4	Analog Test - When set, this bit activates the Analog Test lead to the modem. If provided with this feature, the modem will then perform an analog loopback of transmitted data to the receiver input. The modem must activate all the appropriate control leads (Clear to Send, Data Set Ready, Carrier Detect) for proper data transfer to occur.
5	Send Break - Setting this bit forces the Transmit Data lead to the modem to go SPACING. A Request to Send is not automatically generated.
6	Supervisory Transmit Data - Provides signalling capability on the reverse channel of suitable modems. When this bit is set, the Supervisory Transmit Data lead to the modem is activated (set to ON).
7	Speed Select (1) Asynchronous - This bit selects either one of two data rates. When this bit is set, the low speed option is selected while a cleared bit selects the high speed option. Low Speed = 110 Baud High Speed = 1200 Baud Initialization will clear this bit and thus select the high speed data rate. (2) Isochronous - NOT USED, set to "1".

5.6 CIU/Modem Interface Lead Description

Signal levels on the CIU/Modem interface are compatible with the EIA-RS-232C standard.

5.6.1 Transmitted Data

Direction: From Communication Interface Unit

Asynchronous serial data from the Communication Interface Unit (CIU) is transferred to the modem on this lead. When operating in the isochronous mode,data bit transitions will be presented in phase with the positive transitions of the timing signal (SCT) from the modem. The CIU will hold this lead in a MARKING condition when no data is being transmitted.

5.6.2 Received Data

Direction: To Communication Interface Unit

Asynchronous serial data from the modem is transferred to the CIU on this lead. When operating with synchronous modems (isochronous operation) data bit transitions must be presented in phase with the positive transitions of the timing signal (SCR) from the modem. The Receive Data lead should be held in the MARKING condition when the Carrier Detect lead is in the OFF condition.

5.6.3 Transmitter Signal Element Timing (SCT) - Synchronous Modems Only

Direction: To Communication Interface Unit

This interface lead provides the CIU with signal element timing information for the transmission of data from the CIU (isochronous mode only). This timing information should be present whenever the modem is in a POWER ON condition.

5.6.4 Receiver Signal Element Timing (SCR) - Synchronous Modems Only

Direction: To Communication Interface Unit

This interface lead provides the CIU with signal element timing information for the sampling of the received data from the modem (isochronous mode only) and should be held ON when the Carrier Detect lead is in the OFF condition.

5.6.5 Control to Modem

Direction: From Communication Interface Unit

5.6.5.1 Data Terminal Ready - The ON condition of this lead indicates that the CIU is ready to transmit or receive data.

5.6.5.2 Request to Send - This lead is turned ON to condition the modem for data transmission.

5.6.5.3 Analog Test - The ON condition of this lead causes the modem to disconnect the transmitter and receiver from the channel and loopback the transmitter output to the receiver input. The modem must activate all the appropriate control leads (Clear to Send, Data Set Ready, Carrier Detect) for proper data transfer to occur.

5.6.5.4 Supervisory Transmit Data - This lead is used to modulate the Supervisory Transmit Data Channel of suitable modems.

5.6.6 Control from Modem

Direction: To Communication Interface Unit

5.6.6.1 Data Set Ready - This lead reflects the status of the modem. When ON, this lead indicates that the modem is powered and not in test, talk, or dial mode. The OFF condition is an indication to the CIU to disregard all data from the modem with the exception of the Ring Indicator lead.

5.6.6.2 Clear to Send - This lead indicates to the CIU that the modem is ready to transmit data. When ON, this lead indicates that signals presented on the Transmit Data lead will be transmitted to the communication channel. The OFF condition is an indication to the CIU that it should not transfer data across the Transmit Data lead.

5.6.6.3 Carrier Detect - When ON, this lead indicates to the CIU the presence of line signals at the modem receiver. The OFF condition of this lead indicates that no signal is being received or that the received signal is unsuitable for demodulation. With this lead OFF, the CIU will blind the Received Data lead from the modem.

5.6.6.4 Ring Indicator - When ON, this lead indicates that a ringing signal is being received by the modem. The OFF condition indicates that no ringing signal is being received on the communication channel.

5.6.6.5 Supervisory Receive Data - This lead reflects signal conditions on the Receive Supervisory Data Channel of suitable modems.

6. Supporting Information

6.1 Schematic - 4408 SD

Section II - Circuit Description

1. General

1.1 The voltages required by the 410408 card assembly have the following tolerances:

Voltage	Voltage Range
+12V	+10.8V to +13.2V
+ 5V	+ 4.5V to + 5.5V
-12V	-10.8V to -13.2V

1.2 Other voltages referred to in the circuit description have the following tolerances:

Voltage	Voltage Range
V_L	0.0V to +0.4V
V_H	+2.4V to +5.5V

1.3 Since an integrated circuit package may have a multitude of logic circuits shown separately on the schematic and since they all have the same ML designation, the following convention is used in the circuit description to give a unique designation to each circuit.

MLA6-(8)

ML - Refers to multilogic
A6 - Refers to Circuit Package A6, a unique designation which describes the location of that package on the card assembly.
(8) - Refers to the pin number of the output of the circuit.

Although they contain many complex functions, the MOS integrated circuit packages are shown in the schematic as single blocks.

1.4 Logic Symbols - Positive logic symbols are used in the associated schematic (4408 SD).

1.5 Signal Designation - Signal leads are labeled with a title descriptive of the function of the signal. A line may or may not be drawn over this title, indicating that the signal is in the low (V_L) or high (V_H) state respectively when the state described by the title of the signal is present.

1.6 All signal leads to and from the Telebus have a line drawn over their title. This indicates that the V_L state is the active state and a logic 1 and 0 on the Telebus have a V_L and V_H voltage level respectively.

2. Block Diagram (Figure 1)

2.1 The CIU Block Diagram of Figure 1 shows the relationship between the various functional blocks (FS-1 to FS-9).

Functional block FS-1 interfaces the CIU to the Telebus by providing high impedance receivers and open collector drivers for the Telebus interface leads. The logic for decoding the READ and WRITE commands for the various registers and the address programming switches of the CIU are also in this functional block.

The operating program writes eight bit data into either the TRANSMIT BUFFER (FS-7) or the CONTROL REG (FS-4). Data characters are serialized by the TRANSMIT BUFFER and sent to the data set while the bits in the CONTROL REG provide a means for the program to control the CIU and the data set.

The RECEIVE BUFFER (FS-6) deserializes the data stream from the modem, presents it in parallel format to the DATA OUT MUX, and provides status information of the received data (i.e. vertical parity, overrun information) to FS-5. This STATUS REG functional block provides all status information from the CIU and from the EIA Interface to the Telebus.

When a character has been assembled by the RECEIVE BUFFER, an interrupt may optionally be generated by the CIU. The INTERRUPT (FS-3) block then generates an 8 bit interrupt vector under control of the Telebus line discipline by presenting the vector to DATA OUT MUX (FS-2). This DATA OUT MAX (FS-2) functional block selects the 8 bit data from either the RECEIVE BUFFER, STATUS REG or INTERRUPT logic blocks to pass on to the TELEBUS INTERFACE (FS-1) to be gated out at the proper time.

The OSCILLATOR (FS-9) logic block contains two free running oscillators which provide the high and low speed baud rate clocks for asynchronous operation and the local clock required for loopback testing. Routing of the baud rate clocks and serial data leads for normal operation and for loopback testing is performed by functional block FS-8, SERIAL DATA ROUTING.

3. Detailed Description

3.1 FS-1 Telebus Interface (Refer to TC-3, Telebus Signalling)

3.1.1 General - Functional block FS-1 interfaces the CIU to the Telebus, decodes the address of the CIU card to provide a SELECT signal, and decodes the Telebus controls $\overline{C}_0, \overline{C}_1, \overline{C}_2$ to supply READ or WRITE commands to the various registers. Data, address and control information into the CIU and data, status and interrupt vector information from the CIU are transferred through the bus transceivers MLD5 and MLD6.

3.1.2 Data/Address Lines with Bus Transceivers

All data, control and address information into the CIU and data, status and interrupt vector information from the CIU appear on the eight wires, $\overline{D/A0}$ - $\overline{D/A7}$.

3.1.2 Continued

A V_H on this bus is a logic "0" or SPACE while a V_L is a logic "1" or MARK. The bus drivers of MLD5 and MLD6 are open collector drivers with resistor pull-ups provided externally to the CIU card.

$\overline{\text{OUT EN}}$ is normally V_H, causing bus transceivers MLD5 and MLD6 to act as receivers, transferring bus information to the INØ - IN7 leads. When either the Receive Buffer or the Status Register is read or an interrupt vector is generated, $\overline{\text{OUT EN}}$ changes to V_L, causing bus transceivers MLD5 and MLD6 to output leads OUTØ - OUT7 onto the Telebus.

3.1.3 Telebus Control Decode - (Refer to TC-3, Telebus Signalling)
The six control leads from the Telebus are buffered and inverted by the six bus receivers of MLD1. These leads provide timing and control information for READ, WRITE, LOAD ADDRESS and SEND INTERRUPT VECTOR.

The three control inputs $\overline{C}_0$, $\overline{C}_1$, $\overline{C}_2$ are multiplexed to provide the following functions:

$\overline{C}_2$	$\overline{C}_1$	$\overline{C}_0$	MNEMONIC	FUNCTION
V_H	V_H	V_H	NOP	NO OPERATION
V_H	V_H	V_L	RDV	READ
V_H	V_L	V_H	LAR	LOAD ADDRESS
V_H	V_L	V_L	LAD	LOAD ADDRESS
V_L	V_H	V_H	WW	WRITE
V_L	V_H	V_L	WB	WRITE
V_L	V_L	V_H	NOP	NO OPERATION
V_L	V_L	V_L	NOP	NO OPERATION

When $\overline{\text{BUS EN}}$ is V_L, the control leads $\overline{C}_0$, $\overline{C}_1$, $\overline{C}_2$ and the $\overline{\text{D/A}}$ lines (when they are inputs to the CIU card) are valid. $\overline{\text{BUS EN}}$ is then used as a "sample" signal to clock in this information.

The control leads $\overline{C}_0$, $\overline{C}_1$, $\overline{C}_2$ are decoded by MLC1, which is enabled by $\overline{\text{BUS EN}}$ at a V_L level. The outputs of this decoder are therefore V_L pulses for the duration of $\overline{\text{BUS EN}}$ (approximately 560 ns) when the proper permutation of $\overline{C}_0$, $\overline{C}_1$, $\overline{C}_2$ is provided as an input.

Either the $\overline{\text{LA}}$ or $\overline{\text{LAR}}$ signal being V_L will then cause a V_L LOAD ADDRESS signal on MLC2-6. Whether an address is actually loaded however, is a function of whether the CIU card has been selected (see below).

Similarly either a $\overline{\text{WW}}$ or $\overline{\text{WB}}$ signal being V_L will result in a V_H WRITE Command on MLD2-3. The $\overline{\text{READ}}$ signal is inverted by gate MLB1-(6). The READ and WRITE signals are then gated with a signal indicating whether the CIU card had previously been selected as affirmed by a V_H on MLB5-14. The $\overline{\text{READ SEL}}$ and $\overline{\text{WRITE SEL}}$ signals are therefore V_L respectively when a register in the CIU is being read or written into.

3.1.4 Address Decode and Latch

The high order four bits of the address ($\overline{\text{DA}_4\text{-DA}_7}$) select the CIU card while the low order four bits ($\overline{\text{D/A}_0\text{-D/A}_3}$) select a particular register in the CIU card assembly.

3.1.4 Address Decode and Latch - continued

Switches SPA5-SW5 to SW8 code the CIU card for a particular address. A switch closure is a logic "0" while an open switch is a logic "1". The levels generated by these four switches are then compared by MLB6 against bit D/A4-D/A7 when DEV A EN is V_L. This DEV A EN input is simply an enable from the Telebus to provide additional selection capability over that provided by bits D/A4-D/A7.

Output MLB6-6 then provides a V_H COMPARE signal when a valid comparison is detected. It is important to realize that BUS EN has not been gated in to generate this COMPARE. A free running compare of the high order bits is then reflected in the COMPARE signal, a comparison that is only valid however, when BUS EN is V_L.

The BUS EN signal is used as a clock input on MLB5 to latch in this COMPARE signal and address bits 1-3. Data is clocked in on the low to high transition of BUS EN, when a V_L signal (LOAD ADDRESS) is applied at pin 9.

The SELECT signal being V_H then indicates that the CIU card has been selected and address bits 1-3 have been latched into MLB5. These three address bits select a particular register in the CIU card as follows:

	ADD BIT 3	ADD BIT 2	ADD BIT 1
Receive Buffer	V_L	V_L	V_L
Status Reg	V_L	V_H	V_L
Transmit Buffer	V_H	V_L	V_L
Control Reg	V_H	V_L	V_H

The INIT input is V_L to reset all latches in the CIU. It is used primarily after a power-ON sequence.

3.1.5 WRITE Commands

Decoder MLA3 generates the WRITE commands for the Transmit Buffer and the Control Register. Inputs 4 and 5 are V_L (enabling MLA3) when the CIU card had previously been selected and a WRITE command has now been decoded. Input 6 is V_H (enabling MLA3) when BUS ENABLE is active. Inputs 1, 2 and 3 uniquely select whether the Transmit Buffer or Control Register is being addressed.

Signals W.TBUF or W.CTRL are then V_L signals of approximately 560 NS duration (duration of BUS ENABLE) when the Transmit Buffer or Control Register respectively is being written into.

3.2 FS-2 Data Out Multiplexing

3.2.1 General

The DATA OUT MULTIPLEXING functional block selects one of three input words to present at its outputs. Either the 8 bit STATUS DATA, the 8 bit RBUF DATA (parallel character data from the Receive Buffer) or the interrupt vector is selected to be sent to FS-1 as bits OUT Ø - OUT 7. These bits are then sent to the Telebus at the proper time when $\overline{\text{OUT EN}}$ is V_L

3.2.2 Bits Ø,1,2,7

The GRANT IN signal is V_H when the interrupt vector is generated. This effectively disables MLD9, causing its outputs to be V_L. Bits Ø,1,2 and 7 of the interrupt vector are then generated as logic "0" levels on the Telebus. At all other times MLD9-15 is V_L, enabling the package.

As described in section 3.1.4, address bit 2 determines if the Receive Buffer or the Status Register has been selected. When ADD BIT 2 is V_H the "B" inputs of MLD9 are selected so that STATUS REG information is presented at the outputs. Similarly, when ADD BIT 2 is V_L, Receive Buffer data is selected.

3.2.3 Bits 3,4,5,6

Packages MLD7 and MLD8 are dual 4 in MULTIPLEXERS which function as follows:

INPUT	SELECT B	SELECT A	
C_0	V_L	V_L	INTERRUPT VECTOR
C_1	V_L	V_H	
C_2	V_H	V_L	RECEIVE BUFFER
C_3	V_H	V_H	STATUS REG

Select inputs A and B select one of the four inputs C_0,C_1,C_2 or C_3 to be gated to the output.

$\overline{\text{IV}}$ is V_L when the interrupt vector is generated, thereby selecting the C_0 and C_1 inputs. Bits 3,4,5 and 6 of the generated interrupt vector are therefore bits 4,5,6 and 7 of the CIU card address.

ADD BIT 2 drives the SELECT A inputs of MLD7 and MLD8. When this signal is V_H the Status Reg is selected while a V_L input selects the Receive Buffer.

3.3 FS-3 Interrupt Aribtration

3.3.1 General

The CIU card assembly generates an interrupt vector when the Interrupt Enable bit is set (bit Ø Control Reg) and a new character has been assembled in the Receive Buffer.

3.3.1 General - continued

The INTERRUPT ARBITRATION functional block stores the interrupt request and then generates the interrupt vector under control of the Telebus line discipline.

3.3.2 Operation (See TC-3 Telebus Signalling)

An interrupt is generated only if the INTR EN signal from the Control Reg is V_H, causing output MLC2-11 to be V_H, enabling flip-flop MLC4-(10).

An interrupt request is stored when flip-flop MLC4-(10) is cleared. This occurs when Bit Ø-S of the STATUS DATA changes to V_H, indicating a new character has been assembled in the Receive Buffer. INTR then changes to V_L. If no interrupt grant is then active on the Telebus (INTG IN is V_H), flip-flop MLC4-(6) is set on the next BUS EN cycle, causing INTR on the Telebus to change to V_L. This constitutes an interrupt request by the CIU card. An interrupt grant must now be supplied from the Telebus before further action is taken.

This interrupt grant signal is passed through the various cards of the C400 Controller and is stopped by the first card with an active interrupt request. An INTG IN at V_L would then normally be passed through two gates to drive the INTG OUT signal V_L. When an interrupt request is stored however, INTG OUT is held at V_H, effectively stopping the grant signal from being sensed by the next card.

Once the interrupt grant is received, the next READ command from the Telebus causes the interrupt vector to be generated by means of a V_L signal on $\overline{IV}$. This $\overline{IV}$ signal at a V_L level results in $\overline{OUT\ EN}$ at V_L, causing the data from FS-2 (interrupt vector) to be sent to the Telebus.

A $\overline{READ\ SEL}$ at V_L also causes an $\overline{OUT\ EN}$ at V_L. This occurs when the CIU has previously been selected and has now received a READ command.

The leading edge of $\overline{IV}$ (V_H to V_L transition) resets the interrupt request of flip-flop MLC4-(10) (by setting the flip-flop to a logic "1") while the lagging transition of $\overline{IV}$ (V_L to V_H transition when READ changes to V_L) resets the interrupt request of flip-flop MLC4-(6). The interrupt request to the Telebus is then cleared (INTR V_H) and subsequent interrupt grants would be passed through the CIU card until a new request is generated.

3.4 FS-4 Control Register

3.4.1 General - The eight bits of the Control Register are WRITE ONLY and are set and cleared by the program. These bits enable the program to control the CIU/modem combination. A detailed description of the function of these bits in synchronous, asynchronous and isochronous operation is contained in SECTION I, 4.5 and 5.5 respectively.

3.4.2 All bits of the Control Register are reset to a logic "0" state by a V_L on the INIT lead when the INIT signal from the Telebus is activated (V_L).

A V_L on the W.CTRL lead occurs when the Control Register of the CIU card has previously been selected and a WRITE command has now been decoded. This will cause the data on bits INØ-IN7 to be written into their respective flip-flops of the Control Register on the V_L to V_H transition of W.CTRL. Three of the bits are passed directly to the modem through EIA drivers (package MLD14) as Data Terminal Ready, Analog Test and Supervisory Transmit Data.

For asynchronous operation, MLD10-11 is V_H, enabling the flip-flop and allowing IN7 to provide a LOW SPEED control signal (logic "0" = HIGH SPEED). The SYNC LOSS signal, which is also generated when IN7 is a logic "1", is not used in the asynchronous mode.

For synchronous or isochronous operation, MLD10-11 is V_L, causing MLD10-10 to be V_H irrespective of the state of IN7. This "forced" LOW SPEED indication is used only for loopback testing.

When a "1" is written into bit 7 of the Control Register, one-shot MLA1 is fired. The resultant V_L on SYNC LOSS causes the CIU to drop bit synchronism. One-shot MLA1 will be reset by a V_L on LOSE SYNC after approximately 1 bit duration (send/receive baud rate). The search for the bit pattern to establish new synchronism is started by the CIU when SYNC LOSS and LOSE SYNC are both V_H.

3.5 FS-5 Status Register

3.5.1 General

The eight bits of the Status Register are READ ONLY and are set and cleared by the CIU. A detailed description of the function of these bits in synchronous, asynchronous and isochronous operation is contained in SECTION I, 4.2 and 5.2 respectively.

3.5.2 Status Register Bits Ø to 3

These four bits describe the status of the Receive Buffer. Operation of this circuitry differs for the synchronous, asynchronous and isochronous modes and will be described separately.

a) Asynchronous/Isochronous

In these modes of operation the IN SYNC LATCH does not function as a latch but simply passes the CHAR AVAIL and SYNC SEARCH signals to Bit Ø-S and Bit 3-S respectively. The V_L on the SYNC signal applied to MLB19-10 accomplishes this, resulting in MLB19-8 being V_H at all times and thus not effecting the operation of gates MLC17-(3) and MLC18-(11).

3.5.2 Status Register Bits Ø to 3 - continued

a) Asynchronous/Isochronous - continued

The CHAR AVAIL lead is V_H and BIT Ø-S is therefore set (V_H) when the Receive Buffer has assembled a new character.

Bit 1-S indicates the parity of the character (1=Even Parity) while Bit 2-S is set when two characters have been received without an intervening sampling of the Receive Buffer by the program (i.e. a character has been lost).

In asynchronous and isochronous operation, the SYNC SEARCH lead is a character framing error indication from the Receive Buffer. This lead, and consequently Bit 3-S is set V_H when the assembled character in the Receive Buffer did not have a valid STOP bit.

The $\overline{\text{NO MATCH}}$ signal is not used in these modes.

b) Synchronous

An synchronous operation, character synchronism must be established before character available signals can be sent to the Telebus via BIT Ø-S.

The IN SYNC LATCH is reset (to an "out of sync" state) by a V_L on SYNC SEARCH. This occurs during initialize, when a "1" is written into bit 7 of the Control Register by the program or when the CIU decides it is not in synchronism ($\overline{\text{NO MATCH}} = V_L$). Bit 3-S is then V_L, indicating an "out of sync" state, and the resultant V_L on MLC17-2 prevents Bit Ø-S from being set.

The V_L on SYNC SEARCH also resets the SYNC/ASYNC RCVR MLA8 (functional block FS-6) to an "out of sync" state. When "out of sync", MLA8 does not generate character available signals.

As SYNC SEARCH changes to V_H, the following sync search procedure is initiated. When the first ASCII SYN character is detected by MLA8 (FS-6), MATCH DETECT changes to V_H and the SYNC/ASYNC RCVR is now "in sync". A CHAR AVAIL V_H signal is not generated by this first SYN character but is generated by MLA8 on all subsequent characters until a V_L is again present on SYNC SEARCH.

The IN SYNC LATCH is not set by the first SYN character. If the next character is also a SYN character, the associated CHAR AVAIL V_H signal sets the IN SYNC LATCH by means of a V_L on MLB19-12, sets Bit 3-S (IN SYNC) and BIT Ø-S (CHARACTER AVAILABLE).

If the second character is not a SYN character, a $\overline{\text{NO MATCH}}$ V_L signal is generated by the associated CHAR AVAIL V_H signal. As described in section 3.6, this causes a V_L on SYNC SEARCH, again initiating the complete sync search procedure. Bit Ø-S and Bit 3-S are then cleared and the IN SYNC LATCH is held reset.

b) Synchronous - continued

Although it takes only one SYN character to get the SYNC/ASYNC RCVR MLA8 (FS-6) "in sync" and provide CHAR AVAIL V_H signals, two consecutive SYN characters are required to set the IN SYNC LATCH and pass character available signals to Bit Ø-S.

Bit 1-S and Bit 2-S again indicate character parity and overrun errors, as in the asynchronous mode.

3.5.3 Status Register Bits 4 to 7

Bit 4-S of the Status Register is set (V_H) whenever the Transmit Buffer is empty and Data Set Ready from the data set is ON.

Bit 5-S is set (V_H) when the Carrier Detect signal from the data set is ON or when switch SPB15-SW7 is closed.

Bit 7-S is set (V_H) when the Supervisory Receive Data lead from the data set is ON.

Bit 6-S is multiplexed to provide both RING and RECEIVE BREAK information. Operation differs for the synchronous/asynchronous/isochronous modes:

a) Synchronous

MLC20-15 is held V_L by the V_L level on the $\overline{\text{SYNC}}$ lead. Bit 6-S is then set only when the RING lead from the data set is ON.

b) Asynchronous/Isochronous

In addition to the RING lead from the data set, Bit 6-S can also be set via MLC19-8.

The four bit counter MLC20 counts 16 bits of SPACING receive line, at which time MLC20-15 is V_H, setting Bit 6-S and stopping the counter in that state by the V_L on MLC20-7. The counter and Bit 6-S is reset by a V_L on MLC20-1 whenever a MARKING receive line is detected.

Counter MLC20 is clocked by the XMIT BIT CLOCK rather than the RECV CLOCK. This is of no importance for the operation of the card since send and receive baud rates are always the same.

3.6 FS-6 Receive Buffer

3.6.1 General

The SYNC/ASYNC RCVR MLA8 is a 5,6,7 or 8 bit synchronous/asynchronous/isochronous receiver that deserializes the incoming data stream and presents the parallel data with associated status information at its outputs. SYN character detection, parity check and overrun indicators are some of the major features of this package.

3.6.2 Input Programming

The serial data stream enters MLA8 on the DATA IN lead and is sampled and clocked in by a V_H to V_L transition of RECV CLOCK. In synchronous and isochronous operation a 1X baud rate clock is used while in asynchronous operation a 32X baud rate clock is supplied on the RECV CLOCK lead.

Receiver word length is programmed as follows:

	SPA 5		
	SW2	SW3	SW4
5 BITS	ON	OFF	ON
6 BITS	ON	ON	ON
7 BITS	OFF	ON	ON
8 BITS	ON	ON	OFF

ON = SWITCH CLOSED

Asynchronous and isochronous modes provide a choice of 5,6,7 or 8 bits per character while only the 8 bit option may be used in synchronous systems.

Inputs I_{MHR1} - I_{MHR8} program the ASCII SYN character and consequently only this character is detected as a MATCH CHARACTER by MLA8 in synchronous operation.

The INIT input at V_H resets MLA8 to an "idle" state and sets all data outputs MARKING.

Input I_{CD} (CHIP DISABLE) is held effectively at V_L by R9, enabling MLA8 for operation.

Inputs $I_{\overline{CRL}}$ and $I_{\overline{MHRL}}$ are V_L to enable the word length select inputs and I_{MHRI} - I_{MHR8} (match character program) inputs respectively.

Inputs I_{RMS1}, I_{RMS2} and I_{RMS3} are programmed as follows:

	SPA5 SW1	SPB15 SW4
Synchronous, 1X Clock	OFF	ON
Isochronous, 1X Clock	ON	ON
Asynchronous, 32X Clock	ON	OFF

ON = Switch Closed

The 1X and 32X clock options refer to the fact that the RECV CLOCK signal is one or 32 times the baud rate frequency.

3.6.3 Operation

3.6.3.1 Asynchronous/Isochronous (see TC-1, Typical Data Pattern)

Serial data enters MLA8 on the DATA IN lead and is sampled approximately in the middle of the bit on a V_H to V_L transition of RECV CLOCK. When the START and proper number of data bits have been received, a CHAR AVAIL V_H output is provided by MLA8 in the middle of the STOP bit. The data is

3.6.3.1 Asynchronous/Isochronous - continued

presented on BIT Ø - BIT 7 in right justified format and, since double buffering of the output data is provided, will not change for the duration of the next character time.

Bit 1-S is set if the parity of the assembled character is even and Bit 2-S is set if an overrun condition exists (see below).

Input/Output pin MLA8-28 is an output with an internal pull-up resistor in asynchronous/isochronous operation. The V_L on MLC18-5 causes open collector gate MLA18-10 not to sink any current, thereby allowing MLA8-28 to output onto this lead. A V_H on SYNC SEARCH is an indication that the STOP bit of the assembled character is a SPACE (an error indication).

MATCH DETECT is not used in this mode.

For proper operation, the Receive Buffer is now read by the program before the next character is assembled. One-shot MLA1 is fired and produces a 1 us V_H pulse on MLA1-6 when the Receive Buffer is read. This causes a V_L on inputs $I_{\overline{DRR}}$ and $I_{\overline{SFR}}$, resetting the Receive Buffer and character status information. If another character is received before the Receive Buffer is read, Bit 2-S is set, indicating an overrun condition and consequently a lost character(s).

3.6.3.2 Synchronous (see TC-2, Typical Data Pattern)

Synchronous differs from asynchronous/isochronous operation in that no START or STOP bits are received and consequently character synchronism must be achieved by detection of the ASCII SYN character.

Input/Output pin MLA8-28 is an input in the synchronous mode. A V_L on the SYNC SEARCH input resets the SYNC/ASYNC RCVR MLA8 to an "out of sync" state. In this mode MLA8 does not present any CHAR AVAIL V_H signals and output Bits Ø-7 reflect the serial data stream in a free running manner. A V_L on SYNC SEARCH originates in one of three ways:

a) $\overline{\text{INIT}}$ = V_L, indicating a power on sequence.
b) SYNC LOSS = V_L, indicating the program has told the CIU to drop synchronism by setting bit 7, Control Register.
c) NO MATCH = V_L (see below)

When SYNC SEARCH now changes to V_H, the "sync search" procedure is initiated. The first ASCII SYN character detected causes MLA8 to enter the "in sync" state and present a V_H on MATCH DETECT. The CHAR AVAIL output remains V_L (OFF). Subsequent characters result in a V_H on CHAR AVAIL.

3.6.3.2 Synchronous - continued

If the second character received is also a SYN character, the $\overline{\text{NO MATCH}}$ lead remains V_H and operation of the Receive Buffer proceeds in the same manner as described for asynchronous/isochronous operation. The CHAR AVAIL signal, however, becomes active (V_H) in the middle of the eighth bit rather that the STOP bit.

If the second character is not an ASCII SYN character, as indicated by a V_L on MATCH DETECT, a V_L $\overline{\text{NO MATCH}}$ signal is generated by FS-5. This clears flip-flop MLB18, causing a V_L on SYNC SEARCH for one RECV CLOCK cycle. A new "sync search" procedure is then initiated as described above.

A V_L on the $\overline{\text{SYNC LOSS}}$ signal (bit 7 of Control Register set) also clears flip-flop MLB18. Although $\overline{\text{SYNC LOSS}}$ at V_L directly causes SYNC SEARCH to change to V_L by means of input MLC17-9, flip-flop MLB18 is also cleared to assure a minimum duration of one RECV CLOCK cycle for SYNC SEARCH at a V_L level. As $\overline{\text{LOSE SYNC}}$ changes to V_L, SYNC LOSS is reset to V_H.

3.7 FS-7 Transmit Buffer

3.7.1 General

The SYNC/ASYNC XMTR MLA10 is a 5,6,7 or 8 bit synchronous/asynchronous/isochronous transmitter that serializes the parallel data loaded into its internal buffer on the INØ-IN7 leads when $\overline{\text{W.TBUF}}$ is V_L.

3.7.2 Input Programming

Transmitter word length is programmed as follows:

	SPB15	
	SW1	SW2
5 BITS	ON	ON
6 BITS	ON	OFF
7 BITS	OFF	ON
8 BITS	OFF	OFF

ON = Switch Closed

Asynchronous and isochronous modes provide a choice of 5,6,7 or 8 bits per character while only the 8 bit option may be used in synchronous systems.

Inputs I_{FR1} - I_{FR8} program the ASCII SYN character. In synchronous operation, this character is automatically transmitted as a fill character under certain conditions.

The INIT input at V_H resets MLA10 to an "idle" state and sets O_{TRO} (MLA10-15) to MARK.

3.7.2 Input Programming - continued

Input I_{CD} (CHIP DISABLE) is held effectively at V_L by R11, enabling MLA10 for operation.

Inputs $I_{\overline{CRL}}$ and $I_{\overline{FHRL}}$ are V_L to enable the word length select inputs (5,6, 7,8 bits) and I_{FR1} - I_{FR8} (fill character program) inputs respectively.

Inputs I_{CS1} and I_{CS2} are the clock select inputs:

	I_{CS1}	I_{CS2}	APPLICATION
32X Baud Rate Clock	V_L	V_H	Asynchronous
1X Baud Rate Clock	V_L	V_L	Synchronous/Isochronous

Inputs I_{MS1} and I_{MS2} are the mode select inputs:

	I_{MS1}	I_{MS2}	APPLICATION
One Stop Bit Per Char	V_L	V_L	ASYNCH/ISOCH
Two Stop Bits Per Char	*V_H	V_L	ASYNCH/ISOCH
No Stop Bits	V_L	V_H	SYNCHRONOUS
	V_H	V_H	DO NOT PROGRAM THIS STATE

* 1.5 Stop bits in 5 level code.

Input I_{PI} (PARITY INHIBIT) is V_H to disable the automatic generation of a parity bit. The Transmit Buffer sends all 8 bits loaded on the INØ-IN7 inputs directly, without modfiication for vertical parity.

3.7.3 Operation

3.7.3.1 Asynchronous/Isochronous (see TC-1, Typical Data Pattern)

Characters to be transmitted are loaded into the SYNC/ASYNC XMTR MLA10 on the INØ-IN7 leads when $\overline{W.TBUF}$ is V_L. Double buffering of transmit data is provided in MLA10 to allow the program a complete character time to service the Transmit Buffer.

As the character is loaded, output MLA10-14 changes from V_H to V_L, and consequently Bit 4-S changes to V_L, indicating the Transmit Buffer is full. The character that has been loaded will be transferred to the Transmit Register (internal to MLA10) to be serialized when $\overline{W.TBUF}$ and I_{CTS} are V_H. At this time O_{THRE} and Bit 4-S change from V_L to V_H, indicating the Transmit Buffer is empty and can again be loaded with another character. The START bit of the character being serialized is on the $\overline{DATA\ OUT}$ lead at this time.

3.7.3.1 Asynchronous/Isochronous - continued

The Clear to Send input (I_{CTS}) is V_H when both MLD12-2 and 3 are V_L. Input MLD12-2 is V_L when the Request to Send lead to the modem is held ON by a V_L on MLD12-10, resulting from either the XMIT SYNC bit of the Control Register being set or a character stored in the Transmit Buffer. Input MLD12-3 is V_L when either the Clear to Send lead from the modem is ON or when the LOOPBACK signal is V_H. A Clear to Send signal is thus simulated in the loopback mode (sec. 3.8, FS-8). Input I_{CTS} may be turned OFF (V_L) during transmission of a character without effecting the data stream for that character. However, a character stored in the Transmit Buffer will not be transferred to the Transmit Register, to be serialized, when I_{CTS} is V_L.

Data is clocked out at a rate determined by the frequency of the XMIT CLOCK input I_{TRC} directly (isochronous mode) or at 1/32 times that frequency (asynchronous mode). The SYNC/ASYNC XMTR presents the resultant output baud rate clock on O_{TCO}. The V_L to V_H transition of this output coincides with the bit transitions on O_{TRO}.

Output $O_{\overline{EOC}}$ (End of Character) is V_L during the START and STOP bits and during idle line times.

The serial data stream is present on the $\overline{\text{DATA OUT}}$ lead (MARK = V_L). Since MLB12-12 is V_H in the asynchronous/isochronous modes, a SPACING line is generated when SEND BRK is V_H (i.e. when bit 5 of the Control Register is set).

Flip-flops MLD11-(6) and (10) and associated gates comprise the REQUEST TO SEND CONTROL. When $\overline{\text{RTS}}$ is V_L, the Request to Send lead to the modem is ON (except when in loopback mode).

The primary purpose of this logic block is to automatically activate the Request to Send lead to the modem when data characters are transmitted and thus relieve the program of this function. A means is provided, however, for program control of Request to Send.

When a character is loaded into the Transmit Buffer, output MLA10-14 changes to V_L. Flip-flops MLD11-(6) and (10) are then cleared thru their C_D inputs and $\overline{\text{RTS}}$ is V_L, turning Request to Send to the data set ON. When the Clear to Send is received, the stored character will be transferred into a Transmit Register (internal to MLA10) and begin to be sent serially on pin MLA10-15. Output MLA10-14 then changes to V_H (empty Transmit Buffer), releasing the C_D inputs of flip-flop MLD11.

Since output $O_{\overline{EOC}}$ is V_L during the START bit, flip-flop MLD11-(10) would be set logic "1" thru its J and C_P inputs at the end of the START bit (with the undesireable result of turning Request to Send OFF during transmission of a character), if $\overline{\text{DATA OUT}}$, and therefore MLD12-5, were not V_H during the START bit. Output $O_{\overline{EOC}}$ is not V_L again until the first STOP bit is transmitted, at which time MLD11-(10) is set (Request to Send OFF). Flip-flop MLD11-(6) simply assures that Request to Send is ON long enough for a second STOP bit to be transmitted.

3.7.3.1 Asynchronous/Isochronous - continued

When characters are repeatedly loaded into the Transmit Buffer, Request to Send remains ON (O_{THRE} being "not empty" sets a V_L level on the C_D inputs of MLD11) until the last character has been transmitted.

The program can also control the Request to Send lead by means of bit 1 of the Control Register (XMIT SYNC). When this bit is set (XMIT SYNC V_H), flip flops MLD11-(6) and (10) are cleared, causing $\overline{RTS}$ to be V_L, thereby turning ON Request to Send to the data set.

3.7.3.2 Synchronous (see TC-2, Typical Data Pattern)

Synchronous differs from asynchronous operation in that no START or STOP bits are transmitted, output $O_{\overline{EOC}}$ is V_L during the eighth bit only and a "sync stuff" feature is available.

This feature is activated by setting bit 1 of the Control Register. XMIT SYNC is then V_H, causing Request to Send to the modem and, after a delay in the data set, Clear to Send from the modem to be ON. Before "sync stuffing" occurs, at least one character must be loaded into the Transmit Buffer and sent on the $\overline{DATA\ OUT}$ lead. Subsequently, the SYNC/ASYNC XMTR then automatically transmits ASCII SYN characters as fill characters during idle times as long as its I_{CTS} input is V_H. This assures that there is no idle line time between transmitted data characters, allowing the receiver to stay in synchronism.

3.8 FS-8 Serial Data Routing/Loopback Test

3.8.1 General

Functional block FS-8 routes the serial receive and transmit data, the receive and transmit signal element timing and various EIA control leads to and from the data set for both normal operation and loopback testing.

The loopback test mode is entered from the program by setting bit 3 of the Control Register. In this mode, data entered by the program into the Transmit Buffer is serialized and sent back to the Receive Buffer on the CIU card. SEND DATA and REQ. TO SEND to the modem are held MARK and OFF respectively while a Clear to Send from the modem is simulated. One of the two local oscillators used in the asynchronous mode provides the loopback baud rate clock. Either 110 or 1200 baud may be selected by program control (bit 7, Control Register) with asynchronous operation while 8.448K baud is provided for synchronous or isochronous loopback testing.

3.8.2 Receive and Transmit Signal Element Timing

Package MLB20 is a dual 4 to 1 multiplexer which selects one of four inputs, as determined by its A and B select inputs, to provide one output.

3.8.2 Receive and Transmit Signal Element Timing - continued

In synchronous and isochronous operation, a 1X clock for receive and send data is supplied by the data set on the RECEIVE and TRANSMIT SIGNAL ELEMENT TIMING leads, which are then passed through MLB20 to the RECV. and XMIT CLOCK leads respectively.

In the asynchronous mode or when in loopback test (synchronous, asynchronous or isochronous), the LOCAL CLOCK is selected by MLB20 to appear on both the RECV. and XMIT CLOCK leads.

As mentioned above, the frequency on the RECV and XMIT CLOCK leads is equal to the baud rate frequency in synchronous and isochronous operation while it is equal to 32 times the baud rate in the asynchronous mode.

3.8.3 Serial Data and Control

Package MLB16 is a quad 2 to 1 multiplexer which selects the A or B inputs when the select input S is a logic 0 or 1 respectively. The four outputs of MLB16 are described separately below.

3.8.3.1 $\overline{\text{DATA IN}}$

When not in the loopback mode, serial data from the data set on the RECEIVE DATA lead is passed to the $\overline{\text{DATA IN}}$ lead, which is the serial data input to the Receive Buffer. When CARRIER is V_L, indicating the CARRIER DETECT lead from the data set is OFF, $\overline{\text{DATA IN}}$ is held MARKING.

When the CIU is used in a half-duplex system, it is desireable to blind incoming data when characters are being transmitted to prevent the transmitted data from appearing on the received data lead. This function is performed by MLC16-(4).

Received data is blinded (held MARKING) when both inputs to MLC16-(4) are V_L, resulting in a V_H on MLC16-4. Input MLC16-5 is V_L when REQ. TO SEND to the data set is ON. Switch SPB15-SW5 is closed in half-duplex operation and a V_L is then present on MLC16-6 when ANALOG TST is V_L (OFF).

When in the loopback mode, the $\overline{\text{DATA OUT}}$ signal on input MLB16-3 is gated to output MLB16-4. The serial transmitted data is thus looped back to the serial received data.

3.8.3.2 SEND DATA

When not in the loopback mode, serial transmit data from the Transmit Buffer is sent out on the SEND DATA lead by multiplexer MLB16. In the loopback mode, the ground on input MLB16-6 is gated to output MLB16-7, resulting in a MARK on the SEND DATA Lead.

3.8.3.3 REQ. TO SEND

When not in the loopback mode, a V_L on $\overline{RTS}$ results in the REQ. TO SEND lead to the data set being ON. The V_H on input MLB16-10 is gated to output MLB16-9, turning OFF the REQ TO SEND lead when LOOPBACK is V_H (loopback mode).

Switch SPB15-SW6 may be closed to permanently keep the REQ. TO SEND lead to the data set ON.

3.8.3.4 $\overline{DSR}$

Output MLB16-12 reflects the state of the DATA SET READY lead from the data set when LOOPBACK is V_L. A V_L on $\overline{DSR}$ indicates that DATA SET READY is ON.

The ground on input MLB16-13 is gated to output MLB16-12 when in the loopback mode. A Data Set Ready ON indication is thereby simulated during loopback testing.

3.8.3.5 SPACE/MARK Indicators

Light emitting diodes CR1 and CR2 are ON when a MARK or SPACE respectively is transmitted on the SEND DATA lead. Diodes CR3 and CR4 perform this same function for the RECEIVE DATA lead. When in the loopback mode however, diodes CR3 and CR4 display the data being looped back rather than the state of the RECEIVE DATA lead from the modem.

These indicators provide a visual means of easily detecting an open, idle or busy signal line.

3.9 FS-9 Oscillator Circuits

3.9.1 General

Functional block FS-9 contains two free running crystal controlled oscillators and associated circuitry. When the LOW SPEED signal (bit 7, Control Register) is V_H or V_L, the LOW SPEED or HIGH SPEED OSCILLATOR is selected respectively, divided down and then presented on the LOCAL CLOCK lead.

In asynchronous operation, this LOCAL CLOCK signal is further divided by 32 in the SYNC/ASYNC RCVR and XMTR (MLA8 and MLA10) to be at the send/receive baud rate. The LOW SPEED and HIGH SPEED OSCILLATORS provide clocks compatible with 110 and 1200 baud respectively.

In synchronous and isochronous operation, a 1X baud rate clock for receive and transmit data is supplied by the data set. The LOCAL CLOCK is thus used only in the loopback mode. The LOW SPEED signal is forced V_H (independently of the state of bit 7, Control Register) and thus the LOW SPEED OSCILLATOR is selected. Unlike operation in the asynchronous mode, the LOCAL CLOCK is at the same frequency as the baud rate (8.448K baud).

3.9.2 Detailed Description

The LOW and HIGH SPEED OSCILLATORS are "series resonance" type of oscillators with the crystal in the feedback path. The LOW SPEED signal at a V_L level enables gate MLC22-(13) and disables counter MLC21.

The HIGH SPEED OSCILLATOR output is thereby presented to the input of MLD22. This four bit counter divides the frequency by 16, resulting in a LOCAL CLOCK frequency of 38.4 KHZ.

When the LOW SPEED signal is at a V_H level, gate MLC22-(13) is disabled and counter MLC21 enabled. The 675.84 KHZ signal from the LOW SPEED OSCILLATOR is divided by a number dependent on the state of switches SPD20-SW2,SW3,SW5, SW6 and therefore the levels on MLC21 inputs P_0-P_3.

$$\text{DIVISION FACTOR} = \left[\overline{P}_0+2\overline{P}_1+4\overline{P}_2+8\overline{P}_3\right] +1$$

Where P_0 = Logic Level of P_0 input $\begin{bmatrix} 1 = V_H \\ 0 = V_L \end{bmatrix}$

$\overline{P}_0$ = Inverse of P_0

The output of MLC21 is further divided by 16 in four bit counter MLD22.

FIG. 1
CIU BLOCK DIAGRAM