T.O.33A1-8-771-1

TECHNICAL MANUAL

for

DATA/TELEGRAPH TEST SET ANALYZER

Model DMS-303A

MIL NOM: TS-3378/G

FSN:6625-00-214-8420

CTM-9017

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DMS-303A

ANALYZER

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1. GENERAL

1.01 This manual describes installation, operation, theory, and maintenance of the DMS-303A Analyzer (Fig. 1). A complete listing of replaceable parts and complete schematic coverage are provided at the end of the manual.

(A) Electrical Description

1.02 The Analyzer measures bias and end distortion and detects and counts parity and bit errors present in data signals, of any standard signal level, with bit rates up to 9600 bauds.

Distortion

1.03 For start-stop signals, with code levels of 5, 6, 7, or 8, the Analyzer measures peak distortion, bias, and end distortion. Direct read-out is provided by a front-panel meter, calibrated in per-cent-of-unit interval, and two lamps that indicate whether the distortion is Marking or Spacing. Read-out may be obtained on either all transistions or on selected transitions (first or second or third, etc.).

1.04 For synchronous signals, the Analyzer measures bias and peak distortion.

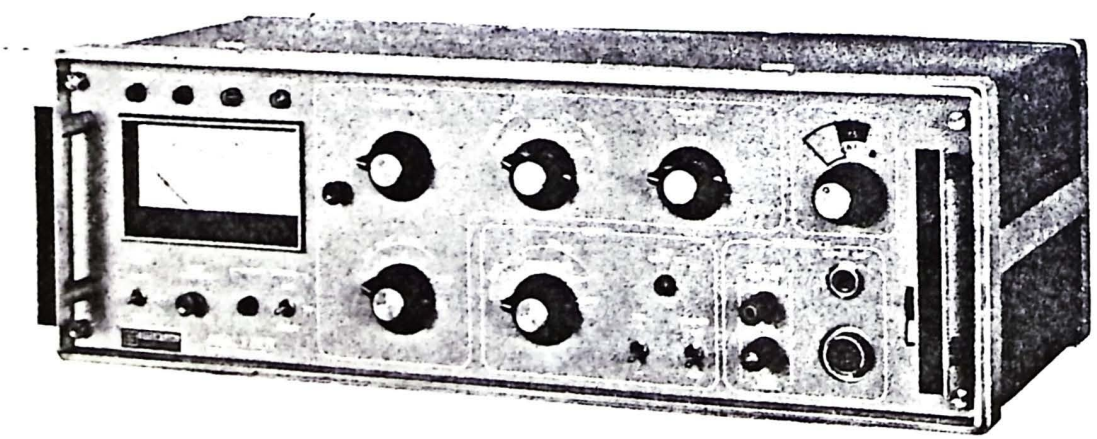


Fig. 1 - Front View - DMS-303A Analyzer

Error Count

1.05 The Analyzer detects errors in either odd or even parity check signals (8-level code start-stop only). A front-panel alarm indicator lamp lights when an error is detected. With optional printed-circuit (PC) cards A3 and A4 installed, the Analyzer also counts parity errors. Bit errors occurring in reversal pattern or in either of the two pseudo random pattern signals may be measured by the Analyzer when equipped with optional A3 and A4 assemblies. (Reversal and either of the two random pattern signals are available from either another Analyzer or from Pattern Generator PG-303A.) The Analyzer counts up to 50 errors per error-count-interval (of either 10^2, 10^3, 10^4, 10^5, or 10^6 bits). A front-panel meter provides direct read-out of the error count, and the interval is determined by the setting of the ERROR COUNT INTERVAL switch. The error count will hold until reset manually or it may be arranged to reset automatically to zero and begin a new count at the end of the selected interval.

(B) Equipment Description

1.06 The Analyzer (Fig. 1 and 2) consists essentially of a chassis housed in an optional portable metal case with removable front and rear covers. The front cover stores the power cord and an optional Data Set Interface Adapter Cable. The chassis mounts nine plug-in PC-cards, one PC-card service extender, two power transformers, a filter capacitor, and front and rear control panels. Frequently used controls and the Data Set Interface connector are accessible on the front panel. Less frequently used controls and accessory connectors are accessible behind the door in the rear cover. Internal adjustments are located on the exposed edge of PC-card A2 directly in front of the removable rear cover.

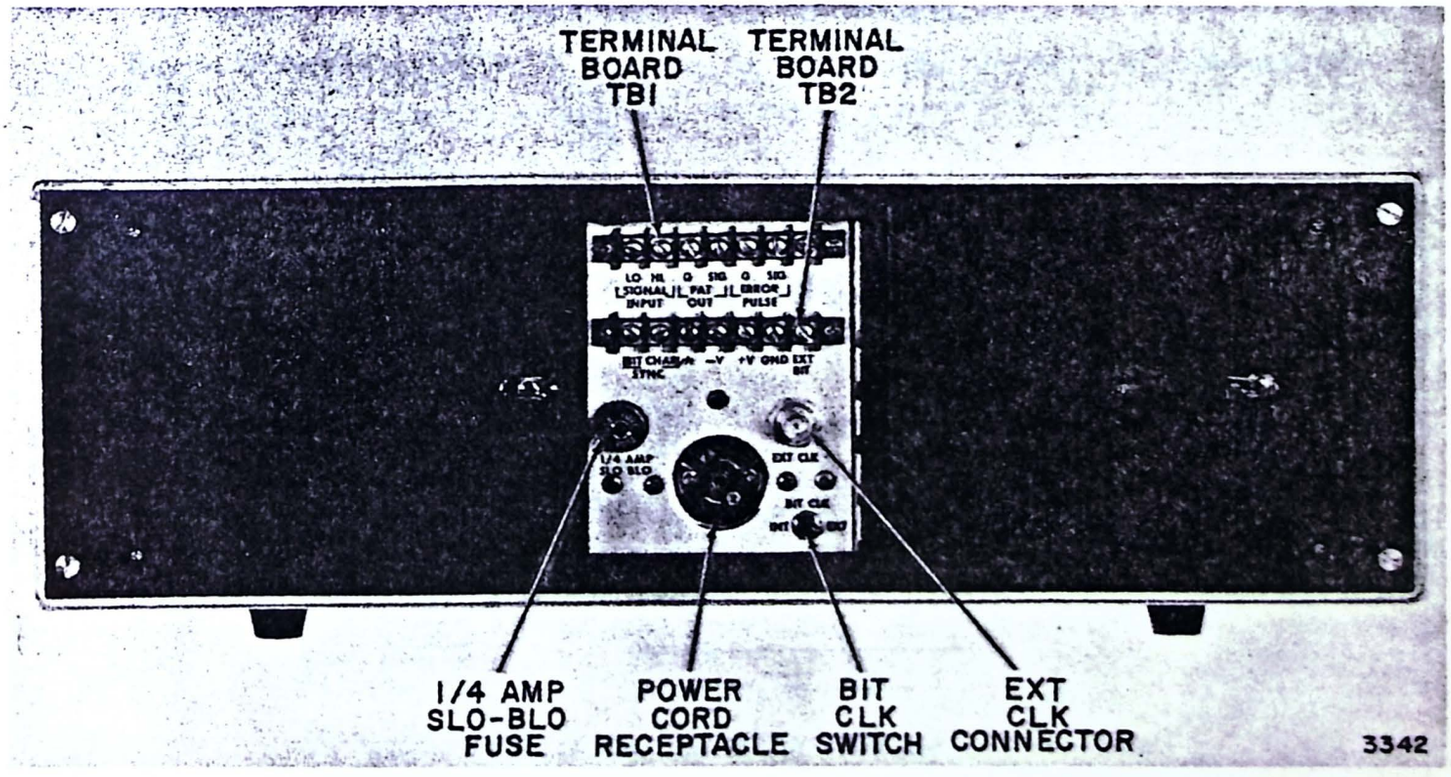
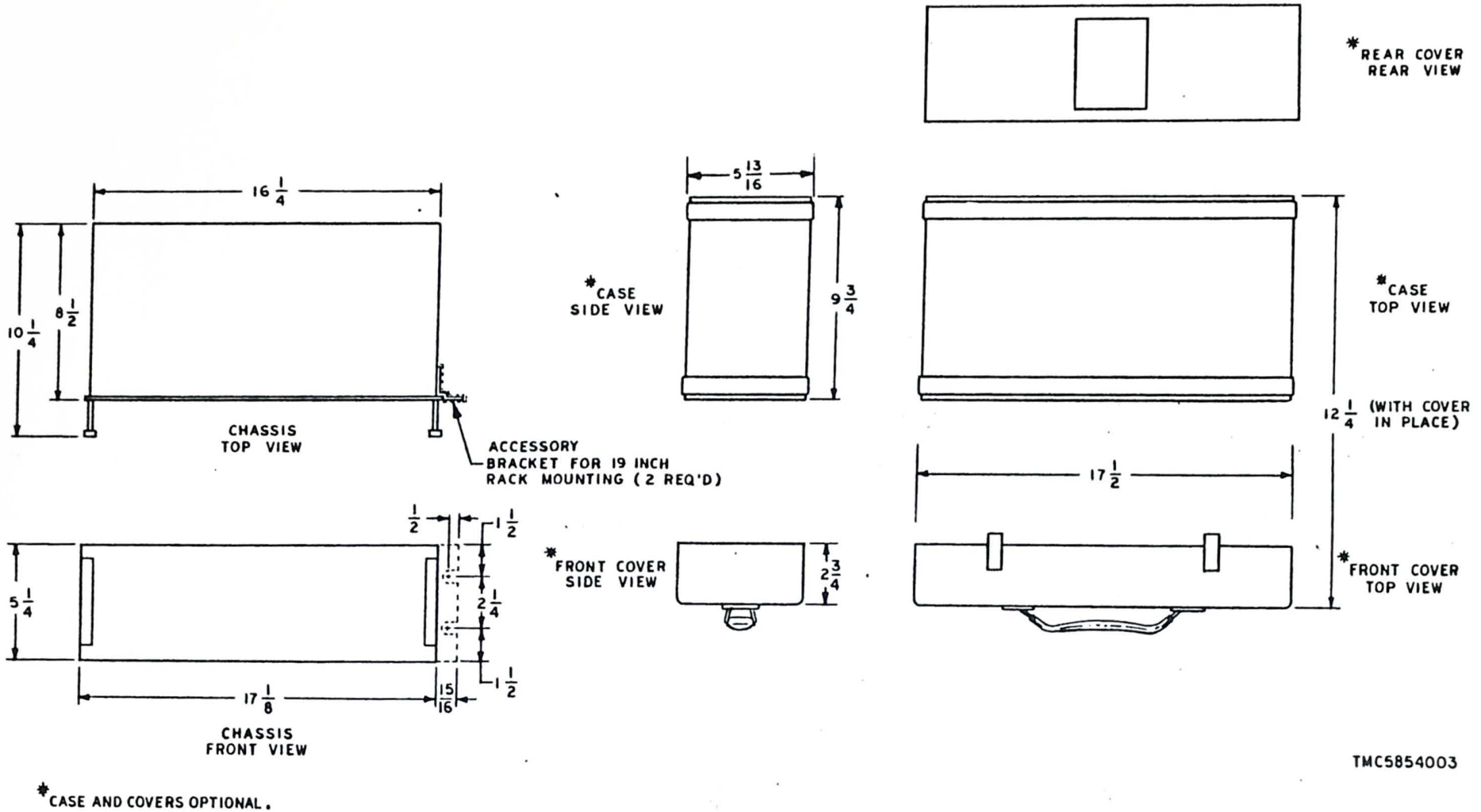


Fig. 2 - Rear View - DMS-303A Analyzer



*CASE AND COVERS OPTIONAL.

Fig. 3 - Outline Drawing - Analyzer and Portable Case

Optional Bit Rates

1.07 A crystal holder (Fig. 34) associated with the internal time-base oscillator is mounted inside the front panel. It mounts the 1.92mHz crystal (Y7) from which the standard 37.5 X 2^n bit rates (including 50 bauds) are derived. The holder also has provisions for mounting six additional crystals (Y1 through Y6) from which to derive any six optional bit rates. The dial plate of the associated BIT RATE switch has blank space on which to write-in or decal optional bit rates installed by the user. Also, the dial plate is easily replaceable so that the user can order sets of optional crystals supplied with a correspondingly marked dial plate. Instructions for adding the optional bit rates are outlined in 4(F) and associated strapping is described in 1.21.

Rack-Mounting

1.08 Although the Analyzer is suitable as a portable instrument when used with optional case, L-brackets (Fig. 3) are supplied to facilitate rack-mounting where permanent installations are required. When the unit is to be rack-mounted, the portable case with front and rear covers is not used.

Separable Items Supplied

1.09 Table I lists the separable items that constitute Analyzer DMS-303A. Table I may be used as a check-list to determine if equipment is complete.

TABLE I

SEPARABLE ITEMS SUPPLIED

QUANTITY	ITEM
1	Chassis
1	Portable metal case (optional)
1	Removable front cover (optional)
1	Removable rear cover (optional)
1	Power cord
2	Technical manual
1	Data Set Interface adapter cable (optional)
2	L-brackets with screws
1	PC-card A1, time-base circuits
1	PC-card A2, power supply circuits
1	PC-card A3, bit error circuits (optional)
1	PC-card A4, error counter circuits (optional)

TABLE I (Cont'd)

QUANTITY	ITEM
1	PC-card A5, input, transfer, and parity error circuits
1	PC-card A6, D/A converter circuits
1	PC-card A7, sync circuits
1	PC-card A8, distortion register circuits
1	PC-card service extender A9
1	PC-card A10, distortion counter circuits
1	Crystal Y7 (1.92mHz)
6	Crystals Y1 through Y6 (optional)
1	BIT RATE-switch dial (37.5×2^n (including 50-baud) markings)*
1	BIT RATE-switch dial with 37.5×2^n markings and optional bit-rate markings (optional)

*Item not supplied when unit is shipped with optional crystals Y1 through Y6 and optional dial.

(C) Performance Specifications

1.10 Table II outlines the specifications applicable to the Analyzer.

TABLE II

PERFORMANCE SPECIFICATIONS

ITEM	DESCRIPTION
Circuit	Solid-state, integrated.
Weight	18 pounds (with portable case).
Outside Dimensions, Including Extending Hardware	Portable: 12-3/4 inches high by 5-13/16 inches wide by 17-1/2 inches deep.
	Rack-mounted: 10-1/4 inches high by 5-1/4 inches wide by 19 inches deep.
Input Power	115/230-volt ac, 60Hz, 10, 20 watts.
Input Data Signals Accepted	5-, 6-, 7-, and 8-level (code) start-stop, or synchronous.

TABLE II (Cont'd)

ITEM	DESCRIPTION
Input Data-Signal Levels Accepted	20ma neutral. 60ma neutral. 10/30ma polar. EIA (RS-232B). Hl-Z (50k-ohm bridge polar). HUB (+60-volt Mark, -30-volt Space).
Input Data-Signal Bit Rates Accepted	37.5, 50, 75, 150, 300, 600, 1200, 2400, 4800, 9600 bauds, using internal time-base range A. Six optional bit rates up to 9600 bauds, using internal time-base range B. Any bit rate up to 9600 bauds, using external time base.
Distortion Components Measured	Peak (Marking or Spacing). Bias (Marking or Spacing). End (Marking or Spacing).
Distortion Read-Out Accuracy	±2 per cent.
Bit and Parity Error Counter Range (Optional)	Zero to 50 errors per error-count interval of 10^2, 10^3, 10^4, 10^5, 10^6 or infinite bits.
External Time-Base Signal Required	Polar, ±6 volts, square-wave, with frequency at 200 times bit rate of input-data signal under test.
External Bit Sync Signal Required	+6-volt square-wave, with frequency at 1 times bit rate of data signal under test.
Pseudo Random or Reversal Pattern Signal Output	±6-volt polar.
Error Pulse Signal Output	+5-volt square pulse.
Bit Sync Signal Output	+5-volt square-wave.
Character Sync Signal Output	+5-volt square pulse.
Automatic Reset	Resets read-out every five seconds when measuring peak distortion and five seconds after end of error-count interval when counting parity or bit errors.
Filter	Switch connectable to remove transients from input signal under test.

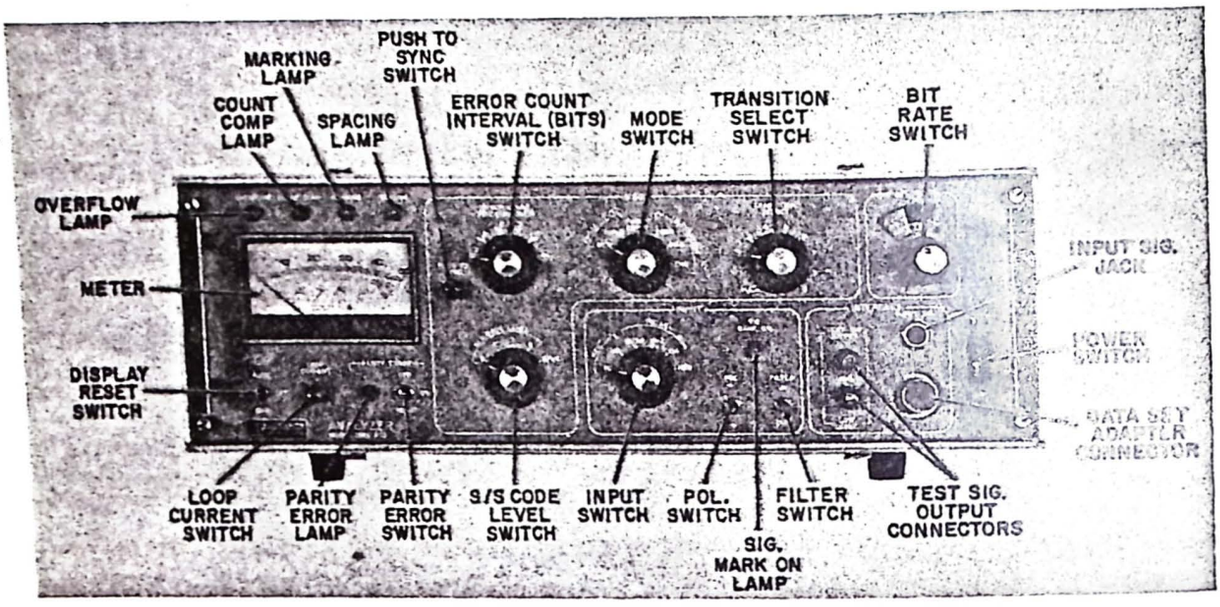


Fig. 4 - Front View - Analyzer Controls and Indicators

(D) Description of Controls and Indicators

1.11 All operating controls and indicators are shown in Fig. 4 and described in Table III.

TABLE III

CONTROLS AND INDICATORS

NAME AND TYPE	CIRCUIT DESIG.	CONTROL POSITIONS	FUNCTION
POWER - 2-position toggle switch with red indicator lamp in handle	S6	POWER	Connects primary power to Analyzer. Red indicator lamp lights.
		OFF	Disconnects primary power.
1/4 AMP SLOW BLOW - cartridge fuse (rear panel)	F1		Fuses primary power.
INPUT SIG-3-circuit telephone jack	J1		Connects data signal under test to Analyzer.

TABLE III (Cont'd)

NAME AND TYPE	CIRCUIT DESIG.	CONTROL POSITIONS	FUNCTION
INPUT - 6-position rotary switch	S9	20	Adjusts unit to accept 20ma neutral input signal.
		60	Adjusts unit to accept 60ma neutral input signal.
		10/30	Adjusts unit to accept 10 to 30ma polar input signal.
		HI-Z	Adjusts unit to bridge input signal with 50k-ohm input impedance (zero-volt trigger).
		EIA	Adjusts unit to accept EIA input signal (±6-volt polar).
		HUB	Adjusts unit to accept HUB input signal (+60-volt Mark, -30-volt Space), input impedance greater than 50k ohms) (+15-volt trigger).
SIG MARK ON - indicator lamp, clear	DS6		Lights when input signal is in Mark condition.
S/S CODE LEVEL - 5-position rotary switch	S10	5	Adjusts unit to accept 5-level code input signals.
		6	Adjusts unit to accept 6-level code input signals.
		7	Adjusts unit to accept 7-level code input signals.
		8	Adjusts unit to accept 8-level code input signals.
		sync	Adjusts unit to accept synchronous input signals.
POL - 2-position toggle switch	S8	+/-	Adjusts unit to accept input signals of normal sense or inverted polarity.

TABLE III (Cont'd)

NAME AND TYPE	CIRCUIT DESIG.	CONTROL POSITIONS	FUNCTION
FILTER - 2-position toggle switch	S7	IN	Connects internal filter to remove noise and transients from input signal (for rates up to 150 bauds).
		OUT	Disconnects filter.
LOOP CURRENT - momentary pushbutton switch	S12		When depressed, current of input loop is indicated on meter.
BIT RATE (select) - 11-position rotary switch	S1	Range A / Range B	
		37.5	
		50	
		75	
		150	
		300 (Six optional rates)	Adjusts unit to accept input signals of corresponding bit rates.
		600	
		1200	
		2400	
		4800	
		9600	
		EXT	Connects external time-base signal to unit. Signal must be square-wave, ±6 volts, 200 x bit rate of signal under test.
BIT RATE - (range) 2-position rotary switch	S1	A	Selects range A of BIT RATE (select) switch above.
		B	Selects range B of BIT RATE (select) switch above.
MODE - 6-position rotary switch	S3	REV	Adjusts unit to detect and count bit errors in reversal pattern input signals.
		RAND	Adjusts unit to detect and count bit errors in a pseudo random pattern input signal.

TABLE III (Cont'd)

NAME AND TYPE	CIRCUIT DESIG.	CONTROL POSITIONS	FUNCTION
		PARITY COUNT	Adjusts unit to detect and count parity errors in 8-level code input signals.
		PEAK	Adjusts unit to measure peak distortion in start-stop and synchronous input signals.
		BIAS	Adjusts unit to measure bias distortion in start-stop and synchronous input signals.
		END	Adjusts unit to measure average end distortion in start-stop input signals.
TRANSITION SELECT-10-position rotary switch	S2	ALL	Adjusts unit to measure distortion of all input signal transitions.
		1 2 4 5 6 7 8 9	Adjusts unit to measure distortion of the selected transition of start-stop input signal characters.
Meter - milliampere meter movement	M1		Indicates distortion in per-cent-of-unit-interval (0-50 scale) when MODE switch is set to END, BIAS, or PEAK. Registers error count (0-50 scale) when MODE switch is set to PARITY COUNT, REV, or RAND. (Optional PC-cards A3 and A4 must be installed.) Indicates input signal current (0-100ma scale) when LOOP CURRENT switch is depressed.

TABLE III (Cont'd)

NAME AND TYPE	CIRCUIT DESIG.	CONTROL POSITIONS	FUNCTION
MARKING - indicator lamp, clear	DS2		Lights to indicate that end or bias distortion is Marking distortion.
SPACING - indicator lamp, clear	DS1		Lights to indicate that end or bias distortion is Spacing distortion.
DISPLAY RESET - 3-position toggle	S13	AUTO	Resets meter indication to zero every five seconds when measuring distortion. When counting bit or parity errors, resets meter to zero five seconds after COUNT COMP indicator lights.
		OFF	Disables automatic reset function.
		MAN	When momentarily depressed, resets meter indication to zero.
ERROR COUNT INTERVAL - 6-position rotary switch	S4	10^2	Lights COUNT COMP indicator lamp and steps error count after an interval of 10^2 bits has occurred.
		10^3	Lights COUNT COMP indicator lamp and stops error count after an interval of 10^3 bits has occurred.
		10^4	Lights COUNT COMP indicator lamp and stops error count after an interval of 10^4 bits has occurred.
		10^5	Lights COUNT COMP indicator lamp and stops error count after an interval of 10^5 bits has occurred.
		10^6	Lights COUNT COMP indicator lamp and stops error count after an interval of 10^6 bits has occurred.
		∞	Error count stop function is disabled.

TABLE III (Cont'd)

NAME AND TYPE	CIRCUIT DESIG.	CONTROL POSITIONS	FUNCTION
COUNT COMP - indicator lamp, green	DS3		Lights to signal end of bit count determined by setting of ERROR COUNT INTERVAL (BITS) switch.
OVERFLOW - indicator lamp, amber	DS4		Lights when error count reaches 50, the maximum count registerable, and holds until reset manually.
PARITY ERROR - indicator lamp, red	DS5		Lights when a parity error is detected.
PARITY ERROR - 3-position toggle switch	S11	OFF	Disable PARITY ERROR indicator lamp.
		ON	Permits PARITY ERROR indicator lamp to light when error is detected.
		RESET	When momentarily depressed to this position, turns off PARITY ERROR indicator lamp.
PUSH TO SYNC - momentary push-button switch	S5		When depressed, input signal reversal or random pattern is synchronized for error counting.
TEST SIG OUTPUT - two binding posts	TP1 TP2		Provides output of internal reversal or pseudo random pattern generator for use with another Analyzer in reversal or random pattern bit error counting.
EXT CLK - 2-position toggle switch (rear panel)	S14	INT	Clocks internal pattern generator with internal time base.
		EXT	Clocks internal pattern generator with external 1 x bit clock signal.

(E) Installation

1.12 As a portable self-contained instrument (optional), the Analyzer is ready for operation when shipped. It can be rack-mounted, however (see 1.13). Also, accessory connections (see 2.02) expand its capabilities; their use is covered in the operating procedures (see 2.03). Furthermore, strapping options (see 1.15 through 1.21) enhance the Analyzer's versatility.

Mounting

1.13 The Analyzer may be used as a portable unit, or two L-brackets (Fig. 3) may be used to rack-mount it in an available slot in any standard 19-inch relay rack.

Connections

1.14 All connections are described in 2.02.

Strapping

1.15 The Analyzer has six strapping options, as described in 1.16 through 1.21. Fig. 5 shows the strapping terminal locations. Solder No. 22 bus wire between the terminals specified for a given option and remove any unspecified straps.

Primary Power Options

1.16 The Analyzer will accept either 115- or 230-volt ac operating power. Inside bottom of chassis, strap terminals E1 through E4 in accordance with Fig. 5 for either 115- or 230-volt ac operation. When shipped, the unit is strapped for 115-volt ac.

Parity Error Options

1.17 The parity error circuits can detect errors in either even or odd parity check signals. On PC-card A5, strap terminals A, B, and C in accordance with Fig. 5 for either even or odd parity. When shipped, the unit is strapped for even parity.

Error Count Options

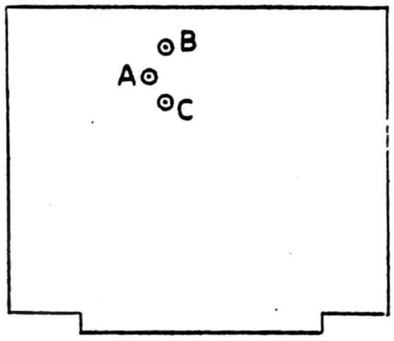
1.18 The Analyzer will function with or without optional PC-cards A3 (bit error circuits) and A4 (error counter circuits). On PC-card A8 (Fig. 5), strap terminals A and B together when optional PC-cards are not used. Remove strap when PC-cards are used. Refer to 4(E) for installation of optional PC-cards.

Pseudo Random Pattern Generator Options

1.19 The internal pseudo random pattern generator will generate any of three patterns: a 511-bit common pattern, a 511-bit CCITT standard pattern, and a 2047-bit pattern. On PC-card A3, strap terminals A through F in accordance with Fig. 5 for either the 511-bit pattern or the 2047-bit pattern. When shipped, PC-card A3 is strapped for the 511-bit pattern.

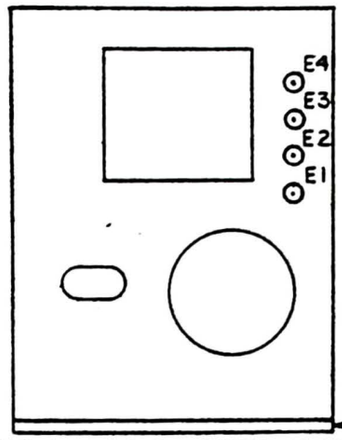
Pseudo Random (and Reversal) Pattern Output Sense Options

1.20 The output of the pseudo random pattern generator may be strapped to produce a signal of EIA-RS-232B (-6-volt Mark) or MIL-STD-188B (+6-volt Mark) signal sense. On PC-card A3, strap terminals G, H, and I in accordance with Fig. 5 for either normal or reverse signal sense. When shipped, A3 is strapped for normal sense.



COMPONENT BOARD A5

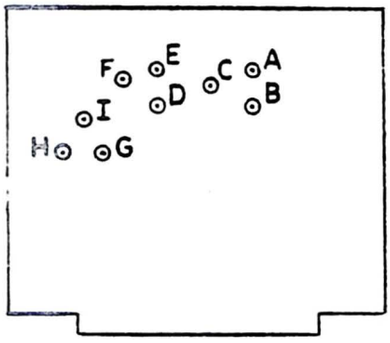
OPTION	STRAP
EVEN PARITY	A-C
ODD PARITY	A-B



OPTION	STRAP
115 VAC	E1-E3 E2-E4
230VAC	E2-E3

REAR PANEL

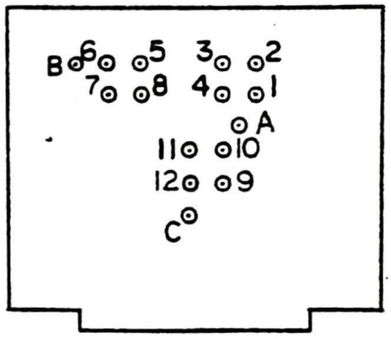
P/O CHASSIS, BOTTOM VIEW



COMPONENT BOARD A3

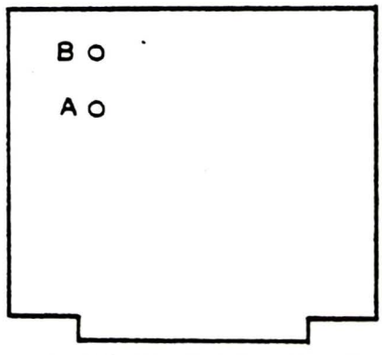
OPTION	STRAP
511-BIT PATTERN	B-C, E-F
2047-BIT PATTERN	A-C, E-F

OPTION	STRAP
LOW MARK	G-I
HIGH MARK	H-I



COMPONENT BOARD A1

CRYSTAL	Y1			Y2			Y3		
DIVISION FACTOR	32	16	1	32	16	1	32	16	1
STRAP TERMINALS	3-4	2-4	1-4	3-A	2-A	1-A	7-B	6-B	5-B
CRYSTAL	Y4			Y5			Y6		
DIVISION FACTOR	32	16	1	32	16	1	32	16	1
STRAP TERMINALS	7-8	6-8	5-8	11-12	10-12	9-12	11-C	10-C	9-C



COMPONENT BOARD A8

OPTION	STRAP
OPTIONAL COMPONENT BOARDS A3, A4 NOT INSTALLED	A-B
OPTIONAL COMPONENT BOARDS A3, A4 INSTALLED	REMOVE STRAP

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Fig. 5 - Strapping

Time-Base Optional Bit Rates

1.21 The Analyzer has provisions to add up to six optional crystals from which to derive six optional bit rates. The crystal frequencies are selected to produce a 200 x bit signal after having been divided by a factor of 1, 16, or 32 by the time-base downcounter. On PC-card A1, strap terminals 1 through 12 and A, B, and C in accordance with Fig. 5 to achieve the required division factor. Installation of the optional crystals is described in 4(G). When shipped, the Analyzer will be strapped in accordance with any optional crystals supplied. If optional crystals are not supplied, the strapping terminals on A1 will be open.

(F) Adjustments Required After Shipping

1.22 Make adjustments as follows:

(a) Remove rear cover.

(b) Using power cord supplied, connect primary power to unit.

(c) Set POWER switch to OFF.

(d) Use screwdriver to adjust zero-adjust screw on meter front to set meter pointer to zero.

(e) Set POWER switch on.

(f) Set DISPLAY RESET switch to OFF.

(g) Set PARITY ERROR switch to ON.

(h) Set MODE switch to PARITY COUNT.

(i) Set TRANSITION SELECT switch to ALL.

(j) Set ERROR COUNT INTERVAL switch to infinity sign ∞.

(k) Set INPUT switch to EIA.

(l) Set POL switch to +.

(m) Set FILTER switch to OUT.

(n) Set BIT RATE (range) switch to A.

(o) Set BIT RATE (select) switch to 75.

(p) Using Pattern Generator PG-303A, or equivalent, apply a low-level (EIA ±6 volts) 8-level selected character signal to INPUT SIG jack on Analyzer. Set Pattern Generator for manual character step. Set selected character to have an even number of Marks if the Analyzer is strapped for odd parity or to have an odd number of Marks if strapped for even parity.

(q) On Analyzer, depress DISPLAY RESET switch to MAN and PARITY ERROR switch to RESET. PARITY ERROR indicator lamp should now be out and meter should indicate zero.

(r) On Pattern Generator, depress manual release switch one time. On Analyzer, PARITY ERROR indicator lamp should light and meter should advance one division. Perform this procedure exactly 39 more times. Analyzer meter should then indicate 40.

(s) At rear of Analyzer, on exposed edge of power supply circuits PC-card A2, adjust R6 (Fig. 34) for an indication of 40 on front-panel meter.

(t) Connect a multimeter to TB2 (+5v) and TB2 (-) on PC-card A2.

(u) Adjust R21 (Fig. 34) on PC-card A2 for +5-volt indication on multimeter.

2. OPERATION

2.01 Front-panel switches and indicators permit the operator to measure loop current, analyze distortion, and count parity and bit errors present in the output signal of data channel or equipment under test. Required and accessory connections are described in 2.02, and operating procedures are outlined in 2.03. (Controls are described in Table III.)

(A) Circuit Connections

2.02 The Analyzer becomes fully operational when the power cord is inserted in the 3-wire receptable at the rear of the unit and the signal under test is patched to the INPUT SIG jack on the front panel. In addition to these two basic connections, there are a number of accessory connectors, as shown in Fig. 6 and described in Table IV.

(B) Operating Procedures

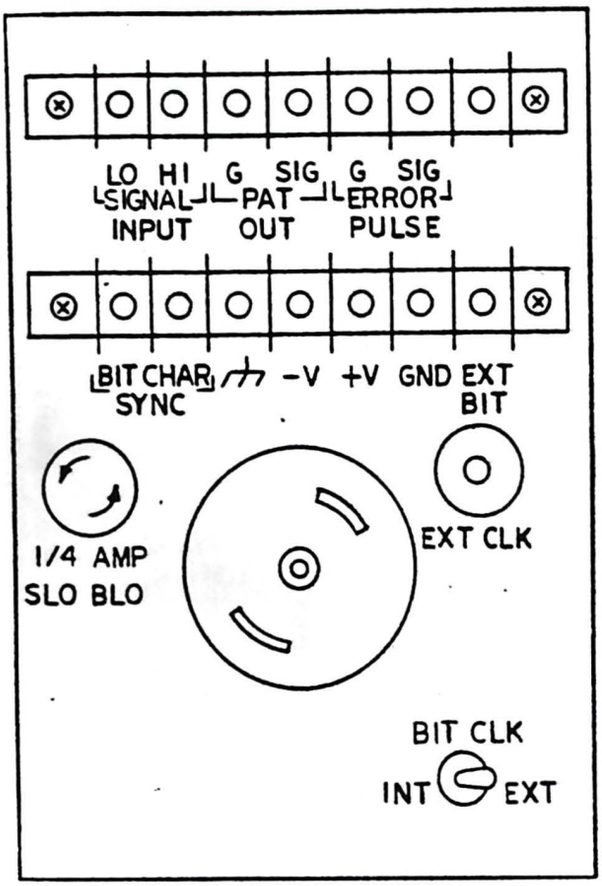
2.03 First, perform the preliminary set-up procedure (see 2.04), and then any one or all of the individual procedures outlined in 2.05 through 2.12.

Preliminary Procedure

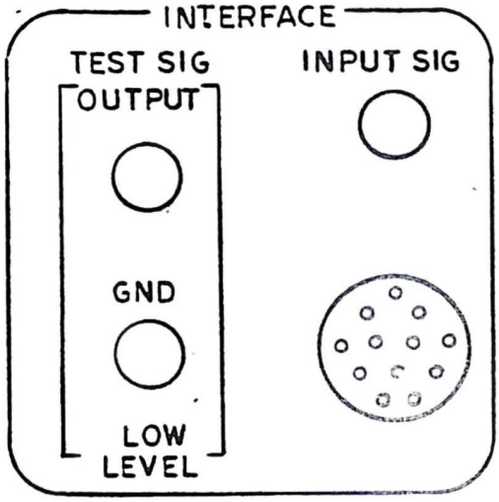
2.04 Perform the following set-up procedure before performing the procedures in 2.05 through 2.12.

(a) Set POWER switch on.

(b) Set INPUT switch to position that corresponds to voltage or current level(s) of signal under test.



REAR PANEL



P/O FRONT PANEL

Fig. 6 - Connections

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TABLE IV

CONNECTIONS

PANEL MARKING	DESCRIPTION	FUNCTION
EXT CLK	BNC connector	External 200 x bit time signal input (±6 volts, square-wave).
SIGNAL INPUT	Terminal board	Signal under test input.
PAT OUT	Terminal board	Internal reversal or pseudo random pattern signal output (±6 volts).
ERROR PULSE	Terminal board	Internal bit error detector output.
BIT SYNC	Terminal board	Internal 1 x bit timing signal output.

TABLE IV (Cont'd)

PANEL MARKING	DESCRIPTION	FUNCTION
CHAR SYNC	Terminal board	Internal 1 x character timing signal output.
EXT BIT	Terminal board	External 1 x bit timing signal input to internal pattern generator. (±6 volts, square-wave).
⏚	Terminal board	Chassis ground.
GND	Terminal board	Signal ground.
+V	Terminal board	Internal +15-volt output.
-V	Terminal board	Internal -15-volt output.
Data Set Interface Connector	12-pin Connector:	Provides the following input and output connections for operation with the optional Test Adapter Unit:
	Pin A	Pattern out
	Pin B	-15 volts out
	Pin C	External clock in (1 x bit)
	Pin D	Bit sync out
	Pin E	Signal ground
	Pin F	Spare
	Pin H	+15 volts out
	Pin J	+5 volts out
	Pin K	Spare
	Pin L	Chassis ground
	Pin M Pin N	Data signal in

(c) Set S/S CODE LEVEL switch to position (5, 6, 7, or 8) that corresponds to code level of start-stop signal under test, or to SYNC if signal under test is synchronous.

(d) Set POL (polarity) switch to (+) if signal under test is of normal sense (high Mark, low Space) or to (-) if signal under test is of reverse sense (low Mark, high Space).

(e) Set FILTER switch to OUT. FILTER switch may be set to IN to remove noise and transients from signal under test.

(f) Set DISPLAY RESET switch to OFF.

(g) Set PARITY ERROR switch to OFF.

(h) Connect signal under test to INPUT SIG jack (unless it is already connected via rear-panel SIGNAL INPUT terminals or front-panel multipin connector.

(i) If signal under test is high-level current (20 or 60ma neutral or 10/30ma polar), depress LOOP CURRENT pushbutton and check meter indication, on lower scale, for correct current indication. Externally, adjust loop current for correct indication, if required.

Note: If signal under test is neutral, place it in steady Mark condition and adjust for correct Mark current. If signal under test is high-level polar, place it in steady Mark and adjust Mark battery current for correct Mark current. Then place signal in steady Space and adjust Space battery current for correct Space current.

(j) Set BIT RATE switches to range A and select the standard bit rate of 37.5, 50, 75, 150, 300, 600, 1200, 2400, 4800, or 9600 baud that corresponds to bit rate of signal under test.

Note: If the bit rate of the signal under test is not one of the above standard rates, the correct bit rate (up to 9600 bauds) can be achieved by one of two methods:
(1) It may be included on range B of the BIT RATE switch as an optional rate, or
(2) the BIT RATE switch may be set to EXT (external), and an external time-base signal (±6 volts, square-wave) can be connected to the rear-panel EXT CLK connector. Set the external time-base frequency to 200 times the bit rate of the signal under test.

Peak Distortion Measurement Procedure

2.05 The measure peak bias distortion, perform the set-up procedure in 2.04 and then continue with the following procedure.

(a) Set MODE switch to PEAK.

(b) Set TRANSITION SELECT switch to ALL.

(c) Read peak distortion on upper scale of meter (0 - 50 per cent of unit interval). Meter pointer will hold at highest deflection obtained during measurement period. Pointer will hold until it is reset to zero by momentarily depressing DISPLAY RESET switch to MAN position.

Note: Reset function can be performed automatically each five seconds by setting DISPLAY RESET switch to AUTO.

Bias Distortion Measurement Procedure

2.06 To measure average bias distortion, perform set-up procedure in 2.04 and then continue with the following procedure.

(a) Set MODE switch to BIAS.

(b) Set TRANSITION SELECT switch to ALL.

(c) Set DISPLAY RESET switch to OFF.

(d) Read average bias distortion on upper scale of meter (0 - 50 per cent of unit interval). If the Space-to-Mark transitions of the signal under test are occurring early, the MARKING indicator lamp will light. If they are occurring late, the SPACING indicator lamp will light.

End Distortion Measurement Procedure

2.07 To measure end distortion, perform the set-up procedure in 2.04 and then continue with the following procedure.

Note: End distortion is not measured for synchronous signals.

(a) Set MODE switch to END.

(b) Set TRANSITION SELECT switch to ALL.

(c) Set DISPLAY RESET switch to OFF.

(d) Read average end distortion on upper scale of meter (0 - 50 per cent of unit interval). If the Mark-to-Space transitions of the signal under test are occurring early, the SPACING indicator lamp will light. If they are occurring late, the MARKING indicator lamp will light.

Individual Transition Distortion Measurement Procedure

2.08 To measure the distortion of individual transitions, perform the set-up procedure in 2.04 and then continue with the following procedure.

Note: Individual transition distortion is not measured for synchronous signals.

(a) Set MODE switch to either BIAS (see 2.06), END (see 2.07), or PEAK (see 2.05).

(b) Set TRANSITION SELECT switch to setting (1 through 9) that corresponds to the position, in the character, of the transition to be measured. (Setting 1 of switch corresponds to the transition ending the start element.)

Note: Where there is no transition between two elements of a character (between two Marks, for example), no distortion will register.

Parity Error Detection Procedure

2.09 To detect parity errors, perform the set-up procedure in 2.04 and then continue with the following procedure.

(a) Set MODE switch to PARITY COUNT.

(b) Set PARITY ERROR switch to ON.

(c) Set S/S CODE LEVEL switch to 8.

(d) Using Pattern Generator PG-303A, or equivalent, apply an 8-level start-stop parity check signal to the equipment under test.

(e) If the equipment under test causes parity errors to occur, the PARITY ERROR indicator lamp will light. Each time a parity error occurs, the lamp will light and remain lit until the PARITY ERROR switch is momentarily depressed to the RESET position.

Parity Error Counting Procedure

2.10 When optional PC-cards A3 and A4 are installed in the Analyzer, the parity errors detected (see 2.09) will register on the front-panel meter. Perform the set-up procedure in 2.04 and then continue with the following procedure.

(a) Using Pattern Generator PG-303A, or equivalent, apply an 8-level start-stop parity check signal to input of equipment under test.

(b) Set MODE switch to PARITY COUNT.

(c) Set S/S CODE LEVEL switch to 8.

(d) Set DISPLAY RESET switch to AUTO. Depress PUSH TO SYNC switch.

(e) Set ERROR COUNT INTERVAL switch to ∞. If equipment under test causes parity errors to occur, the number of errors will register on the front-panel meter. The meter pointer will advance up scale one division per error. When 50 errors have occurred, the OVERFLOW indicator lamp will light and no further errors will be

counted. If, however, the ERROR COUNT INTERVAL switch is set to a position other than ∞, the COUNT COMP indicator lamp will light and the error count will stop after the selected interval (of 10^2, 10^3, 10^4, 10^5, or 10^6 bits) has occurred. Five seconds after the COUNT COMP indicator lamp lights the count is reset to zero and the count begins again.

(f) Set ERROR COUNT INTERVAL switch to position (of 10^2 through 10^6) that causes the COUNT COMP indicator lamp to light before the OVERFLOW indicator lamp can light.

(g) The count registered on the meter at the time the COUNT COMP indicator lamp lights is the number of parity errors per error-count interval.

Example: If the ERROR COUNT INTERVAL switch is set to 10^3 and the meter registers 32 at the time the COUNT COMP indicator lamp lights, the ratio of parity errors to error-count interval bits is 32 errors/1000 bits.

Bit Error Counting, Reversal Pattern, Procedure

2.11 When optional PC-cards A3 and A4 are installed in the Analyzer, bit errors in reversal pattern signals can be detected and counted. Perform the set-up procedure in 2.04 and then continue with the following procedure.

(a) Using Pattern Generator PG-303A, or equivalent, apply a reversal pattern signal to the equipment under test.

(b) Set MODE switch to REV and S/S CODE LEVEL switch to SYNC.

(c) Set DISPLAY RESET switch to AUTO. Depress PUSH TO SYNC switch.

(d) Set ERROR COUNT INTERVAL switch to ∞. If the equipment under test causes bit errors to occur, the number of errors will register on the front-panel meter. The meter pointer will advance up scale one division per error. When 50 errors have occurred, the OVERFLOW indicator lamp will light and no further errors will be counted. If however, the ERROR COUNT INTERVAL switch is set to a position other than ∞, the COUNT COMP indicator lamp will light and the error count will stop after the selected interval (of 10^2, 10^3, 10^4, 10^5, or 10^6 bits) has occurred. Five seconds after the COUNT COMP indicator lamp lights, the count is reset to zero and the count begins again.

(e) Set ERROR COUNT INTERVAL switch to position (10^2 through 10^6) that causes COUNT COMP indicator lamp to light before OVERFLOW indicator lamp can light.

(f) The count registered on the meter at the time the COUNT COMP indicator lamp lights is the number of bit errors per error-count interval.

Example: If the ERROR COUNT INTERVAL switch is set to 10^2 and the meter registers 47 at the time the COUNT COMP indicator lamp lights, the ratio of bit errors to error-count interval bits is 47 errors/100 bits.

Note: If it is required to count more than 50 bit errors, an external electronic counter may be connected to the ERROR PULSE terminals on the rear panel.

Bit Error Counting, Pseudo Random Pattern, Procedure

2.12 When optional PC-cards A3 and A4 are installed in the Analyzer, bit errors in a pseudo random pattern signal can be detected and counted. The procedure is the same as in 2.11 except that Pattern Generator PG-303A is used to apply a pseudo random pattern signal to the equipment under test and the MODE switch is set to RAND.

Note: The Analyzer can be strapped (see 1.19) for either 511-bit (common or CCITT) or 2047-bit random patterns. Both the Analyzer and the Pattern Generator must be strapped for the same pattern. Another Analyzer may be used to apply the random pattern signal to the equipment under test. The internally generated random pattern signal is available at the front-panel connectors (TEST SIG OUTPUT).

3. PRINCIPLES OF OPERATION

(A) General

3.01 This section provides a simplified block diagram analysis (see (B)), a detailed block diagram analysis (see (C)), and an over-all logic diagram analysis (see (D)). The power supply circuits are covered in (E).

(B) Simplified Block Diagram Analysis (Fig. 7)

3.02 The data signal under test is applied to the input circuits. There, it is converted to logic level signal MS for distribution to the other Analyzer circuits.

3.03 The time-base circuits generate a timing signal whose negative transitions occur at 200 times the bit rate of MS. The sync circuits divide 200 x bit by two to produce 100 x bit timing signal DC. The distortion counter circuits divide DC by 100 to produce 1 x bit timing signal BT.

3.04 When MS is synchronous, the sync circuits synchronize DC with the average time position of the MS transitions. This is accomplished by comparing BT with MS and adding the subtracting DC pulses as required.

3.05 When MS is start-stop, the sync circuits synchronize DC with the first transition of each start element. This is accomplished by enabling DC at each start element and disabling DC at each stop element.

3.06 The distortion counter circuits count the negative transitions of DC. The binary coded decimal (BCD) output of the counter steps from zero to 50 to zero during

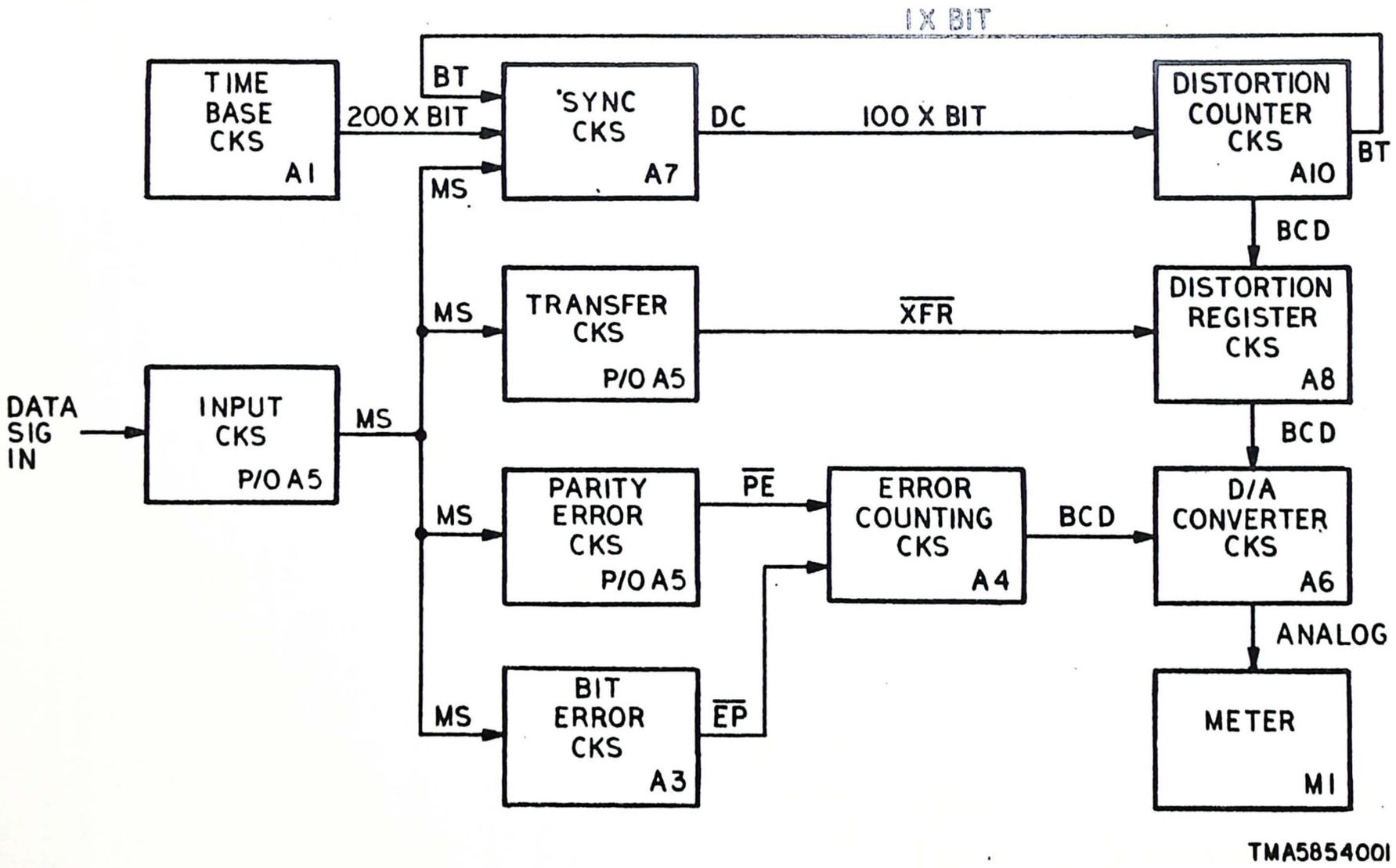


Fig. 7 - Simplified Block Diagram

the interval of each MS bit. If MS is not distorted, the count will reach zero as the actual MS transitions occur. If the actural MS transitions occur early or late, the BCD count, at the time the transitions occur, will be numerically equal to the per cent of displacement.

3.07 Each time an actual MS transition occurs, it initiates a transfer pulse $\overline{XFR}$ in the transfer circuits. Transfer pulse $\overline{XFR}$ gates the BCD count, of that instant, into the distortion register circuits. There it is stored until the next $\overline{XFR}$ pulse is generated. The D/A converter circuits constantly monitor and convert the stored count to an equivalent analog current. The analog current drives meter M1 to read transition displacement in per-cent-of-unit interval.

3.08 When MS is an 8-level code start-stop signal, the parity error circuits emit a parity error pulse ($\overline{PE}$) each time they detect a parity error in MS. Also, when MS is either a reversal pattern signal or a pseudo random pattern signal, the bit error circuits emit an error pulse ($\overline{EP}$) each time they detect a bit error in MS. Either $\overline{EP}$ or $\overline{PE}$ steps the error counting circuits. The BCD output of the error counting circuits is converted to an equivalent analog current by the D/A converter circuits. The analog current drives meter M1, causing its pointer to advance up scale one division each time an error is detected.

(C) Detailed Block Diagram Analysis

3.09 The distortion measuring circuits are described in 3.11 through 3.22, and the error counting circuits are covered in 3.23 through 3.27.

Note: The block diagrams (Fig. 27 and 28) are fold-out illustrations located at the end of this section to facilitate viewing them while reading the following text and associated timing diagrams (Fig. 8 through 11).

Distortion Measuring Circuits

3.10 The distortion measuring circuits are described in 3.11 through 3.22.

Input Circuits (Fig. 27)

3.11 The data signal under test is coupled through POL switch S8 to the input circuits and to LOOP CURRENT switch S12. The POL switch adjusts the input to accept either normal or reverse polarity signals. The LOOP CURRENT switch facilitates reading loop current on meter M1. INPUT switch S9 adjusts the input circuits to accept data of any standard current or voltage level. FILTER switch S7 connects a filter across the loop to remove noise from the data, if required (not to be used at bit rates over 150). The input circuits convert the incoming data to a logic level signal (MS) that is compatible with the rest of the Analyzer circuits. Signal MSP consists of a train of spikes that coincide with the negative transitions of MS. The SIG MARK ON indicator lamp, DS6, lights when the data signal is in the Mark condition.

Time-Base Circuits (Fig. 27)

3.12 BIT RATE switch S1 adjusts the time-base circuits to produce an output square-wave (200 x BIT) whose negative transitions occur at 200 times the bit rate of MS. The BIT RATE switch has an external position that facilitates substituting an externally generated 200 x bit signal (EXT CLK connector).

Sync Circuits (Fig. 27)

3.13 The 200 x bit timing signal is divided by two in the sync circuits to produce 100 x bit timing signal DC. DC is coupled to the distortion counter circuits, where it is divided by 100 to produce 1 x bit timing signal BT. When MS is synchronous, the sync circuits compare the rate of BT with the rate of MS. If BT is fast, pulses are subtracted from DC. If BT is slow, pulses are added to DC. In this way, DC, and subsequently BT, are synchronized with MS in rate and phase. Timing signal CTB has a rate of 200 times bit. It is derived from the 200 x BIT output of the time-base circuits and is synchronized with MS.

3.14 When DC is start-stop, the sync circuits utilize MSP and $\overline{TO}$ to synchronize DC with the first transition of each start element of MS and to derive additional timing signal RST and ST. Shortly after the first transition of each stop element, DC is inhibited and ST inhibits the transfer circuits. At the first transition of each start element, DC is enabled and RST resets the distortion counter circuits to zero. Then, shortly after the first transition of each start element, ST enables the transfer circuits. In this way, DC and the distortion counter are synchronized with the first transition of each start element, and the transfer circuits are disabled during the time of that transition.

3.15 S/S CODE LEVEL switch S10 adjusts the sync circuits for either synchronous or 5-, 6-, 7-, or 8-level start-stop operation. The CHAR SYNC output provides positive transitions to coincide with the first transition of each start element and negative transitions one unit after the first transition of each stop element. The BIT SYNC output provides a 1 x bit signal derived from BT.

Distortion Measurement (Fig. 8, 9, and 27)

3.16 The distortion counter circuits count the negative transitions of DC. The BCD output steps from 50 through zero through 50 for each transition of MS. The BCD count reaches zero at the ideal time position of each transition of MS. When an actual transition of MS occurs, it initiates a transfer pulse $\overline{XFR}$ in the transfer circuits. Each time $\overline{XFR}$ occurs, it transfers the BCD count into the distortion

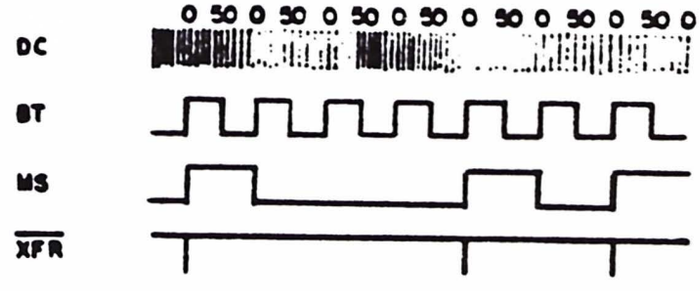


Fig. 8 - Over-All Timing, Synchronous Distortion Measurement

register circuits. The transferred BCD count is there stored until the next $\overline{XFR}$ pulse occurs to displace it with a new count. If MS is not distorted, its actual transitions will occur as the counter BCD output is at zero. If the transitions are displaced either early or late, however, the counter will be at some count between zero and 50 when $\overline{XFR}$ occurs.

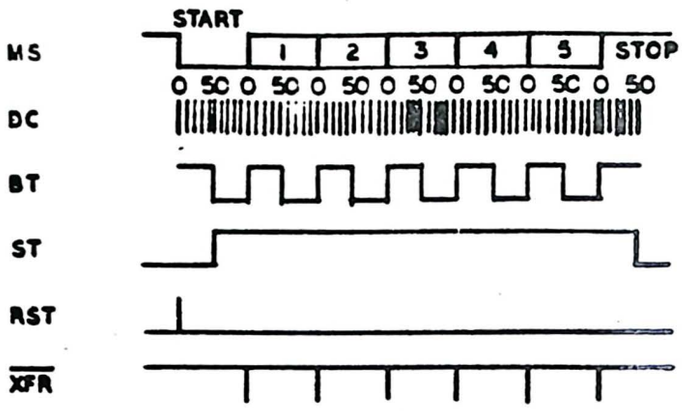


Fig. 9 - Over-All Timing, Start-Stop Distortion Measurement

Example: If MS transitions are displaced early or late by 21 per cent of a unit interval from their ideal time positions, the BCD count at the output of the counter will be at count 21 when $\overline{XFR}$ occurs. BCD count 21 will therefore be transferred into the distortion register each time XFR occurs. The BCD output of the register is continuously converted to an equivalent analog current by the D/A converter circuits. The ANALOG current in this case would drive meter M1 to indicate 21 per cent.

Extra Count (Fig. 27)

3.17 As the distortion counter down-counts from 50 to zero, it is always one count short. During the down-count, BT adds a constant one count to the distortion register to compensate.

Marking and Spacing Indicator Lamps (Fig. 27)

3.18 Signal EL lights either the Marking or Spacing indicator lamp to signal whether the distortion indication (M1) represents early or late distortion.

Bias Distortion (Fig. 27)

3.19 When set to BIAS, MODE switch S3 adjusts the transfer circuit to permit only the Space-to-Mark transitions of MS to initiate transfer pulses.

End Distortion (Fig. 27)

3.20 When set to END, MODE switch S3 adjusts the transfer circuits to permit only the Mark-to-Space transitions of MS to initiate transfer pulses. For synchronous operation, end distortion does not apply, and S/S CODE LEVEL switch S10 inhibits the transfer pulses during all Mark-to-Space transitions of MS.

Peak Distortion (Fig. 27)

3.21 When set to PEAK, MODE switch S3 adjusts the transfer circuits to permit both Space-to-Mark and Mark-to-Space transitions of MS to initiate transfer pulses. Signal PT inhibits $\overline{XFR}$ except when the BCD count at the input to the distortion register exceeds the BCD count at the output. Again, end distortion does not apply during synchronous operation, and S/S CODE LEVEL switch S10 inhibits the transfer circuits during all Mark-to-Space transitions of MS.

Individual Transitions (Fig. 27)

3.22 For start-stop operation only, the end, bias, or peak distortion of an indivdual transition of each character may be measured. TRANSITION SELECT switch S2 may be set to inhibit the transfer circuits during all transitions of each character except the one selected (1 through 9). Transition 1 corresponds to the first transition of the first information bit.

Error Detection and Counting Circuits (Fig. 28)

3.23 The time-base circuits, sync circuits (and associated function of distortion counter circuits) and input circuits are described in 3.11 through 3.15 above.

Parity Error Circuits (Fig. 10 and 28)

3.24 The parity error circuits monitor MS to produce a parity error pulse ($\overline{PE}$) for each character that contains the wrong number of Mark elements. The circuits are strappable to detect either even or odd parity errors. For even parity, each character that contains an odd number of Marks initiates a $\overline{PE}$ pulse. For odd parity, each character that contains an even number of Marks initiates a $\overline{PE}$ pulse. The negative transition of ST produces the PE pulse during the stop element of each character that contains the incorrect number of Marks. Reset pulse $\overline{RST}$ resets the circuits at the first transition of each start element. Signal $\overline{T9}$ inhibits the circuits before the stop element can be counted as a Mark. Each time a PE pulse is generated, PARITY ERROR indicator lamp DS5 lights. The lamp remains lit until PARITY ERROR switch S11 is operated to put it out. Each time a PE pulse is emitted, it steps the error counting circuits one count (see 3.26 and 3.27 below).

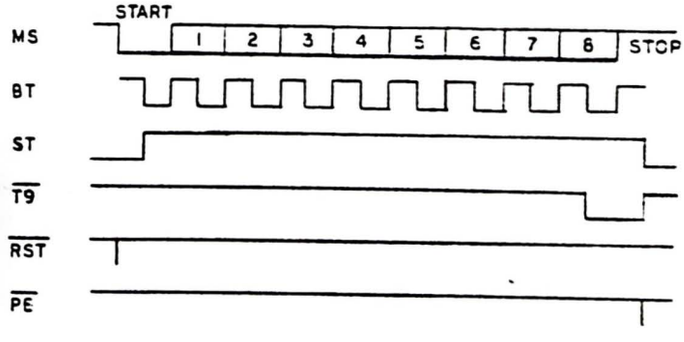


Fig. 10 - Over-All Timing, Parity Error Detection

Bit Error Circuits (Fig. 11 and 28)

3.25 The bit error circuits monitor MS when MS is either a reversal pattern or pseudo random pattern signal. MS is compared with identical internally generated patterns. Should MS lose a bit, the incoming and internal signal patterns would not be coincident during the time of the missing bit (Fig. 11). The lack of coincidence initiates an error pulse (EP). PUSH TO SYNC switch S5 is operated to synchronize the incoming pattern with the internal pattern. During synchronization, signal CS inhibits the error counting circuits (see 3.26 and 3.27 below). Signal SP is a 1 x bit spike train that steps the interval counter in the error counter circuits (see 3.26 and 3.27 below). SP is derived from timing signal BT applied through BIT CLK switch A12S1. The BIT CLK switch may also be set to substitute an external 1 x bit signal from EXT BIT terminals on TB2. Error pulse EP is coupled out through ERROR PULSE terminals on TB1. The output of the internal pseudo random pattern generator is made available at the TEST SIG OUTPUT connectors, TP1 and TP2, on the front panel.

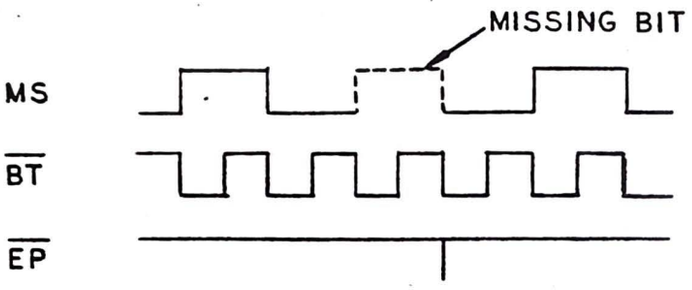


Fig. 11 - Over-All Timing, Bit Error Detection

Error Counting Circuits (Fig. 28)

3.26 As determined by the setting of MODE switch S3, the error counter circuits count either the bit error pulse $\overline{EP}$ or the parity error pulse $\overline{PE}$. The BCD output of the error counting circuits is monitored by the D/A converter circuits. The D/A converter circuits convert the count to an equivalent analog current. The analog current drives meter M1. Each time an error pulse occurs, the BCD count steps up one count, causing the meter pointer to advance up scale one division. At count 51 the OVERFLOW indicator lamp lights and error counting is inhibited.

3.27 While error pulses are being counted, SP spikes are also being counted. The spikes occur at the bit rate of MS. After a number of spikes have occurred, as selected by the ERROR COUNT INTERVAL switch (10^2, 10^3, 10^4, 10^5, or 10^6 bits), the error counting circuits become inhibited, the COUNT COMP indicator lamp lights, and $\overline{CS}$ enables the automatic function of the reset circuits. Five seconds later reset pulse ECR resets the error counter circuits (if DISPLAY RESET switch S13 is set to AUTO). The COUNT COMP or OVERFLOW indicator lamp goes out and a new error count begins.

Note: Both indicator lamps do not light at the same time. Error count 51 lights the OVERFLOW indicator lamp, and the selected interval count lights the COUNT COMP indicator lamp. The first completed count lights its associated indicator lamp. As soon as one of the two counts is complete both counts are inhibited. Both counts remain inhibited and the lit indicator lamp remains lit until ECR resets both counts to zero. ECR will occur five seconds after one of the two counts is

complete if DISPLAY RESET switch is set to AUTO. If the DISPLAY RESET switch is set to OFF, ECR will occur when the DISPLAY RESET switch is depressed to MAN. The operator must select the position of the ERROR COUNT INTERVAL switch that permits the interval count to become complete before the error count overflows.

(D) Logic Diagram Analysis

3.28 The logic functions of each major circuit area are detailed in 3.29 through 3.77. Logic standards used in this analysis are described in Fig. 12.

Note: The logic diagrams (Fig. 27 through 33) are fold-out illustrations and are therefore located at the end of Section 4 to facilitate viewing them while reading the following text and timing diagrams (Fig. 13 through 24).

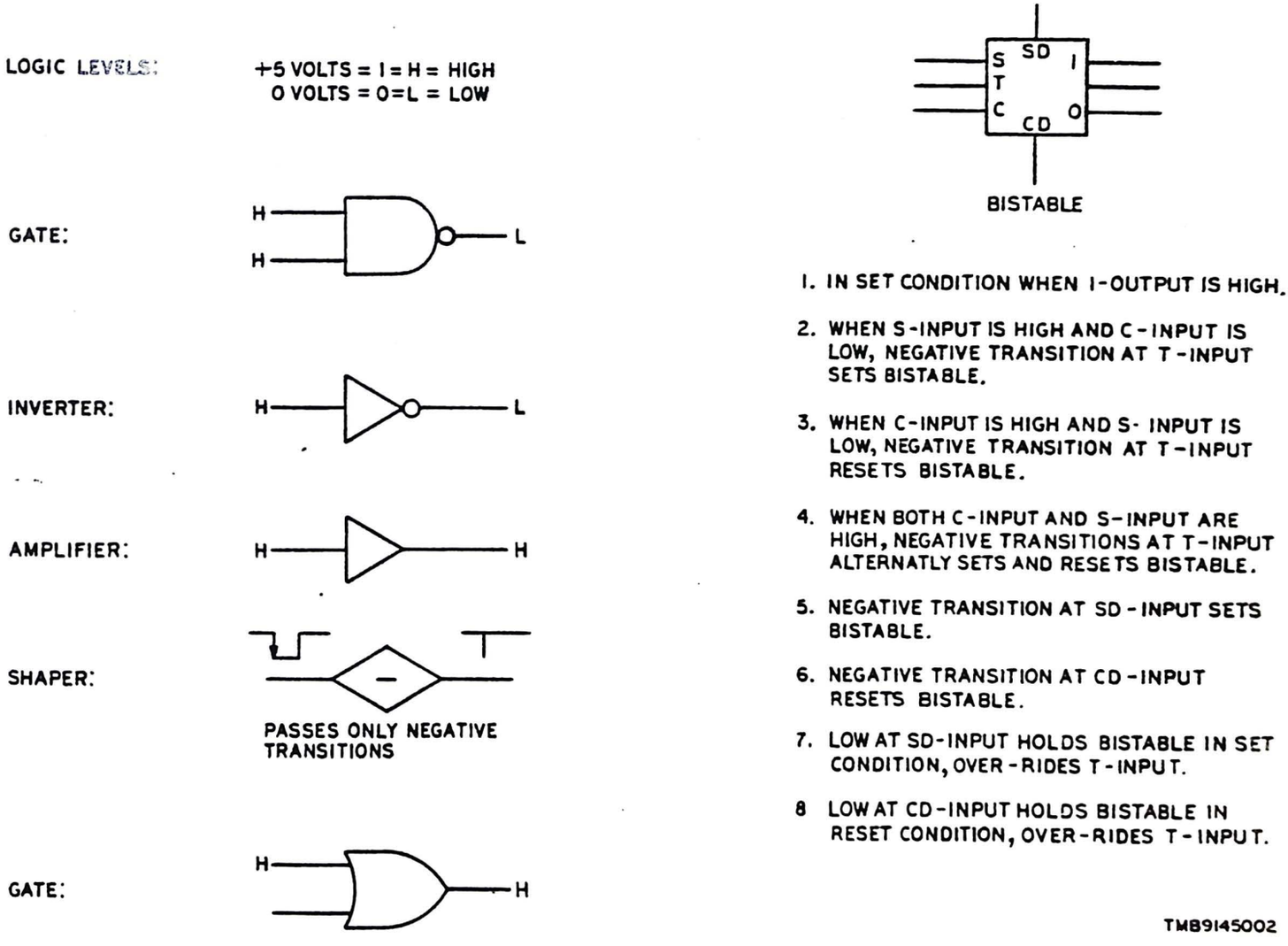


Fig. 12 - Logic Standards

Input Circuits (Fig. 13 and 29)

3.29 The data signal under test is coupled in through POL (polarity) switch S8, LOOP CURRENT switch S12, and resistors A5R4 and A5R5 to the input of electronic relay A5Q1-A5Q6. The signal at the output of the relay is coupled through inverter I1 to become logic-level data signal $\overline{MS}$. $\overline{MS}$ is coupled through inverter I2 to become signal MS. When MS is high (Mark condition), it produces a low at the output of I4, which lights SIG MARK ON indicator lamp DS6. Each negative transition of MS is coupled through shaper SH-1 to produce positive spikes MSP at the output of I3.

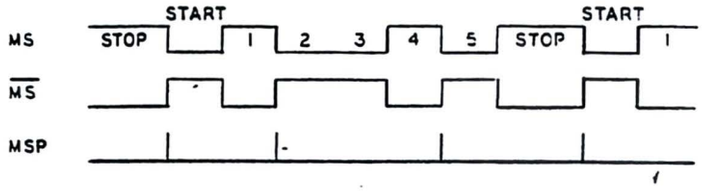


Fig. 13 - Input Network Timing

3.30 When the data signal under test is connected to the Analyzer via INPUT SIG jack J1, inputs from TB1 and J2 are disconnected at J1 contacts, opened when a phone plug is inserted in J1. POL switch S8 adjusts the input circuits to accept either normal polarity (low Mark) signals. With S8 set to (+), a normal polarity input signal produces a normal polarity output signal MS. With S8 set to (-), a reverse polarity input signal produces a normal polarity output signal MS. When LOOP CURRENT pushbutton switch S12 is depressed, meter bridge rectifier A5CR8-CR11 is connected in series with the input loop. Front-panel meter M1 then reads loop current. With INPUT switch S9 set to 20 or 10/30, the input loop is loaded by 300-ohm resistor R1. With S9 set to 60, the loop is loaded by 100-ohm resistor R2. When S9 is set for either 20 or 60, the loop connects via A5R26 to the neutral input of the relay. With S9 set to H1-Z or HUB, 43k-ohm resistor R4 is connected in series with the loop. With S9 set to HUB, resistor R27 connects across both inputs to the relay. With S9 set to EIA, only resistors A5R4 and A5R5 are in series with the loop. Electronic relay A5Q1-A5Q6 isolates the external loop from the rest of the Analyzer circuits. FILTER switch S7, when set to IN, connects capacitor A5C3 across the loop to filter out noise and transients.

Time-Base Circuits (Fig. 14 and 30)

3.31 With BIT RATE range switch S1 set to range A, as shown, the oscillator frequency is controlled by the 1.92mHz crystal, Y7, and output gate G18 is enabled. The negative transitions of the 1.92mHz signal from the oscillator step downcounter FF1-FF8. The 1-output of each bistable, therefore, provides a different output frequency as follows:

OUTPUT	DIVIDE 1.92MHZ BY	FREQUENCY
OSC OUT	1	(200 x 9600)Hz
FF1	2	(200 x 4800)Hz
FF2	4	(200 x 2400)Hz

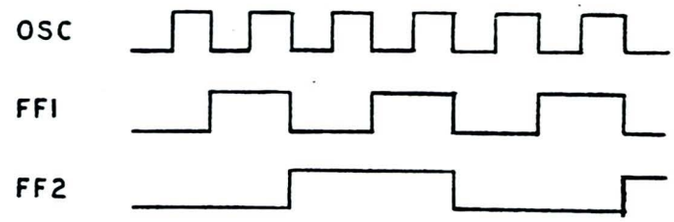
OUTPUT	DIVIDE 1.92MHZ BY	FREQUENCY
FF3	8	(200 x 1200)Hz
FF4	16	(200 x 600)Hz
FF5	32	(200 x 300)Hz
FF6	64	(200 x 150)Hz
FF7	128	(200 x 75)Hz
FF8	256	(200 x 37.5)Hz
	(192)*	(200 x 50)Hz

*Downcounter FF1-FF8 divides by 192 instead of the normal 256 when FF1 and FF2 are implemented to divide by 3 instead of the normal 4 (Fig. 14).

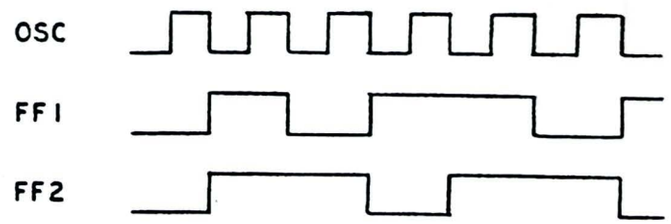
3.32 The setting of BIT RATE select switch S1 determines which gate of G1 through G11 is enabled. For each bit rate selected, the gate enabled connects the correct 200 x bit rate signal to G18. The negative transitions of the output signal (200 x bit) then occur at 200 times the bit rate selected. When the BIT RATE select switch is set to EXT, gate G1 is enabled, thus permitting an external 200 x bit signal to be coupled through amplifier Q1-Q2 to output gate G18.

3.33 When the BIT RATE select switch is set to rate 50, the output of gate G20 goes low to enable gate G21 and disable gate G22. Bistables FF1 and FF2 then divide by 3 instead of the normal 4 (Fig. 14). The 1-output of FF8 is then 1.92mHz divided by 192, or (200 x 50)Hz.

3.34 When the BIT RATE range switch is set to range B, output gate G18 is disabled and output gate G19 is enabled. Also the 1.92mHz crystal, Y7, is disconnected and the oscillator is controlled by one of the optional crystals of Y1 through Y6. The first six positions of the BIT RATE select switch select the optional crystals. When each crystal of Y1 through Y6 is selected, the corresponding gate of G12 through G17, respectively, is enabled. The six gates are strappable



A. DIVIDE BY 4



A. DIVIDE BY 3

Fig. 14 - Time Base, Divide-By-Three Function

to connect either the $\frac{\cdot}{1}$, $\frac{\cdot}{16}$, or $\frac{\cdot}{32}$ signal to output gate G19. Selection of optional crystal frequencies and gate strapping are explained in 1.21 and 4(F).

Sync Circuits (Fig. 31)

3.35 Time-base signal 200 x bit is coupled through G13 and G15 to toggle FF6. FF6 divides 200 x bit by two to produce 100 x bit signal DC at the output of G18. DC is coupled to the distortion counter circuits (not shown) where it is divided by 100 to produce 1 x bit signal BT.

Synchronous (Fig. 31)

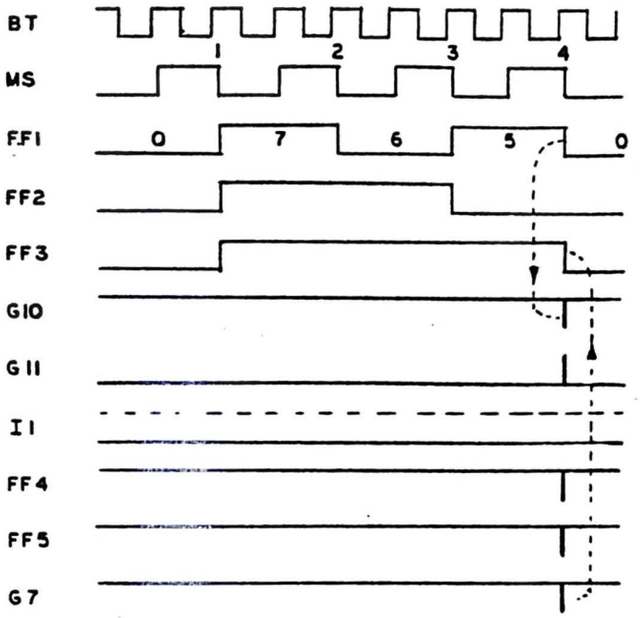
3.36 When MS is synchronous, the sync circuits add pulses to and subtract pulses from DC as required to synchronize BT rate and phase with MS.

Subtracting (Fig. 15A, 15B, and 31)

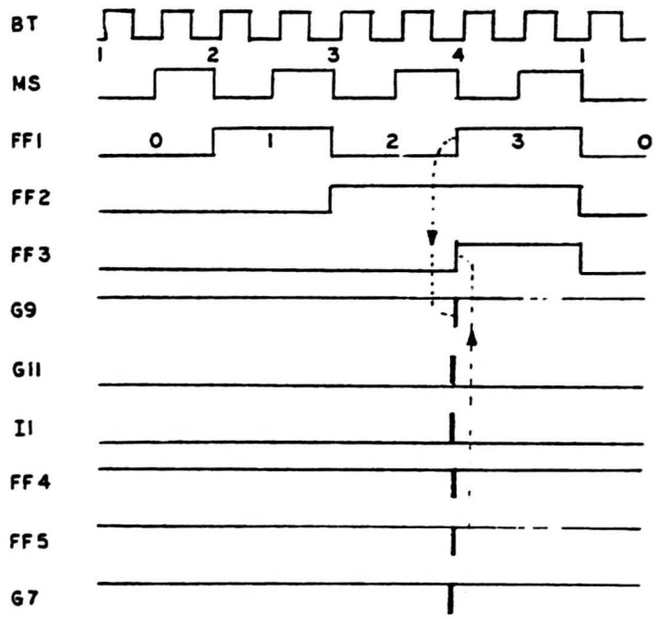
3.37 When BT rate is fast (Fig. 15A) with respect to MS rate, BT will be high during the negative transitions of MS. When BT is high, gates G2 and G5 enable the 0-outputs of FF1 and FF2. MS steps counter FF1-FF3. At each fourth negative transition of MS, G10 goes low, causing G11 to go high. With G11 high, the next negative transition of 200 x bit resets FF4. With FF4 reset, the next negative transition of 200 x bit resets FF5. The resultant positive transition at the 0-output of FF5 produces a negative transition at the output of G8, which resets FF3. During the time when FF4 is reset and FF5 is set, G12 goes low (Fig. 15B). The low disables G13 just long enough to subtract one pulse from 200 x bit at the output of G13. Since each fourth negative transition of MS thus initiates the removal of one pulse in 800 from 200 x bit, the effect is to remove 1/2 pulse in 400 from 100 x bit signal DC. This function produces only a slight corrective shift in the phase and rate of BT. In this way, pulses are subtracted from DC until BT shifts into phase and rate with MS.

Adding (Fig. 15C, 15D, and 31)

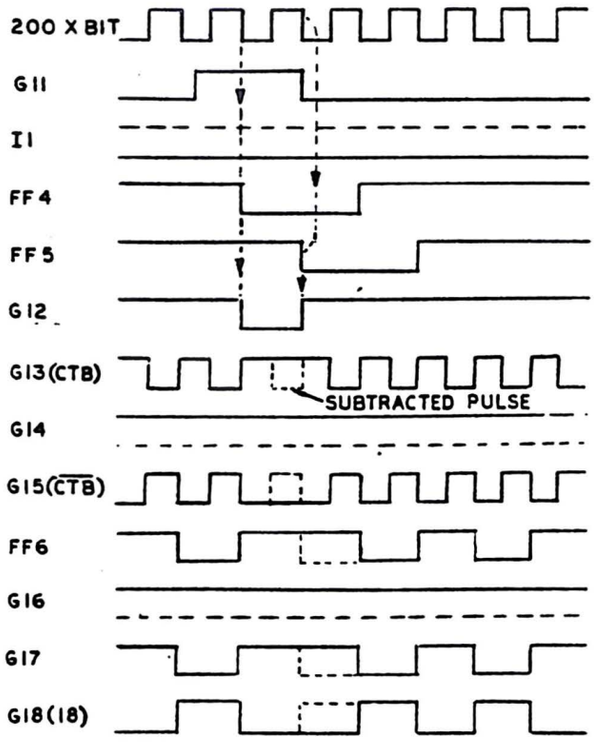
3.38 When BT rate is fast with respect to MS rate, BT will be high during the negative transitions of MS. When $\overline{BT}$ is high, gates G1 and G4 enable the 1-outputs of FF1 and FF2. MS steps counter FF1-FF3. At each fourth negative transition of MS, G9 goes low, causing G11 and I1 to go high. With G11 high, a pulse is subtracted from 200 x bit as described in 3.37 above. The high at the output of I1 enables G14. G14 is enabled just long enough to pass one 200 x bit pulse through G14 and G16. The pulse is added to 100 x bit (DC) at the output of G18. The sum effect of having subtracted 1/2 pulse in 400 from DC having added one pulse in 400 to DC is the addition of 1/2 pulse in 400 to DC. This function produces a slight corrective shift in the phase and rate of BT. In this way, pulses are added to DC until BT shifts into phase and rate with MS.



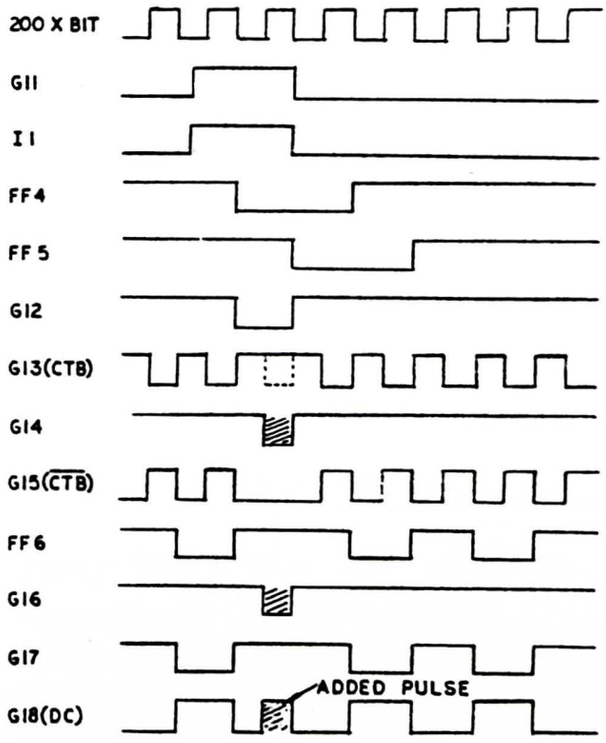
A. BT PHASE EARLY OR RATE FAST



C. BT PHASE LATE OR RATE SLOW



B. SUBTRACT PULSE



D. ADD PULSE

Fig. 15 - Sync Network Timing, Synchronous

Noise Rejection (Fig. 31)

3.39 Note in the timing diagram (Fig. 15A and 15C) that when BT is fast (early) counter FF1-FF3 down counts (7-6-5-4). Note (Fig. 15B) that when BT is slow (late) counter FF1-FF3 up counts (0-1-2-3). Count 4 on the downcount initiates the subtract function. Count 3 on the upcount initiates the add function. Counter FF1-FF3 therefore permits only every fourth negative transition of MS to initiate an add or subtract function. If data signal MS contains noise spikes, they will step the counter but will not initiate the add or subtract functions. The noise spikes will not initiate false add or subtract functions because they occur in random order. That is, as many will occur late as early. They will therefore step the counter alternately up and down, never reaching count 3 or 4. Only the negative transitions of MS are able to complete a count to initiate a true add or subtract function.

Start-Stop (Fig. 16 and 31)

3.40 When the data signal under test is start-stop (Fig. 16), the start-stop sync network inhibits DC (at G15) shortly after the first transition of each stop element of MS and enables DC (at G15) at the first transition of each start element. This function synchronizes DC with the first transition of each start element of data signal MS.

Transition Counter

3.41 DC is coupled to the distortion counter circuits (Fig. 32) where it is divided by 100 to produce 1 x bit timing signal BT. BT steps the transition counter (Fig. 32). Each of the ten output lines (T0 through T9) go low during their corresponding transition of data signal MS (Fig. 21). Lines $\overline{T0}$ and $\overline{T6}$ through $\overline{T9}$ are coupled to the sync circuits (Fig. 31).

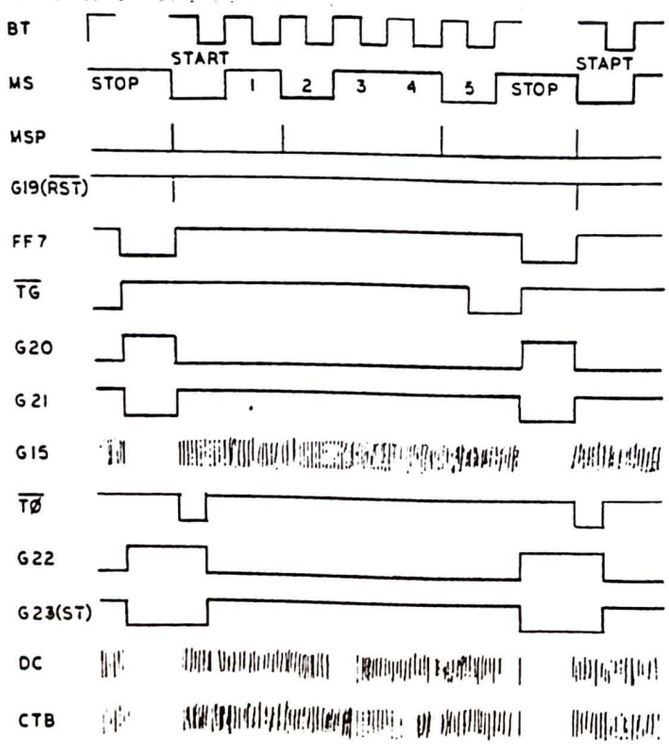


Fig. 16 - Sync Network Timing, Start-Stop

Reset Signal RST (Fig. 16 and 31)

3.42 With the S/S CODE LEVEL switch set to 5, $\overline{T6}$ connects via I6 to FF7. Each positive transition of $\overline{T6}$ resets FF7 prior to the first transition of each start element of MS. The next MSP spike occurs at the first transition of the start element and is inverted by G19 to set FF7. When set, FF7's 1-output goes high to produce a low at the output of G20, which disables G19. Therefore, no further MSP spikes are able to be coupled through G19 until $\overline{T6}$ again resets FF7. Reset signal $\overline{RST}$ is thus produced at G19. $\overline{RST}$ then consists of a train of spikes that coincide with the first transition of each start element of MS.

Synchronization (Fig. 16 and 31)

3.43 Since FF7 is set at the first transition of each start element and reset a half unit later, the output of G21 inhibits DC during the stop element of each MS character, and enables DC at the first transition of each start element.

Stop Transfer Signal ST (Fig. 16 and 31)

3.44 When G21 goes low, G22 goes high, producing a low at the output of G23. When $\overline{T0}$ goes high, G22 goes low, producing a high at the output of G23. The output of G23 (ST) is, therefore, low during the first transition of each start element of MS.

Distortion Counter Circuits (Fig. 32)

3.45 The negative transitions of timing signal DC (100 x bit) step the distortion counter repeatedly from count zero to 99. Both decades repeatedly count from zero to 9 and reset to zero at count ten. The first decade (units) is stepped by DC and the second decade (tens) is stepped by each count ten reset of the first decade.

Decade Weighting (Fig. 17 and 32)

3.46 The binary coded decimal (BCD) notation of the outputs of each decade has 1-2-4-2 weighting instead of the normal 1-2-4-8 weighting (Table V). Up to count four, the decade counts as a conventional binary counter. At count five, however, G1 goes negative to set FF2 and FF3, which resets FF4. This function steps the count to five (1-2-4-2 weighting). The decade then continues to count as a conventional binary and, at count ten (1-2-4-2 weighting), resets to count zero.

TABLE V

DECADE WEIGHTING

1-2-4-8 WEIGHTING		1-2-4-2 WEIGHTING	
0000 = 0	0101 = 5	0000 = 0	1011 = 5
0001 = 1	0110 = 6	0001 = 1	1100 = 6
0010 = 2	0111 = 7	0010 = 2	1101 = 7
0011 = 3	1000 = 8	0011 = 3	1110 = 8
0100 = 4	1001 = 9	0100 = 4	1111 = 9

3.47 As counter outputs FF1, FF2, $\overline{FF3}$, $\overline{FF4}$, FF5, FF6, $\overline{FF7}$, and $\overline{FF8}$ up count from zero to 99, the complementary outputs FF1, FF2, FF3, $\overline{FF5}$, $\overline{FF6}$, FF7, and FF8 down-count from 99 to zero.

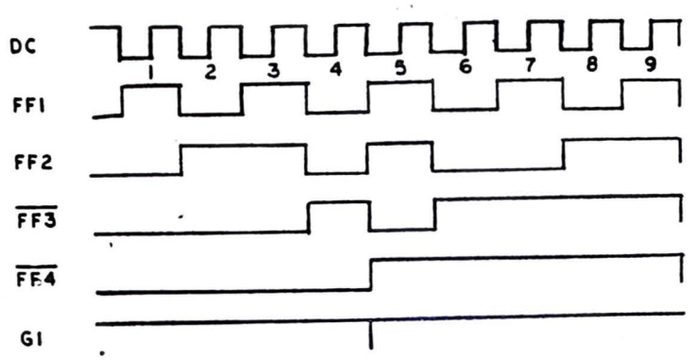


Fig. 17 - Decade Timing

Transfer Gates (Fig. 18 and 32)

3.48 Since BT is low during count zero to 49 and high during count 50 to 99, transfer gates G7 through G20 alternately connect the upcount and downcount (Fig. 18) to the S-inputs of distortion register FF2 through FF8. The BCD count applied to the S-inputs of the distortion register, therefore, steps repeatedly from 50 to zero to 50.

Note: Transfer gates G7 through G20 invert and therefore transform the upcount to a downcount and vice versa.

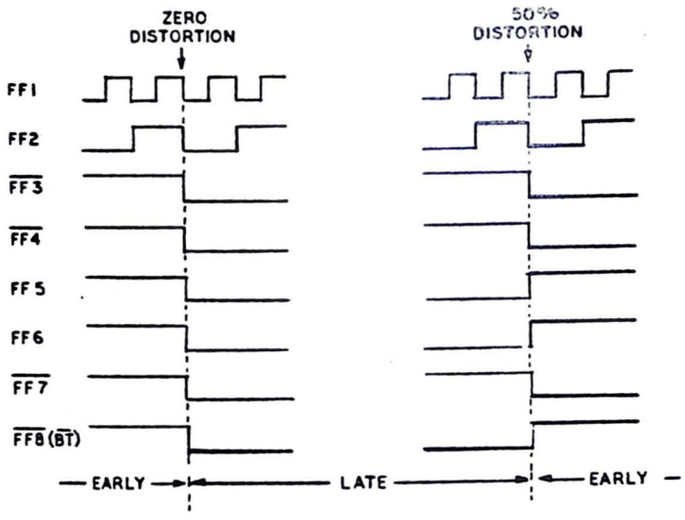


Fig. 18 - Distortion Counter Timing

Distortion Register Circuits (Fig. 18 and 32)

3.49 The 50-to-zero-to-50 count applied to the S-inputs of the distortion register reaches count zero at the ideal time position of each transition of data signal MS. Transfer pulse $\overline{XFR}$ occurs at the actual time positions of the transitions of MS. Each time an $\overline{XFR}$ pulse occurs, it transfers the count into the distortion register. There the count is stored until the next $\overline{XFR}$ pulse transfers a new count. If MS is not distorted, the count transferred will be zero. If MS is distorted (early or late), the count transferred is numerically equal to the per cent of displacement (0-50%).

D/A Converter Circuits (Fig. 32)

3.50 The BCD count stored in the distortion register is coupled through gates G1 through G7, in the D/A converter circuits, to amplifiers AM1 through AM7. The sum of the resultant currents in resistors R4, R8, R12, R16, R20, and R28 deflect meter M1 to the decimal equivalent of the stored BCD count.

Example: Assume that an MS transition occurs 23 per cent late (23% early). $\overline{XFR}$ transfers BCD count 23 (0010 0011) into the register. This produces highs at the 1-outputs of FF7, FF2, and FF3. The three highs produce lows at the outputs of AM1, AM2, and AM6. The sum of the resultant currents in R4, R8, and R24 deflect M1 to read 23 per cent.

Add 1 Per Cent (Fig. 32)

3.51 Note in Fig. 18 that the distortion counter counts correctly from zero to 49 (late distortion) but then steps to count 49 again, skipping count 50. On the downcount from 49 to zero (early distortion), the counter, therefore, always registers one count short. For example, if an MS transition is displaced 20 per cent in advance (early) of its ideal time position, the count transferred will be 19 (one count short). To compensate for early distortion measurement, FF9 in the distortion register adds to a steady count of one to the D/A converter during the entire downcount.

MARKING and SPACING Indicator Lamps (Fig. 32)

3.52 When a data signal (MS) Space-to-Mark transition occurs early, MS and $\overline{BT}$ are high, producing a high at the output of I5, which sets FF1 to light the MARKING indicator lamp.

3.53 When an MS Space-to-Mark transition occurs late, $\overline{MS}$ and $\overline{BT}$ are low producing a high at the output of G5-G6, which resets FF1 to light the SPACING indicator lamp.

3.54 When an MS Mark-to-Space transition occurs early, BT and MS are low, producing a high at the output of G5-G6, which resets FF1 to light the SPACING indicator lamp.

3.55 When an MS Mark-to-Space transition occurs late, $\overline{MS}$ and BT are high, producing a high at the output of I5, which sets FF1 to light the MARKING indicator lamp.

Transfer Circuits (Fig. 32)

3.56 Transitions of data signal MS initiate $\overline{XFR}$ transfer pulses in accordance with 3.57 through 3.60 below.

Bias Distortion (Fig. 19A, 20A, and 32)

3.57 With MODE switch S3B set to BIAS, it disables G2 and enables G1. Each negative transition of $\overline{MS}$, therefore, produces a negative spike at the output of G1. Each time a negative spike occurs it resets FF1, producing a high at the output of G5, which resets FF2. When the 1-output of FF2 goes low, it sets FF1 and drives the output of G4 high to set FF2 and drive the output of G5 low. A positive spike is therefore produced at the output of G5 for each negative transition of $\overline{MS}$. The positive spike at the output of G5 enables G7 long enough to permit one positive pulse of CBT to be coupled through G7 to become transfer pulse $\overline{XFR}$. The other inputs of G7 (PT, G6, ST, and DC) are all high at this time.

End Distortion (Fig. 20 and 32)

Note: End distortion does not apply to synchronous operation. During synchronous operation, S/S CODE LEVEL switch S10A disables gate G2.

3.58 With MODE switch S3B set to END, it disables G1 and enables G2. Each negative transition of MS, therefore, produces a positive spike at the output of G5. Each spike initiates an $\overline{XFR}$ pulse except the spike produced by the first transition of each start element. During the time of that transition, ST is low to disable G7.

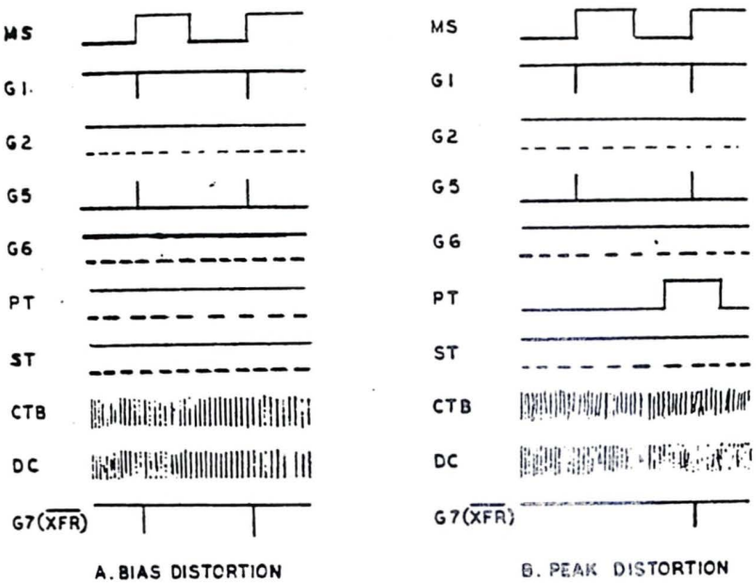


Fig. 19 - Transfer Network Timing, Synchronous

Peak Distortion (Fig. 19B, 20C, and 32)

Note: For synchronous operation, where end distortion does not apply, S/S CODE LEVEL switch disables G2.

3.59 With MODE switch S3B set to PEAK, it enables G1 and G2 in the transfer circuits and enables FF10 in the distortion register circuits. Each negative transition of MS and $\overline{MS}$ produces a positive spike at the output of G5. These spikes can produce an $\overline{XFR}$ pulse only when PT is high. PT will be high only when the comparator network sets FF10 in the distortion register circuits. The comparator network maintains FF10 in the set condition only when the BCD count at the input to the distortion register exceeds the BCD count at the output of the distortion register.

Individual Transitions (Fig. 20D, 21 and 32)

Note: Individual transition measurement does not apply to synchronous operation. During synchronous operation, S/S CODE LEVEL switch S10A disables G6.

3.60 In the distortion counter circuits, BT steps the transition counter (Fig. 21). The transition counter output produces a low on each of lines $\overline{T1}$ through $\overline{T9}$ during the time of the corresponding transitions (first through ninth) in each character of MS. If, for example, TRANSITION SELECT switch S2 is set to 3, it connects line $\overline{T3}$ to gate G6 in the transfer circuits. Gate G6 will therefore enable G7 to produce an $\overline{XFR}$ pulse only during the time of the third transition of each character. Only the third transition of each character can, therefore, initiate a transfer pulse. The MODE switch may be set to either PEAK, BIAS, or END.

Reset Network (Fig. 32)

3.61 When DISPLAY RESET switch S13 is momentarily set to MAN, the resultant negative transition is coupled through SH1, AM1, and AM2 to reset the distortion register. When set to AUTO, the resultant high at the output of I3 enables G2 to pass the reset pulses produced by the 5-Sec timer. The timer produces a reset pulse every five seconds.

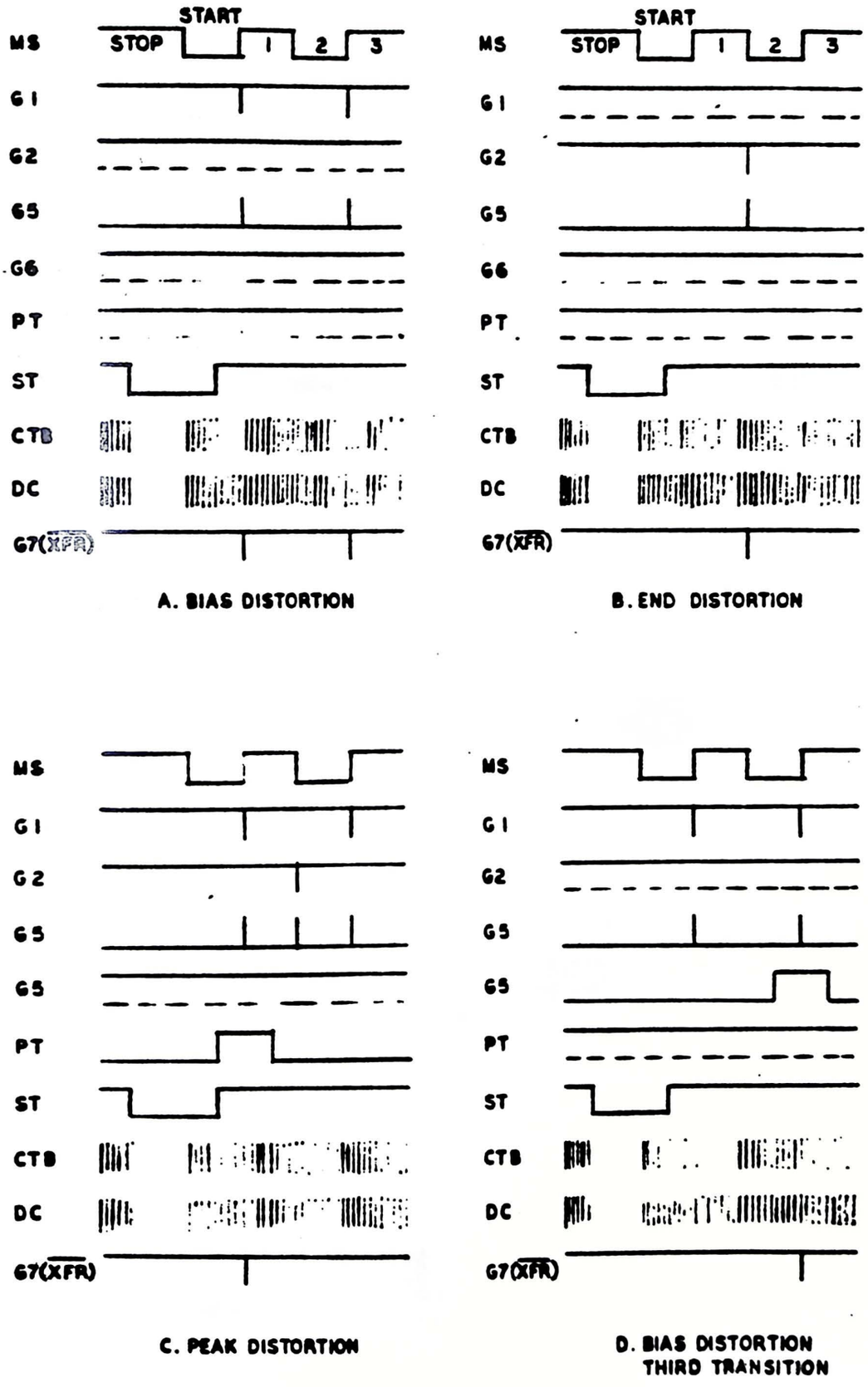


Fig. 20 - Transfer Network Timing, Start-Stop

Reset Signal RST (Fig. 32)

3.62 During stop-start operation, RST consists of a train of spikes that reset the distortion counter and transition counter at the first transition of each start element.

Parity Error Circuits (Fig. 22 and 33)

3.63 The parity error circuits may be strapped at the output of FF3 for either even or odd parity error detection. When strapped for even parity, the circuits emit a parity error pulse ($\overline{PE}$) each time a character of data signal MS contains an odd number of Mark elements. When strapped for odd parity, the circuits emit a $\overline{PE}$ pulse each time a character off data signal MS contains an even number of Mark elements.

Note: Parity error detection applies only when MS is an 8-level code start-stop signal.

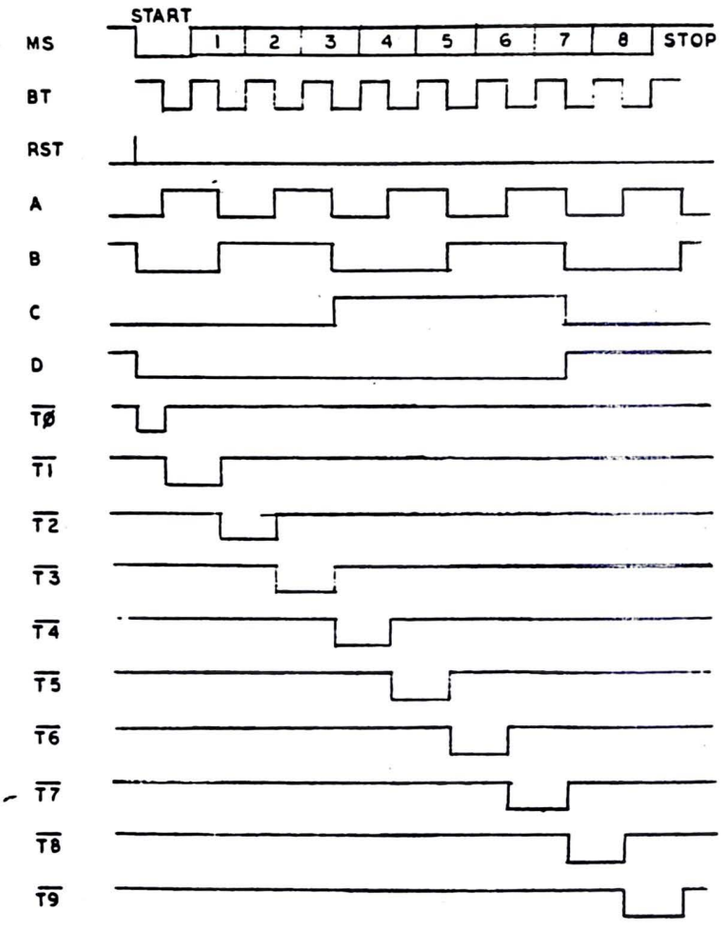


Fig. 21 - Transition Counter Timing

Even Parity (Fig. 22 and 33)

3.64 With $\overline{T9}$ and ST high, BT is able to pass through G8 to produce a train of spikes at the output of SH-4. The spike train steps FF3 in accordance with MS applied to the S- and C-inputs. If MS contains an even number of Mark elements, the 1-output of FF3 will be low when ST goes low. Since the 1-output of FF3 is low, G9 is disabled and the spike produced by ST at the output of I6 is unable to pass through G9. If MS contains an odd number of Mark elements, the 1-output of FF3 will be high when ST goes low. Since the 1-output of FF3 is high, G9 is enabled and the spike produced by ST at the output of I6 passes through G9 to become parity error pulse $\overline{PE}$.

Odd Parity (Fig. 22 and 33)

3.65 The circuit function is the same as that described above except the 0-output of FF3 enables or disables G9 (Fig. 22). An even number of Mark elements in MS, therefore, produces a $\overline{PE}$ pulse and an odd number of Mark elements does not.

Parity Error Indicator Lamp (Fig. 22 and 33)

3.66 PARITY ERROR indicator lamp DS5 lights each time a $\overline{PE}$ pulse is emitted. It then remains lit until PARITY ERROR switch S11 is set to either OFF or RESET.

Reset Signal $\overline{RST}$ (Fig. 22 and 33)

3.67 $\overline{RST}$ resets the parity error circuit at the first transition of each start element.

Bit Error Circuits (Fig. 23 and 33)

3.68 The bit error circuits detect bit errors in either reversal pattern or pseudo random pattern signals. Detection is accomplished by comparing the signal under test (MS) with an identical internally generated signal. As long as the two signals coincide, no errors exist. Should MS lose a bit, the two signals will not coincide during the time of the missing bit and the error is detected. Each time a missing bit is detected, the bit error circuits emit an error pulse ($\overline{EP}$). The bit error circuits are clocked by three spike trains (SP, BTP, and $\overline{BTP}$), all of which are derived from 1 x bit timing signal BT when the rear-panel BIT CLK switch A12S1 is set to INT. With the BIT CLK switch set to EXT, the spike trains may be derived from an external 1 x bit timing signal that is coupled in through amplifier Q5-Q6.

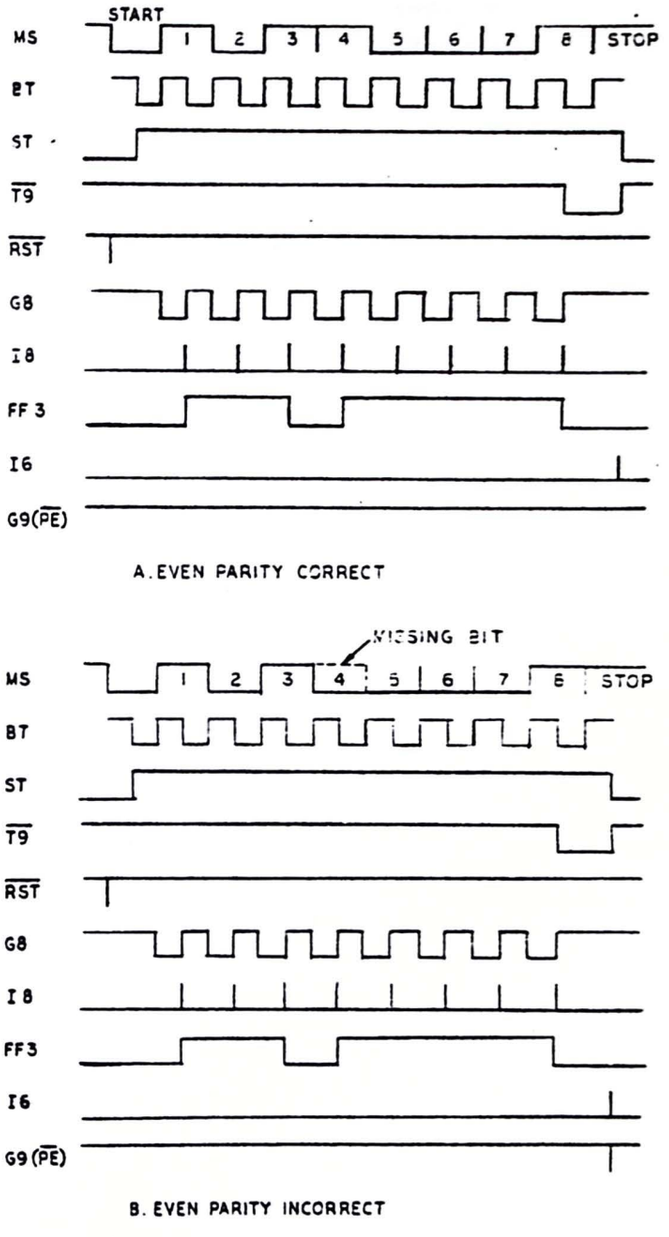


Fig. 22 - Parity Error Timing

Reversal Pattern Error Detection (Fig. 23 and 33)

3.69 Spike train BTP (1 x bit) steps reversal pattern generator FF3, producing reversals at the 0-output. The bit rate of the reversal pattern is the same as the bit rate of the reversal pattern signal under test (MS). MS is coupled into FF1, producing a delayed replica of MS at the output of FF1. When PUSH TO SYNC switch S5 is momentarily depressed, it permits the next SP spike to set FF2, which remains set until the next SP spike resets it. While FF2 is set, its 1-output enables G1 and G2. During the time they are enabled, G1 and G2 permit the output of FF1 to control the stepping of FF3. The output of FF3 is thus synchronized with the delay replica of MS at the output of FF1.

Comparison (Fig. 23 and 33)

3.70 With MODE switch S3B set to REV, it enables G10, and, since FF2 is normally reset, it enables G4. The reversal pattern at the output of FF3 is, therefore, applied to one input of G5 and its complement to one input of G6. The delayed replica of the reversal pattern under test and its complement are applied to the other input of G5 and G6, respectively. Since the two reversal patterns at the inputs to G5 are in phase and the two reversal patterns at the input to G6 are in phase, the output of G5-G6 (G) is at a constant low to disable G12.

Error Pulse (Fig. 23 and 33)

3.71 Should MS lose a bit, G will go high during the time of the missing bit. G12 is thus enabled long enough to pass one SP spike, which becomes error pulse $\overline{EP}$ at the output of G12.

Pseudo Random Pattern Generator (Fig. 24 and 33)

3.72 The bit error circuits contain a pseudo random pattern generator that consists, essentially, of the two 5-bit shift registers, bistable FF4, and gates G7 and G8. The output of G7-G8 feeds back through I5, G11, G4, and I2 to the input of the first 5-bit register. Depending on the strapping of the connection between the two 5-bit registers, the generator produces either a 511-bit pattern or a 2047-bit pattern. For the 511-bit pattern, the strapping bypasses the last two bistables in the first 5-bit register. The two 5-bit registers plus FF4 then constitute a 9-bit shift register. For the 2047-bit pattern, the strapping connects the output of the

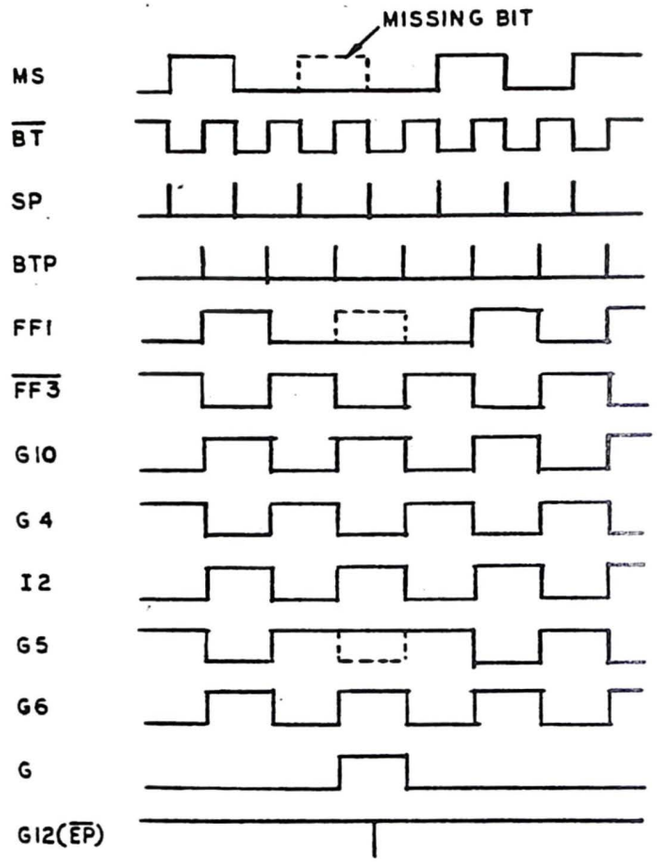


Fig. 23 - Bit Error, Reversals, Timing

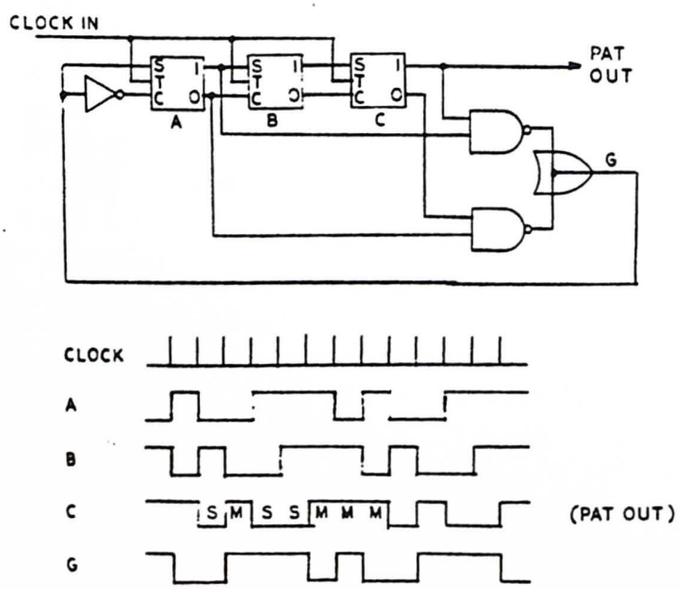


Fig. 24 - Pseudo Random Pattern Generator

first 5-bit register to the input of the second register. The two 5-bit registers plus FF4 then constitute an 11-bit shift register. The input to amplifier Q1-A4 may be strapped to connect either the random signal or its complement to front-panel connector TP1. A timing diagram for a random pattern generator using a 9-bit or 11-bit shift register, would be unwieldy. Therefore, a hypothetical random pattern generator using a 3-bit shift register is shown in Fig. 24 and described below. Before the first clock spike occurs, the three bistables may be in any state. In Fig. 24 it is assumed that A is reset and B and C are each set. G, therefore, is high. The clock spikes then clock G into A to produce the random pattern. The random pattern repeats itself every 7 bit and is therefore a pseudo random pattern. The relationship between the number of bistables in the shift register and the number of bits in the random pattern is given by the following expression: $2^N - 1$ = number of bits, where N is the number of bistables. The hypothetical generator (Fig. 24) using a 3-bit register therefore produces a 7-bit random pattern: $2^3 - 1 = 8 - 1 = 7$. The actual generator (Fig. 33) using a 9-bit register produces a 511-bit random pattern: $2^9 - 1 = 512 - 1 = 511$. The actual generator using an 11-bit register produces a 2047-bit random pattern: $2^{11} - 1 = 2048 - 1 = 2047$.

Random Pattern Error Detection (Fig. 33)

Note: To detect errors in the pseudo random pattern, the data signal under test (MS) must consist of a pseudo random pattern signal identical to the pattern produced by the internal pseudo random pattern generator. The correct pseudo random pattern signal may be obtained from one of two sources: either from the TEST SIG OUTPUT of another Analyzer DMS-303A or from Pattern Generator PG-303A.

3.73 Spike train BTP steps the pseudo random pattern generator to produce a random pattern identical to the random pattern that constitutes the data signal under test (MS). When PUSH TO SYNC switch S5 is momentarily depressed, the next SP spike sets FF2. When S5 is released, the next SP spike resets FF2. While set, FF2 disables G4 (disrupting the random pattern generator feedback) and enables G3. While enabled, G3 feeds the incoming pseudo random pattern into the pseudo random pattern generator. When FF2 resets to its normal condition. G3 is disabled and G4 is enabled. The random pattern from the generator is then synchronized with the incoming random pattern. The two signals will be coincident at the inputs to G5 and G6, producing a constant low at the output of G5-G6 (G). G12 is therefore disabled. Should MS lose a bit, G will go high to enable G12 long enough to pass one SP spike, which becomes error pulse $\overline{EP}$ at the output of G12.

Error Counting Circuits (Fig. 33)

3.74 With MODE switch S3B set to PARITY COUNT, it enables G4 in the error counting circuits to pass all parity error pulses ($\overline{PE}$) to the input of the error counter. With MODE switch S3B set to either REV or RAND, it enables G12 in the bit error circuits to pass any bit error pulses $\overline{EP}$ to the input of the error counter.

Error Counter (Fig. 33)

3.75 The error counter, consisting of two decade counters, counts up to 50 $\overline{EP}$ or $\overline{PE}$ pulses. The BCD output of the counter is continuously monitored by the D/A converter circuits. The D/A converter converts the BCD output of the error counter to an equivalent analog current that drives front-panel meter M1. Each time an error pulse ($\overline{PE}$ or $\overline{EP}$) occurs, the counter steps up 1 count and the meter pointer advances one division. When 51 errors have occurred and the counter reaches count 51, G5 goes low to light OVERFLOW indicator lamp DS4, and it is coupled through G3 to inhibit the error counter and disable G1, which inhibits the input to the interval counter. The error count and interval count then stop until the error counter decades are reset to count zero by one error count reset pulse (ECR) from the output of the reset circuits (see 3.77 below). With the error counter reset to zero, G5 goes high to extinguish OVERFLOW indicator lamp DS4, and to enable the error counter and interval counter. Then the parity error or bit error count begins again.

Interval Counter (Fig. 33)

3.76 While the error counter is counting parity or bit errors, the interval counter is counting SP spikes which occur one per data-signal (MS) bit. The interval counter, consisting of six decade counters, can count as high as 10^6 data-signal (MS) bits. ERROR COUNT INTERVAL switch S4 connects the output of either the second, third, fourth, fifth, or sixth decade to the T-input of FF1. When the selected number of MS bits (10^2, 10^3, 10^4, 10^5, or 10^6, respectively) has occurred, the wiper of S4A goes low to reset FF1. The high at the 0-output of FF1 lights COUNT COMP indicator lamp DS3 and produces a low at the output of I2 to inhibit the input to the error counter and interval counter. The 1-output of FF1 goes low to enable the automatic section of the reset circuits (see 3.77 below). Since the error counter is inhibited, the meter indicates how many bit errors have occurred during the error-count interval.

Reset Circuits (Fig. 33)

3.77 When DISPLAY RESET switch S13 is momentarily depressed to the MAN position, the resultant negative transition connects SH1 and AM1 to be one error count reset pulse $\overline{ECR}$. $\overline{ECR}$ and ECR set AHFF1 and reset the interval counter and error counter. When S1 is set to AUTO, it enables G2. With G2 enabled, ECR and $\overline{ECR}$ are produced automatically five seconds later by the 5-second timer. The timer is disabled by the 1-output of FF1 until the interval count reaches the selected count. At that time $\overline{CS}$ enables the timer and five seconds later ECR and $\overline{ECR}$ reset the two counters and set FF1. With FF1 set, its 1-output disables the reset circuits.

Summary of Major Signal Functions

3.78 The major signal functions are listed in Table VI.

TABLE VI

MAJOR SIGNAL FUNCTIONS

SIGNAL	DEFINITION	FUNCTION
MS $\overline{MS}$	Mark-Space	Logic-level (+5-volt Mark, 0-volt Space) replica of data signal under test.
MSP	Mark-Space pulse	Train of positive spikes that coincide with negative transitions of MS.
200 X BIT	----------	Time-base signal, square-wave, negative transitions occur at 200 times the bit rate of MS.
CTB $\overline{CTB}$	Corrected time base	200 x bit timing signal derived from 200 X BIT and synchronized with MS.
DC	Distortion count	100 x bit timing signal derived from CTB.
BT $\overline{BT}$	Bit time	1 x bit timing signal derived from DC.
1 and $\overline{1}$ through 40 and $\overline{40}$	----------	Binary coded decimal (BCD) output of distortion counter. Derived from counting negative transitions of DC. Steps from 50 through 0 through 50 during the interval of each MS bit.
1% through 40% & ADD 1%	----------	BCD output of distortion register. Derived from BCD output of distortion counter.
$\overline{XFR}$	Transfer pulse	Train of spikes that coincide with transitions of MS. Each spike initiates transfer of BCD output of distortion counter into distortion register.
ST	Stop transfer	During start-stop operation, inhibits $\overline{XFR}$ during time of first transition of each start element of MS.

TABLE VI (Cont'd)

SIGNAL	DEFINITION	FUNCTION
RST $\overline{\text{RST}}$	Reset pulse	Train of spikes that coincide with the first transition of each start element of MS. Resets distortion counter and parity error circuits at that time.
PT	Peak transfer	For peak distortion measurement, inhibits $\overline{\text{XFR}}$ except when BCD count at input to distortion register exceeds BCD count at output.
$\overline{\text{T0}}$ through $\overline{\text{T9}}$	Transition	During start-stop operation, each line provides a low pulse at the time of corresponding transition (of 0 through 9) of each character.
EL $\overline{\text{EL}}$	Early-late	Lights MARKING or SPACING indicator lamp as required.
$\overline{\text{PE}}$	Parity error	For parity error detection (When MS is 8-level code start-stop), a $\overline{\text{PE}}$ pulse occurs for each character of $\overline{\text{MS}}$ that contains parity error.
$\overline{\text{EP}}$	Error pulse	For bit error detection (When MS is synchronous reversal or pseudo random), an $\overline{\text{EP}}$ pulse occurs each time MS loses a bit.
CT1 thru CT40	-	BCD output of error counter. Count reflects number of $\overline{\text{PE}}$ or $\overline{\text{EP}}$ pulses that occur during a given interval.
SP	Spikes, positive	Train of spikes that coincide with transitions of MS. Steps interval counter.
OP	Operate	Disables interval counter during manual synchronization of MS and internal reversal of pseudo random pattern.
$\overline{\text{CS}}$	Count stop	Enables automatic reset circuits when interval count is complete.
ECR $\overline{\text{ECR}}$	Error count reset	Resets error counter and interval counter either when DISPLAY RESET switch is momentarily set to MAN or automatically, five seconds after error count reaches count 51 (overflow).

(E) Power Supply Circuits (Fig. 25 and 26)

3.79 Operating voltages for the Analyzer circuits are obtained from three separate, but interrelated, regulated power supplies furnishing outputs of +15 volts, -15 volts, and +5 volts. The essentials of these power supplies are depicted in the functional block diagram of Fig. 26. One power transformer is used for the three supplies; full-wave rectification, in conjunction with center-tapped secondary windings, is also used in all three cases. Rectifiers CR3 and CR4 are connected in opposite polarity to the other rectifiers, as required to furnish a negative 15-volt output with respect to ground. The Zener reference diode for the +15-volt supply is also used as the reference source for the +5-volt supply. The remaining circuitry of these supplies is conventional in configuration and in circuit details. The 5-volt power supply employs a series-regulator circuit with a protective over-voltage circuit connected across the output terminals. The 5-volt supply is the operating power source for all the integrated-circuit modules of the Analyzer. For this reason, prevention of an over-voltage condition at the output of this supply is essential. An over-voltage condition would probably result in the destruction of many of the integrated-circuit modules in a small fraction of a second.

3.80 The over-voltage protection circuit (Fig. 25) functions in the following manner. Under normal operating conditions Zener diode VR3 is back-biased (nonconducting), thereby keeping transistor Q9 in a cut-off state. The SCR (CR7) is thereby also nonconducting, since its gate electrode is at ground (0-volt) potential when Q9 is nonconducting. Any over-voltage condition of greater than 7.5 volts will cause Zener VR3 to break down and will thereby turn on both Q9 and CR7 to full conduction. The fully conducting SCR effectively short-circuits the power supply and blows dc fuse F3, which is located at the input to the series regulator stage. This removes the supply from service. The circuit operates automatically and is self-resetting after the fuse is replaced and the fault condition is remedied.

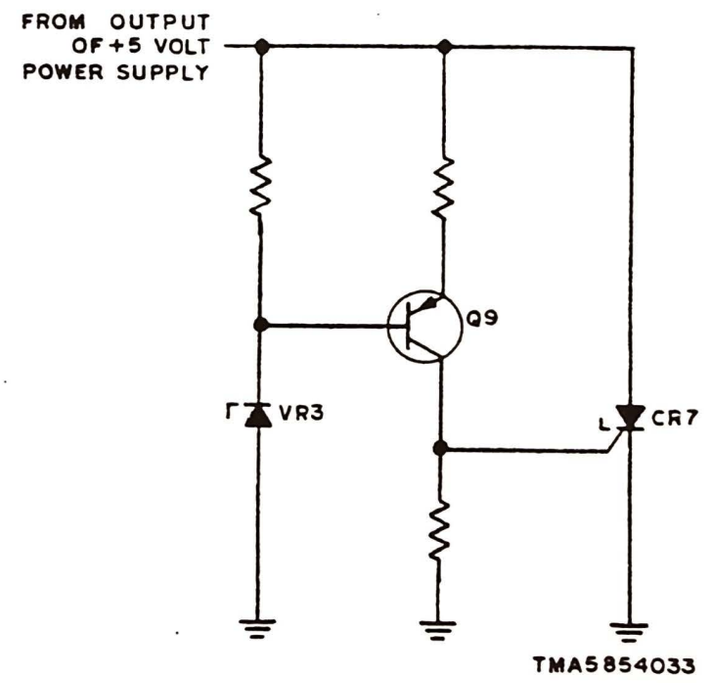


Fig. 25 - Over-Voltage Protection Network

3.81 Each of the three supplies contains a series dc fuse for the purpose of short-circuit protection. It should be noted that a momentary short circuit will not normally cause a fuse to open; the short-circuit condition must be sustained in order to blow the fuse. In either case, full protection is provided for all circuit components.

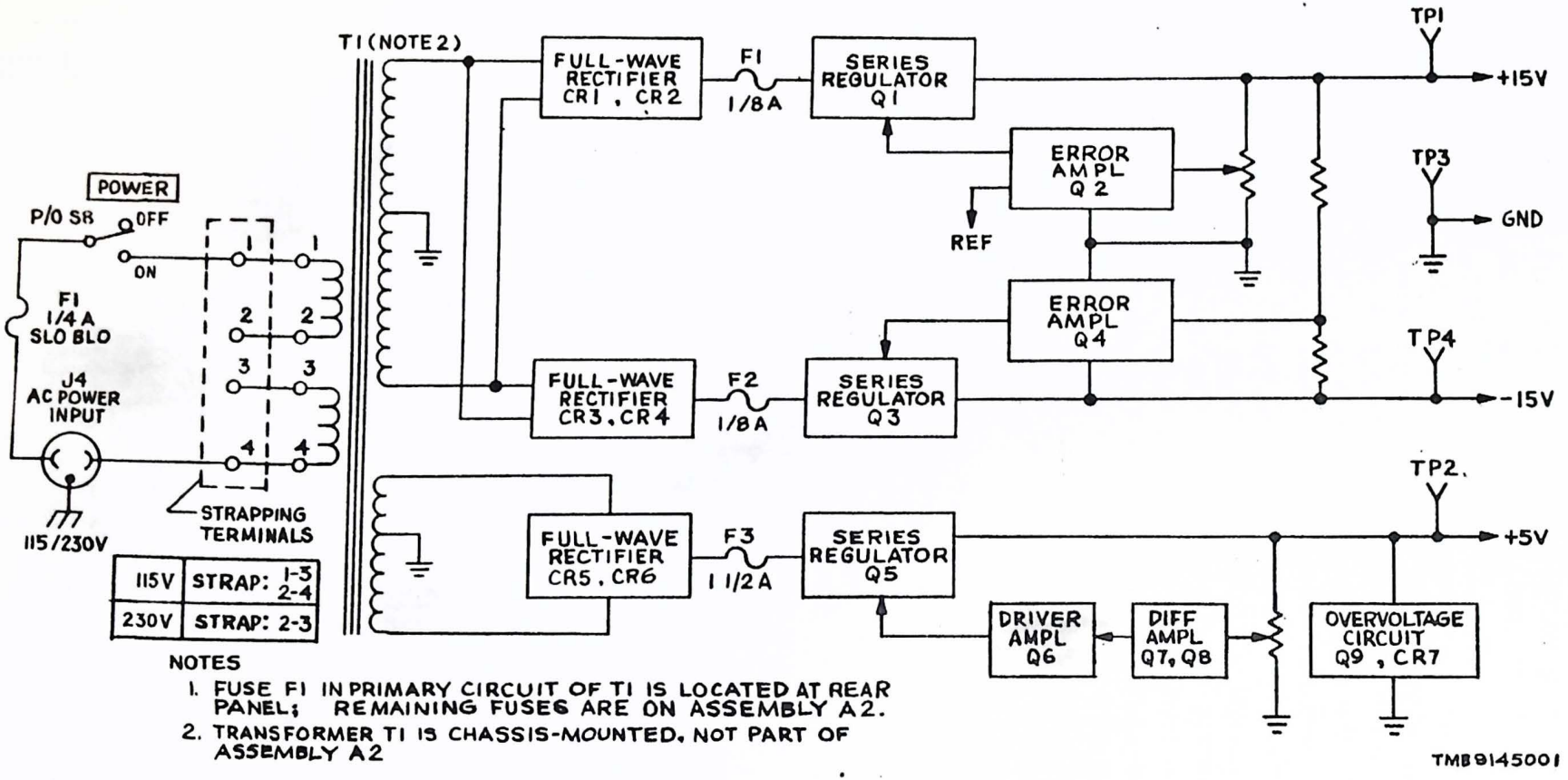
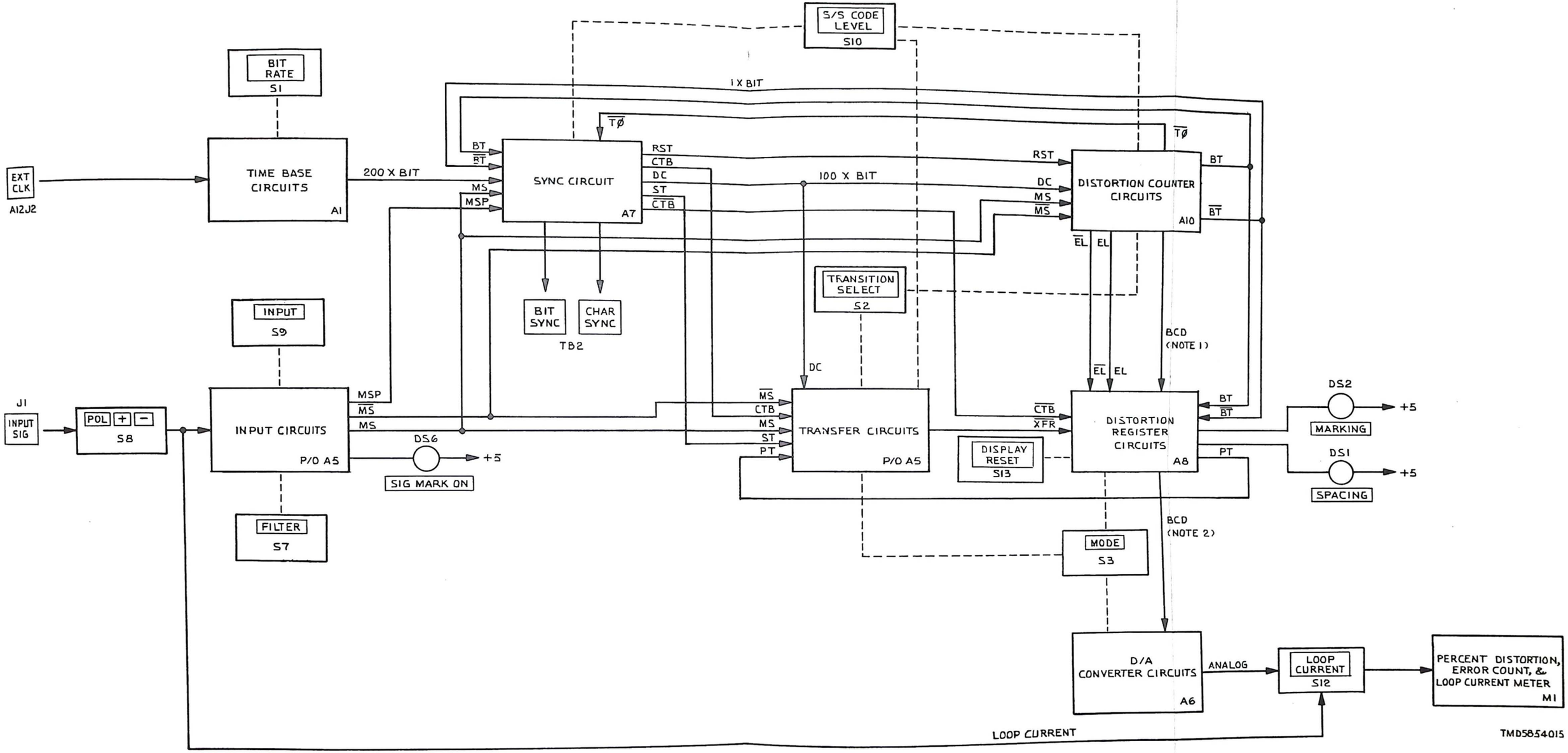


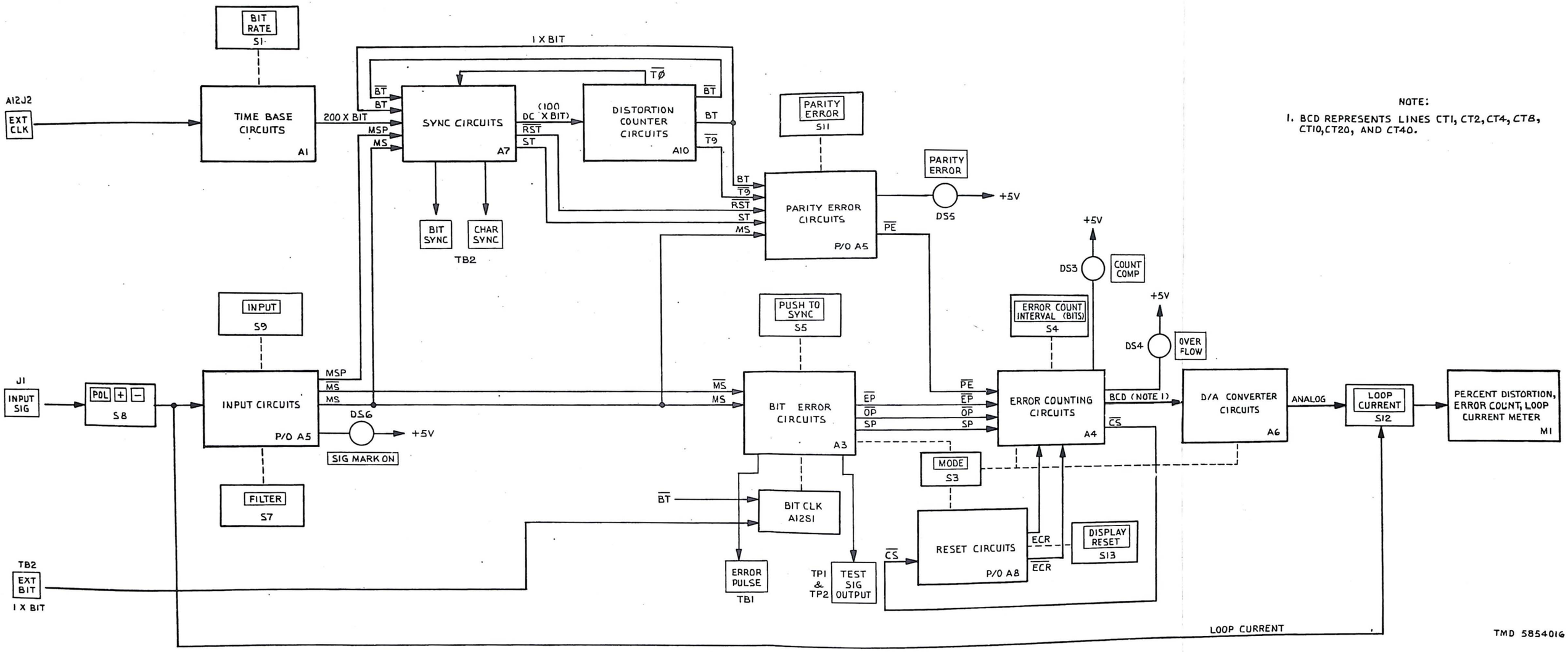
Fig. 26 - Power Supply Circuits - Block Diagram



NOTES:

1. BCD REPRESENTS LINES 1, $\overline{1}$, 2A, $\overline{2A}$, 4, $\overline{4}$, 2B, $\overline{2B}$, 4 $\overline{4}$ 2B $\overline{2B}$ 10 $\overline{10}$ 20 $\overline{20}$ 40 AND $\overline{40}$.
2. BCD REPRESENTS LINES 1%, 2%A, 4%, 2%B, 10%, 20% 40% AND ADD 1%.

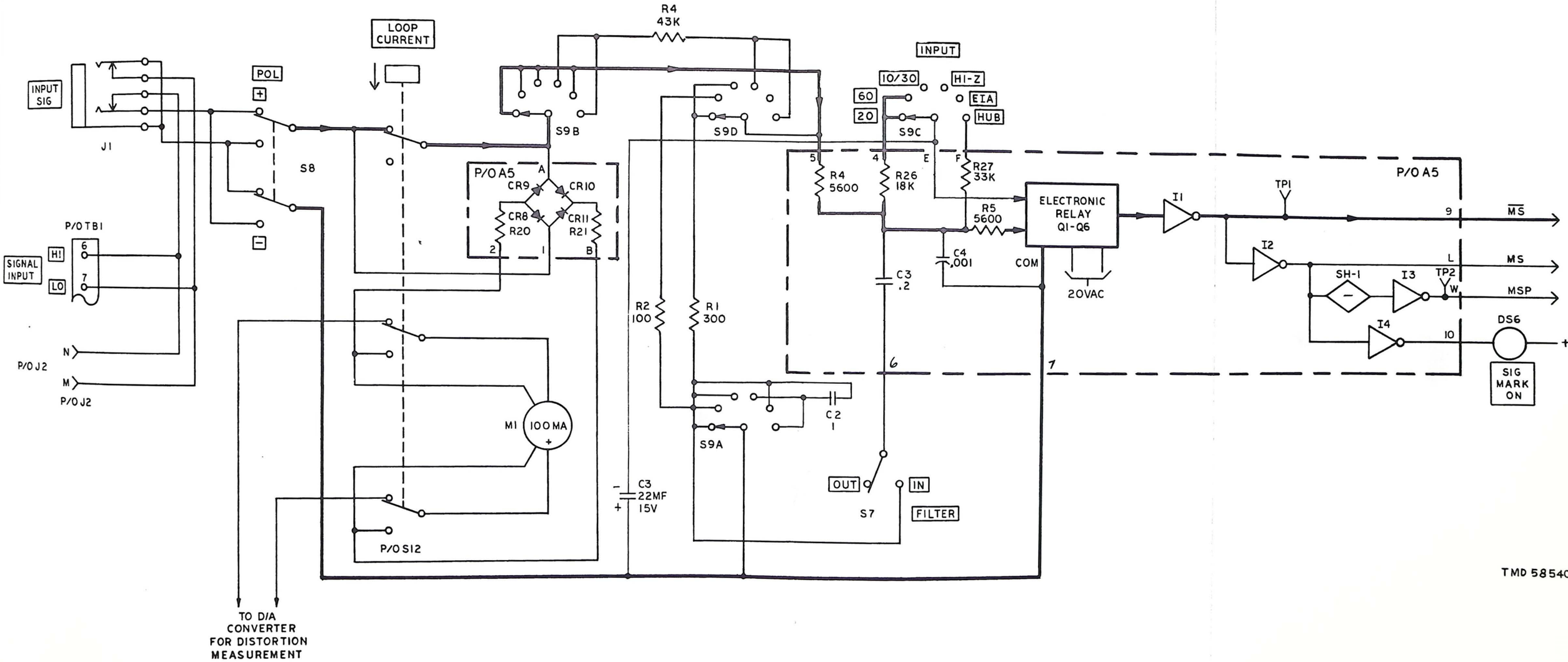
Fig. 27 - Detailed Block Diagram - Distortion Measurement



NOTE:

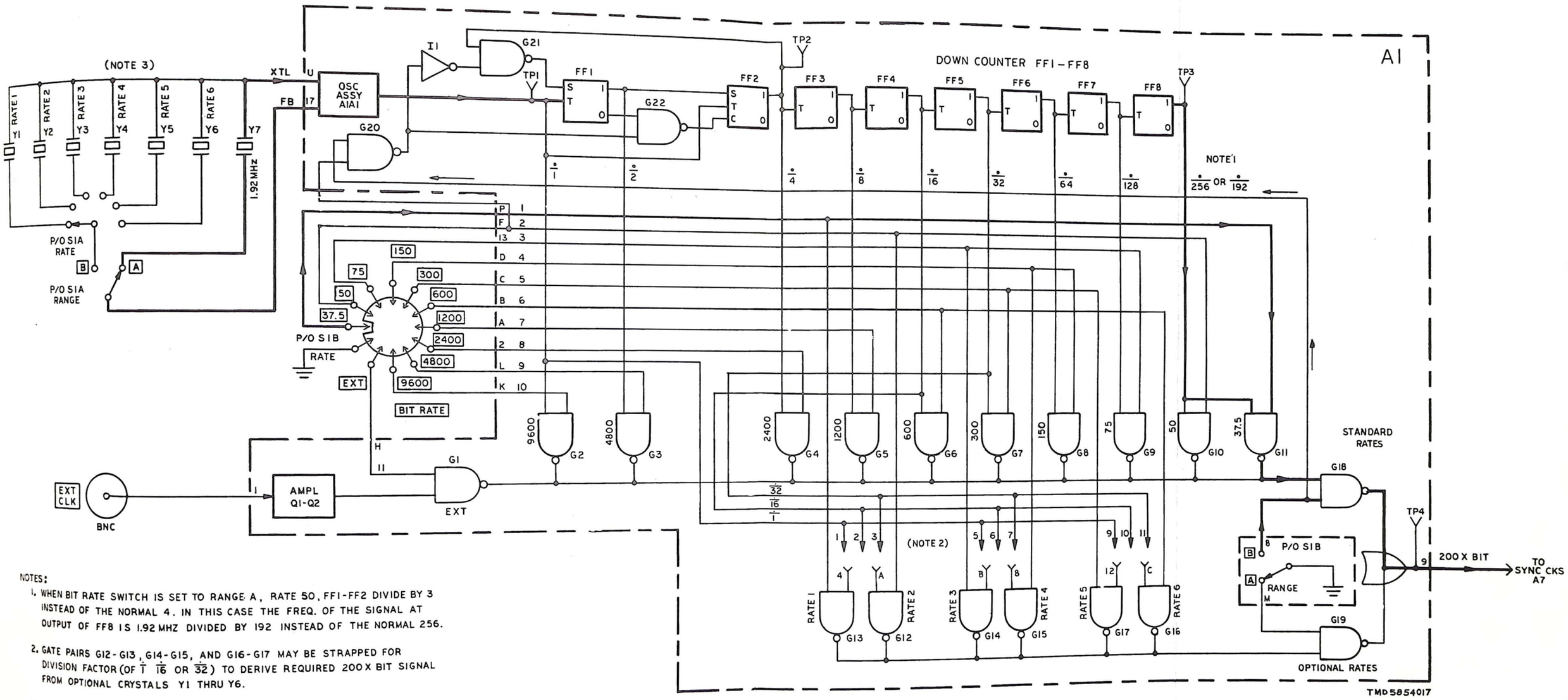
1. BCD REPRESENTS LINES CT1, CT2, CT4, CT8, CT10, CT20, AND CT40.

Fig. 28 - Detailed Block Diagram - Error Detection and Counting



TMD 5854018

Fig. 29 - Simplified Schematic Diagram - Input Circuits



NOTES:

1. WHEN BIT RATE SWITCH IS SET TO RANGE A, RATE 50, FF1-FF2 DIVIDE BY 3 INSTEAD OF THE NORMAL 4. IN THIS CASE THE FREQ. OF THE SIGNAL AT OUTPUT OF FF8 IS 1.92 MHZ DIVIDED BY 192 INSTEAD OF THE NORMAL 256.
2. GATE PAIRS G12-G13, G14-G15, AND G16-G17 MAY BE STRAPPED FOR DIVISION FACTOR (OF $\overline{1}$ $\overline{16}$ OR $\overline{32}$) TO DERIVE REQUIRED 200X BIT SIGNAL FROM OPTIONAL CRYSTALS Y1 THRU Y6.
3. CRYSTALS Y1 THRU Y6 ARE OPTIONAL ITEMS.

Fig. 30 - Logic Diagram - Time-Base Circuits

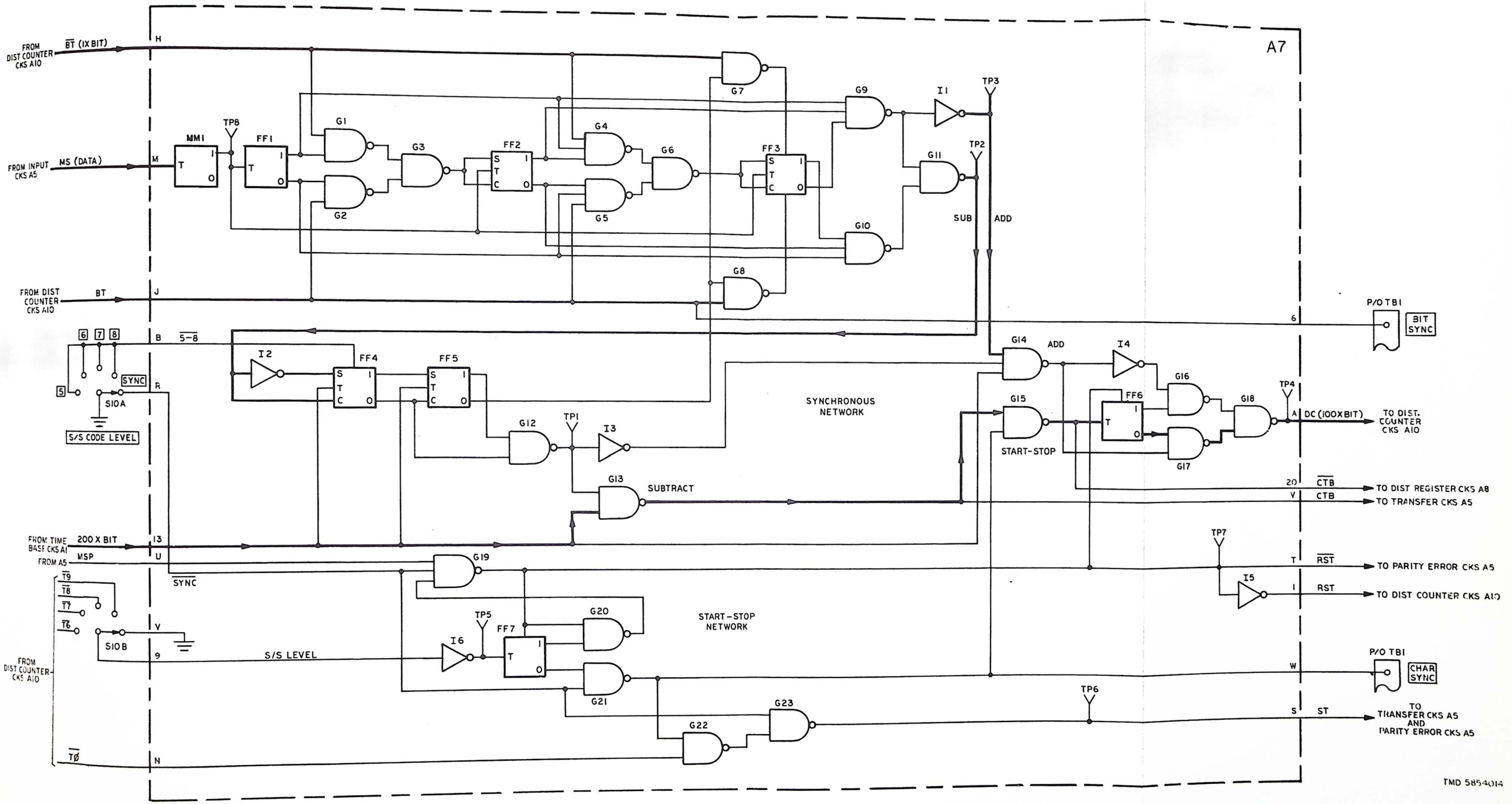
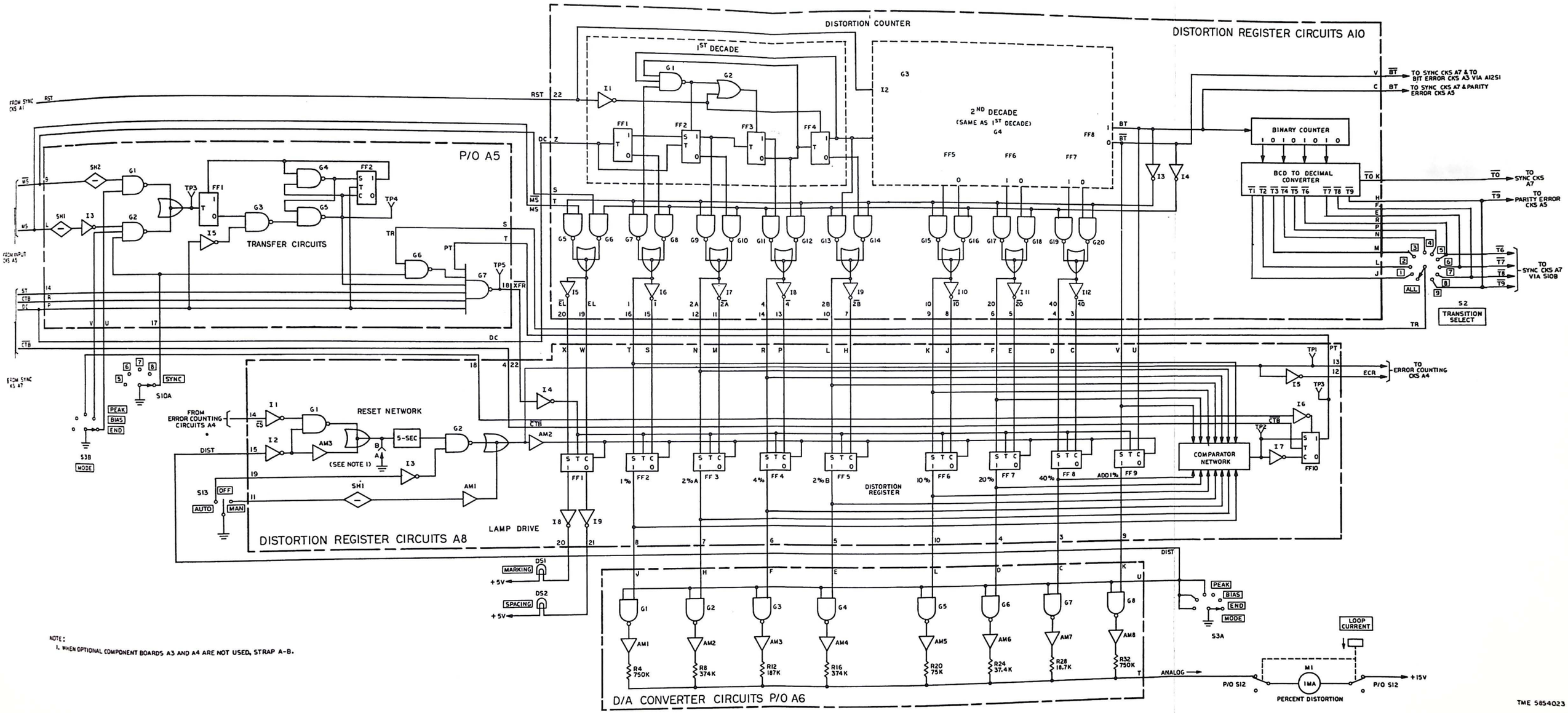


Fig. 31 - Logic Diagram - Sync Circuits



NOTE:
1. WHEN OPTIONAL COMPONENT BOARDS A3 AND A4 ARE NOT USED, STRAP A-B.

TME 5854023

Fig. 32 - Logic Diagram - Distortion Measurement Circuits

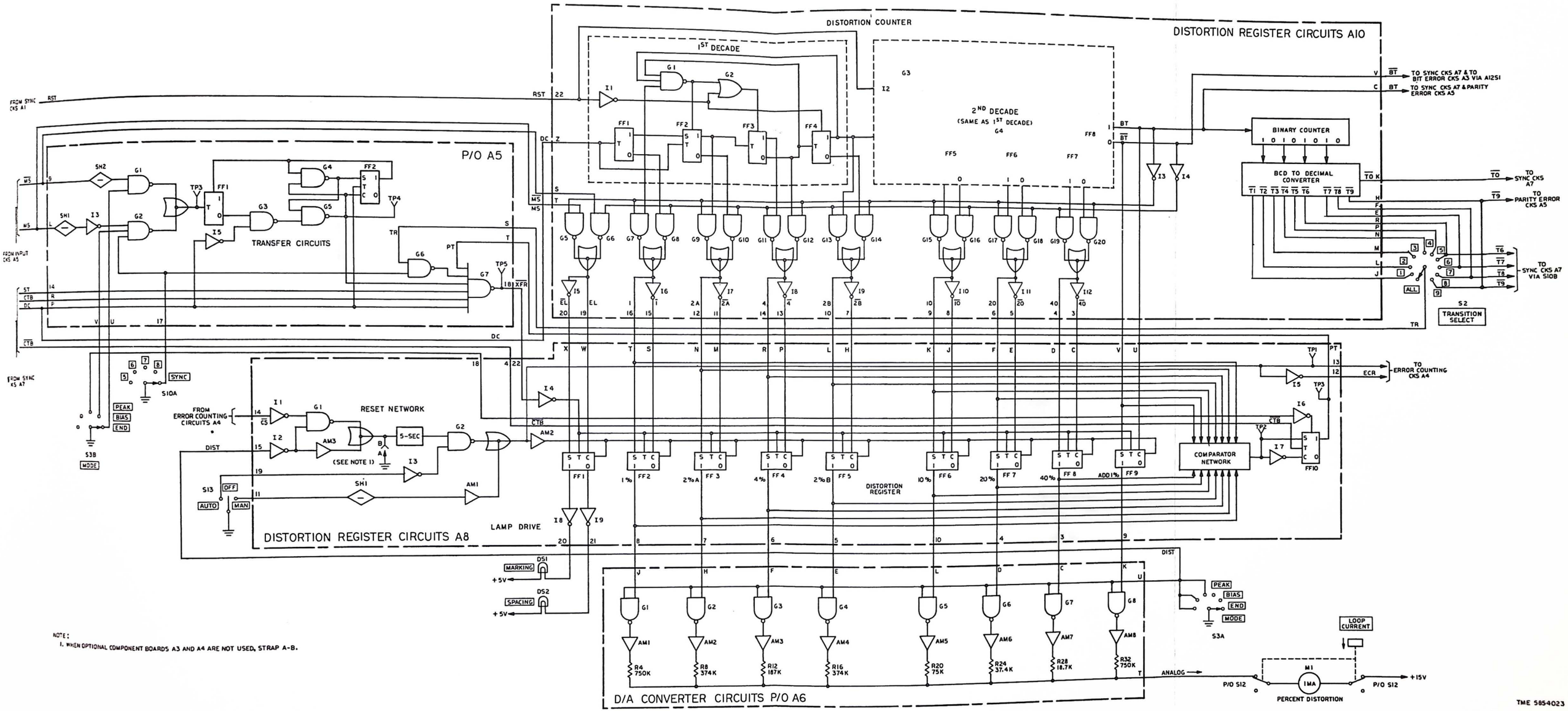
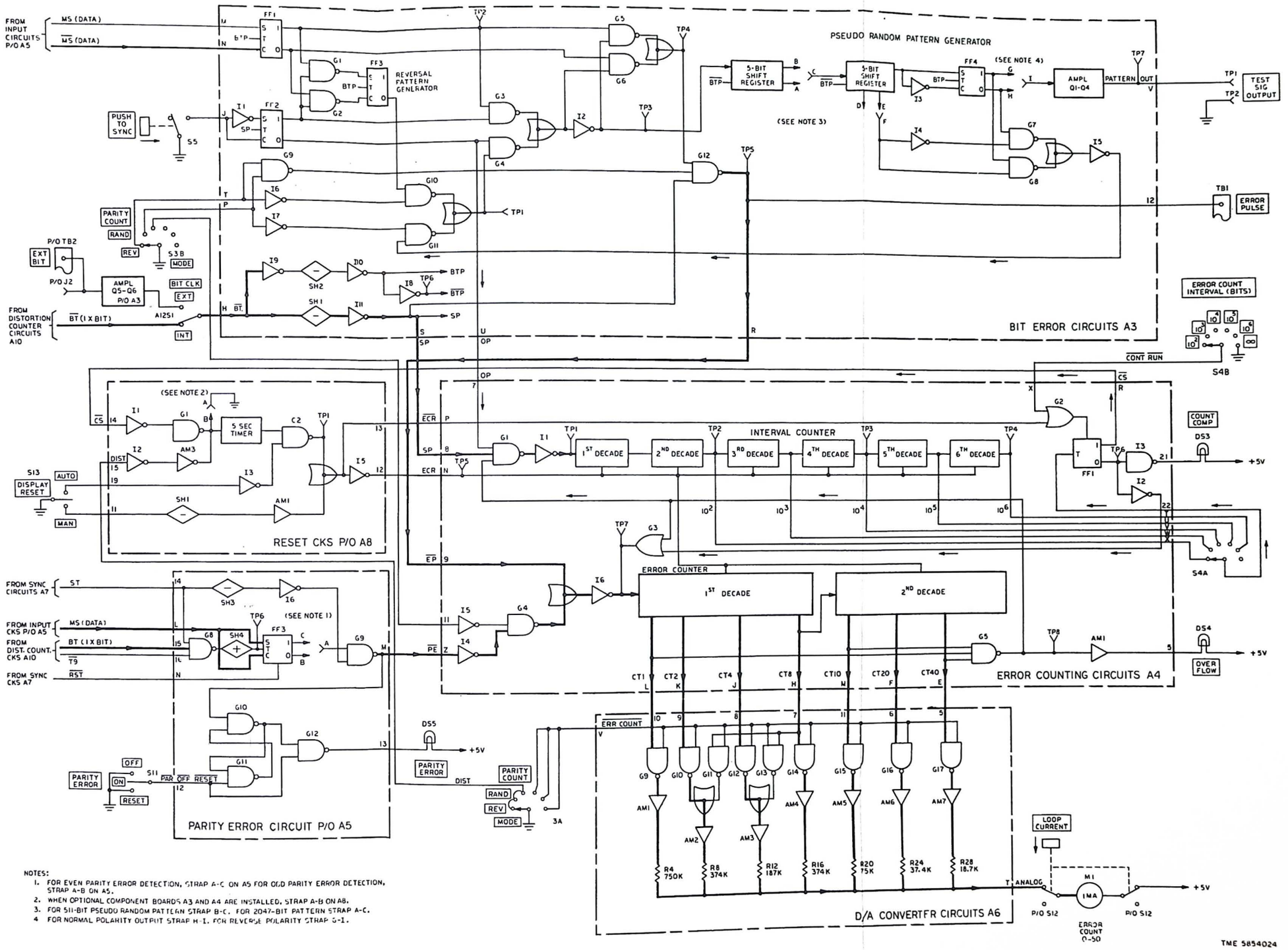


Fig. 32 - Logic Diagram - Distortion Measurement Circuits



NOTES:
1. FOR EVEN PARITY ERROR DETECTION, STRAP A-C ON A5 FOR ODD PARITY ERROR DETECTION, STRAP A-B ON A5.
2. WHEN OPTIONAL COMPONENT BOARDS A3 AND A4 ARE INSTALLED, STRAP A-B ON A8.
3. FOR 511-BIT PSEUDO RANDOM PATTERN STRAP B-C. FOR 2047-BIT PATTERN STRAP A-C.
4. FOR NORMAL POLARITY OUTPUT STRAP H-I. FOR REVERSE POLARITY STRAP G-I.

Fig. 33 - Logic Diagram - Error Counting Circuits

4. MAINTENANCE

4.01 This section provides performance, troubleshooting, repair, and field installation procedures for the Analyzer. For schematic and parts location diagrams, see Fig. 34 through 55.

(A) Required Test Equipment

4.02 Table VII lists test equipment required for maintenance.

TABLE VII

REQUIRED TEST EQUIPMENT

NAME	COMMON NAME	FUNCTION
Oscilloscope, Tektronix type 535, or equivalent	Oscilloscope	For waveform observation.
Multimeter, KS-14510-L1, or equivalent	Multimeter	For voltage and resistance measurement.
Pattern Generator, PG-303A, or equivalent	Pattern Generator	To provide test pattern signals.

(B) Performance Tests

4.03 Perform the procedures outlined in 4.04 through 4.07 in the order given.

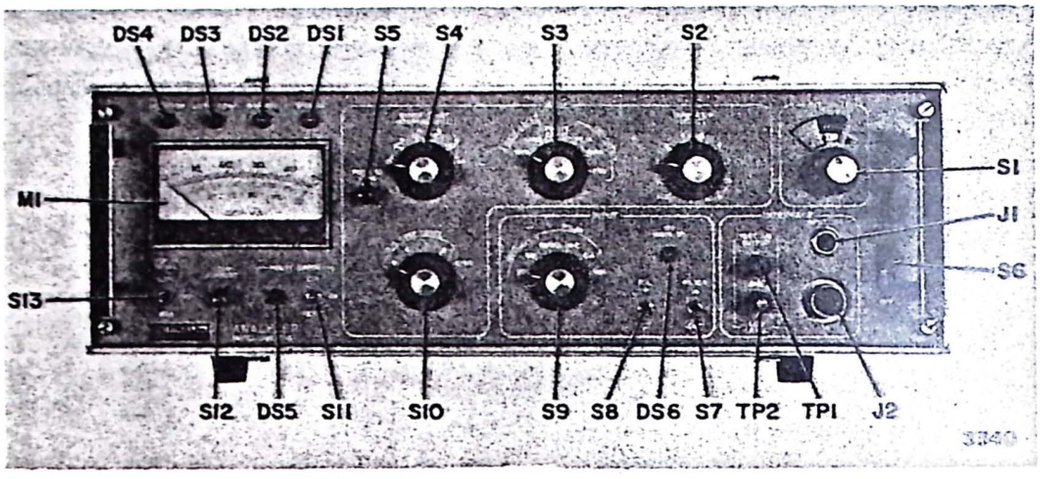
Preliminary Procedure

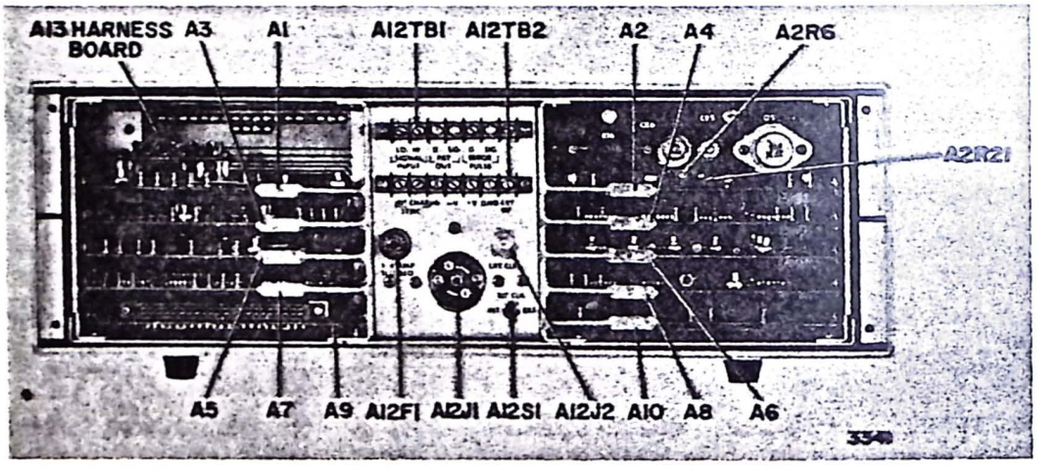
4.04 Perform the following initial procedure.

(a) Connect power cord to rear-panel receptacle.

(b) Set POWER switch on.

(c) Set INPUT switch to EIA.





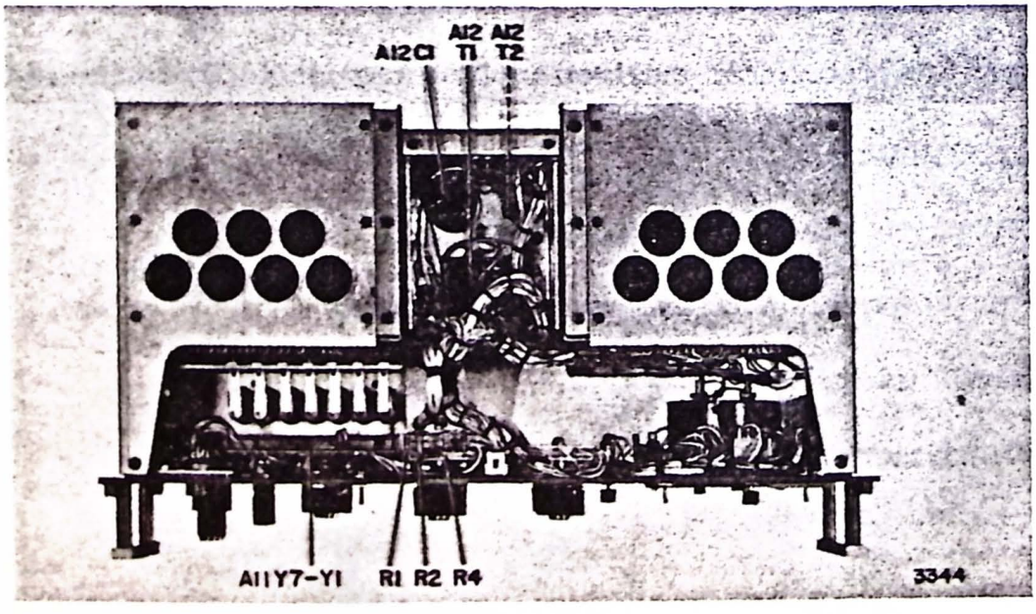


Fig. 34 - Parts Locations - Chassis

(d) Set POL switch to (+).

(e) Set FILTER switch to OUT.

(f) Set S/S CODE LEVEL switch to 8.

(g) Set PARITY ERROR switch to ON.

(h) Set DISPLAY RESET switch to OFF.

(i) Set ERROR COUNT INTERVAL switch to ∞.

(j) Set MODE switch to BIAS.

(k) Set TRANSITION SELECT switch to ALL.

(l) Set BIT RATE switch to range A and select rate 37.5.

(m) Connect low-level signal from Pattern Generator PG-303A to INPUT SIG jack on Analyzer.

(n) Adjust Pattern Generator for 37.5-baud, low-level (EIA), zero per cent bias Marking distortion, 8-level code start-stop (selected characters programed for reversal pattern, making first information bit a Mark).

(o) On Analyzer, meter should indicate zero. SIG MARK ON indicator lamp should light.

Distortion Circuits Check-Out Procedure

4.05 Continue with following procedure to check performance of distortion measuring circuits.

(a) Adjust distortion of Pattern Generator in 1 per cent steps from zero to 8 per cent. Analyzer meter indication should follow. MARKING indicator lamp should light.

(b) Adjust distortion of Pattern Generator to 40 per cent Spacing bias. Analyzer meter should indicate 40 per cent ±2 per cent. SPACING indicator lamp should light.

(c) On Analyzer, set MODE switch to END.

(d) Adjust Pattern Generator to 40 per cent Spacing end. Analyzer meter should indicate 40 per cent. SPACING indicator lamp should light.

(e) Adjust distortion of Pattern Generator to 40 per cent Marking end. Analyzer meter should indicate 40 per cent. MARKING indicator lamp should light.

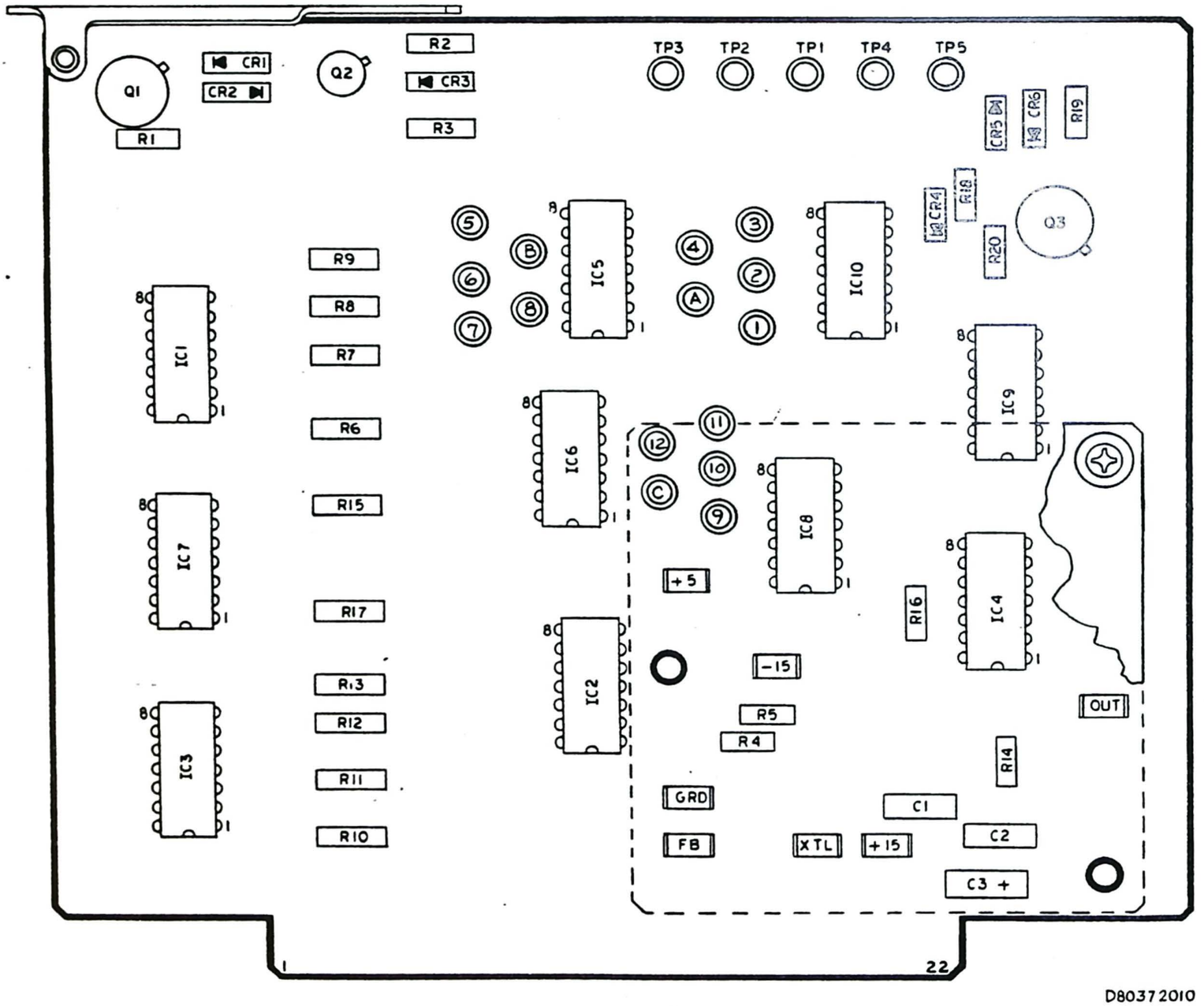


Fig. 35 - Parts Locations - PC-Card A1

(f) On Analyzer, set BIT RATE switch to each bit rate, setting Pattern Generator bit rate to correspond. At each setting, Analyzer meter should indicate 40 per cent.

(g) On Analyzer, Set BIT RATE switch to 75 and set Pattern Generator bit rate to 75.

(h) On Analyzer, set S/S CODE LEVEL switch to 5, 6, and 7, setting Pattern Generator to correspond. At each setting, Analyzer meter should indicate 40 per cent.

(i) Set S/S CODE LEVEL switch to 8.

(j) Set TRANSITION SELECT switch to each setting of 1 through 9. (Depress DISPLAY RESET switch to MAN at each setting.) At each even number setting, meter should indicate 40 per cent.

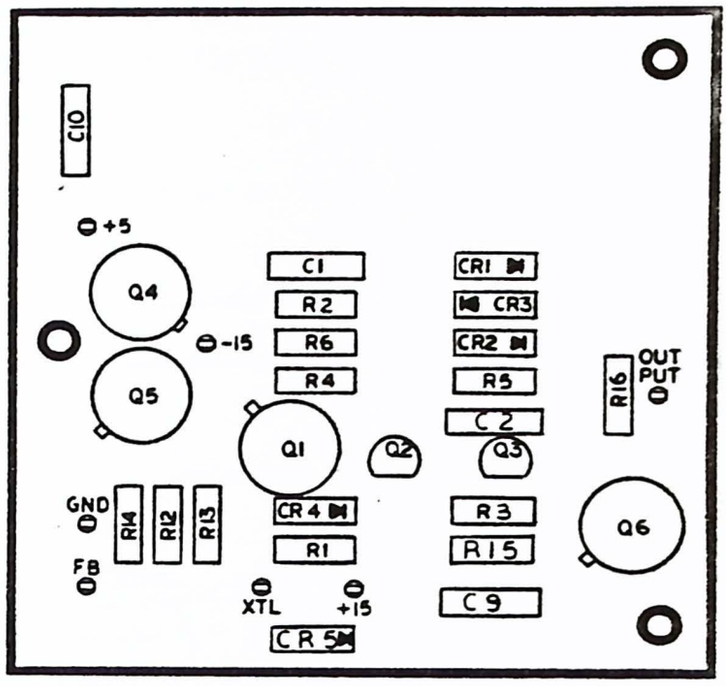


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Fig. 36 - Parts Locations - PC Card A1A1

(k) Set MODE switch to BIAS.

(l) Adjust Pattern Generator for bias distortion.

(m) Set TRANSITION SELECT switch to each setting of 1 through 9. (Depress DISPLAY RESET switch to MAN at each setting.) At each odd number setting, meter should indicate 40 per cent.

(n) Set TRANSITION SELECT switch to ALL.

(o) Set MODE switch to PEAK. Meter should indicate 40 per cent.

(p) Adjust Pattern Generator for 20 per cent distortion. Analyzer meter should hold at 40 per cent.

(q) Momentarily depress DISPLAY RESET switch to MAN. Meter should reset to zero and then deflect to 20 per cent and hold.

(r) Set DISPLAY RESET switch to AUTO. Meter should reset every five seconds. (Pointer will not have time to fall to zero.)

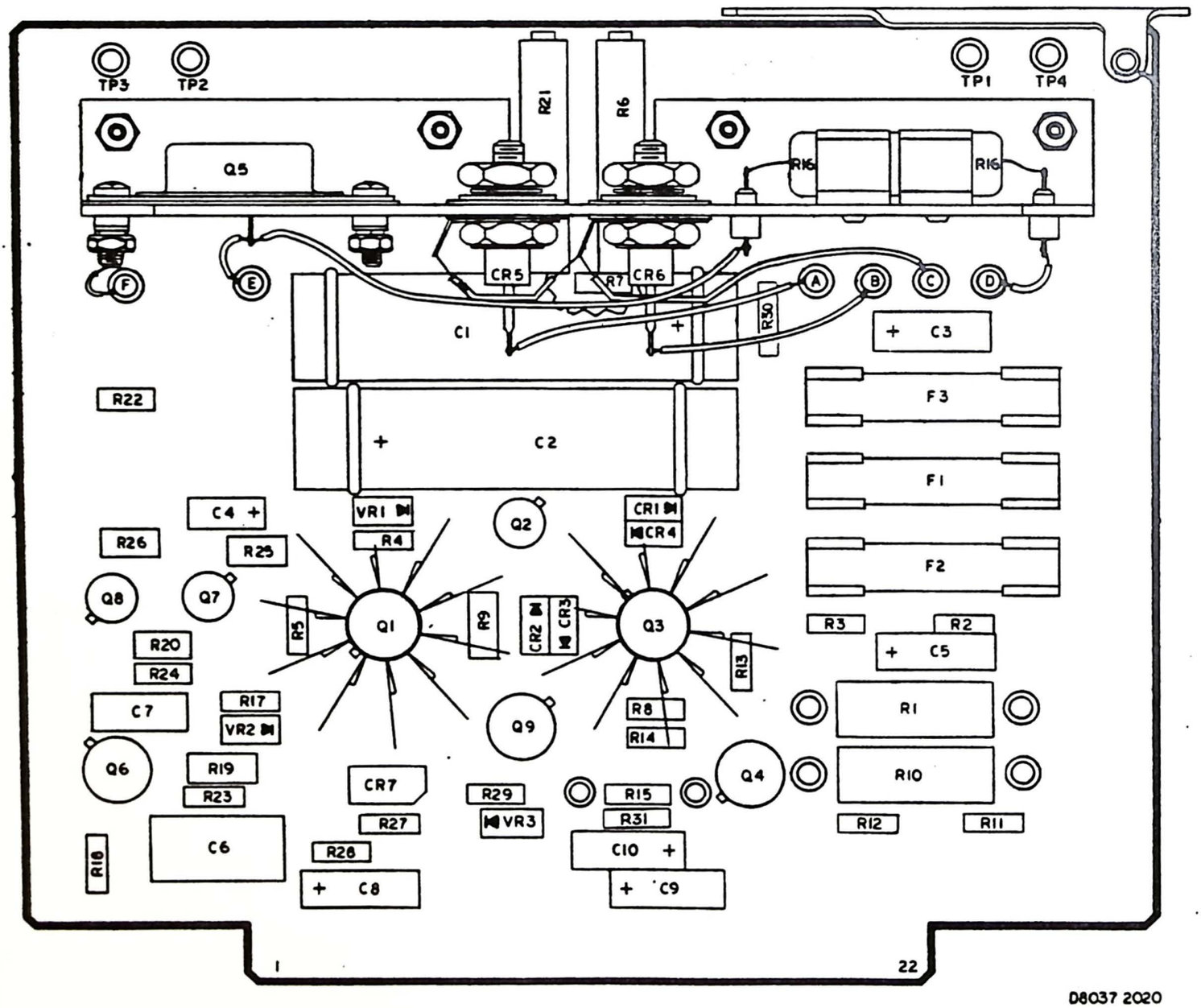


Fig. 37 - Parts Location - PC-Card A2

(s) Set S/S CODE LEVEL switch to SYNC. Set Pattern Generator to provide a synchronous reversal signal with 40 per cent bias Marking distortion. Analyzer meter should reset every five seconds.

(t) Set MODE switch to BIAS. Meter should indicate 40 per cent. MARKING indicator lamp should light.

(u) Set POL switch to (-). SPACING indicator lamp should light. Set POL lamp to (+).

Parity Error Circuits Check-Out Procedure

4.06 Continue with following procedure to check out performance of parity error detection and counting circuits.

(a) Set MODE switch to PARITY COUNT.

(b) Set PARITY ERROR switch to ON.

(c) Set S/S CODE LEVEL switch to 8.

(d) Set ERROR COUNT INTERVAL switch to ∞.

(e) Set Pattern Generator for 8-level selected character, manual character step. Set first selected character to have an odd number of Marks if the Analyzer is strapped for even parity (see 1.17), or set first selected character to have an even number of Marks if Analyzer is strapped for odd parity.

(f) On Analyzer, depress DISPLAY RESET switch to MAN and PARITY ERROR switch to RESET. PARITY ERROR indicator lamp should now be out and meter should indicate zero.

(g) On Pattern Generator, depress manual sequence switch one time.

(h) On Analyzer, PARITY ERROR indicator lamp should light.

(i) Depress PARITY ERROR switch to RESET; indicator lamp goes out.

Note: The remainder of this procedure does not apply unless optional PC-cards A3 and A4 are installed.

(j) Repeat steps (g) through (i) until meter indicates 50 and OVERFLOW indicator lamp lights.

(k) Depress DISPLAY RESET switch to MAN; meter resets to zero. Set switch to AUTO.

(l) Set ERROR COUNT INTERVAL switch to 10^2.

(m) Repeat steps (g) through (i) about a dozen times until COUNT COMP indicator lamp lights. Five seconds later lamp goes out and meter resets to zero.

Bit Error Circuits Check-Out Procedure

4.07 Continue with the following procedure to check out performance of the bit error detection and counting circuits.

(a) Set MODE switch to REV.

(b) Set ERROR COUNT INTERVAL switch to ∞.

(c) Adjust Pattern Generator for undistorted reversal pattern output.

(d) Set S/S CODE LEVEL switch to SYNC.

(e) Momentarily depress PUSH TO SYNC pushbutton.

(f) Momentarily depress DISPLAY RESET switch to MAN. OVERFLOW and COUNT COMP indicator lamps should be out and meter should indicate zero.

(g) Introduce bit errors into signal by momentarily disconnecting the input signal line. Each time bit errors are thus caused to occur, the meter pointer should advance up scale to register the number of bit errors. When 50 errors have occurred, the OVERFLOW indicator lamp should light.

(h) Depress DISPLAY RESET switch to MAN. OVERFLOW indicator lamp should go out and meter should reset to zero.

(i) Set ERROR COUNT INTERVAL switch to 10^3.

(j) Depress PUSH TO SYNC switch; set DISPLAY RESET switch to MAN, and then set it to AUTO. Introduce some bit errors by disconnecting the input signal. About 14 seconds later COUNT COMP indicator lamp should light; five seconds after that it should go out and the meter should reset to zero.

(k) Repeat above procedure with MODE switch set to RAND and Pattern Generator adjusted for pseudo random pattern output signal.

(C) Troubleshooting

4.08 When the Analyzer is suspected of malfunction, use the test equipment listed in 4.02 to perform the following procedure.

(a) Check that unit is being used correctly, in accordance with 2(B).

(b) Remove rear cover and check that all PC-cards are secure in their correct receptacles.

(c) Check that the rear-panel 1/4 AMP SLO BLO fuse is good.

(d) Measure secondary voltages at test points on PC-card A2 (TP3 common):

+15 volts: TP1

-15 volts: TP4

+5 volts: TP2

Caution: Do not make voltage adjustments except in accordance with 1(F).

(e) Remove portable case and visually inspect unit. Check front-panel switches for damage, corrosion, and bent contacts. Check all wiring and mounted components for damage and burns.

(f) Check each PC-card by substitution. When a faulty card is found, perform steps (g) through (i) below.

Note: If substitute PC-cards are not available, perform steps (g) through (i) for each card.

(g) Use PC-card service extender to extend suspected card in its slot.

(h) Refer to appropriate schematic diagram (Fig. 45 through 54), and use oscilloscope to observe waveforms shown on apron of schematic diagram.

(i) When an incorrect waveform is found, the circuit area at fault has been localized. Refer to the logic analysis of that circuit (see 3(C)), and use the oscilloscope to isolate the trouble to a faulty integrated circuit chip.

(D) Adjustments

4.09 Because the Analyzer consists primarily of digital circuits, only the power supply adjustments, outlined in 1(F), are required to maintain accurate performance.

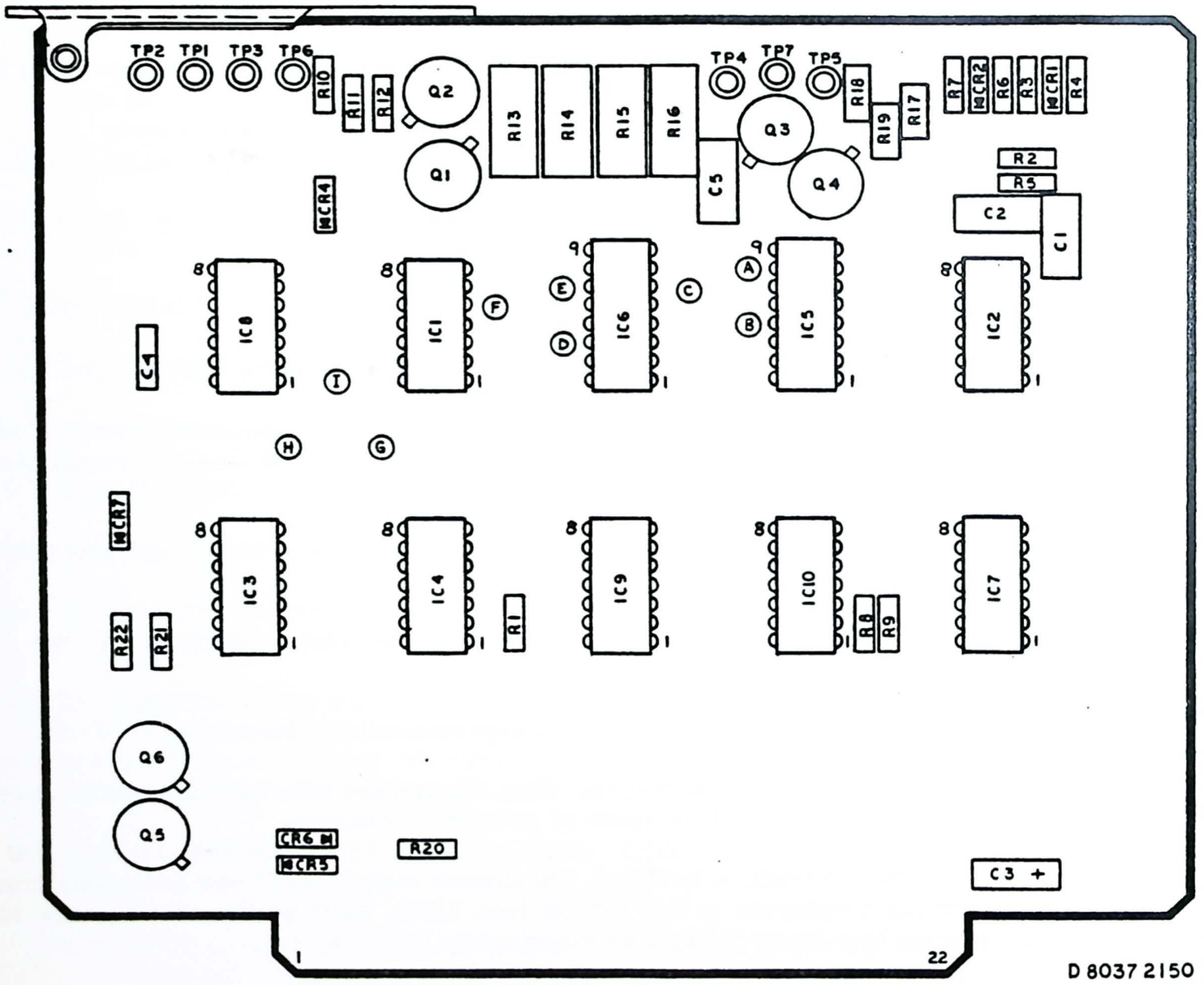


Fig. 38 - Parts Locations - PC-Card A3

(E) Repair

4.10 Special repair procedures are outlined in 4.11 through 4.13. Replacement of PC-card parts should be accomplished in accordance with good soldering techniques. Take the precautions necessary to prevent overheating solid-state components. In most cases, component replacement will not necessitate re-adjustment of Analyzer. If, however, components are replaced on either PC-card A2 (power supply) or A6 (D/A converter), perform the adjustment procedure outlined in 1(F).

Removal of Portable Case

4.11 Use the following procedure to remove portable case from chassis.

(a) Remove front cover.

(b) Remove any external wires or cables from front- and rear-panel connectors.

(c) Loosen the captive screw at each corner of rear cover and remove rear cover.

(d) Loosen the captive screw at each corner of front panel and slide case off over rear of chassis.

Removal of Bottom Access Plate

4.12 Use following procedure to remove access plate from bottom of chassis to expose wiring to power transformers T1 and T2, filter capacitor C1, and wiring to inside of rear panel.

(a) Perform procedure in 4.11.

(b) Remove the ten flat-head screws from bottom of chassis.

(c) Lift access plate clear.

Removal of Rear Panel Subassembly

4.13 If it becomes necessary to replace either power transformer T1 or T2 or filter capacitor C1 or to gain access to inside of terminal boards TB1 and TB2, perform the following procedure.

(a) Perform the procedures outlined in 4.11 and 4.12.

(b) Remove two flat-head screws from top of chassis directly over the rear panel.

(c) Rest chassis on its top.

(d) Lift subassembly out of its cavity far enough to facilitate repairs.

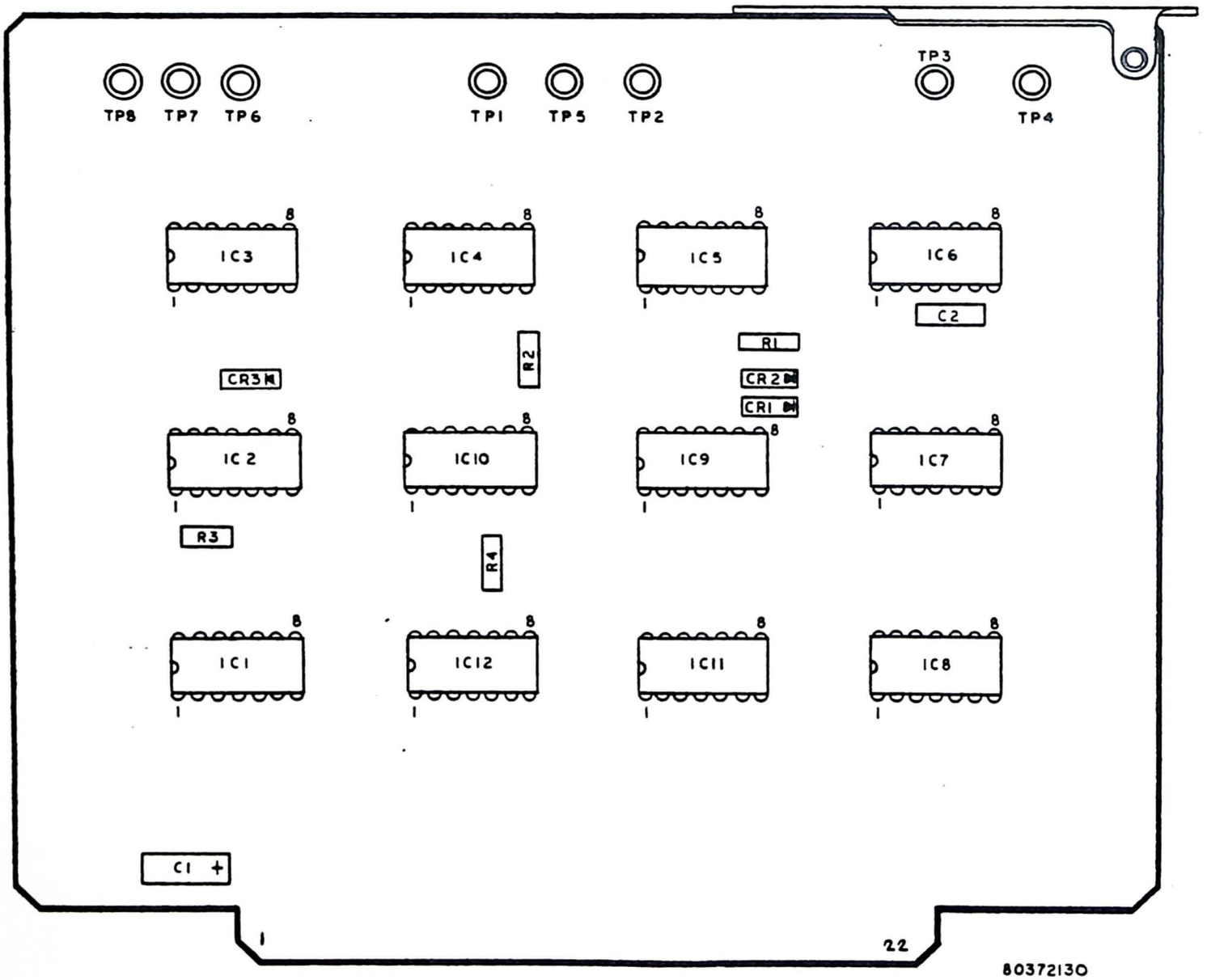


Fig. 39. - Parts Locations - PC-Card A4

(F) Field Installation of Optional PC-cards A3 and A4

4.13 Install PC-cards A3 and A4 as follows:

(a) Strap PC-card A3 in accordance with 1.19 and 1.20.

(b) Strap PC-card A8 in accordance with 1.18. (Refer to 4.11 for instructions pertaining to removal of portable case from chassis, to expose harness board.)

(c) Insert PC-cards A3 and A4 in their correct slots (Fig. 34).

(G) Field Installation of Optional Crystals

4.14 Install optional crystals Y1 through Y6 as follows:

Note: Study entire procedure before selecting crystal frequencies.

(a) Select crystals Y1 through Y6, each with a frequency factor of either 200, 3200, or 6400 times required bit rates.

(b) Remove portable case from chassis (see 4.11).

(c) Insert crystals in sockets XY1 through XY6 (Fig. 34). (Sockets XY1 through XY6 correspond to positions 1 through 6, respectively, on the B-range of the BIT RATE switch.)

(d) Strap PC-card A1 in accordance with Fig. 5. Referring to the table associated with A1 in Fig. 5, strap together the terminals listed opposite the correct division factor. (Division factor 1 applies to a crystal with a frequency factor of 200; division factor 16 applies to a crystal with a frequency factor of 3200; and division factor 32 applies to a crystal with a frequency factor of 6400.)

(e) Write in or decal positions 1 through 6, on the B-range scale of the BIT RATE switch, with the bit rates derived from crystals Y1 through Y6, respectively. (If a set of optional crystals has been supplied with a new BIT RATE switch dial, pull the old dial off the side of the shaft and snap the new one in place.)

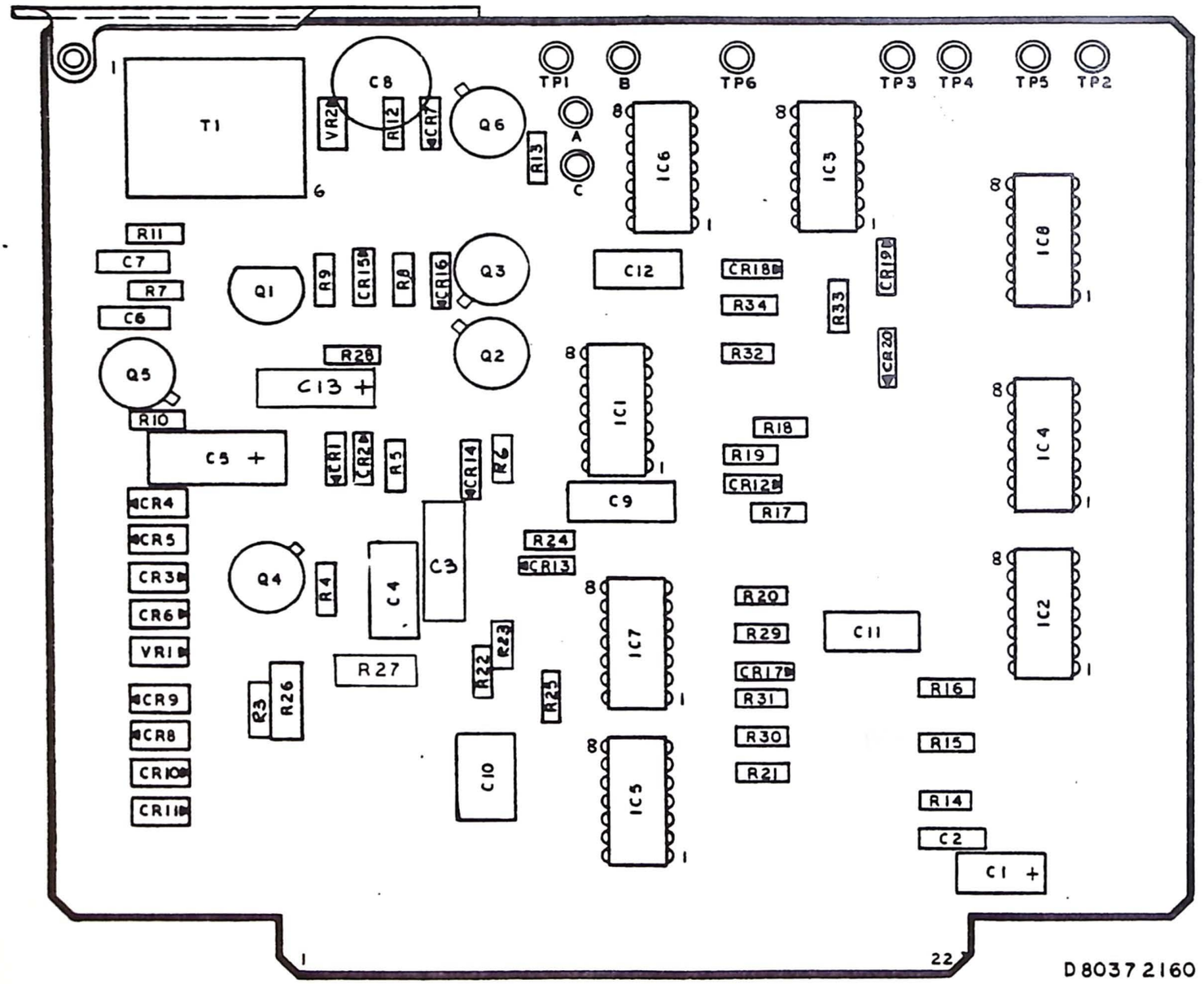


Fig. 40 - Parts Locations - PC-Card A5

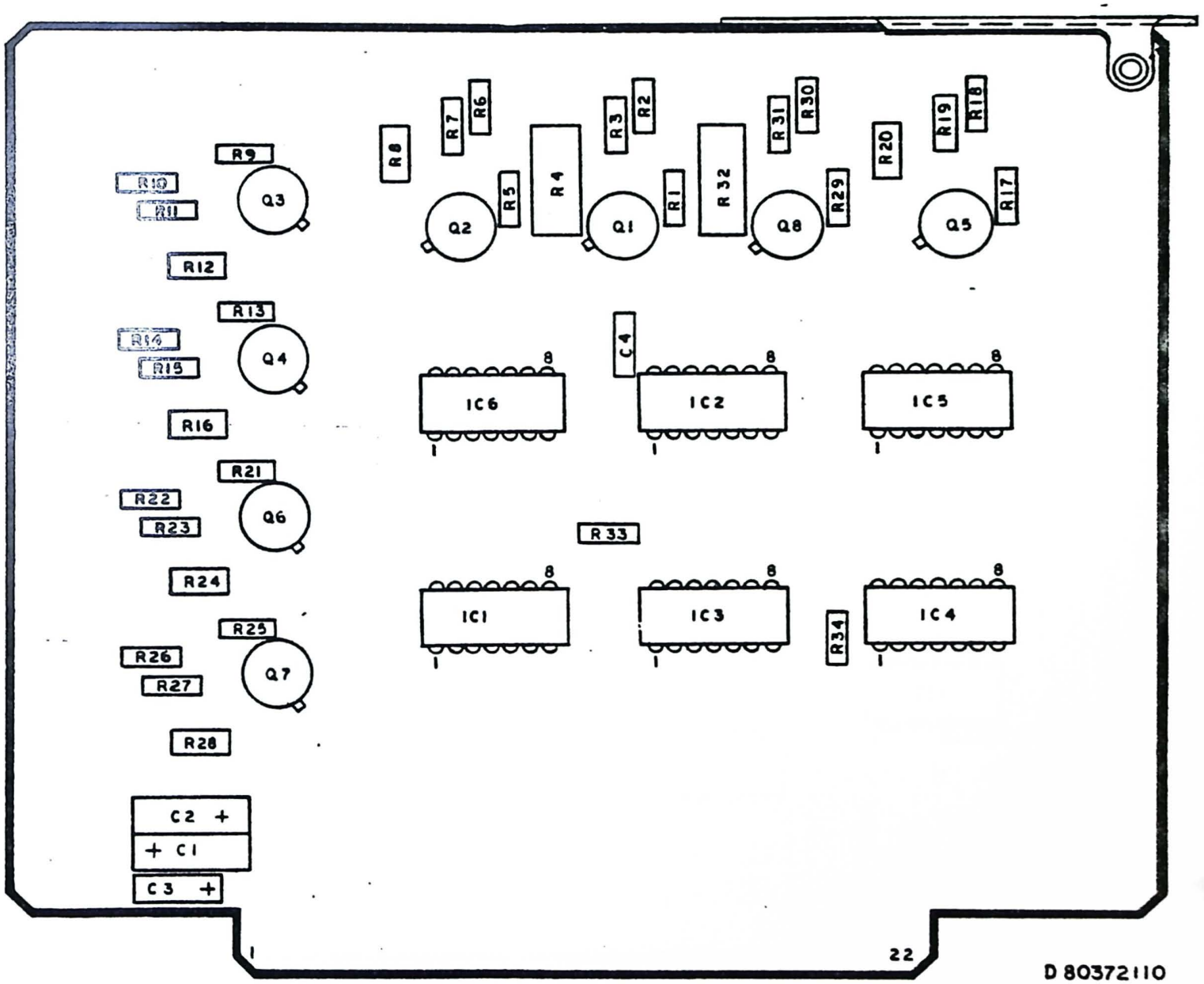


Fig. 41 - Parts Locations - PC-Card A6

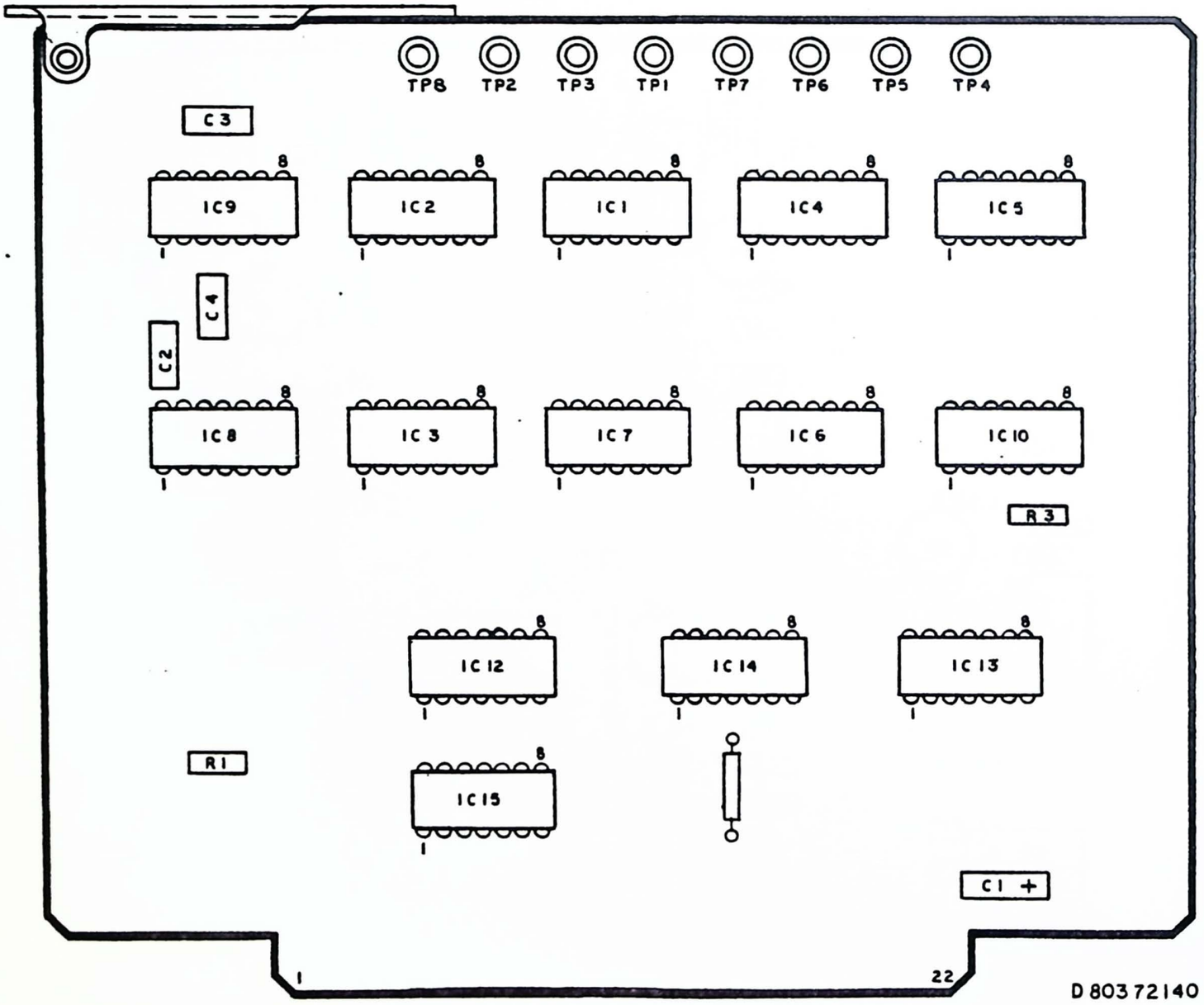


Fig. 42 - Parts Locations - PC-Card A7

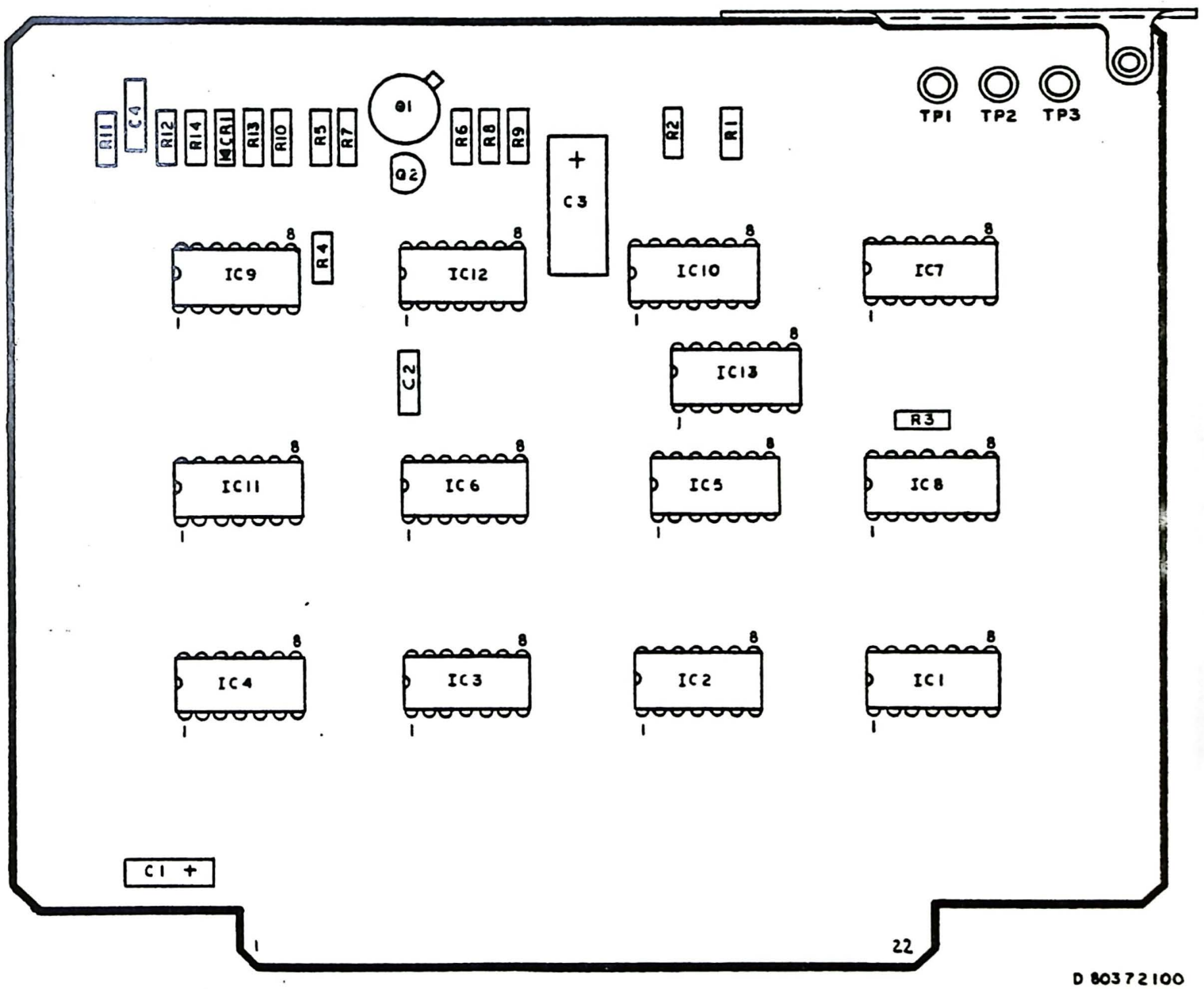


Fig. 43 - Parts Locations - PC-Card A8

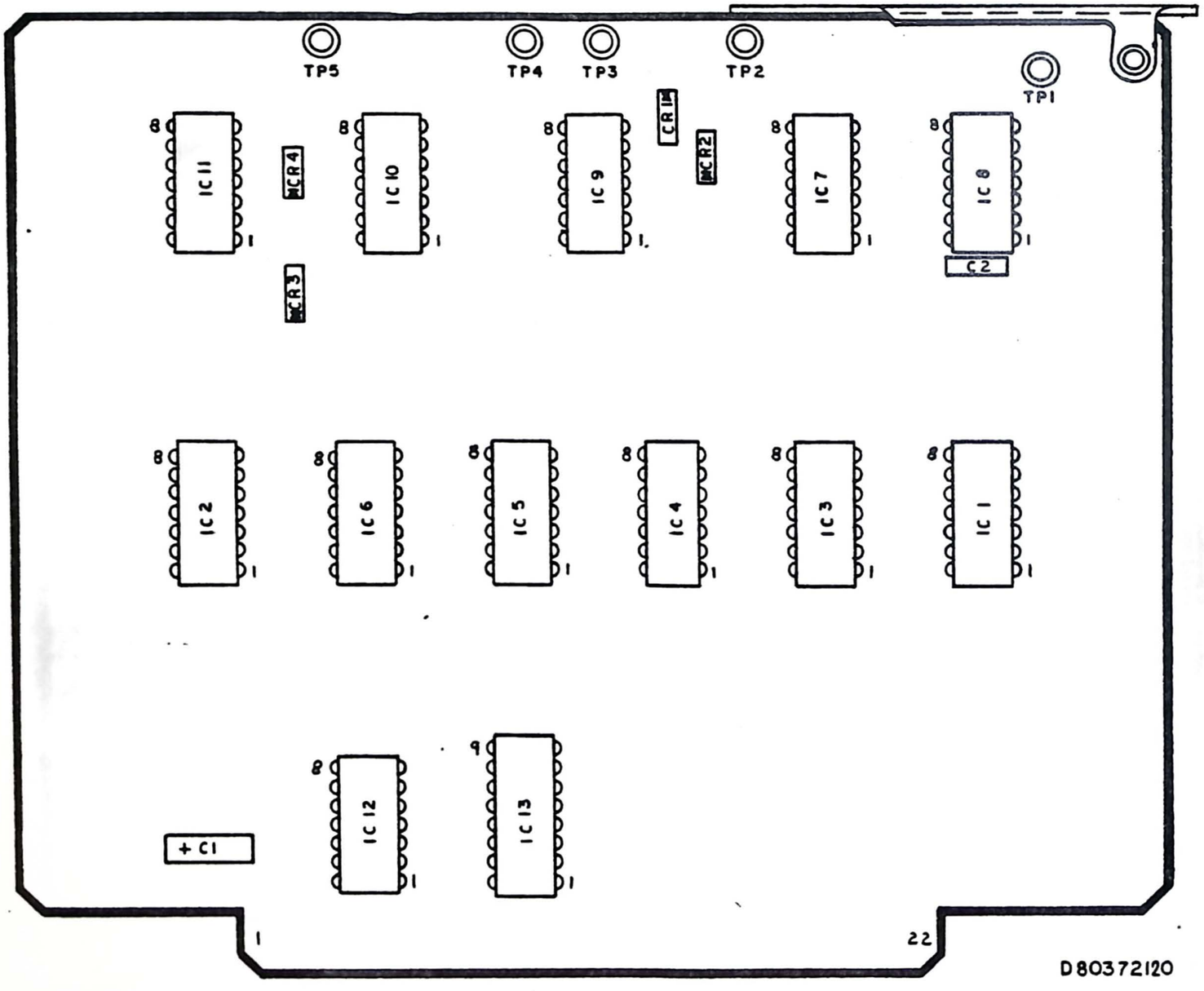
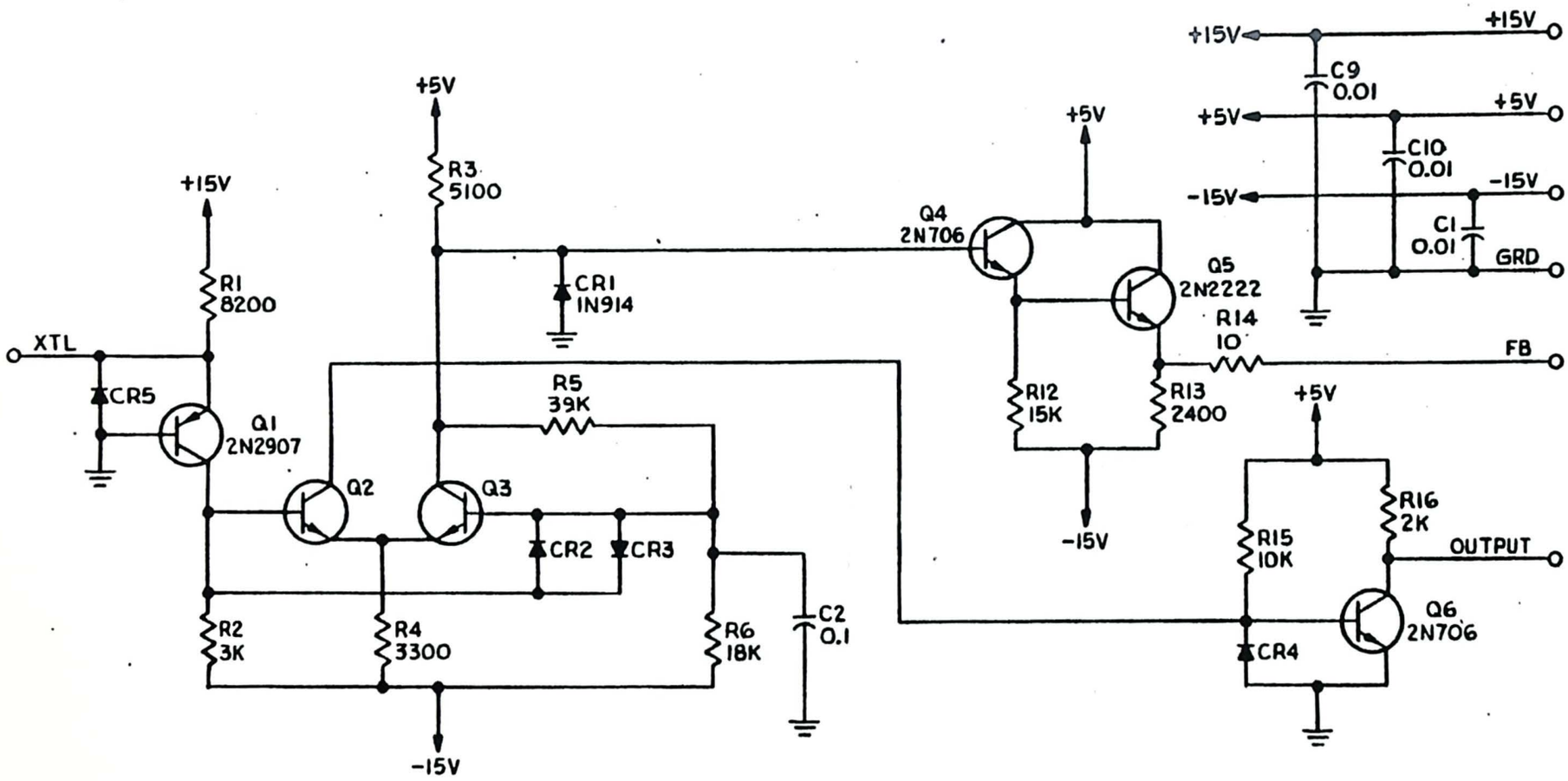


Fig. 44 - Parts Locations - PC-Card A10

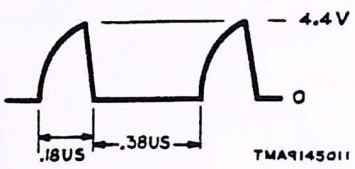
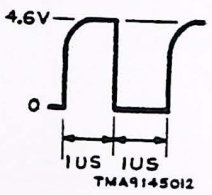
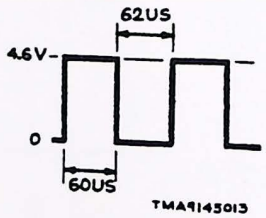
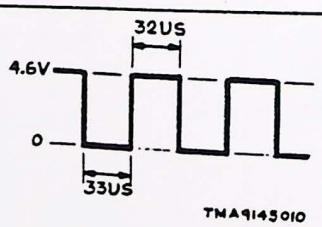


NOTES:

1. UNLESS OTHERWISE INDICATED,
   ALL RESISTANCES ARE IN OHMS,
   1/4W, ±5% (K=1000)
   ALL CAPACITANCES ARE IN UF.
   ALL TRANSISTORS ARE 2N5222.
   ALL DIODES ARE IN277.
2. PREFIX REF DESIG. A1A146

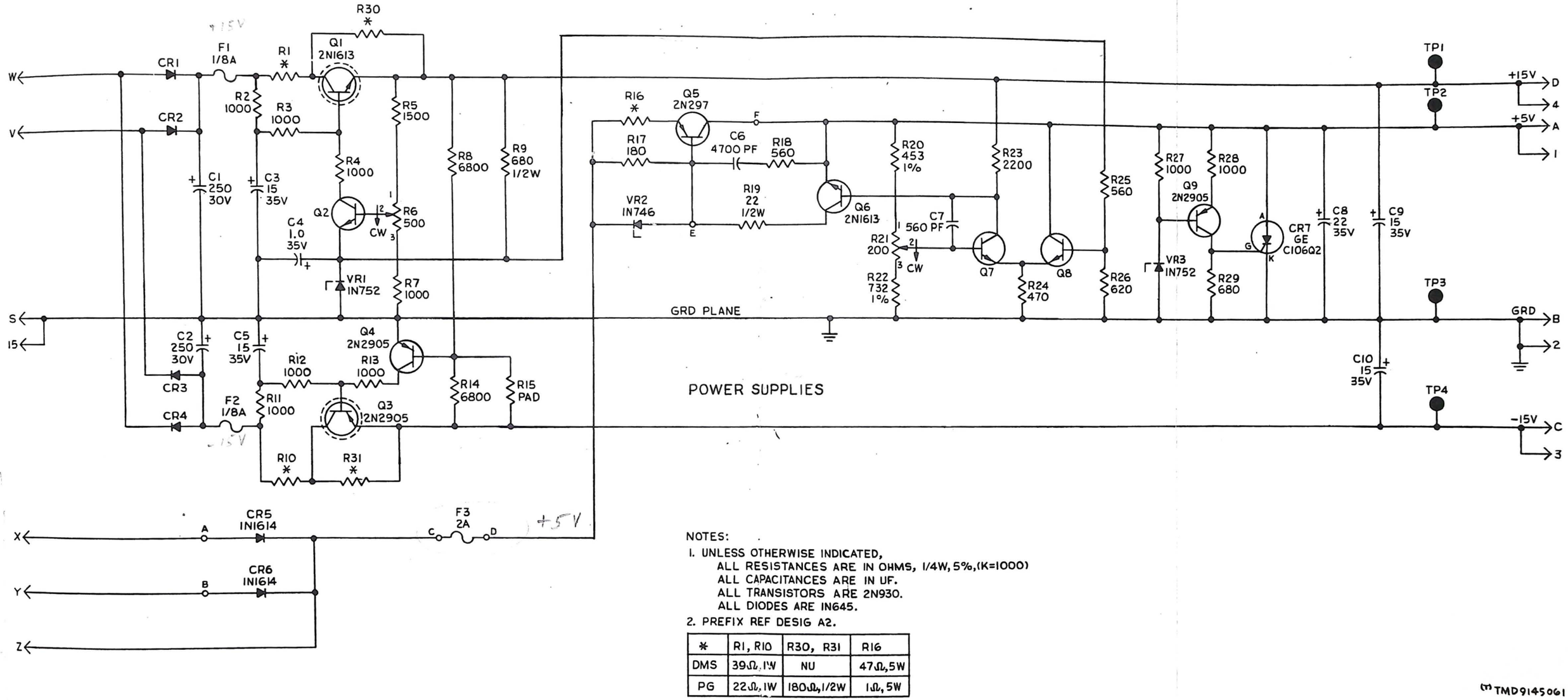
(1) TMC 9145 060

Fig. 45 - Schematic Diagram - PC-Card A1A1 (Time-Base Oscillator)

TEST POINT	WAVEFORM	CONDITIONS
TP1		INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: N/A
TP2		INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: 75
TP3		INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: 75
TP4		INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: 75

NOTES:
1. UNLESS OTHERWISE INDICATED,
   ALL RESISTANCES ARE IN OHMS, 1/4W, ±5%,(K=1000)
   ALL CAPACITANCES ARE IN UF.
   ALL TRANSISTORS ARE 2N2222.
   ALL DIODES ARE IN914.
2. PREFIX REF DESIG. A1.

Fig. 46 - Schematic Diagram - PC-Card A1 (Time-Base Circuits)



NOTES:

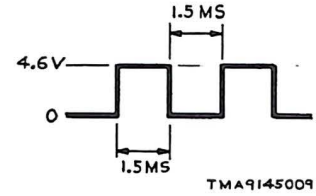
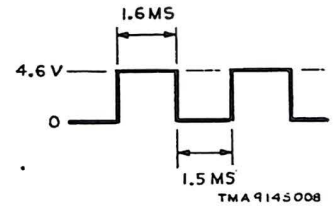
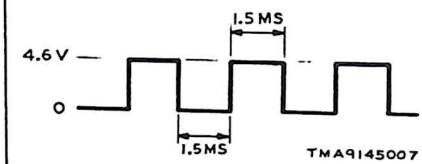
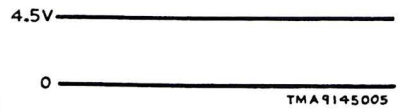
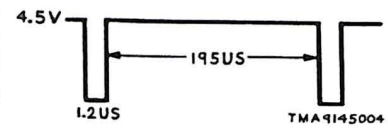
1. UNLESS OTHERWISE INDICATED,
   ALL RESISTANCES ARE IN OHMS, 1/4W, 5%, (K=1000)
   ALL CAPACITANCES ARE IN UF.
   ALL TRANSISTORS ARE 2N930.
   ALL DIODES ARE IN645.
2. PREFIX REF DESIG A2.

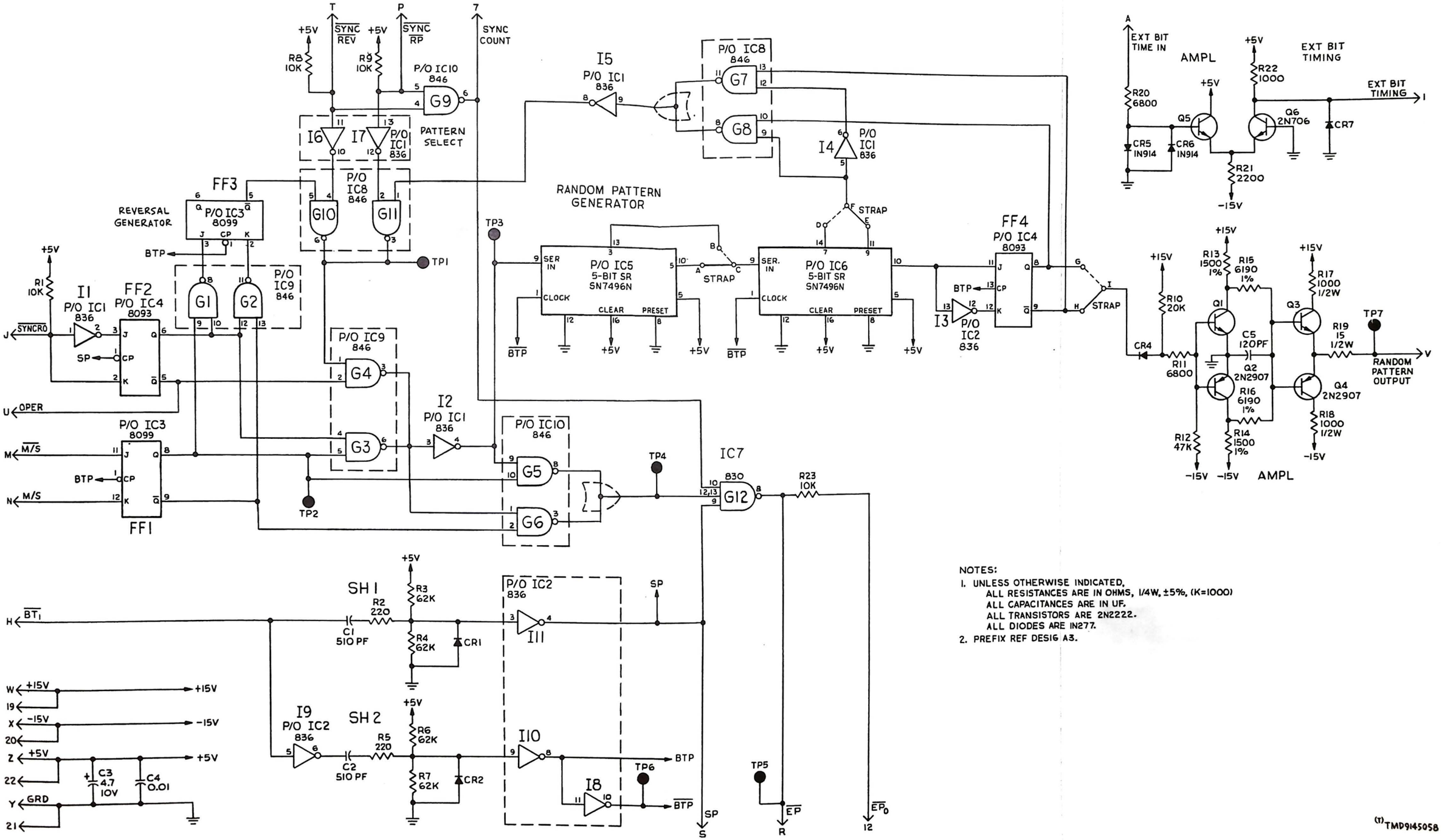
*	R1, R10	R30, R31	R16
DMS	39Ω, 1W	NU	47Ω, 5W
PG	22Ω, 1W	180Ω, 1/2W	1Ω, 5W

TMD9145061

Fig. 47 - Schematic Diagram - PC-Card A2 (Power Supply Circuits)

Pg. 50, 70

TEST POINT	WAVEFORM	CONDITIONS
TP1		INPUT SIGNAL: REV, SYNC, 600 BPS SWITCH SETTINGS: BIT RATE: 600 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP2		INPUT SIGNAL: REV, SYNC, 600 BPS SWITCH SETTINGS: BIT RATE: 600 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP3 & TP7		INPUT SIGNAL: REV, SYNC, 600 BPS SWITCH SETTINGS: BIT RATE: 600 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP4	 NOTE: Set BIT RATE switch to 1200 to obtain waveform.	INPUT SIGNAL: REV, SYNC, 600 BPS SWITCH SETTINGS: BIT RATE: 600 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP5	 NOTE: Set BIT RATE switch to any rate except 600 to obtain spikes.	INPUT SIGNAL: REV, SYNC, 600 BPS SWITCH SETTINGS: BIT RATE: 600 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP6		INPUT SIGNAL: REV, SYNC, 4800 BPS SWITCH SETTINGS: BIT RATE: 4800 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF

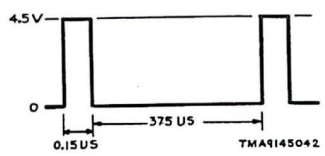
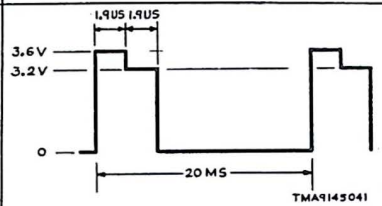
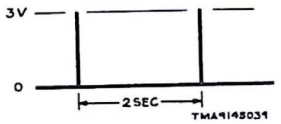
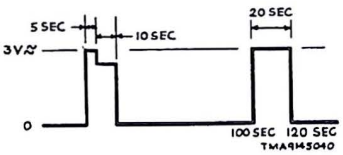
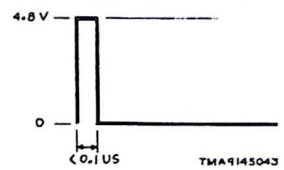
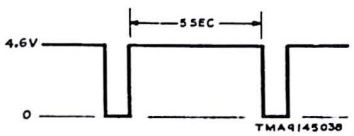
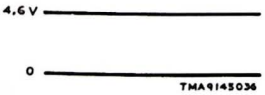


NOTES:

1. UNLESS OTHERWISE INDICATED,
   ALL RESISTANCES ARE IN OHMS, 1/4W, ±5%, (K=1000)
   ALL CAPACITANCES ARE IN UF.
   ALL TRANSISTORS ARE 2N2222.
   ALL DIODES ARE IN277.
2. PREFIX REF DESIG A3.

(1) TMD9145058

Fig. 48 - Schematic Diagram - PC-Card A3 (Bit Error Circuits)

TEST POINT	WAVEFORM	CONDITIONS
TP1		INPUT SIGNAL: REV, SYNC, 2400 BPS SWITCH SETTINGS: BIT RATE: 2400 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP2		INPUT SIGNAL: REV, SYNC, 4800 BPS SWITCH SETTINGS: BIT RATE: 4800 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP3	 NOTE: Goes high about every 1 second.	INPUT SIGNAL: REV, SYNC, 4800 BPS SWITCH SETTINGS: BIT RATE: 4800 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP4	 NOTE: Goes high about every 70 seconds.	INPUT SIGNAL: REV, SYNC, 9600 BPS SWITCH SETTINGS: BIT RATE: 9600 MODE: REV S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP5	 NOTE: Observe positive spike as DISPLAY RESET switch is set to MAN.	INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: 2400 MODE: PEAK S/S CODE LEVEL: SYNC ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP6	 NOTE: Trace goes low every 5 seconds.	INPUT SIGNAL: REV, SYNC, 9600 BPS SWITCH SETTINGS: BIT RATE: 9600 MODE: REV S/S CODE LEVEL: SYNC TRANSITION SELECT: ALL ERROR COUNT INTERVAL: 10^3 PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN AUTO
TP7	 NOTE: Observe positive spike after setting BIT RATE switch to 50.	INPUT SIGNAL: REV, SYNC, 37.5 BPS SWITCH SETTINGS: BIT RATE: 37.5 MODE: REV S/S CODE LEVEL: SYNC TRANSITION SELECT: ALL ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF
TP8	 NOTE: Goes low shortly after setting BIT RATE switch to 9600.	INPUT SIGNAL: REV, SYNC, 4800 BPS SWITCH SETTINGS: BIT RATE: 4800 MODE: REV S/S CODE LEVEL: SYNC TRANSITION SELECT: ALL ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF

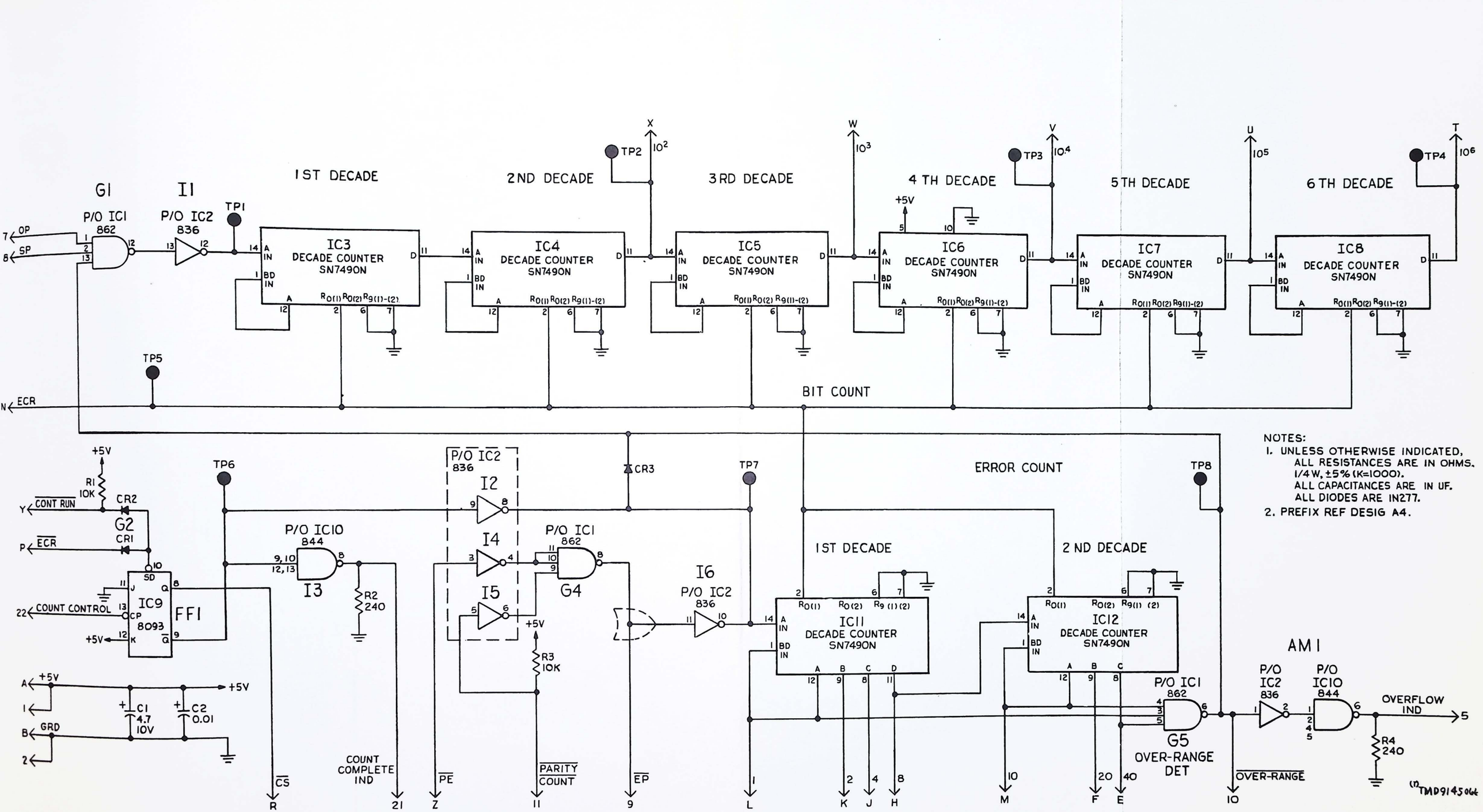
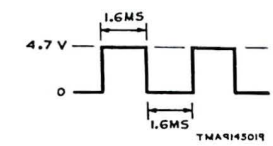
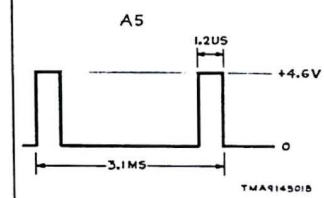
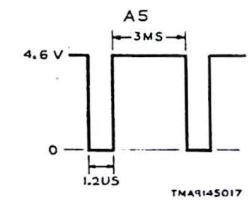
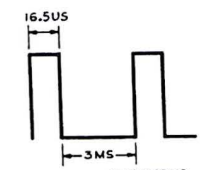
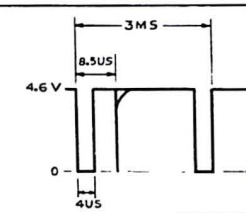
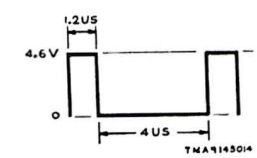
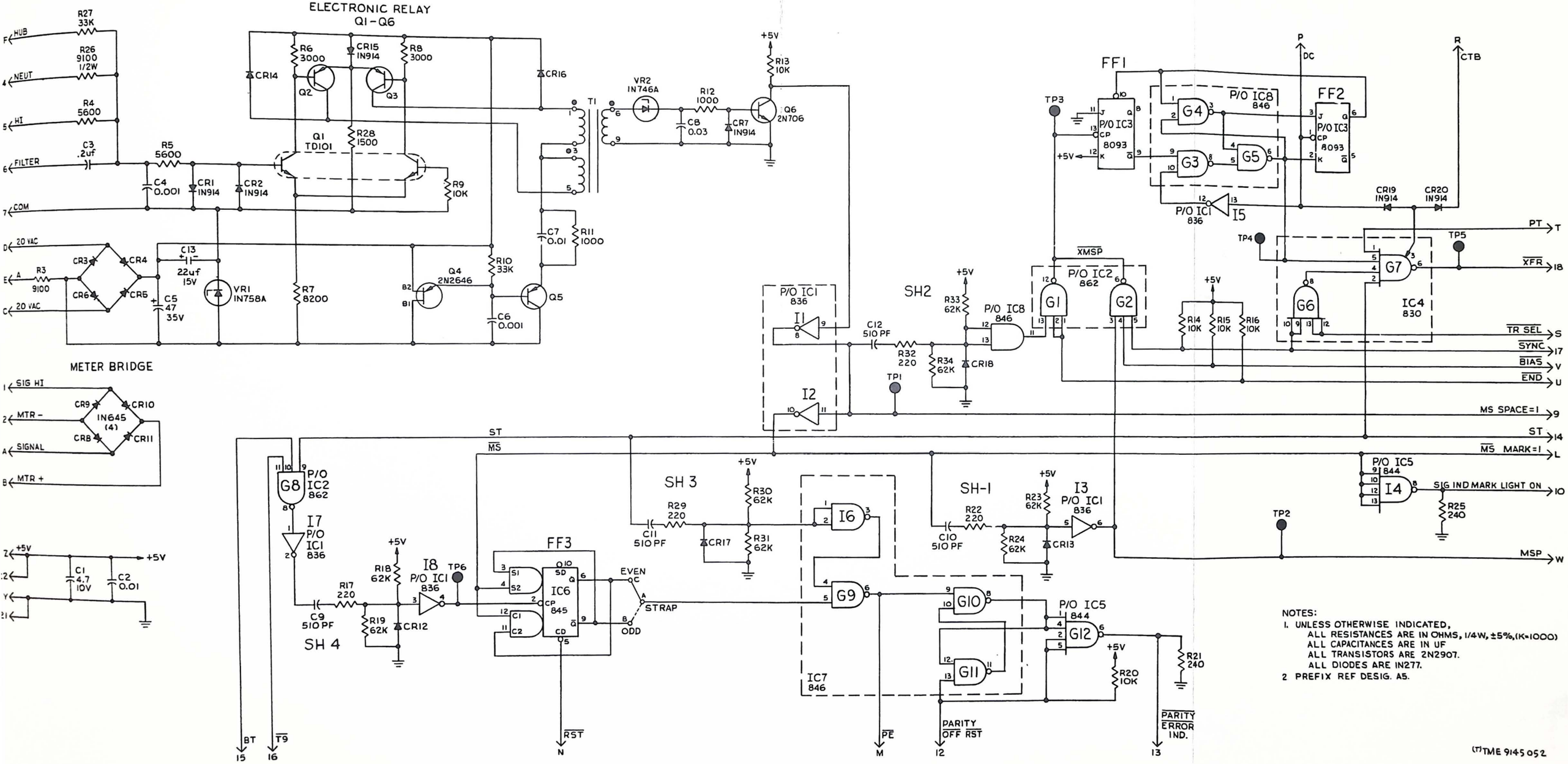


Fig. 49 - Schematic Diagram - PC-Card A4 (Error Counter Circuits)

TEST POINT	WAVEFORM	CONDITIONS
TP1		INPUT SIGNAL: REV, SYNC, 600 BPS
TP2		INPUT SIGNAL: REV, SYNC, 600 BPS
TP3		INPUT SIGNAL: REV, SYNC, 600 BPS SWITCH SETTINGS: BIT RATE: 600 MODE: BIAS S/S CODE LEVEL: SYNC TRANSITION SELECT: ALL DISPLAY RESET: MAN, THEN OFF
TP4		INPUT SIGNAL: REV, FREE RUN, 600 BPS SWITCH SETTINGS: BIT RATE: 600 MODE: PEAK S/S CODE LEVEL: SYNC TRANSITION SELECT: ALL DISPLAY RESET: MAN, THEN OFF
TP5	 NOTE: Waveform is obtained by applying 10% bias distortion to input signal.	INPUT SIGNAL: REV, SYNC, 600 BPS SWITCH SETTINGS: BIT RATE: 600 MODE: BIAS S/S CODE LEVEL: SYNC TRANSITION SELECT: ALL DISPLAY RESET: MAN, THEN OFF
TP6		INPUT SIGNAL: REV, 8-LEVEL, 600 BPS SWITCH SETTINGS: BIT RATE: 600 MODE: PARITY COUNT S/S CODE LEVEL: 8 ERROR COUNT INTERVAL: ∞ PUSH TO SYNC: DEPRESS DISPLAY RESET: MAN, THEN OFF



NOTES:
1. UNLESS OTHERWISE INDICATED,
   ALL RESISTANCES ARE IN OHMS, 1/4W, ±5%, (K=1000)
   ALL CAPACITANCES ARE IN UF
   ALL TRANSISTORS ARE 2N2907.
   ALL DIODES ARE IN277.
2. PREFIX REF DESIG. A5.

(T)TME 9145052

Fig. 50 - Schematic Diagram - PC-Card A5 (Input, Transfer, and Parity Error Circuits)

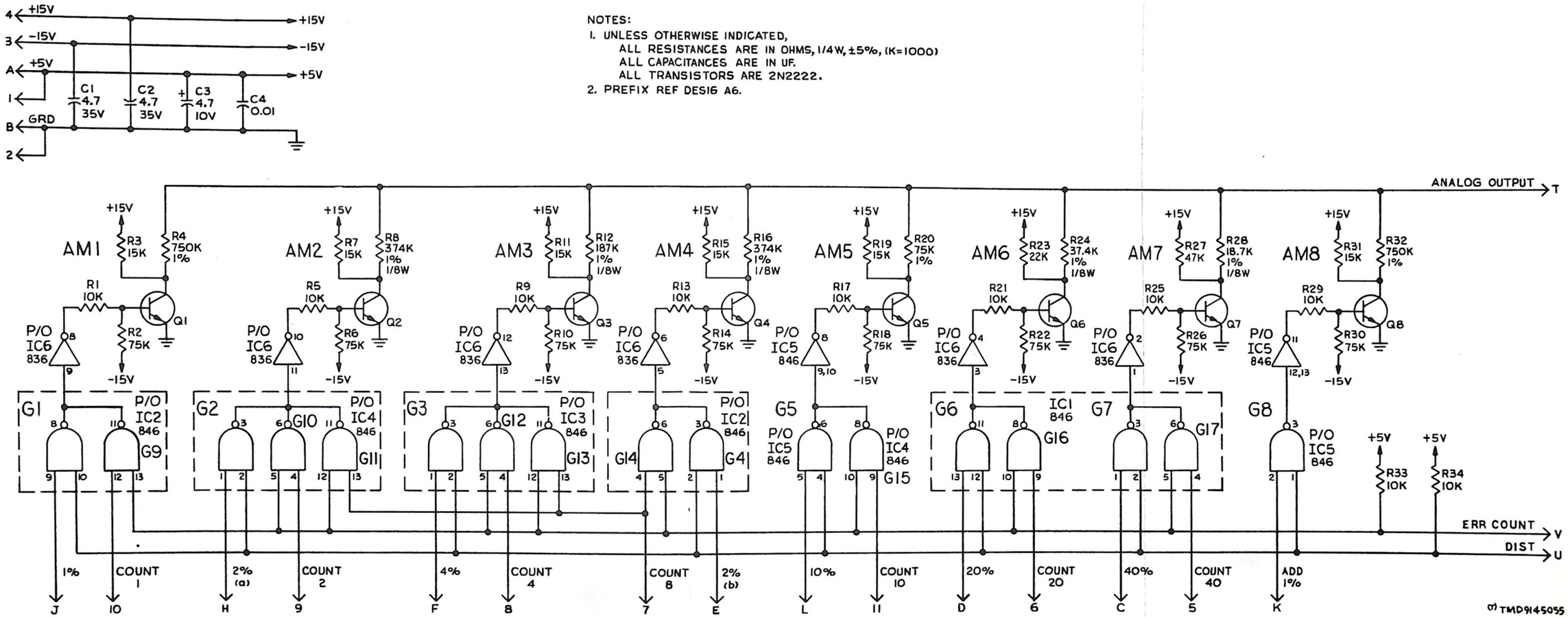
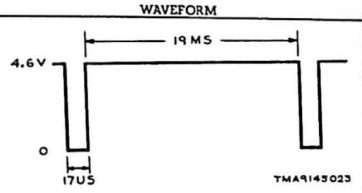
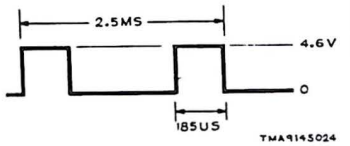
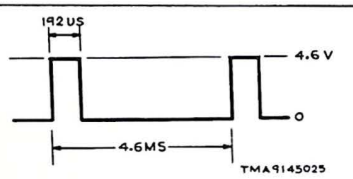
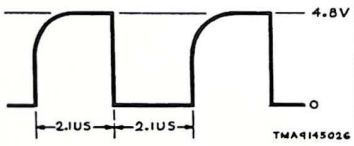
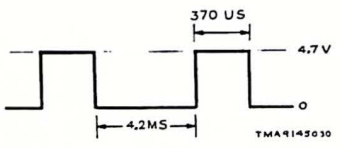
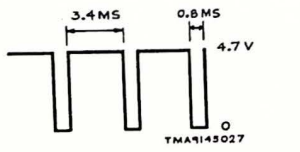
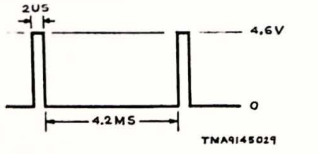
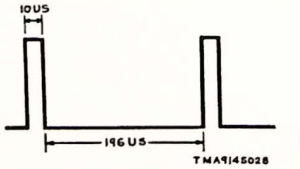
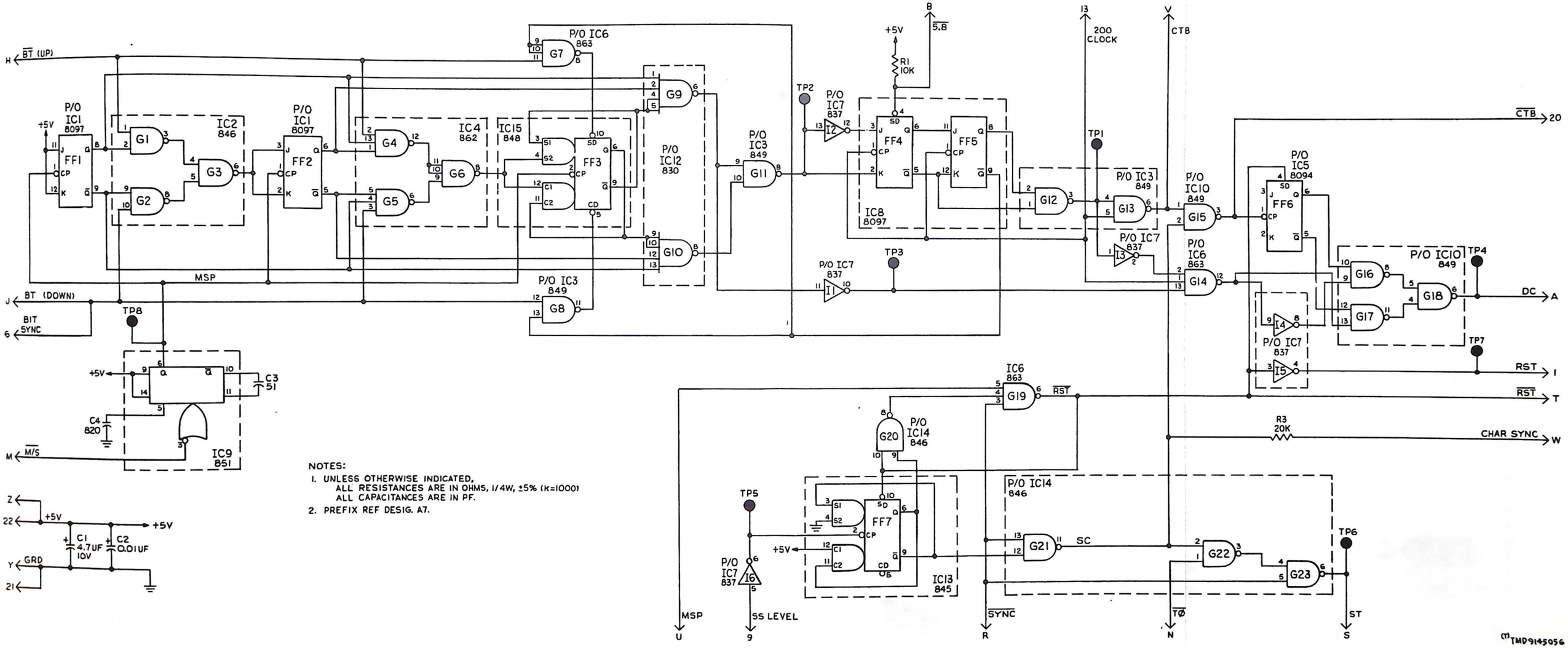


Fig. 51 - Schematic Diagram - PC-Card A6 (D/A Converter Circuits)

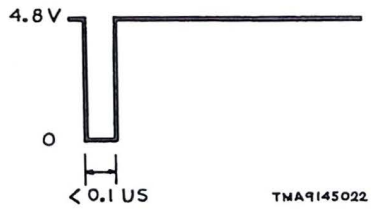
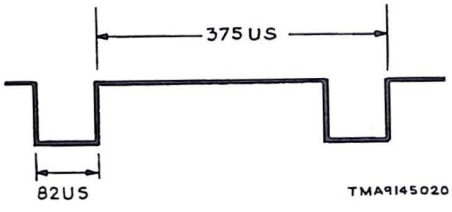
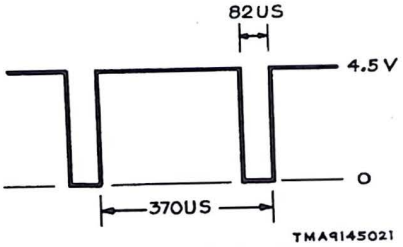
TEST POINT	WAVEFORM	CONDITIONS
TP1		INPUT SIGNAL: REV, SYNC, 300 BPS SWITCH SETTINGS: BIT RATE: 300 S/S CODE LEVEL: SYNC
TP2		INPUT SIGNAL: REV, SYNC, 2400 BPS SWITCH SETTINGS: BIT RATE: 2400 S/S CODE LEVEL: SYNC
TP3		INPUT SIGNAL: REV, SYNC, 2400 BPS SWITCH SETTINGS: BIT RATE: 2400 S/S CODE LEVEL: SYNC
TP4		INPUT SIGNAL: REV, SYNC, 2400 BPS SWITCH SETTINGS: BIT RATE: 2400 S/S CODE LEVEL: SYNC
TP5		INPUT SIGNAL: 8-LEVEL, REV, 2400 P SWITCH SETTINGS: BIT RATE: 2400 S/S CODE LEVEL: 8
TP6		INPUT SIGNAL: 8-LEVEL, REV, 2400 BPS SWITCH SETTINGS: BIT RATE: 2400 S/S CODE LEVEL: 8
TP7		INPUT SIGNAL: 8-LEVEL, REV, 2400 BPS SWITCH SETTINGS: BIT RATE: 2400 S/S CODE LEVEL: 8
TP8		INPUT SIGNAL: REV, SYNC, 9600 BPS SWITCH SETTINGS: BIT RATE: 9600 S/S CODE LEVEL: SYNC

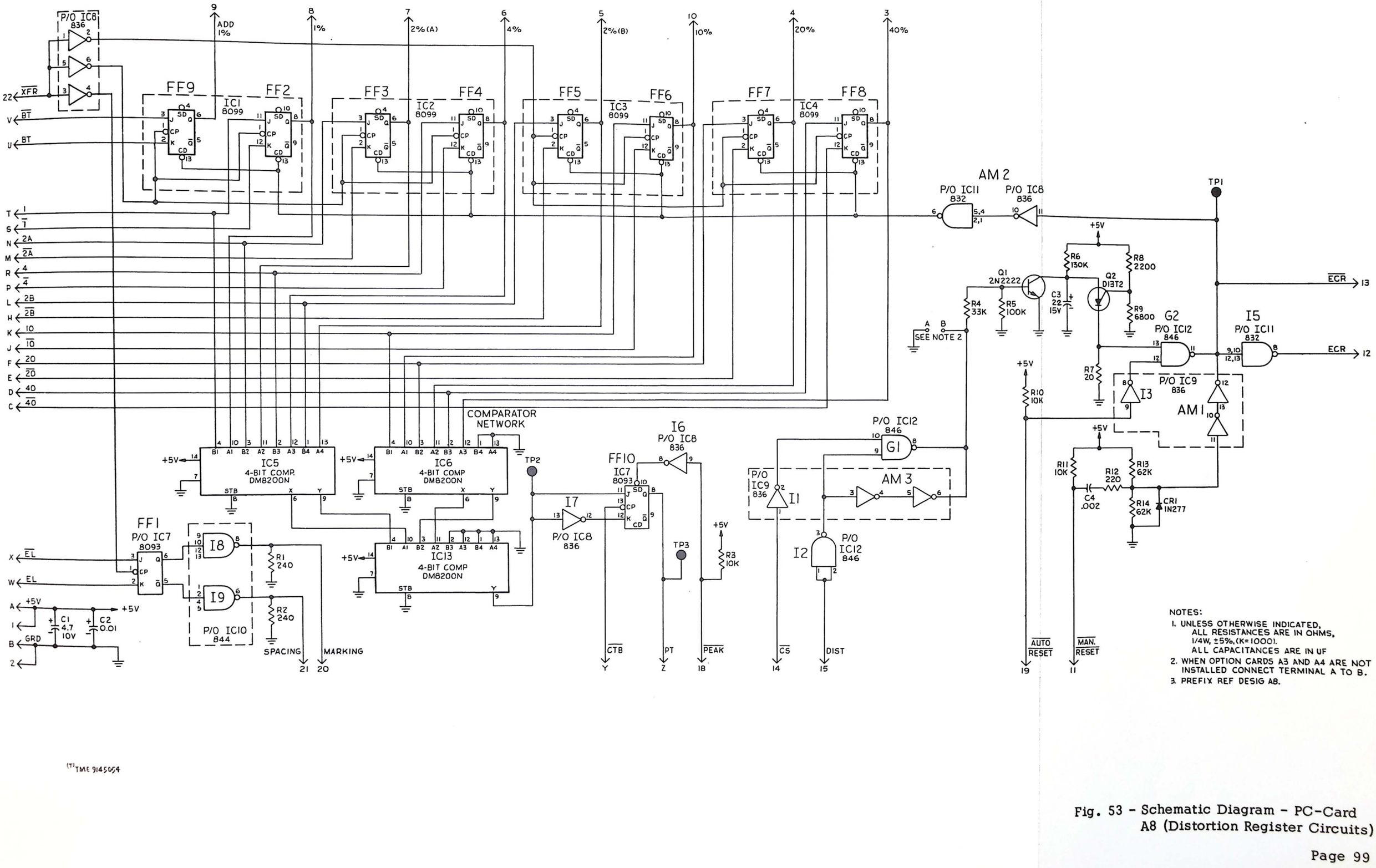


NOTES:

1. UNLESS OTHERWISE INDICATED,
   ALL RESISTANCES ARE IN OHMS, 1/4W, ±5% (K=1000)
   ALL CAPACITANCES ARE IN PF.
2. PREFIX REF DESIG. A7.

Fig. 52 - Schematic Diagram - PC-Card A7 (Sync Circuits)

TEST POINT	WAVEFORM	CONDITIONS
TP1	 NOTE: Observe negative spike as DISPLAY RESET switch is set to MAN.	INPUT SIGNAL: NONE SWITCH SETTINGS: MODE: PEAK
TP2	 NOTE: Obtain high by applying 10% bias distortion to input signal.	INPUT SIGNAL: REV, SYNC, 2400 BPS SWITCH SETTINGS: BIT RATE: 2400 MODE: PEAK S/S CODE LEVEL: SYNC TRANSITION SELECT: ALL DISPLAY RESET: MAN, THEN OFF
TP3		INPUT SIGNAL: REV, SYNC, 2400 BPS SWITCH SETTINGS: BIT RATE: 2400 MODE: PEAK S/S CODE LEVEL: SYNC TRANSITION SELECT: ALL DISPLAY RESET: MAN, THEN OFF

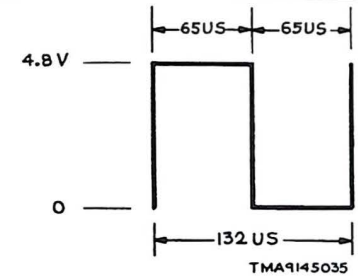
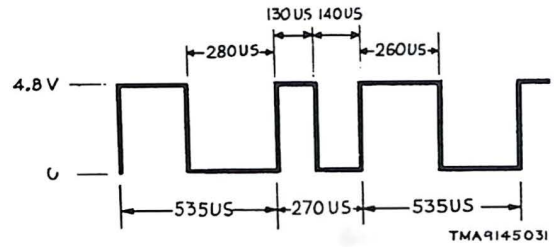
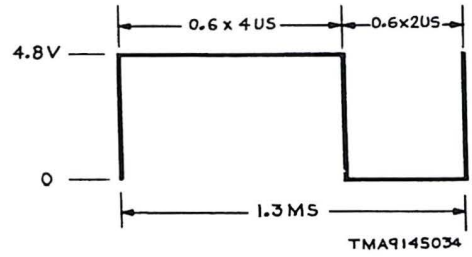
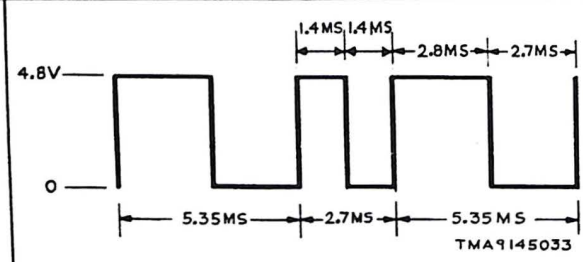
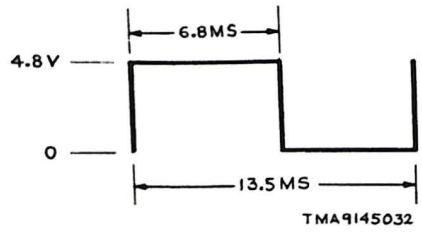


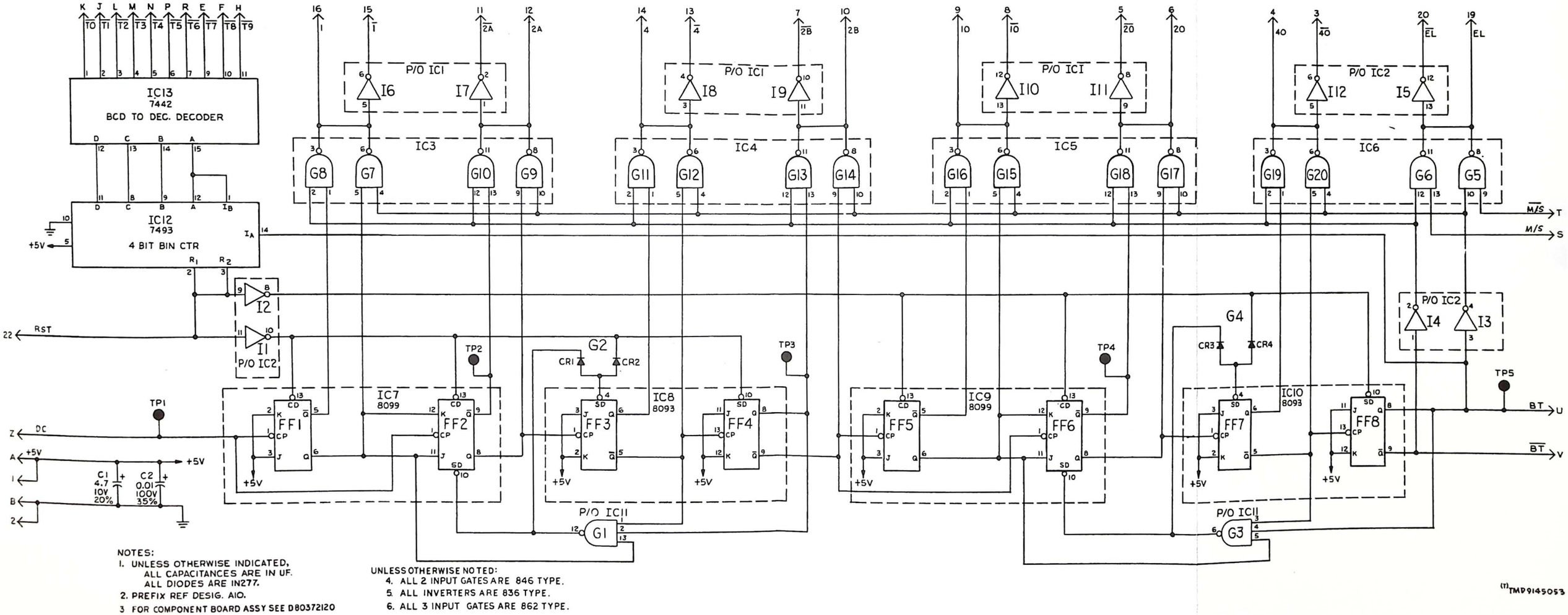
NOTES:

1. UNLESS OTHERWISE INDICATED, ALL RESISTANCES ARE IN OHMS, 1/4W, ±5%, (K=1000). ALL CAPACITANCES ARE IN UF
2. WHEN OPTION CARDS A3 AND A4 ARE NOT INSTALLED CONNECT TERMINAL A TO B.
3. PREFIX REF DESIG A8.

(T) TME 9145054

Fig. 53 - Schematic Diagram - PC-Card A8 (Distortion Register Circuits)

TEST POINT	WAVEFORM	CONDITIONS
TP1		INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: 75 S/S CODE LEVEL: 5
TP2		INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: 75 S/S CODE LEVEL: SYNC
TP3		INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: 75 S/S CODE LEVEL: SYNC
TP4		INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: 75 S/S CODE LEVEL: SYNC
TP5		INPUT SIGNAL: NONE SWITCH SETTINGS: BIT RATE: 75 S/S CODE LEVEL: SYNC



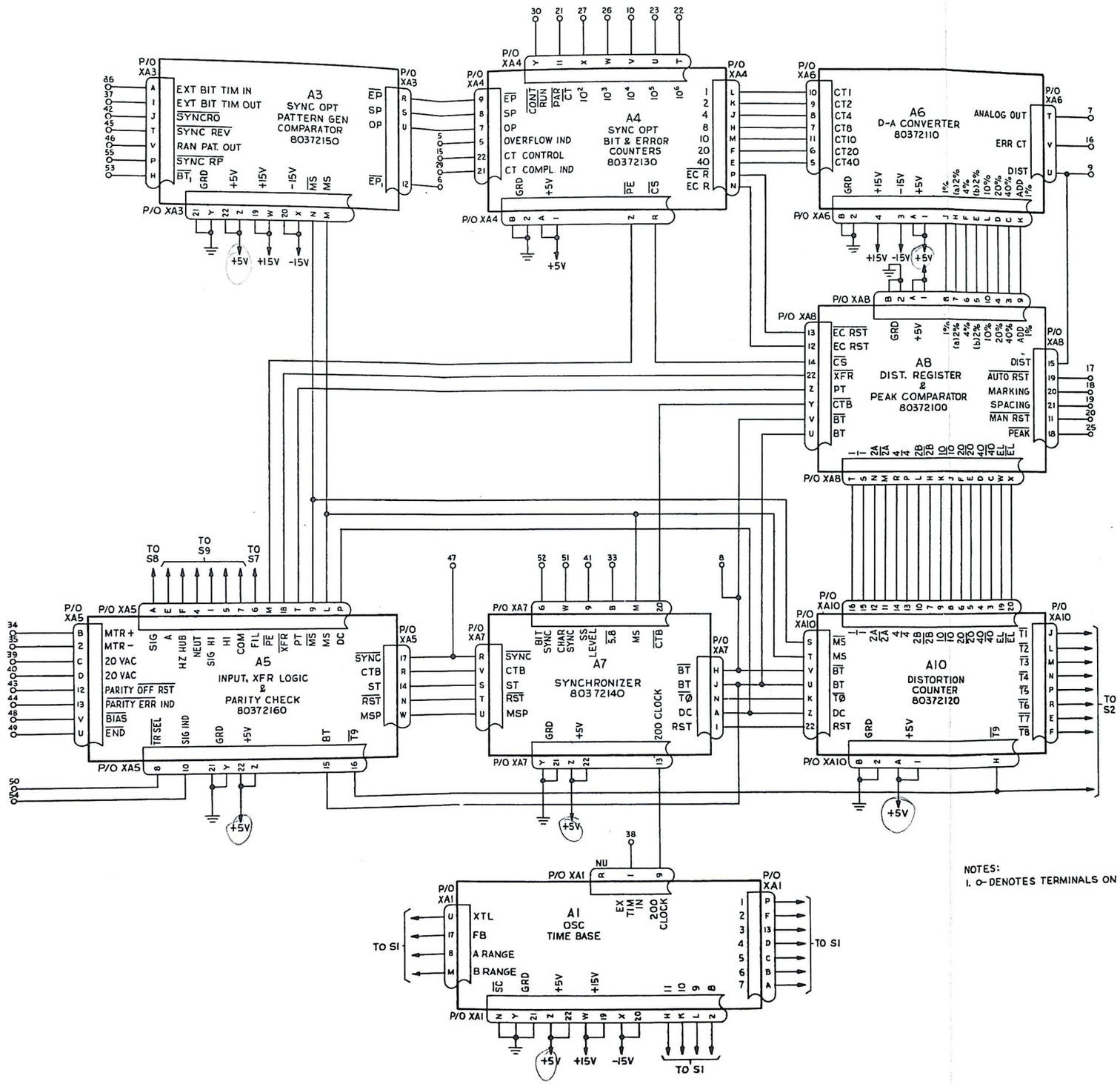
NOTES:

1. UNLESS OTHERWISE INDICATED, ALL CAPACITANCES ARE IN UF. ALL DIODES ARE IN277.
2. PREFIX REF DESIG. A10.
3. FOR COMPONENT BOARD ASSY SEE D80372120

UNLESS OTHERWISE NOTED:

4. ALL 2 INPUT GATES ARE 846 TYPE.
5. ALL INVERTERS ARE 836 TYPE.
6. ALL 3 INPUT GATES ARE 862 TYPE.

Fig. 54 - Schematic Diagram - PC-Card A10 (Distortion Counter Circuits)



NOTES:
1. O- DENOTES TERMINALS ON HARNESS BOARD.

D78800999

Fig. 55 - Over-All Schematic Diagram
(Sheet 1 of 2)

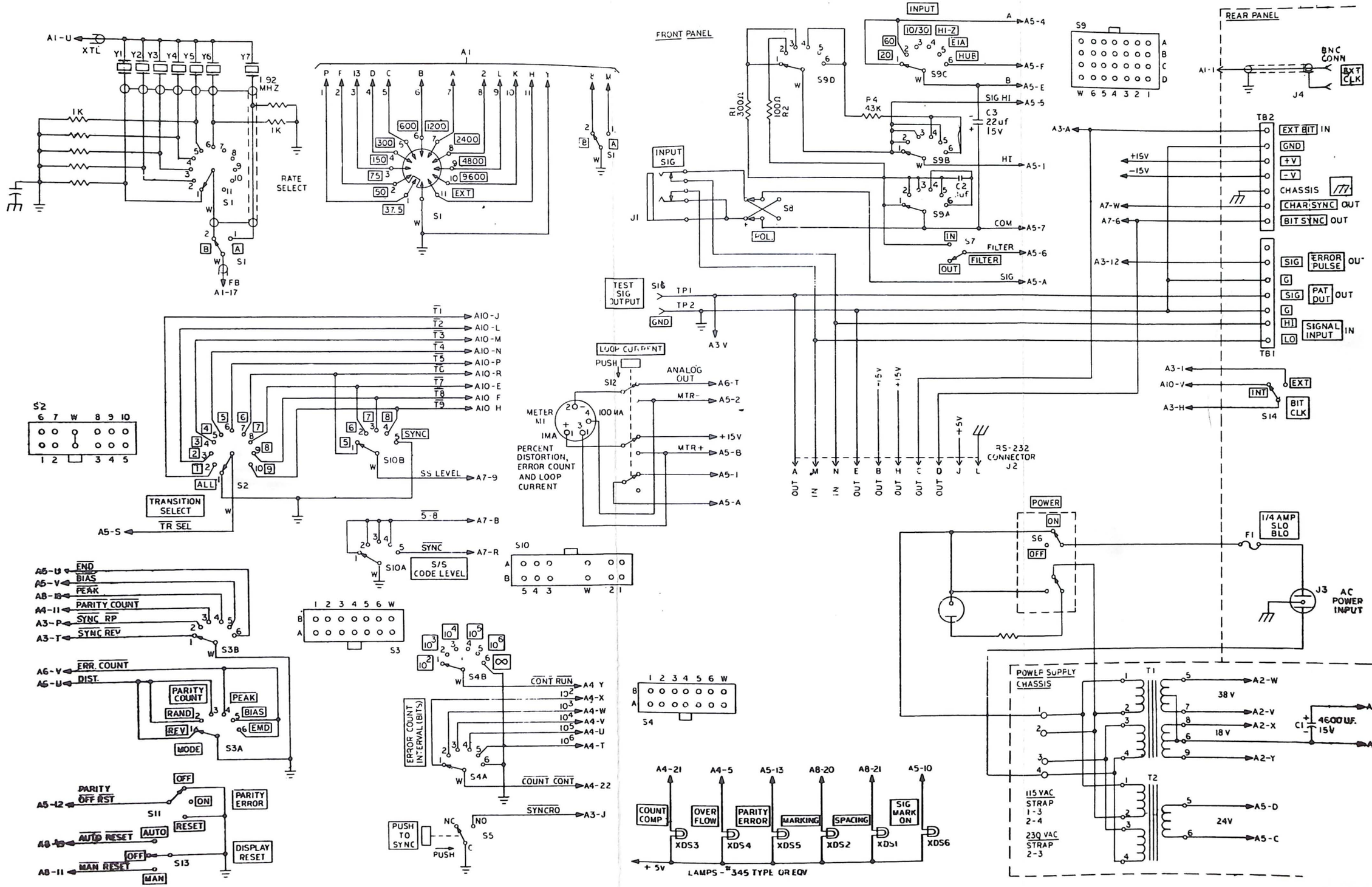


Fig. 55 - Over-All Schematic Diagram
(Sheet 2 of 2)

5. PARTS LIST

(A) Introduction

5.01 A complete list of replaceable electronic parts for the DMS-303A Analyzer is presented in (B) below. Table IX consists of an equipment breakdown into assemblies, subassemblies, and detailed parts; Table X consists of an optional accessories breakdown; and Tables XI through XXIV consist of breakdowns of PC-cards and assemblies into detailed parts.

(a) Within each table, parts are listed in alphanumeric order, by reference-designation symbol; for each entry, a brief description and the manufacturer part and code number are provided.

(b) Manufacturer codes are identified in Table VIII.

TABLE VIII

MANUFACTURER CODES

CODE NO.	MANUFACTURER	
01295	Texas Instruments, Semiconductor Div.	Dallas, Texas
02660	Amphenol Corp.	Broadview, Illinois
03508	General Elec. Co.	Syracuse, New York
04713	Motorola Semiconductor Products, Inc.	Phoenix, Arizona
12040	National Semiconductor Corp.	Danbury, Connecticut
21604	Buckeye Stamping Co.	Columbus, Ohio
22753	UID Electronics Corp.	Hollywood, Florida
24446	General Electric Co.	Schenectady, New York
56289	Sprague Electric Co.	North Adams, Massachusetts
71279	Cambridge Thermionic Corp.	Cambridge, Massachusetts
71400	Bussmann Mfg. Co.	St. Louis, Missouri
71450	CTS Corp.	Elkhart, Indiana

TABLE VIII (Cont'd)

CODE NO.	MANUFACTURER	
71785	Cinch Mfg. Co.	Chicago, Illinois
72136	Electro Motive Mfg. Co.	Willimantic, Connecticut
72619	Dialight Corp.	Brooklyn, New York
74545	Harvey Hubbell, Inc.	Bridgeport, Connecticut
74970	E.F. Johnson Co.	Waseca, Minnesota
75382	Kulka Electric Co.	Mount Vernon, New York
75915	Littelfuse, Inc.	Des Plaines, Illinois
81349	Military Specifications	
82389	Switchcraft, Inc.	Chicago, Illinois
91418	Radio Materials Co.	Chicago, Illinois
95146	Alco Electric	Lawrence, Massachusetts
96238	STELMA, Inc.	Stamford, Connecticut

(B) Parts List, Tabular Listing

5.02 Refer to Tables XI through XXIV for parts lists of Analyzer components listed in Table IX and of accessory items listed in Table X.

TABLE IX

ANALYZER MODULE, DMS-303A: 90372002-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
A1	CKT CARD ASSY, TIME BASE LOGIC	80372010-000	96238
A2	CKT CARD ASSY, POWER SUPPLY	80372020-000	96238
A5	CKT CARD ASSY, INPUT RELAY TRANS-LOGIC-PARITY CHECK:	80372160-000	96238
A6	CKT CARD ASSY, D-A	80372110-000	96238

TABLE XI (Cont'd)

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
A7	CKT CARD ASSY,SYNCHRONIZER:	80372140-000	96238
A8	CKT CARD ASSY,DISTORTION REG & PEAK COMPARATOR:	80372100-000	96238
A9	CKT CARD ASSY,EXTENDER CARD:	80372180-000	96238
A10	CKT CARD ASSY,DISTORTION COUNTER:	80372120-000	96238
A11	CRYSTAL BRACKET ASSY:	90372006-000	96238
A12	POWER SUPPLY,ANALYZER:	90372004-001	96238
A13	CKT CARD ASSY,ANALYZER HARNESS CARD:	80372170-000	96238
A14	LINE CORD ASSY:	74000054-000	96238
A14P1	CONN,PLUG,ELEC:	7571	74545
A14W1	CABLE ASSY,PWR:	74000000-002	96238
DS1,DS2	LIGHT,INDICATOR: colorless lens	507-3905-1437-500	72619
DS3	LIGHT,INDICATOR: green lens	507-3905-1432-500	76219
DS4	LIGHT,INDICATOR: yellow lens	507-3905-1433-500	72619
DS5	LIGHT,INDICATOR: red lens	507-3905-1431-500	72619
DS6	Same as DS1		
J1	JACK,TELEPHONE:	N114B	82389
J2	CONN,RCPT,ELEC: 12 pin	90372005-000	96238
M1	METER,DC: 0-100	48081098-000	96238
MP1	KNOB FOR S1	PS70D95C1BLK 2BLK	21604
MP2,3,4,9,10	KNOB FOR S2,S3,S4,S9, and S10	PS70BLS2BLK	21604
MP11,12	HANDLE	56025087-000	96238
R1	300Ω		
R2	100Ω		
R3	Not used		
R4	43k		
S1	(P/O A11 ASSY: 90372006-000)		
S2	SWITCH,ROTARY: 1 pole, 10 pos	46020384-000	96238
S3,S4	SWITCH,ROTARY: 2 pole, 6 pos	46020383-000	96238
S5	SWITCH,PB: SPDT, 115vac mom.	MSP105F	95146
S6	SWITCH,ROCKER:	LRSW322N30KCR	22753
S7	SWITCH,TOGGLE: SPDT, 115vac	MST105D	95146
S8	SWITCH,TOGGLE: DPDT, 115vac	MST205N	95146
S9	SWITCH,ROTARY: 4 pole, 6 pos	46020385-000	96238
S10	SWITCH,ROTARY: 2 pole, 5 pos	46020382-000	96238

TABLE IX (Cont'd)

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
S11	SWITCH,TOGGLE: SPDT, 115vac	MST105H	95146
S12	SWITCH,PB: 125 vac	MSPE406E	95146
S13	Same as S11		
TP1	POST,BINDING: red	111-102	74970
TP2	POST,BINDING: black	111-103	74970
XDS1-XDS6	SOCKET,IND LIGHT:	515-0012	72619
Y1-Y6	FREQUENCY values of crystals are determined by the rate specified by the customer		
Y7	XTAL UNIT,QTZ: 1.920mHz	40040081-000	96238

TABLE X

ACCESSORY ITEMS: (OPTIONAL)

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
A3	CKT CARD ASSY,SYNC OPTION PATTERN GEN & COMPARATOR:	80372150-000	96238
A4	CKT CARD ASSY,SYNC OPTION BIT-ERROR COUNTERS:	80372130-000	96238
	CASE AND COVER ASSEMBLY	64030083-000	96238
	DIAL ASSEMBLY:	57025141-000	96238
Y1	XTAL UNIT,QTZ: 291.200kHz	40040082-001	96238
Y2	XTAL UNIT,QTZ: 363.712kHz	40040082-002	96238
Y3	XTAL UNIT,QTZ: 391.296kHz	40040082-004	96238
Y4	XTAL UNIT,QTZ: 474.880kHz	40040082-006	96238
Y5	XTAL UNIT,QTZ: 352.000kHz	40040082-003	96238
Y6	XTAL UNIT,QTZ: 430.400kHz	40040082-005	96238
	(Dial ASSY 57025141-000 AND CRYSTALS Y1-Y6 ARE USED SIMULTANEOUSLY)		
	DIAL ASSEMBLY:	57000021-000	96238
Y1-Y6	(CRYSTALS SPECIFIED BY CUSTOMER)		

TABLE XI

PC-CARD ASSEMBLY, TIME-BASE LOGIC: A1, 80372010-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
A1	CKT CARD ASSY,OSCILLATOR:	80372190-000	96238
C1,C2	CAP,FXD,CERAMIC: 0.01uf, ±35%, 100V	TA01UF	91418
C3	CAP,FXD,ELCTLT: 4.7uf, ±20% 10V	CS13BC475M	81349
CR1,CR2	SEMICOND,DIODE: silicon	1N914	81349
CR3-CR5	SEMICOND,DIODE: Germanium	1N277	81349
CR6	Same as CR1		
IC1,IC2	INTEGRATED CKT: NAND/NOR Gate	SN15849N	01295
IC3,IC4	INTEGRATED CKT: NAND/NOR Gate	MC858P	04713
IC5,IC6	INTEGRATED CKT: Quad 2-input NAND/ NOR Gate	SN15846N	01295
IC7	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158097N	01295
IC8	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158099N	01295
IC9	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158094N	01295
IC10	INTEGRATED CKT: 4 bit binary counter	SN7493N	01295
Q1	TRANSISTOR: NPN	2N2222	81349
Q2	TRANSISTOR: NPN	2N706	81349
Q3	Same as Q1		
R1	RES,FXD,COMP: 6.8k ohms, ±5%, 1/4W	RC07GF682J	81349
R2	RES,FXD,COMP: 2.2k ohms, ±5%, 1/4W	RC07GF222J	81349
R3	RES,FXD,COMP: 1k ohms, ±5%, 1/4W	RC07GF102J	81349
R4-R16	RES,FXD,COMP: 10k ohms, ±5%, 1/4W	RC07GF103J	81349
R17	Same as R3		
R18	RES,FXD,COMP: 3k ohms, ±5%, 1/4W	RC07GF302J	81349
R19	RES,FXD,COMP: 47k ohms, ±5%, 1/4W	RC07GF473J	81349
R20	Same as R18		

TABLE XII

PC-CARD ASSEMBLY, OSCILLATOR: A1A1, 80372190-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,CERAMIC: 0.01uf, ±35%, 100V	TA01UF	91418
C2	CAP,FXD,CERAMIC: 0.1uf, ±20%, 25V	5C023104X0250B3	56289
C3-C8	Not used		
C9,C10	Same as C1		
CR1	SEMICOND,DIODE: Silicon	1N914	81349
CR2-CR5	SEMICOND,DIODE: Germanium	1N277	81349
Q1	TRANSISTOR: PNP	2N2907	81349
Q2,Q3	TRANSISTOR:	2N5222	04713
Q4	TRANSISTOR: NPN	2N706	81349
Q5	TRANSISTOR: NPN	2N2222	81349
Q6	Same as Q4		
R1	RES,FXD,COMP: 8.2k ohms, ±5%, 1/4W	RC07GF822J	81349
R2	RES,FXD,COMP: 3k ohms, ±5%, 1/4W	RC07GF302J	81349
R3	RES,FXD,COMP: 5.1k ohms, ±5%, 1/4W	RC07GF512J	81349
R4	RES,FXD,COMP: 3.3k ohms, ±5%, 1/4W	RC07GF332J	81349
R5	RES,FXD,COMP: 39k ohms, ±5%, 1/4W	RC07GF393J	81349
R6	RES,FXD,COMP: 18k ohms, ±5%, 1/4W	RC07GF183J	81349
R7-R11	Not used		
R12	RES,FXD,COMP: 15k ohms, ±5%, 1/4W	RC07GF153J	81349
R13	RES,FXD,COMP: 2.4k ohms, ±5%, 1/4W	RC07GF242J	81349
R14	RES,FXD,COMP: 10 ohms, ±5%, 1/4W	RC07GF100J	81349
R15	RES,FXD,COMP: 10k ohms, ±5%, 1/4W	RC07GF103J	81349
R16	RES,FXD,COMP: 2k ohms, ±5%, 1/4W	RC07GF202J	81349

TABLE XIII

PC-CARD ASSEMBLY, POWER SUPPLY: A2, 80372020-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1,C2	CAP,FXD,ELCTLT: 250uf, 30V	39D257G030EL4	56289
C3	CAP,FXD,ELCTLT: 15uf, ±10%, 35V	CS13BF156K	81349
C4	CAP,FXD,ELCTLT: 1uf, ±10%, 35V	CS13BF105K	81349
C5	Same as C3		
C6	CAP,FXD, MICA: 4700pf, ±5%, 500V	DM19E472J0500 WV4CR	72136
C7	CAP,FXD,MICA: 560pf, ±10%, 500V	DM15F561K0500 WV4CR	72136

TABLE XIII (Cont'd)

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C8	CAP,FXD,ELCTLT: 22uf, ±10%, 35V	CS13BF226K	81349
C9,C10	Same as C3		
CR1-CR4	SEMICOND, DIODE: Silicon	1N645	81349
CR5,CR6	SEMICOND, DIODE: Silicon	1N1614	81349
CR7	RECTIFIER, Silicon:	C106Q21	03508
F1,F2	FUSE, CARTRIDGE: 1/8 AMP	312-125	75915
F3	FUSE, CARTRIDGE: 3/4 AMP	312-250	75915
Q1	TRANSISTOR: NPN	2N1613	81349
Q2	TRANSISTOR: NPN	2N930	81349
Q3,Q4	TRANSISTOR: PNP	2N2905	81349
Q5	TRANSISTOR: PNP	2N297	81349
Q6	Same as Q1		
Q7,Q8	Same as Q2		
Q9	Same as Q3		
R1	RES, FXD, COMP: 39 ohms, ±5%, 2W	RC42GF390J	81349
R2-R4	RES, FXD, COMP: 1k ohms, ±5%, 1/4W	RC07GF102J	81349
R5	RES, FXD, COMP: 1.5k ohms, ±5%, 1/4W	RC07GF152J	81349
R6	RESISTOR, VAR: 500 ohms, 1/4W	200P1-501	80294
R7	Same as R2		
R8	RES, FXD, COMP: 6.8k ohms, ±5%, 1/4W	RC07GF682J	81349
R9	RES, FXD, COMP: 680 ohms, ±5%, 1/2W	RC20GF681J	81349
R10	Same as R1		
R11-R13	Same as R2		
R14	Same as R8		
R15	RES, FXD, COMP: (Factory Select)		
R16	RES, FXD, WW: 1 ohm, ±5%, 5W	RW67V1R0	81349
R17	RES, FXD, COMP: 180 ohms, ±5%, 1/4W	RC07GF181J	81349
R18	RES, FXD, COMP: 560 ohms, ±5%, 1/4W	RC07GF561J	81349
R19	RES, FXD, COMP: 22 ohms, ±5%, 1/2W	RC20GF220J	81349
R20	RES, FXD, FILM: 453 ohms, ±1%, 1/8W	RN55D4530F	81349
R21	RESISTOR, VAR: 200 ohms, 1/4W	200P1-201	80294
R22	RES, FXD, FILM: 732 ohms, ±1%, 1/8W	RN55D7320F	81349
R23	RES, FXD, COMP: 2.2k ohms, ±5%, 1/4W	RC07GF222J	81349
R24	RES, FXD, COMP: 470 ohms, ±5%, 1/4W	RC07GF471J	81349
R25	Same as R18		
R26	RES, FXD, COMP: 620 ohms, ±5%, 1/4W	RC07GF621J	81349
R27,R28	Same as R2		
R29	RES, FXD, COMP: 680 ohms, ±5%, 1/4W	RC07GF681J	81349

TABLE XIII (Cont'd)

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
VR1	SEMICOND, DIODE: Zener	1N752	81349
VR2	SEMICOND, DIODE: Zener	1N748	81349
VR3	Same as VR1		

TABLE XIV

PC-CARD ASSEMBLY, SYNC OPTION PATTERN GENERATOR AND COMPARATOR: A3, 80372150-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1, C2	CAP, FXD, MICH: 510pf, ±5%, 500V	DM15F511J0500 WV4CR	72136
C3	CAP, FXD, ELCTLT: 4.7uf, ±20%, 10V	CS13BC475M	81349
C4	CAP, FXD, CERAMIC: 0.01uf, ±35%, 100V	TA01UF	91418
C5	CAP, FXD, MICA: 120pf, ±10%, 500V	DM15E121K0500 WV4CR	72136
CR1, CR2	SEMICOND, DIODE: Germanium	1N277	81349
CR3	Not used		
CR4	Same as CR1		
CR5, CR6	SEMICOND, DIODE: Silicon	1N914	81349
CR7	Same as CR1		
IC1, IC2	INTEGRATED CKT: Hex inverter	SN15836N	01295
IC3	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158099N	01295
IC4	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158093N	01295
IC5, IC6	INTEGRATED CKT: 5-bit shift reg.	SN7496N	01295
IC7	INTEGRATED CKT: Dual 4-input expandable NAND gate	SN15830N	01295
IC8-IC10	INTEGRATED CKT: Quad 2-input NAND/NOR gate	SN15846N	01295
Q1	TRANSISTOR: NPN	2N2222	81349
Q2	TRANSISTOR: PNP	2N2907	81349
Q3	Same as Q1		
Q4	Same as Q2		
Q5	Same as Q1		
Q6	TRANSISTOR:	2N706	81349

TABLE XIV (Cont'd)

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
R1	RES, FXD, COMP: 10k ohms, ±5%, 1/4W	RC07GF103J	81349
R2	RES, FXD, COMP: 1.5k ohms, ±5%, 1/4W	RC07GF152J	81349
R3, R4	RES, FXD, COMP: 62k ohms, ±5%, 1/4W	RC07GF623J	81349
R5	Same as R2		
R6, R7	Same as R3		
R8, R9	Same as R1		
R10	RES, FXD, COMP: 20k ohms, ±5%, 1/4W	RC07GF203J	81349
R11	RES, FXD, COMP: 6.8k ohms, ±5%, 1/4W	RC07GF682J	81349
R12	RES, FXD, COMP: 47k ohms, ±5%, 1/4W	RC07GF473J	81349
R13, R14	RES, FXD, FILM: 1.5k ohms, ±1%, 1/4W	RN65B1501F	81349
R15, R16	RES, FXD, FILM: 6190 ohms, ±5%, 1/4W	RN60D6191F	81349
R17, R18	RES, FXD, COMP: 1k ohms, ±5%, 1/2W	RC20GF102J	81349
R19	RES, FXD, COMP: 15 ohms, ±5%, 1/2W	RC20GF150J	81349
R20	Same as R11		
R21	RES, FXD, COMP: 2.2k ohms, ±5%, 1/4W	RC07GF222J	81349
R22	RES, FXD, COMP: 1k ohms, ±%5, 1/4W	RC07GF102J	81349

TABLE XV

PC-CARD ASSEMBLY, SYNC OPTION BIT-ERROR COUNTERS: A4, 80372130-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP, FXD, ELCTLT: 4.7uf, ±20%, 10V	CS13BC475M	81349
C2	CAP, FXD, CERAMIC: 0.01uf, ±35%, 100V	TA01UF	91418
CR1, CR2	SEMICOND, DIODE: Germanium	1N277	81349
IC1	INTEGRATED CKT: Triple 3-input NAND/ NOR gate	SN15862N	01295
IC2	INTEGRATED CKT: Hex inverter	SN15836N	01295
IC3-IC8	INTEGRATED CKT: Decade counter	SN7490N	01295
IC9	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158093N	01295
IC10	INTEGRATED CKT: Dual 4 input NAND/ NOR Power gate	SN15844N	01295
IC11, IC12	Same as IC3		
R1	RES, FXD, COMP: 10k ohms, ±5%, 1/4W	RC07GF103J	81349
R2	RES, FXD, COMP: 240 ohms, ±5%, 1/4W	RC07GF241J	81349
R3	Same as R1		
R4	Same as R2		

TABLE XVI

PC-CARD ASSEMBLY, INPUT RELAY TRANSFER LOGIC-PARITY CHECK: A5, 80372160-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP, FXD, ELCTLT: 4.7uf, ±20%, 10V	CS13BC475M	81349
C2, C3	CAP, FXD, CERAMIC: 0.01uf, ±35%, 100V	TA01UF	91418
C4	CAP, FXD, CERAMIC: 0.001uf, ±20% 1000V	5GAD10	56289
C5	CAP, FXD, ELCTLT: 47uf, ±10%, 35V	CS13BF476K	81349
C6	Same as C4		
C7	Same as C2		
C8	CAP, FXD, CERAMIC: 0.03uf, ±35%, 100V	TA03UF	91418
C9-C12	CAP, FXD, MICA: 510pf, ±5%, 500V	DM15E511J0 500WV4CR	56289
CR1, CR2	SEMICOND, DIODE: Silicon	1N914	81349
CR3-CR6	SEMICOND, DIODE: Germanium	1N277	81349
CR7	Same as CR1		
CR8-CR11	SEMICOND, DIODE: Silicon	1N645	81349
CR12-CR14	Same as CR3		
CR15	Same as CR1		
CR16-CR18	Same as CR3		
CR19, CR20	Same as CR1		
IC1	INTEGRATED CKT: Hex inverter	SN15836N	01295
IC2	INTEGRATED CKT: Triple 3-input NAND/ NOR gate	SN15862N	01295
IC3	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158093N	01295
IC4	INTEGRATED CKT: Dual 4-input expandable NAND gate	SN15830N	01295
IC5	INTEGRATED CKT: Dual 4-input NAND/ NOR Power gate	SN15844N	01295
IC6	INTEGRATED CKT: flip-flop	SN15845N	01295
IC7, IC8	INTEGRATED CKT: Quad 2-input NAND/ NOR gate	SN15846N	01295
Q1	TRANSISTOR: Dual	TD101	56289
Q2, Q3	TRANSISTOR: PNP	2N2907	81349
Q4	TRANSISTOR: Unijunction	2N2646	04713
Q5	Same as Q2		
Q6	TRANSISTOR: NPN	2N706	81349

TABLE XVI (Cont'd)

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
R1-R3	Not used		
R4, R5	RES, FXD, COMP: 5.6k ohms, ±5%, 1/4W	RC07GF562J	81349
R6	RES, FXD, COMP: 3k ohms, ±5%, 1/4W	RC07GF302J	81349
R7	RES, FXD, COMP: 8.2k ohms, ±5%, 1/4W	RC07GF822J	81349
R8	Same as R6		
R9	RES, FXD, COMP: 10k ohms, ±5%, 1/4W	RC07GF103J	81349
R10	RES, FXD, COMP: 33k ohms, ±5%, 1/4W	RC07GF333J	81349
R11, R12	RES, FXD, COMP: 1k ohms, ±5%, 1/4W	RC07GF102J	81349
R13-R16	Same as R9		
R17	RES, FXD, COMP: 220 ohms, ±5%, 1/4W	RC07GF221J	81349
R18, R19	RES, FXD, COMP: 62k ohms, ±5%, 1/4W	RC07GF623J	81349
R20	Same as R9		
R21	RES, FXD, COMP: 240 ohms, ±5%, 1/4W	RC07GF241J	81349
R22	Same as R17		
R23, R24	Same as R18		
R25	Same as R21		
R26	RES, FXD, COMP: 18k ohms, ±5%, 1/2W	RC20GF183J	81349
R27	Same as R10		
R28	RES, FXD, COMP: 1.5k ohms, ±5%, 1/4W	RC07GF152J	81349
R29	Same as R17		
R30, R31	Same as R18		
R32	Same as R17		
R33, R34	Same as R18		
T1	TRANSFORMER, PULSE:	43003041-000	96238
VR1	SEMICOND, DIODE: Zener	1N758A	81349
VR2	SEMICOND, DIODE: Zener	1N746A	81349

TABLE XVII

PC-CARD ASSEMBLY, D-A CONVERTER: A6, 80372110-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1, C2	CAP, FXD, ELCTLT: 4.7uf, ±20%, 35V	CS13AF4R7M	81349
C3	CAP, FXD, ELCTLT: 4.7uf, ±20%, 10V	CS13BC475M	81349
C4	CAP, FXD, CERAMIC: 0.01uf, ±35%, 100V	TA01UF	91418
IC1-IC5	INTEGRATED CKT: Quad 2-input NAND/ NOR gate	SN15846N	01295
IC6	INTEGRATED CKT: Hex inverter	SN15836N	01295

TABLE XVII (Cont'd)

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
Q1-Q8	TRANSISTOR: NPN	2N2222	81349
R1	RES, FXD, COMP: 10k ohms, ±5%, 1/4W	RC07GF103J	81349
R2	RES, FXD, COMP: 75k ohms, ±5%, 1/4W	RC07GF753J	81349
R3	RES, FXD, COMP: 15k ohms, ±5%, 1/4W	RC07GF153J	81349
R4	RES, FXD, FILM: 750k ohms, ±10%, 1/4W	RN65C7503F	81349
R5	Same as R1		
R6	Same as R2		
R7	Same as R3		
R8	RES, FXD, COMP: 374k ohms, ±1%, 1/8W	RN60C3743F	81349
R9	Same as R1		
R10	Same as R2		
R11	Same as R3		
R12	RES, FXD, FILM: 187k ohms, ±1%, 1/8W	RN60C1873F	81349
R13	Same as R1		
R14	Same as R2		
R15	Same as R3		
R16	Same as R8		
R17	Same as R1		
R18	Same as R2		
R19	Same as R3		
R20	RES, FXD, FILM: 75k ohms, ±1%, 1/8W	RN60C7502F	81349
R21	Same as R1		
R22	Same as R2		
R23	RES, FXD, COMP: 22k ohms, ±5%, 1/4W	RC07GF223J	81349
R24	RES, FXD, FILM: 37.4k ohms,	RN60C3742D	81349
R25	Same as R1		
R26	Same as R2		
R27	RES, FXD, COMP: 47k ohms, ±5%, 1/4W	RC07GF473J	81349
R28	RES, FXD, FILM: 18.7k ohms, ±5%, 1/8W	RN60C1872D	81349
R29	Same as R1		
R30	Same as R2		
R31	Same as R3		
R32	Same as R4		
R33, R34	Same as R1		

TABLE XVIII

PC-CARD ASSEMBLY, SYNCHRONIZER: A7, 80372140-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,ELCTLT: 4.7uf, ±20%, 10V	CS13BC475M	81349
C2	CAP,FXD,CERAMIC: 0.01uf, ±35%, 100V	TA01UF	91418
C3	CAP,FXD,MICA: 51pf, ±5%, 500V	DM15E510J0500 WV4CR	72136
C4	CAP,FXD,MICA: 820pf, ±5%, 500V	DM15E821J0500 WV4CR	72136
IC1	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158097N	01295
IC2	INTEGRATED CKT: Quad 2-input NAND/ NOR gate	SN15846N	01295
IC3	INTEGRATED CKT: 2 input gate	SN15849N	01295
IC4	INTEGRATED CKT: Triple 3-input NAND/ NOR gate	SN15862N	01295
IC5	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158094N	01295
IC6	INTEGRATED CKT: 3 input gate	SN15863N	01295
IC7	INTEGRATED CKT: Hex inverter	SN15837N	01295
IC8	Same as IC1		
IC9	INTEGRATED CKT: one-shot multivibrator	SN15851N	01295
IC10	Same as IC3		
IC11	Not used		
IC12	INTEGRATED CKT: Dual 4-input expand-able NAND gate	SN15830N	01295
IC13	INTEGRATED CKT: flip-flop	SN15845N	01295
IC14	Same as IC2		
IC15	INTEGRATED CKT: flip-flop	SN15848N	01295
R1	RES,FXD,COMP: 10k ohms, ±5%, 1/4W	RC07GF103J	81349
R2,R3	RES,FXD,COMP: 20k ohms, ±5%, 1/4W	RC07GF203J	81349

TABLE XIX

PC-CARD ASSEMBLY, DISTORTION REGULATOR AND PEAK COMPARITOR: A8, 80372100-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,ELCTLT: 4.7uf, ±20%, 10V	CS13BC475M	81349
C2	CAP,FXD,CERAMIC: 0.01uf, ±35%, 100V	TA01UF	91418

TABLE XIX (Cont'd)

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C3	CAP,FXD,ELCTLT: 56uf, ±10%, 15V	CS13BD566K	81349
C4	CAP,FXD,CERAMIC: 2000pf, 1000V	DD202	71590
CR1	SEMICOND,DIODE: Germanium	1N277	81349
IC1-IC4	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158099N	01295
IC5,IC6	INTEGRATED CKT: 4 Bit comparitor	DM8200N	12040
IC7	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158093N	01295
IC8,IC9	INTEGRATED CKT: Hex inverter	SN15836N	01295
IC10	INTEGRATED CKT: Dual 4-input NAND/ NOR power gate	SN15844N	01295
IC11	INTEGRATED CKT: Dual 4-input NAND/ NOR buffer	SN15832N	01295
IC12	INTEGRATED CKT: Quad 2-input NAND/ NOR gate	SN15846N	01295
Q1	TRANSISTOR: NPN	2N2222	81349
Q2	TRANSISTOR: Unijunction	D13T2	24446
R1,R2	RES,FXD,COMP: 240 ohms, ±5%, 1/4W	RC07GF241J	81349
R3	RES,FXD,COMP: 10k ohms, ±5%, 1/4W	RC07GF103J	81349
R4	RES,FXD,COMP: 33k ohms, ±5%, 1/4W	RC07GF333J	81349
R5	RES,FXD,COMP: 100k ohms, ±5%, 1/4W	RC07GF104J	81349
R6	RES,FXD,COMP: 47k ohms, ±5%, 1/4W	RC07GF473J	81349
R7	RES,FXD,COMP: 20 ohms, ±5%, 1/4W	RC07GF200J	81349
R8	RES,FXD,COMP: 2.2k ohms, ±5%, 1/4W	RC07GF222J	81349
R9	RES,FXD,COMP: 6.8k ohms, ±5%, 1/4W	RC07GF682J	81349
R10,R11	Same as R3		
R12	RES,FXD,COMP: 1.5k ohms, ±5%, 1/4W	RC07GF152J	81349
R13,R14	RES,FXD,COMP: 62k ohms, ±5%, 1/4W	RC07GF623J	81349

TABLE XX

PC-CARD ASSEMBLY, EXTENDER CARD: A9, 80372180-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
J1	CONN,RCPT,ELEC 22 Pin, dual	225-22221-10500	02660

TABLE XXI

PC-CARD ASSEMBLY, DISTORTION COUNTER: A10, 80372120-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,ELCTLT: 4.7uf, ±20%, 10V	CS13BC475M	81349
C2	CAP,FXD,CERAMIC: 0.1uf, ±35%, 100V	TA01UF	91418
CR1-CR4	SEMICOND,DIODE: Germanium	1N277	81349
IC1,IC2	INTEGRATED CKT: Hex Inverter	SN15836N	01295
IC3-IC6	INTEGRATED CKT: Quad 2-input NAND/ NOR gate	SN15846N	01295
IC7	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158099N	01295
IC8	INTEGRATED CKT: Dual J-K clocked flip-flop	SN158093N	01295
IC9	Same as IC7		
IC10	Same as IC8		
IC11	INTEGRATED CKT: triple 3-input NAND/ NOR gate	SN15862N	01295
IC12	INTEGRATED CKT: 4 bit binary counter	SN7493N	01295
IC13	INTEGRATED CKT: BCD to decimal 4-10 line decoder	SN7442N	01295

TABLE XXII

CRYSTAL BRACKET ASSEMBLY: A11, 90372006-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
R1-R7	RES,FXD,COMP: 1k ohms, ±5%, 1/4W	RC07GF102J	81349
S1	SWITCH,ROTARY:	C212-26036-2-1	71450
XY1-XY7	SOCKET,CRYSTAL:	TS0205P01	81349

TABLE XXIII

POWER SUPPLY, ANALYZER: A12, 90372004-001

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
C1	CAP,FXD,ELCTLT: 4600uf, 15V	36D462G015AA2A	56289
E1-E4	Terminal, Standoff:	4820-1-0516	71279
F1	FUSE, CARTRIDGE: 1/4 Amp-3AG	312-250	75915
J1	CONN,RCPT,ELEC:	7595	74545
J2	CONN,RCPT,ELEC: coaxial	UG1094U	81349
S1	SWITCH,TOGGLE: SPDT	MST105D	95146
T1	TRANSFORMER,PWR: 132Vac, 47Hz	43000276-000	96238
T2	TRANSFORMER,PWR: 115-230Vac	43000277-000	96238
TB1,TB2	TERMINAL BOARD: 7 term	599-2004-7	75382
XF1	FUSEHOLDER:	HKP	71400

TABLE XXIV

PC-CARD ASSEMBLY, ANALYZER HARNESS CARD: A13,80372170-000

REF DESIG.	DESCRIPTION	MFR'S PART NO.	MFR'S CODE NO.
XA1-XA10	CONN,RCPT,ELEC: 22 pin	252-22-30-220	71785