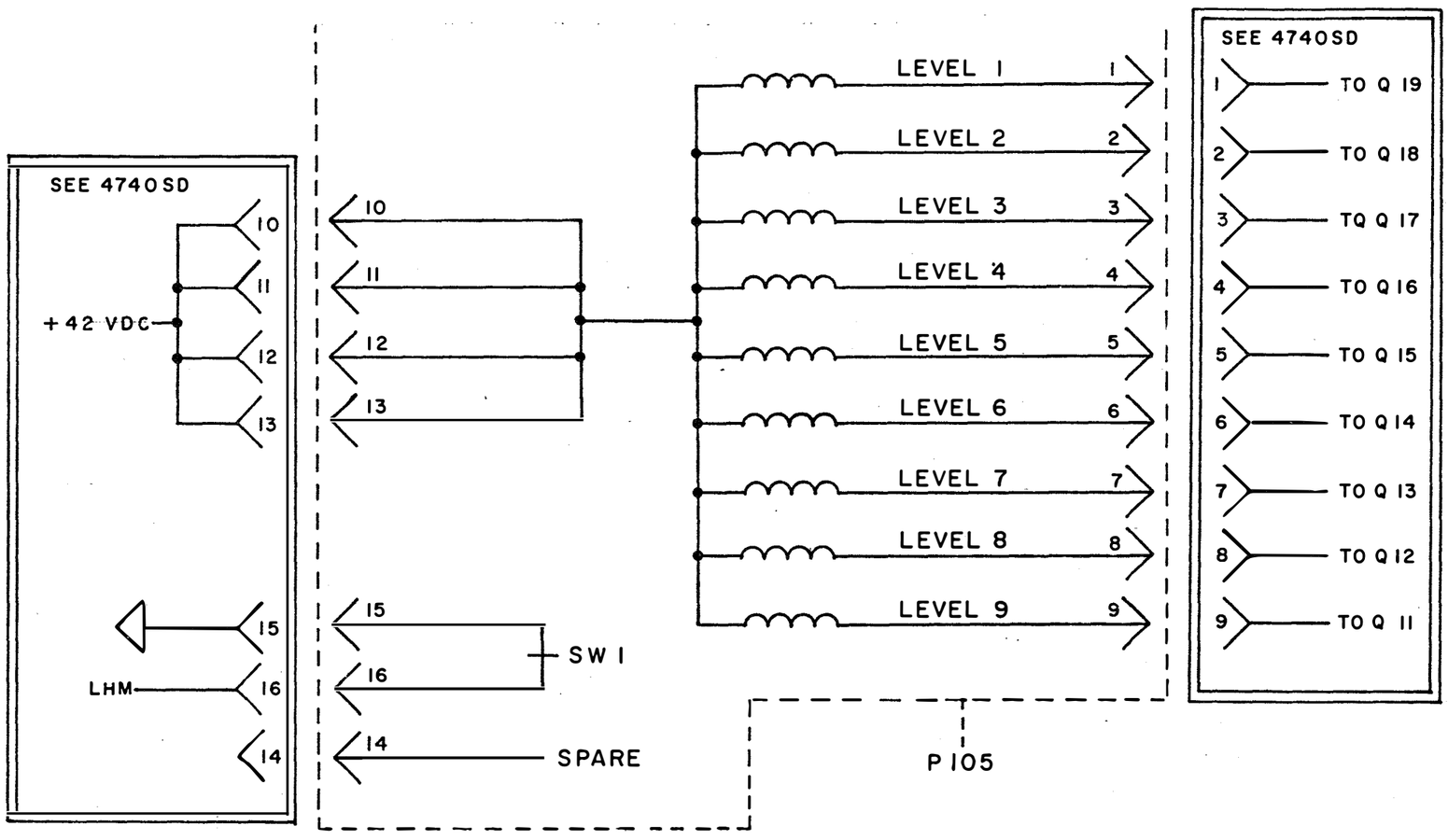
MODEL 43 KSR SETS (4320 SERIES) — WDP 0493

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
		SCHEMATIC DIAGRAMS																														
4013 SD	1	430850 WIRE MATRIX PRINT HEAD	1	1	1																											
4080 SD	ALL	OPCON (43K 101 CAA)	2	2	2																											
4700 SD	ALL	POWER SUPPLY	6	6	6																											
4740 SD	ALL	410740 LOGIC CARD	4	5	6																											
		ACTUAL DIAGRAMS																														
9100 WD	1	LOGIC SYMBOLS AND TRUTH TABLES	2	2	2																											
9612 WD	1	430550 REAR FRAME ASSEMBLY	1	1	1																											
9635 WD	1	AUXILIARY AND DATA TERMINAL	1	1	1																											
		CIRCUIT CARD ASSEMBLIES																														
410080	1	CONSOLE LOGIC	6	7	7																											
410700	1	POWER SUPPLY	9	9	9																											
410740	ALL	K.P. LOGIC	6	6	6																											
		CIRCUIT CARD DESCRIPTION																														
4700 CD	ALL	POWER SUPPLY	1	1	1																											
4740 CD	ALL	M43 LOGIC CARD	1	2	2																											
4080 CD	ALL	410080 CONSOLE LOGIC CARD	2	2	2																											

TELETYPE CORPORATION — 25249-R — NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP. — SHEET 1 OF 1

R&D FORM 361 (6-66)



NOTE – 430803 CABLE ASSEMBLY IS SOLDERED TO AND IS PART OF 410013 CIRCUIT CARD ASSEMBLY.

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	8-3-76	24352R

SCHEMATIC
FOR
430850
WIRE MATRIX
PRINT HEAD

APPROVALS		
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

ENGR. D.G.G	DSGNR.
DRN. J.K.	DATE 6-10-76
R&D FILE 2-30171.261A	
S-NUMBER 4013SD	

TELETYPE

4013SD

TC 255 (3-69)

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	SHEET NO.
SHEET INDEX, SUPPORTING INFORMATION	A1	1	2																								A1
FS-1 KEYSWITCHES AND SENSE AMPLIFIERS	B1	1	1																								B1
FS-2 KEYSWITCH AND INTERFACE LOGIC	B2	1	1																								B2
FS-3 CLOCK GENERATION AND DRIVERS	B3	1	2																								B3
FS-4 POWER DISTRIBUTION	B4	1	1																								B4
NOTES	D1	1	1																								D1
TC-1 DATA INTERCHANGE TIMING	E1	1	1																								E1
TC-2 CLOCK TIMING	E2	1	1																								E2
BD-1 CIRCUIT BLOCK DIAGRAM	H1	1	1																								H1

SUPPORTING INFORMATION

CATEGORY	NO.
CONSOLE LOGIC CIRCUIT CARD CC080 CIRCUIT DESCRIPTION	4080CD
CIRCUIT CARD CC080 CONSOLE LOGIC ASSEMBLY DRAWING	410080
LOGIC SYMBOLS, TRUTH TABLES, AND GENERAL NOTES	9100HD

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING:

1. ONLY CHANGED SHEETS WILL BE REISSUED (INCLUDING SHEET 1).
2. UNCHANGED SHEETS RETAIN EXISTING ISSUE NUMBER.

THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDICATES THE LATEST ISSUE PER SHEET.

REVISIONS

ISSUE	DATE	AUTH. NO.
1	6-14-76	24330R
2	2-19-77	16857

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

ENGR. RHF	DSGNR. R.E.G.
DRN.	DATE 2-2-76
R B D FILE	2-30.171.263AA
S-NUMBER	62176

TELETYPE

4080SD-A1

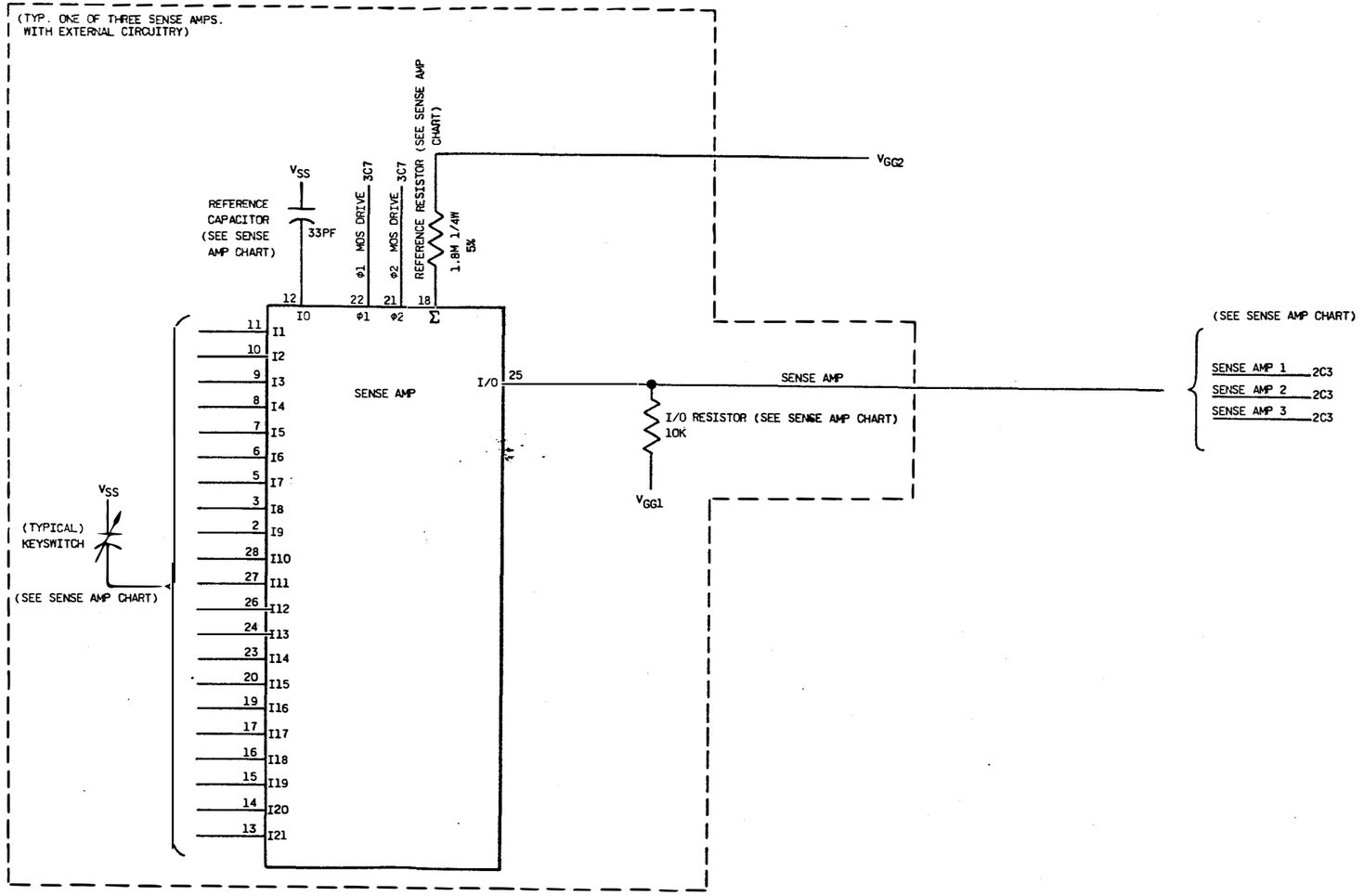
TC 654 (8-71)

FS-1

KEYSWITCHES AND SENSE AMPLIFIERS

SENSE AMP CHART

SENSE AMP PIN NO.	SENSE AMP 1 (MLA6)	SENSE AMP 2 (MLB4)	SENSE AMP 3 (MLA1)
	KEYTOP CHARACTER		
11	SHIFT (RIGHT)	CONTROL	SHIFT (LEFT)
10	/	K	S
9	.	U	2
8	▲	5	Z
7	:	R	Q
6	,	F	A
5	BACK SPACE	SPACE	W
3	L	V	1
2	O	C	X
28	-	B	LO (LOCAL TALK)
27	0 (ZERO)	G	L1 (DATA)
26	P	T	L2 (AUTO. ANSW)
24	+	6	ESCAPE
23	=	N	(CPT. SPARE)
20	RETURN	H	L3 (INTRPT)
19	(	Y	3
17	\	7	E
16	DELETE	M	D
15	LINE FEED	J	4
14	8	9	I
13	◣	REPEAT	CAPS LOCK
18	REFERENCE RESISTOR		
	R27	R30	R6
25	I/O RESISTOR		
	R26	R21	R22
	KEYSWITCH LOGIC (MLA5) INPUT PIN NO.		
	10	11	12
12	REFERENCE CAPACITOR		
	C10	C15	C2



ISSUE 1

CONSOLE LOGIC
CC080

TELETYPE

4080 SD - BI

TC 640-0388

FS-2

KEYSWITCH AND INTERFACE LOGIC

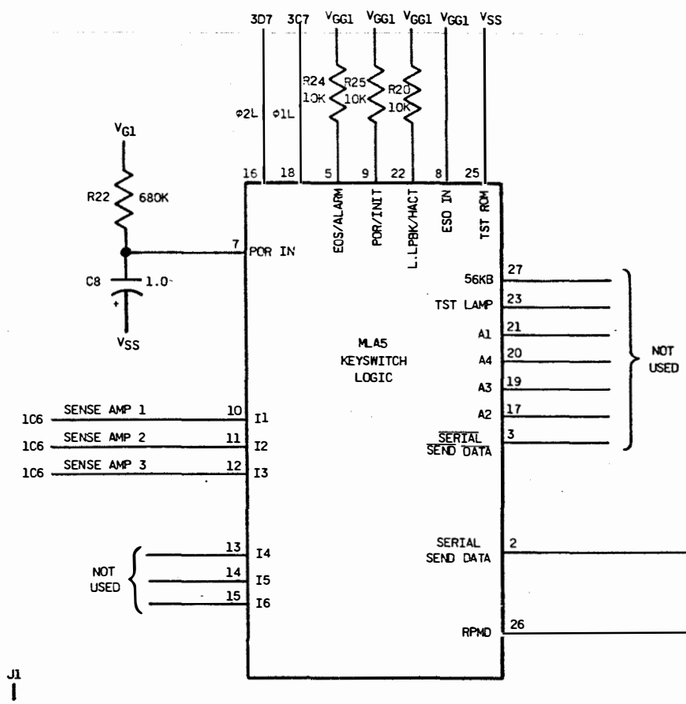
ISSUE 1

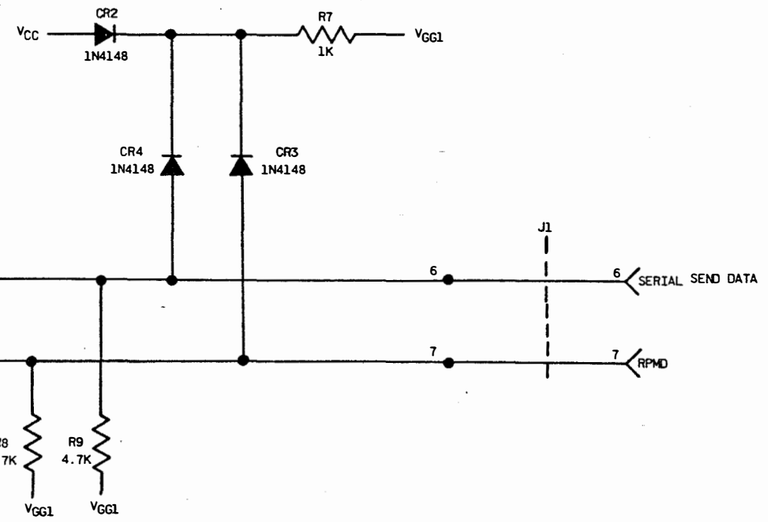
NOTES:

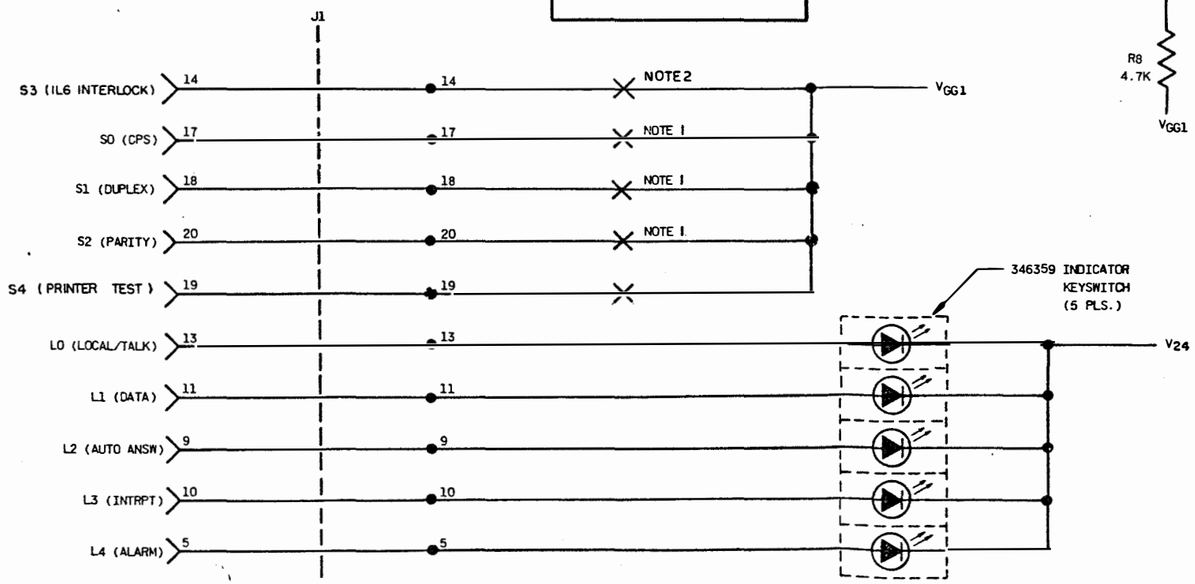
1.

SWITCH KEYTOP	OPEN (UP)	CLOSED (DOWN)
CPS (SC)	30	10
DUPLEX (S1)	HALF	FULL
PARITY (S2)	ON	OFF

2. WHEN THE COVER IS OPEN SWITCH S3 IS UP (OPEN) THIS SIGNAL WILL INHIBIT THE PRINTER FROM RECEIVING DATA. CLOSING THE COVER WILL DEPRESS (CLOSE) THE SWITCH ENABLING THE PRINTER.







CONSOLE LOGIC CC080	TELETYPE 4080SD-B2

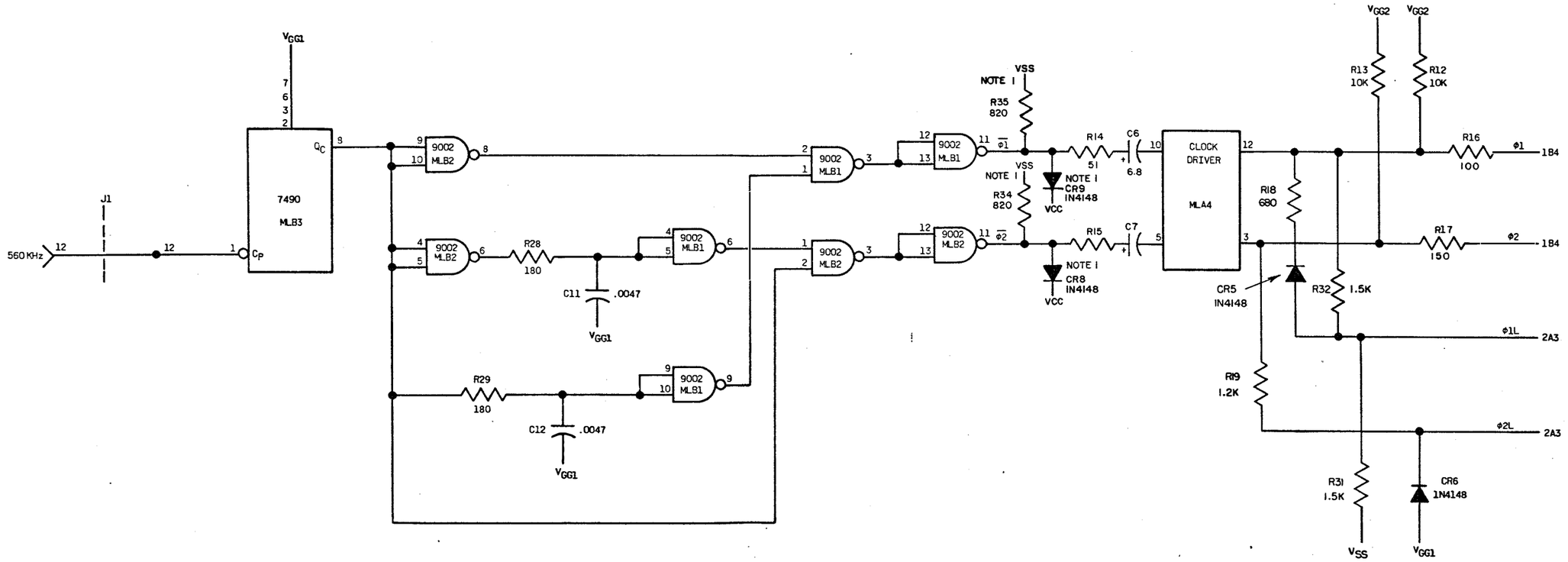
TC 640-0368

NOTE:
1 CR8, CR9, R34 & R35 WHERE ADDED AT CUSTOMER IDENTIFICATION ISSUE 18.

ISSUE
1
2

FS-3

CLOCK GENERATION AND DRIVERS



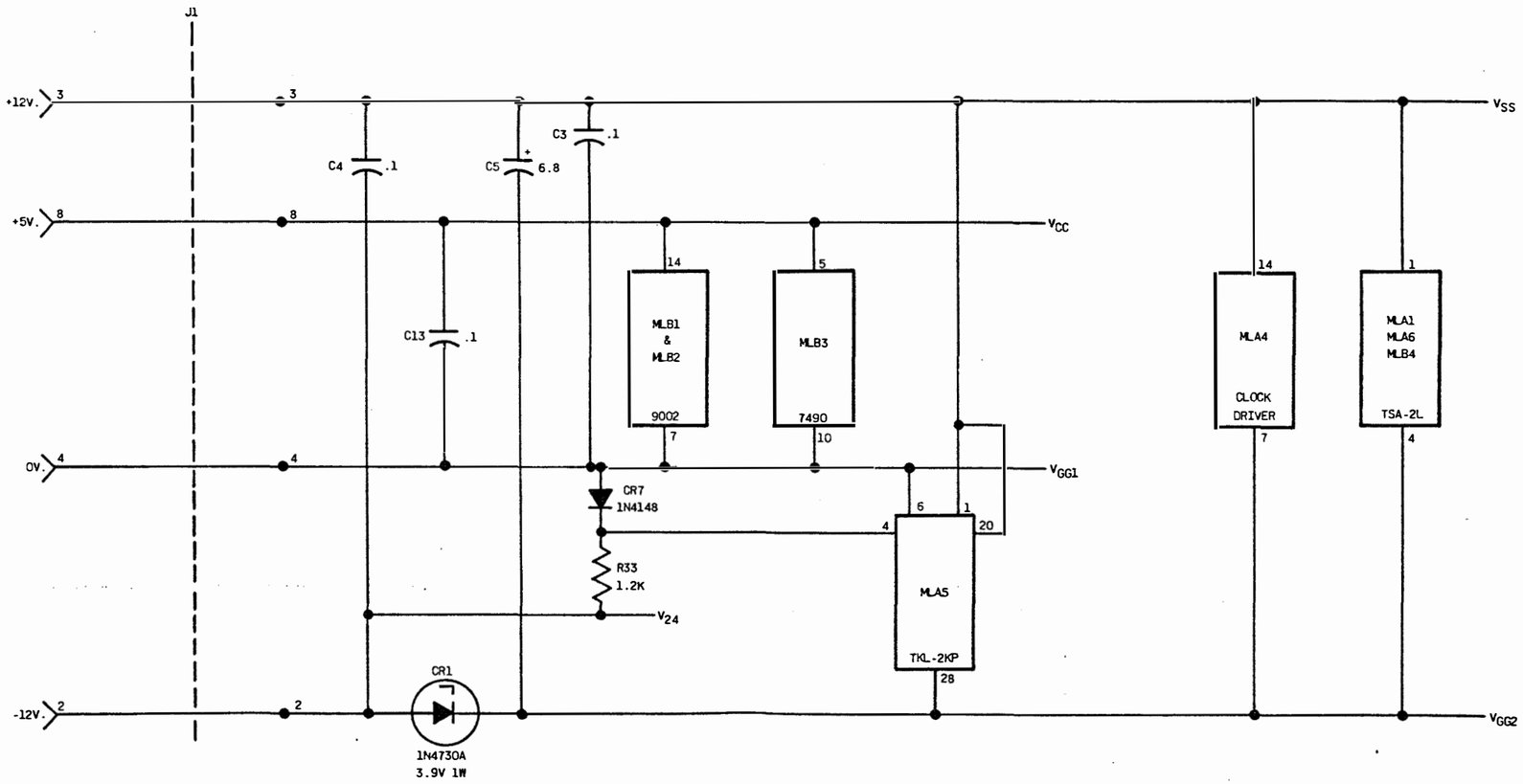
CONSOLE LOGIC CC080	TELETYPE 4080SD-B3

TC 640-0369

ISSUE 1

FS-4

POWER DISTRIBUTION



CONSOLE LOGIC
CC080

TELETYPE

4080SD-B4

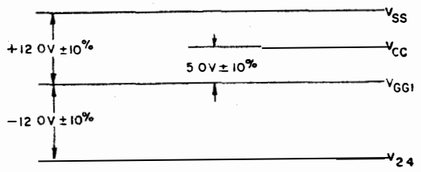
TC 640.0360

NOTES

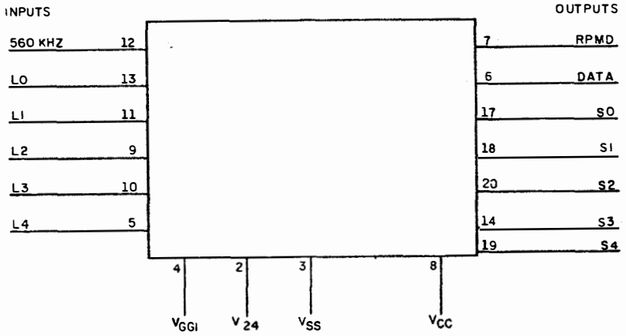
ISSUE 1

CIRCUIT NOTES

101. SUPPLY VOLTAGES:
THE FOLLOWING VOLTAGES ARE MEASURED IN RESPECT TO V_{GG1}.



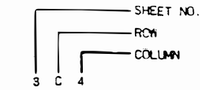
102. SIGNAL VOLTAGES:
THE INPUT VOLTAGE FOR PIN NUMBER 12 SWINGS BETWEEN V_{GG1} AND V_{CC}. THE INPUT VOLTAGES FOR PIN NUMBERS 13,11,9,10,& 5 SWING BETWEEN V_{24} AND V_{24} + 2.0V. THE OUTPUT VOLTAGES FOR PIN NUMBERS 14, 17,18,19 & 20 ALL SWING BETWEEN V_{GG1} AND V_{CC}. THE OUTPUT VOLTAGES FOR PIN NUMBERS 6 AND 7 SWING BETWEEN V_{GG1} AND V_{CC}



EQUIPMENT NOTES

INFORMATION NOTES

301. SHEET COORDINATE LOCATION LEGEND:



* SECTION LETTERS ARE NOT REQUIRED UNLESS REFERENCE IS TO OTHER SECTIONS OF THE DRAWING. WHEN SECTION LETTERS ARE REQUIRED, THE SECOND LETTER SHALL PRECEDE THE SHEET NO., (E.G. B1D4).

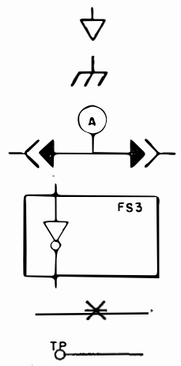
302. TERMINAL DESIGNATIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENTS.

303. ALL RESISTANCE VALUES IN OHMS UNLESS OTHERWISE SPECIFIED.

304. ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SHOWN.

305. ALL CAPACITANCE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

306. SYMBOLS:



SIGNAL GROUND

FRAME OR CHASIS GROUND

LETTER OR TITLE IN CIRCLE INDICATES PRESENCE OF AN OPTION WHICH THE CUSTOMER CAN ARRANGE TO SUIT HIS CHOICE OR REQUIREMENT WITHIN THE POSSIBILITIES SHOWN.

CIRCUITRY WITHIN SINGLE SOLID LINE ENCLOSURE IS SHOWN FOR REFERENCE ONLY. IT IS SHOWN IN DETAIL ELSEWHERE IN THE SAME SD.

NORMALLY OPEN CONTACT

TP — TEST POINT

307. ABBREVIATIONS:

DE - DATA ENABLE	I - INPUT	RPMD - REPEAT MODE
DEP - DEPRESSION	Σ - SUMMATION	R_{REF} - REFERENCE RESISTOR
MR - MASTER RESET	POR - POWER ON RESET	
EOS - END OF SCAN	KL - KEYSWITCH LOGIC	
I/O - INPUT/OUTPUT	C_{REF} - REFERENCE CAPACITOR	

CONSOLE LOGIC
CC080

TELETYPE

4080SD-D1

TC 640-0368

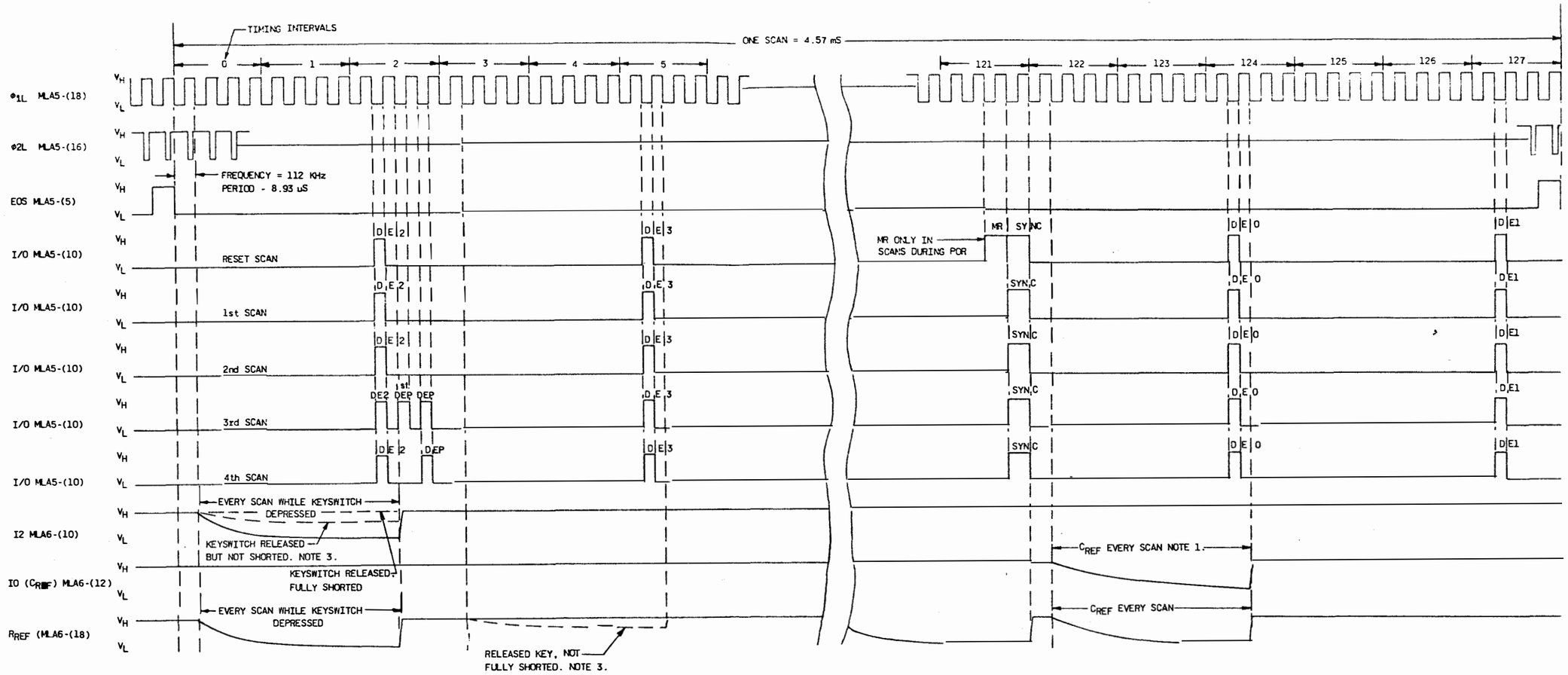
NOTES:

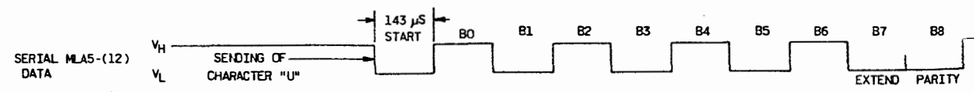
1. FIRST DEPRESSION AND DEPRESSION DO NOT EXIST FOR INPUT I_0 (C_{REF}).
2. SEE SHEET 01 FOR MEANING OF ABBREVIATIONS.
3. THE NOT FULLY SHORTED CONDITION IS USUAL FOR THE CAPACITATIVE KEYSAITCHES.

TC-1
DATA INTERCHANGE TIMING

(FS-1, FS-2)
(4080SD-B1, B2)

ISSUE 1





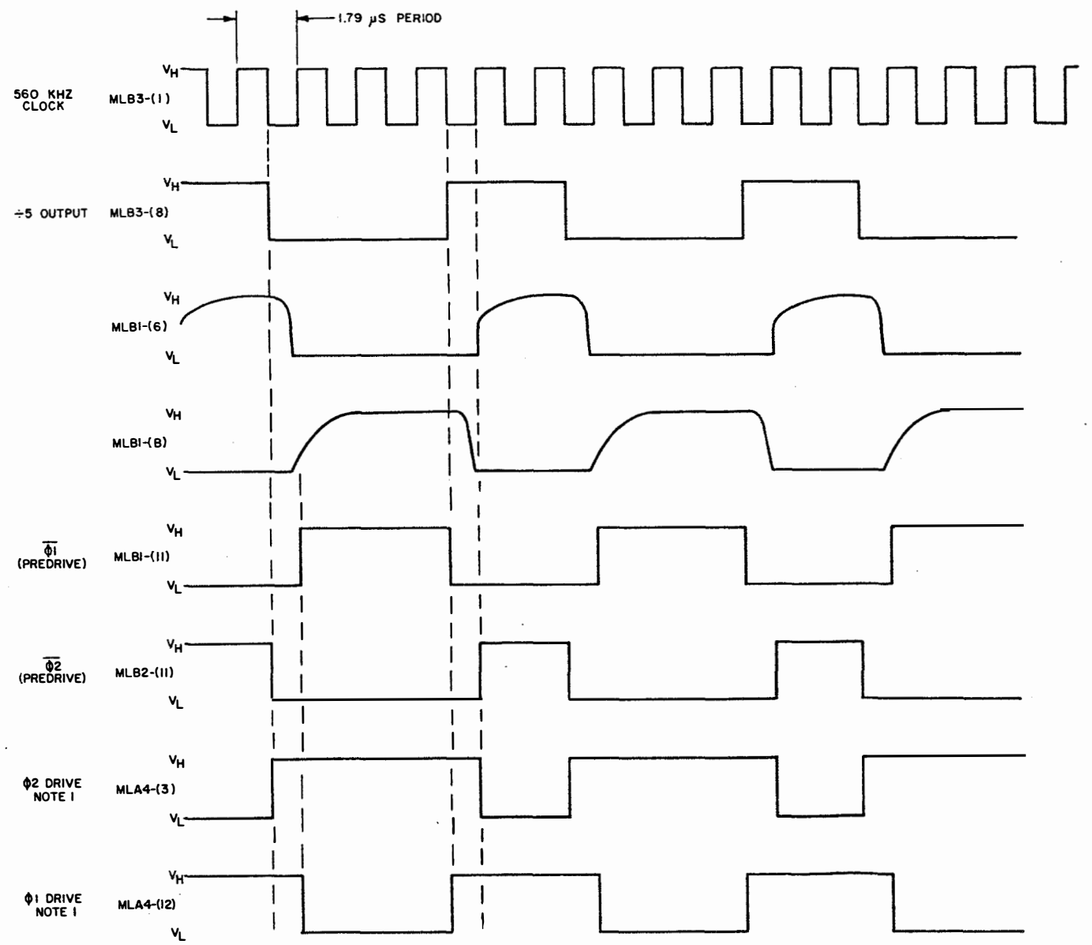
CONSOLE LOGIC CC080	TELETYPE 4080SD-E1

TC 640-0369

ISSUE 1

TC-2
CLOCK TIMING

(FS-3)
(4080SD-83)



NOTE 1. φ1 AND φ1L, φ2 AND φ2L HAVE THE SAME TIMING AND LOGIC SENSE, BUT DIFFERENT VALUES OF V_L.

CONSOLE LOGIC
CC080

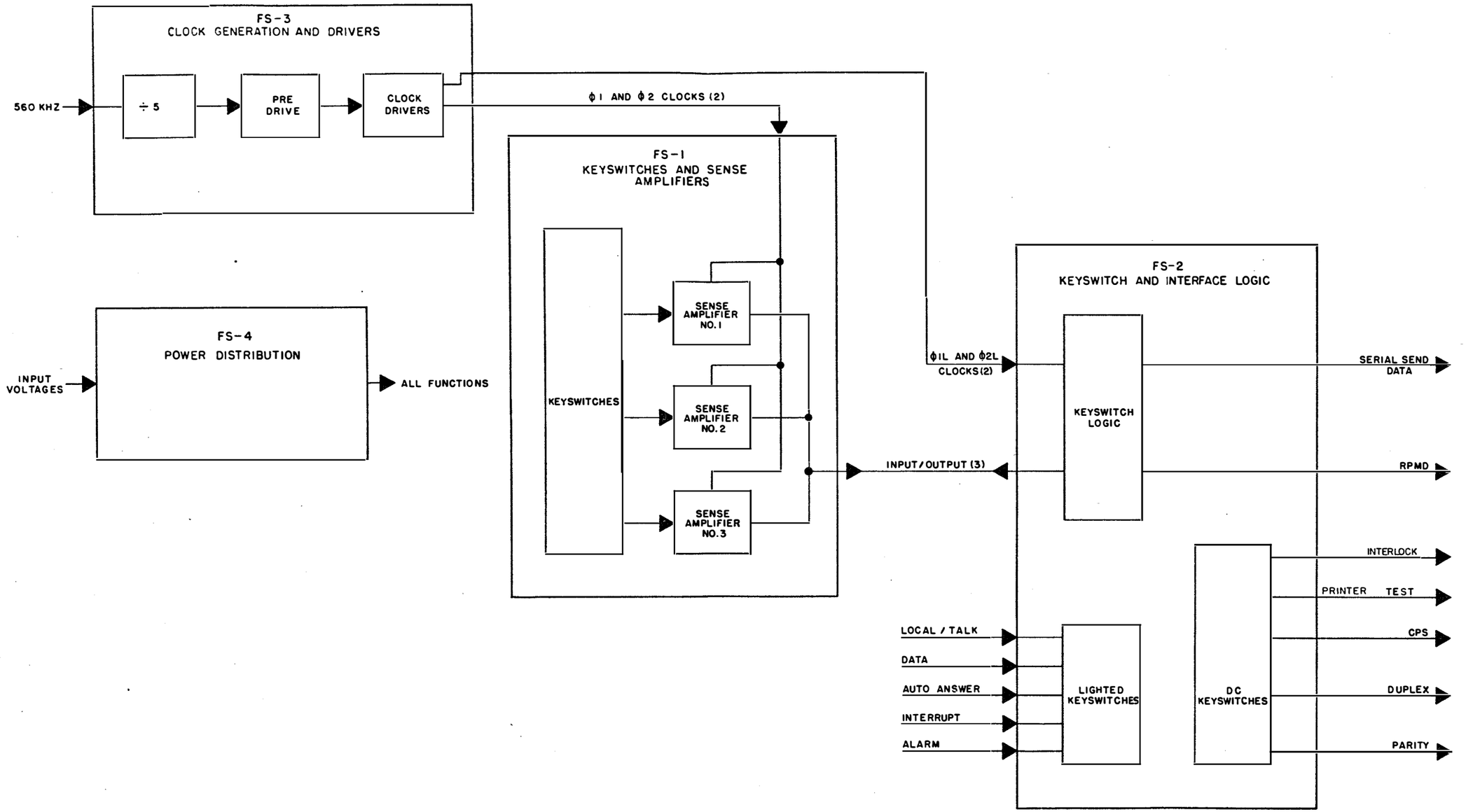
TELETYPE

4080SD-E2

TC 640-0368

ISSUE 1

BD-1
CIRCUIT BLOCK DIAGRAM



CONSOLE LOGIC CC080	TELETYPE
	4080SD-H1

TC 640-0369

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4	5	6	7	9	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	SHEET NO.
SHEET INDEX SUPPORTING INFORMATION	A1	1	2	3	4	5	6																							A1
FS-1 AC-DC CIRCUIT	B1	1	1	1	1	1	1																							B1
FS-2 DC-DC CONVERTER (PRIMARY)	B2	1	2	3	4	4	4																							B2
FS-3 DC-DC CONVERTER (SECONDARY)	B3	1	1	2	3	3	3																							B3
FS-4 OSCILLATOR & CONTROL CIRCUIT	B4	1	1	2	2	3	4																							B4
CIRCUIT NOTES EQUIPMENT NOTES INFORMATION NOTES	D1	1	1	1	1	1	1																							D1
VOLTAGE-CURRENT WAVE FORMS	E1	1	1	1	1	1	1																							E1
VOLTAGE-CURRENT WAVE FORMS	E2	1	1	1	1	2	2																							E2
FS BLOCK DIAGRAM	H1	1	1	1	1	1	1																							H1

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT DESCRIPTION FOR 430700 POWER SUPPLY	470000
ACTUAL WIRING DIAGRAM FOR 430550 REAR FRAME ASSEMBLY	96124A0

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND UPDATED EACH TIME ANY SHEET OF THE DRAWING IS REISSUED OR A NEW SHEET IS ADDED.
3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.

REVISIONS

ISSUE	DATE	AUTH. NO.
1	9-3-75	245939
2	9-10-76	16674
3	10-5-76	16838
4	11-24-76	16898
5	2-2-77	17109
6	8-4-77	18566

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

ENGR. DLS	DSGNR.
DRN.	DATE
R&D FILE	1-30.171.2114
S-NUMBER	

TELETYPE

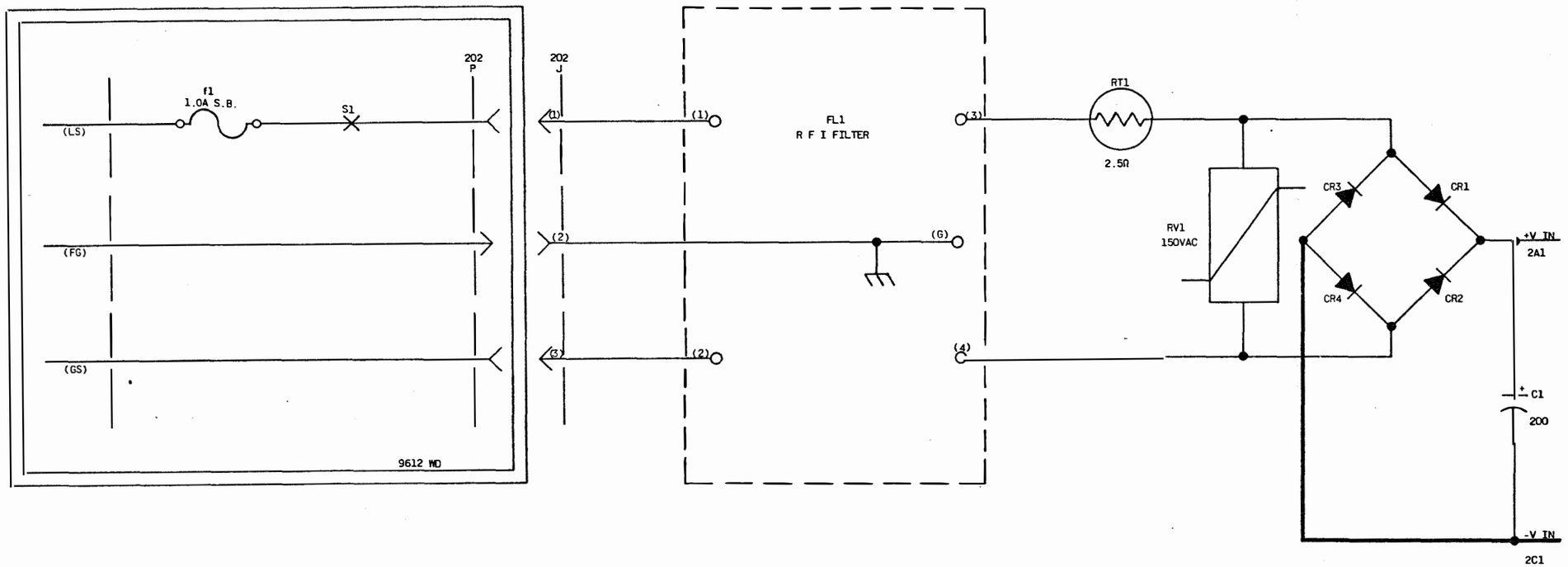
4700 SD-A1

TC 641 (3-69)

ISSUE 1

FS-1

AC - DC CIRCUIT

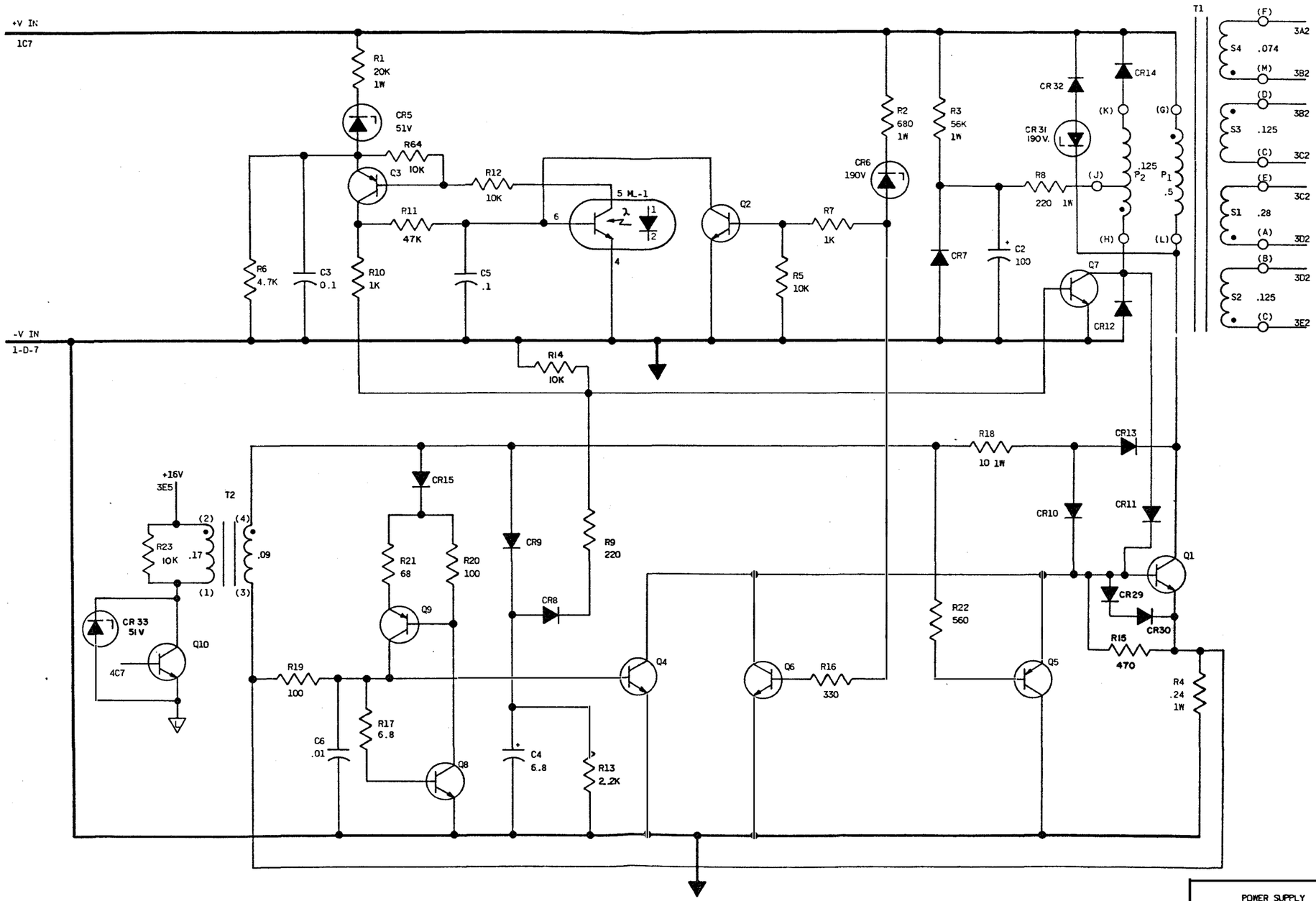


POWER SUPPLY 410700	TELETYPE 4700 SD-B1

TC 640-0369

ISSUE
1
2
3
4

FS-2
DC-DC CONVERTER
(PRIMARY CIRCUIT)

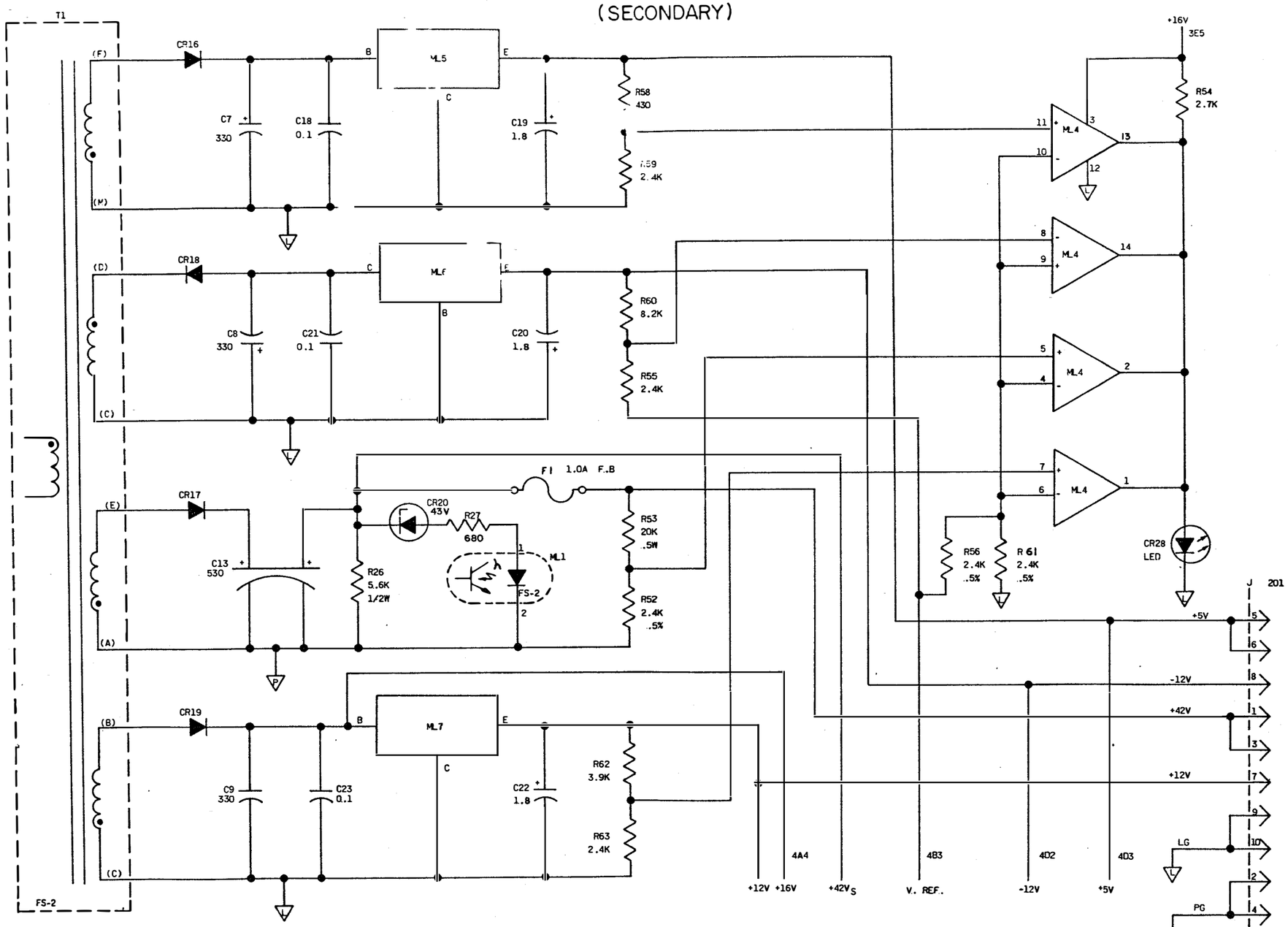


POWER SUPPLY 410700	TELETYPE 4700 SD-B2

TC 640-0369

FS-3
DC-DC CONVERTER
(SECONDARY)

ISSUE
1
2
3



POWER SUPPLY
410700

TELETYPE

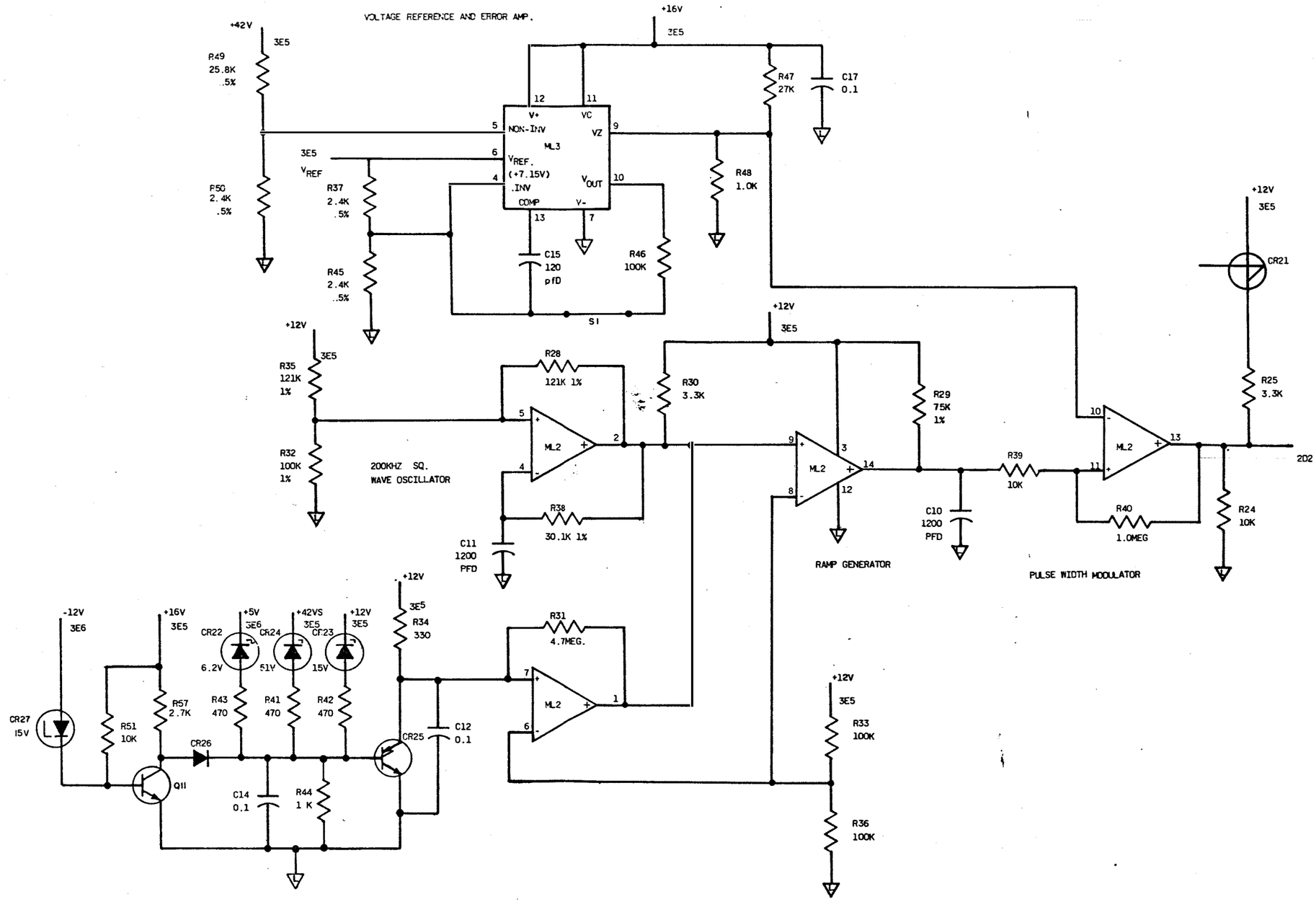
4700 SD-B3

TC 640-0369

FS-4

OSCILLATOR & CONTROL CIRCUIT

ISSUE
1
2
3
4



POWER SUPPLY 410700	TELETYPE 4700 SD B4

TC 640-0369

101 CIRCUIT NOTES

DESIG.	FUSE	POTENTIAL
F201	1.0 FB	42VDC

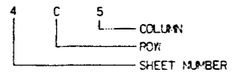
BATTERY SYMBOL	VOLTAGE RANGE
VREF	6.80 TO 7.50
+16V DC	15.4 TO 19.5
-16 DC	-15.4 TO -19.5
+9V DC	8.2 TO 10.4
+5V DC	4.6 TO 5.4
+12V DC	11.1 TO 12.8
-12V DC	-11.1 TO 12.8
+42V DC	39 TO 45
115V AC	103 TO 127

EQUIPMENT NOTES

1. THE PROTECTIVE GROUND IS NOT CONNECTED TO THE PRIMARY CIRCUIT GROUND. CARE MUST BE EXERCISED TO PREVENT DIRECT CONNECTION OF THESE GROUNDS UNLESS THE POWER SUPPLY IS PLUGGED INTO AN ISOLATION TRANSFORMER. DIRECT CONNECTION OF THESE GROUNDS WITHOUT ISOLATION WILL CAUSE COMPONENTS TO FAIL.

INFORMATION NOTES

301. SHEET COORDINATE LOCATION LEGEND



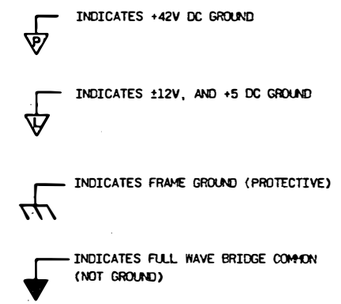
302. TERMINALS DESIGNATION ENCLOSED IN PARENTHESIS ARE NOT MARKED ON THE COMPONENT.

303. ALL RESISTORS ARE 1/4 W, ±5% AND ALL IN OHMS UNLESS OTHERWISE SPECIFIED.

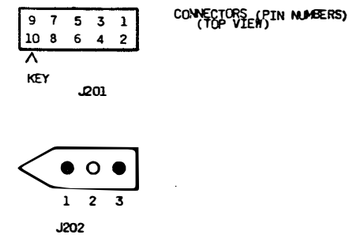
304. ALL CAPACITORS VALUES IN MICRO FARADS UNLESS OTHERWISE SPECIFIED

305. TRANSFORMER WINDINGS DC RESISTANCE INDICATED IN OHMS.

306.



307.



ISSUE
1

POWER SUPPLY
410700

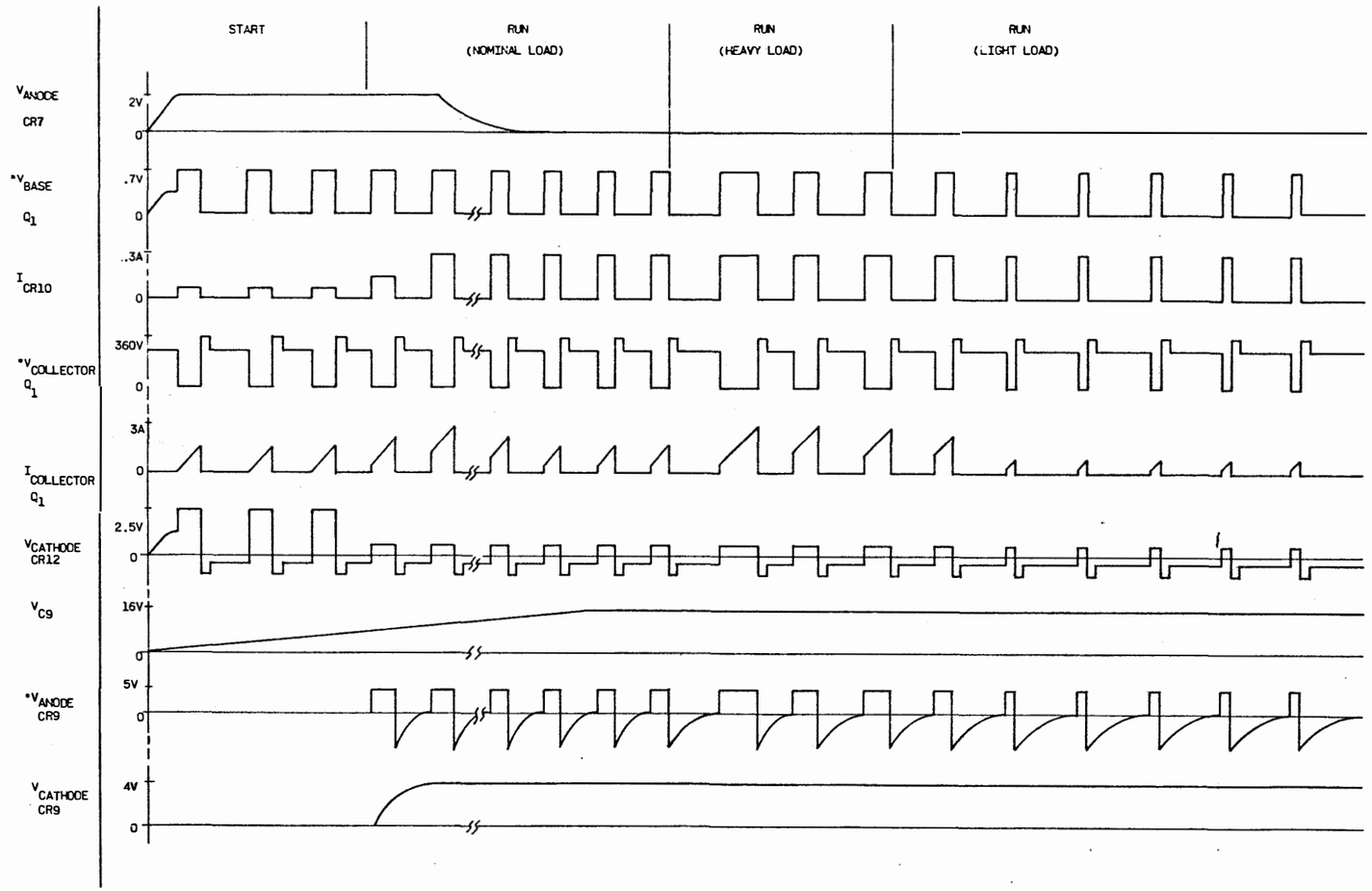
TELETYPE

4700 SD-D1

TC 640-0388

ISSUE
1

TC-1
VOLTAGE-CURRENT WAVEFORMS



NOTE:
WAVE FORMS MEASURED WITH POWER SUPPLY PLUGGED INTO AN ISOLATION TRANSFORMER AND ($-V_{IN}$) TIED TO PROTECTIVE GROUND. ALL VOLTAGES MEASURED WITH RESPECT TO PROTECTIVE GROUND UNLESS OTHERWISE NOTED.

* WAVE FORMS MEASURE WITH RESPECT TO EMITTER ON Q_1.

POWER SUPPLY 410700	TELETYPE 4700SD-E1

TC 640-0348

ISSUE
1
2

TC-2

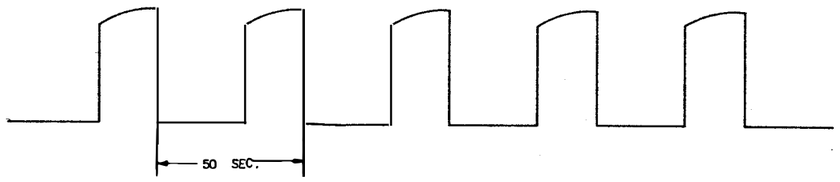
VOLTAGE - CURRENT WAVEFORMS

OSCILLATOR DRIVEN MODE

20 KHZ SQUARE WAVE
OSCILLATOR ML2-2

+12V

0V



RAMP GENERATOR
ML2-14

+ 3.5V

0V

CONTROL VOLTAGE
ML3-9

+ 5V

0V

PULSE WIDTH MODULATOR
ML2-13

+ 1.0V

0V

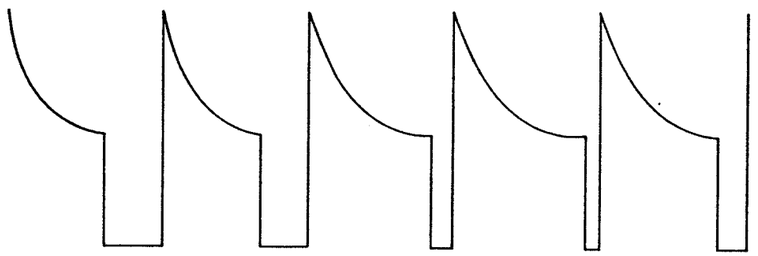
PULSE TRANSFORMER DRIVE
Q10-COLLECTOR

+30V

+20V

+10V

0V



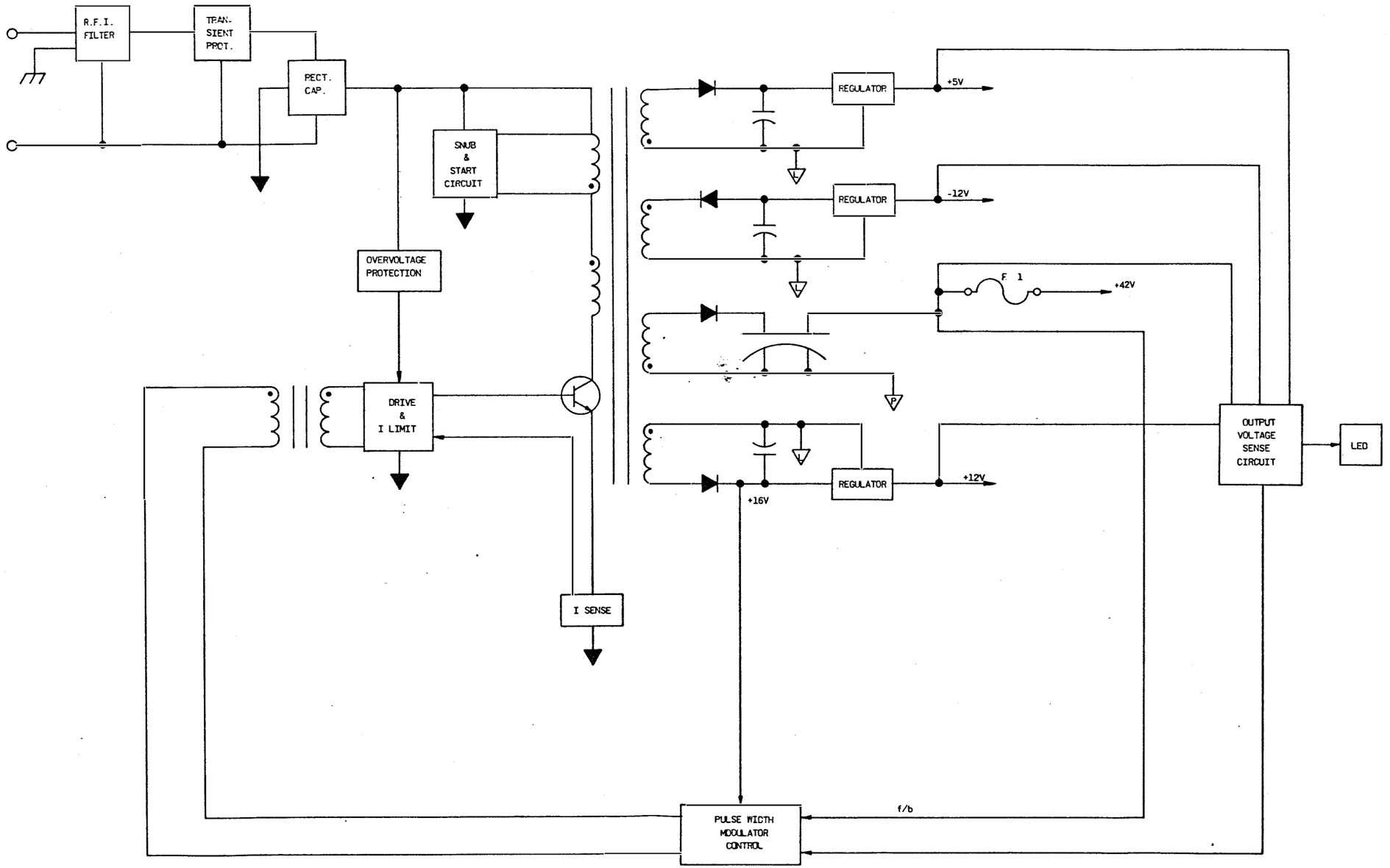
POWER SUPPLY 410700	TELETYPE 4700 SD E2

TC 640-0369

ISSUE 1

BD-1

FS BLOCK DIAGRAM



POWER SUPPLY
410700

TELETYPE

4700 SD-HI

TC 640-0388

SHEET INDEX

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FS-2 PRINTER TIMING LOGIC	4	1	1	1	2	2	2																							4
FS-3 PRINT HEAD AND BELL DRIVERS	5	1	1	.	1	1	1																							5
FS-4 CARRIAGE MOTOR AND LINEFEED MOTOP DRIVERS	6	1	1	1	1	1	1																							6
FS-5 VOLTAGE DISTRIBUTION	7	1	2	3	4	4	4																							7
TC-1 TERMINAL CONTROLLER TIMING	8	1	1	1	1	1	1																							8
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SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT DESCRIPTION	4740CD
SCHEMATIC DIAGRAM	4013SD
CIRCUIT DESCRIPTION	4080CD
SCHEMATIC DIAGRAM	4080SD

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND UPDATED EACH TIME ANY SHEET OF THE DRAWING IS REISSUED OR A NEW SHEET IS ADDED.
3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.

REVISIONS

ISSUE	DATE	AUTH. NO.
1	8-2-76	24598R
2	9-28-76	16673
3	11-5-76	16429 1
4	6-15-77	18619
5	10-25-77	18760
6	11-7-77	18952

M43 LOGIC CARD
(BASIC KSR)
410740 (CC740)

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

ENGR. YCK	DSGNR.
DRN.	DATE
R&D FILE	1-30.171.234A
S-NUMBER	

TELETYPE

4740SD-1

TC 641 (3-69)

ISSUE
1
2
3

CIRCUIT NOTES:

101. VOLTAGE

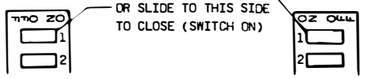
VOLTAGE	VOLTAGE RANGE
+42V	+37.8 TO +46.2
+12V	+10.8 TO +13.2
+5V	+4.5 TO +5.5
-4V	-3.4 TO -4.6
-5V	-4.5 TO -5.5
-12V	-10.8 TO -13.2

102. INTEGRATED CIRCUIT BATTERY CONNECTIONS:

TYPE	DESIG.	+5V	LOGIC GND	-4V	-5V	-12V	
TTL	339109 (74109)	16	8				
TTL	339417 (7417)	14	7				
TTL	474004 (74LS04)	14	7				
DTL	339380 (380)	8	1				*ISSUE 2A OR LATER
LINEAR	404324 (324)	4			11		
CMOS	404050 (4050)	1		8			
MOS	430601 (MAPL)	1	20		40		
MOS	430651 (MACON)	1,33	40		20	21	
* MOS	430641 (MAPL)	1			40	21	
* MOS	430671 (MACON)	1,33			20	21	

103. SWITCH OPTIONS:

OFF = SWITCH OPEN
ON = CLOSED



DESIGNATION		FUNCTION	SWITCH STATE (TO ENABLE FUNCTION)
	SW1	AUTOMATIC NEW LINE	OFF
	SW2	PRINTER TEST	ON
	SW3	VERTICAL PARITY SEND	OFF
	SW4	EDT DISCONNECT	OFF
SPD4	SW5, SW6	LINE LENGTH	
	SW7, SW8	CHARACTER FONT SELECT	

	SW5	SW6
UNUSED	OFF	OFF
72 COLUMNS	OFF	ON
80 COLUMNS	ON	OFF
132 COLUMNS	ON	ON

	SW7	SW8
NU FONT	OFF	OFF
UNDEFINED	OFF	ON
ME FONT	ON	OFF
TV FONT	ON	ON

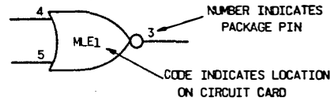
INFORMATION NOTES:

201. ALL RESISTORS 1/4 WATT AND RESISTANCE VALUE IN OHMS, UNLESS SPECIFIED. ALL COIL RESISTANCES IN OHMS.

202. ALL CAPACITOR VALUES IN MICROFARADS, UNLESS SPECIFIED.

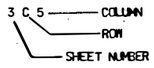
203. ——< INDICATES FEMALE TERMINAL
——> INDICATES MALE TERMINAL

204. LOGIC DESIGNATION

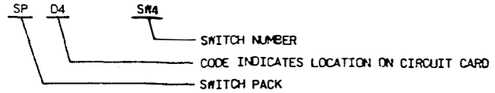


205. POSITIVE LOGIC SYMBOLS ARE EMPLOYED

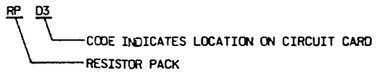
206. CROSS REFERENCE DESIGNATION



207. SWITCH PACK DESIGNATION



208. RESISTOR PACK DESIGNATION



209. OFF-BOARD SWITCHES

SWITCH FUNCTION	OPEN POSITION INDICATION
PAPER OUT	NO PAPER IN MACHINE
LOW PAPER	LOW PAPER ROLL (FRICTION FEED ONLY)
LEFT HAND MARGIN	CARRIAGE AGAINST LEFT SIDE FRAME

210. GROUND DESIGNATION

L ——— LOGIC GROUND (+12V, +5V, -4V, -5V, -12V RETURNS)

P ——— POWER GROUND (+42V RETURN)

THESE GROUNDS SHOULD BE CONNECTED AT THE POWER SOURCE AND NOT ON THE 410740 CARD.

211. ALL TRANSISTORS REFERENCING THIS NOTE REQUIRE HEATSINK (PN 430612)

212. CONNECTOR INFORMATION

CONN.	PIN NO.	DESIGNATION	FS	LOCATION
P1	1	DIGITAL LOOP	FS-1	3C7
	3	ANALOG LOOP	FS-1	3D7
	5	TERMINAL READY	FS-1	3D7
	7	+5V	FS-5	7C7
	6, 9	REQUEST TO SEND / LOGIC GROUND	FS-1 / FS-5	3E7 / 7B7
	11	-12V	FS-5	7C7
	13	+12V	FS-5	7C7
	14	DUPLEX	FS-1	3E7
	15	TAU / TDU READY	FS-1	3C7
	17	RECEIVE DATA	FS-1	3C7
	19	SEND DATA	FS-1	3B7
J101	1	LOW PAPER	FS-1	3D2
	2, 3	KEY POSITION	NOT SHOWN	
	4	PAPER OUT	FS-1	3D2
	5, 6	LOGIC GROUND	FS-1	3D2
J102	1	LINE FEED MOTOR PHASE 4	FS-4	6A4
	2, 8	+42V (FUSED)	FS-4	6E3
	3	LINE FEED MOTOR PHASE 3	FS-4	6B4
	5	LINE FEED MOTOR PHASE 2	FS-4	6C4
	7	LINE FEED MOTOR PHASE 1	FS-4	6D4
J103	1	OPTICAL SW. PHOTO TRANSISTOR EMITTER	FS-2	4B2
	2	OPTICAL SWITCH LED CATHODE	FS-2	4A2
	3	OPTICAL SWITCH LED ANODE	FS-2	4A2
	4, 5	KEY POSITION	NOT SHOWN	
	6	+5V	FS-2	4A2
J104	1	CARRIAGE MOTOR PHASE 3	FS-4	6C7
	2	CARRIAGE MOTOR PHASE 2	FS-4	6B7
	3	CARRIAGE MOTOR PHASE 4	FS-4	6D7
	4	CARRIAGE MOTOR PHASE 1	FS-4	6A7
	5	+42V	FS-4	6E7
	6	KEY POSITION	NOT SHOWN	

212 CONT'D

CONN.	PIN NO.	DESIGNATION	FS	LOCATION
J105	1	PRINT LEVEL 1	FS-3	5B4
	2	PRINT LEVEL 2	FS-3	5C4
	3	PRINT LEVEL 3	FS-3	5C4
	4	PRINT LEVEL 4	FS-3	5C4
	5	PRINT LEVEL 5	FS-3	5A7
	6	PRINT LEVEL 6	FS-3	5B7
	7	PRINT LEVEL 7	FS-3	5C7
	8	PRINT LEVEL 8	FS-3	5C7
	9	PRINT LEVEL 9	FS-3	5D7
	10, 11, 12, 13	+42V	FS-3	5E7, 5E3
	15	LOGIC GROUND	FS-2	4C4
	16	LEFT HAND MARGIN	FS-2	4D4
J106	1	BELL COIL	FS-3	5A3
	2	+42V	FS-3	5A3
J107	1	KEY POSITION	NOT SHOWN	
	2	-12V	FS-5	7D7
	3	+12V	FS-5	7D7
	4	LOGIC GROUND	FS-5	7D7
	5	ALARM	FS-1	3B1
	6	KEYBOARD SEND DATA	FS-1	3D2
	7	REPEAT MODE	FS-1	3E2
	8	+5V	FS-5	7D7
	9	AUTO ANSWER	FS-1	3B1
	10	INTERRUPT	FS-1	3B1
	11	DATA	FS-1	3B1
	12	CLOCK	FS-1	3E2
	13	LOCAL / TALK	FS-1	3B1
	14	INTERLOCK	FS-1	3C1
	16	KEY POSITION	NOT SHOWN	
	17	CHARACTERS PER SECOND	FS-1	3C1
	18	DUPLEX	FS-1	3C1
	19	SELF TEST	FS-1	3B1
	20	PARITY	FS-1	3D1
P201	1, 3	+42V	FS-5	7D2
	2, 4	POWER GROUND	FS-5	7D2
	5, 6	+5V	FS-5	7C2
	7	+12V	FS-5	7C2
	8	-12V	FS-5	7C2
	9, 10	LOGIC GROUND	FS-5	7B2

M43 LOGIC CARD
(BASIC KSR)
410740 (CC740)

TELETYPE

4740 SD 2

TC 640-0388

FS-1 TERMINAL CONTROLLER

ISSUE
1
2
3

+5V 14 — RPD3 6.8K — 5 7 4 3 6

SPD4 SW2 2 15

7A7 V_{DD} (8) SEE NOTE 1a SHEET 7

40 V_{DD}

4080SD -12V

J107

9	R41 1K .5W	AUTO ANSW.	38	ANS
10	R40 1K .5W	INTRPT	37	INT
5	R39 1K .5W	ALARM	36	ALM
11	R38 1K .5W	DATA	35	DAT
13	R37 1K .5W	LOCAL / TALK	34	TLK
19	MLE3 3 4	SELF TEST	24	TST
18	MLE3 13 12	DUPLEX	31	DX
14	MLE3 11 10	INTERLOCK	27	ILS
17	MLE3 1 2	CHARACTERS PER SECOND	25	SPD
20	MLE3 5 6	PARITY	8	PAR

P101 — J101

1	MLB4 5 6	LOW PAPER	28	LP
4	MLB4 3 4	PAPER OUT	22	PO

J107

6	R42 1K	KEYBOARD SEND DATA	32	KSD
7	R43 1K	REPEAT MODE	29	RPT
12	CLOCK		2	CLK

6.8K R14 — 6.8K R13 — +5V

4D5

C14 470 pF — C15 470 pF

MLC4

RHM	19	RIGHT HAND MARGIN	4C5
RNC	18	REQUEST NEXT CHAR.	4C5
DQ	17	DATA BIT 0	4C5
D1	16	DATA BIT 1	4C5
D2	15	DATA BIT 2	4C5
D3	14	DATA BIT 3	4C5
D4	13	DATA BIT 4	4C5
D5	12	DATA BIT 5	4B5
D6	11	DATA BIT 6	4B5
D7	10	DATA BIT 7	4B5
LDP	9	LOAD DATA PRINTER	4C5
SD	39		
RD	7		
DR	6		
DL	5		
AL	4		
TR	3		

EOT	30	SW4 4 13	
VPS	26	SW3 3 14	
ANL	23	SW1 16	

12 13 1 — 6.8K RPD3 — 14 +5V — SPD4

P301

SEND DATA	MLB5 13 12	19	19	
RECEIVE DATE	MLB5 6 5	17	17	
TAU / TDU READY	MLB5 4 3	15	15	
DIGITAL LOOP	MLB5 1 2	1	1	
ANALOG LOOP	MLB5 9 8	3	3	
TERMINAL READY	MLB5 11 10	5	5	
DUPLEX	MLB4 1 2	14	14	
REQUEST TO SEND			6	

M43 LOGIC CARD
(BASIC KSR)
410740 (CC740)

TELETYPE

4740SD-3

TC 640-0368

FS-2 PRINTER TIMING LOGIC

ISSUE
1
2

P103 / J103
6 +5V
3 R7 220 → 7 MLA8 (+5, -6) → 100K R1
2 -5V
.01 C1
1 R6 100K
OPTICAL SWITCH 430097 PART OF 430047 ASSEMBLY

-5V R5 12K → 9 MLA8 (10, 8) ← +5V 2.4K R4
C2 22pf
R3 180K
R2 2.4K

RPD3 6.8K (14 → +5V; 11 10 9 8)
SW8 SW7 SW6 SW5 (9 10 11 12; 8 7 6 5)
SPD4

7A7 V_{DD} (B) SEE NOTE 1& SHEET 7
20 V_{DD}

MLC 7

	DATA BIT 7	6	D7	PH0	39 PRINT LEVEL 1
	DATA BIT 6	7	D6	PH1	38 PRINT LEVEL 2
	DATA BIT 5	8	D5	PH2	37 PRINT LEVEL 3
	DATA BIT 4	9	D4	PH3	36 PRINT LEVEL 4
	DATA BIT 3	10	D3	PH4	35 PRINT LEVEL 5
	DATA BIT 2	11	D2	PH5	34 PRINT LEVEL 6
	DATA BIT 1	12	D1	PH6	33 PRINT LEVEL 7
	DATA BIT 0	13	D0	PH7	32 PRINT LEVEL 8
	LOAD DATA PRINTER	14	LDP	PH8	31 PRINT LEVEL 9
	REQUEST NEXT CHAR.	15	RNC	BEL	30 BELL
	RIGHT HAND MARGIN	16	RHM	LM1	29 LINE FEED MOTOR PHASE 1
	LEFT HAND MARGIN	17	LHM	LM2	28 LINE FEED MOTOR PHASE 2
	VELOCITY ENCODER	18	VEN	LM3	27 LINE FEED MOTOR PHASE 3
	CLOCK	19	CLK	LM4	26 LINE FEED MOTOR PHASE 4
				CM1	25 CARRIAGE MOTOR PHASE 1
				CM2	24 CARRIAGE MOTOR PHASE 2
				CM3	23 CARRIAGE MOTOR PHASE 3
				CM4	22 CARRIAGE MOTOR PHASE 4
				CSW	21 CLAMP SWITCH

3C5	5B1
3C5	5C1
3B5	5D1
3B5	5D1
3B5	5A4
3B5	5B4
3B5	5C4
3B5	5D4
3B5	5D4
3C5	5A1
3B5	6D1
3B5	6C1
3B5	6B1
3B5	6A1
3B5	6A5
3B5	6B5
3B5	6C5
3B5	6D5
3C5	6E1

PART OF PRINT HEAD ASSEMBLY 4013 SD
J105 15 16
+5V R12 6.8K
MLB4 (9 → 8)

R46 2.7K
MLE1 MLE1 MLE1 MLE1 (9 10 14; 6 7 2; 12 11 13; 4 5 3)
C18 .01
R45 10K
R44 10K
C19 33pf
1.12 MHZ XTAL
+5V 10K R47
± C20 22

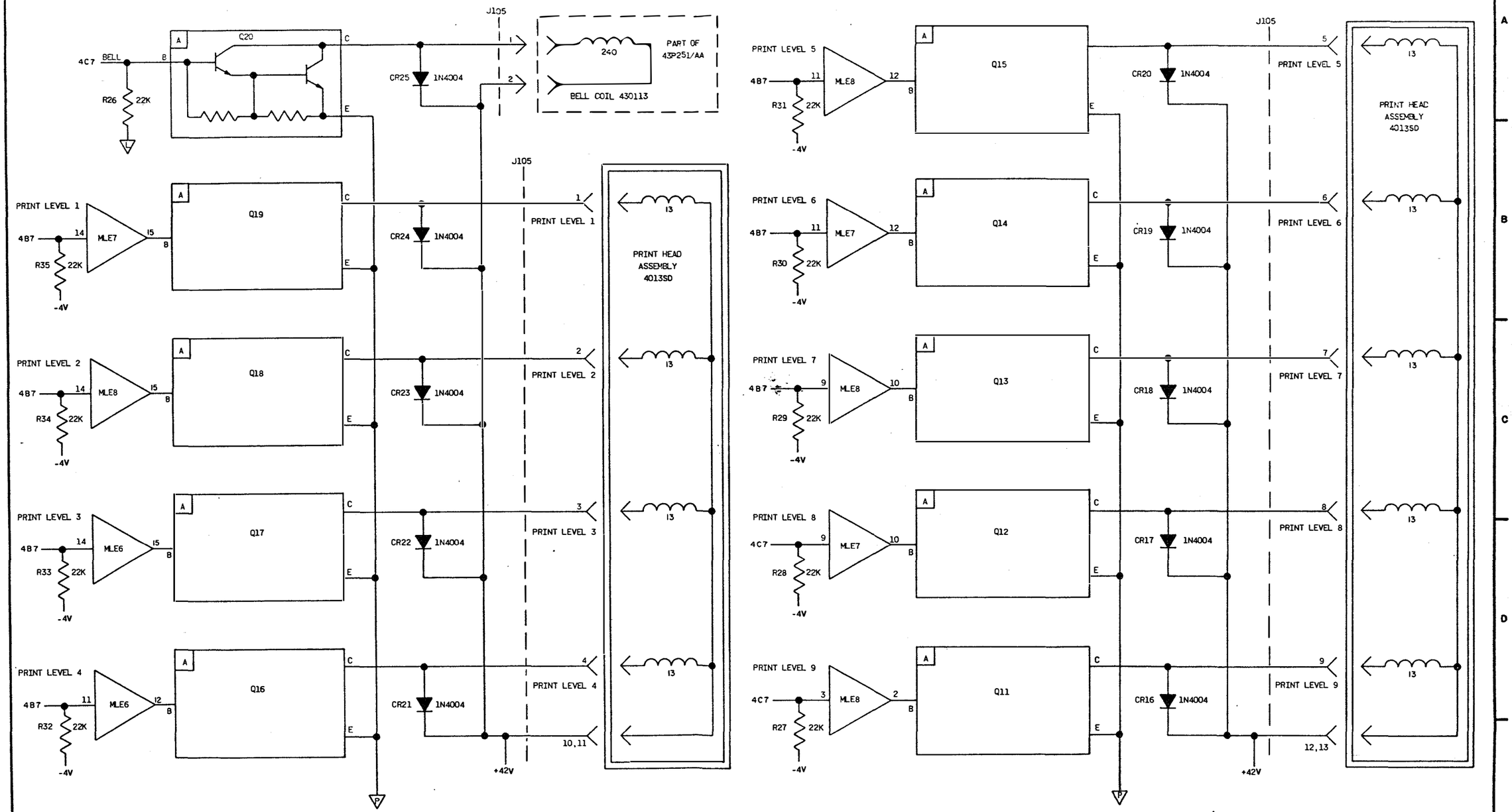
MLD2 (PR 11, Q 10, CLK 12, CLR 15)
MLD2 (PR 5, Q 6, J 2, CLK 4, K 3, CLR 1)
+5V
3E3
470 R36 +5V

M43 LOGIC CARD (BASIC KSR) 410740 (CC740)	TELETYPE	4740SD4	

TC 14-0369

FS-3 PRINT HEAD AND BELL DRIVERS

ISSUE 1

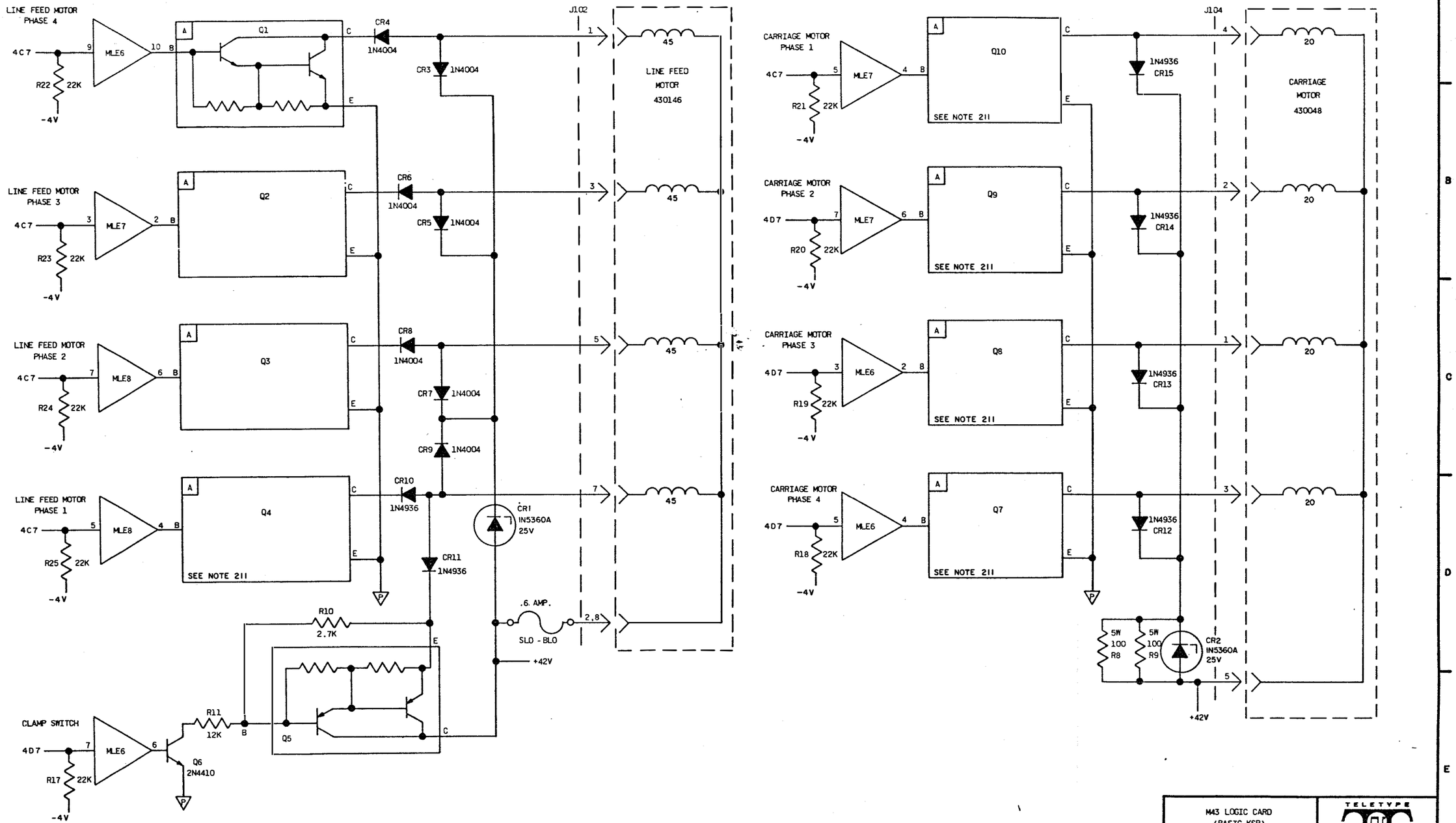


M43 LOGIC CARD (BASIC KSR) 410740 (CC740)	TELETYPE 4740SD-5

TC 640-0368

FS-4 LINE FEED MOTOR AND CARRIAGE MOTOR DRIVERS

ISSUE 1

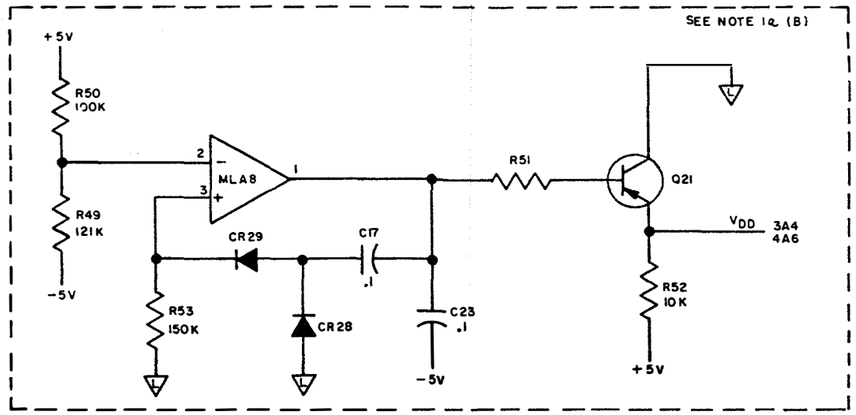


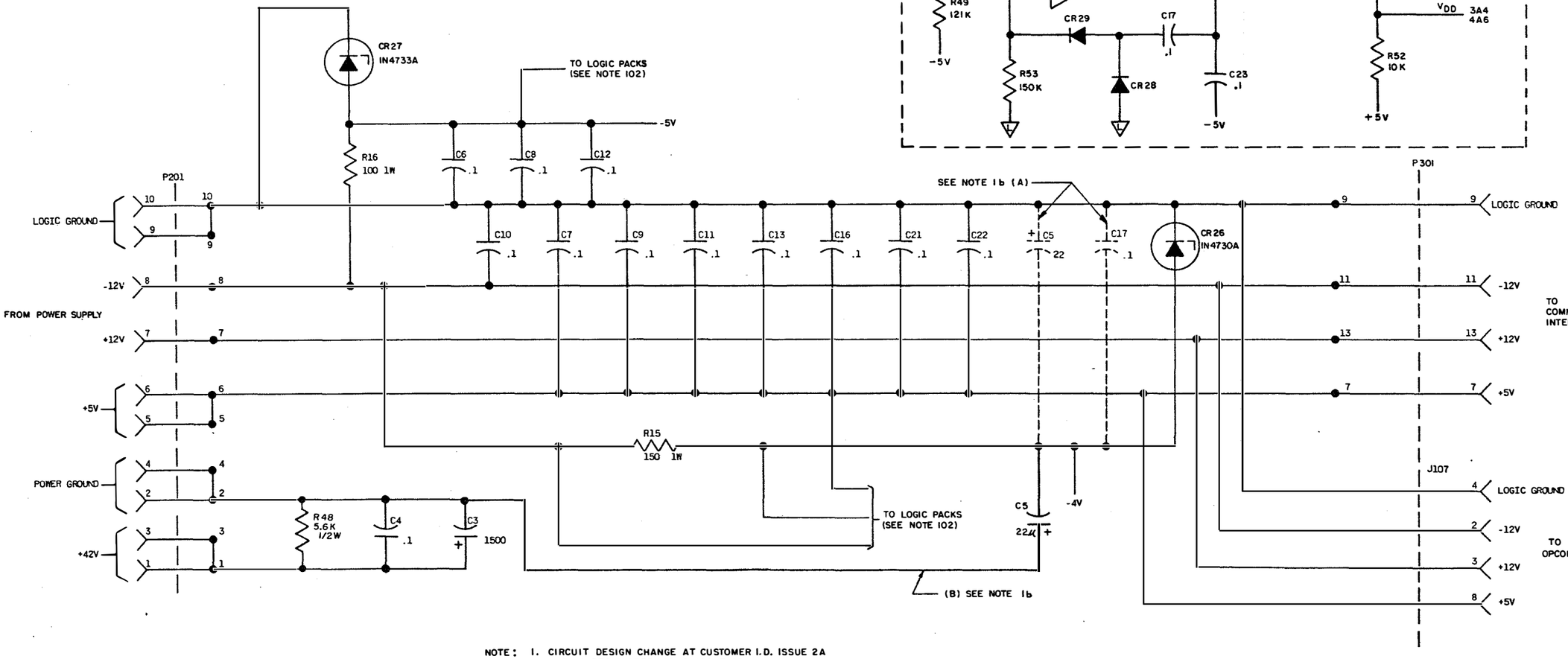
M43 LOGIC CARD (BASIC KSR) 410740 (CC740)	TELETYPE 4740 SD-6

TC 840-0369

FS-5 VOLTAGE DISTRIBUTION

ISSUE
1
2
3
4





NOTE: 1. CIRCUIT DESIGN CHANGE AT CUSTOMER I.D. ISSUE 2A
WIRING DESIGNATED (A) IS ISSUE 1B
WIRING DESIGNATED (B) IS ISSUE 2A OR LATER.
CHANGE RELATED TO ISSUE 2A OF 409740 BOARD

a. ADD P.O.R. CIRCUITRY FOR MACON (MLC4) AND MAPL (MLC7), NEW MACON (430671) AND MAPL (430641) ADDED.

b. TO IMPROVE NOISE IMMUNITY, CAPACITORS C17 REMOVED AND C5 RELOCATED.

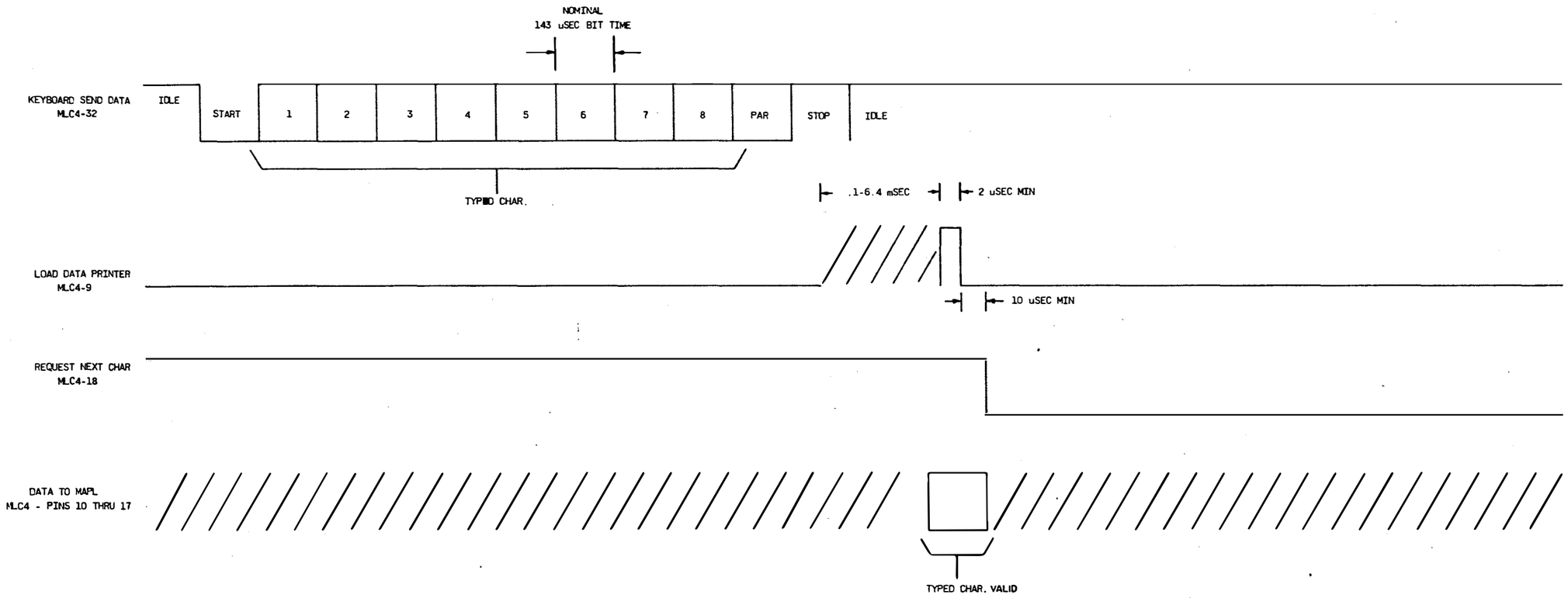
M43 LOGIC CARD (BASIC KSR) 410740 (CC740)	TELETYPE 4740SD-7

TC 640-0360

TC-1 TERMINAL CONTROLLER TIMING

MODE: LOCAL

ISSUE 1



NOTE: TIMING FOR RECEIVED CHARACTER FROM THE LINE IS SIMILAR TO ABOVE EXCEPT THE 'PAR' BIT IS ABSENT AND THE NOMINAL BIT TIME IS 3.33mSEC (30CPS SELECTED) OR 9.09 mSEC (10CPS SELECTED).

M43 LOGIC CARD
(BASIC KSR)
410740 (CC740)

TELETYPE

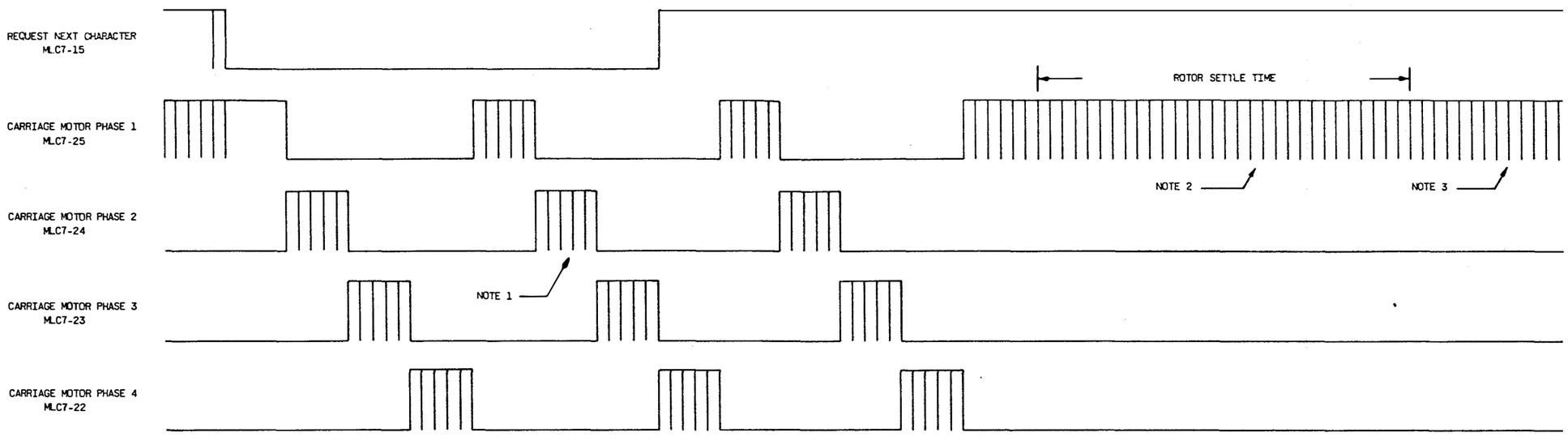
4740SD-8

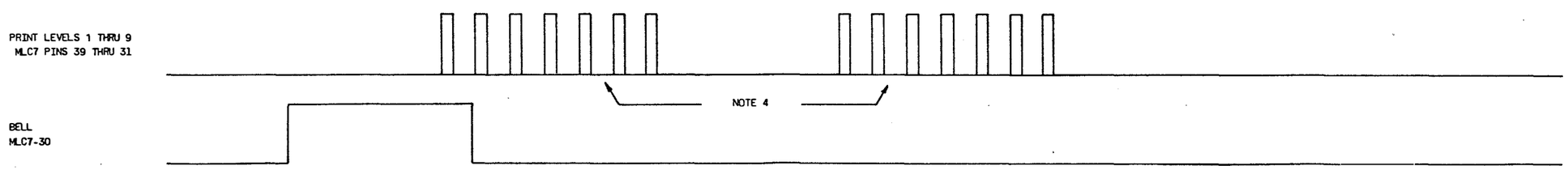
TC 640-0368

ISSUE 1

TC-2 PRINT CHARACTER TIMING

MODE TWO CHARACTER BURST (AT BELL COLUMN)





NOTES: ||||| → INDICATES PULSE WIDTH MODULATION

1. VARIABLE DUTY CYCLE
2. SETTLING POWER DUTY CYCLE
3. IDLE POWER DUTY CYCLE
4. PRESENCE OF PULSE ON A GIVEN LEVEL DEPENDS ON CHARACTER PRINTED.

M43 LOGIC CARD
(BASIC KSR)
410740 (CC 740)

TELETYPE

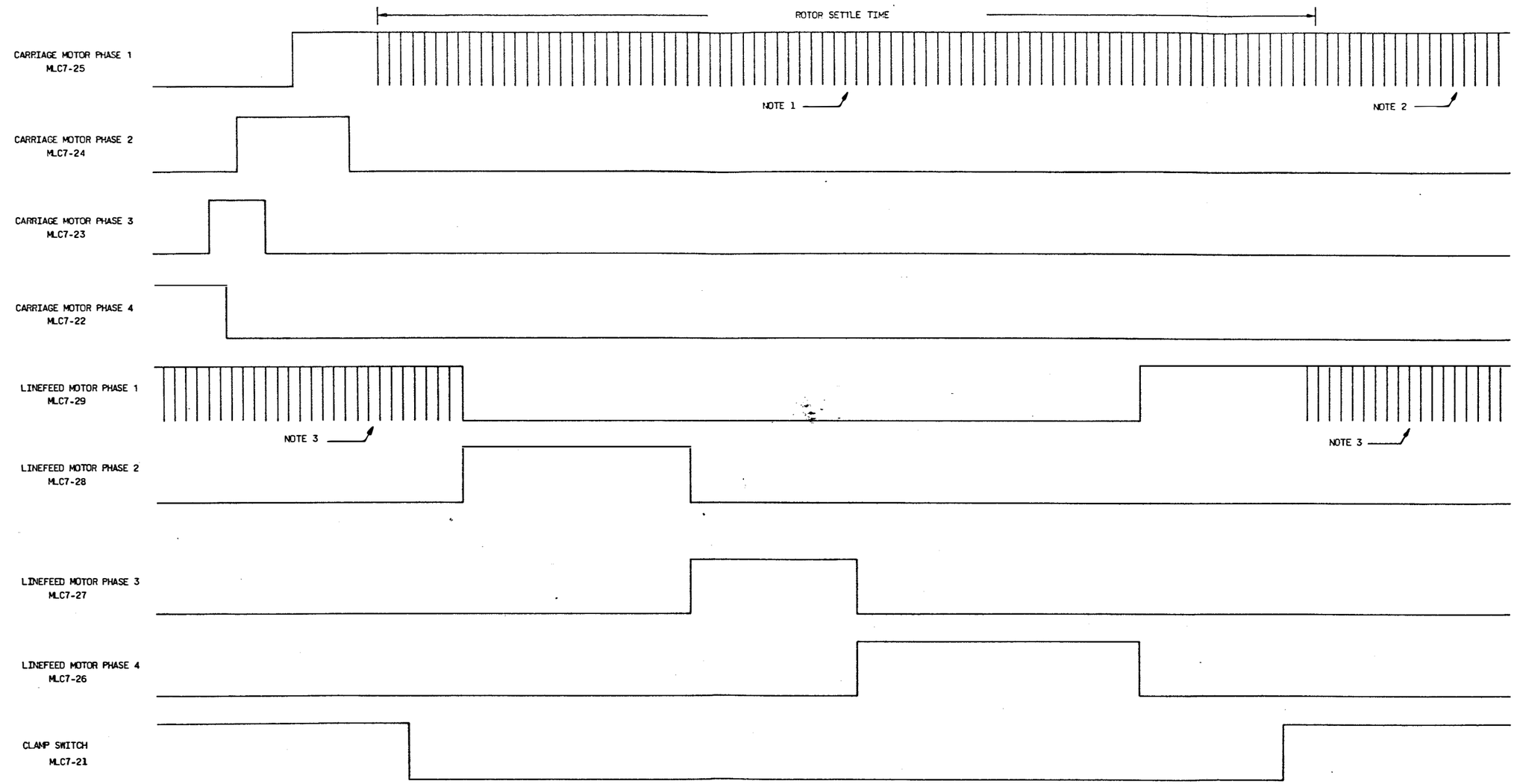
4740SD-9

TC 640.0369

TC-3 CARRIAGE RETURN-LINEFEED TIMING

(SHOWING END OF CARRIAGE RETURN AND BEGINNING OF LINEFEED)

ISSUE 1



NOTES: INDICATES PULSE WIDTH MODULATION

1. SETTLING POWER DUTY CYCLE
2. IDLE POWER DUTY CYCLE
3. LINEFEED DETENT POWER DUTY CYCLE

SEE SPECIFICATION 62,200S FOR SPECIFIC TIMING INFORMATION

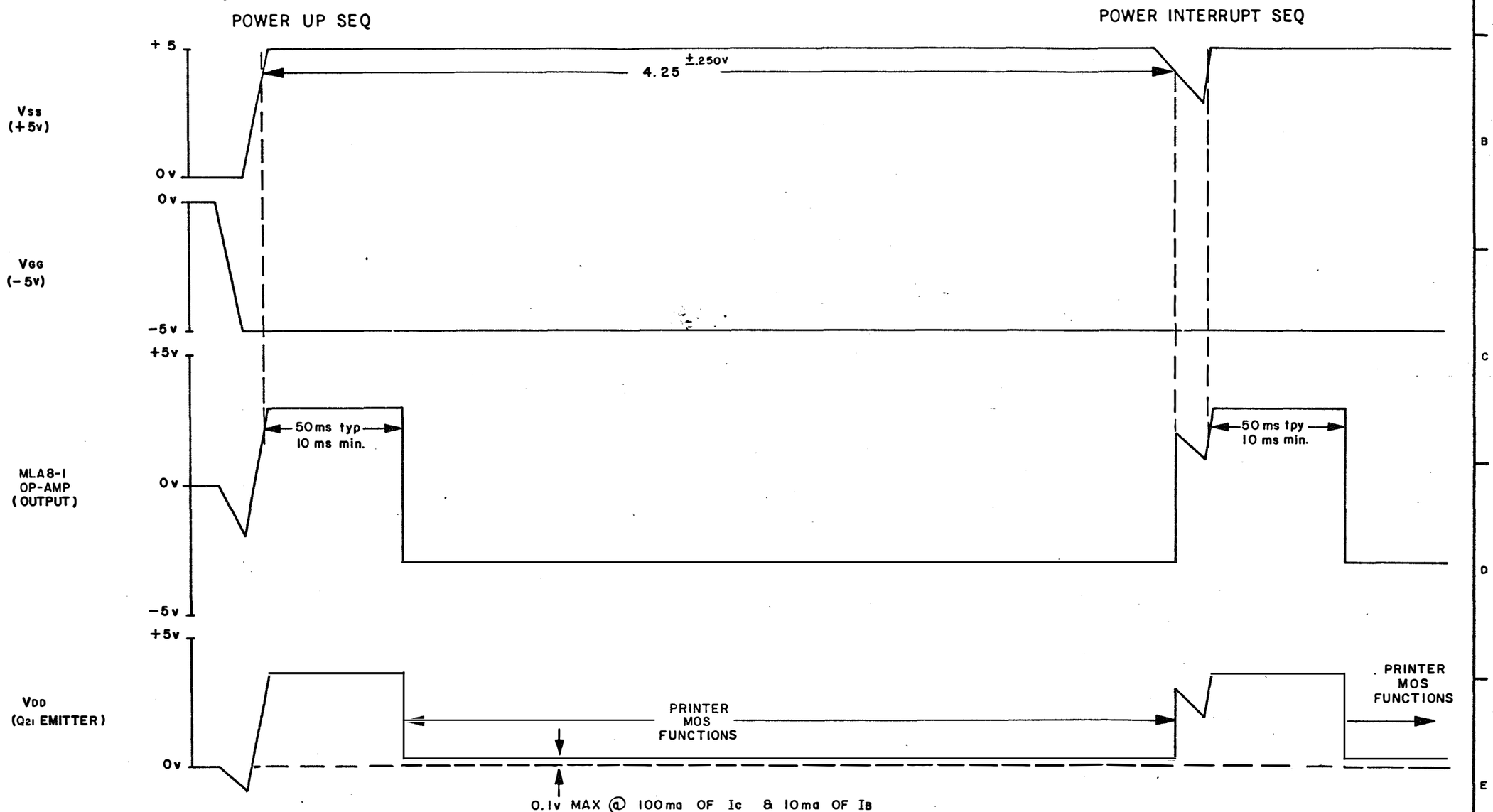
M43 LOGIC CARD
(BASIC KSR)
410740 (CC740)

TELETYPE

4740SD-10

TC 640-0788

TC — 4 TIMING DIAGRAM



ISSUE 1

POWER UP/
POWER INTERRUPT
SEQUENCE

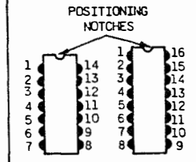
TELETYPE

4740SD-11

TC 640-0369

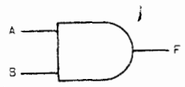
NO.	NOTES
1.	ALL VOLTAGES DC UNLESS OTHERWISE SPECIFIED.
2.	GRAPHICAL SYMBOLS AND THE ASSOCIATED TRUTH TABLES ILLUSTRATED ON THIS PAGE ARE TYPICAL SYMBOLS.
3.	LOGIC NEGATION A SMALL CIRCLE (o) DRAWN AT THE POINT WHERE A SIGNAL LINE JOINS A LOGIC SYMBOL INDICATES A LOGIC NEGATION.
4.	ABBREVIATIONS USED: 0 - LOW STATE (MORE NEGATIVE) 1 - HIGH STATE (MORE POSITIVE) X - STATE OF INPUT DOES NOT AFFECT STATE OF CIRCUIT. NC - NO CHANGE U - INDETERMINATE STATE N_M - STATE OF N AT TIME M. $\overline{N}_M$ - INVERSION OF STATE OF N AT TIME M.
5.	PIN LOCATIONS FOR DUAL-IN-LINE INTEGRATED CIRCUIT PACKAGES.
6.	UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES IN OHMS, ALL CAPACITANCE VALUES IN MICROFARADS.
7.	INTEGRATED CIRCUIT PACKAGE DESIGNATION N1 B3 N1 - ROW ON BOARD B3 - COLUMN ON BOARD INTEGRATED CIRCUIT PACKAGE
8.	H = HIGH VOLTAGE LEVEL > V_{IH} L = LOW VOLTAGE LEVEL > V_{IL} X = DON'T CARE H L = HIGH TO LOW VOLTAGE LEVEL TRANSITION L H = LOW TO HIGH VOLTAGE LEVEL TRANSITION.

POSITIONING NOTCHES



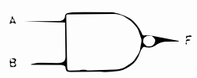
TOP VIEW OF DUAL IN-LINE

AND GATE



A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

NAND GATE

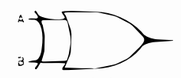


A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

OR GATE

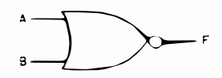
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

EXCLUSIVE - OR GATE



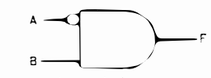
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

NOR GATE



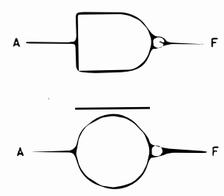
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

PNP - INHIBIT GATE



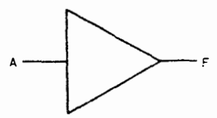
A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

LOGIC INVERTERS



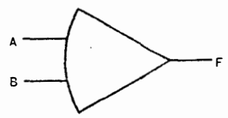
A	F
0	1
1	0

AMPLIFIER

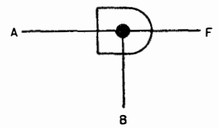


NOTE: INDICATE TYPE OF AMPLIFIER WITHIN SYMBOL WITH THE FOLLOWING CHARACTERISTICS:
PA - PULSE AMPLIFIER
EF - EMITTER FOLLOWER
LD - LAMP DRIVER
RD - RELAY DRIVER
SQ - SQUARING AMPLIFIER

OPERATIONAL AMPLIFIER

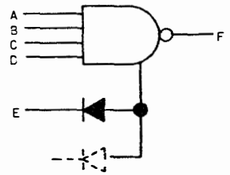


WIRED AND



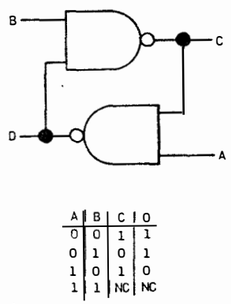
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

NAND GATE



A	B	C	D	E	F
1	1	1	1	1	0
1	0	0	0	0	1
0	0	0	0	0	1
0	1	1	1	1	1

SET-RESET FLIP-FLOP UTILIZING NAND GATES

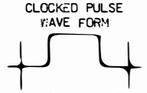


A	B	C	O
0	0	1	1
0	1	0	1
1	0	1	0
1	1	NC	NC

CLOCKED FLIP-FLOP

SYNCHRONOUS TRUTH TABLE 32E845

CLOCKED PULSE WAVE FORM



S_1	S_2	C_1	C_2	N
0	X	0	X	NC
0	X	X	0	NC
X	0	0	X	NC
X	0	X	0	NC
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

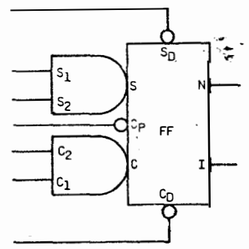
ASYNCHRONOUS TRUTH TABLE 326845

C_C	S_D	N	I
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	1	1

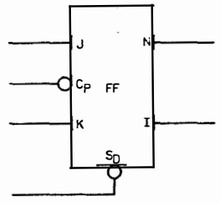
J-K TRUTH TABLES (CONNECT S_2 TO I. C_2 TO N)

T_M		T_{M+1}
S_1	C_1	N
0	0	N_M
1	0	1
0	1	0
1	1	N_M

ASYNCHRONOUS INPUTS, DIRECT SET (S_D) ANY DIRECT CLEAR (C_D), OVERRIDE THE SYNCHRONOUS INPUTS. THEY ARE INDEPENDENT OF ALL OTHER INPUTS.



J-K FLIP-FLOP

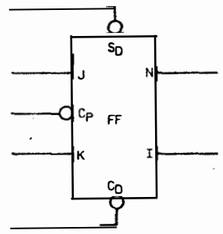


S_D	N	I
1	NC	NC
0	1	0

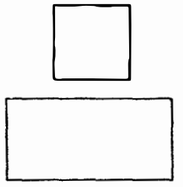
J-K TRUTH TABLE BOTH TYPES

T_M		T_{M+1}
J	K	N
0	0	N_M
1	0	1
0	1	0
1	1	$\overline{N}_M$

J-K FLIP-FLOP



S_D	C_D	N	I
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1



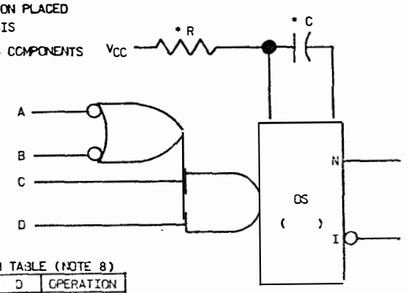
GENERAL SYMBOLS

THE SYMBOL SHALL BE ADEQUATELY LABELED TO IDENTIFY THE FUNCTION PERFORMED. IF A TIME INTERVAL IS INVOLVED, THE TIMING INFORMATION SHALL ALSO BE INCLUDED.

RETRIGGERABLE ONE SHOT

TIMING INFORMATION PLACED WITHIN PARENTHESIS

* EXTERNAL TIMING COMPONENTS



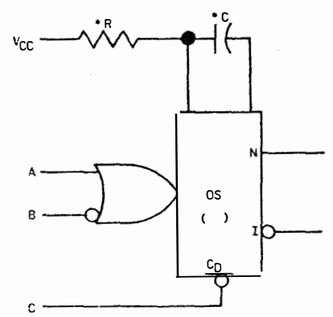
TRIGGERING TRUTH TABLE (NOTE 8)

A	B	C	D	OPERATION
H→L	H	H	H	TRIGGER
H	H→L	H	H	TRIGGER
L	X	L→H	H	TRIGGER
X	L	L→H	H	TRIGGER
L	X	H	L→H	TRIGGER
X	L	H	L→H	TRIGGER

RETRIGGERABLE AND RESETTABLE ONE SHOT

TIMING INFORMATION PLACED WITHIN PARENTHESIS

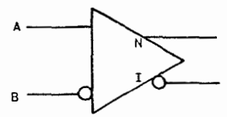
* EXTERNAL TIMING COMPONENTS.

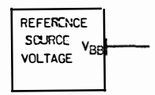


TRIGGERING TRUTH TABLE (NOTE 8)

A	B	C	OPERATION
L	H→L	H	TRIGGER
L→H	H	H	TRIGGER
X	X	L	RESET

LINE RECEIVER





TRUTH TABLE

INPUT MODE	DEFINITIONS OF INPUTS A AND B	OUTPUTS N & I	A	B	N	I
BALANCED	H = > OTHER INPUT L = < OTHER INPUT	NOTE 8	H	L	H	L
			L	H	L	H
UNBALANCED	H = > V_{BB} L = < V_{BB}		H	V_{BB}	H	L
			L	V_{BB}	L	H
			V_{BB}	L	H	L
			V_{BB}	H	L	H

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	4-24-72	00559
2	4-27-73	02269

LOGIC SYMBOLS AND TRUTH TABLES

APPROVALS		
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
D&R	R&D	bm
ENGR. M.F.	DSGNR. M.F.	
DRN. A.R.A.	DATE 10-10-69	
R&D FILE 36 (5)		

S-NUMBER

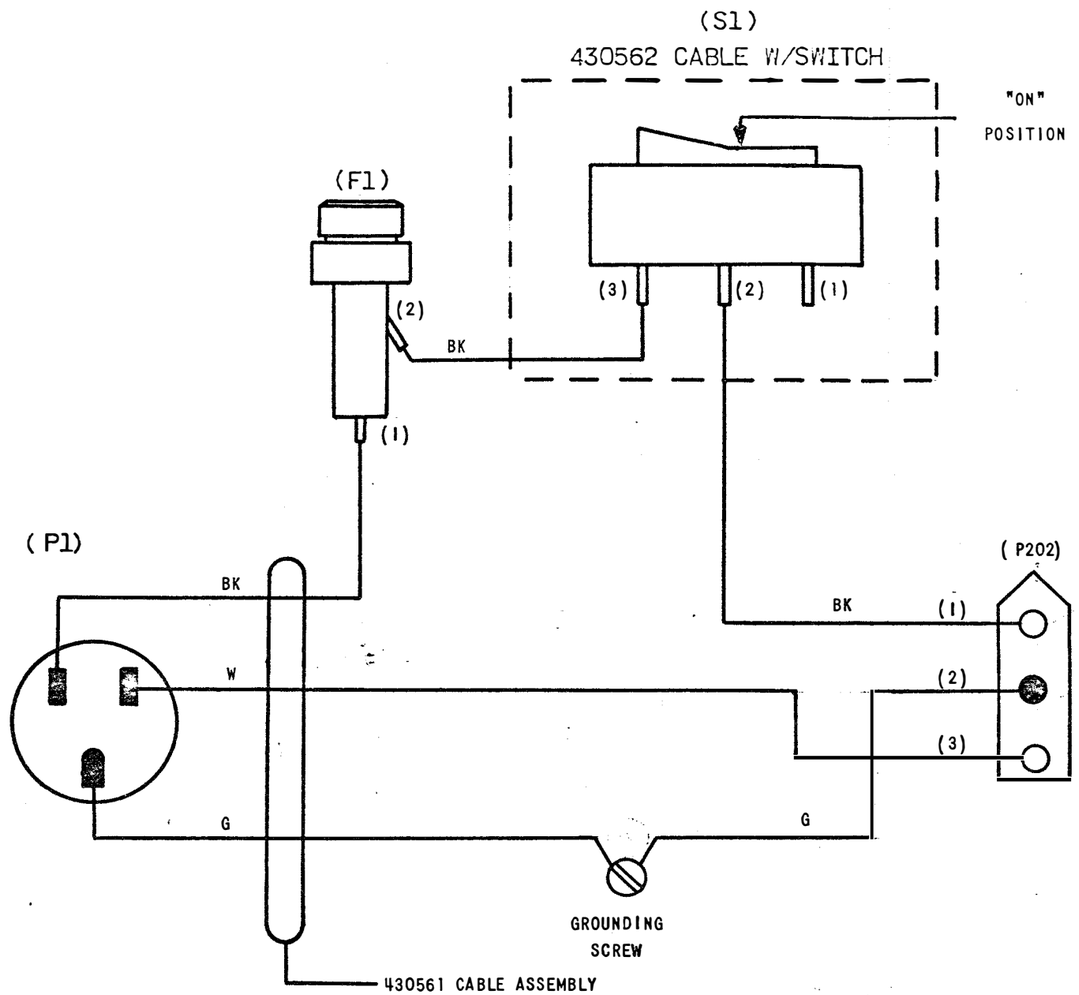
TELETYPE

9100WD

TC 434 (3-69)

NO. NOTES

1. ALL VOLTAGES 115VAC.
2. TERMINAL DESIGNATIONS IN PARENTHESES ARE FOR REFERENCE AND ARE NOT MARKED ON COMPONENT.
3. ○ INDICATES FEMALE TERMINAL
   ● INDICATES MALE TERMINAL
4. ALL WIRE 18 AWG.
5. FUSE 1.0A SL-BL(PART NO. 113431)



REVISIONS		
ISSUE	DATE	AUTH. NO.
1	7-27-76	24596R

ACTUAL WIRING DIAGRAM
FOR
430550 REAR FRAME
ASSEMBLY

APPROVALS		
PROJ. SUPV. 6-28-76	PROJ. DIR. 6-28-76	MFG. REL. COMPL.
ENGR.	DSGNR.	
DRN.	DATE 6-25-76	
R & D FILE 1-30.171.211A		
S-NUMBER		

TELETYPE

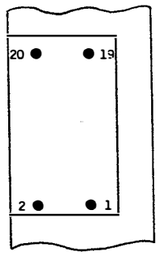
9612 WD

TC 255 (3-69)

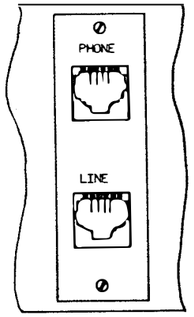
REVISIONS		
ISSUE	DATE	AUTH. NO.
1	9-20-77	25249-R

TDU
TERMINAL DATA UNIT
430750

PLUG
(TOP CENTER)



CONNECTORS
(BACK, LEFT END)

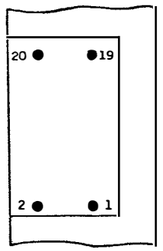


TERMINAL INTERFACE

PIN NUMBER	CODE	FUNCTION	DIRECTION (TERMINAL)
1	DL	DIGITAL LOOP	FROM
2	-		
3	AL	ANALOG LOOP	FROM
4	-		
5	TR	TERMINAL READY	FROM
6	-		
7	-		
8	-		
9	GND	CIRCUIT GROUND	
10	-		
11	-12V SUPPLY		
12	-		
13	+12V SUPPLY		
14	-		
15	DR	DATA READY	TO
16	-		
17	RD	RECEIVED DATA	TO
18	-		
19	SD	SEND DATA	FROM
20	-		

TAU
TERMINAL AUXILIARY UNIT
430751

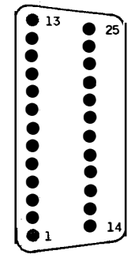
PLUG (TOP CENTER)



TERMINAL INTERFACE

PIN NO.	CODE	FUNCTION	DIRECTION (TERMINAL)	EIA EQUIVALENT
1	DL	DIGITIAL LOOP	FROM	
2	DSI	DATA SPEED INDICATOR	TO TERMINAL	CI
3	AL	ANALOG LOOP TEST	FROM	
4	DSS	DATA SPEED SELECT	FROM TERMINAL	CH
5	TR	TERMINAL READY	FROM	CD
6	RS	REQUEST TO SEND	FROM	CA
7	+5	+5 VOLTS		
8	-	-		
9	GND	CIRCUIT GROUND		
10		-		
11	-12	-12 VOLTS		
12	-	-		
13	+12	+12 VOLTS		
14	-	-		
15	DR	DATA READY	TO	CB.CC.CF
16	TW2	TWX INDICATOR (FUTURE)	TO	
17	RD	RECEIVE DATA	TO	BB
18	TW1	TWX CONTROL		
19	SD	TRANSMIT DATA	FROM	BA
20	-	-		

PLUG (BACK, LEFT END)



DATA SET INTERFACE SIGNALS

CONNECTOR PIN	SIGNAL	EIA CIRCUIT
1	PROTECTIVE GROUND	AA
2	TRANSMIT DATA	BA
3	RECEIVE DATA	BB
4	REQUEST TO SEND	RS
5	CLEAR TO SEND	CB
6	DATA SET READY	CC
7	SIGNAL GND	AB
8	RECEIVED LINE SIGNAL DETECTOR	CF
9		
10		
11	TWX CONTROL	-
12	DATA SPEED INDICATOR	SCF
13		
14		
15		
16		
17		
18	TWX INDICATOR	-
19		
20	DATA TERMINAL READY	CD
21		
22		
23	DATA SPEED SELECT	CH
24		
25	ANALOG LOOP TEST	

MODEL 43
TERMINAL DATA UNIT
(430750)
AND
TERMINAL AUXILIARY
UNIT
(430751)

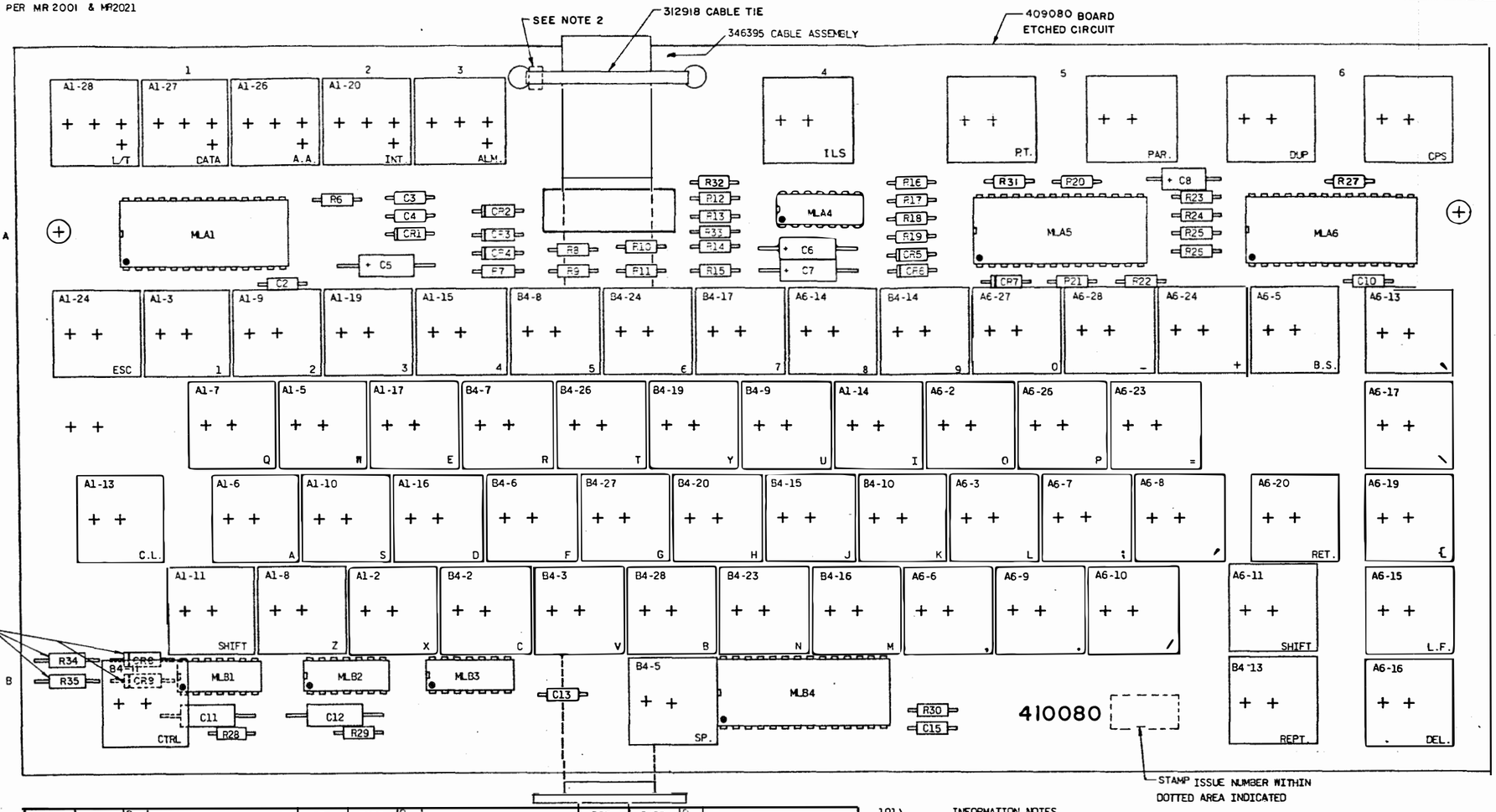
APPROVALS		
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL. DC 9.77
ENGR. LDM	DSGNR.	
DRN. MUSK	DATE 8-16-77	
R&D FILE 2.30.171.261A		
S-NUMBER 96/65 & 96/75		

TELETYPE

9635WD

TC 434 (3-69)

NOTE: MANUFACTURE PER MR 2001 & MP2021

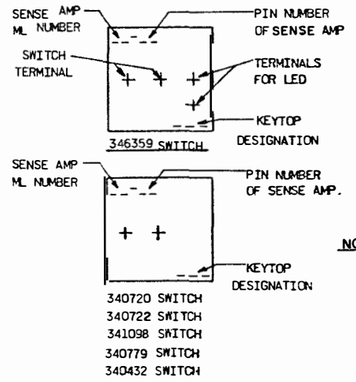


REF. DESIG.	PART NO. REQ.	QTY.	DESCRIPTION
MLA1	342280	3	SENSE AMP TSA-2L
MLB1	339002	2	QUAD 2 INPUT GATE (9002)
MLB2			SAME AS MLB1
MLB3	315990	1	DECADE COUNTER (7490)
MLA4	404027	1	CLOCK DRIVER
MLB4			SAME AS MLA1
MLA5	342238	1	KEYSWITCH LOGIC TKL-2KP
MLA6			SAME AS MLA1
CR1	346394	1	DIODE, ZENER 1N4730A
CR2-9	197464	8	DIODE 1N4148
C2	346238	3	CAPACITOR 33 pf
C3-4	405324	3	CAPACITOR 0.1 MFD
C5-7	333727	3	CAPACITOR 6.8 MFD
C8	336948	1	CAPACITOR 1.0 MFD
C10			SAME AS C2
C11-12	300384	2	CAPACITOR, .0047 MFD
C13			SAME AS C3
C15			SAME AS C2
R34-35	315952	2	RESISTOR, 820 OHM 1/4 W
R6	326573	3	RESISTOR, 1.8M OHM 1/4W
R7	321213	1	RESISTOR, 1K OHM 1/4W
R8-11	315959	4	RESISTOR, 4.7K OHM 1/4W
R12-13	320275	8	RESISTOR, 10K OHM 1/4W
R14-15	315947	2	RESISTOR, 51 OHM 1/4W

REF. DESIG.	PART NO. REQ.	QTY.	DESCRIPTION
R16	315948	1	RESISTOR, 100 OHM 1/4W
R18	315971	1	RESISTOR, 630 OHM 1/4W
R19	315953	2	RESISTOR, 1.2K OHM 1/4W
R20-22			SAME AS R12
R23	333417	1	RESISTOR 680K OHM 1/4W
R24-26			SAME AS R12
R27			SAME AS R6
R28-29	328783	2	RESISTOR 180 OHM 1/4W
R30			SAME AS R6
R17	330640	1	RESISTOR 150 OHM 1/4W
R31-32	315954	2	RESISTOR 1.5K OHM 1/4 W
R33			SAME AS R19
	340730	6	CHANNEL
	346426	1	LOCATING PLATE
	151152	2	SCREW 4-40
	3640	2	WASHER, LOCK
	125011	1	WASHER, FLAT
	340720	57	KEYSWITCH, BASIC
	340722	1	KEYSWITCH, LATCH
	340359	5	KEYSWITCH, IND
	341098	3	KEYSWITCH, LATCH DC
	346235	3	HOUSING
	340762	1	HOUSING ASSEM.
	346432	1	KEYSWITCH, DC CONTACT
	340779	1	KEYSWITCH, DC CONTACT
	340704	1	HOUSING
	346410	1	LABEL (NOTE 3)

REF. DESIG.	PART NO. REQ.	QTY.	DESCRIPTION
	346293	9	SPACER, SHORT
	346301	2	SPACER .188
	346302	3	SPACER .375
	346303	6	SPACER, .562
	346304	1	SPACER .750
	346700	1	FRAME, FRONT
	346701	1	FRAME, REAR
	346398	1	FRAME, LEFT W/POST
	346399	1	FRAME, RIGHT W/POST
	181241	8	SCREW W/WASHER 6-40
	7935IRM	15FT	TAPE
	79324RM	6FT	TAPE, FOAM
	79266RM	24FT	TAPE, FOAM
	79331RM	24FT	TAPE, FOAM
	312918	1	CABLE TIE
	346395	1	CABLE ASSEMBLY
	409080	1	BOARD, ETCHED

101) INFORMATION NOTES



340720 SWITCH
340722 SWITCH
341098 SWITCH
340779 SWITCH
340432 SWITCH

NOTE:

102. AT CUSTOMER IDENTIFICATION ISSUE 1B R34, 35, CR8 AND CR9 WERE ADDED

MANUFACTURING NOTES:

1). REFER TO 43K100AC ANALYSIS CHART FOR POSITION & PART NUMBER OF COMPONENTS AND CHANNEL ASSEMBLY INFORMATION.

2). CABLE TIE SHOULD BE POSITIONED SUCH THAT THE TIE LOCK IS LOCATED BETWEEN HOLE AND CABLE SHOWN (OTHER SIDE).

3). REFER TO 40K/MC FOR LABEL POSITION.

SIMILAR TO:

REVISIONS

CUSTOMER IDENTIFICATION ISSUE LTR.	ENGR. REVISION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.
-	-	1	1	6-11-76	24330 R
1	A	2	2	9-8-76	16609
1	A	-	3		16692
1	A	-	4	3-11-77	18184
1	B	102	5	5-1-77	16857
1	B	3	6	11-14-77	18370
1	B	—	7	8-31-77	18844
1	B	—	8	—	15121
1	B	—	9	—	15148

P

CIRCUIT CARD
CC 080

CONSOLE LOGIC

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

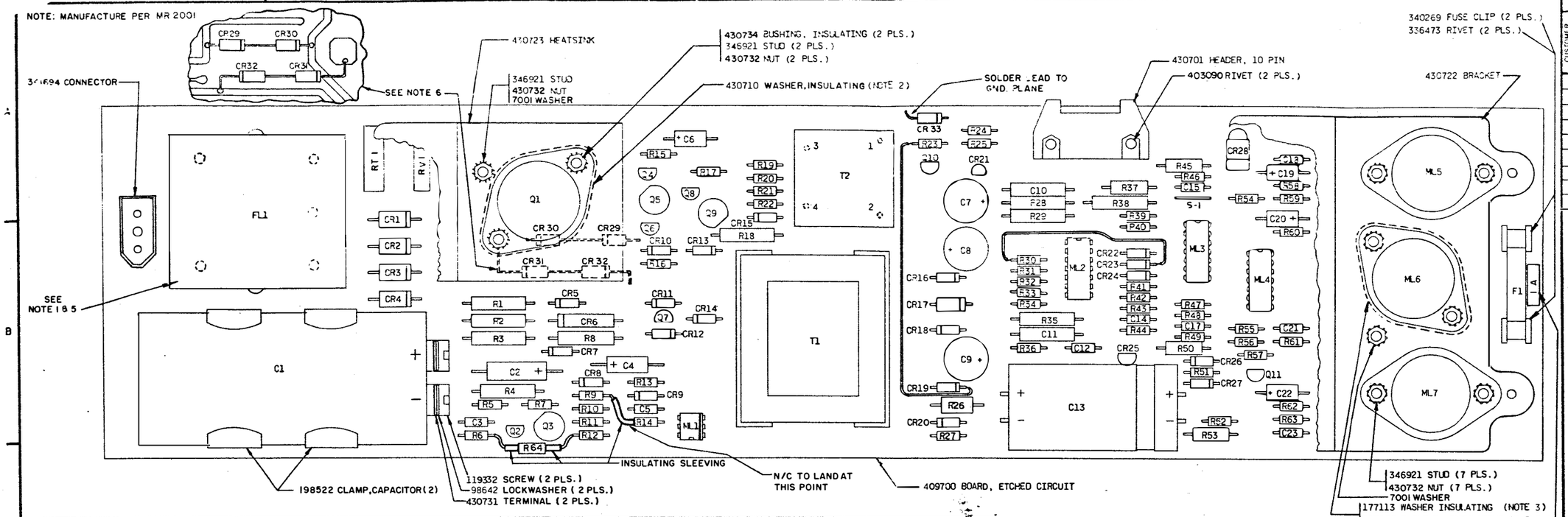
ENGR. R.H.F. DSGNR. R.E.G.
DRAWN DATE 1-30-76
E-NUMBER
SD-CD NO. 4080
R&D FILE NO. 2-30 171 263A

TELETYPE

410080

TC 661-1174

NOTE: MANUFACTURE PER MR 2001



REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
C1	430706		CAPACITOR, 200 MFD
C2	310930		CAPACITOR, 100 MFD
C3	405324		CAPACITOR, .1 MFD
C4	333727		CAPACITOR, 6.8 MFD
C5	405324		CAPACITOR, .1 MFD
C6	300057		CAPACITOR, .01 MFD
C7	430704		CAPACITOR, 330 MFD
C8	430704		CAPACITOR, 330 MFD
C9	430704		CAPACITOR, 330 MFD
C10	430721		CAPACITOR, 1200 PFD
C11	430721		CAPACITOR, 1200 PFD
C12	405324		CAPACITOR, .1 MFD
C13	430705		CAPACITOR, 530 MFD
C14	405324		CAPACITOR, .1 MFD
C15	325034		CAPACITOR, 120 PFD
C17	405324		CAPACITOR, .1 MFD
C18	405324		CAPACITOR, .1 MFD
C19	310929		CAPACITOR, 1.8 MFD
C20	310929		CAPACITOR, 1.8 MFD
C21	405324		CAPACITOR, .1 MFD
C22	310929		CAPACITOR, 1.8 MFD
C23	405324		CAPACITOR, .1 MFD
CR1	408037		DIODE, 400V
CR2	408037		DIODE, 400V
CR3	408037		DIODE, 400V
CR4	408037		DIODE, 400V
CR5	430725		DIODE, ZENER 51V
CR6	430713		DIODE, ZENER 190V
CR7	430605		DIODE, 1N4936
CR8	300102		DIODE, 1N4156
CR9	430605		DIODE, 1N4936
CR10	430605		DIODE, 1N4936
CR11	430605		DIODE, 1N4936
CR12	430605		DIODE, 1N4936
CR13	430605		DIODE, 1N4936
CR14	430605		DIODE, 1N4936
CR15	430605		DIODE, 1N4936
CR16	430605		DIODE, 1N4936

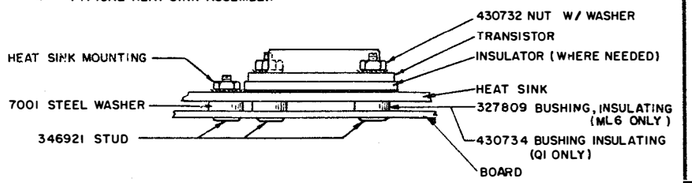
REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
CR17	430715		DIODE, 200V 3A FR
CR18	430605		DIODE, 1N4936
CR19	430605		DIODE, 1N4936
CR20	312401		DIODE, ZENER 1N4755A
CR21	430729		DIODE, 4 LAYER
CR22	321135		DIODE, ZENER 1N4735A
CR23	430724		DIODE, ZENER 15V
CR24	430725		DIODE, ZENER 51V
CR25	336694		THYRISTOR, SCR .8A
CR26	197464		DIODE, 1N4148
CR27	430724		DIODE, ZENER 15V
CR28	405029		LED, PCB MOUNTABLE
CR29	430605		DIODE, 1N4936
CR30	430605		DIODE, 1N4936
CR31	430713		DIODE, ZENER 190V.
CR32	430605		DIODE, 1N4936
CR33	430725		DIODE, ZENER 51V.
FL1	430709		FILTER, RFI
F1	120139		FUSE, 1A
ML1	335522		IC, OPTICAL COUPLER
ML2	404239		QUAD VOLT COMPARATOR
ML3	326823		REGULATOR, VOLTAGE
ML4	404239		QUAD VOLT COMPARATOR
ML5	402202		REGULATOR, +5V
ML6	402204		REGULATOR, -12V
ML7	402201		REGULATOR, +12V

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
R1	120211		RESISTOR, 20K 1W
R2	182763		RESISTOR, 680 1W
R3	118198		RESISTOR, 56K 1W
R4	430714		RESISTOR, .24 1W
R5	320275		RESISTOR, 10K 1/4W
R6	315959		RESISTOR, 4700 1/4W
R7	321213		RESISTOR, 1K 1/4W
R8	144464		RESISTOR, 220 1W
R9	318302		RESISTOR, 220 1/4W
R10	321213		RESISTOR, 1K 1/4W
R11	318801		RESISTOR, 47K 1/4W
R12	320275		RESISTOR, 10K 1/4W
R13	315955		RESISTOR, 2200 1/4W
R14	320275		RESISTOR, 10K 1/4W
R15	320276		RESISTOR, 470 1/4W
R16	323785		RESISTOR, 330 1/4W
R17	177101		RESISTOR, 6.8 1/2W
R18	178362		RESISTOR, 10 1W
R19	315948		RESISTOR, 100 1/4W
R20	315948		RESISTOR, 100 1/4W
R21	315948		RESISTOR, 100 1/4W
R22	315948		RESISTOR, 100 1/4W
R23	341696		RESISTOR, 121K 1%
R24	341592		RESISTOR, 75K 1%
R25	315957		RESISTOR, 3300 1/4W
R26	113186		RESISTOR, 5600 1/2W
R27	315971		RESISTOR, 680 1/4W
R28	341696		RESISTOR, 121K 1%
R29	341592		RESISTOR, 75K 1%
R30	315957		RESISTOR, 3300 1/4W
R31	327721		RESISTOR, 4.7 MEG. 1/4W
R32	324902		RESISTOR, 100K 1%
R33	321508		RESISTOR, 100K 1/4W
R34	328785		RESISTOR, 330 1/4W
R35	341696		RESISTOR, 121K 1%
R36	321503		RESISTOR, 100K 1/4W
R37	401067		RESISTOR, 2400 .5%
R38	324902		RESISTOR, 30.1K 1%
R39	320275		RESISTOR, 10K 1/4W
R40	330641		RESISTOR, 1 MEG. 1/4W
R41	320276		RESISTOR, 470 1/4W

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
R42	320276		RESISTOR, 470 1/4W
R43	320276		RESISTOR, 470 1/4W
R44	321213		RESISTOR, 1 K 1/4W
R45	401067		RESISTOR, 2400 .5%
R46	321508		RESISTOR, 100K 1/4W
R47	315938		RESISTOR, 27K 1/4W
R48	321213		RESISTOR, 1K 1/4W
R49	430719		RESISTOR 25.8K .5%
R50	401067		RESISTOR, 2400 .5%
R51	320275		RESISTOR, 10K 1/4W
R52	318803		RESISTOR, 2400 1/4W
R53	321258		RESISTOR, 20K 1/2W
R54	315956		RESISTOR, 2700 1/4W
R55	318803		RESISTOR, 2400 1/4W
R56	401067		RESISTOR, 2400 .5%
R57	315956		RESISTOR, 2700 1/4W
R58	336697		RESISTOR, 430 1/4W
R59	318803		RESISTOR, 2400 1/4W
R60	315961		RESISTOR, 8200 1/4W
R61	401067		RESISTOR, 2400 .5%
R62	320026		RESISTOR, 3900 1/4W
R63	318803		RESISTOR, 2400 1/4W
R64	320275		RESISTOR, 10K 1/4W
RT1	430707		THERMISTOR
RV1	430708		VARISTOR
T1	430702		TRANSFORMER, POWER
T2	430703		TRANSFORMER, PULSE
S1	336470		STRAP

NOTES:

1. MOUNT FL1 WITH TWO PIN SIDE ADJACENT TO 341694 CONNECTOR AND BEND SIDE TABS ON UNDERSIDE TOWARD EACH OTHER.
2. MOUNT 430710 INSULATING WASHER BETWEEN HEAT SINK AND TRANSISTOR Q1.
3. SUITABLE HEAT SINK COMPOUND UNDER Q1, ML5, ML6 AND ML7. COMPOUND TO BE APPLIED BETWEEN INSULATOR AND HEAT SINK OF Q1 AND ML6
4. TYPICAL HEAT SINK ASSEMBLY.



5. A MINIMUM OF .020 CLEARANCE MUST BE MAINTAINED BETWEEN CIRCUIT BOARD AND CASE OF FILTER. USE 131228 INSULATING WASHERS OVER MOUNTING TABS IF REQUIRED.
6. AT CUSTOMER IDENTIFICATION ISSUE 2A, C19, C20, C22 WAS CHANGED FROM 1 MFD., R23 WAS CHANGED FROM 3.3K, R44 WAS CHANGED FROM 10K, CR31, CR32 AND CR33 WERE ADDED, AS SHOWN ABOVE.
7. AT CUSTOMER IDENTIFICATION ISSUE 3A, THE FOLLOWING CHANGES WERE MADE, CR20 WAS CHANGED FROM 328696, R11 CHANGED FROM 320275, R27 CHANGED FROM 321213, R64 WAS ADDED, AND ONE LEAD OF R14 WAS MOVED FROM ML-1 TO BASE OF Q7.
8. AT CUSTOMER IDENTIFICATION ISSUE 4A, CONDUCTOR ON NON-COMPONENT SIDE FROM CR21 TO R23 AND PIN 2 OF 430703 TRANSFORMER WAS CUT AT CR21. CONDUCTOR FROM R29 TO C9 WAS CUT ON COMPONENT SIDE, STRAP ADDED FROM LEFT SIDE OF R23 TO CATHODE OF CR19 AND STRAP ADDED FROM LEFT SIDE OF R30 TO CATHODE OF CR23. S1 REPLACED C16.
9. AT CUSTOMER IDENTIFICATION ISSUE 4B, ML1 WAS CHANGED FROM 404325.
10. AT CUSTOMER IDENTIFICATION ISSUE 4C THE FOLLOWING CHANGE WAS MADE: BUSHING UNDER Q1 CHANGED FROM 327809 TO 430734.
11. AT CUSTOMER IDENTIFICATION ISSUE 4D R34 WAS CHANGED FROM 321213

REVISIONS

CUSTOMER IDENTIFICATION ISSUE	MFG VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO
1	A	1T04	1	7-27-76	24582R
1	A	5	2	—	16674
2	A	6	3	10-11-75	16938
3	A	7	4	11-1-76	16898
4	A	8	5	2-2-77	18109
4	B	9	6	—	11802
4	C	10	7	4-1-77	18273
4	C	——	8	——	18287
4	D	11	9	9-1-77	18666

CIRCUIT CARD

CC 700

POWER SUPPLY CARD

P

APPROVALS

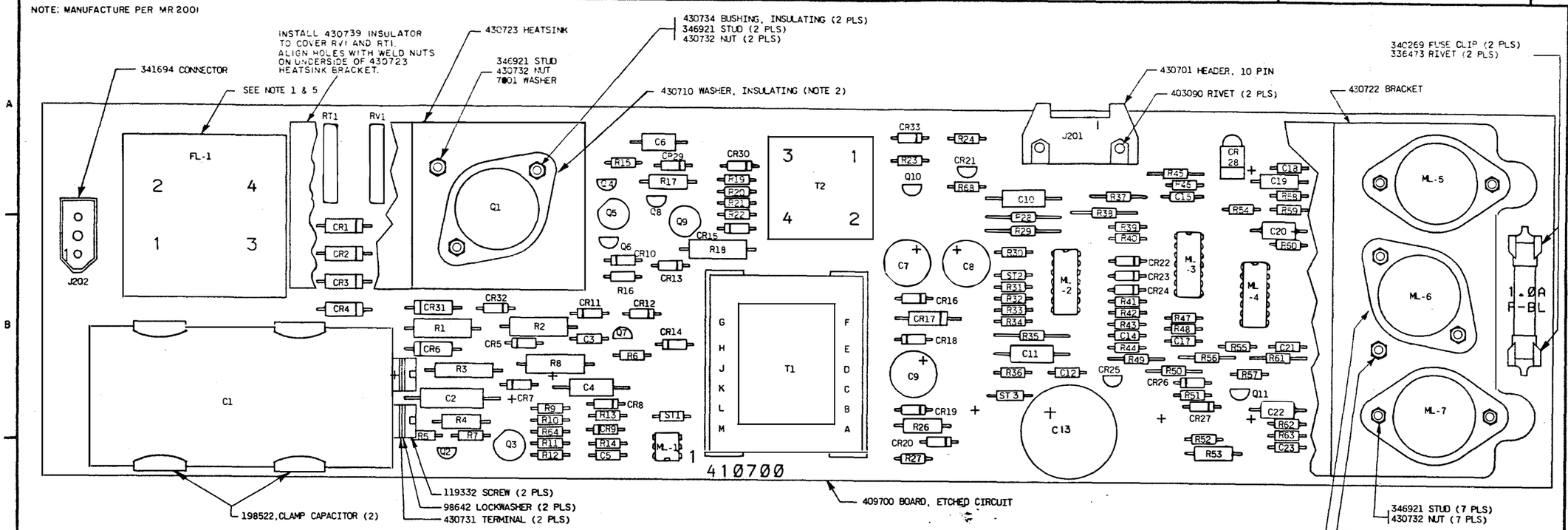
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

ENGR. F.P.K.	DSGNR.
DRAWN	DATE
PROD. NO.	410700
SD-CD NO.	4700
R&D FILE NO.	1-30.171.211A

TELETYPE

410700

TC 661-1174



REF DESIG.	PART NO.	REQ	Q_{TY}	DESCRIPTION
C1	430706			CAPACITOR, 200 MFD
C2	310930			CAPACITOR, 100 MFD
C3	405324			CAPACITOR, .1 MFD
C4	333727			CAPACITOR, 6.8 MFD
C5	405324			SAME AS C3
C6	300057			CAPACITOR, .01 MFD
C7	430704			CAPACITOR, 330 MFD
C8	430704			SAME AS C7
C9	430704			SAME AS C7
C10	430721			CAPACITOR, 1200 PFD
C11	430721			SAME AS C10
C12	405324			SAME AS C3
C13	430738			CAPACITOR, 530 MFD
C14	405324			SAME AS C3
C15	325034			CAPACITOR, 120 PFD
C17	405324			SAME AS C3
C18	405324			SAME AS C3
C19	310929			CAPACITOR, 1.8 MFD
C20	310929			SAME AS C19
C21	405324			SAME AS C3
C22	310929			SAME AS C19
C23	405324			SAME AS C3
CR1	408037			DIODE, 400V IN5060
CR2	408037			SAME AS CR1
CR3	408037			SAME AS CR1
CR4	408037			SAME AS CR1
CR5	430725			DIODE, ZENER 51V IN4757
CR6	430713			DIODE, ZENER 190V IN5387
CR7	430605			DIODE, IN4936
CR8	430605			DIODE, SAME AS CR7
CR9	430605			SAME AS CR7
CR10	430605			SAME AS CR7
CR11	430605			SAME AS CR7
CR12	430605			SAME AS CR7
CR13	430605			SAME AS CR7
CR14	430605			SAME AS CR7
CR15	430605			SAME AS CR7
CR16	430605			SAME AS CR7

REF DESIG.	PART NO.	REQ	Q_{TY}	DESCRIPTION
CR17	430715			DIODE, 200V 3A FR
CR18	430605			SAME AS CR7
CR19	430605			SAME AS CR7
CR20	312401			DIODE, ZENER IN4755A
CR21	430729			DIODE, 4 LAYER
CR22	321135			DIODE, ZENER IN4735A
CR23	430724			DIODE, ZENER 15V
CR24	430725			SAME AS CR5
CR25	336694			THYRISTOR, SCR .8A
CR26	197464			DIODE, IN4148
CR27	430724			SAME AS CR23
CR28	405029			LED, PCB MOUNTABLE
CR29	430605			SAME AS CR7
CR30	430605			SAME AS CR7
CR31	430713			SAME AS CR6
CR32	430605			SAME AS CR7
CR33	430725			SAME AS CR5
FL1	430709			FILTER, RFI
F1	120139			FUSE, 1A
ML1	335522			IC, OPTICAL COUPLER
ML2	404239			QUAD VOLT COMPARATOR
ML3	326823			REGULATOR, VOLTAGE
ML4	404239			QUAD VOLT COMPARATOR
ML5	402202			REGULATOR, +5V
ML6	402204			REGULATOR, -12V
ML7	402201			REGULATOR, +12V
Q1	430711			TRANSISTOR, 450V
Q2	400909			TRANSISTOR, 60V NPN
Q3	325077			TRANSISTOR, 2N4355
Q4	400909			SAME AS Q2
Q5	325077			SAME AS Q3
Q6	400909			SAME AS Q2
Q7	400909			SAME AS Q2
Q8	400909			SAME AS Q2
Q9	325077			SAME AS Q3
Q10	400909			SAME AS Q2
Q11	400909			SAME AS Q2

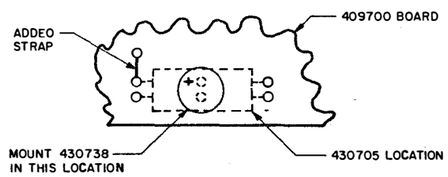
REF DESIG	PART NO.	REQ	Q_{TY}	DESCRIPTION
R1	120211			RESISTOR, 20K 1W
R2	182763			RESISTOR, 680 1W
R3	118198			RESISTOR, 56K 1W
R4	430714			RESISTOR, .24 1W
R5	320275			RESISTOR, 10K 1/4W
R6	315959			RESISTOR, 4700 1/4W
R7	321213			RESISTOR, 1K 1/4W
R8	144464			RESISTOR, 220 1W
R9	318802			RESISTOR, 220 1/4W
R10	321213			SAME AS R7
R11	318801			RESISTOR, 47K 1/4W
R12	320275			SAME AS R5
R13	315955			RESISTOR, 2.2K 1/4W
R14	320275			SAME AS R5
R15	320276			RESISTOR, 470 1/4W
R16	328785			RESISTOR, 330 1/4W
R17	177101			RESISTOR, 6.8 1/2W
R18	178862			RESISTOR, 10 1W
R19	315948			RESISTOR, 100 1/4W
R20	315948			SAME AS R19
R21	335622			RESISTOR, 68 1/4W
R22	315951			RESISTOR, 560 1/4W
R23	320275			SAME AS R5
R24	320275			SAME AS R5
R26	118186			RESISTOR, 5600 1/2W
R27	315971			RESISTOR, 680 1/4W
R28	341596			RESISTOR, 121K 1%
R29	341592			RESISTOR, 75K 1%
R30	315957			RESISTOR, 3300 1/4W
R31	327721			RESISTOR, 4.7 MEG 1/4W
R32	324902			RESISTOR, 100K 1%
R33	321508			RESISTOR, 100K 1/4W
R34	321213			SAME AS R7
R35	341596			SAME AS R28
R36	321508			SAME AS R33
R37	401067			RESISTOR, 2400 .5%
R38	324908			RESISTOR, 30.1K 1%
R39	320275			SAME AS R5
R40	330641			RESISTOR, 1 MEG, 1/4W
R41	320276			SAME AS R15

REF DESIG	PART NO.	REQ	Q_{TY}	DESCRIPTION
R42	320276			SAME AS R15
R43	320276			SAME AS R15
R44	321213			SAME AS R7
R45	401067			SAME AS R37
R46	321508			SAME AS R33
R47	315988			RESISTOR, 27K 1/4W
R48	321213			SAME AS R7
R49	430719			RESISTOR 25.8K .5%
R50	401067			SAME AS R37
R51	320275			SAME AS R5
R52	318803			RESISTOR, 2400 1/4W
R53	321258			RESISTOR, 20K 1/2W
R54	315956			RESISTOR, 2700 1/4W
R55	318803			SAME AS R52
R56	401067			SAME AS R37
R57	315956			SAME AS R54
R58	336697			RESISTOR, 430 1/4W
R59	318803			SAME AS R52
R60	315961			RESISTOR, 8200 1/4W
R61	401067			SAME AS R37
R62	320026			RESISTOR, 3900 1/4W
R63	318803			SAME AS R52
R64	320275			SAME AS R5
R68	315955			SAME AS R13
RT1	430707			THERMISTOR
RV1	430708			VARISTOR
ST1	336470			STRAP
ST2	336470			STRAP
ST3	336470			STRAP
T1	430702			TRANSFORMER, POWER
T2	430703			TRANSFORMER, PULSE

NOTES:

FOR NOTES 1 TO 11 SEE SHEET 1.

12. USE DRAWING 410700 (2) & ASSOCIATED 4700SD SHEETS 85, 86 & 87 WITH 409700 BOARD ISSUE 4 OR LATER
13. THROUGH CUSTOMER IDENTIFICATION ISSUE 5A CAPACITOR C13 USED PART NO. 430705. IF REPAIR REQUIRES REPLACEMENT OF C13 USE PART NO. 430738 PLUS A WIRE STRAP, AND INSTALL AS FOLLOWS (USING EXISTING HOLES IN BOARD):



REVISIONS

CUSTOMER IDENTIFICATION ISSUE	MFG VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.

CIRCUIT CARD

CC 700

POWER SUPPLY CARD

P

APPROVALS

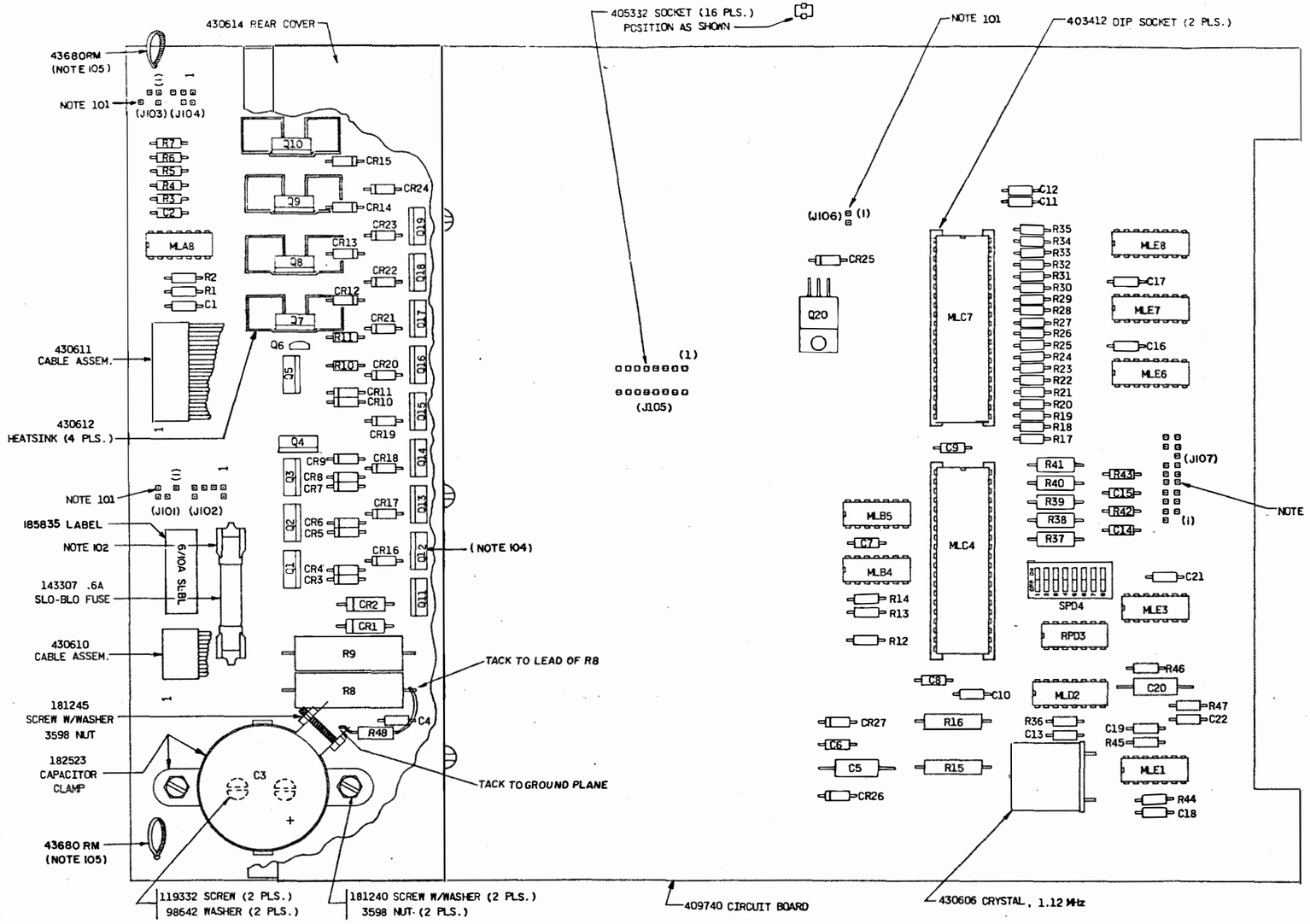
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR. DLS		DSGNR. EAK
DRAWN JA		DATE
E – NUMBER		
SD – CD NO		
R & D FILE NO.		

TELETYPE

410700 (2)

TC 661-1174

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
C1	300057		CAPACITOR, .01 MFD
C2	335901		CAPACITOR, 22 PFD
C3	430607		CAPACITOR, 1500 MFD
C4	405324		CAPACITOR, .1 MFD
C5	337333		CAPACITOR, 22 MFD
C6			SAME AS C4
C7			SAME AS C4
C8			SAME AS C4
C9			SAME AS C4
C10			SAME AS C4
C11			SAME AS C4
C12			SAME AS C4
C13			SAME AS C4
C14	323714		CAPACITOR, 470 PFD
C15			SAME AS C14
C16			SAME AS C4
C17			SAME AS C4
C18			SAME AS C1
C19	346238		CAPACITOR, 33 PFD
C20			SAME AS C5
C21			SAME AS C4
C22			SAME AS C4
R1	321508		RESISTOR, 100K, 1/4W
R2	319803		RESISTOR, 2.4K, 1/4W
R3	333412		RESISTOR, 180K, 1/4W
R4			SAME AS R2
R5	321545		RESISTOR, 12K, 1/4W
R6			SAME AS R1
R7	318802		RESISTOR, 220, 1/4W
R8	171521		RESISTOR, 100, 5W
R9			SAME AS R8
R10	315956		RESISTOR 2.7K, 1/4W
R11	321545		RESISTOR, 12K, 1/4W
R12	300092		RESISTOR, 6.8K, 1/4W
R13			SAME AS R12
R14			SAME AS R12
R15	310988		RESISTOR, 150, 1W
R16	171469		RESISTOR, 100, 1W
R17	315972		RESISTOR, 22K, 1/4W
R18			SAME AS R17
R19			SAME AS R17
R20			SAME AS R17
R21			SAME AS R17
R22			SAME AS R17
R23			SAME AS R17
R24			SAME AS R17
R25			SAME AS R17
R26			SAME AS R17
R27			SAME AS R17
R28			SAME AS R17
R29			SAME AS R17
R30			SAME AS R17
R31			SAME AS R17
R32			SAME AS R17
R33			SAME AS R17
R34			SAME AS R17
R35			SAME AS R17
R36	320276		RESISTOR, 470, 1/4W
R37	137440		RESISTOR, 1K, 1/2W
R38			SAME AS R37
R39			SAME AS R37
R40			SAME AS R37
R41			SAME AS R37
R42	321213		RESISTOR, 1K, 1/4W
R43			SAME AS R42
R44	320275		RESISTOR, 10K, 1/4W
R45			SAME AS R44
R46			SAME AS R10
R47			SAME AS R44
R48	116186		RESISTOR 5.6K 1/2W
CR1	400923		DIODE, 1N5350A
CR2			SAME AS CR1
CR3	312341		DIODE, 1N4004
CR4			SAME AS CR3
CR5			SAME AS CR3
CR6			SAME AS CR3
CR7			SAME AS CR3
CR8			SAME AS CR3
CR9			SAME AS CR3
CR10	430605		DIODE, 1N4936
CR11			SAME AS CR10



REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
CR12			SAME AS CR10
CR13			SAME AS CR10
CR14			SAME AS CR10
CR15			SAME AS CR10
CR16			SAME AS CR3
CR17			SAME AS CR3
CR18			SAME AS CR3
CR19			SAME AS CR3
CR20			SAME AS CR3
CR21			SAME AS CR3
CR22			SAME AS CR3
CR23			SAME AS CR3
CR24			SAME AS CR3
CR25			SAME AS CR3
CR26	346394		DIODE, 1N4730A
CR27	312922		DIODE, 1N4733A
Q1	430604		TRANSISTOR, 80V NPN DARL

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
Q2			SAME AS Q1
Q3			SAME AS Q1
Q4			SAME AS Q1
Q5	430608		TRANSISTOR, 40V PNP DARL
Q6	334133		TRANSISTOR, 2N4410
Q7			SAME AS Q1
Q8			SAME AS Q1
Q9			SAME AS Q1
Q10			SAME AS Q1
Q11			SAME AS Q1
Q12			SAME AS Q1
Q13			SAME AS Q1
Q14			SAME AS Q1
Q15			SAME AS Q1
Q16			SAME AS Q1
Q17			SAME AS Q1
Q18			SAME AS Q1

REF. DESIG.	PART NO. REQ.	QTY	DESCRIPTION
Q19			SAME AS Q1
Q20			SAME AS Q1
MLA8	404324		IC, QUAD OP AMP
MLB4	339417		IC, HEX BUFFER
MLB5	474004		IC, HEX INVERTER
MLC4	420651		IC, MACON (TML)
MLC7	420601		IC, MAPL (TML)
MLD2	331109		IC, DUAL JK FF
MLE1	339380		IC, QUAD NOR
MLE3	339417		IC, HEX BUFFER
MLE6	404050		IC, HEX BUFFER
MLE7			SAME AS MLE6
MLE8			SAME AS MLE6
RPD3	341733		MODULE, RESISTOR 6.8K
SPD4	341838		SWITCH, 8 POS DIP

NOTES:

101. 341618 PIN CONNECTOR (39 PLS.)

102. 340269 FUSE CLIP, 2 PLS., FASTEN WITH 336473 RIVET, 2 PLS..

103. CONNECTOR DESIGNATIONS IN PARENTHESES ( ) ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON THE CARD.

104. BODY OF TRANSISTOR Q1 TO Q5, AND Q7 TO Q19, TO BE SPACED .125 TO .250 INCH ABOVE BOARD.

105. 43680 RM STRAP TO BE FORMED TO APPROX. 1" DIA. (TOP SIDE) AND FREE END CUT TO WITHIN 1/32" OF HOUSING ON BOTTOM SIDE.

REVISIONS

CUSTOMER IDENTIFICATION ISSUE	MFG. VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.
1	A		1	7-26-76	24576R
1	A		2	8-16-76	16673
1	A		3	11-23-76	16429-1
1	B		4		16835
1	B		5	—	8619

FOR CUSTOMER I.D. 2A AND ABOVE SEE SHEET 2

CIRCUIT CARD

CC 740

M43 LOGIC CARD ASSEMBLY

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL
JFB 6-22-76		

ENGR. N.C.K.	DSGNR.
DRAWN	DATE
PROD. NO.	410740
SD-CD NO.	4740
R&D FILE NO.	1-30,171,234

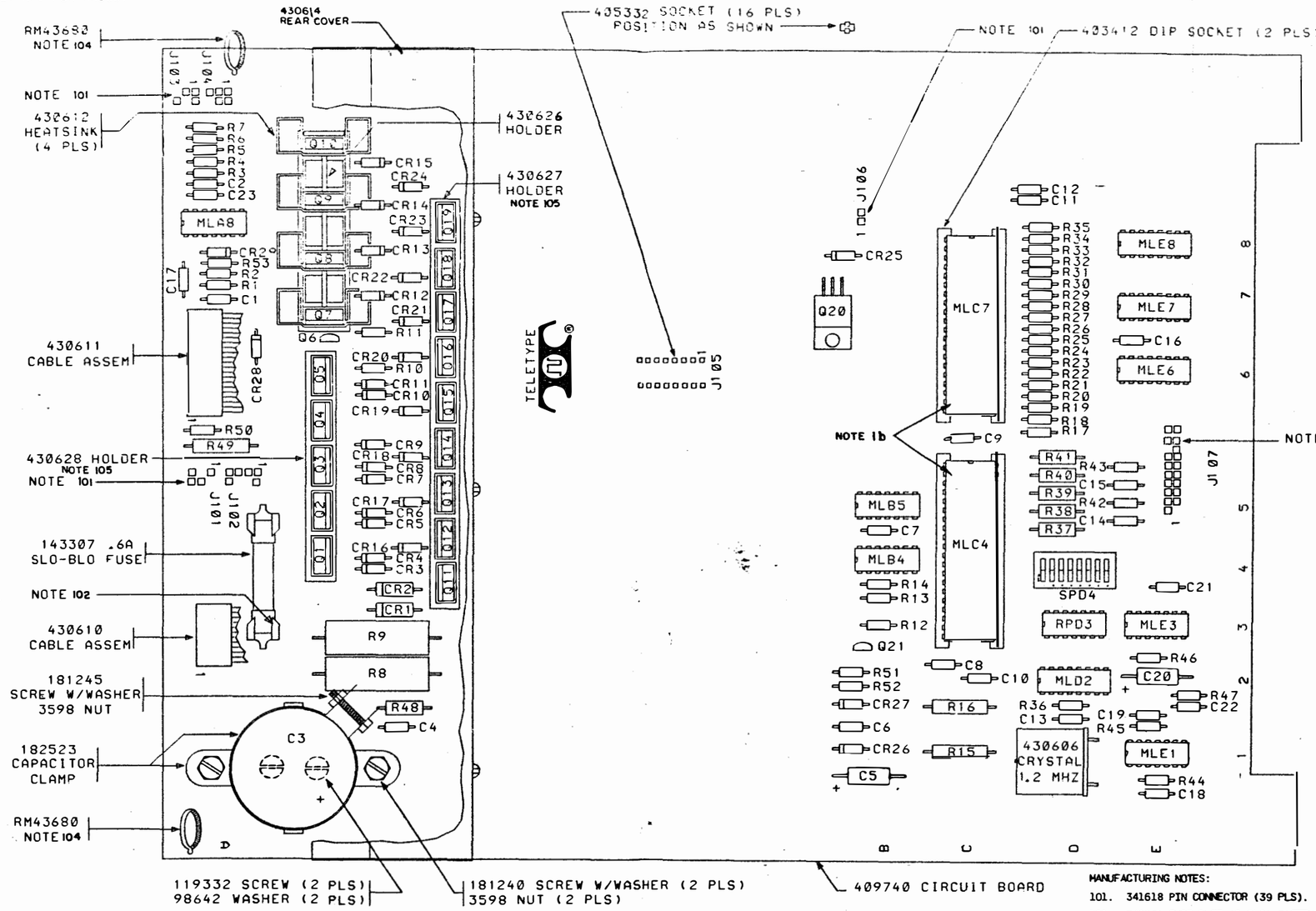
TELETYPE

410740 (1)

TC 637-0173

REF DESIG	PART NO REQ	QTY	DESCRIPTION
C1	325057		CAPACITOR, .01 MFD
C2	335621		CAPACITOR, 22 MFD
C3	430623		CAPACITOR, 1500 MFD
C4	405324		CAPACITOR, .1 MFD
C5	337333		CAPACITOR, 22 MFD
C6			SAME AS C4
C7			SAME AS C4
C8			SAME AS C4
C9			SAME AS C4
C10			SAME AS C4
C11			SAME AS C4
C12			SAME AS C4
C13			SAME AS C4
C14	323714		CAPACITOR, 470 PFD
C15			SAME AS C14
C16			SAME AS C4
C17			SAME AS C4
C18			SAME AS C1
C19	346238		CAPACITOR, 33 PFD
C20			SAME AS C5
C21			SAME AS C4
C22			SAME AS C4
C23			SAME AS C4
R1	321508		RESISTOR,100K,1/4W
R2	318803		RESISTOR,2.4K,1/4W
R3	333412		RESISTOR,180K,1/4W
R4			SAME AS R2
R5	321545		RESISTOR,12K,1/4W
R6			SAME AS R1
R7	318802		RESISTOR,220,1/4W
R8	171521		RESISTOR,100,5W
R9			SAME AS R8
R10	315956		RESISTOR,2.7K,1/4W
R11			SAME AS R5
R12	300092		RESISTOR,6.8K,1/4W
R13			SAME AS R12
R14			SAME AS R12
R15	310988		RESISTOR,150,1W
R16	171469		RESISTOR,100,1W
R17	315972		RESISTOR,22K,1/4W
R18			SAME AS R17
R19			SAME AS R17
R20			SAME AS R17
R21			SAME AS R17
R22			SAME AS R17
R23			SAME AS R17
R24			SAME AS R17
R25			SAME AS R17
R26			SAME AS R17
R27			SAME AS R17
R28			SAME AS R17
R29			SAME AS R17
R30			SAME AS R17
R31			SAME AS R17
R32			SAME AS R17
R33			SAME AS R17
R34			SAME AS R17
R35			SAME AS R17
R36	320276		RESISTOR,470,1/4W
R37	137440		RESISTOR,1K,1/2W
R38			SAME AS R37
R39			SAME AS R37
R40			SAME AS R37
R41			SAME AS R37
R42	321213		RESISTOR,1K,1/4W
R43			SAME AS R42
R44	320275		RESISTOR,10K,1/4W
R45			SAME AS R44
R46			SAME AS R10
R47			SAME AS R44
R48	118186		RESISTOR,5.6K,1/2W
R49	341596		RESISTOR,121K,1/8W
R50	324902		RESISTOR,100K,1/8W
R51			SAME AS R7
R52			SAME AS R44
R53	326601		RESISTOR,150K,1/4W

NOTE. MFG PER MR2001



REF DESIG	PART NO REQ	QTY	DESCRIPTION
CR1	400923		DIODE,IN5360A
CR2			SAME AS CR1
CR3	312341		DIODE,IN4004
CR4			SAME AS CR3
CR5			SAME AS CR3
CR6			SAME AS CR3
CR7			SAME AS CR3
CR8			SAME AS CR3
CR9			SAME AS CR3
CR10	430605		DIODE,IN4936
CR11			SAME AS CR10
CR12			SAME AS CR10
CR13			SAME AS CR10
CR14			SAME AS CR10
CR15			SAME AS CR10
CR16			SAME AS CR3
CR17			SAME AS CR3
CR18			SAME AS CR3

REF DESIG	PART NO REQ	QTY	DESCRIPTION
CR19			SAME AS CR3
CR20			SAME AS CR3
CR21			SAME AS CR3
CR22			SAME AS CR3
CR23			SAME AS CR3
CR24			SAME AS CR3
CR25			SAME AS CR3
CR26	346394		DIODE,IN4730A
CR27	320010		DIODE,ZENER,1%
CR28	177108		DIODE,D2
CR29			SAME AS CR28
Q1	430604		TRNSTR,80V,NPN,DARL
Q2			SAME AS Q1
Q3			SAME AS Q1
Q4			SAME AS Q1

REF DESIG	PART NO REQ	QTY	DESCRIPTION
Q5	430608		XISTOR,40V,PNP,DARL
Q6	334133		XISTOR,2N4410
Q7			SAME AS Q1
Q8			SAME AS Q1
Q9			SAME AS Q1
Q10			SAME AS Q1
Q11			SAME AS Q1
Q12			SAME AS Q1
Q13			SAME AS Q1
Q14			SAME AS Q1
Q15			SAME AS Q1
Q16			SAME AS Q1
Q17			SAME AS Q1
Q18			SAME AS Q1
Q19			SAME AS Q1
Q20			SAME AS Q1
Q21	325077		XISTOR,60V,PNP

REF DESIG	PART NO REQ	QTY	DESCRIPTION
MLA8	404324		IC,QUAD OP AMP
MLB4	339417		IC,HEX BUFFER
MLB5	474304		IC,HEX INVERTER
MLC4	430671		IC,MACON (TML)
MLC7	430641		IC,MAPL (TML)
MLD2	339109		IC,DUAL JK FF
MLE1	339380		IC,QUAD NOR
MLE3	339417		IC,HEX BUFFER
MLE6	484250		IC,HEX BUFFER
MLE7			SAME AS MLE6
MLE8			SAME AS MLE6
RPD3	341733		MODULE,RES, 6.8K
SPD4	341808		SWITCH,8 POS DIP

MANUFACTURING NOTES:

101. 341618 PIN CONNECTOR (39 PLS).
102. 340269 FUSE CLIP (2 PLS) FASTEN WITH 336473 RIVET (2 PLS)
103. .025 INCH DOT NEXT TO DIODE REPRESENTS CATHODE.
104. RM43680 STRAP TO BE FORMED TO APPROX. 1" DIA.(TOP SIDE) AND FREE END CUT TO WITHIN 1/32" OF HOUSING ON BOTTOM SIDE.
105. 430627 AND 430628 HOLDER SHOULD BE POSITIONED SUCH THAT IT IS APPROXIMATELY FLUSH WITH THE BOARD.

NOTES: 1. a- CIRCUIT ASSM CHANGED AT CUSTOMER ID ISS.2 TO ADD P.O.R. CIRCUITRY FOR MACON AND MAPL AND TO IMPROVE NOISE IMMUNITY SHEET 2 REFLECTS CHANGE.

b- ADD NEW MACON (430671) AND MAPL (430641).

c- 409740 BOARD ISSUE 2A OR LATER INCLUDES THIS CHANGE. REFER TO 4740SD SHEET 7 ISS.4

SCALE 3/2

REVISIONS

CUSTOMER IDENTIFICATION ISSUE	MFG VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.
2	A	1	6	9-1-77	18619

CIRCUIT CARD

CC740

M43 LOGIC CARD ASSEMBLY

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.

ENGR.	W.C.K.	DSGNR.	G.B.O.
DRAWN	R.O.K.	DATE	4-25-77

PROD. NO. 410740
SO-CO NO. 4740
R & D FILE NO. 1-30.171.234

TELETYPE

410740 (2 of 2)

TC 637-0173

SHEET INDEX AND ISSUE CONTROL

4700CD

Sheet 1

CIRCUIT DESCRIPTION FOR 430700 POWER SUPPLY

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	7/1/76	24599R

SHEET ISSUE NUMBER

SHEET NUMBER													
1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	1	1	1	1	1	1	1	1	1	1	1	1	1

APPROVALS

ENG.	DSGNR.	DRN.
FPK		

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.	DATE	S-NUMBER
1-1-76	7-1-76	DM		4700SD

RAD FILE NO.	E-NUMBER
1-30.171.211A	4700CD

TELETYPE

32-1272

CIRCUIT DESCRIPTION FOR 430700 POWER SUPPLY

TABLE OF CONTENTS

SECTION I - GENERAL TECHNICAL DATA

1. PURPOSE

1.1 The 430700 Power Supply is designed to provide the DC power required to operate the basic Model 43 KSR Set consisting of the Model 43 Printer, OPCON, Controller, and Terminal Data Unit (TDU) or Terminal Auxiliary Unit (TAU). Line input power may be 115 VAC ± 10%, 58/62 hertz or 165 VDC ± 10%. Four regulated DC output voltages are produced; +5V, +12V -12V, +42V.

1.2 The input and output ratings are as follows:

Input: 115VAC, ±10%, 58/62 Hz - 0.9 amp

Output: +5 VDC ± 8% - 0.75A
+12 VDC ± 7% - 0.4A
-12 VDC ± 7% - 0.4A
+42 VDC ± 8% - 1.0A (Average)

1.3 All circuitry for the 430700 Power Supply is contained on the 410700 Power Supply Card. This card and associated heat sinks, brackets, and covers are assembled to form the 430700 Power Supply unit which is mounted in the cabinet rear frame. Line power is applied to the unit through a cable having a three terminal connector. A line fuse is provided in the cabinet rear frame adjacent to the ON/OFF switch. The output is available through a 10 pin connector located at the top edge of the circuit card in the supply.

2. OPERATION

2.1 The 430700 Power Supply is of the "Off-the-Line" Switching Regulator type utilizing a "Ringing Choke" design to accomplish power conversion at a nominal frequency of 20 KHz. This design provides a relatively high power conversion efficiency, and minimizes the size and weight of the supply.

2.2 The AC line voltage is directly converted to DC by a bridge rectifier connected directly to the AC input and filtered by a capacitor on the output side of the bridge rectifier. The primary of a power transformer is connected to the DC source in series with a primary switching transistor. In operation, the transistor is driven into conduction for a controlled period of each cycle during which the current in the primary increases. During the remainder of the cycle, the transistor is non-conducting, but the energy stored in the primary inductance is transferred to four secondary windings. The secondaries each contain a semiconductor diode which provides half wave rectification.

2.3 The +5V, +12V and -12V outputs are derived from three separate windings which drive integrated circuit voltage regulators. These regulators are of the linear type.

2.4 The +42V output is derived from the fourth secondary winding. This output is sensed by a feedback circuit which controls the conduction period of the primary switching transistor so that the output is regulated to the correct voltage in response to line and load variations. A more detailed description of operation is contained in Section II.

2.5 The Protective Ground is not connected to the Primary Circuit ground. Care must be exercised during trouble shooting to prevent direct connection of these grounds because this will effectively by-pass one of the bridge rectifier diodes and cause full line voltage to be directly applied to another diode in the forward direction. This rectifier and other line components will fail under this condition.

2.6 The secondary voltage returns are tied together and directly connected to the Protective Ground. However, isolation is maintained between the AC line and the secondary circuits.

3. SUPPORTING INFORMATION

4700SD - Schematic Diagram
62,097S - Specification

SECTION II - DETAILED DESCRIPTION AND THEORY OF OPERATION

1. GENERAL

1.1 Operating Modes

1.1.1 During normal operation, the 430700 Power Supply functions as a fixed frequency, pulse width modulated switching regulator. However, whenever power is initially applied, the oscillator and control circuitry which are on the secondary side of the main power transformer, T1, are not operational. An auxiliary mode of operation is provided which is operational only during start-up while the oscillator and control circuitry are non-operating. In this auxiliary mode, the primary switching transistor is driven by an extra winding on transformer T1 which is connected such that positive feedback is provided to its base. This results in a blocking oscillator like mode of operation during start-up.

1.1.2 Operation of the Power Supply in the power-up mode results in energy transfer to the secondary windings so that the oscillator and control circuitry, which are powered from the unregulated voltage which drives the +12V Regulator, will commence operation. With a low secondary voltage, the control circuitry provides a maximum pulse width which is constrained to be slightly less than 50% of a cycle. Whenever the oscillator drive has gained sufficient amplitude to reliably drive the primary switching transistor, the blocking oscillator action is automatically terminated and operation continues under oscillator driven control.

1.2 Features

1.2.1 An RFI filter is included in the AC line input to reduce conducted interference resulting from the use of a switching regulator "Off-the-Line".

1.2.2 In-rush currents on start-up are controlled by the use of a series line resistance and by a current limited drive on start-up.

1.2.3 AC line transient protection has also been provided which both tends to limit peak voltages as well as suppress the transfer of the transient to the secondary circuits.

1.2.4 An Output voltage detector circuit is included which will light an LED indicator only whenever all four secondary output voltages are present, although not necessarily within tolerance. This indicator may be viewed for maintenance purposes without removal of the unit.

1.2.5 The +5V, +12V, -12V logic voltages are automatically protected against accidental load shorts and recover upon removal of the short. The +42V is also protected against load shorts by means of a fuse in the output.

1.2.6 All outputs are protected against sustained overvoltages. Detecting circuitry monitors each output and in the event of a fault, the oscillator drive is immediately removed so that the secondary circuits are no longer powered.

2. POWER UP MODE

2.1 AC Line Input (FS-1)

2.1.1 Nominal input voltage (115 VAC) is applied to connector J202. The hot side of the line is applied to terminal #1. Protective earth ground is applied to terminal #2,and line neutral to terminal #3 of J202.

2.1.2 An R.F.I. filter, FL1, reduces conducted interference entering and leaving the power supply.

2.1.3 Thermistor RT1 is in the hot side of the line to limit initial inrush current into capacitor C1. Initial resistance of RT1 is 2.5 ohms which after the supply is operational reduces to approximately 1.0 ohm due to self heating.

2.1.4 The transient protector RV1 is a voltage clamping device to limit the potential applied to primary circuits of the power supply. RV1 avalanches at approximately 150 VAC (RMS), limiting the voltage applied to other devices.

2.2 AC Line Rectifier

2.2.1 AC to DC rectification occurs through the full wave bridge consisting of the four diodes CR1, CR2, CR3 and CR4. Capacitor C1 filters the DC.

2.2.2 The anodes of CR3 and CR4 and the negative end of C1 are connected to a common buss for all primary circuits. This buss is not to be confused or connected with any ground buss on the secondary circuits unless the power supply is floated through an isolation transformer. Grounding of the primary buss might cause distruction of diode CR3, as well as thermistor RT1.

2.3 Blocking Oscillator Operation (FS-2)

2.3.1 Upon initial application of DC voltage to R3, current flows to charge C2. The time constant of R3 and C2 delays the start-up until capacitor C1 is fully charged.

2.3.2 The voltage across C2 biases the base of Q1 into the active region by applying DC potential through R8, terminal (J, H) of P2 and diode CR11. This causes current to flow into the base of Q1 tending to turn it on. As Q1 turns on, terminal L of P1 is forced toward primary buss common. Since Q1 turns on, terminal L of P1 is forced toward primary buss common. Since coil P1 is tightly coupled to P2 an equivalent potential is applied across P2 according to the dot notation shown. R15 is a base bias resistor for Q1.

2.3.3 A portion of P2 is tapped at J to act as a source to further drive the base of Q1 toward saturation. Regenerative action occurs because of positive feedback driving Q1 into saturation.

2.3.4 Base drive into Q1 is limited by resistor R8. The Q1 collector current ramps up due to the magnitizing inductance of T1. This current is limited by the gain hFE of Q1. For constant current base drive, Q1 remains in saturation until IC exceeds hFE times I_B.

2.3.5 As Q1 comes out of saturation voltage across J-H is reduced, lowering the base drive to Q1. Regenerative action occurs forcing Q1 off. Q1 remains off until the energy in T1 collapses via dumping energy into the secondaries (S1, S2, S3, S4). The cycle then repeats itself until the pulse width modulator mode takes over.

2.4 Snubing Circuit (FS-2)

2.4.1 The snubing network consisting of coil P2 and diodes CR14 and CR12, clamp the collector of transistor Q1 during turn off to twice the DC supply voltage. During turn off terminal L of P1 exceeds the potential at terminal G due to the inductive kick of the transformer T1. The potential across terminals L-G is mirrored on terminals K-H by observing the dot notation polarity.

2.4.2 Upon turn off terminal K becomes more positive than +VDC in and is clamped by CR14. Terminal H becomes more negative than the -VDC buss common. This forces a clamping of coil P2 which reflects to coil P1 due to tight coupling. The voltage on the collector of Q1 is limited to that across P2 or twice V_{IN}. Diode CR7 prevents capacitor C2 from being reversed biased.

3. OSCILLATOR DRIVEN MODE

3.1 20 KHz Square Wave Oscillator

3.1.1 During start-up, the secondaries of T1 receive a limited amount of power which results in an increasing rectified voltage. The oscillator is fabricated from one of the comparators in ML2 which derives its power from the unregulated +16V supply used to power the +12V linear regulator. As this voltage increases to approximately 4 volts, oscillation commences.

3.1.2 If the oscillator output (Pin 2) has just switched to ground, the voltage at the non-inverting input (Pin 5) will be determined by the divider of R35 and R28 in parallel with R32. This voltage is 31% of the +16V supply. The voltage on the inverting input (Pin 4) discharges toward ground at a rate determined by R38 and C11. As this voltage drops to 31% of the +16V supply, the comparator output switches to the high state. Now, the voltage on Pin 5 is essentially determined by the divider of R28 in parallel with R35 and R32. This voltage is 62% of the +16V supply. The voltage or Pin 4 charges toward the +16V supply at a rate determined by R30 and R38 in series, and C11. As this voltage now reaches 62% of the +16V supply, the comparator output (Pin 2) switches to the low state.

3.1.3 Since the comparator switch points are a fixed ratio of the +16V supply, the frequency will be virtually independent of the actual voltage of the +16V supply. In fact, from approximately +4 to +20 volts, the frequency and duty cycle are essentially constant.

3.2 Ramp Generator (FS-4)

3.2.1 The Ramp Generator is fabricated from a second comparator of ML2. The inverting input (Pin 8) of ML2 is biased to approximately 50% of the +16V supply by a divider composed of R33 and R36. The output of the 20KHz Square Wave Oscillator is connected to the non-inverting input (Pin 9). Whenever the oscillator output is low, the output (Pin 14) is held in the low state. The voltage capacitor C10 is held low during this time.

3.2.2 Whenever the oscillator output goes to the high state, the output of the Ramp Generator is unclamped. The voltage on C10 begins to charge toward the +16V supply by means of resistor R29. The voltage reaches approximately 3.5 volts during the time that the oscillator output is high. Whenever the oscillator output goes to the low state, C10 is discharged and the Ramp voltage goes to a few tenths of a volt above ground.

3.3 Pulse Width Modulator (FS-4)

3.3.1 A third section of ML2 is used for a Pulse Width Modulator. The output of the Ramp Generator is connected to the non-inverting input (Pin 11) by means of Resistor R39. The inverting input (Pin 10) is connected to a divider network consisting of R47 and R48 which derives a bias of approximately 0.6 volt from the +16V supply.

3.3.2 In the absence of any output from Pin 9 of ML3, the bias voltage of 0.6 volt appears on Pin 10 of ML2. Consequently, whenever the Ramp Generator output is low, the Pulse Width Modulator output (Pin 13) will be low shunting any current flowing through R25. Whenever the Ramp Generator output exceeds the bias voltage, the Pulse Width Modulator will go to a high state. Any current flowing through R25 will now be available to drive the base of transistor Q10.

3.3.3 Resistor R25 is connected to the +16V supply through 4-Layer Diode CR21. This diode is non-conducting until the +16V supply exceeds approximately 8 volts, at which point the diode triggers into conduction with a drop of approximately one volt. During start-up, even-though the oscillator is running and the Pulse Width Modulator producing drive pulses, transistor Q10 will not receive drive pulses until CR21 becomes conducting.

3.3.4 Whenever an output is produced on Pin 9 of ML3 that exceeds the 0.6 volt bias, the pulse width of the output on Pin 13 of ML2 will be reduced. The Pulse Width Modulator output will be in the high state for the time that the Ramp Generator output exceeds the voltage produced on Pin 9 of ML3.

3.3.5 Resistor R40 is connected between the Ramp Generator output and the non-inverting input to provide hysteresis and snap-action switching. Resistor R24 provides a base leakage path for transistor Q10.

3.4 Voltage Reference and Error Amplifier (FS-4)

3.4.1 The Voltage Reference and Error Amplifier is contained in ML3, a Type 723 Precision Regulator. The voltage reference, V_{REF} (Pin 6), is nominally 7.15 volts with a 5% tolerance. This voltage is applied to a precision divider consisting of R37 and R55 to provide a 3.57 volt reference which is applied to the inverting input (Pin 4) of the Error Amplifier.

3.4.2 The +42 volt rectified DC output is connected to a precision divider consisting of R49 and R50. The resulting voltage is applied to the non-inverting input (Pin 5) of the Error Amplifier. In operation, the voltage at Pin 5 is very close to that at Pin 4. Frequency compensation of the Error Amplifier is accomplished by connection of capacitor C15 between the compensation terminal (Pin 13) and the inverting input (Pin 4).

3.4.3 The full DC gain of the Error Amplifier is utilized to produce the control signal at Pin 9. However, the AC gain of the Error Amplifier is reduced by the use of negative feedback from the direct output at Pin 10 through resistor R46 and capacitor C16. Capacitor C17 is used to by-pass any high frequency noise in proximity to the Error Amplifier.

3.5 Primary Power Conversion

3.5.1 As previously noted, the 20 KHz Oscillator will commence operation and produce drive pulses to the base of transistor Q10 whenever the +16V supply exceeds approximately 8 volts. At this point, the pulse transformer T2, in the collector of Q10 will be driven so as to produce a positive pulse of similar duration on its secondary. This pulse is connected through resistor R18 and diode CR10 to the base of the primary switching transistor, Q1.

3.5.2 The positive drive on the base of Q1 causes current to flow in the collector of Q1 and the primary winding (P1) of transformer T1. The current increases, linearly during the duration of the pulse, from its initial value to its final value which is dependent upon the pulse width as well as the DC supply voltage. Diode CR13 effectively prevents Q1 from reaching full saturation, reducing the storage time for Q1.

3.5.3 The positive pulses are also connected through diode CR9 which rectifies the signal to produce a DC signal on capacitor C4 and bleeder resistor R14. When the power supply begins operating in the oscillator driven mode, the DC signal is connected through diode CR8 and resistor R9, to the base of transistor Q7. The collector of Q7 is connected to the feedback winding used to provide the blocking oscillator action. Turning Q7 on will short the signal produced by the feedback winding and effectively inhibit blocking oscillator action. This control is automatically transferred from the start-up mode to the oscillator driven mode.

3.5.4 Whenever the drive to the base of Q10 is shunted by the Pulse Width Modulator, the drive pulse is terminated. The collector of Q10 rises from the saturated value of Q10 to a voltage above the +16V supply. This results in a negative pulse on the secondary of T2. This pulse is connected through resistor R22 to the base of transistor Q5. Transistor Q5 is turned on which effectively grounds the base of Q1. The stored base charges in Q1 is discharged through Q5 resulting in rapid turn-off of Q1.

3.5.5 When Q1 turns OFF, the energy which was stored in the magnetic core of T1, is transferred to the secondary windings. Each winding is driven in proportion to its relative turns ratio.

3.6 Feedback Regulation (FS-4)

3.6.1 As DC line power is transferred to the secondary circuits, the rectified secondary voltages increase. The +42V supply is sensed by means of divider R49 and R50 and compared in the Error Amplifier with the voltage reference established by divider R37 and R45. Whenever the sensed voltage exceeds the reference voltage, the Error Amplifier output (Pin 9) is increased which has the effect of reducing the pulse width supplied to drive Q1. As a result, the net energy transferred to the secondary is reduced. This also causes the rectified secondary voltages to decrease. Consequently, the +42V supply is regulated against line and load changes. In addition, the remaining three secondaries are also regulated against line changes and to some extent, load changes, to the degree that they are reflected in the +42V supply voltage.

3.6.2 The +42V supply is derived from a secondary winding of T1. The voltage on winding S1 is half-wave rectified by diode CR17 and filtered by capacitor C13. A bleeder resistor R26 is provided to discharge C13.

3.6.3 The +42V supply is connected through fuse F1, a 1 amp fast acting device, to terminals 1 and 3 of connector J201. The return for the +42V supply is made through terminals 9 and 10 of J201. It is also connected to the logic supply secondary return.

3.7 Optical Coupler (FS-2)

3.7.1 The purpose of the optical coupler is to deactivate the blocking oscillator mode of operation used for start-up in the event there is a failure in the oscillator drive and/or regulating control loop. Under light loads, the secondary voltages may substantially exceed their ratings during this condition. The over voltage protective circuitry which functions by inhibiting the clock is not capable of inhibiting the blocking oscillator action.

3.7.2 Whenever the +42V supply voltage exceeds approximately 30 volts, a zener diode, CR20 will conduct and drive the LED in optical isolator ML1. Resistor R27 limits the current through the diode.

3.7.3 The phototransistor in ML1 in conjunction with transistor Q3 forms a latch on the AC line side of the power supply. Whenever the latch is OFF, a voltage appears on the emitter of Q3 which is the result of a fixed drop across the zener diode CR5, and a divider consisting of R1 and R6. Capacitor C3 filters noise appearing on the emitter. As the associated LED in the optical isolator is driven into emission of light, the phototransistor conducts current through resistor R12 which is connected to the base of Q3. This base current causes collector current to flow through Q3 which in turn drives the base of the phototransistor by means of resistor R11 and the base of transistor Q7 by means of resistor R10. Transistor Q3 becomes latched so that in the event that the LED in the isolator loses its drive, transistor Q7 will continue to be driven. Resistor R14 provides base stabilization for the phototransistor, and capacitor C5 filters noise transients to prevent spurious triggering of the latch.

3.7.3 Zener diode CR5 is provided to permit the latch to clear whenever the rectified primary DC voltage drops below approximately 50 volts and the +42V supply below 30V. This allows the power supply to automatically restart under the blocking oscillator mode of operation if the oscillator driven mode has also become inoperative.

3.8 Primary Circuit Overcurrent Protection (FS-2)

3.8.1 A resistor, R4, in the emitter of the primary switching transistor, Q1, senses the current conducted during each pulse drive period. If this current should exceed a safe level, the base drive current is shunted for the remainder of that drive pulse.

3.8.2 The voltage developed on R4 is applied through resistor R19 to capacitor (6) which acts to filter spurious transients, to R17 which is in series with the base of transistor Q8, and to the base of transistor Q4. Whenever the voltage developed is high enough to cause Q8 to conduct sufficient current through the collector resistor, R20, which is connected through diode CR15 to the drive pulse transformer T2, to bias transistor Q9 into conduction, a regenerative action is initiated. This allows current to flow through the emitter resistor, R21, of Q9. The current drives both the base of Q8 and the base of Q4. Whenever Q4 conducts, the base drive current to Q1 is shunted to the primary common, effectively terminating the primary switching transistor current pulse for that cycle. Whenever the drive pulse from transformer T2 terminates, transistors Q8, Q9 and Q4 are returned to their non-conducting state.

3.9 Primary Circuit Overvoltage Protection (FS-4)

3.9.1 In the event that a transient spike occurs on the AC line that exceeds the normal voltage range, circuitry has been provided which will maintain the primary switching transistor in the non-conducting state even through base drive pulses are being generated. This protection is accomplished by shunting the oscillator drive pulses during the transient.

3.9.2 Zener diode CR6 is connected to the primary DC power through resistor R2. Whenever the DC voltage is high enough to exceed the zener diode voltage, current flows to the base of transistor Q2 by means of resistor R7, and the base of Q6 by means of resistor R16. Base bias resistor R5 serves to bypass leakage current for both Q2 and Q6.

4. LOGIC VOLTAGES (FS-3)

4.1 +5V Supply

4.1.1 The +5V supply is derived from a secondary winding of T1. The voltage on winding S4 is half wave rectified by diode CR16 and filtered by capacitors C7 and C18. This unregulated voltage, +9V, is applied to the base connection (B) of a linear regulator, ML5, which is a self contained three terminal integrated circuit located on a common heat sink with ML6 and ML7. A capacitor, C19, on the output (E) of the regulator filters high frequency load transients.

4.1.2 The +5V supply is connected to terminals 5 and 6 of connector J201 on the power supply. Logic supply return is connected to terminals 9 and 10.

4.2 +12 Volt Supply

4.2.1 The +12V supply is derived from a secondary winding of T1. The voltage on winding S2 is half wave rectified by diode CR19 and filtered by capacitors C9 and C23. This unregulated voltage, +16V, is applied to the base connection (B) of a linear regulator, ML6, which is a self-contained three terminal integrated circuit located on a common heat sink with ML5 and ML7. A capacitor, C22, on the output (E) of the regulator filters high frequency load transients. The +16V supply is also used to drive the oscillator and control circuits.

4.2.2 The +12V supply is connected to terminal 7 of connector J201.

4.3 -12 Volt Supply

4.3.1 The -12V supply is derived from a secondary winding of T1. The voltage on winding S3 is half-wave rectified by diode CR18 and filtered by capacitors C8 and C21. This unregulated voltage, -16V, is applied to the collector connection (C) of a linear regulator, ML6, which is a self-contained three terminal integrated circuit located on a common heat sink with ML5 and ML7. A capacitor, C20, on the output (E) of the regulator, filters high frequency load transients.

4.3.2 The -12V supply is connected to terminal 8 of connector J201.

5. OUTPUT VOLTAGE INDICATOR (FS-3)

5.1 Each DC output voltage has a divider network which senses the output level. The sensed output level is compared with a voltage reference derived by a divider network composed of R56 and R61 from the 7.15 volt reference voltage, V_{REF}, available from ML3. The comparison is done using four comparators in ML4.

5.2 The +5V output voltage sense divider is composed of R58 and R59. The +12V output divider is composed of R62 and R63. The +42V supply is sensed by a divider composed of R52 and R53. The -12V supply is sensed by a divider composed of R55 and R60. These sense voltages are connected to pins 11, 7, 5 and 8 respectively of ML4. The voltage reference is connected to pins 4, 6, 9 and 10.

5.3 The outputs of each comparator (pins 1, 2, 13 and 14) are connected together. Each comparator will go to a high state on the output whenever its sensed input exceeds the reference voltage. If all four comparators outputs are in the high state, then the current which flows through resistor R54 from the +16V supply will be available to drive the LED indicator, CR28. If any output voltage should fail, its associated comparator will go to a low state, shunting the current drive to CR28. Note that the sense divider for the +42V supply is located on the load side of the fuse.

6. FAULT PROTECTION ON SECONDARY

6.1 Short Circuit Protection

6.1.1 The +5V, +12V and -12V supply outputs are protected against short circuits to ground by means of the current limiting characteristics inherent in the integrated circuit voltage regulator which is in each of these outputs. Fault currents are limited to approximately 1.5 amperes. Whenever the fault is removed, the output voltage automatically recovers.

6.1.2 These regulators are also thermally protected so that in the event that their power dissipation in conjunction with the ambient temperature exceeds their limit, automatic shutdown occurs. Whenever the internal temperature decreases to a safe level, the device will reset and restore the output voltage.

6.1.3 The +42V supply is protected against overloads on the output by means of a 1 amp fast blow fuse, F1. Whenever this fuse opens, the Output Voltage Indicator will go dark even though the supply is otherwise functional.

6.2 Overvoltage Protection (FS-4)

6.2.1 Each secondary output voltage has an overvoltage sense circuit which will cause the power supply to shut down whenever an overvoltage is detected on an output. This is accomplished by means of a voltage comparator in integrated circuit ML2 which clamps the 20 KHz Square Wave Oscillator output to the low state, preventing the generation of drive pulses to the primary switching transistor, Q1.

6.2.2 The inverting input (Pin 6) of the comparator is biased by the divider network consisting of R33 and R36 to approximately one-half the voltage of the +16V supply. The non-inverting input (Pin 7) is normally biased to the voltage of the +16V supply by means of R34. An SCR, CR25, is also connected to Pin 7.

6.2.3 A zener diode, CR22, is connected to the +5V supply in series with current limiting resistor, R43, and to the SCR gate bias resistor R44. Whenever the +5V supply voltage reaches a level sufficient for the gate voltage to turn on the SCR, Pin 7 of the comparator is driven below the bias voltage on Pin 6 resulting in a low state on the output, Pin 1. This condition is maintained until the +16V supply drops so low that the oscillator is no longer operational. Capacitor C14 acts as a filter for high frequency transients. Capacitor C12 provides a short time delay on oscillator operation during start-up as well as enhances triggering of the SCR. Resistor R31 is intended to provide snap action during start-up.

6.2.4 The +12V supply is sensed in a similar manner by zener diode CR23 and resistor R42.

6.2.5 The +42V supply is detected in the same manner by zener diode CR24 and resistor R41.

6.2.6 The -12V supply is also sensed, but in a slightly different manner. A zener diode CR27 is connected directly to the base of transistor Q11. Normally, Q11 is biased into saturated conduction by resistor R51 which is directly connected to the +16V supply. Whenever the zener diode voltage is substantially exceeded, the base bias current is shunted so that Q11 becomes non-conducting. While Q11 is saturated, its collector voltage is held low. However, whenever the transistor becomes unsaturated, the collector pull-up resistor, R57, connected to +16V will raise the collector voltage. This voltage is applied through diode CR26 to the gate of CR25, causing the SCR to conduct.

SHEET INDEX AND ISSUE CONTROL

4740CD

Sheet 1

CIRCUIT DESCRIPTION OF THE M43 LOGIC CARD
(BASIC KSR)

REVISIONS		
ISSUE	DATE	AUTH. NO.
1	8-2-76	24598R
2	10-26-77	18760

SHEET ISSUE NUMBER

SHEET NUMBER												
1	2	3	4	5	6	7	8	9	10	11	12	13
1	1	1	1	1	1	1	1	1	1	1	1	–
2	1	1	2	1	1	2	1	1	1	2	2	1

APPROVALS			ENG. WCK	OSGNR.	DRN.	TELETYPE
PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.	DATE 6/28/76		S-NUMBER	
			RAD FILE NO. 1-30.171.234A		E-NUMBER	4740CD

TC482-1272

CIRCUIT DESCRIPTION OF THE M43 LOGIC CARD (BASIC KSR)

TABLE OF CONTENTS

SECTION I - GENERAL TECHNICAL DATA

1. GENERAL DESCRIPTION

1.1 The 410740 M43 Logic Card serves a threefold purpose in the M43 Basic KSR. It provides the control logic for the operator console, line interface and printer functions; it provides the drivers for the printer mechanism; and it serves as a harness card into which all the printer subassemblies are connected.

1.2 The 410740 Card controls all information flow among the three terminal subassemblies - operator console (OPCON), line interface (TAU/TDU) and printer. It retains the present terminal state (e.g., LOCAL/TALK) and determines each new terminal state from incoming OPCON or TAU/TDU information.

1.3 The 410740 Card also provides all the necessary timing and drive levels to cause proper operation of the various printer subassemblies.

2. FEATURES

2.1 Basic KSR Operational Features

The 410740 Card, when part of the basic KSR set, can perform a number of operator accessible features activated from either OPCON or TAU/TDU data streams. Detailed descriptions of these features can be found in the Basic KSR Set Specification.

2.2 Set Configuration Features

An 8 position DIP switch pack is provided to configure the terminal for certain optional functions.

2.2.1 Printer Related Options

Two switches select maximum printer line length. The options available are 72, 80 and 132 column line lengths.

Two switches select graphic character font. The options available are TV, ME and NU fonts.

2.2.2 Line Interface Related Options

One switch enables the automatic new line feature. This feature insures no loss of data received from the TAU/TDU in the event of improper line formatting.

One switch enables the sending of even parity to the TAU/TDU. When disabled the parity bit is forced marking.

One switch enables automatic disconnect of a call upon receipt of the ASCII EOT character.

2.2.3 Maintenance Related Option

One switch enables a printer test feature, causing the printer mechanism to continuously print its selected character font.

3. SWITCH OPTIONS

3.1 The following convention is used in the schematic wiring diagram and circuit description to designate each switch.

SPD4-SW4

SP - Refers to switch pack.
D4 - Refers to location D4 on the card assembly.
SW4 - Refers to the fourth switch of package SPD4.

3.2. Detailed Description

ON - Switch Closed (SW1 is always oriented toward center of card.)
OFF - Switch Open

Designation	Function	Switch State (To Enable Function)
SW1	Automatic New Line	OFF
SW2	Printer Test	ON
SW3	Vertical Parity Send	OFF
SW4	EOT Disconnect	OFF
SPD4 — SW5, SW6	Line Length Select	(see table below)
SW7, SW8	Character Font Select	(see table below)

	SW5	SW6
Unused	OFF	OFF
72 Columns	OFF	ON
80 Columns	ON	OFF
132 Columns	ON	ON

	SW7	SW8
NU Font	OFF	OFF
Undefined	OFF	ON
ME Font	ON	OFF
TV Font	ON	ON

4. SUPPORTING INFORMATION

M43 Logic Board Schematic	- 4740SD
OPCON Schematic, Circuit Description	- 4080SD, 4080CD
Print Head Schematic	- 4013SD
MAPL Spec.	- 430641S
MACON Spec.	- 430671S

SECTION II - DETAILED DESCRIPTION

1. GENERAL

1.1 The voltage and current requirements of the 410740 Card are as follows:

Voltage	Voltage Range	Avg. Current Drain	
+42V	+37.8V to +46.2V	1.0A (with printer load)	
+12V	+10.8V to +13.2V	-	Excluding OPCON and Communications Interface
+ 5V	+ 4.5V to + 5.5V	450 ma	
-12V	-13.2V to -10.8V	150 ma	

1.2 Other supply voltages developed on the card from the -12V supply have the following tolerances:

Voltage	Voltage Range
-4V	-4.6V to -3.4V
-5V	-5.5V to -4.5V

1.3 Other voltages referred to in the circuit description have the following tolerances:

Voltage	Voltage Range
V_H	+3.5V to +5.5V
V_L	0V to + .5V
V_{TH}	+2.4V to +5.5V
V_{TL}	0V to +0.4V
V_{BH}	+ 1V to + 2V
V_{BL}	-4.6V to - 3V

1.4 The following convention is used in the circuit description to designate each circuit entering or leaving a multilogic (ML) pack.

MLE1-3

ML - Refers to multilogic.
E1 - Refers to location E1 on card assembly.
3 - Refers to pin number of the associated circuit connection.

1.5 Logic Symbols - Positive logic symbols are used in the associated schematic.

1.6 Complex logic packs are represented by rectangles. These include the terminal controller logic - MACON (MLC4) and the printer timing logic - MAPL (MLC7).

1.7 Signal Designation - Signal leads are labeled with a title descriptive of the function of the signal. A line drawn over this title indicates that the signal is in its most negative state when the function described by the title of the signal is present.

2. BLOCK DIAGRAM

2.1 The block diagram of Figure 1 shows the interconnection and signal flow between the functional blocks FS-1 to FS-4.

2.2 The Terminal Controller (FS-1) controls overall terminal operation. It retains the present terminal state and displays that state in the light-emitting diode (LED) indicators on the set OPCON. It receives serial data from the OPCON, interprets it for terminal control functions and steers data to either the printer logic or the TAU/TDU or both. It controls serial data streams to and from the TAU/TDU, interprets incoming information for terminal control functions and buffers data before steering it to the printer logic.

2.3 The Printer Timing Logic (FS-2) controls all printer functions. It receives parallel data from the Terminal Controller, decodes it and performs the corresponding operation. The basic printer functions are character print, carriage return, line feed, backspace, bell, margin set, margin clear and margin release.

2.4 Functional Blocks FS-3 and FS-4 contain the power devices which drive the electro-mechanical subassemblies comprising the printer mechanism.

3. THEORY OF OPERATION

3.1 FS-1 Terminal Controller (See TC-1 Timing Diagram.)

3.1.1 General - Functional block FS-1 interfaces the M43 logic card to the set OPCON and the TAU/TDU. It also provides the input data to the printer timing logic and senses various switches for features and options.

3.1.2 OPCON Interface - Both a serial and a parallel data interface exist between OPCON and logic board. The serial interface consists of a 560 KHz clock, a repeat mode signal and a serial data signal. The repeat mode signal (J107 pin 7) is active (character repeating) in the high state (V_H) and inactive in the low ($\measuredangle V_L$). The serial data lead (J107 pin 6) is normally marking at V_H. The transmission code used on this lead consists of eleven bits - one start bit, eight data bits, one parity bit and one stop bit. The spacing level is $\measuredangle V_L$. One bit time = 143 microsec.

The R-C filters (R42, C14 and R43, C15) are present to minimize noise picked up on the interface cable.

The parallel data interface consists of five DC contact switch leads (J107 pins 14, 17, 18, 19, 20) and five LED drive signals (J107 pins 5, 9, 10, 11, 13).

The DC contact switches when depressed (closed) apply ground to the corresponding inputs of a 7417 open collector buffer (MLE3). When released (open), 6.8K resistors (RPD3) pull the buffer inputs to V_H. These buffers in turn drive the MACON pack (MLC4 - 8, 24, 25, 27, 31) with the non-inverted switch state. V_H will be present on the corresponding MLC4 pin when the associated switch is open and V_L will be present when the switch is closed.

The printer test signal (MLC4-24) is provided with an on-board DC contact switch (SPD4-SW2), wire 'AND'ed with MLE3-4, that can enable printer test independent of the OPCON.

The five LED drivers in MACON (MLC4-34 thru 38) pull their respective leads to V_H when activating an LED. The 1K resistors (R37-R41) limit the LED forward current to 15 ma nominal.

3.1.3 Eleven parallel data leads (MLC4-9 thru 19) interface the MACON logic pack with the printer timing logic.

The eight data leads transmit coded information to the printer timing logic. V_H (V_L) represents a binary 1(0).

The Request Next Character signal (MLC4-18) is an input which goes to V_H when the printer timing logic is ready to accept more information. Otherwise it remains at V_L.

The Load Data Printer signal (MLC4-9) drives momentarily (>2 microsec) to V_L when information is to be transferred (via data leads) to the printer timing logic. The trailing edge of this pulse causes Request Next Character to be set to V_L.

Right Hand Margin is a bi-directional signal which, during normal operation is an input to MACON (MLC4-19). This signal goes to V_H coincident with Request Next Character whenever the print mechanism is at the right hand margin. This signal is driven to V_H by MACON (MLC4) whenever the power is turned on with the interlock switch (J107 pin 14) open and the TEST SWITCH is not activated. It remains at V_H until the interlock switch is depressed.

3.1.4 The TAU/TDU interface is comprised of six lines from the MACON (MLC4) pack.

Two control lines provide the normal interface control to the line interface. Terminal Ready (MLC4-3) is active when driven to V_H by MACON. TAU/TDU Ready (MLC4-6) is active when driven to V_{TH} by MLB5-4.

Two data lines provide the bi-directional asynchronous serial data path. Send Data (MLC4-39) is marking (spacing) when driven to V_L (V_H) by MACON. Receive data is marking (spacing) when driven to V_{TL} (V_{TH}) by MLB5-6.

Two test signals are provided for maintenance testing. Both Digital Loop (MLC4-5) and Analog Loop (MLC4-4) are active when driven to V_H by MACON.

A seventh signal, Duplex, is provided at the TAU/TDU interface for future use. It is identical to the signal on MLC4-31 except that no pullup to +5V is provided on the card.

3.1.5 Paper Out and Low Paper switches are connected to the logic card through J101. Each switch drives a 7417 buffer (MLB4-3, 5) with 6.8K input pullup resistors (R13, R14). The 7417 buffer drives MACON (MLC4-22, 28) to V_{TL} when the corresponding switch is closed. Internal resistors in MACON pull these leads to V_H when the corresponding switch is open.

3.1.6 Three option switches (SPD4-SW1, SW3, SW4) are provided for Terminal Controller options.

When a switch is open the associated pin on MACON (MLC4-23, 26, 30) is pulled to V_H. Closing the switch applies logic ground to the corresponding MACON pin.

3.2 FS-2 Printer Timing Logic (See TC-2 and TC-3 Timing Diagrams.)

3.2.1 General - Functional Block FS-2 receives 8 bit parallel information from the Terminal Controller and in turn generates all the necessary timing to produce the corresponding printer function. This functional block also provides the system clock for the M43 Basic KSR.

3.2.2 System Clock - The clock circuit consists of a crystal controlled oscillator and a divide-by-2 squaring circuit with power-on gating.

One half of the NOR gate pack (MLE1) provides the amplifier section for a series resonant oscillator circuit with a 1.12 MHz crystal in the feedback path. The output at MLE1-2 is buffered by another NOR gate with a disabling input (MLE1-12) provided for testing purposes. In normal operation resistor R46 keeps this gate enabled.

One flip-flop of a 74109 Pack (MLD2) is connected as an RS latch (not clocked). The presence of C20 on the CLR input (MLD2-15) sets this latch (MLD2-10) at V_{TL} on power turn on. Approximately 100 msec later C20 will have charged positive enough to reach the NOR gate input threshold (MLE1 pins 4, 5), causing the latch preset (MLD2-11) to switch to V_{TL} and setting MLD2-10 to V_{TH} where it will remain till power is removed. This circuit prevents erratic operation of the clock line during the power-up mode, when the oscillator is starting.

The second flip-flop of the 74109 pack is connected to divide the clock signal (from the oscillator) by two when the 'J' input (MLD2-2) is at V_{TH}. This gives a symmetric 560 KHz clock at MLD2-6 which swings from V_{TL} to V_H. Pullup resistor R36 is needed to attain this positive level. When the J input is at V_{TL} the flip-flop output (MLD2-6) will be set to and remain at V_{TL}.

3.2.3 Terminal Controller Interface - Eleven parallel data lines interface the MAPL (MLC7) logic pack with the Terminal Controller (FS-1). These lines operate as described in Section 3.1.3.

3.2.4 Four option switches are provided for printer options. SPD4-SW7 and SW8 select one of three character fonts. SPD4-SW5 and SW6 select one of three line lengths.

3.2.5 Left Margin Sensor - A DC contact switch is provided on the print head assembly which when depressed (open) allows the input of a 7417 buffer (MLB4 pin 9) to be pulled to V_H by R12. The 7417 output transistor turns off and the MAPL Left Hand Margin signal (MLC7-17) is internally pulled to V_H, indicating that the print mechanism is at the left margin position.

3.2.6 Velocity Encoder - This circuit is comprised of an optical switch, feedback amplifier and hysteresis amplifier which produce a pulse train with repetition rates proportional to the average carriage motor rotor velocity.

The phototransistor section of the optical switch (FS-2, A1) is connected in a common collector configuration. The emitter (J103 pin 1), with load resistor R5 drives both the feedback amplifier through R6 and the hysteresis amplifier (MLA8-9).

The feedback amplifier with elements R6 and C1 serves as both a low pass filter and current amplifier capable of driving the light emitting diode of the optical switch.

As the optical switch beam is interrupted by a slotted disk mounted on the carriage motor rotor shaft, voltage pulses of approximately 600 microsec period and 1V to 3V peak-to-peak amplitude are developed at MLA8-9. This repetition rate is too fast for the feedback amplifier (with low pass filter) to respond to, so no correction is made for this signal. However all slower variations (including DC offsets due to parameter variations) are cancelled out by the action of the feedback amplifier driving the optical switch LED. Consequently the desired velocity dependent signal is present at the input of the hysteresis amplifier (MLA8-9) centered about 0V.

The hysteresis amplifier, with approximately 100 mV hysteresis, amplifies this input signal, supplying a velocity dependent pulse train to the MAPL pack (MLC7-18). This signal swings from V_H to -5V (-0V, +.5V).

3.2.7 Print Mechanism Driver Interface - Nine leads from the MAPL pack (MLC7-31 thru 39) supply the print commands to the nine print mechanism coil drivers. When a print command is to be given, MAPL drives the desired print level lead(s) to V_H for a pre-programmed time. (See TC-2 timing diagram.)

3.2.8 One lead from the MAPL pack (MLC7-30) supplies the input to the bell driver. This lead is driven to V_{BH} for the duration of time required to ring the bell.

3.2.9 Line Feed Motor Driver Interface - Four leads from the MAPL pack (MLC7-26 thru 29) supply the stator timing for the four line feed motor phases. A fifth lead, the clamp switch (MLC7-21), controls a variable clamp in the kickback circuit of the phase 1 coil. To energize a stator coil MAPL drives the appropriate lead to V_H. (See TC-3 Timing Diagram.)

3.2.10 Carriage Motor Driver Interface - Four leads from the MAPL pack (MLC7-22 thru 25) supply the stator timing for the four carriage motor phases. To energize a stator coil MAPL drives the appropriate lead to V_H. (See TC-2 for typical stator timing during printing.)

3.3 FS-3 Print Head and Bell Drivers

3.3.1 General - Each print head driver consists of a CMOS pre-driver and Darlington power driver. The bell driver consists of a Darlington power driver only.

3.3.2 When the bell driver input (Q20-B) is driven to V_{BH} by MAPL the collector (Q20-C) goes to 1.5V nominal, driving approximately 175 mamp through the bell coil. When MAPL releases the input, R26 pulls Q20-B to ground turning off the driver. Inductive kickback from the bell coil attempts to drive Q20-C highly positive. CR25 however clamps the collector preventing it from going more positive than 43V nominal.

3.3.3 When a print level pre-driver (MLE6, E7 or E8) input is driven to V_H by MAPL it in turn drives the base of its associated power driver (Q11-Q19) to V_{BH}. The power driver then turns on to V_{CE} = 1.5V nominal causing a current pulse in the associated print head coil. When MAPL releases the input, the pull down resistor (R27 through R35) brings the pre-driver input to V_{BL} causing the pre-driver to pull the associated power driver base to V_{BL} turning off the driver. The collector voltage rise due to the inductive kick of each head coil is clamped by diodes CR16 thru CR24 to 43V nominal.

3.4 FS-4 Line Feed Motor and Carriage Motor Drivers

3.4.1 General - Each driver for both the line feed and carriage motor coils consist of a CMOS pre-driver and Darlington power driver. In addition the line feed motor circuit contains a Darlington switch across the phase 1 coil to provide hard clamping of the inductive kick during the idle condition.

3.4.2 Line Feed Motor Circuit - To energize stator coil 4 (J102-1) MAPL drives the corresponding pre-driver input (MLE6-9) to V_H, which in turn drives the associated power driver base (Q1-B) to V_{BH}. This turns on the power driver to V_{CE} = 1.5V nominal causing current flow in the stator coil.

3.4.2 (Continued)

When MAPL releases the input, R22 pulls the pre-driver input to V_{BL} which then pulls Q1-B to V_{BL} turning off the power driver. The inductive kick of the coil when Q1 turns off is clamped by CR3 and CR1 (25V zener) to a nominal 68V, resulting in a fast decay of the stator current. Blocking diode CR4 is needed to prevent negative voltages induced in coil 4 (at J102 pin 1), due to mutual coupling with stator coil 2, from forward biasing the Q1 base-collector junction and pulling current through the coil (via the logic supply). The above description applies also to the other three stator coils, except as described below.

When the line feed mechanism is idle, MAPL drives the clamp switch (MLE6-7) to V_H. MLE6-6 drives Q6 into saturation. This in turn pulls enough base current through R11 to turn on Q5. With Q5 on, stator coil is hard clamped (via CR11 and Q5) to 44V nominal. During this idle state, the phase 1 drive signal is pulse width modulated at a 20 KHz rate. In conjunction with the hard clamp this provides a low level recirculating current in coil 1, keeping the motor in a detented position.

When stepping the line feed motor, MAPL releases the clamp switch input which then is pulled to V_{BL} by R17. This causes Q6 and thus Q5 to turn off. In this condition, the clamping network for coil 1 is identical to that described above for the other coils.

3.4.3 Carriage Motor Circuit - The pre-driver and driver circuits for each stator coil (J104-1, 2, 3, 4) operate as described in 3.4.2 for the line feed motor. The coils are again zener clamped as described for the line feed motor. However, the zener in this case is in parallel with resistors R8 and R9, which help the zener dissipate the kickback energy. Because of this the kick voltage will remain below the zener clamp voltage till the coil current at turn off reaches approximately .5 amp.

3.5 FS-5 Voltage Distribution

3.5.1 The power on reset circuit is intended to function during two power states: a) At V_{SS} power up time it will provide a delayed V_{DD} potential and will ensure that the V_{SS} power supply has reached $4.25 \pm .250$V before turning V_{DD} on. b) At V_{SS} power interruption, $V_{SS} = 4.25 \pm .250$V, the circuit will turn V_{DD} off for the duration of the interrupt and provide a delayed V_{DD} potential only after the return of $V_{SS} = 4.25 \pm .250$V. This delayed V_{DD} potential from V_{GG} and V_{SS} will force both MAPL and MACON into their respective POR routines.

Precision resistors R_{49} and R_{50} form a voltage divider which determines the value at which V_{SS} must be before MLA8-1 will switch states. Based upon the assumption that V_{GG} holds slightly longer or precedes V_{SS}, the V_{SS} trip voltage is set at $4.25 \pm .250$V. The power up sequence is as follows: V_{GG} (-5V) precedes or is coincident with V_{SS} (+5V) which causes MLA8-1 to track the rising positive supply voltage, V_{SS}, which in turn causes the emitter of Q_{21}, V_{DD}, to also track the rising V_{SS} voltage ($V_{DD} = V_{SS}-2V+VBEQ_{21}$). At such time that V_{SS} reaches $4.25 \pm .250$V, the timing network of R_{53}, CR_{29}, and C_{17} continues to hold the plus input

3.5 (Continued)

(MLA8-3) positive with respect to the negative input, hence, forcing MLA8-1 and Q_{21} emitter (V_{DD}) to continue to track V_{SS}. Approximately 50 msec. later C_{17} will be charged such that the voltage across R_{53} (MLA8-3) will drop below that voltage on MLA8-2; at which time, MLA8-1 switches to V_{GG} + 2V (-3V) causing Q_{21} to saturate and thus forcing $V_{DD} = O_V + V_{CE}$ (SAT) Q_{21} (Transistor Q_{21} is specified as having a V_{CE} (SAT) of 0.1V max. at I_C = 100 ma and I_B = 10 ma.) Resistor R_{51} sets the minimum base drive of Q_{21} at 10ma in the saturated mode and resistor R_{52} ensures V_{DD} will pull towards V_{SS} in the emitter follower mode. Diode CR_{28} provides a rapid discharge path for C_{17} in order to ready the detector for future V_{SS} interrupt. Capacitor C_{23} protects the detector from static discharge. The power interrupt sequence is as follows: V_{GG} (-5V) holds longer than V_{SS} (+5V) which drops to 4.25 $\pm$ .250V causing MLA8-2 to go negative with respect to the plus input; MLA8-1 then switches to V_{SS}-2V and again tracks V_{SS} as does Q_{21} emitter (V_{DD}) as stated earlier. This positive output step plus initial voltage on C_{17} is coupled to R_{53} adding to the voltage difference at MLA8-2 and MLA8-3; thereby causing the timing delay as stated previously if V_{SS} returns immediately. Should V_{SS} continue to drop, MLA8-1 continues to track the fault condition of V_{SS} and the detector would behave as stated earlier upon the return of V_{SS} (power up sequence).

TC-4 Timing diagram illustrates typical waveforms for the power sequences stated previously and depicts the detector parameters of interest:

1) V_{GG}'s must precede or be coincident with V_{SS} on powering up.

2) V_{DD} must pull-up to within 2V of V_{SS} in the lower V_{SS} power mode.

3) V_{DD} must continue to track V_{SS} for a minimum of 10 msec. after return of V_{SS}.

4) Q_{21} must saturate at equal to or less than 0.1 volts during normal MOS operation.

5) The trip range on V_{SS} is approximately 4.25 $\pm$ .250 volts.

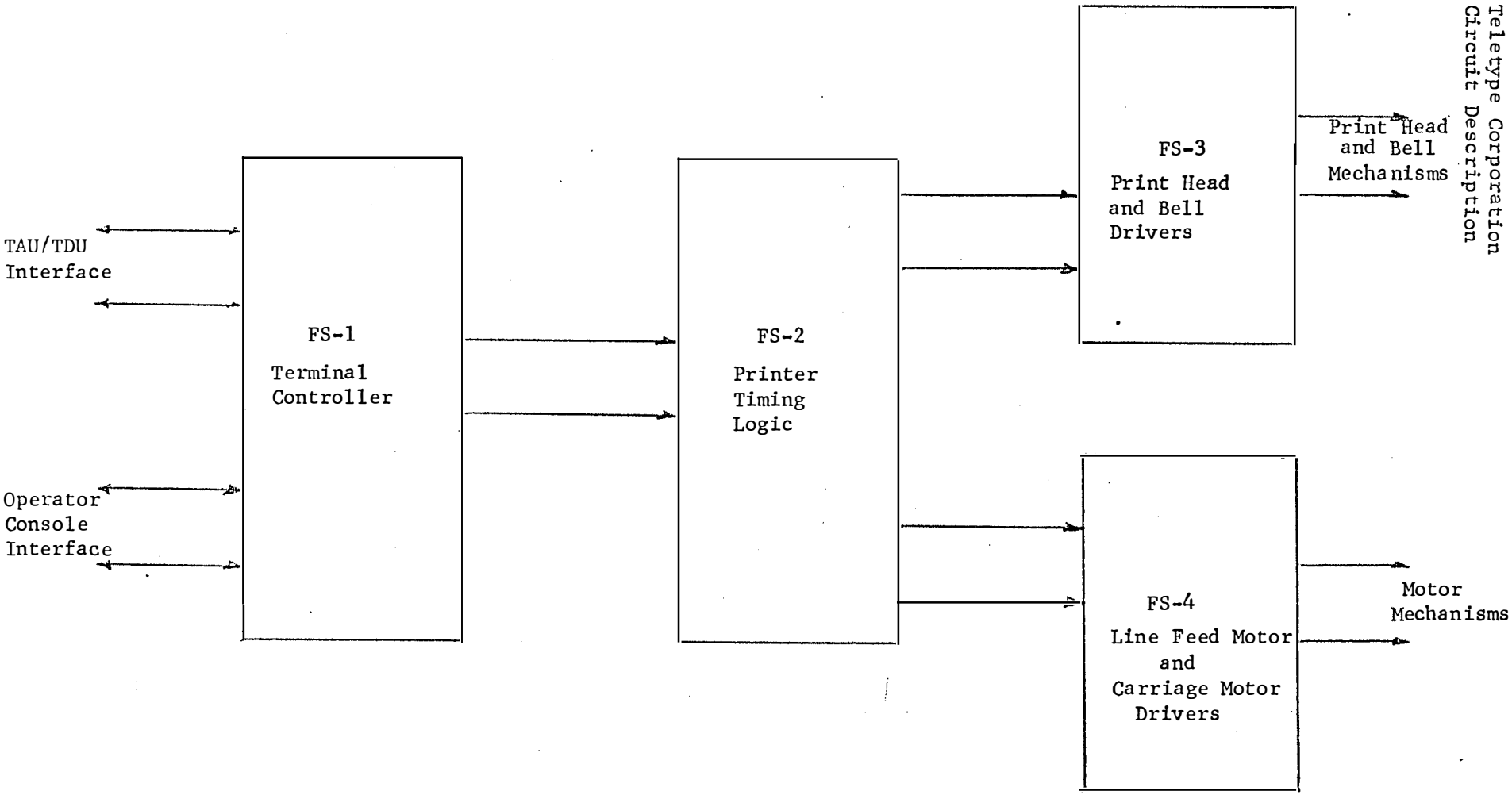
3.5.2 Zener diode CR26 develops a nominal -4V from the -12V supply through limiting resistor R15.

Zener diode CR27 develops a nominal -5V from the -12V supply through limiting resistor R16.

3.5.3 The various .1 MFD capacitors are filters for the logic voltages. C4 is a high frequency bypass for the +42V.

Capacitor C3 is a filter on the +42V used to average out the pulsed energy requirements of the print mechanism.

FIGURE 1


TAU/TDU
Interface
Operator
Console
Interface
FS-1
Terminal
Controller
FS-2
Printer
Timing
Logic
FS-3
Print Head
and Bell
Drivers
Print Head
and Bell
Mechanisms
FS-4
Line Feed Motor
and
Carriage Motor
Drivers
Motor
Mechanisms

SHEET INDEX AND ISSUE CONTROL

4080CD

Sheet 1

CIRCUIT DESCRIPTION OF THE 410080 CONSOLE LOGIC CARD

REVISIONS			SHEET ISSUE NUMBER				
ISSUE	DATE	AUTH. NO.	SHEET NUMBER 1	2	3	4	5
/	6/11/76	24331R	1	1	1	1	1
2	2-21-77	16857	2	1	1	1	2

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG.REL. COMPL.	ENG. RHF	DSGNR. -	DRN. -
			DATE 6/11/76	S-NUMBER -	
			R&D FILE NO. 2-30.171.263AA	E-NUMBER -	

TELETYPE

4080CD

TC482-1272

CIRCUIT DESCRIPTION OF THE 410080 CONSOLE LOGIC CARD

TABLE OF CONTENTS

SECTION I - GENERAL TECHNICAL INFORMATION (Basic Function)

1. The 410080 Console Logic Circuit Card (CC080) is a double sided circuit card, 5-1/2" x 12", containing Teletype MOS circuit packs, commercial integrated circuit packages and discrete components. The console frame, the keyswitch channels and all keyswitches mount to this card.

2. The CC080 assembly provides the following features:

2.1 Sense up to 67 keys depressed by an operator.

2.2 Generate and transmit codes for up to 58 keys.

2.3 Generate alternate codes, when required, when shift or control keys are depressed.

2.4 Generate characters repeatedly with a universal repeat key.

2.5 Provide 5 Light Emitting Diode (LED) indicators controlled and powered by an external source.

2.6 Provide a "CAPS LOCK" mode for selectively shifting only alpha characters.

SECTION II - DETAILED DESCRIPTION

1. ASSOCIATED DOCUMENTS - 410080 Assembly Drawing, 4080SD Schematic Diagram.

2. THEORY OF OPERATION

2.1 Keyswitches and Sense Amplifiers (FS-1, Sheet B1)

2.1.1 Each capacitive keyswitch is connected to a single input of a Sense Amplifier MLA1, MLA6 or MLB4. The Sense Amplifier determines the logic state applied to an input by comparing the charging time of the keyswitch connected to an input to the charging time of a Reference Capacitor (C2, C10 or C15) which is connected to input 0. Charging current for the Sense Amplifiers is provided by Reference Resistors (R6, R27 or R30) connected to each Sense Amplifier's summing pin (Σ) and returned to V_{GG2}.

2.1.2 When power is first applied to CC080 the Keyswitch Logic MLA5 initializes all Sense Amplifiers by transmitting two consecutive pulses, Master Reset (MR) and SYNC. The I/O leads are active when at V_H. The MR and SYNC pulses, which last for one complete clock cycle each, initiate Master Reset and Synchronizing functions. The Synchronizing pulse forces the Sense Amplifiers to the Reference Input (IO) to begin a scan. ($V_H \geq V_{SS}$-1V.)

2.1.3 The Sense Amplifiers charge their associated Reference Capacitor to measure a reference charging time. Subsequently, the Keyswitch Logic transmits Data Enable (DE) pulses which advance the Sense Amplifiers to their first keyswitch inputs and places the keyswitches under test. Each Sense Amplifier determines the state of the keyswitch by determining that the keyswitch charges faster or slower than the reference capacitor.

2.1.4 After 12 clock cycles the Keyswitch Logic transmits Another Data Enable pulse. The Sense Amplifiers respond by transmitting two Data Bits (active to V_{SS} when Ø1 is at V_{GG2}). Data Bit 1 will be active at V_H when the keyswitch being sensed is first encountered as "depressed". Data Bit 2 will be active at V_H as long as the keyswitch continues to be depressed. This action continues until the Sense Amplifiers have tested all inputs (21 keyswitches). The Keyswitch logic transmits a number of extra Data Enable pulses (ignored by the Sense Amplifiers) while internal logic functions are being performed. The Keyswitch Logic then re-transmits the SYNC pulse and the scan cycle repeats.

2.2 Keyswitch and Interface Logic (FS-2, Sheet B2)

2.2.1 The Keyswitch Logic (MLA5) controls the operation of the Sense Amplifiers (see Section 2.1.3 and 2.1.4) and provides coded output to the interface.

2.2.2 When power is first applied to CC080, Capacitor C8 is discharged. During the time that it is charging (through R22) the Keyswitch Logic will send Master Reset and Sync pulses to the Sense Amplifiers. In addition, the Serial Send Data output will be held to V_H. After C8 has charged beyond the threshold of the Power-On-Reset Input (PORIN), the Keyswitch Logic will transmit only SYNC and Data Enable pulses to the Sense Amplifiers and normal operation of the CC080 can begin.

2.2.3 Once each scan the Keyswitch Logic transmits a SYNC pulse to establish synchronization. After the SYNC pulse and a timing interval the Keyswitch Logic transmits a serial of Data Enable pulses, one pulse per every 12 clock cycles. The Sense Amplifiers respond to each Data Enable pulse by transmitting the two data bits corresponding to their input under test. Data Bits are valid on the two consecutive Ø1 periods following the Data Enable pulse, when Ø1 is at V_{GG2}.

2.2.4 After all keyswitches have been tested the scanning cycle repeats. A test signal, End of Scan (EOS/ALARM) is provided for use as a timing reference. EOS is active to V_H for 8.9 microseconds with a repetition rate of 4.57 milliseconds. End of Scan is active twenty-four Ø1 periods after the SYNC pulse.

2.2.5 When a keyswitch has been sensed as "depressed" the Keyswitch Logic will determine if it is to be sent as a character or is to modify the code of another keyswitch (i.e., if the switch is Caps Lock, Shift, Control, or Repeat). If the code is to be sent it will appear as Mark-Space data on the Serial Send Data lead. This lead (pin 6 at J1) is normally marking (at V_{CC} +0,-.5V). The high level of both Serial Send Data and Repeat Mode (RPMD) is limited to V_{CC} by CR2, CR3, CR4 and R7. The code consists of 11 bits: one start bit, 8 code bits, one parity bit and one stop bit. The low level (space) is $\leq (V_{GG1} + .5V)$. One bit time = 143 uS. Output impedance for both Serial Data and RPMD shall be $\leq$5000 ohms in either logic state.

2.2.6 Repeat Mode (RPMD) is $\leq (V_{GG1} + .5V)$ as long as the Repeat key is not depressed. When the Repeat key is depressed, the RPMD lead of MLA5 goes to V_H and RPMD (pin 7 of J1) goes to $(V_{CC} + 0 - .5V)$. RPMD will return to V_{GG1} when the Repeat key is released. If any other keyswitch is depressed while the Repeat key is depressed, the character associated with that keyswitch will be sent once per scan (4.57 ms.).

2.2.7 Switches S0, S1, and S2 are normally open D.C. contact latching switches. The depressed (latched) state connects the corresponding pin in J1 to V_{GG1}. S3 and S4 are normally open D.C. Contact switches. When S3 or S4 is depressed, the corresponding pin in J1 is connected to V_{GG1}.
2.2.8 Light Emitting Diodes (LED's) in the indicating keyswitches are controlled by their respective pins in J1. On current shall be $>$ 10 ma but $<$ 15 mA.

2.3 Clock Generation and Drivers (FS-3, Sheet B3)

2.3.1 The 560 KHz. clock from pin 12 of J1 is divided by 5 by MLB3. The QC (pin 8) output of MLB3 is a 40% duty cycle waveform with a 112 KHz. repetition rate. R28, R29, C11 and C12 delay appropriate edges of the 112 KHz signal and are recombined in MLB1 and MLB2 to produce a non-overlaping $\overline{Ø1}$ and $\overline{Ø2}$ predrive signals at pins 11 of MLB1 and MLB2. The non-overlap time is .3 uS min to 1.2 uS max. for both non-overlaps.

2.3.2 The predrive signals are coupled to MLA4 by C6 and C7. R14 and R15 limit the current levels. CR8, R34 and CR9, R35 insure a proper voltage swing for the Clock Driver. Clock Driver MLA4 is a high voltage dual inverter. R16 and R17 prevent inductive ringing of the fast transitions on Ø1 and Ø2. R12 and R13 bias the outputs of MLA4 slightly "ON" to prevent clock excursions above V_{SS}. The high clock levels (for Ø1, Ø2, Ø1L and Ø2L) shall be V_{SS} but (V_{SS}-1.7V). The low Ø1 and Ø2 levels shall be V_{GG2}-1.2V).

2.3.3 R18 and R19 limit current so that CR5 and CR6 can clamp Ø1L and Ø2L to V_{GG1}. Ø1L and Ø2L are the clocks to MLA5 which requires a lower clock voltage than the other MOS devices. The low Ø1L and Ø2L levels shall be V_{GG1} but (V_{GG1} -1V).

2.4 Power Distribution (FS-4, Sheet B4)

2.4.1 Zener Diode CR1 reduces the -12V by 3.9V, so as to make V_{GG2} approximately -20V with respect to V_{SS}. Voltage to Pin 4 of MLA5 is fixed at one diode drop more negative than V_{GG1} by CR7 and R33.

2.4.2 Capacitors C3, C4, C5 and C13 are filter capacitors for the various power supplies.

2.5 Power Requirements

+12V $\pm$ 10% at 160 ma. max.
+ 5V $\pm$ 10% at 100 ma. max.
-12V $\pm$ 10% at 140 ma. max.

Maximum power dissipation = 4.5 W.

2.6 Temperature Ranges:

Operation: 40^{o}F to 130^{o}F at 2% to 95% Relative Humidity

Storage: -40^{o}F to 150^{o}F