PROPERTY OF [redacted]

INSTRUCTION MANUAL

MODEL 1203

FSK DEMODULATOR

TUP

FREDERICK ELECTRONICS CORPORATION
Hayward Road, Post Office Box 502
Frederick, Maryland 21701

Manufactured under
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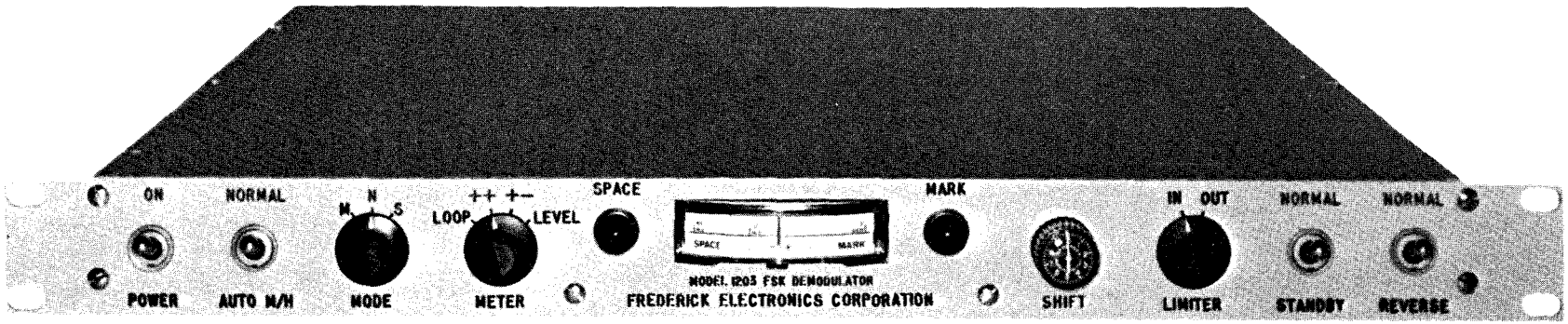

Figure 1-1. Model 1203 FSK Demodulator

SECTION I

INTRODUCTION

1.1 PURPOSE OF EQUIPMENT

The Model 1203 FSK Demodulator is designed to provide optimum detection of frequency shift keying signals with shifts between 0 and 1000 Hz, and with keying rates up to 74.2 baud. The Model 1203 accepts audio signals from a standard communications receiver, demodulates these signals, and uses the resultant output for keying a standard neutral telegraph loop. The effects of frequency selective fading are minimized in the Demodulator through the use of variable decision threshold techniques. This function is performed by a patented Decision Threshold Computer (DTC) circuit, which varies the threshold or transition point between marks and spaces in accordance with receiving conditions.

Additional outputs are provided on the rear panel of the Model 1203 for diversity demodulator operation, and for visual tuning with an optional FEC Model 1251 data tuning and display monitor. Chassis space is also provided for an optional 130 volt internal loop power supply.

1.2 PHYSICAL DESCRIPTION

The Model 1203 FSK Demodulator contains plug-in Filter and Detector cards, a plug-in power supply and optional loop supply, a tuning meter, and associated front panel controls and switches, all conveniently packaged for mounting in a standard 19-inch equipment rack. A vertical rack space of 1-3/4 inches is required.

1.3 SPECIFICATIONS

Specifications for the Model 1203 FSK Demodulator are shown in Table 1-1.

Table 1-1. Specifications, Model 1203

Input Signal	0 dbm audio with a mark frequency of 2125 Hz and any space frequency between 2125 and 3125 Hz.
Input Frequency Shift. . . .	From 0 to 1000 Hz
	NOTE Below 85 Hz shift, the mark and space band-pass filters begin to overlap and optimum performance will no longer be obtained.

Table 1-1. Specifications, Model 1203 (cont.)

Input Baud Rate.	74.2 baud
Input Impedance.	Balanced 500 ohms
Mark Center Frequency. . . .	2125 Hz with 85 Hz bandwidth
Space Center Frequency . . .	1500 Hz with 85 Hz bandwidth
Outputs.	EIA-RS-232 or MIL-STD-188C compatible. High level 20/60 ma neutral or polar loops (optional).
Power Requirements	115 vac, 47 to 63 Hz, 15 watts

SECTION II

INSTALLATION

2.1 UNPACKING AND INSPECTION

Carefully unpack and remove the Model 1203 FSK Demodulator from its shipping container. Inspect the unit for damage. If any damage is found, file a written claim with the shipping agency. Send a copy of this claim to Frederick Electronics Corporation.

2.2 POWER REQUIREMENTS

The required input power for the Model 1203 FSK Demodulator is 115 vac, 60 Hz at approximately 15 watts. Satisfactory operation is possible with line voltages between 105 and 130 vac, and with frequencies from 47 to 63 Hz.

2.3 INSTALLATION

2.3.1 MOUNTING

The Model 1203 FSK Demodulator is designed to mount in a standard 19-inch equipment rack. A vertical rack space of 1-3/4 inches is required. Low power consumption permits operation over a temperature range of 0^{o} to 50^{o} C.

2.3.2 TERMINAL BOARD WIRING

Figure 2-1 shows the rear panel terminal board connections for a typical demodulator installation with an external 130 volt loop power supply. Figure 2-2 shows a typical installation utilizing the optional 130 volt internal loop supply. Figure 2-3 shows a typical installation for diversity operation.

2.3.3 POWER SUPPLY ADJUSTMENTS

It is recommended that the +11.5 vdc power supply voltage be checked, and adjusted if necessary, before the unit is placed in operation.

CAUTION

P.C. board NO392 should be disconnected from connector J5 prior to any power supply check and adjustment.

The +11.5 vdc can be checked at pin B of connector J3. The voltage should be between +11.3 and +11.5 vdc and can be adjusted by potentiometer R22, located in the upper right hand corner of power supply board NO1378.

Table 2-1. Input/Output Connections

CONNECTOR	PIN NUMBER	FUNCTION
TB1	1, 2	Audio input
	3, 4	Ground
	5	Optional Neutral Keyer output (MK)
	6	Loop supply (-)
	7	Loop supply (com)
	8	Optional Neutral Keyer output (no current limiting)
	9	NC } Mark/Hold relay contacts
	10	NO } Mark/Hold relay contacts
	11	C } Mark/Hold relay contacts
	12	Loop supply (+)
J1 External Display Connector	1	Mark Tone output
	2	Space Tone output
	3	Waveform output
	4	Ground
	5	Low-pass filter output
	6	Switching waveform output

Table 2-1. Input/Output Connections (cont.)

CONNECTOR	PIN NUMBER	FUNCTION
J1 External Display Connector (cont.)	7	Mark } Optional Polar Keyer outputs
	8	Common } Optional Polar Keyer outputs
	9	Space } Optional Polar Keyer outputs
	10	Ground } EIA-MIL Low Level Keyer
	11	EIA-MIL output } EIA-MIL Low Level Keyer
	12	Standby } EIA-MIL Low Level Keyer
J2 Diversity Connector	1	Mark channel
	2	Space channel (+)
	3	Space channel (-)
	4	Ground
	5-12	Not used

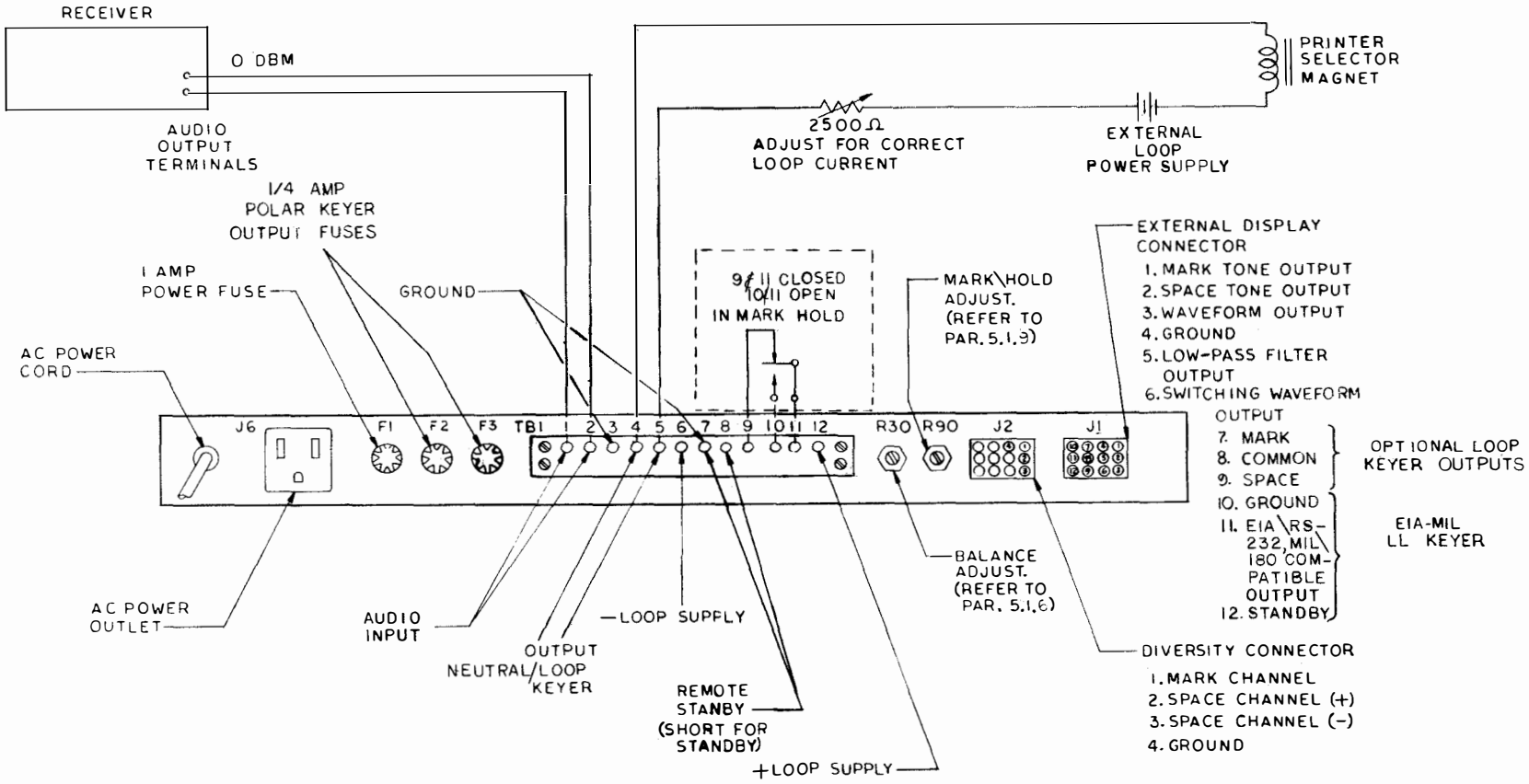

Figure 2-1. Typical Demodulator Installation C1100C

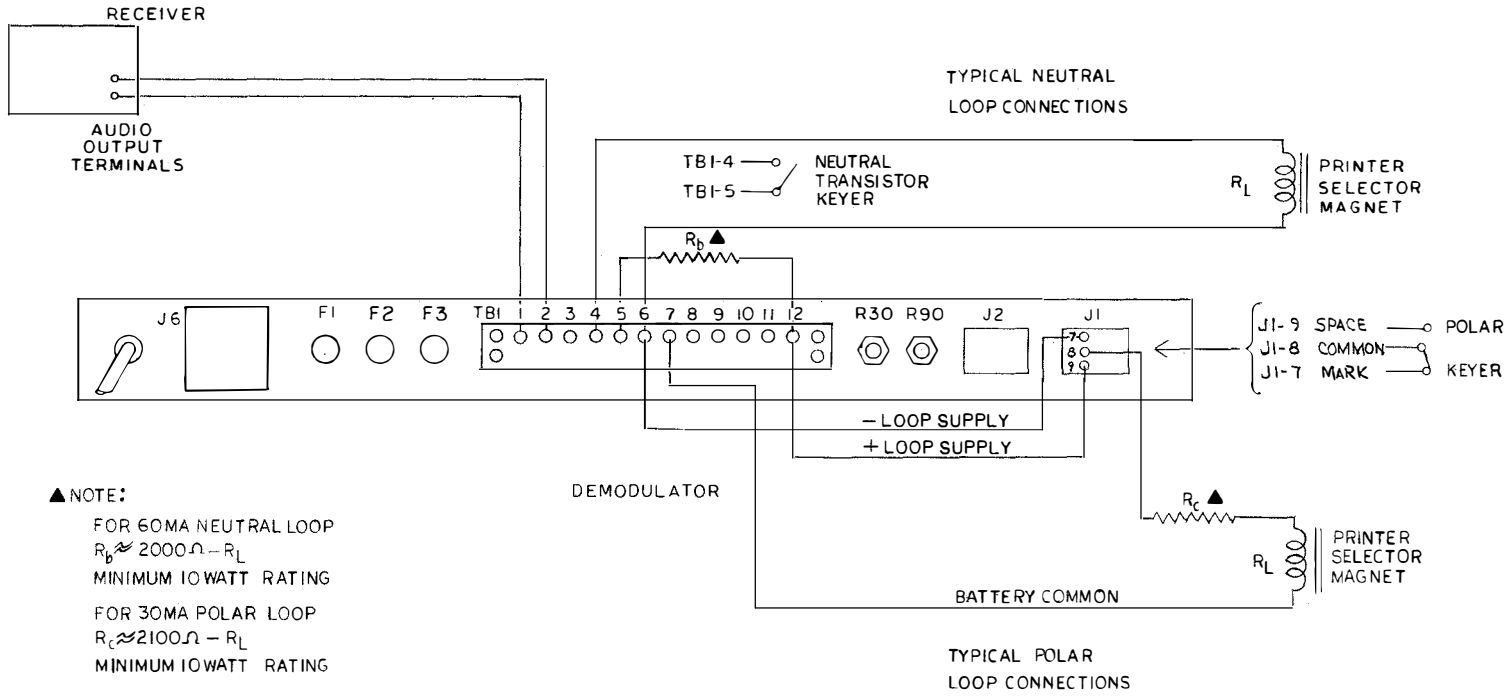

Figure 2-2. Typical Demodulator Connections For Optional Neutral And Polar Loop Supplies
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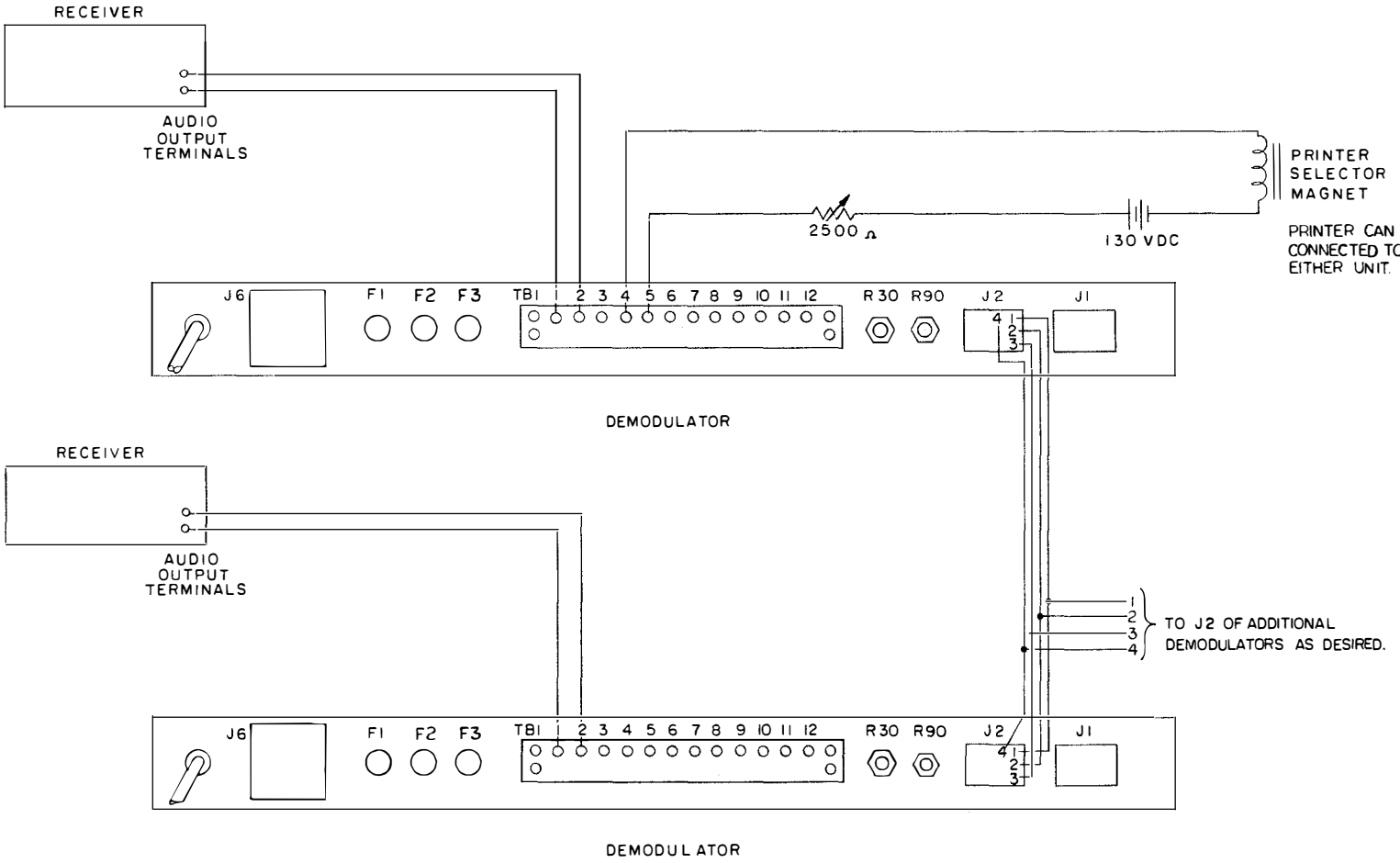

Figure 2-3. Typical Demodulator Connections For Diversity Reception C0951B

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SECTION III

OPERATION

3.1 GENERAL

To obtain optimum performance from the Model 1203 FSK Demodulator, it is essential that the operator thoroughly understand: (1) how the Demodulator works; (2) the function of each control and indicator; (3) how to tune the associated receiver to an FSK signal. Item (1) is covered in Section IV of this manual. Items (2) and (3) are presented in this section.

3.2 CONTROLS AND INDICATORS

Table 3-1 lists all front panel controls and indicators on the Model 1203. Notice that an asterisk (*) appears after one position or function of certain controls. The asterisk indicates that the control function is engraved in red on the front panel. The red engraving identifies normally-used positions and provides a "home base" or departure point for various operating situations. Thus, if the operator experiences any difficulty or confusion in operation he can return these controls to the red position until he determines the correct operating procedure.

Table 3-1. Controls and Indicators

NAME	REFERENCE NUMBER	FUNCTION
POWER-ON* switch	S1	Controls ac power to FSK Demodulator.
AUTO M/H-NORMAL* switch (functions only when MODE M-N*-S switch is in the N* position, and LIMITER switch is in the IN position)	S3	AUTO M/H position: In the absence of an input signal, places output of Demodulator in mark-hold. NORMAL* position: mark-hold circuit is inoperative.
MODE M-N*-S switch	S4	N* position: Selects both mark and space signals. M position: Selects mark signal only. S position: Selects space signal only.

Table 3-1. Controls and Indicators (cont.)

NAME	REFERENCE NUMBER	FUNCTION
METER switch LOOP, ++*, +-, LEVEL	S7	LOOP position: Monitors current in teleprinter circuit: has marking at 20 ma and 60 ma (full scale). ++* position: Used in tuning receiver to an FSK signal. Receiver is properly tuned when meter needle has maximum deflection and minimum oscillation. +- position: Indicates presence of mark and space signals by deflecting to right for mark and to left for space. LEVEL position: Monitors level of input signals; normal indication is 0 DBM.
SPACE indicator	DS1	Glows when Demodulator output is spacing.
MARK indicator	DS2	Glows when Demodulator output is marking.
SHIFT* vernier dial	R91	Adjusts Model 1203 local oscillator to receive an input signal with a mark-space shift of from 0 to 1000 Hz.
LIMITER IN-OUT switch	S5	IN position: Activates limiter circuit. OUT position: Deactivates limiter circuit.
NORMAL*-STANDBY switch	S6	NORMAL* position: Permits normal Demodulator output. STANDBY position: Places Demodulator output in steady mark.

Table 3-1. Controls and Indicators (cont.)

NAME	REFERENCE NUMBER	FUNCTION
NORMAL*-REVERSE switch	S2	Reverses mark and space polarity at output.

3.3 OPERATING AIDS

3.3.1 RECEIVER

The performance of the FSK Demodulator depends to a large extent upon the type of receiver used, and upon careful tuning. For best results, use a single-sideband receiver with good frequency stability, variable IF bandwidth selectivity, a product detector, slow AVC, and passband tuning. The operator should read the instruction manual for the receiver, and thoroughly familiarize himself with its operation.

3.3.1.1 FREQUENCY STABILITY. Receiver frequency stability is important in the reception of FSK signals. Frequency stability becomes extremely important with the narrower shifts. Any slow frequency drift, even with 850 Hz shift, can quickly interrupt copy from the strongest of signals.

3.3.1.2 SELECTIVITY. The normal AM broadcast receiver passes a band of frequencies five kilohertz or more in width. If such bandwidths were used in receiving FSK signals, background noise and adjacent-channel interference could ruin reception. Narrow IF bandwidths are thus desirable, since they can reduce and even eliminate much of this interference. Good single-sideband receivers will normally have two or more switch-selectable IF bandwidths. The proper IF bandwidths to use in a particular application depends upon the frequency shift of the received signal. In practice, always use the next widest receiver bandwidth than the bandwidth of the shift frequency. For example, with 850 Hz shift, the bandwidth should be greater than 850 Hz.

3.3.1.3 PRODUCT DETECTOR. A product detector in the receiver will improve the performance of the FSK Demodulator. This type of detector greatly reduces both intermodulation and harmonic distortion, thereby providing a cleaner signal from the receiver. Since automatic volume control can be used with the product detector, a more constant output will be obtained even during fading signal conditions.

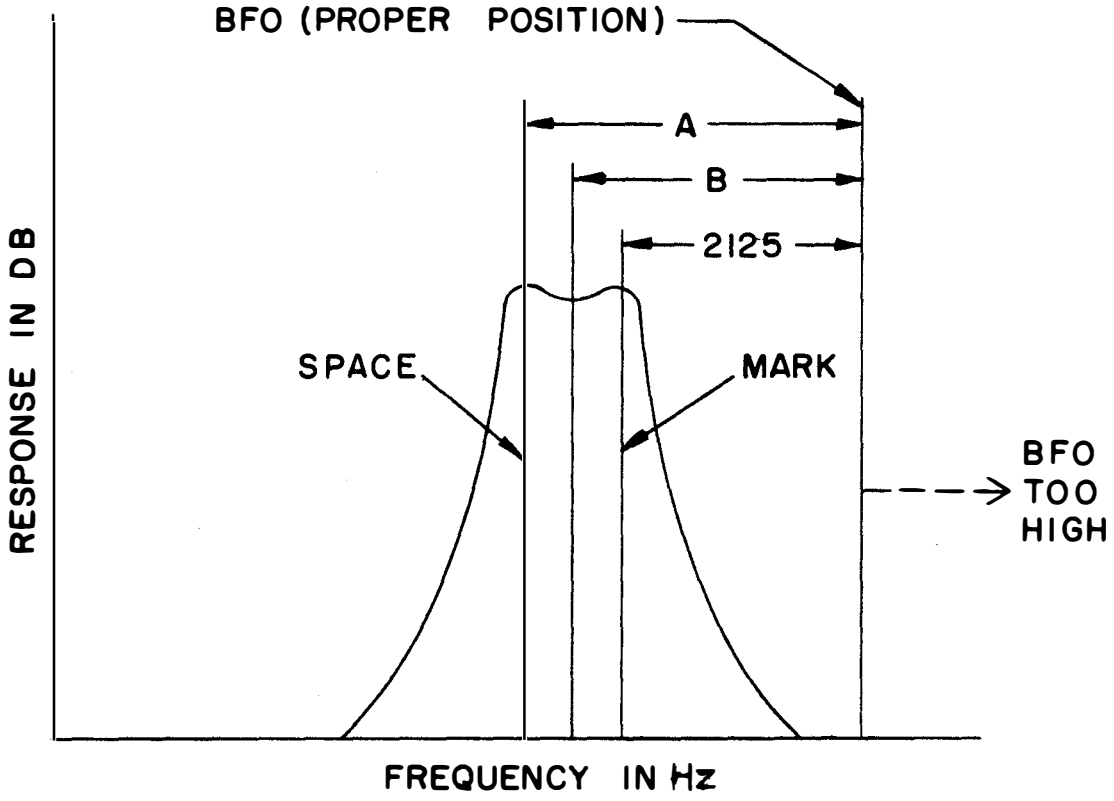
3.3.1.4 AUTOMATIC VOLUME CONTROL. Some receivers provide slow and fast automatic volume control (AVC). Slow AVC should be used in receiving FSK signals, since a fast attack and a slow release are necessary. Slow AVC introduces the proper amount of delay in release to suppress noise during momentary absences of either signal frequency. With fast AVC, the receiver sensitivity recovers too quickly, thereby permitting excessive noise to appear.

3.3.1.5 BEAT FREQUENCY OSCILLATOR. Positioning of the mark and space frequencies in the IF passband of the receiver is critical for good performance. The two frequencies must be positioned so that they straddle the center point with equal amplitude. Failure to do this, especially with a very narrow band-pass, can result in a loss of the mark or space frequency. If the receiver Beat Frequency Oscillator (BFO) is varied to produce the mark and space frequencies, the operator must also know whether the BFO is tuned higher or lower than the received signals. This is illustrated in Figure 3-1. If the BFO is set higher in frequency than the received signals, the mark will be the lower frequency and the space will be the higher. This is the correct position for the mark and space signals. If the BFO is set too high, the space signal will be shifted outside the receiver passband, and the mark signal will approach the original position of the space signal.

Figure 3-2 shows the resultant signal relationship when the BFO is set to a frequency below that of the received signals. The mark and space signals have now changed places. Space is the low frequency and mark is the high frequency. If the BFO is set too low, the mark signal will be shifted outside the receiver passband, and the space signal will approach the original position of the mark signal.

All is not lost if the operator tunes the BFO to the wrong side of the signal frequency, provided that the mark and space signals still straddle the center point as shown in Figures 3-1 and 3-2. A wrong choice can be corrected by means of the NORMAL*-REVERSE switch on the FSK Demodulator. This switch reverses the mark and space signals at the output of the detector, thereby permitting the printer to function with the normal mark-space relationship.

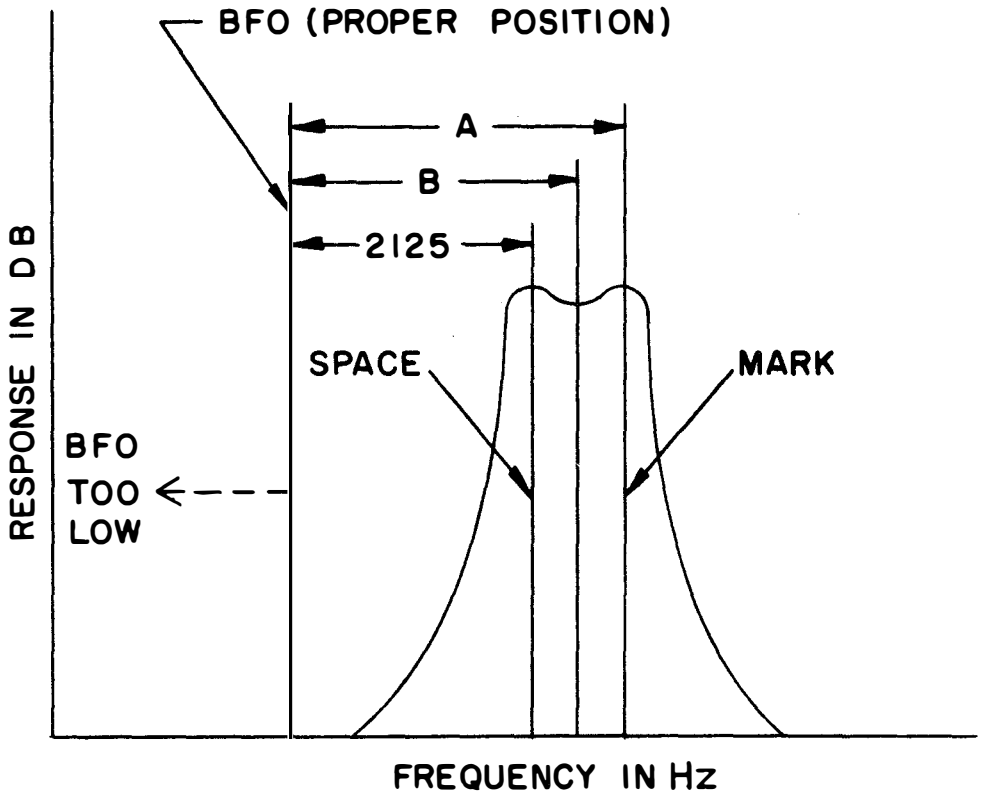
To adjust a variable BFO, the receiver is tuned to noise only (i.e., a no-signal frequency), the METER switch on the Demodulator is placed in the +- position, and the BFO control is set for a zero reading (center scale) on the meter. This operation balances the noise in the mark and space channels, thereby insuring equal amplitude signals when the receiver is properly tuned to keying.



A = 2125 to 3125

B = Frequency Halfway Between MARK and SPACE Tones

Figure 3-1. BFO Frequency Higher Than Signal Frequency



A= 2125 to 3125

B= Frequency Halfway Between MARK and SPACE Tones

Figure 3-2. BFO Frequency Lower Than Signal Frequency

3.3.1.6 PASSBAND TUNING. Passband tuning in a receiver permits the IF to be shifted a few kilohertz above and below its normal frequency. The shift is effected without altering the shape of the passband. This is particularly useful with interfering signals, since the passband can often be tuned to eliminate the unwanted signal. If the receiver has a passband tuning control, this control is substituted for the BFO control. The tuning procedure is the same.

3.3.2 DEMODULATOR

3.3.2.1 MODE M-N*-S SWITCH. The MODE M-N*-S switch permits the operator to select mark signals only (M position), mark and space signals together (N* position), or space signals only (S position). This switch is usually placed in the N* position.

3.3.2.2 METER SWITCH. This switch has four positions. The LOOP position of the METER switch is used to adjust and monitor the loop current in the external teleprinter circuit. The meter scale has readings at 20 MA and at 60 MA (full scale).

The ++* position of the METER switch is used in tuning the receiver to an FSK signal. If only a carrier is present (no keying), the receiver is tuned for maximum needle deflection with the MARK indicator on. If keying is present, the receiver is tuned for maximum deflection and minimum oscillation of the meter needle. Both the MARK and SPACE indicators will flicker during keying.

The +- position of the METER switch is used to obtain equal amplitude response (noise balance) from the mark and space channels. This response is obtained by first tuning the receiver to noise only, and then by adjusting either the BFO or passband control until the needle rests at 0 (center scale). When the receiver is tuned to an FSK signal, deflection of the needle to the right indicates reception on the mark channel, and deflection to the left indicates reception on the space channel.

The LEVEL position is used to adjust and monitor the amplitude of the audio input to the Demodulator. The input level is properly set when adjustment of the receiver audio gain control positions the meter needle to 0 DBM.

3.3.2.3 MARK AND SPACE INDICATORS. The MARK and SPACE indicators flicker when signals are being received on the mark and space channels. These indicators will also flicker when the receiver is tuned to noise only, thus providing a rough indication of noise balance in the mark and space channels.

3.3.2.4 SHIFT* VERNIER DIAL. The SHIFT* vernier dial setting indicates the input signal mark-to-space shift in Hz. The associated vernier potentiometer adjusts the local oscillator frequency for proper mixing with a space tone shift of 0 to 1000 Hz. (Rotate dial to full counterclockwise position for 0 shift.)

3.3.2.5 LIMITER IN-OUT SWITCH. The LIMITER IN-OUT switch inserts or removes the limiter from the Demodulator circuit. During receiver tuning, this switch is placed in the IN position. Afterwards, use of the limiter depends upon receiving conditions. Generally, the LIMITER switch should remain in the OUT position. For receiving conditions which include noise and/or fading, the operator must recognize the type of noise and fading in order to determine the best position of the LIMITER switch.

3.3.2.5.1 Noise. As far as the operator is concerned, noise is any undesired disturbance within the frequency range to which the receiver is tuned. This noise can be both atmospheric and manmade. Atmospheric noise (static) is caused by electrical storms, magnetic storms, etc. Manmade noise is caused by electrical appliances, automobile ignition systems, etc. Perhaps the worst type of noise that the operator will encounter is common to both the atmospheric and manmade categories. This noise is impulse noise. It is caused by such things as lightning discharges in the atmosphere, and arcing in automobile ignitions systems. Impulse noise is characterized by high amplitude and short duration bursts of energy. To counteract it, the LIMITER switch must be placed in the IN position.

3.3.2.5.2 Fading. Fading is any variation in signal strength at the receiver. The operator will most probably experience the following types of fading: frequency selective fading, flutter fading, and back scatter fading.

Frequency selective fading is a phenomenon in which signals of slightly different frequencies are not propagated with the same amplitude and phase they had at the transmitter. The mark and space signals will thus vary independently with this type of fading. To counteract frequency selective fading, the full effect of the Decision Threshold Computer (DTC) must be realized. The LIMITER switch is therefore placed in the OUT position.

Flutter fading is a very rapid type of fading produced by an unstable propagation medium. Since the rate of fading is too fast for the time constants of the DTC circuit, optimum operation is obtained by placing the LIMITER switch in the IN position.

Back scatter is a phenomenon produced when the transmitted signal passes beyond the receiving zone, returns to earth, and is then reflected backwards into the receiving zone. Signals propagated

in this manner are usually weak, and are recognized by a rapid fade or flutter. To counteract this type of fading, the LIMITER switch is placed in the IN position.

NOTE

A good general rule to follow in using the LIMITER switch is:

When in doubt,
Leave it out.

3.3.2.6 NORMAL*-STANDBY SWITCH. This switch controls the output circuit. In the NORMAL* position, the Demodulator output keys the output circuit. In the STANDBY position, the Demodulator output is held in steady mark. This latter position is used during tuning.

3.3.2.7 NORMAL*-REVERSE SWITCH. This switch is used to reverse the mark and space signals at the output of the detector, thereby permitting the output to function with the proper mark-space relationship. The NORMAL* position is used when the marks and spaces are properly positioned both at the transmitter and at the receiver. The REVERSE position is used when the marks and spaces either are transmitted "upside down" or are tuned improperly at the receiver.

3.3.2.8 AUTO M/H-NORMAL * SWITCH. This switch inserts or removes an automatic mark/hold (auto-start) circuit at the output loop of the Demodulator. The mark/hold circuit will function only when the LIMITER switch is in the IN position, and the MODE M-N*-S switch is in the N* position. Generally, the AUTO M/H-NORMAL* switch is placed in the NORMAL* position.

3.4 OPERATING THE EQUIPMENT

Figure 3-3 is a flow chart diagram which shows the operator, in a suggested step-by-step form, how to operate the Demodulator and its associated receiver. Obviously, the flow chart cannot include all possible operating situations. Some steps refer the operator to particular paragraphs in the manual for a more detailed explanation of the procedure. As the operator acquires additional experience, he will doubtlessly find many procedural short cuts for obtaining optimum performance from the equipment.

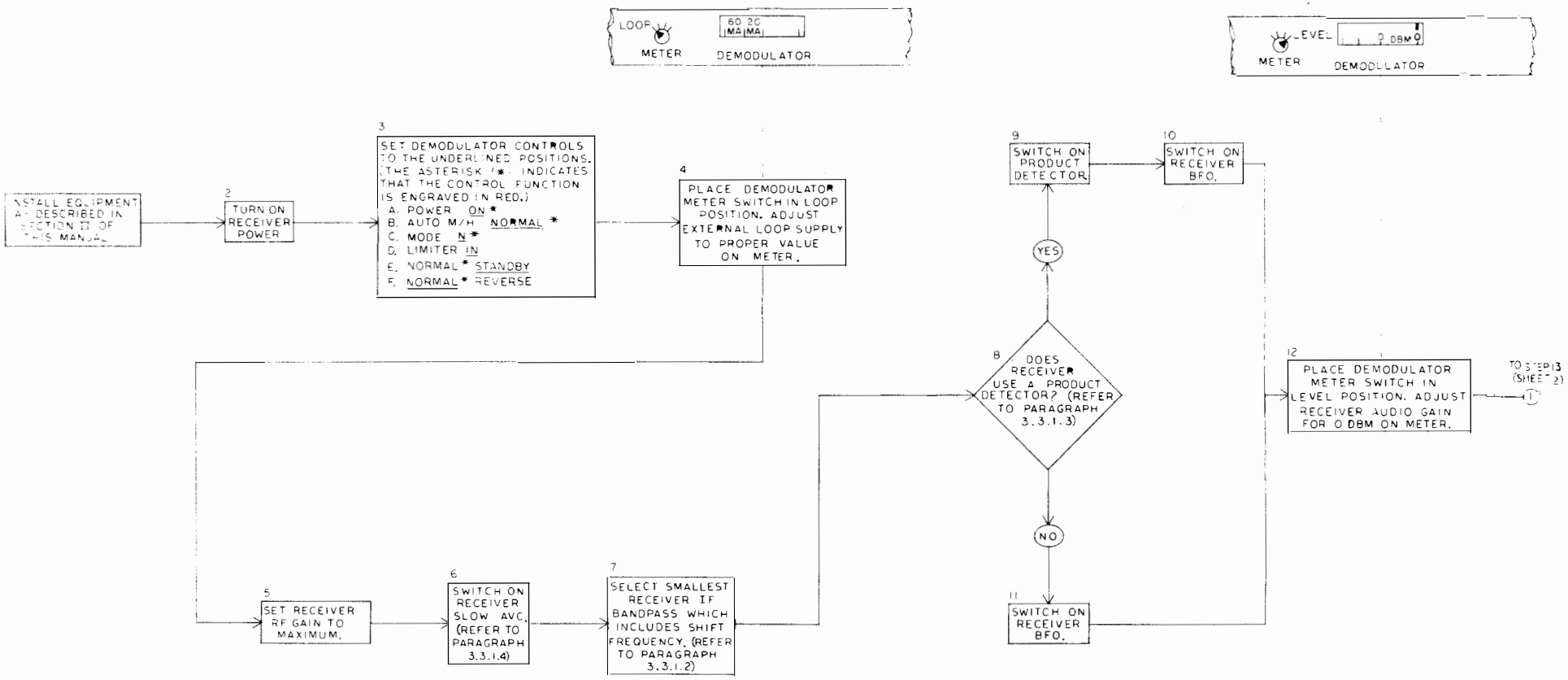


Figure 3-3. Flow Chart Operation of FSK Demodulator
(Sheet 1 of 2)

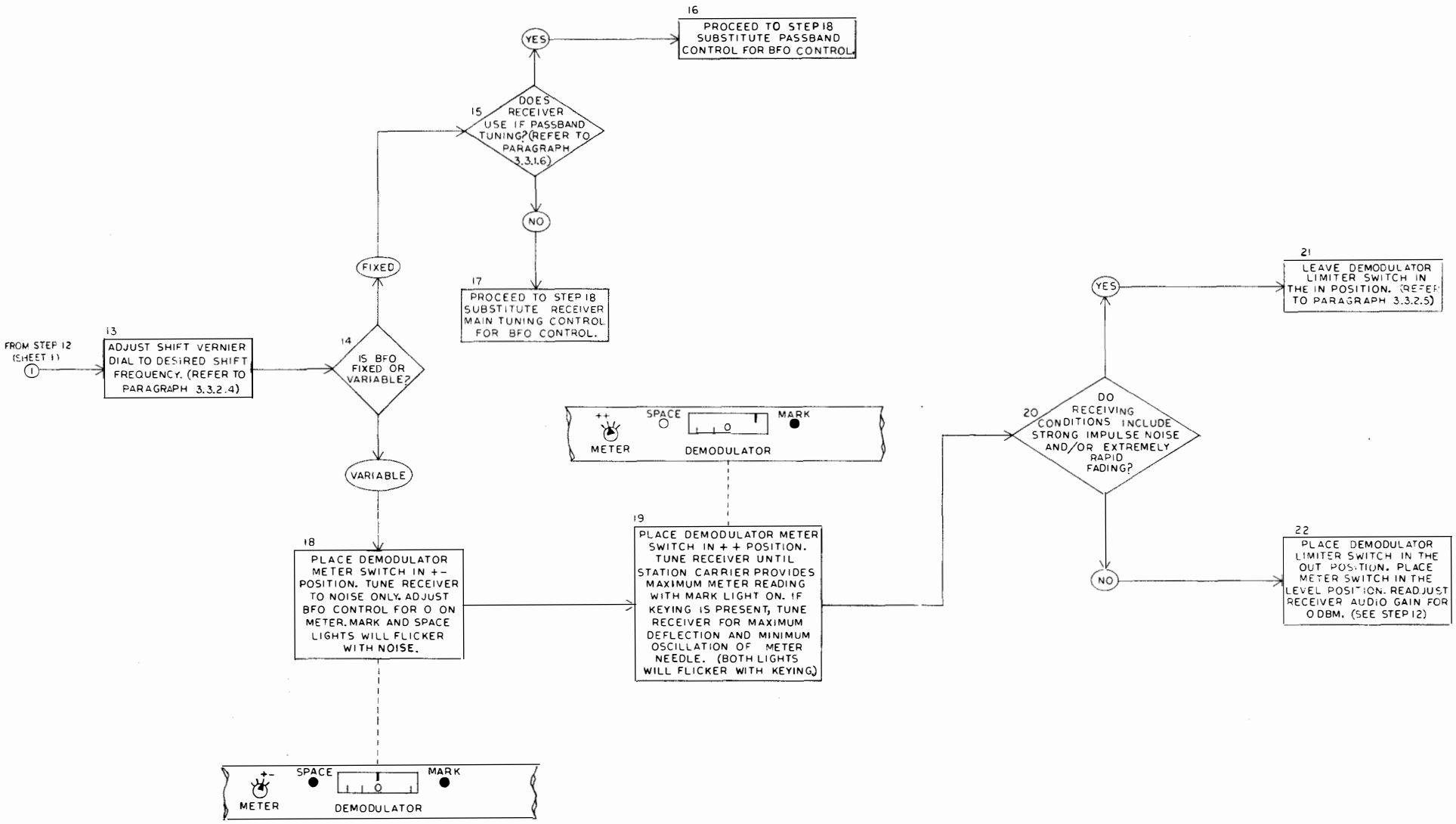


Figure 3-3. Flow Chart Operation of FSK Demodulator
(Sheet 2 of 2)

SECTION IV

THEORY OF OPERATION

4.1 FUNCTIONAL DESCRIPTION

A functional block diagram of the Model 1203 FSK Demodulator is shown in Figure 4-1. An external communications receiver supplies frequency shift keying audio signals at zero dbm level to the Demodulator. The input signals are initially connected to an input band-pass filter. Output signals from the filter are then applied to an amplifier/limiter circuit.

The amplifier/limiter circuit provides either amplification or limiting as required for optimum performance of the Demodulator. A front panel switch permits insertion or removal of the limiting action. The amplifier/limiter output is then routed to the mark channel band-pass filter and the space channel mixer.

The mark channel filter separates the mark tone from the space tone for application to a mark channel detector circuit.

The space channel mixer circuit operates in conjunction with a local oscillator to provide a correct space tone for application to a space channel filter. The variable frequency shift input (0 - 1000 Hz) dictates the use of a mixer-local oscillator arrangement to provide a single space tone to the space channel filter. The local oscillator frequency is adjustable via a front panel vernier control. This control is set to read the frequency shift desired.

The space channel filter output tone is then applied to a space channel detector circuit. Both the mark and space channel filters have a narrow band-pass, designed for aiding the detectors in achieving optimum signal detection. The detector outputs are summed and then applied to a post-detection low-pass filter. After post-detection filtering, the resultant signal is connected to a Decision Threshold Computer.

The Decision Threshold Computer (DTC) is a variable threshold device which automatically determines the halfway or transition point between the mark and space signals. The DTC is particularly advantageous with fading signal conditions. If one channel should fade during keying, the signal would remain centered about the decision level. If the keyed signal should rest in a steady state (mark condition), the DTC would maintain a steady mark output. This latter operation provides maximum discrimination against impulse noise and sudden fades on the mark channel in the absence of keying. Output signals from the DTC are connected to a loop keyer for operating an external teleprinter.

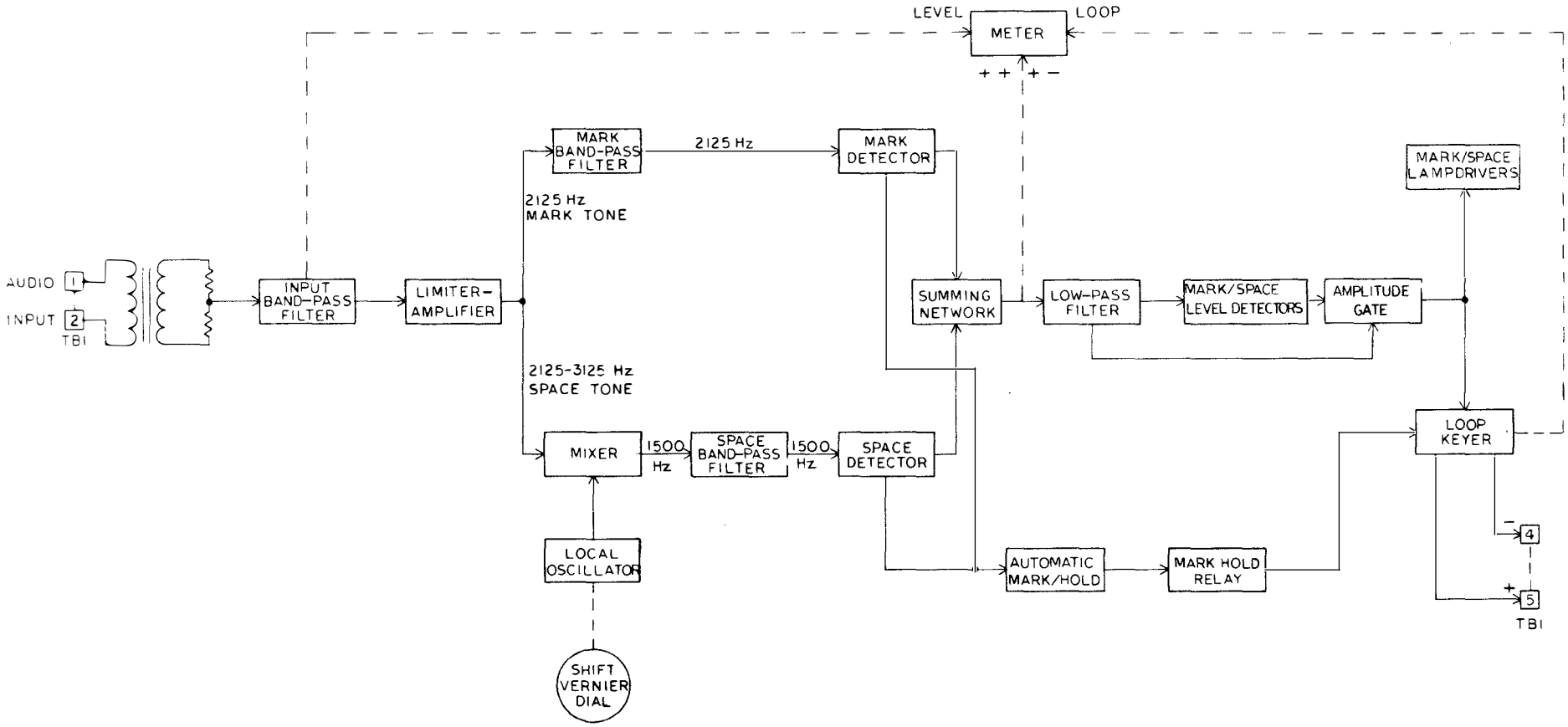


Figure 4-1. Block Diagram, Model 1203 FSK Demodulator
C1101

An additional output from each channel detector is used to control an automatic mark/hold circuit (AUTO M/H). This circuit functions as an auto-start system, and returns the Demodulator output to the mark state when the received signal drops below the noise level, or when non-FSK signals such as Morse Code or noise are present.

A front panel meter permits four circuit functions to be adjusted and monitored. These circuit functions are selected by a four-position METER switch labeled LOOP, ++, +-, and LEVEL. In the LOOP position, the meter monitors the current in the teleprinter circuit. In the ++ position, the meter is used to tune the receiver to an FSK signal. In the +- position, the meter is used to obtain equal amplitude response (noise balance) from the mark and space channels. In the LEVEL position, the meter reads the audio input level from the receiver.

4.2 CIRCUIT DESCRIPTION

4.2.1 INPUT CIRCUIT

The input circuit of the Model 1203 consists of audio coupling transformer T1 (refer to Figure 6-1). The transformer primary matches the 500-ohm audio output terminals normally found in better quality communications receivers.

4.2.2 INPUT BAND-PASS FILTER

The input band-pass filter consists of capacitors, inductors, and associated resistive matching networks (refer to Figure 6-1). The filter bandwidth is just wide enough to pass the mark and space frequencies and exclude unwanted noise. Thus the filter bandwidth is 1000 Hz (2125-3125 Hz) to allow for frequency shifts from 0 to 1000 Hz. Output signals from the filter are connected to a limiter circuit.

4.2.3 AMPLIFIER/LIMITER CIRCUIT

The limiter circuit consists of differential amplifiers Q1 through Q5, and the LIMITER IN-OUT switch (refer to Figure 6-2). The limiter is used primarily during tuning to provide a constant signal level. The limiter is also useful in reducing the effects of certain types of noise and flutter fading.

The first section of the limiter consists of differential amplifier Q1-Q2 and its associated constant current source Q3. Output signals from this section are coupled through T1 to the opposite inputs of differential amplifier Q4-Q5. Together, the two differential amplifiers limit the input signal, with Q4-Q5 providing the initial limiting, and Q1-Q2 being captured as the signal

level increases. The OUT position of the LIMITER switch reduces the amplitude of the input audio by connecting an attenuator across the input of the input band-pass filter. Output signals at the collectors of Q4 and Q5 are routed respectively to the mark channel band-pass filter and the space channel mixer.

4.2.4 SPACE CHANNEL MIXER AND LOCAL OSCILLATOR

The Space Channel Mixer consists of low-pass filter (R66, L11, C35, and C36) matching resistance pad R64, R67, and R68, mixing transformer T2, and output amplifier Q18 (refer to Figure 6-1). The Local Oscillator consists of free-running multivibrator Q4-Q5, divide-by-two circuit Q14-Q15, amplifiers Q16-Q17, and a voltage feedback circuit comprising one-shot Q6-Q7, feedback amplifiers Q10-Q13, differential amplifier Z1, and variable voltage source Q3. The Space Channel Mixer accepts input signals from both the amplifier/limiter circuit and the local oscillator, and combines these two signals to produce a 1500 Hz difference frequency for application to the input of the space channel filter.

The input signal from the amplifier/limiter circuit is routed through low-pass filter L11, R66, C35, before connection to the mixer circuit. The filter shapes the amplifier/limiter signal in order to reduce the harmonic content of the mixer output. After shaping, the amplifier/limiter signal is coupled through resistance pad R64, R67, and R68 to one input of mixing transformer T2. The other input to T2 is supplied by local oscillator divider Q14-Q15.

The oscillator is essentially a free-running multivibrator with one base connected to variable voltage source Q3. The voltage feedback network and the local oscillator utilize zener regulator CR6 to provide the required local oscillator stability. The oscillator frequency from divider Q14-Q15 is adjustable from 3625 to 4625 Hz by means of the front panel SHIFT* vernier dial. This dial indicates frequency shift between 0 and 1000 Hz corresponding to the above-mentioned oscillator frequency range. Potentiometers R45 and R46 are used in conjunction with the SHIFT* vernier control to provide accurate calibration at the high and low ends, respectively, of the oscillator frequency scale.

Initial selection of a shift frequency by means of the front panel SHIFT* vernier dial (R91) causes oscillator Q4-Q5 to run at the frequency related to the selected shift. In operation, the control voltage is applied to the oscillator via differential amplifier Z1 and variable voltage source Q3. The oscillator output is used to trigger one-shot Q6-Q7. This one-shot provides two outputs, one for the local oscillator output circuit, and one for the voltage feedback generating circuits.

The first output drives divide-by-two counter stage Q14-Q15 to produce equal and opposite phase square waves. The square waves are then individually amplified by Q16-Q17 and connected to mixing transformer T2.

The second output from one-shot Q6-Q7 enters the voltage feedback generating circuits by way of Q10-Q13. This output is a constant duration pulse which provides a corrective action to offset oscillator drift. In operation, the one-shot output (via Q10-Q13) forms an input to differential amplifier Z1; the other input to Z1 is derived from the SHIFT* vernier dial, as explained previously. If the oscillator begins to drift from the selected frequency, the pulse repetition rate of the one-shot increases or decreases in accordance with the drift, and the resultant voltage change is sensed by Z1. The total effect of this action is that Z1 varies the impedance characteristics of Q3 in order to correct the local oscillator frequency.

The local oscillator and incoming space tone signals are combined in mixing transformer T2 to produce a 1500 Hz difference frequency output. This difference frequency is routed through driver stage Q18 and applied to the space channel band-pass filter.

4.2.5 MARK AND SPACE CHANNEL BAND-PASS FILTERS

The channel band-pass filters provide separate predetection filtering of the mark and space frequencies. Each filter is a three-pole Butterworth designed for optimum response without loss of the input signal-to-noise ratio. Both filters have a bandwidth of 85 Hz. Q1 and Q2 (Figure 6-1) are the respective input coupling elements for the channel filters. The output from the space channel filter is routed through contacts of the MODE switch and connected to amplifier stage Q7. The output from the mark channel filter is routed through individual contacts of the MODE switch and connected to amplifier stage Q6.

The front panel MODE switch permits selection of mark only (M position), space only (S position), or both mark and space (N* position) from the channel band-pass filters. If the M position is selected, the output from the mark channel filter is routed to the base of Q6. Q7 receives no input at this time. Similarly, if the S position is selected, the output from the space channel filter is routed to the base of Q7. Q6 then receives no input at this time. If the N* position is selected, the output from each filter is routed to its respective amplifier stage.

Q6 and Q7 are functionally identical stages which respectively accept the mark and space tones for amplification and coupling to separate detectors. Additional outputs are obtained at the

collectors of Q6 (J5-15) and Q7 (J5-S) for connection to an external data tuning and display monitor. These outputs are available at rear panel connector J1.

4.2.6 DETECTOR CIRCUITS

Active detector circuits are used to recover the envelopes of the mark and space signals. The mark signal detector consists of stages Q8 and Q9 (refer to Figure 6-2). The space signal detector consists of stages Q10 and Q11. Circuit operation is similar to that of the infinite impedance detector. Diodes CR22 and CR23 supply base bias voltages for the detectors. The detected outputs, negative mark at C5 and positive space at C6, are summed in the emitter-follower outputs of Q8-Q9 and Q10-Q11. The summed outputs are then coupled through complementary emitter-follower Q14-Q15 to the input of a low-pass post-detection filter. Diodes CR5 and CR6 provide base-emitter compensation for complementary emitter-follower stage Q14-Q15. Potentiometer R30 is used to balance the junction of CR5, CR6, and R29 for an approximate zero level.

The signal outputs from the mark and space tone detectors are also used for two additional circuit applications. The first application is diversity operation. The diversity outputs, which are obtained at C5 and C6, are connected to terminals U and 13, respectively, of connector J5. These outputs are available at rear panel connector J2. The other application is automatic mark/hold or auto-start. Since the mark/hold circuit normally requires negative inputs from each tone detector, it is necessary to invert the space signal. This is done by developing a negative version of the space signal through a third detector circuit (Q12-Q13). The mark/hold circuit inputs are obtained at C5 and C7. Operation of the mark/hold circuit is discussed in Paragraph 4.2.12.

4.2.7 POSTDETECTION FILTER

The Postdetection Filter (refer to Figure 6-1) is a three-pole Butterworth low-pass filter which functions in conjunction with the input circuit band-pass filter and the mark and space channel filters to provide the minimum overall system bandwidth necessary for optimum detection of the FSK signals. Low-pass filters for specific frequency shifts and keying rates are available on special order. The postdetection filter consists of capacitors, an inductor, and associated resistive matching networks. Two switch-selectable meter functions at the input to the filter permit the received signals to be properly tuned and balanced. The meter circuits are described in Paragraph 4.2.11. The output from the low-pass filter, which consists of the detected and summed mark-space tones, is routed to the Decision Threshold Computer.

4.2.8 DECISION THRESHOLD COMPUTER

The Decision Threshold Computer (DTC) adjusts the transition point (decision level) between mark and space signals in accordance with predetermined information concerning the amplitude of the two signals. Figure 4-2 illustrates what the DTC does. It is important to remember during this discussion that either signal channel contains the complete message or transmitted information. At point A, optimum receiving conditions exist, and the mark and space signals are of equal amplitude. The DTC thus determines the transition point to be halfway between mark and space, or at the zero level. The decision level is represented by the dotted line.

Assume that the space signal is affected by selective fading (point B), and as a result, its amplitude is gradually reduced to the zero level. Through the action of the DTC, the decision level is raised approximately halfway between zero and maximum mark amplitude. During this time, all information is obtained from the mark channel both accurately and without interruption. After the fading condition has ended, the space signal regains its original amplitude, and the decision level returns to the zero position.

If the received signal goes to a steady mark and remains there (point C), the decision level does not remain at the halfway point as it did for the fading space signal. Instead, the decision level falls to zero. The reason for this is that the DTC does not know the actual level of the space signal, since it cannot accumulate valid data in the absence of keying. Therefore, for lack of better information, the DTC assumes that the space level is the same as the mark level, and returns the decision level to zero. This is the most probable level and the DTC will always return to it for a steady state signal.

A simplified diagram of the DTC circuit is shown in Figure 4-3. Since the mark and space channels are functionally identical, only the mark channel is described. In operation, when a keyed signal is applied at point X, the negative mark portion of the signal charges capacitor C2 via diodes CR1, CR3, and capacitor C1. This latter capacitor has a long charging time constant, and thus follows the signal variations without accumulating any appreciable charge. When the input signal drops below the peak negative mark level or changes to a space, diode CR3 is back-biased, and capacitor C2 then begins to discharge slowly through R3. The same action (with opposite polarities) takes place in the space channel for the space portion of the input signal. If the signals in each channel are equal in amplitude, the resultant summed output at point Y is zero. This condition corresponds to point A in Figure 4-2, where the decision threshold is at the zero level.

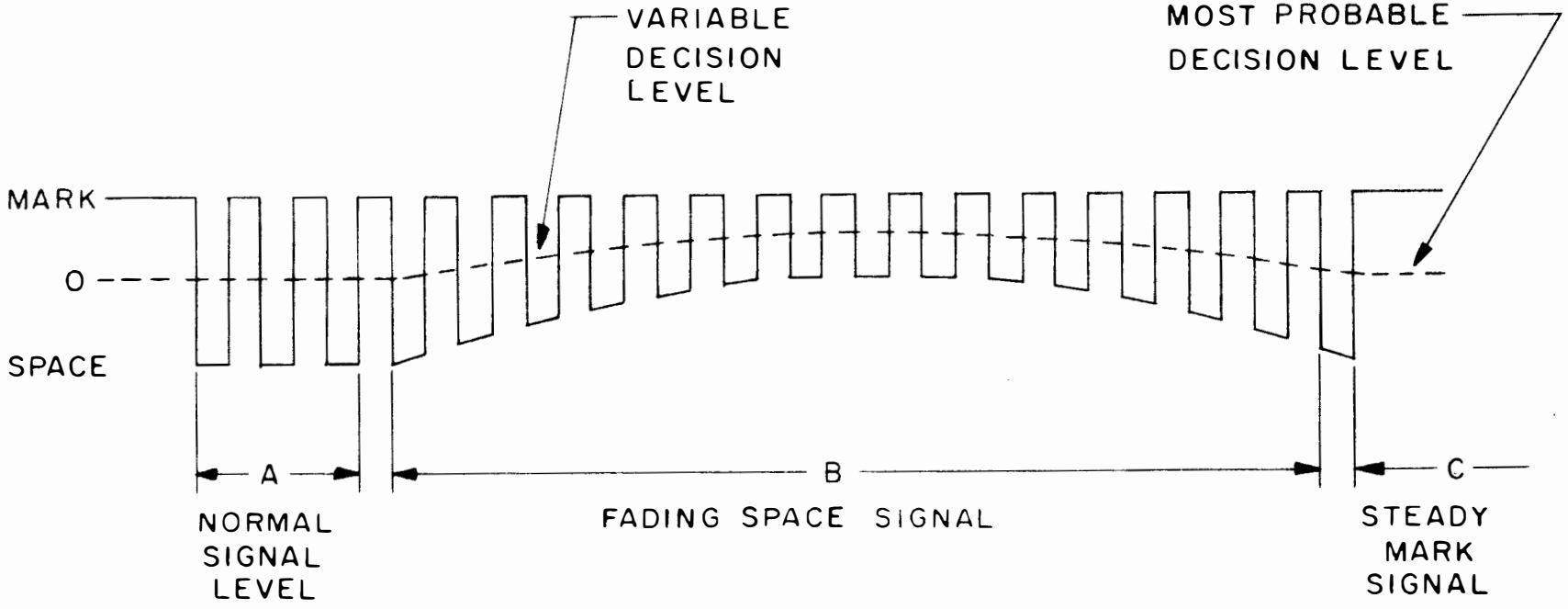


Figure 4-2. Decision Levels in the DTC

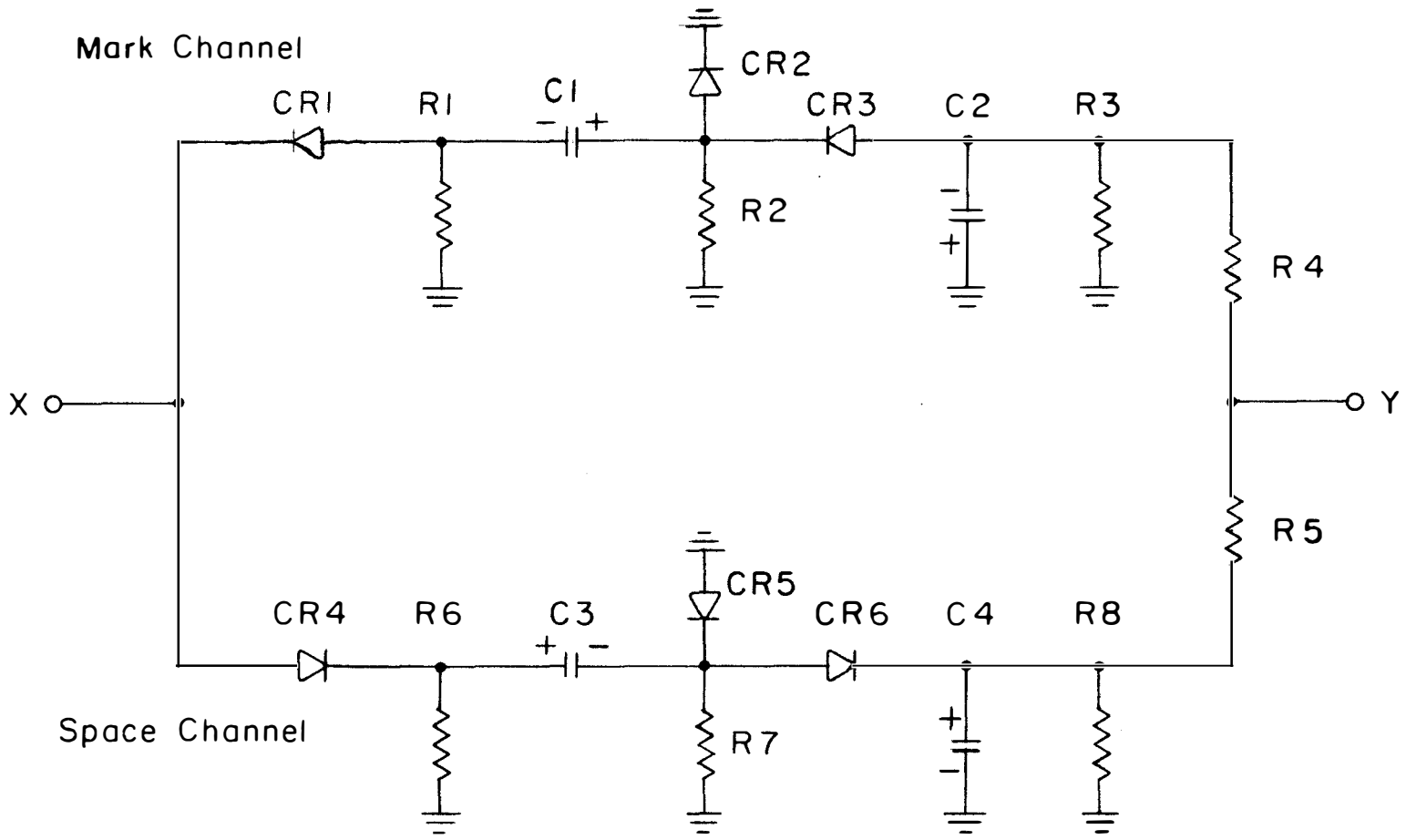


Figure 4-3. Threshold Generator, Simplified Circuit Diagram

If the space input signal at point X of Figure 4-3 momentarily fades, the output at point Y rises to one-half the amplitude of the mark signal. The operation takes place in this manner: At the beginning of the space signal fade, a valid sample of the previous space level is stored in capacitor C4. This charge level in C4 is slowly reduced by the discharge path through R8. Since information is still being received on the mark channel, eventually, only the mark output remains. The resultant output at point Y (now equally divided by the summing resistors) becomes equal to one-half the input level. This condition corresponds to point B in Figure 4-2.

If the input signal at point X in Figure 4-3 becomes a steady mark, capacitors C1 and C2 both charge to the peak signal level. Capacitor C1 remains at this level, and capacitor C2 discharges through R3. Since diode CR3 is now back-biased, capacitor C2 can no longer acquire a charge, and the output level at point Y drops to zero. This condition corresponds to point C in Figure 4-2.

Refer to the schematic diagram of the Decision Threshold Computer (Figure 6-2). The combined mark and space output from the post-detection filter is simultaneously applied to the input of the DTC and to one input of the amplitude gate (Q26-Q27). Diodes CR11 and CR12, at the DTC input, provide base-emitter compensation for stages Q16 and Q21, respectively. The upper circuit is the mark level detector, and the lower circuit is the space level detector. Since both circuits are functionally identical, only the mark circuit is described.

The input to the mark level detector is coupled through diode CR11 to the base of emitter-follower Q16. The output from Q16 is then coupled through a complementary emitter-follower consisting of transistors Q17-Q18. This complementary stage supplies the current gain required by the level detector storage circuits. Capacitor C10 couples the output from Q17-Q18 to the base of emitter-follower Q20.

Capacitor C10 has a long charging time constant for following the keyed signal. Its discharge time constant, however, is very short. The output from C10 is selected by the N* position of the MODE M-N*-S switch. For reception of a steady mark signal, capacitor C10 must be in the circuit. Use of the other switch positions (M and S) provides a threshold level which shifts in the direction of the received signal.

The negative mark input at the base of Q20 charges capacitor C12 to the peak signal amplitude. Resistor R92 is the discharge path

for C12. The output of the mark level detector is then combined with the output of the space level detector at the junction of R48 and R59. This resultant signal is used as a reference level for the amplitude gate.

4.2.9 AMPLITUDE GATE

Amplitude Gate Q26-Q27 (Figure 6-2) accepts outputs from the DTC and the postdetection filter at its separate control inputs, and provides a difference output representative of a mark or space decision. The reference input at the base of Q26 is supplied by the DTC. The variable signal level at the base of Q27 is supplied from the output of the postdetection low-pass filter. Output signals from the amplitude gate are obtained at the junction of R64-R65 in the collector circuit of Q27. Constant current source Q28, in the emitter circuit of the amplitude gate, provides common mode rejection.

When normal marks and spaces are being received, the detected level at the base of Q26 is centered about zero. The signal input at the base of Q27 thus varies about this level to produce a positive collector output for marks, and a negative collector output for spaces. These outputs are coupled through Q29 and Q30 to the junction of R69 and R72. If the signal at this point is a positive mark, Q33 is held off, and its negative collector output turns on the MARK indicator (DS2) via Q32. Simultaneously, the positive mark at the junction of R69 and R72 closes the output loop via the NORMAL* contacts of the NORMAL*-REVERSE switch and Q37. If the signal at the junction of R69-R72 is a negative space, the SPACE indicator (DS1) is turned on via Q31, and the output loop is opened via the NORMAL* contacts of the NORMAL*-REVERSE switch and Q37.

During fade-out periods on one channel, the amplitude gate continues to provide an output from the non-fading channel. For example, if the space signal fades, the DTC output at the base of Q26 eventually becomes some negative level from the mark channel. The base input to Q27 at this time is a zero-level signal, since the signal transition is from a mark to a faded space. Transistor Q27 thus provides a negative output which lights the SPACE indicator (DS1) and opens the output loop. During the transition from faded space to negative mark, Q27 provides a positive output which lights the MARK indicator (DS2) and closes the output loop.

During a steady mark condition, the DTC output at the base of Q26 drops to the zero level. Since the base input to Q27 is negative at this time, Q27 provides a positive output which places the output circuit in the mark condition.

4.2.10 OUTPUT LOOP CIRCUIT

The output loop circuit consists of a transistor switch (Q7) and a high level keyer module, NO982A (refer to Appendix HK), mounted on the power supply P.C. board (NO1378). Refer to Figure 6-3. In operation, a positive mark level from driver transistor Q37 of the detector circuit provides a positive turn-on voltage to the base of transistor Q7 in the output loop circuit, turning on the mark keyer. The loop current can be monitored by placing the METER switch to the LOOP position.

An optional second high level keyer may be used for polar high level keying. The keyer is installed on the power supply board in the position marked SPACE. When using the polar high level keying option, jumpers A and B are removed. The space high level keyer is turned on by transistor switch Q8.

EIA-RS-232 or MIL-STD-188C compatible outputs may be selected by inserting the Molex connector, on the power supply board, into the appropriate position. If the EIA position is selected, a negative mark signal is output from operational amplifier Z3. If the 188 position is selected, zener diodes CR1 and CR2 limit the output of Z3 to a +6 v mark and a -6 v space signal level.

4.2.11 METER CIRCUITS

The meter circuits provide four, front panel, switch-selectable functions labeled LOOP, ++*, +-, and LEVEL. Refer to Figure 6-4. In the LOOP position, the METER switch connects the meter in the output loop circuit. This permits the loop current to be adjusted and monitored. The meter has markings for loop currents of 20 ma and 60 ma (full scale).

In the ++* position, the METER switch connects the meter through a bridge circuit (Figure 6-2) to the input of the postdetection low-pass filter. This switch position permits the receiver signal to be tuned visually for maximum signal amplitude as explained in Section III of this manual.

In the +- position, the METER switch connects the meter through an 18K resistor to the input of the postdetection low-pass filter. This switch position permits the mark and space channels to be balanced for noise as explained in Section III.

In the LEVEL position, the METER switch connects the meter through a full-wave bridge circuit (Figure 6-1) to the input of the band-pass filter. This switch position thus permits the audio input level to be adjusted and monitored as explained in Section III.

4.2.12 AUTOMATIC MARK/HOLD CIRCUIT (AUTO-START)

The Automatic Mark/Hold circuit (Figure 6-2) is essentially an auto-start system which places the output of the Model 1203 in the mark state when the received signal drops below the noise level, or when non-FSK signals such as Morse code or voice are present. The mark/hold circuit functions only when the AUTO M/H-NORMAL* switch is in the AUTO M/H position, the LIMITER switch is in the IN position, and the MODE switch is in the N* position.

Basically, the automatic mark/hold circuit functions to open or close the demodulator output loop via contacts of a relay. Control signals for this action are supplied by the output of the mark and space channel detectors. During normal reception of marks and spaces, a negative input appears at the cathode of either diode CR19 or diode CR20. This negative input turns on transistor stage Q34. The resultant positive-going collector voltage of Q34 reverse-biases CR21, thereby blocking the forward bias path for Q35. In its off state, Q35 forward biases relay driver Q36. This operation energizes the collector circuit relay of Q36, thus preventing the relay contacts from closing the output loop.

During abnormal reception, if both diode inputs drop below a certain level, Q34 is turned off, and capacitor C16 quickly charges through R82 and CR21. The discharge of C16 through R85 and the base-emitter circuit of Q35 turns on Q35, and turns off relay driver Q36. This operation de-energizes the collector circuit relay of Q36, thus connecting the relay contacts across the output loop, and placing the Demodulator in mark/hold. Since the discharge time of C16 is much longer than the charge time, the mark/hold condition will remain until C16 is almost completely discharged.

4.2.13 POWER SUPPLY

The power supply circuits are contained on P.C. board NO1378 and are shown schematically on Figure 6-3.

The power supply may be operated from either a 110 vac or 220 vac power source. Switch S1, located on the power supply board must be set to the corresponding power source position otherwise serious damage to the equipment may result. Switch S1 also controls the ac input to the optional loop supply (refer to Appendix AA) thru connector J11.

The ac output of transformer T1 is rectified by full-wave bridge rectifier CR15 thru CR18, filtered, and zener regulated to produce ±24 vdc. Also, unfiltered and unregulated -24 vdc is taken from the negative leg of the bridge rectifier to provide lamp voltage.

A second full-wave bridge rectifier, consisting of CR6 thru CR9, is used to supply the regulated ±11.5 vdc. Precision voltage regulator Z1 is a temperature compensated reference device and is controlled by feedback from potentiometer R22. The regulated +11.5 vdc is provided thru series regulator transistor Q1 and current limiting resistor R10 to board connector J3, pin B.

The regulator circuit for the -11.5 vdc consists of Z2 and Q5 which act as feedback elements to control voltage changes, current limiter Q4 and series-pass transistors Q2 and Q3. The regulated -11.5 vdc is output on board connector J3, pin K.

SECTION V

CHECKOUT AND ALIGNMENT PROCEDURES

5.1 CHECKOUT

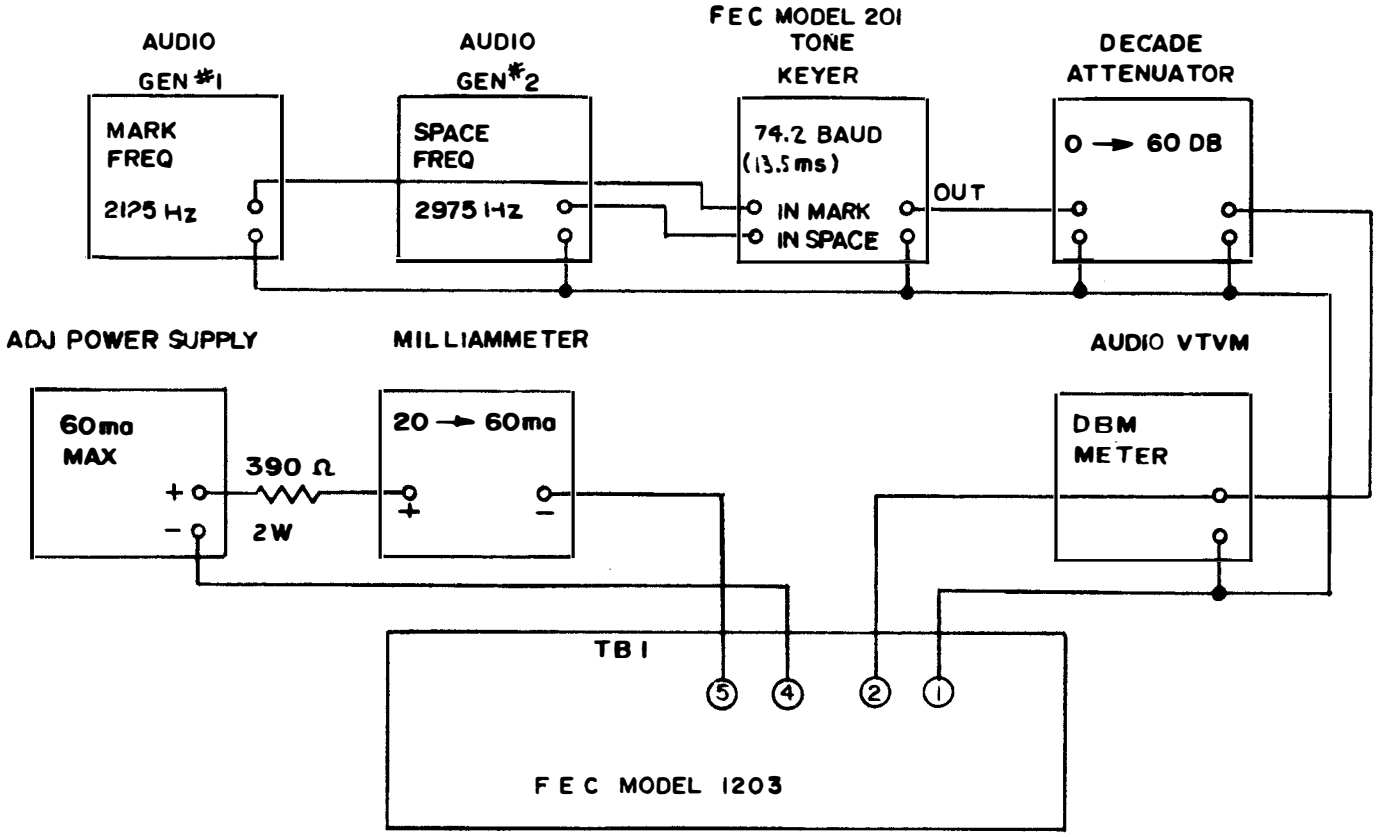
5.1.1 REQUIRED TEST EQUIPMENT

1. Oscilloscope, Tektronix Model 531A.
2. Audio Generator (2), Hewlett-Packard Model 200CD.
3. Pulse Pattern Generator, Frederick Electronics Model 201.
4. Decade Attenuator, General Radio Co. Model 1450-TA.
5. AC Vacuum Tube Voltmeter, RCA Model WV-76A.
6. DC Milliameter, (150 ma), Sensitive Research Instrument Corporation.
7. Variable DC Power Supply, 24 volts, 60 ma.
8. Voltmeter, Triplett Model 630.
9. Loop current limiting resistor, 390 ohms, 2 watt.
10. Electronic Counter, Transistor Specialties, Inc. Model 373.
11. Potentiometer, 2500 ohm, 10 watt. (Not required if Model 1203 uses external loop supply.)

5.1.2 INITIAL SETUP

The test setup for the Standard Model 1203 is shown in Figure 5-1. After the test setup is completed, perform the following operations:

1. Adjust audio generator #1 to a mark frequency of 2125 Hz. Use a frequency counter for this adjustment.
2. Adjust audio generator #2 to a space frequency of 2975 Hz. Use a frequency counter.
3. Adjust pulse pattern generator tone keyer for a rate of 74.2 baud (13.5 milliseconds duration). Use oscilloscope for this adjustment.
4. Set decade attenuator controls to zero and set tone keyer for a steady mark output. Adjust mark output of audio generator #1 for zero dbm reading on audio vacuum tube voltmeter.
5. With decade attenuator controls still at zero, set tone keyer for a steady space output. Adjust space output of audio generator #2 for zero dbm reading on audio vacuum tube voltmeter. Return keyer to keyed mark and space output.
6. Connect oscilloscope ground to - terminal of filter capacitor C2 in Demodulator power supply. Refer to Figure 6-3, Power Supply Schematic Diagram.



FOR INTERNAL LOOP SUPPLY, PINS 4 AND 5 ARE WIRED AS BELOW

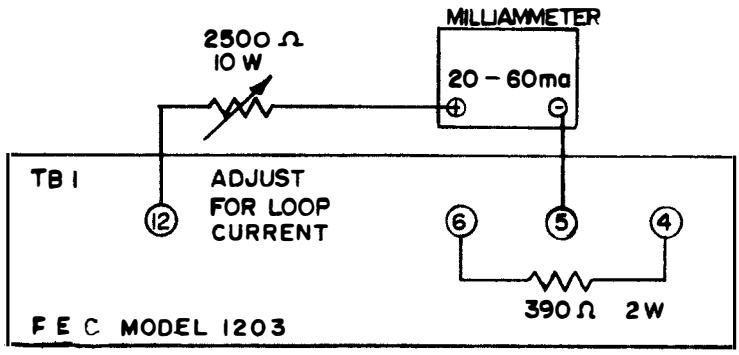


Figure 5-1. Model 1203 Test Setup

NOTE

The Demodulator front panel controls should now be set to the positions engraved in red. Unless otherwise stated, these control positions must be maintained throughout the following checkout procedures.

5.1.3 POWER SUPPLY CHECKOUT

With a nominal input voltage of either 110 vac or 220 vac, the dc voltages should be as listed in Table 5-1. All voltages should be referenced to the + side of capacitor C1. The ±11.5 v can be adjusted by potentiometer R22.

Table 5-1. Power Supply Voltages

MEASURING POINT	VOLTAGE
+ side of C6	+24 v ±10%
- side of C7	-24 v ±10%
+ side of C5	+11.5 +0, -.4 v
- side of C4	-11.5 +0, -.4 v

5.1.4 LOOP CURRENT CHECKOUT

With no input signal, proceed as follows:

1. Set METER switch to LOOP position.
2. Set NORMAL*-STANDBY switch to STANDBY position.
3. Adjust loop current to 60 milliamperes. Demodulator meter needle should read 60 ma.
4. Return NORMAL*-STANDBY switch to NORMAL* position.

5.1.5 LOCAL OSCILLATOR ALIGNMENT

Proceed as follows:

1. Connect electronic counter to Q15 collector of local oscillator divide-by-two flip-flop.
2. Set SHIFT* vernier dial to 0. (Rotate dial fully counterclockwise.)
3. Adjust potentiometer R46 for output frequency of 3625 Hz.
4. Rotate SHIFT* vernier dial to 1000. (Rotate dial fully clockwise to zero reading.)
5. Adjust potentiometer R45 for output frequency of 4625 Hz.
6. Repeat steps 2 through 5 until no further adjustment is required at either end of SHIFT* vernier dial.

5.1.6 NOISE BALANCE CHECKOUT

With no input signal, proceed as follows:

1. Place METER switch in +- position.
2. Adjust balance potentiometer R30 (rear panel of Demodulator) until MARK and SPACE lights either flicker or a point is reached where both lights are at half brilliance. This is the desired balance point. The meter needle should rest at center zero position.

NOTE

Another adjustment point may be reached in which the following conditions exist: 1) Both lights are off; 2) A very slight adjustment clockwise turns on one light; 3) A very slight adjustment counterclockwise turns on the other light. This threshold point is also correct.

5.1.7 SIGNAL LEVEL CHECKOUT

Proceed as follows:

1. Apply zero dbm input signal to Demodulator.
2. Set METER switch to LEVEL position and set LIMITER switch to OUT.
3. Check that level reading is zero dbm on Demodulator meter.

5.1.8 DETECTOR LEVEL CHECKOUT

Proceed as follows:

1. Apply zero dbm reversals at input to Demodulator.
2. Connect oscilloscope probe at junction of R71 and NORMAL*-REVERSE switch.
3. Set LIMITER switch to IN.
4. Set MODE switch to M.
5. Adjust mark channel potentiometer (R11 on standard filter board) for minimum bias distortion on oscilloscope.
6. Set MODE switch to S.
7. Adjust space channel potentiometer (R17 on standard filter board) for minimum bias distortion on oscilloscope.

8. Set MODE switch to N*. Bias distortion on oscilloscope should be negligible.
9. Connect oscilloscope probe at junction of R81 and R90. There should be no limiting from detector. If there is limiting, re-adjust R11 or R17 as necessary.

5.1.9 MARK/HOLD CHECKOUT

Proceed as follows:

1. Set AUTO M/H-NORMAL* switch to AUTO M/H.
2. Apply zero dbm input signal to demodulator.
3. Set METER switch to ++* position. Meter needle should read in MARK area.
4. Insert attenuation by means of decade attenuator until meter needle falls halfway between zero center and the letter M in the word MARK. Insert a minimum of -30 db attenuation. The Demodulator should still operate normally.
5. Continue inserting attenuation until meter needle falls just below halfway point obtained in step 4 above. If mark/hold relay does not close, adjust R90 until relay closes and Demodulator output goes to mark/hold condition.

NOTE

Closure of the mark/hold relay is accompanied by an audible click. The mark/hold condition may also be ascertained by reading the meter in the LOOP position. (A constant current will be indicated.)

6. Remove all attenuation. Note that after approximately five seconds, the mark/hold relay opens and normal operation is restored.

5.2 MARK AND SPACE BAND-PASS FILTERS

The mark and space band-pass filters are tuned at the factory for optimum operation. Normally, these filters should not require adjustment. If, at any time, it is suspected that the filters need adjustment, the technician should make sure that the apparent trouble is actually in the filters and not due to some external cause such as wrong signals, defective transistors, etc. It is important that the technician adopt a hands-off policy concerning the filters, since they can be easily misaligned and damaged.

As a first approach in determining whether a filter is defective, the technician should (if possible) substitute a known good filter board for the suspected one. If this test indicates that the filter is defective, the technician should then check the bandwidth of the filter.

5.2.1 MARK FILTER BANDWIDTH CHECKOUT

1. Set up equipment as described in Paragraph 5.1.2.
2. Connect audio vtvm at J4-S.
3. Insert steady mark (2125 Hz) at input to Demodulator by means of generator #1. Use a frequency counter for this adjustment. Note reading on vtvm.
4. Tune generator to a frequency higher than 2125 Hz until vtvm reading drops 3 db below that obtained in step 3 above. Check frequency with counter. The frequency should be approximately 2165 Hz.
5. Tune generator to a frequency lower than 2125 Hz until vtvm reading drops 3 db below that obtained in step 3 above. Check frequency with counter. The frequency should be approximately 2083 Hz.

NOTE

The filter bandwidth is correct if the two 3 db or half-power points are approximately symmetrical with respect to the center frequency of 2125 Hz. That is, the higher and lower frequencies should be displaced about the same amount from the center mark frequency with the tolerance stated above. If such is not the case, the filter needs to be aligned. Refer to Paragraph 5.2.3.

5.2.2 SPACE FILTER BANDWIDTH CHECKOUT

1. Set up equipment as described in Paragraph 5.1.2.
2. Connect audio vtvm at J4-14.
3. Insert steady space (2975 Hz) at input to Demodulator by means of generator #2. Use a frequency counter for this adjustment.
4. Set local oscillator frequency exactly 1500 Hz above space tone (4475 Hz). Use a frequency counter for this adjustment. Note reading on vtvm.
5. Tune generator #2 to a frequency higher than 2975 Hz until vtvm reading drops 3 db below that obtained in step 4 above. Check frequency with counter. The frequency should be approximately 3017 Hz.

6. Tune generator to a frequency lower than 2975 Hz until vtvm reading drops 3 db below that obtained in step 4 above. Check frequency with counter. The frequency should be approximately 2933 Hz.

NOTE

The filter bandwidth is correct if the two 3 db or half-power points are approximately symmetrical with respect to the center frequency of 2975 Hz. That is, the higher and lower frequencies should be displaced about the same amount from the center space frequency with the tolerance stated above. If such is not the case, the filter needs to be aligned. Refer to Paragraph 5.2.4.

5.2.3 MARK BAND-PASS FILTER ALIGNMENT

1. Set up equipment as described in Paragraph 5.1.2.
2. Disconnect one end of terminating resistor R14 from L5.
3. Connect audio vtvm between ground and junction of R13-L5.
4. Connect a jumper between ground and junction of C14-L6. This operation effectively detunes the resonant circuit immediately following the one being tuned.
5. Insert steady mark at input to Demodulator. Adjust L5 for maximum reading on voltmeter. Remove jumper.
6. Connect jumper between ground and junction of L7-C17. Adjust L6 for minimum reading on voltmeter. Remove jumper.
7. Adjust L7 for maximum reading on voltmeter. This completes the alignment procedure. Remove vtvm and input signal. Reconnect R14.

5.2.4 SPACE BAND-PASS FILTER ALIGNMENT

1. Set up equipment as described in Paragraph 5.1.2.
2. Disconnect one end of terminating resistor R20 from L8.
3. Connect audio vtvm between ground and junction of R19-L8.
4. Connect a jumper between ground and junction of C22-L9. This operation effectively detunes the resonant circuit immediately following the one being tuned.
5. Insert steady space at input to Demodulator. (Refer to Paragraph 5.2.2 steps 3 and 4.) Adjust L8 for maximum reading on voltmeter. Remove jumper.

6. Connect jumper between ground and junction of L10-C24. Adjust L9 for minimum reading on voltmeter. Remove jumper.
7. Adjust L10 for maximum reading on voltmeter. This completes the alignment procedure. Remove vtvm and input signal. Reconnect R20.

5.2.5 OUTPUT LOW-PASS FILTER

The output low-pass filter is of fixed design for the specified baud rate of 74.2 (100 wpm).

SECTION VI

SCHEMATIC DIAGRAMS

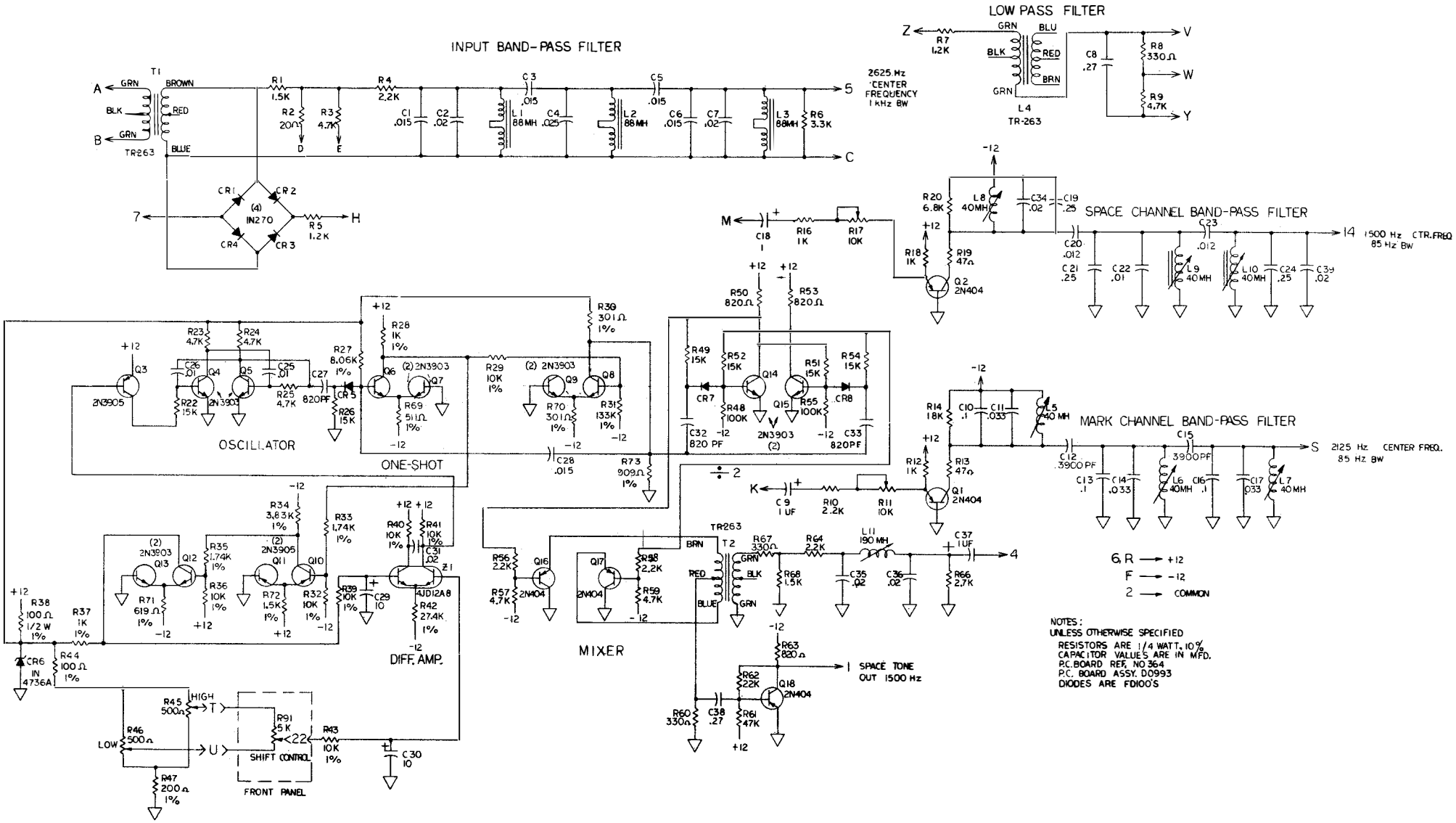


Figure 6-1. Mixer, Local Oscillator, and Filter Schematic Diagram D0995J

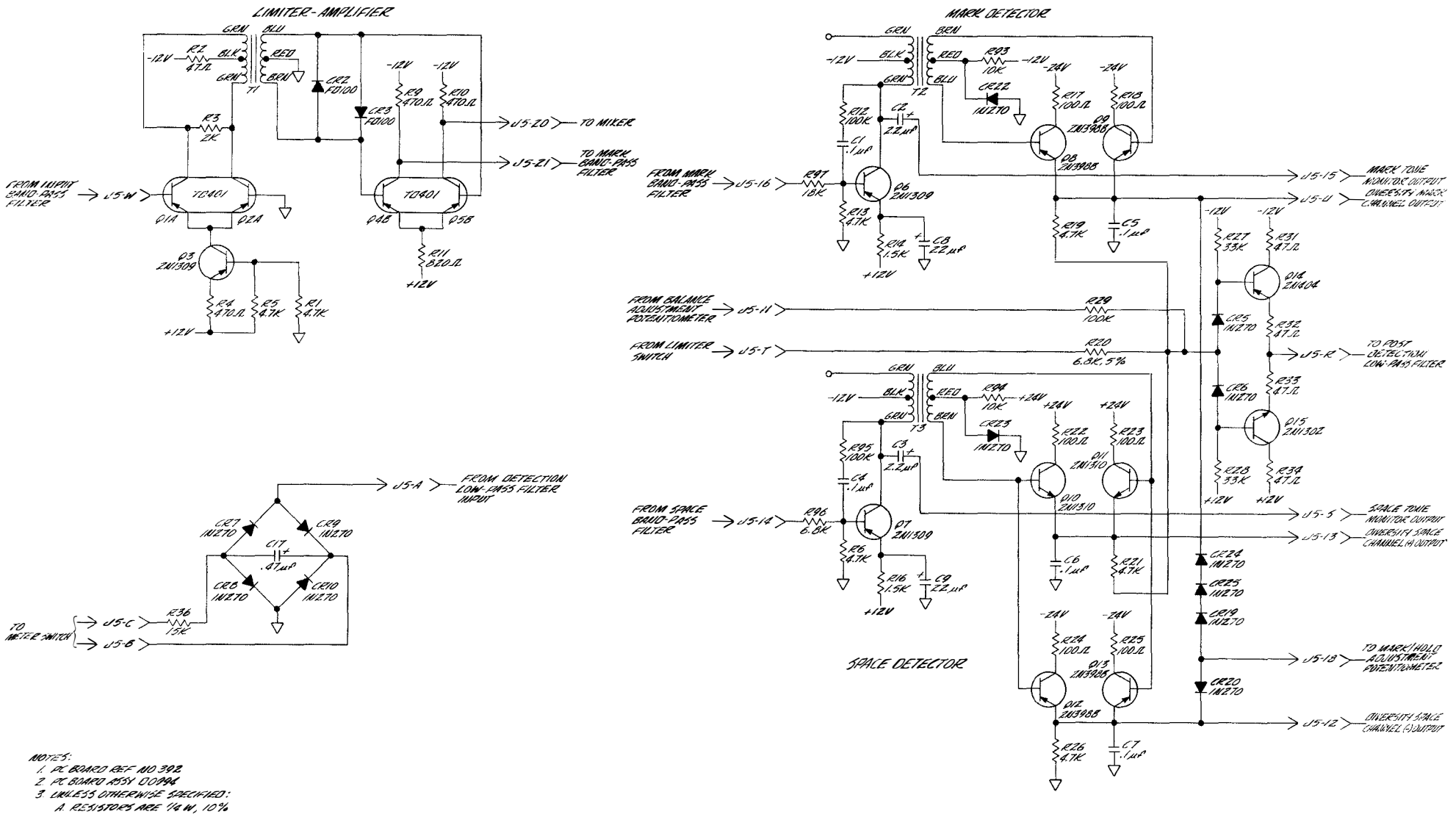


Figure 6-2. Detector Circuits Schematic Diagram
D3668A, Sheet 1

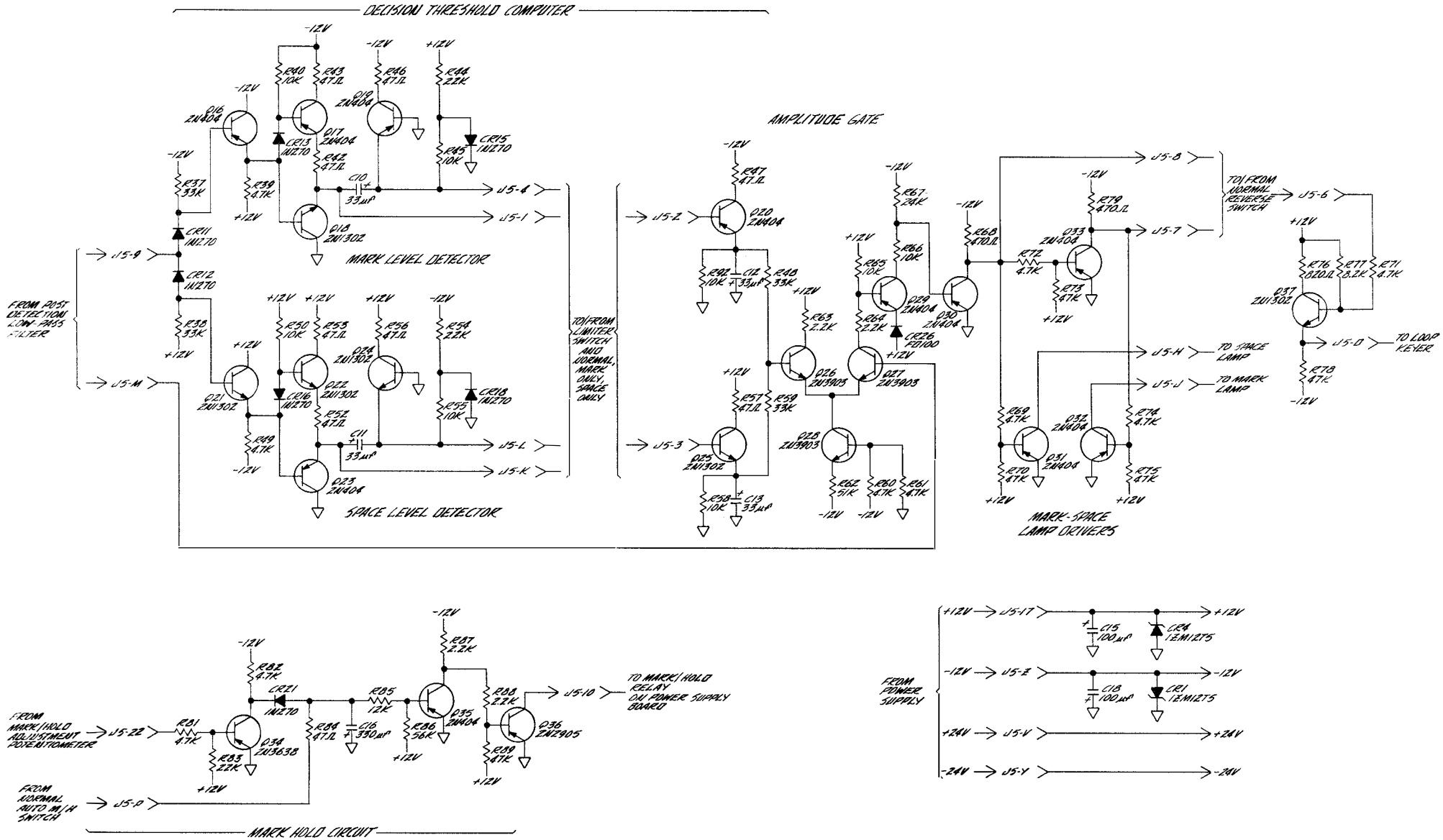


Figure 6-2. Detector Circuits Schematic Diagram
D3668A, Sheet 2

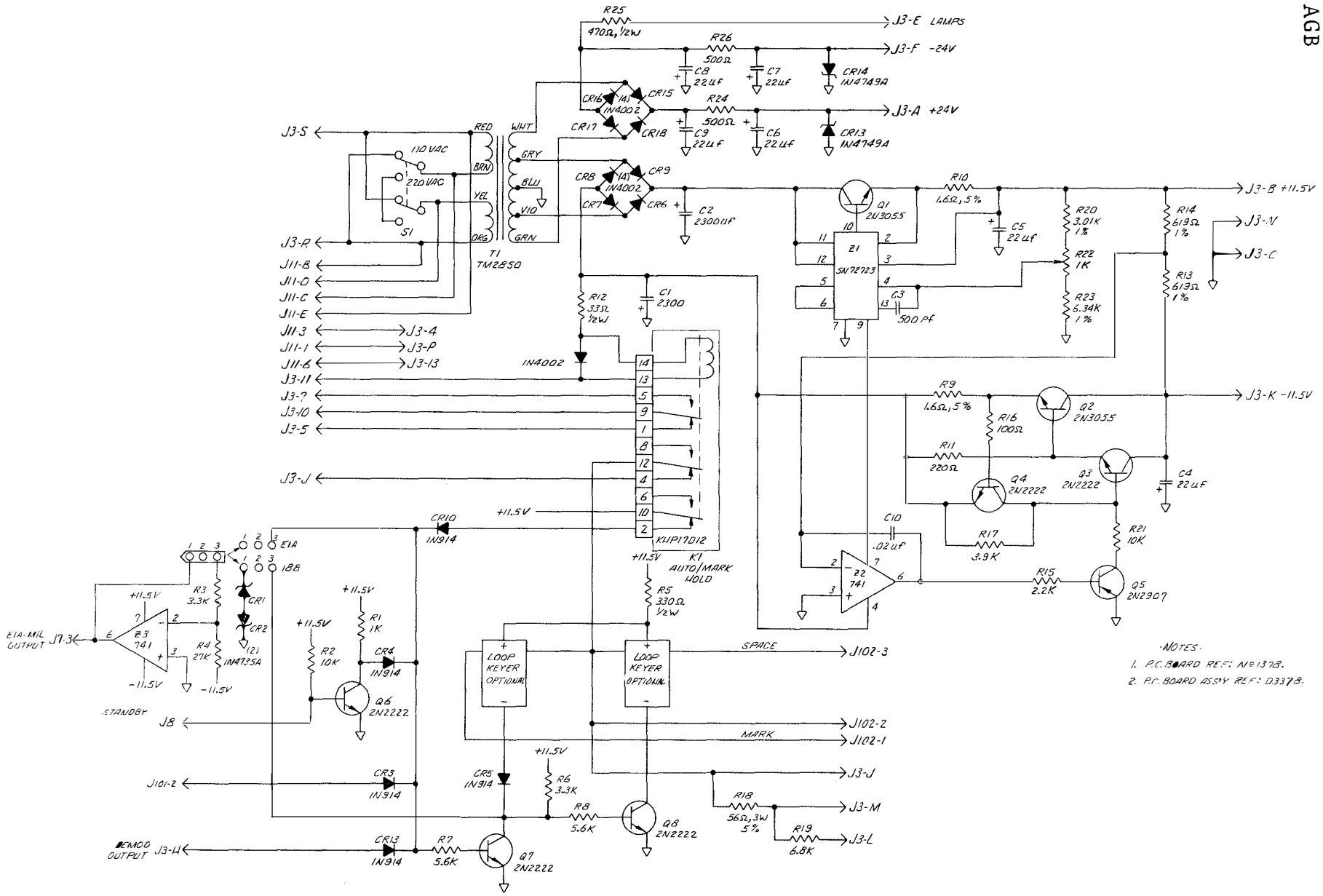


Figure 6-3. Power Supply Schematic Diagram
D3446B

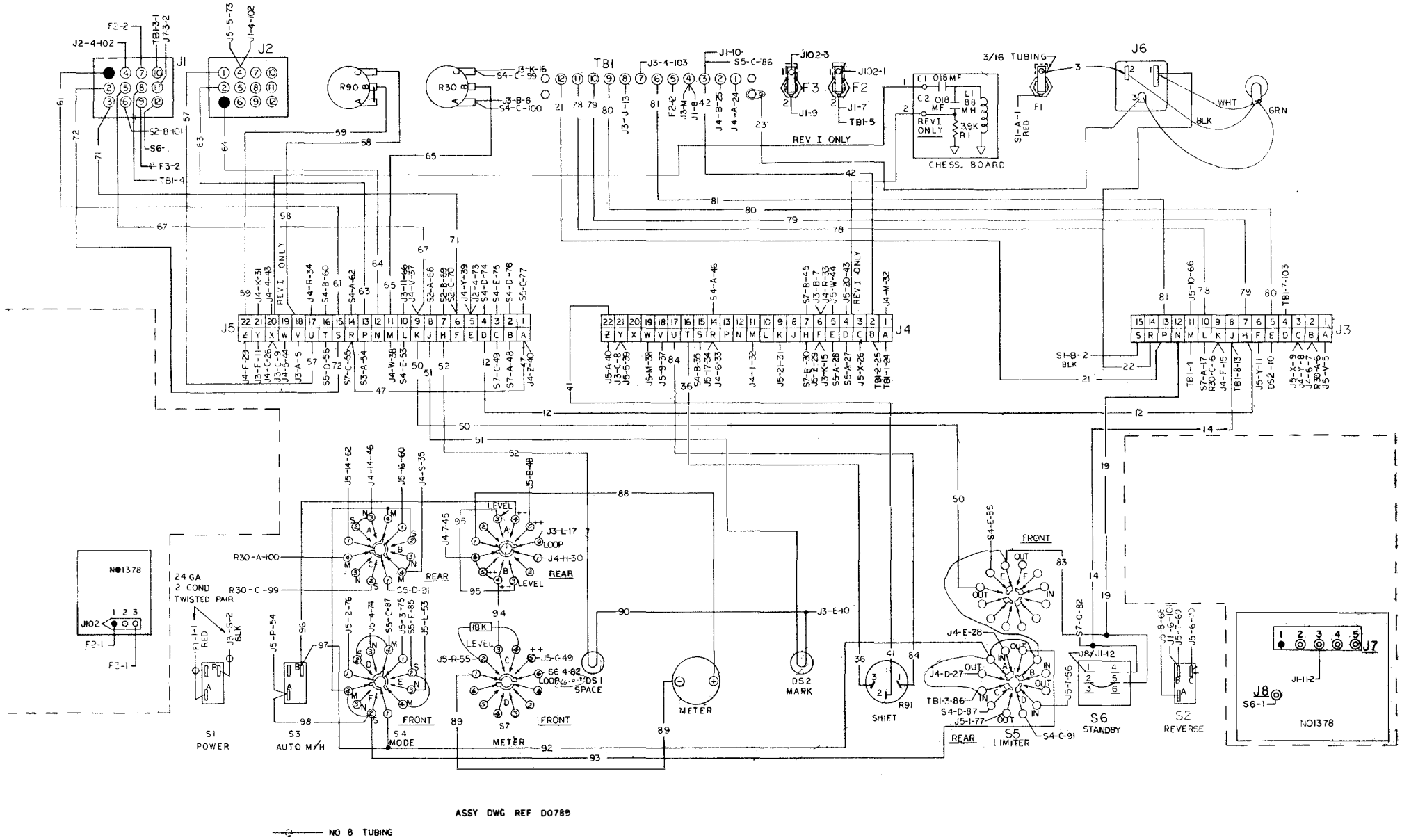


Figure 6-4. Model 1203 Wiring Diagram
D07900, Sheet 5

AGB

SECTION VII

PART REPLACEMENT DRAWINGS

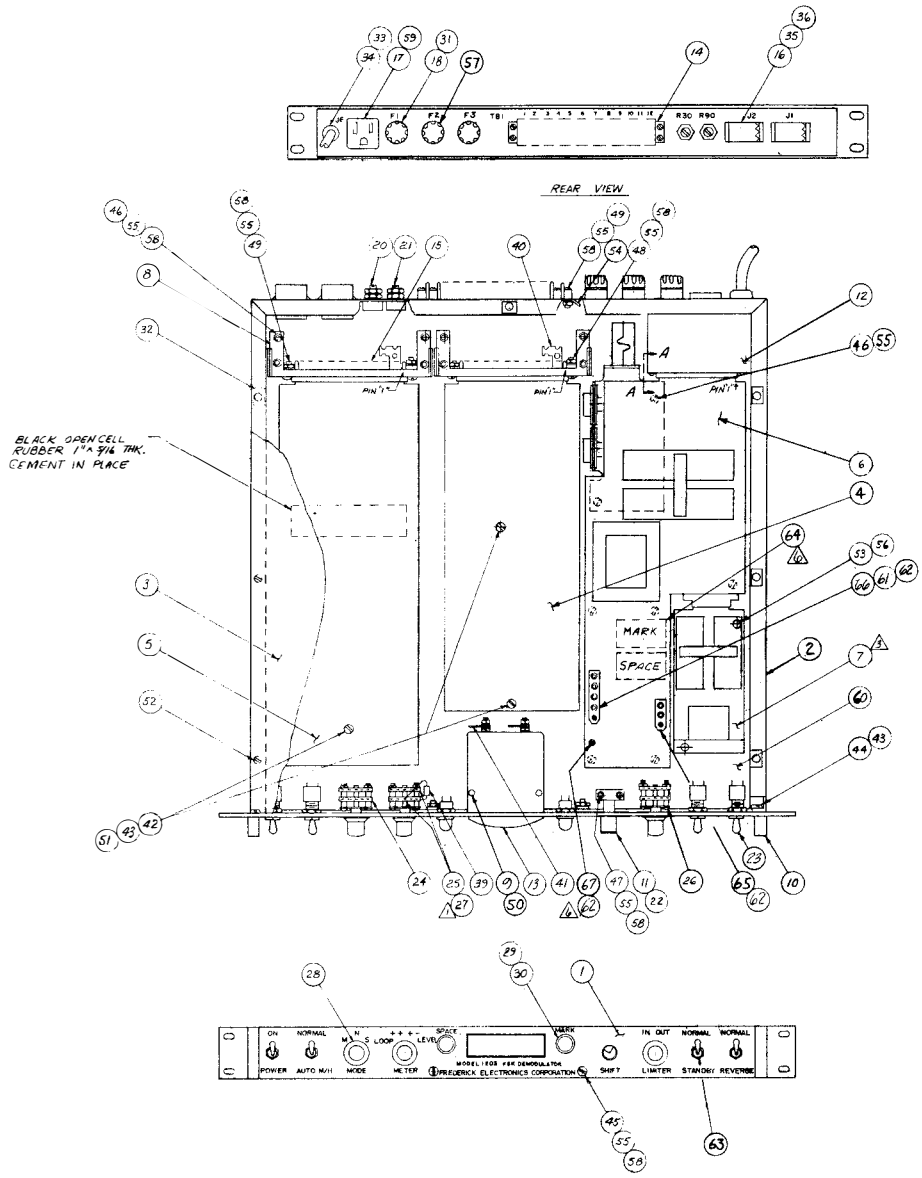
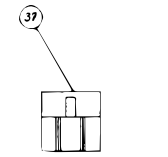
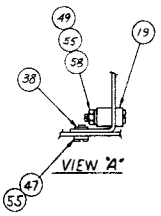


Figure 7-1. Model 1203 Assembly
D0789M, Sheet 5

AGB



2 CONNECTORS 1360P (ITEM 37) WITH 8 1380TL (ITEM 36) AND 2 1381TL (ITEM 35) TO BE SUPPLIED WITH EACH UNIT.



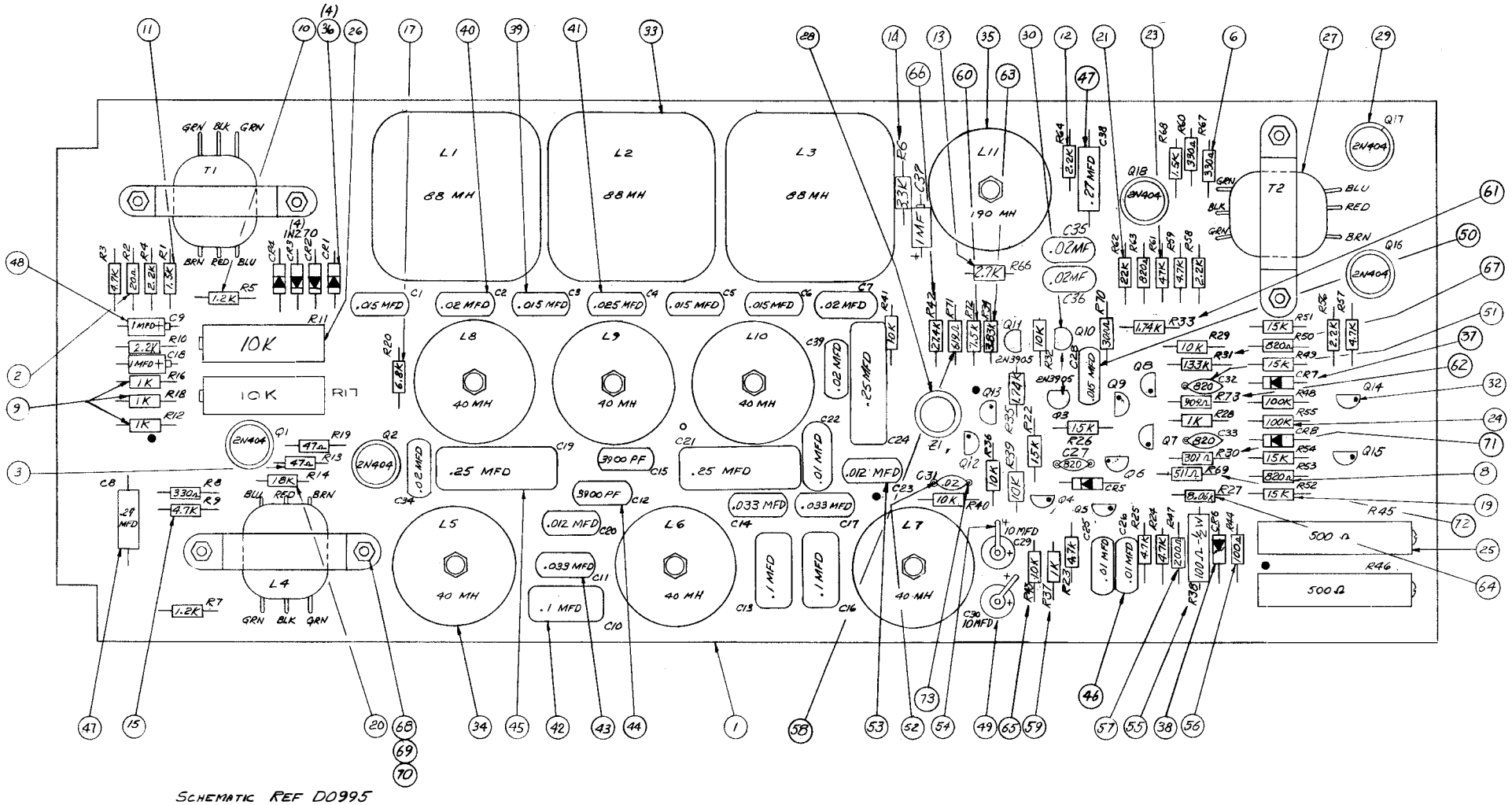
ITEM	REQ'D	PART NO	DESCRIPTION	MFR
68	2	C3240	H/L LOOP KEYER	FEC NO1452
67	1	1625-1R	CONNECTOR	MOLEX 246225
66	1	1625-3R1	CONNECTOR	MOLEX 246501
65	1	1625-3R1	CONNECTOR	MOLEX 246715
64	2	C2434	H/L LOOP KEYER	FEC NO982
63	1	8363K7	SWITCH DPDT	C-H 727275
62	4	1561-TL	TERMINAL, FEMALE	MOLEX 744410
61	2	1560-TL	TERMINAL, MALE	MOLEX 744400

NOTES

1. ASSEMBLE 1 INDEX & SHAFT ASSY (PS03) & 2 WAFER SECTIONS (PS23) TO MAKE SWITCH.
2. TERMINALS 1380TL & 1381TL ARE ASSEMBLED WITH CONNECTOR AT TIME OF FINAL WIRING.
3. ITEM 7 IS OPTIONAL EQUIPMENT
4. STENCIL REAR PLATE PER C0855
5. WIRING DIAGRAM D07905 SHT. 5.
6. ITEM 64 & 68 QUANTITY IS ONE REQ'D FOR OPTIONAL NEUTRAL ASSY. & 1 ADDITIONAL FOR OPTIONAL POLAR.

ITEM	REQ'D	PART NO	DESCRIPTION	MATL OR MFR	MATL SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
60	A/R		WIRE #22 STRANDED INSUL.	MILW-76				
59	1	1416-6	SOLDER LUG	BRASS	242756			
58	22		NUT, HEX 4-40 1/4 A.F.	BRASS	403030			
57	2	312.250	FUSE 1/4A STD	LIT-FUSE	368125			
56	3		WASHER, NO.6 INT. TOOTH	BRASS	404893			
55	28		WASHER, NO.4 INT. TOOTH		404878			
54	1	1416-4	SOLDER LUG.		SMITH	242754		
53	3		SCREW, 6-32×3/8 LG. BD. HD.		404373			
52	7		6-32×5/16 LG. FL. HD.		UNDER CUT	404368	SST	
51	3		6-32×1/4 LG. BD. HD.		404361			
50	2		4-40×1" LG. PHILLIPS		SHEET METAL	404245		
49	8		4-40×5/8 LG. BH. HD.		404220			
48	2		4-40×3/8 LG. BH. HD.		404227			
47	2		4-40×5/16 LG. BD. HD.		404203			
46	15		4-40×1/4 LG. BD. HD.		404194			
45	2		4-40×3/8 LG. OVAL HD.		404213			
44	4		SCREW, 6-32×3/8 LG. FILLISTER	BRASS	404375			
43	7		WASHER, NO.6 SPLIT LOCK	PHOS. BRZ.	404895			
42	3	1246-12	STAND-OFF	C.T.C.	683182			
41	2	1410-4	SOLDER LUG	SMITH	242704			
40	2	B1124-2	CABLE TIE	FEC				
39	1		RESISTOR, 18K, 1/4W ±10%	A-B	602576			
38	2	4-40×.050	PRESS NUT	LAMSON	403325			
37	2	1360P	CONNECTOR	MOLEX	246025			
36	10	1380TL	TERMINAL (MALE)	MOLEX	744300			
35	10	1381TL	TERMINAL (FEMALE)	MOLEX	744325			
34	1	17237	LINE CORD	BELDEN	366050			
33	1	5PH4	STRAIN RELIEF	HEYCO	688025			
32	7	C8020-632-24	SPEED NUT	TINNERMAN	403180			
31	1	3AG1A	FUSE (SLO BLO)	LITTELFUSE	368250			
30	2	327	BULB	G.E.	481050			
29	2	MS25256-6	BULB HOLDER ASSY. (RED)	DIALCO	481200			
28	3	50-3-16	CONTROL KNOB	RAYTHEON	460125			
27	1	P503	INDEX & SHAFT ASSY.	CENTRALAB	723702			
26	1	PS119	SWITCH, (ROTARY)		723468			
25	2	PS23	SWITCH, WAFER SECTION		723306			
24	1	PS117	SWITCH, (ROTARY)	CENTRALAB	723450			
23	3	8282K14	SWITCH	C.H	727225			
22	1	3600S-1-502	POTENTIOMETER 5K	BOURNS	627288			
21	1	PF 3948	POTENTIOMETER 5K	CTS	627324			
20	1	PF 3947	POTENTIOMETER 10K	CTS	627444			
19	1	67054-A	CONNECTOR	AMP	241525			
18	3	342004	FUSEHOLDER	LITTELFUSE	368425			
17	1	M-1536-98	CONNECTOR	CIRCLE F	247025			
16	2	1360R	CONNECTOR	MOLEX	246050			
15	2	2-67031-7	CONNECTOR	AMP	241475			
14	1	Y-140-12	TERMINAL STRIP	CJ	100400			
13	1	B0873	METER	INTER MET.	1136 HC			
12	1	B1174	PLUG MTG. BRACKET	FEC				
11	1	B1066	BRACKET, POT.					
10	2	B1132	BAR					
9	2	B0866-1	SPACER					
8	2	C1303-4	PLUG HOLDER ASSY.					
7	1	C2324	LOOP POWER SUPPLY ASSY.		NO 829			
6	1	D3378	POWER SUPPLY ASSY.		NO1378			
5	1	D0994	DETECTOR CIRCUIT ASSY.		NO 392			
4	1	D0993	LOCAL MIXER & FILTER ASSY.		NO 364			
3	1	C0706	COVER					
2	1	C0824	CHASSIS					
1	1	C0991	FRONT PANEL ENGRAVING	FEC	C0788			

Figure 7-1. Parts List



SCHEMATIC REF D0995

Figure 7-2. Mixer, Local Oscillator, and Filter PC Board D0993J

ITEM	REQ	PART NO	DESCRIPTION	MFR	CHT. PART NO	FINISH	FINISH SPEC	CKT SYM
73	5	56064	EYELETS	U.S.				
72	1	RN60D5110F	RESISTOR, 511 Ω, 1/4 W, 1%	I.R.C.				
71	2	RN60D3010F	RESISTOR, 301 Ω, 1/4 W, 1%	I.R.C.				
70	6		NUT, HEX., No. 2-56 x 3/16 A.F.	BRASS		N.P.		
69	6		WASHER, No. 2 SPLIT LOCK	BRASS		N.P.		
68	6		SCREW, No. 2-56 x 1/4 BD. HD.	BRASS		N.P.		
67	1	RN60D1333F	RESISTOR, 133K, 1/4 W, 1%	I.R.C.				
66	1	2742F	27.4K					
65	7	1002F	10K					
64	1	8061F	8.06K					
63	1	3831F	3.83K					
62	1	9090F	909 Ω					
61	2	1741F	1.74K					
60	1	RN60D1501F	RESISTOR, 1.5K, 1/4 W, 1%	I.R.C.				
59	2	RN60D1102F	RESISTOR, 1K, 1/4 W, 1%	I.R.C.				
58	1	6190F	619 Ω					
57	1	2000F	200 Ω					
56	1	RN60D1000F	100 Ω, 1/4 W, 1%					
55	1	RN65D1000F	RESISTOR, 100 Ω, 1/2 W, 1%	I.R.C.				
54	AR		TEFLON TUBING, INSULATION					
53	2	1MD-1-123J	CAPACITOR, .012 MFD, 100V	ARCO ELM				
52	1	5835Y5U203Z	.02 MFD 25V	ERIE				
51	3	831Z5F821K	820 PF 500V	ERIE				
50	1	DM-30-153J	15,000 PF, 500V	ARCO ELM				
49	2	150D-106X7035R2	10 MF 35VDC	SPRAGUE				
48	3	150D-105X7035A2	1 MF 35VDC	SPRAGUE				
47	2	MF575	.27 MFD, 100V ±10%	PACITRON				
46	3	1DP1-103J	.01 MFD 100V	ARCO ELMENCO				
45	3	1DP3-254J	.25 MFD 100V					
44	2	6MPD1-392J	3900 PF 600V					
43	3	1DP1-333J	.033 MFD 100V					
42	3	1DP2-104J	.1 MFD 100V					
41	1	1DP1-253J	.025 MFD 100V					
40	6	1DP1-203J	.02 MFD 100V					
39	4	1DP1-153J	CAPACITOR .015 MFD 100V	ARCO ELMENCO				
38	1	1N4736A	ZENER DIODE	MOT.				
37	3	FD100	DIODE	FAIRCHILD				
36	4	1N270	DIODE	G.I.				
35	1	B1013-2	INDUCTOR 190 MH	FEC				
34	6	B1013-1	INDUCTOR 40 MH	FEC				
33	3	B0974	INDUCTOR 88 MH	FEC				
32	10	2N3903	TRANSISTOR	MOT				
31	"	"	"	GE				
30	3	2N3905		MOT.				
29	5	2N404	TRANSISTOR	GE				

ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
28	1	4JD12A8	INTEGRATED CIRCUIT DIFF. AMP	GE				
27	3	TR-263	TRANSFORMER	THOR				
26	2	3067P-1-103	POTENTIOMETER 10K	BOURNS				
25	2	RP501U	POTENTIOMETER 500 Ω	A.B.	TYPE 'P'			
24	2	RC07GF104K	RESISTOR 100K 1/4W ± 10%	A-B				
23	1	473	47K					
22								
21	1	223	22K					
20	1	183	18K					
19	6	153	15K					
18								
17	1	682	6.8K					
16								
15	7	472	4.7K					
14	1	332	3.3K					
13	1	272	2.7K					
12	5	222	2.2K					
11	2	152	1.5K					
10	2	122	1.2K					
9	3	102	1K					
8	3	821	820 Ω					
7								
6	3	331	330 Ω					
5								
4								
3	2	470	47Ω					
2	1	RC07GF200K	RESISTOR 20Ω 1/4 W ± 10%	A-B				
1	1	NO364-E	P.C. BOARD	FEC				

Figure 7-2. Parts List

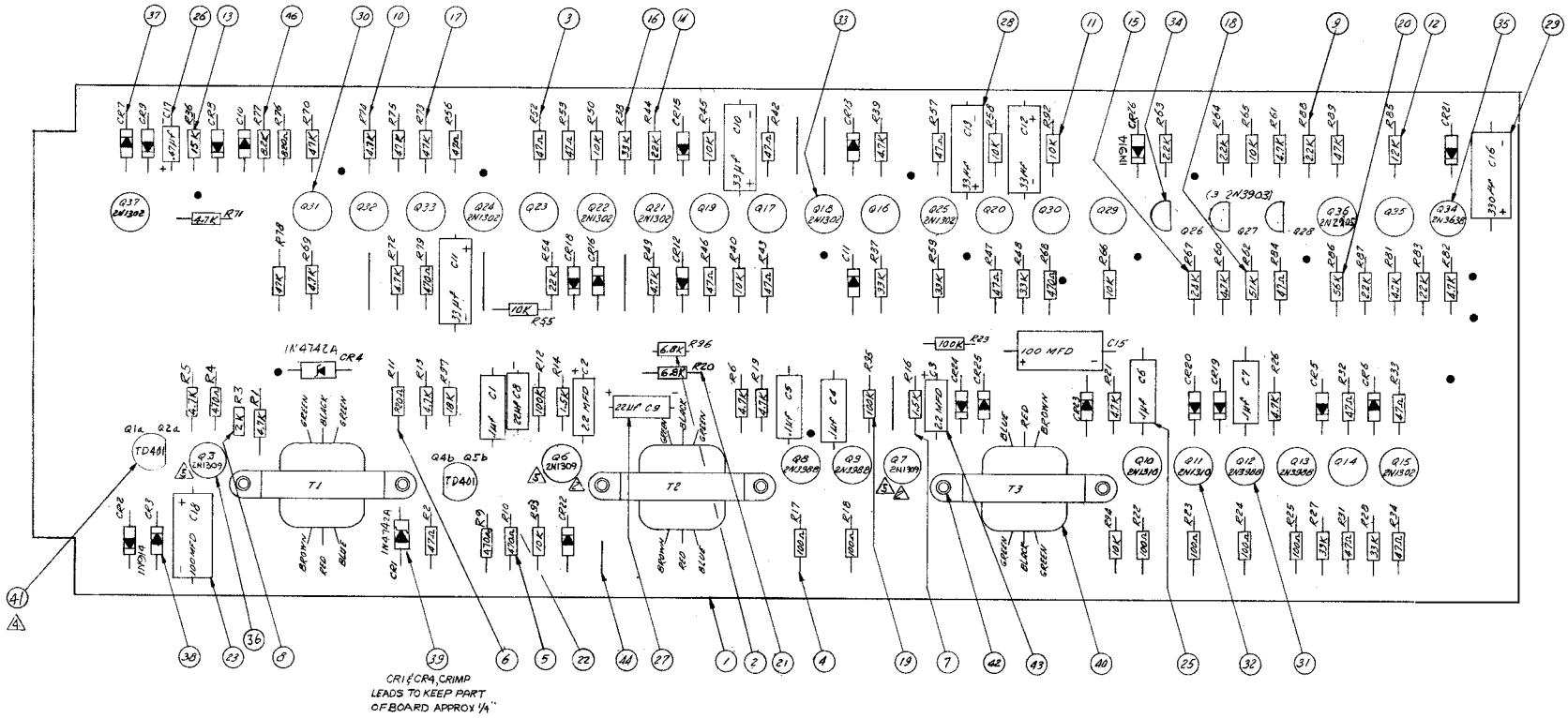
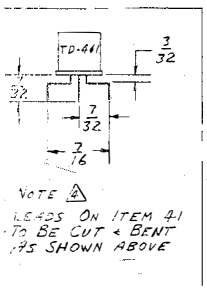


Figure 7-3. Detector Circuits PC Board
D0994L

(5) THE FOLLOWING TRANSISTORS (2N404) ARE TO BE H'FE TESTED ON FEC MODEL 1100 TESTER BEFORE ASS'Y ON BD.:

MIN. GAIN FOR Q6 & Q7 SHOULD BE 140. THE TRANSISTORS THAT DO NOT MEET THIS MIN. REQ. ARE TO BE USED IN OTHER POSITIONS ON THE SAME BOARD



NOTE (4)
LEADS ON ITEM 41 TO BE CUT & BENT AS SHOWN ABOVE

NOTE:
1. SCHEMATIC REF. D366B.
(2) THESE MUST BE GENERAL ELECTRIC 2N1309's ONLY.
(5) Q3, Q6 & Q7 MAY BE 2N404 OR 2N1309

ITEM	REQ'D	PART NO.	DESCRIPTION	MFR.	MFR P/N	FINISH	PARTS SPEC	CKT SYM
46	1		RESISTOR, 3.2K, ¼W, 10%	ALLEN B.	602528			
45	1	2N2905	TRANSISTOR	MOT	080520			
44	A/R		WIRE #22					
43	2	150D225X9020A2	CAPACITOR, 2.2MF, 20 V	SPRAGUE	028308			
42	6	4919	EYELET	STIMPSON				
41	2	TD401	DUAL TRANSISTOR	SPRAGUE	080129			
40	3	TY55X	TRANSFORMER	U.T.C.	765260			
39	2	IN4742A	DIODE	MOT	040792			
38	3	IN914	DIODE	GE	040238			
37	18	80402	DIODE	G.I.	IN270	040044		
36	3	2N1309	TRANSISTOR	G.E.	080395			
35	1	2N3638	TRANSISTOR	FAIRCHILD	080594			
34	3	2N3903		MOT.	080682			
33	7	80507		FCA	2N1302	080374		
32	2	2N1310		FCA	080396			
31	4	2N338B		FCA	080110			
30	12	2N404	TRANSISTOR	G.E.	~~080132~~			
29	1	150D SERIES	CAPACITOR 330 MF 6V	SPRAGUE	028880			
28	4		33 MF 20V		028660			
27	2		22 MF 15 V		028594			
26	1	150D SERIES	.47 MF 35 V		028132			
25	5	150D SERIES	.1 MF 200 V.	SPRAGUE	025176			
24								
23	2	CS13AE101K	CAPACITOR 100 MFD, 20V	ASTRON	028814			
22	1		RESISTOR, 18K, ¼W, 10%	ALLEN B	602576			
21	1		RESISTOR 6.8K, ¼W, 5%	ALLEN B.	601480			
20	1		RESISTOR 56 K, ¼W, 10%	ALLEN B.	602648			
19	3		RESISTOR 100K, ¼W, 10%	ALLEN B.	602684			
18	1		RESISTOR 51K, ¼W, 10%	ALLEN B.	601736			
17	5		47K		602636			
16	6		33K		602612			
15	1		24K		601656			
14	3		22K ¼W, 10%		602588			
13	1		15K ¼W, 5%		601592			
12	1		12K ¼W, 10%		602552			
11	10		10K		602540			
10	17		4.7K		602492			
9	4		2.2K		602420			
8	1		2K		602415			
7	2		1.5K		602396			
6	2		820Ω		602360			
5	5		470Ω		602324			
4	6		100Ω		602228			
3	14		RESISTOR 47Ω, ¼W, 10%	ALLEN B	602180			
2	1		RESISTOR, 6.8K, ½W, 10%	ALLEN B	602516			
1	1	N0392B	P.C. BOARD	F.E.C.				
ITEM	REQ'D	PART NO.	DESCRIPTION	MATL OR MFR	MATL SPEC OR CAT. PART NO.	FINISH	FINISH SPEC.	CKT SYM

Figure 7-3. Parts List

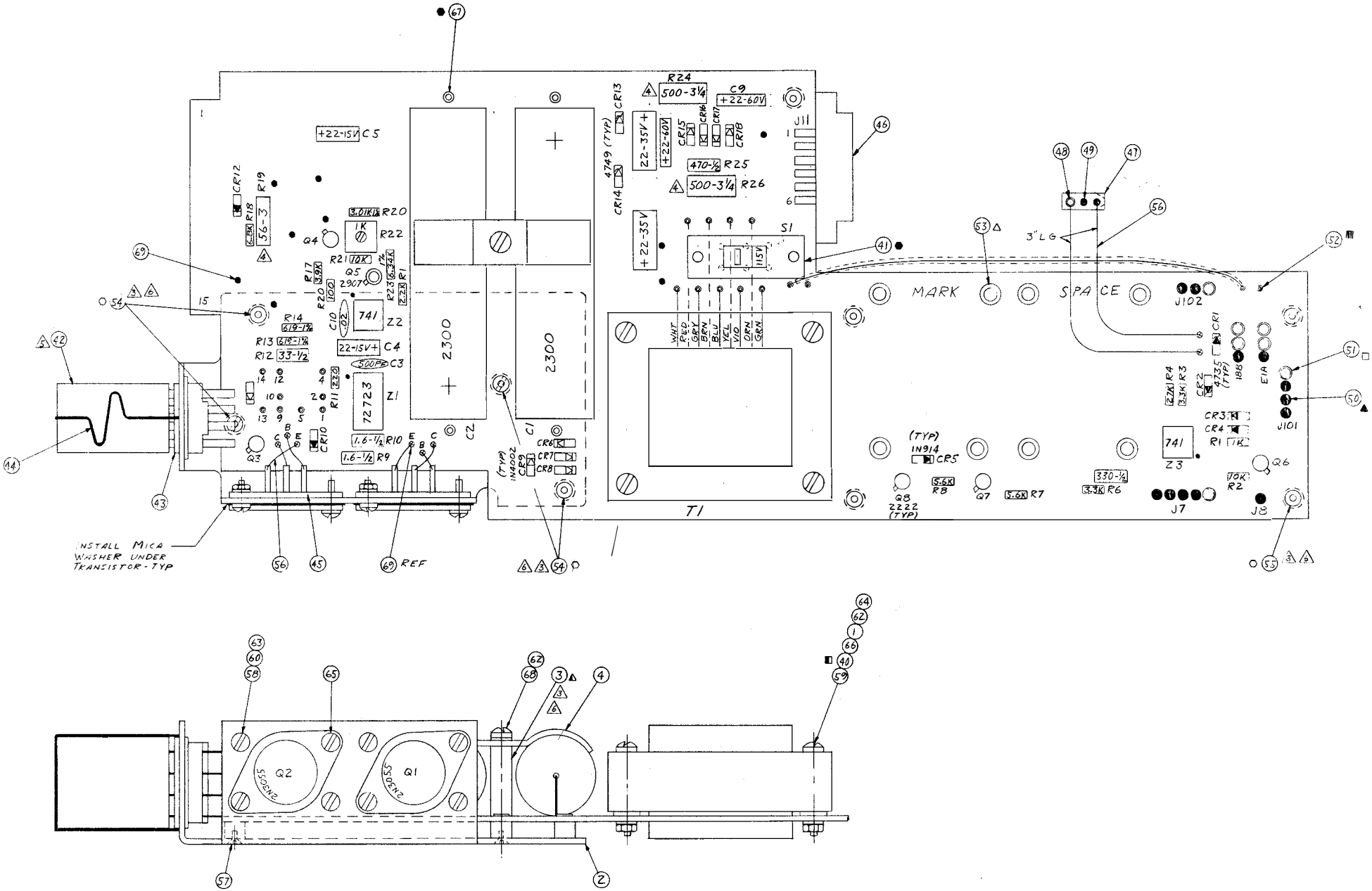


Figure 7-4. Power Supply PC Board
D3378C

AGB

NOTES:

1. SCHEMATIC REF 03446
2. UNLESS OTHERWISE NOTED DRILL ALL HOLES NO.55 (.052) DR. & INSTALL 46410 GRIPLETS
   INT CIR'S REQUIRE NO. 68 (.031) DR.
   - ■ NO.55 (.052) DR. - AS REQUIRED FOR ITEM 52
   - ▲ NO.52 (.063) DR. - 12 PLACES FOR ITEM 50
   - ❻ NO.49 (.073) DR. - 4 PLACES FOR ITEM 67; 6 PLACES FOR ITEM 41
   - ▢ NO.43 (.089) DR. - 7 PLACES FOR ITEM 51
   - △ NO.30 (.128) DR. - 8 PLACES FOR ITEM 53
   - ◯ NO.28 (.140) DR. - 4 PLACES FOR ITEM 54; 5 PLACES FOR ITEM 55
   - ◧ 5/32 (.156) DR. - 4 PLACES FOR ITEM 40
   - ◭ NO.11 (.191) DR. - 1 PLACE FOR ITEM 3
3. MOUNT ITEMS 54 & 55 ON TRACK SIDE AND ITEM 3 ON COMPONENT SIDE OF PC BOARD
4. RAISE ITEMS 22 & 23 1/8" OFF BOARD PRIOR TO SOLDERING
5. WIRE RELAY TERMINALS TO CORRESPONDING EYELET NO. ON PC BOARD
6. DO NOT SOLDER STANDOFFS

ITEM	REQ'D	PART NO.	DESCRIPTION	MFR	CAT NO.
70	A/R		WIRE 24 GA SOLID	ALPHA	
69	A/R	46410	GRIPLET	BERG	
68	1		SCREW NO.6-32x3/8 BH	SST	404373
67	4	2059	EYELET	STIMPSON	
66	4	2162	WASHER FIBER NO.6	SMITH	404970
65	4		SCREW NO.6-32x3/8 BH SELF	TAP SST	404791
64	4		NUT 6-32x1/4 AF	SST	403035
63	8		NUT 4-40x1/4 AF	SST	403030
62	5		WASHER NO.6 SPLIT LOCK	SST	404895
61					

ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO	FINISH	FINISH SPEC	CAT SYM
60	4		WASHER NO.4 SPLIT LOCK	SST	404880			
59	4		SCREW NO.6-32x1 BH	SST	404415			
58	4		SCREW NO.4-40x5/16 BH	SST	404203			
57	2		SCREW NO.4-40x1/4 FH	SST	404192			
56	A/R		WIRE 24 GA STRANDED	ALPHA				
55	5	1300-11	STANDOFF	CTC	683476			
54	4	1300-10	STANDOFF	CTC	683462			
53	8	A919	EYELET	STIMPSON				
52	A/R	S-6064	EYELET	US				
51	7	M93-102ET	STAKE PIN FEMALE	B.CHAIN	744555			
50	12	R62-3ET	STAKE PIN MALE	B.CHAIN	744550			
49	2	1560TL8	TERMINAL MALE	MOLEX	744400			
48	1	1561TL8	TERMINAL FEMALE	MOLEX	744410			
47	1	1625-3R1	CONNECTOR	MOLEX	246275			
46	1	251-06-30-160	CONNECTOR	CJ	241625			
45	2	2TS-1	SOCKET TRANSISTOR	CJ	248275			
44	1	9KH3	SPRING RELAY	P&B	570300			
43	1	9KH1	SOCKET RELAY	P&B	248200			
42	1	KHP17D11	RELAY 12V	P&B	570005			
41	1	4620CLFR5-6	PC SWITCH SLIDE	SW/CRAFT	725100			
40	1	TM-2850	TRANSFORMER	TRANS INC	766285			
39	2	1N4749A	DIODE, ZENER	MOT	040815			
38	2	1N4735A	DIODE, ZENER	MOT	040704			
37	9	1N4002	DIODE	MOT	040550			
36	5	1N914	DIODE	GE	040238			
35	2	LM741CN	INT CIR	NAT	060140			
34	1	SN72723N	INT CIR	TI	060429			
33	2	2N3055	TRANSISTOR	RCA	080550			
32	1	2N2907	TRANSISTOR	MOT	080522			
31	5	2N2222	TRANSISTOR	NAT	080467			
30	1	5835Y5U203Z	CAPACITOR .02MFD 25V	ERIE	021580			
29	2	MTP226M060P1B	22MFD 60V	MALLORY	028620			
28	1	00501	500PF 1KV	CRL	021210			
27	2	150D226X9015B2	22MFD 15V	SPRAGUE	028594			
26	2	150D226X9035R2	22MFD 35V	SPRAGUE	028616			
25	2	390238G050J4	CAPACITOR 2300MFD 50V	SPRAGUE	023590			
24	1	72PR1K	POTENTIOMETER 1K	BECKMAN	627134			
23	2	4411	RESISTOR 500Ω 3 1/4W 5%	OHMITE	622165			
22	1	242E560	56Ω 3W 5%	SPRAGUE	622112			
21	1	RC20GF331K	330Ω 1/2W 10%	AB	604400			
20	1	RC20GF471K	470Ω 1/2W 10%	AB	604450			
19	1	RC20GF330K	33Ω 1/2W 10%	AB	604150			
18	2	RC20GF1R6J	1.6Ω 1/2W 5%	AB	603010			
17	1	RN60D3011F	3.01K 1/2W 1%	CORNING	624614			
16	1	RN60D6341F	6.34K 1/2W 1%	CORNING	625080			
15	2	RN6006190F	619Ω 1/2W 1%	CORNING	624180			
14	1	RC07GF273K	27K 1/4W 10%	AB	602600			
13	2	103K	10K		602540			
12	1	682K	6.8K		602516			
11	2	562K	5.6K		602504			
10	1	392K	3.9K		602392			
9	2	332K	3.3K		602468			
8	1	222K	2.2K		602420			
7	1	102K	1K		602372			
6	1	221K	220Ω		602276			
5	1	RC07GF101K	RESISTOR 100Ω 1/4W 10%	AB	602228			
4	1	B2075-1	CLAMP	FEC				
3	1	B1193-14	STANDOFF	FEC				
2	1	C3126	HEAT SINK	FEC				
1	1	N01378	PC BOARD	FEC				

Figure 7-4. Parts List

APPENDICES

APPENDIX AA

LOOP POWER SUPPLY

AA.1 GENERAL

The Loop Power Supply module NO829A can be obtained in any one of three configurations supplying the following currents and voltages.

100 ma	±48 vdc
100 ma	±65 vdc
40 ma	±80 vdc

AA.2 INSTALLATION

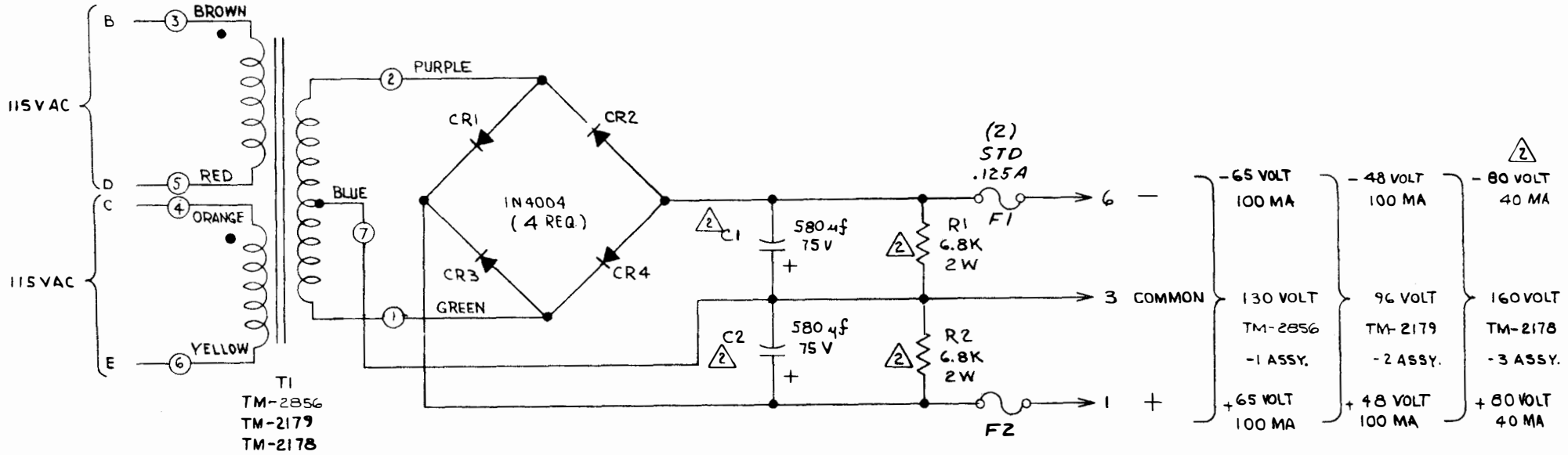
Section II of the manual explains the mounting location for the Loop Power Supply.

To install the supply, it is only necessary to plug it into the Loop Supply jack of the mother unit, and to attach the supply to the chassis as designated in Section II.

AA.3 CIRCUIT DESCRIPTION

The loop supply is schematically illustrated in Figure AA-1.

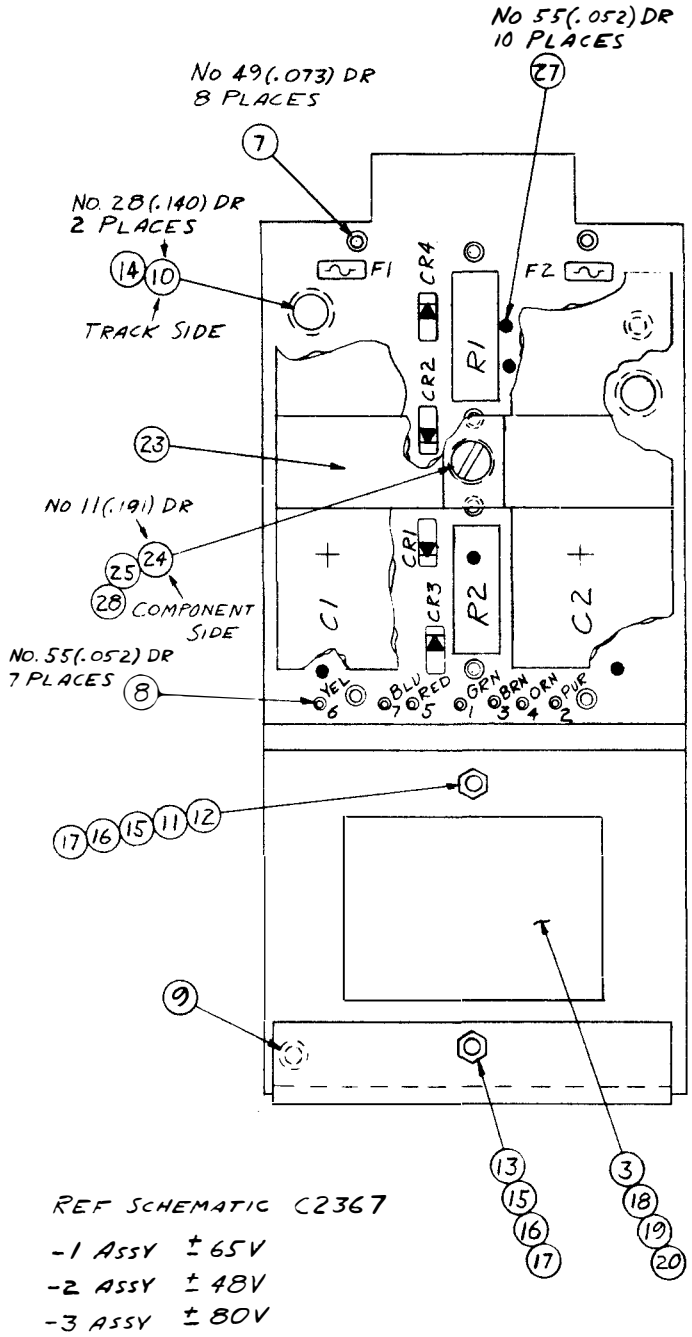
The polar loop power supply consists of T1, full-wave bridge rectifier CR1 thru CR4, negative voltage filter section C1-R1, and positive voltage filter section C2-R2. Each section furnishes the nominal voltages and current listed. T1 will operate from either a 115 or 230 vac power source, controlled by the ac POWER and selector switches of the mother unit.



NOTES:

1. REF. ASSY. C2324
2. ON - 3 ASSY. R1, R2 ARE 10K, 2W & C1, C2 ARE 300 MFD. 100 VOLT.
3. P.C. BOARD N0829

Figure AA-1. Loop Power Supply Schematic
C2367C



ITEM	REQ -3	REQ -2	REQ -1	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT PART NO
28	1	1	1		WASHER, 6 INT TOOTH	SST	
27	10	10	10	46410	GRIPLET	BERG	
26	2	2	2	275.125	FUSE PICO	LITTLEFUSE	368110
25	1	1	1		SCREW 6-32x5/16 BH	SST	
24	1	1	1	1246-15	STANDOFF	CTC	683224
23	1	1	1	B2075	HOLD DOWN CLIP	FEC	
22	2			066HL301T100B	CAPACITOR 300MFD 100V	SANGAMO	023398
21	2			RC42GF103K	RESISTOR 10K 2W ±10%	AB	608508
20	1			TM-2178	TRANSFORMER	TI	765678
19		1		TM-2179	TRANSFORMER	TI	765679
18	A/R	A/R	A/R	SST1	CABLE TIE	PANDUIT	
17	2	2	2		NUT HEX 4-40x1/4 AF	SST	
16	2	2	2		WASHER NO.4 INT TOOTH	PHOS.BRZ	
15	2	2	2		WASHER NO.4 FLAT	BRASS	NI.P.
14	2	2	2		SCREW 4-40x5/16 LG FL HD	SST	UNDERCUT
13	1	1	1		SCREW 4-40x1" BD HD	SST	
12	1	1	1		SCREW 4-40x1 3/8 LG FL HD	SST	
11	1	1	1	8706	SPACER	SMITH	683890
10	2	2	2	1300-10	STANDOFF	CTC	683462
9	2	2	2	PN46N.062	FLUSH NUT	PMP	403582
8	7	7	7	S6064	EYELET	US	
7	8	8	8	2059	EYELET	STIMPSON	
6		2	2	066HL581T075B	CAPACITOR 580MFD 75VDC	SANGAMO	023464
5	4	4	4	1N4004	DIODE	MOT	040572
4		2	2	RC42GF682K	RESISTOR 6.8K 2W 10%	AB	608585
3			1	TM2856	TRANSFORMER	TRAN.IND.	766290
2	1	1	1	C2368	CHASSIS	FEC	
1	1	1	1	NO829A	PC BOARD	FEC	

Figure AA-2. Loop Power Supply Assembly
C2324C

APPENDIX HK

HIGH LEVEL KEYER

HK.1 GENERAL

High level keyer module N0982 provides dry contacts which enable the unit to key data in standard 20/60 ma neutral or polar loops.

HK.2 INSTALLATION

Section II of the manual explains the mounting locations for the mark and space keyers. Plug a keyer into the mark mounting holes for a neutral loop. Plug a second keyer into the space mounting holes for a polar loop. The mounting holes and mating expansion pins are patterned to prevent incorrect mounting of the keyers.

CAUTION

External limiting is required to inhibit loop current from exceeding 100 ma, and external filtering across the loop is required for inductive loops.

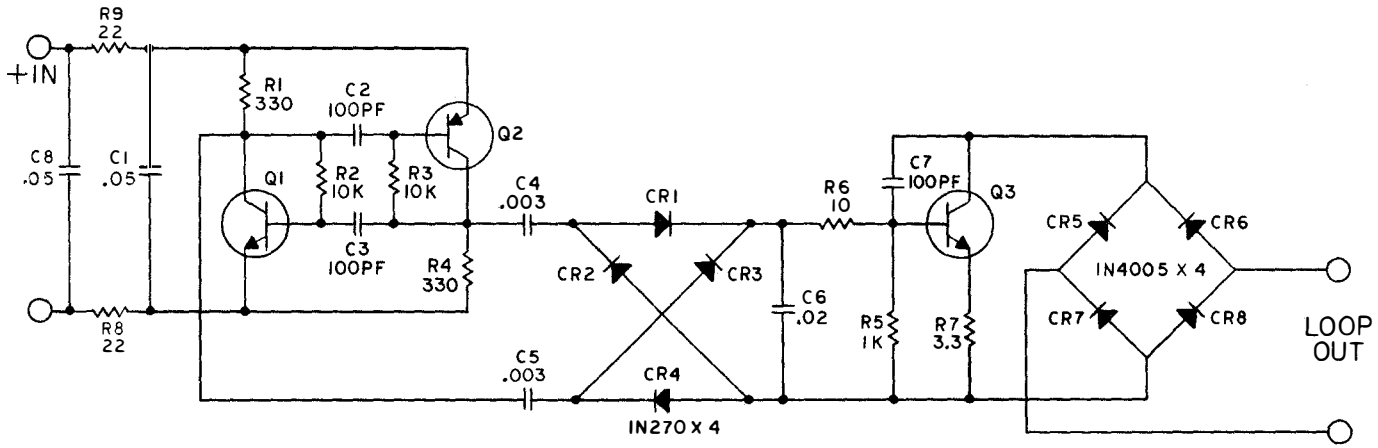
Section II in the manual specifies the connection points on the unit for high level keyer module outputs.

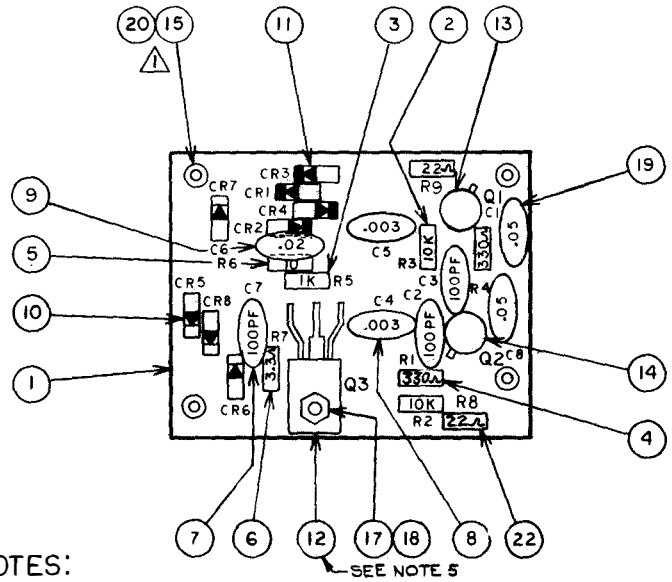
HK.3 CIRCUIT DESCRIPTION

The keyer circuit, shown in Figure HK-1, is comprised of voltage-keyed oscillator Q1-Q2, isolation capacitors C4 and C5, full-wave bridge rectifier CR1 thru CR4, filter C6-R6, transistor switch Q3, and the CR5 thru CR8 loop bridge circuit. Only the mark keyer is used in a neutral loop. The space keyer is added for use in a polar loop.

The Q1-Q2 oscillator is a complementary RC multivibrator controlled by elements C2 and C3. The oscillator can be keyed on by switching a +5 vdc to the +IN terminal with the common terminal connected to ground, or by connecting a continuous +5 vdc to the +IN terminal and switching the common terminal to ground. The oscillator free-runs at approximately 750 kHz until the input is removed. The oscillator output is coupled

by C4 and C5 to the CR1 thru CR4 bridge rectifier. Elements C6 and R6 filter the rectifier output, which turns on transistor switch Q3. Current flows thru the CR5 thru CR8 bridge circuit into the transmission loop, so the keyer module is not polarity sensitive.





NOTES:

1. UNLESS NOTED OTHERWISE, DRILL ALL HOLES WITH NO55 & INSTALL 46410 GRIPLETS
   ⚠1 DRILL NO30 (.128) & INSTALL ON COMPONENT SIDE OF BOARD
2. SOLDER STAND OFF TO TRACK SIDE OF BOARD
3. KEEP ITEM 19 CLOSE TO BOARD AS POSSIBLE
4. INSTALL ITEM 20 IN STD CONFIGURATION
5. ITEM 12 TO BE INSTALLED WITH GOLD PLATING FACE DOWN ON BOARD

ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
22	2	RC07GF220K	RES. 22Ω 1/4W 10%	AB				
20	4	192	BANANA PLUG	SMITH				
19	2	5855Y5U503Z	DISC CAP. .05UF 25V	ERIE				
18	1		4-40X3 8 BH SCREW	SST				
17	1		4-40NUT 1/4AF	SST				
16	AR	46410	GRIPLET	BERG				
15	4	2188-12	STANDOFF	CTC				
14	1	2N2907	TRANSISTOR	MOT.				
13	1	2N2222	TRANSISTOR	MOT.				
12	1	MJE340	TRANSISTOR	MOT.				
11	4	IN270	DIODE	TI				
10	4	IN4005	DIODE	MOT.				
9	1	5835Y5U203Z	DISC CAP .02 UF 25V	ERIE				
8	2	DD302	DISC CAP .003 UF 1KV	CRL				
7	3	DD101	DISC CAP 100 PF 1KV	CRL				
6	1	RC07GF3R3K	RES. 3.3Ω 1/4W 10%	AB				
5	1	100K	10Ω					
4	2	331K	330Ω					
3	1	102K	1K					
2	2	RC07GF103K	RES. 10K 1/4W 10%	AB				
1	1	NO982A	PC BOARD	FEC				

LIST OF MATERIAL

Figure HK-1. High Level Keyer
C2434A

APPENDIX OI

OPTICALLY ISOLATED

HIGH LEVEL NEUTRAL KEYER

OI.1 GENERAL

The C3240 Optically Isolated High Level Neutral Keyer interfaces TTL level output signals with high level neutral teleprinter loop circuits. The keyer provides greater than 3500 volts (peak) isolation between the logic circuitry and the external loop.

OI.2 INSTALLATION

The C3240 Keyer circuitry is contained on a 1 5/8" x 2" printed circuit board. The board is equipped with stand-off miniature banana plugs for plug-in installation into the mother unit. The banana plugs make all required electrical connections in addition to mechanically securing the Keyer to the mother unit circuit board. Non-symmetrical placement of the plugs assures correct orientation of the Keyer. Refer to the mother unit Instruction Manual, Section II, for specific installation location and requirements.

OI.3 CIRCUIT DESCRIPTION

Reference to the Schematic Diagram, Figure OI-1, shows that the circuit operation is straightforward. A logic level 1 at the input turns on the LED of Z1, which turns on the photo-transistor. The output of Z1 turns on Q1/Q2 combination and enables current to flow in the teleprinter loop.

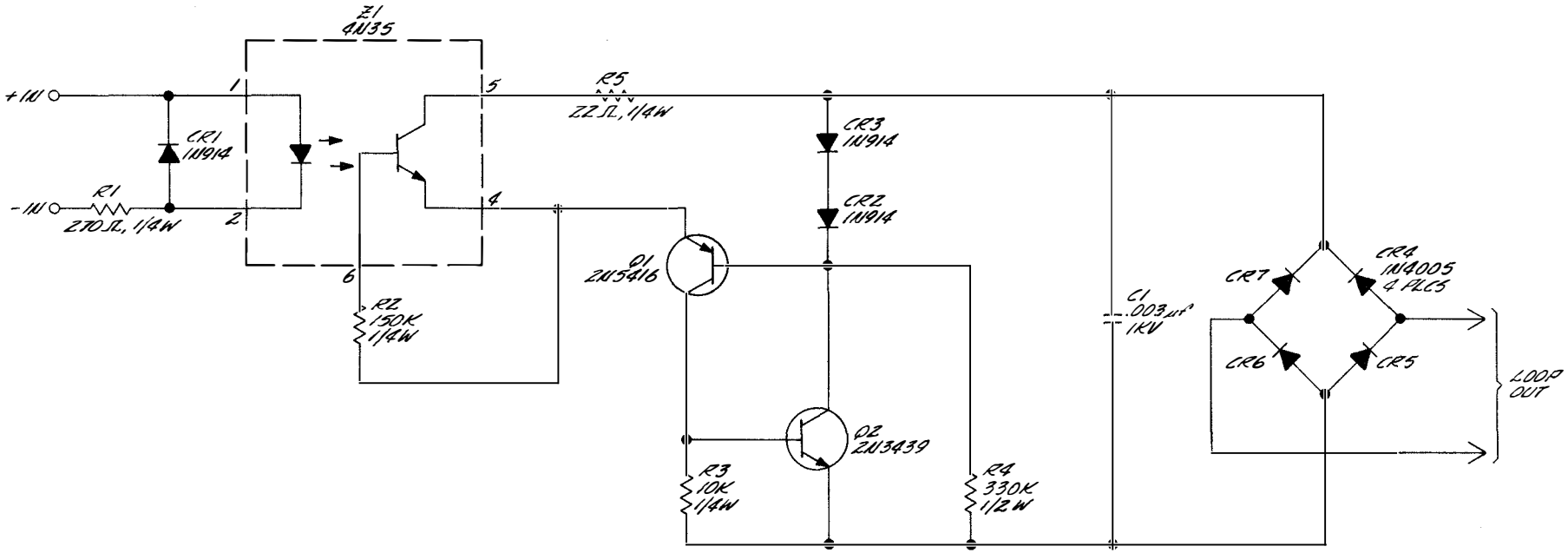
The input level required to reliably turn the keyer on is +4 volts, with a maximum limit of +8 volts. To reliably turn the keyer off requires less than 0.4 volt at the input. CR1 protects the Z1 LED from reversed polarity inputs, while R1 limits the current through Z1 LED.

Optical coupler Z1 has an input/output electrical isolation rating of greater than 3500 volts peak, and is specially mounted on the circuit board to retain this isolation rating in use.

Transistor circuit Q1/Q2 is self-reinforcing in either the on state or the off state, as commanded by Z1 output. For example, Z1 turns on, turning on Q1. Q1 turns on Q2, which

tends to turn on Q1 harder. The same logic is applicable for the off state of the circuit. Capacitor C1 limits the rise time of the voltage across Q1 and Q2, while bridge CR4 through CR7 allows use of either positive or negative neutral teleprinter loops.

External loop voltage may be up to 300 volts. Arc suppression and loop current limiting (100 ma max) must be provided externally.



NOTES:
1. PC BOARD REF 1101452
2. PC BOARD ASSY C3240

Figure OI-1. Optically Isolated High Level Neutral Keyer Schematic Diagram C3308

NOTES:

1. SCH. REF. C3308.
2. UNLESS OTHERWISE SPECIFIED DRILL ALL HOLES NO55 (.052) DR. & INSTALL 46410 GRIPLETS.
   - ■NO.60 (.040) DR. 6 PLACES & INSTALL TRANSISTORS.
   - ●NO.68 (.031) DR.- 6 PLACES & INSTALL I.C.
   - ▲NO.30 (.128) DR. 4 PLACES & INSTALL STANDOFFS.
3. INSTALL STANDOFFS ON COMPONENT SIDE & SOLDER ON TRACK SIDE.
4. JOG I.C. LEADS.
5. AFTER PRODUCTION TESTING, SPRAY ENTIRE P.C. BOARD WITH HUMISEAL TYPE 1B-15. DO NOT SPRAY BANANA PLUGS.

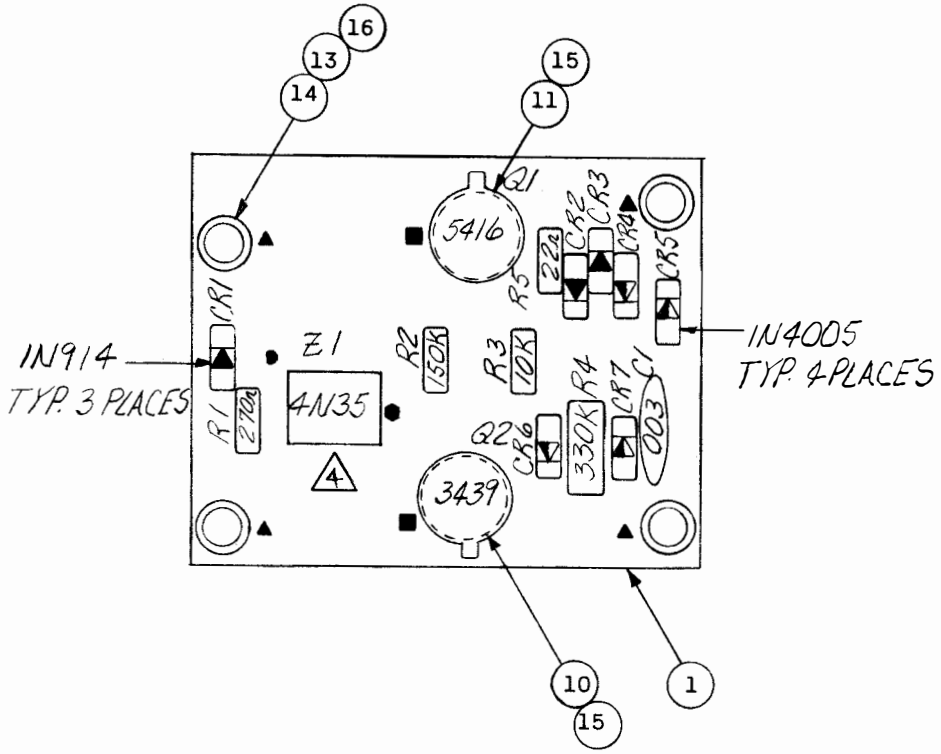


Figure OI-2. Optically Isolated High Level Neutral Keyer Assembly C3240B

CNN

16	4		WASHER NO.2 SPLIT LOCK	SST	404861			
15	2	A10020	INSULATOR	ROSS	080836			
14	4	2188-12	STANDOFF	CAMBION	683840			
13	4	192	BANANA PLUG	SMITH	246321			
12	1	4N35	INTEGRATED CIRCUIT	GE	060448			
11	1	2N5416	TRANSISTOR	MOT	080889			
10	1	2N3439	TRANSISTOR	MOT	080566			
9	4	1N4005	DIODE	GE	040594			
8	3	1N914	DIODE	MOT	040238			
7	1	DD-302	CAPACITOR .003 MFD 1KV	CRL	021390			
6	1	RC20GF334K	RESISTOR 330K 1/2W 10%	AB	604890			
5	1	RC07GF154K	RESISTOR 150K 1/4W 10%	AB	602708			
4	1	RC07GF103K	RESISTOR 10K 1/4W 10%	AB	602540			
3	1	RC07GF271K	RESISTOR 270Ω 1/4W 10%	AB	602288			
2	1	RC07GF220K	RESISTOR 22Ω 1/4W 10%	AB	602132			
1	1	N01452	P.C. BOARD	FEC				
ITEM	REQ'D	PART NO	DESCRIPTION	MAT'L OR MFR	MAT'L SPEC OR CAT PART NO.	FINISH	FINISH SPEC	CKT SYM

Figure OI-2. Parts List