4.3 CONTROL ASSEMBLY A2

The Control Board (Assembly A2) is a microprocessor based sub-assembly that contains all Modem Board (Assembly A3) filter frequency synthesizers, the AFSK transmit tone synthesizer, control bit latches, and the front panel interface circuits. In addition, the Transmit Data (TXD) and Receive data (RXD) polarity, regeneration, and receive clock recovery circuits are included on this board.

The following sections contain detailed descriptions of the Control Board circuit illustrated in Figures A1806 to A1827. Please refer to the block diagram in Figure 4.11 and the schematic diagrams during this discussion.

4.3.1 Microprocessor Controller

The ST-8000A Control Board (Assembly A2) uses a conventional dedicated microprocessor architecture with 32K bytes of read only (EPROM) memory for firmware storage, 2K bytes of read/write (RAM) memory, and 2K bytes of electrically alterable (EEPROM) memory. The Z80A microprocessor uses a 4.9152 MHz clock (PCLK) generated by a TTL crystal oscillator. The 330 ohm pullup resistor on U15-6 ensures that the clock signal meets the minimum high voltage level requirements of the Z80A. The Control Board uses both memory mapped and I/O port mapped peripheral devices and latches. The Z80A operates with no wait states.

Note the 10K ohm pullup resistors on the microprocessor write, WRM_L (U15-22), and read, RDM_L (U15-21), control signals. These resistors hold these control lines high when the processor is in the power on reset condition since these control lines are in a high impedance tri-state condition at that time. Without the pullup resistors, a false memory write signal might corrupt the parameters stored in the non-volatile parameter storage memory (U2).

The Z80A has two maskable interrupt sources: the serial channel controller interrupt, INT_L (U56-12), and the front panel keypad interrupt, KBINT (U64-1). These two interrupt sources are combined by a 2 input NAND gate (U56) to produce a common interrupt signal to drive the microprocessor interrupt input (U15-16). The front panel interrupt signal, KBINT, must be inverted since it is an active high signal. When an interrupt occurs, the microprocessor must poll both the serial controller (U66) shown in Figure A1815 and the front panel controller to see which device requested the interrupt.

The non-maskable interrupt, NMI (U15-17), provides a real time clock reference for correctly calculating ST-8000A timing delays. This square wave timing signal is generated by the programmable timer (U1) in Figure A1807, and it is set for a 0.5 ms period.

The RESET (U9-5) and RESET_L (U9-6, U15-26) signals are generated by a "deadman" timer and power on reset circuit (U9). During normal ST-8000A operation, the deadman timer reset signal, SANITY_L (U9-7), is pulsed low periodically by the microprocessor. Should some abnormal situation cause the microprocessor to cease operation, the deadman timer will force a hardware reset of the ST-8000A. When a reset occurs, the RESET and RESET_L outputs are pulsed low and high, respectively, for approximately 0.25 seconds.

Due to the number of latches and devices on the control board, the Z80A read and write control signals are buffered by two buffer gates to generate RD_L (U10-8) and WR_L (U10-11), respectively. Note that the un-buffered signals RDM_L and WRM_L are connected directly to the EPROM (U4), the RAM (U3), and the EEPROM (U2).

4.3.2 System Clocks

A programmable timer (U1) in Figure A1807 generates the reference frequency for all of the frequency synthesizers, CKREF (U1-10), the low pass filter clock, LPCLK (U1-13), and the microprocessor real time reference clock, NMI (U1-17).

All of the ST-8000A frequency synthesizers are referenced to the same 4.9152 MHz crystal oscillator that drives the microprocessor clock, PCLK (U1-9,15). One 16 bit programmable timer divides PCLK by 6 to generate the 819,200 Hz reference clock, CKREF (U1-10), used by all filter synthesizers. In addition, the 4.9152 MHz clock is divided by various constants to generate the low pass filter clock, LPCLK (U1-13), for the modem board. An inverting buffer is provided on CKREF to increase the fan-out capability.

A separate 6.144 MHz oscillator reference is used for the NMI clock. This clock is divided by 3072 to produce a 2000 Hz square wave signal, NMI (U1-17), for the 0.5 ms real time clock. Note that the NMI signal is disabled until the NMI control signal, NMIENA (U1-16) is set high.

The block diagram in Figure 4.12 identifies the significant Control Board (Assembly A2) clock signals.

4.3.3 Memory and I/O Address Map

The microprocessor memory is divided into memory mapped and I/O port mapped sections. All memory and I/O port address decoding is illustrated in Figures A1806 and A1807.

Decoding for the firmware memory (U4) is illustrated in Figure A1806. Memory address bit 15, A15 (U15-5), and memory request, MREQ_L (U15-19) are combined by a two input OR gate (U10) to generate the EPROM chip select signal (U4-20) when both signals are low.

Except for the firmware memory chip select, all memory and I/O address decoding is contained in Figure A1807. A 3-to-8 line decoder (U11) is the primary memory mapped device decoder, and it is enabled by the combination of address bit 15, A15 (U11-6), high and memory request, MREQ_L (U11-5), low. A second address decoder (U12) provides additional decoding for several write only latches when it is enabled by write, WR_L (U12-4), low and one memory address select line (U11-13) low.

The I/O port mapped devices are decoded by two 3-to-8 line decoders (U13, U14). The devices on the first decoder (U13) are both I/O input and output peripheral devices while those on the second decoder (U14) are I/O output only latched registers.
The memory and I/O address map for the ST-8000A control board is summarized below (all addresses are shown in HEX format):

MEMORY MAPPED ADDRESSES

ADDRESS	DESCRIPTION	R/W

0000H - 7FFFH	U4-20	27256 EPROM for firmware storage	READ
8000H - 87FFH	U3-18	2K x 8 RAM for temporary storage	READ/WRITE
8800H - 8FFFH	U2-18	2K x 8 EEPROM for parameter storage	READ/WRITE
A000H - A007H	U12-5	Synthesizer latches	WRITE
A000H	U41-11	MARK transmit tone, low byte	WRITE
A001H	U43-11	MARK transmit tone, high byte	WRITE
A002H	U40-11	SPACE transmit tone, low byte	WRITE
A003H	U42-11	SPACE transmit tone, high byte	WRITE
A004H	U45-11	MARK filter synthesizer, low byte	WRITE
A005H	U46-11	MARK filter synthesizer, high byte	WRITE
A006H	U49-11	SPACE filter synthesizer, low byte	WRITE
A007H	U50-11	SPACE filter synthesizer, high byte	WRITE
E000H	U5-1,19	Transmit delay switch SW1	READ
E800H	U6-1,19	Transmit delay switch SW2	READ

I/O PORT MAPPED ADDRESSES

PORT	DESCRIPTION		I/O
00H	U66-33	Serial controller	INPUT/OUTPUT
08H			
10H	J8-12	Front Panel select (FP_L)	INPUT/OUTPUT
18H	U1-21	Programmable timer	INPUT/OUTPUT
20H	U8-1,19	Unit Address switch SW4	INPUT
28H	U7-1,19	Remote Port rate switch SW3	INPUT
30H	U44-1,19	AMHO, level, RS232/MIL, KBINT, TXD	INPUT
38H - 3FH	U14-5	Misc. control latches	OUTPUT
38H	U47-11	MARK and SPACE filter Q latch	OUTPUT
39H	U48-11	NMI, Regen, RX/TX control latch	OUTPUT
3AH	U51-11	AMHC, Det. Mode, Channel, Mute, BIT	OUTPUT
3BH	U9-7	Sanity timer	OUTPUT
3CH	J8-13	Front panel LED latch 0 (LED0_L)	OUTPUT
3DH	J8-14	Front panel LED latch 1 (LED1_L)	OUTPUT
3EH	U52-11	High speed RX synthesizer, low byte	OUTPUT
3FH	U53-11	High speed RX synthesizer, high byte	OUTPUT

4.3.4 EPROM, EEPROM, and RAM Memory

The ST-8000A memory address map is summarized below:

MEMORY ADDRESSES

ADDRESS	DESCRIPTION		R/W
0000H - 7FFFH	U4-20	27256 EPROM for firmware storage	READ 8000H -
87FFH	U3-18	2K x 8 RAM for temporary storage	READ/WRITE
8800H - 8FFFH	U2-18	2K x 8 EEPROM for parameter storage	READ/WRITE

Figure A1806 illustrates the firmware EPROM (U4), the non-volatile parameter EEPROM (U2), and the 2k x 8 RAM memory (U3). The ST-8000A firmware is loaded in an industry standard 32k x 8 byte EPROM with 250 ns access time. In this unit, address bit 15, A15 (U15-5) selects either the EPROM when A15 is low or the EEPROM and RAM when A15 is high. Note that the memory request signal, MREQ_L (U15-19) enables memory decoding only

during memory access cycles, not during I/O port access cycles. The microprocessor read signal, RDM_L (U15-21), is connected directly to the EPROM (U4-22), RAM (U3-20), and EEPROM (U2-20) output enable inputs. The microprocessor write signal, WRM_L (U15-22), is connected to the RAM write input (U3-21) and the EEPROM write input (U2-21).

4.3.5 Memory Mapped Latches and Buffers

The ST-8000A controls the MARK and SPACE transmit tone and bandpass filter synthesizers through memory mapped latches. In addition, the transmit delay time switch setting is read from memory mapped switch buffers. These buffer addresses are summarized below:

MEMORY MAPPED LATCHES AND BUFFERS

ADDRESS	DESCRIPTION		R/W
A000H - A007H	U12-5	Synthesizer latches	WRITE
A000H	U41-11	MARK transmit tone, low byte	WRITE
A001H	U43-11	MARK transmit tone, high byte	WRITE
A002H	U40-11	SPACE transmit tone, low byte	WRITE
A003H	U42-11	SPACE transmit tone, high byte	WRITE
A004H	U45-11	MARK filter synthesizer, low byte	WRITE
A005H	U46-11	MARK filter synthesizer, high byte	WRITE
A006H	U49-11	SPACE filter synthesizer, low byte	WRITE
A007H	U50-11	SPACE filter synthesizer, high byte	WRITE
E000H	U5-1,19	Transmit delay switch SW1	READ
E800H	U6-1,19	Transmit delay switch SW2	READ

Each of the synthesizers requires a 16 bit constant to set the output square wave frequency. A detailed description of these registers is presented in a subsequent section and only the memory addresses are listed here.

Two other modem square wave signals are generated on the control board; the high speed synthesizer, HSCLK (U23-19), and the low pass filter clock, LPCLK (U64-12). The HSCLK synthesizer uses I/O mapped latches while LPCLK is a square wave signal generated by the on board programmable timer (U1).

The ST-8000A reads the transmit delay setting as a 16 bit value set by switches SW1 and SW2 in Figure A1810. For both switches, the OPEN or OFF position is read as a TTL 1 or high signal while CLOSED or ON is read as TTL 0 or low signal.

4.3.6 I/O Mapped Peripherals

The ST-8000A uses I/O input and output addresses for several peripheral devices and control bit latches. An I/O memory map is shown below:

I/O PORT MAPPED ADDRESSES

PORT	DESCRIPTION		I/O
00H	U66-33	Serial controller - Regen control	INPUT/OUTPUT
01H	U66-33	Serial controller - Regen data	INPUT/OUTPUT
02H	U66-33	Serial controller - Remote control	INPUT/OUTPUT
03H	U66-33	Serial controller - Remote data	INPUT/OUTPUT
10H	J8-12	Front Panel controller - data	INPUT/OUTPUT
11H	J8-12	Front Panel controller - control	INPUT/OUTPUT
18H	U1-21	Programmable timer - CKREF clock	INPUT/OUTPUT
19H	U1-21	Programmable timer - LPCLK clock	INPUT/OUTPUT
1AH	U1-21	Programmable timer - NMI clock	INPUT/OUTPUT
1BH	U1-21	Programmable timer - control register	INPUT/OUTPUT
20H	U8-1,19	Unit Address switch SW4	INPUT
28H	U7-1,19	Remote Port rate switch SW3	INPUT
30H	U44-1,19	AMHO, level, RS232/MIL, KBINT, TXD	INPUT
38H	U47-11	MARK and SPACE filter Q latch	OUTPUT
39H	U48-11	NMI, Regen, RX/TX control latch	OUTPUT
3AH	U51-11	AMHC, Det. Mode, Channel, Mute, BIT	OUTPUT
3BH	U9-7	Sanity timer	OUTPUT
3CH	J8-13	Front panel LED latch 0 (LED0_L)	OUTPUT
3DH	J8-14	Front panel LED latch 1 (LED1_L)	OUTPUT
3EH	U52-11	High speed RX synthesizer, low byte	OUTPUT
3FH	U53-11	High speed RX synthesizer, high byte	OUTPUT

Figure A1815 illustrates the dual channel serial controller (U66) used for receive data regeneration and the remote control port. This serial controller contains internal baud rate generators to independently set the data rate for the remote control port and receive data regeneration. For a detailed description of the regeneration circuit and remote control circuit, see Section x.x.x.

The front panel controller is a programmable keyboard/display interface device described in a subsequent section. For this discussion, note that the interface requires two I/O addresses; one for control and the other for data.

The programmable timer, U1, in Figure A1807, contains three 16 dividers. These registers are loaded at the I/O addresses shown above to set the selected low pass filter cutoff frequency, LPCLK (U1-13), and the two fixed rate clocks: NMI_L (U1-01) and CKREF (U64-12).

The remaining I/O address assignments control various operational latched output bits. The sections below detail each of these registers.

4.3.6.1 UNIT ADDRESS and REMOTE PORT RATE

PORT	DESCRIPTION		I/O
20H	U8-1,19	Unit Address switch SW4	INPUT
28H	U7-1,19	Remote Port rate switch SW3	INPUT

The Unit Address switch, SW4 in Figure A1809, sets the ST-8000A unit address. This register is an 8 bit, read only input.

The remote port rate switch, SW3 in Figure A1809, selects the data rate for the remote control port. This registers is an 8 bit, read only input.

4.3.6.2 RECEIVE SIGNAL LEVEL and STATUS BITS

PORT	DESCRIPTION	I/O
30H	U44-1,19 AMHO, level, RS232/MIL, KBINT, TXD	INPUT

The microprocessor can read the audio level of the receive signal and the Automatic Mark Hold condition with an I/O mapped buffer shown in Figure A1808. In addition, this register contains the state of the transmit data RS232/MIL188 option jumper setting in Figure A1816, and the remote port RS232/MIL188 option jumper setting in Figure A1815.

The state of KBINT (U64-2) in Figure A1806 is also provided in this register. Since two different interrupt sources are combined in a single microprocessor interrupt signal, this register may be read to see whether the interrupt came from the front panel keyboard/display controller.

The state of the TXD input may be read in this register as well.

The bit assignments in this register are shown below:

Input: LEVEL_L

BIT	PIN		DESCRIPTION
0	U44-4	J7-23	Automatic Mark Hold (AMHO): 1 = LOS, 0 = SIGNAL
1	U44-17	J7-20	AGC Gain A (DGA)
2	U44-2	J7-21	AGC Gain B (DGB)
3	U44-6	J7-22	AGC Gain C (DGC)
4	U44-11	U64-2	Front Panel controller Interrupt (KBINT'): 0 = intr req
5	U44-15	J2SW	Transmit Data RS232/MIL188: 1 = MIL188, 0 = RS232
6	U44-8	J5SW	Remote Port RS232/MIL188: 1 = MIL188, 0 = RS232
7	U44-13	U59-3	Transmit Data input (TXD'): 1 = MARK, 0 = SPACE

4.3.6.3 MARK/SPACE BANDPASS FILTER Q

PORT	DESCRIPTION	I/O
38H	U47-11 MARK and SPACE filter Q latch	OUTPUT

The Q's of the MARK and SPACE input filters on the modem board are selected with latched control bits on the Control Board. Since each filter requires 4 bits, a single 8 bit latch is used as shown in Figure A1808.

Output: OUT0_L

PIN	DESCRIPTION	
U47-2	MARK Filter Q High/Low	to J7-15
U47-5	MARK Filter Q bit 3	to J7-14

U47-6	MARK Filter Q bit 2	to J7-13
U47-9	MARK Filter Q bit 1	to J7-12
U47-12	SPACE Filter Q High/Low	to J7-19
U47-15	SPACE Filter Q bit 3	to J7-18
U47-16	SPACE Filter Q bit 2	to J7-17
U47-19	SPACE Filter Q bit 1	to J7-16

The Q values selected with these control bits are listed in Table 4.2.

4.3.6.4 CONTROL REGISTER 1

PORT	DESCRIPTION	I/O
39H	U48-11 NMI, Regen, RX/TX control latch	OUTPUT

Several miscellaneous control signals are latched in an octal D-type latch (U48) shown in Figure A1808. This latch contains a reset input, RESET_L (U48-1), that will force all of the control signals to a low state when the power is first turned ON. This reset ensures that the NMI control signal, NMIENA (U48-2), signal is low during power on initialization.

The function of each control signal is summarized below:

Output: OUT1_L, BIT 7

PIN	DESCRIPTION	
U48-2	NMI Enable bit (NMIENA)	to U1-16

The NMI Enable bit (NMIENA) activates the NMI real time clock in Figure A1807 for the microprocessor. A high signal enables NMI (NMIENA = 1). When a reset occurs, this bit is forced low to disable NMI (NMIENA = 0).

Output: OUT1_L, BIT 6

PIN	DESCRIPTION	
U48-5	REGEN Enable (REGEN)	to U63-5, U64-5

The Regeneration Enable bit (REGEN) determines whether the data terminal RXD output in Figure A1816 is connected to the demodulated RX data from the modem or to the control board regeneration serial controller. When regeneration mode is disabled (REGEN = 0), the modem receive data signal, RXDTR (U57-2), is connected to the modem terminal receive data output, RXDFR (U63-11). When regeneration is enabled (REGEN = 1) the modem receive data, RXDTR, is connected to the regeneration serial controller receive data input, RXDB (U66-27) and the regenerated data from the transmit data output, TXDB (U66-25) is connected to the modem terminal data connector receive data output, RXDFR. For regeneration to work properly, the correct data rate and word length must be programmed into the serial controller channel B.

Output: OUT1_L, BIT 5

PIN	DESCRIPTION	
U48-6	Resync RXD (RSYNC)	to U64-11, U56-1, U65-2

The ST-8000A has the ability to resynchronize the receive data, RXDTR, signal to a recovered receive data clock. D-latch U55 in Figure A1816 samples the RXDTR signal from the modem and re-clocks this data with a stable internal data rate clock. The result of this resynchronizing operation is to reduce the jitter in the data terminal receive data output, RXDFR (U63-11). When enabled (RSYNC = 1) the receive data is resynchronized. When disabled (RSYNC = 0) receive data is passed to the data terminal without re-clocking.

Output: OUT1_L, BIT 4

PIN	DESCRIPTION	
U48-9	RXD Normal/Reverse (RXDNR)	to U57-1

The ST-8000A provides independent control over transmit and receive data polarity, as shown in Figure A1816. When set for NORMAL receive data (RXDNR = 0), RXDTR from the modem is passed through to RXDB (U57-3) without change. When enabled (RXDNR = 1) the RXDTR signal from the modem is inverted before it reaches RXDB (U57-3).

Output: OUT1_L, BIT 3

PIN	DESCRIPTION	
U48-12	TXD Normal/Reverse (TXDNR)	to U57-4

The ST-8000A provides independent control over transmit and receive data polarity, as shown in Figure A1816. When set for NORMAL transmit data (TXDNR = 0), TXDIN from the modem is passed through to TXD (U57-6) without change. When enabled (TXDNR = 1) the TXDIN signal from the modem is inverted before it reaches TXD.

Output: OUT1_L, BIT 2

PIN	DESCRIPTION	
U48-15	TXD Enable (TXENABLE)	to U56-10

The ST-8000A Built In Tests (BIT) require that the external TXD input be disabled during testing. When disabled (TXENABLE = 0) the data terminal TXDIN input is blocked at U56-8. When enabled (TXENABLE = 1) the data terminal TXDIN input is connected to the TXD (U57-6) output.

Output: OUT1_L, BIT 1

PIN	DESCRIPTION

U48-16 [not assigned]

Output: OUT1_L, BIT 0

PIN	DESCRIPTION	
U48-19	Diversity Enable (DIVC)	to J7-25

If the diversity option is installed in the ST-8000A, diversity mode is enabled when this signal is high (DIVC = 1) and disabled otherwise.

4.3.6.5 CONTROL REGISTER 2

PORT	DESCRIPTION	I/O
3AH	U51-11 AMHC, Det. Mode, Channel, Mute, BIT	OUTPUT

Several miscellaneous control signals are latched in an octal D-type latch (U51) shown in Figure A1808. All of these control signals are passed to the modem board.

The function of each control signal is summarized below:

Output: OUT2_L, BIT 7

PIN	DESCRIPTION	
U51-2	Automatic Mark Hold Enable (AMHC)	to J7-24

The Automatic Mark Hold Enable signal (AMHC) enables and disables the AMH circuit on the modem board. The automatic mark hold feature is enabled when AMHC = 1 and is disabled when AMHC = 0.

Output: OUT2_L, BIT 6

PIN	DESCRIPTION	
U51-5	High Speed Enable (HSLS)	to J7-26

The High Speed Enable selects the low or high speed demodulator on the modem card. The high speed demodulator is enabled when HSLS = 1 and is disabled when HSLS = 0.

Output: OUT2_L, BIT 5,4

PIN	DESCRIPTION	
U51-6	Detector Mode (DMA)	to J7-27
U51-9	Detector Mode (DMB)	to J7-28

The detector mode is selected with these two bits. The detector options are listed below:

B	A	Detector Mode
0	0	MARK/SPACE
0	1	MARK ONLY
1	0	SPACE ONLY
1	1	MARK/SPACE = ATC.

Output: OUT2_L, BIT 3

PIN	DESCRIPTION	
U51-12	Channel Select (CHSEL)	to J7-32

The modem board has two channels: the modulator and the demodulator. The Channel Select control signal determines whether the transmit or receive tones are displayed on the front panel bar graph displays. The demodulator is selected when CHSEL = 1, and the modulator channel is selected when CHSEL = 0.

Output: OUT2_L, BIT 2

PIN	DESCRIPTION	
U51-15	Transmit Mute (MUTE)	to J7-33

The Transmit Mute signal enables and disables the output AFSK tones. When MUTE = 0, the transmit tones are enabled and the radio keyline relay is activated or closed. When MUTE = 1, the transmit tones are disabled, and the PTT relay is not activated.

Output: OUT2_L, BIT 1

PIN	DESCRIPTION	
U51-16	Loopback Enable (BCB)	to J7-36
U51-19	Loopback Enable (BCA)	to J7-34

The Loopback enable control bits enable and disable an analog loopback that connects the AFSK output signal to the audio input. Three different loopback gain options are available:

B	A	Loopback Gain
0	0	Disabled
0	1	0 dBm
1	0	-20 dBm
1	1	-40 dBm

4.3.7 MARK/SPACE Transmit Tone Generator

The AFSK tone oscillator illustrated in Figure A1811 is a 16 bit full adder operating as a digital signal synthesizer with a square wave output set to 50 times the audio tone frequency. Two sets of latches store the constants for the MARK and SPACE tones, and the transmit data signal, TXD

(U55-12), selects either the MARK tone (TXD = 0) or SPACE tone (TXD = 1).

The D-type latch is included to synchronize the changes between MARK and SPACE to that portion of the synthesized sine wave output where the slope is 0. In this fashion, the distortion is minimized. The synchronizing signal, FSKCLK (U55-11) pulses once per sine wave cycle.

The MARK/SPACE tone digital synthesizer is a 16 bit full adder implemented with four 4 bit full adders, U24 - U27. On each rising edge of CKREF (U17-11, U16-11), a 819,000 Hz clock, the current 16 bit sum is latched into two D-type latches, (U16, U17). These latch outputs are then added to the tone constant stored in either the MARK or SPACE tone latch depending on the state of the sampled TXD signal (U55-9, U55-8). When a MARK is transmitted, the MARK constant registers (U41, U43) are enabled on the adder inputs. When a SPACE is transmitted, the SPACE constant registers (U40, U42) are enabled on the adder inputs. The selected constant is summed with the previous sum latched in U16 and U17 to form a new sum that will be latched on the next rising edge of CKREF to complete the cycle. The output of this synthesizer, TFSK (U17-19) has a nominal frequency of 50 times the selected tone frequency.

Figure 4.13 summarizes the digital frequency synthesizer operation. The digital synthesizers generate their output frequency through addition. The frequency is determined by the magnitude of the constant loaded into the input latches and the clock reference frequency driving the synthesizer. For example, if a constant 001 hex is loaded into the MARK latch, and TXD = 0, then the sum at the output of the latches U16 and U17 will be incremented by 1 count for each rising edge of CKREF. After 32,768 rising edges, the TFSK output will change from 0 to 1. Then, after another 32,768 rising edges, the TFSK signal will change from 1 to 0. The total time for one cycle is 65,536 clock cycles of CKREF. If CKREF is set to 819,200 Hz, the TFSK output will have a frequency of 12.5 Hz. If the MARK latch is changed to a constant of 002 hex, then TFSK will equal 25 Hz. The largest constant that can be loaded into the MARK register is 32,767, and the resulting output signal is approximately 409,587 Hz. Thus, this synthesizer may be set to any frequency between 12.5 Hz and 409,600 Hz in steps of 12.5 Hz.

At low frequencies or when the constant is an exact divisor of 819,200, the output waveform on TFSK (U17-19) is nearly a 50% duty cycle square wave. However, if the constant is not an integer divisor, the relationship between the constant and CKREF generates signal jitter. While this jitter is visible on an oscilloscope, the resulting sine wave output is smoothed by the sine wave approximation process and the 50 times over sampling.

In the ST-8000A the tone synthesizer generates output frequencies on TFSK of 15,000 Hz and 150,000 Hz in steps of 25 Hz. The resulting output from the AFSK generator on the modem card is 300 to 3000 Hz in 0.5 Hz increments. For each tone frequency, the constant loaded into the MARK and SPACE register is calculated using the following formulae:

MARK AFSK TONE CONSTANT = MARK TONE FREQUENCY * 4
SPACE AFSK TONE CONSTANT = SPACE TONE FREQUENCY * 4

For example, to transmit a MARK tone of 2125 Hz and a SPACE tone of 2295 Hz, the MARK constant is 8,500 and the SPACE constant is 9,180. The

lowest tone constant is 1,200 for 300 Hz, and the highest is 12,000 for 3000 Hz.

4.3.8 MARK Filter Synthesizer

The MARK filter synthesizer is illustrated in Figure A1812. This synthesizer generates the clock, MCLK (U19-19), used to set the center frequency of the MARK bandpass filter on the modem board (J7-1). The operation of this synthesizer is identical to the transmit tone synthesizer described in the previous section, and the output of this synthesizer is 50 times the selected MARK frequency.

The MARK filter constant is loaded into two octal D-type latches (U45, U46). The output frequency of the MARK filter synthesizer is calculated using the following formula:

MARK FILTER CONSTANT = MARK TONE FREQUENCY * 4

4.3.9 SPACE Filter Synthesizer

The SPACE filter synthesizer is illustrated in Figure A1813. This synthesizer generates the clock, SCLK (U21-19), used to set the center frequency of the SPACE bandpass filter on the modem board (J7-3). The operation of this synthesizer is identical to the transmit tone synthesizer described in the previous section, and the output of this synthesizer is 50 times the selected SPACE frequency.

The SPACE filter constant is loaded into two octal D-type latches (U49, U50). The output frequency of the SPACE filter synthesizer is calculated using the following formula:

SPACE FILTER CONSTANT = SPACE TONE FREQUENCY * 4

4.3.10 HIGH SPEED Filter Synthesizer

The HIGH SPEED filter synthesizer is illustrated in Figure A1814. This synthesizer generates the clock, HSCLK (U23-19), used to set the center frequency of the HIGH SPEED bandpass filter on the modem board (J7-7). The operation of this synthesizer is identical to the transmit tone synthesizer described in the previous section, except that the output of this synthesizer is set to the center frequency of the HIGH SPEED filter plus 10,000 Hz.

The HIGH SPEED filter constant is loaded into two octal D-type latches (U52, U53). The output frequency of the HIGH SPEED filter synthesizer is calculated using the following formula:

HIGH SPEED FILTER CONSTANT = (CENTER FREQUENCY + 10,000) / 12.5

4.3.11 LOW PASS Filter Oscillator

The LOW PASS filter oscillator controls the corner frequency of the low pass filter in the detector of the modem board. The programmable timer (U1) in Figure A1807 generates this clock signal, LPCLK (U1-13), and it

is passed to the filter on the modem board (J7-5). This oscillator is simply a 16 bit counter with a clock reference frequency of 4.9152 MHz. The 16 bit constant is loaded into the programmable timer.

For a given data rate, the LOW PASS filter constant is calculated using the following formula:

LOW PASS CONSTANT = (4,915,200) / (96 * DATA RATE)

This constant varies between 5,120 for 10 bits per second to 43 for 1200 bps.

4.3.12 Regeneration

Figure A1815 illustrates the serial channel controller (U66) used for receive data regeneration and the remote control port. This controller has an internal baud rate clock that sets the data rate for both channels.

When regeneration is active (REGEN = 1) asynchronous characters received on the RXDB (U66-27) input of the serial controller are passed to the TXDB (U66-25) output. Regeneration generates each receive character removing any received jitter and noise. Note that regeneration is only possible when receiving asynchronous start-stop characters with character lengths of 5 to 8 data bits.

The serial controller operates in an interrupt driven mode during regeneration. Any character received on the RSCB (U66-27) input causes INT_L (U66-5) to go low signaling a data available interrupt. The microprocessor controller reads the serial controller to clear this interrupt flag.

Note that regeneration can only work properly when the data presented to the RXDB (U66-27) input has polarity set such that a MARK equals TTL high and SPACE equals TTL low. This should be the case when the MARK tone is set for the correct tone and the receive data normal/reverse, RXDNR (U57-1), are set correctly for the desired signal. The regenerated signal on RXDFR (U63-11) will have MARK high and SPACE low independent of the RXDNR setting.

Whether regeneration is enabled or not, a data rate clock equal to 16 times the baud rate is generated on the TXCLK (U66-26) output of the serial controller. This clock provides a time reference signal for the clock recovery circuit described in the next section. The frequency of this clock is set by the BAUD RATE setting on the front panel; it is set to 16 times that rate.

4.3.13 Remote Control Port

The dual channel serial controller (U66) channel A is connected to the Remote Control port on the ST-8000A. In Figure A1815, note that the polarity of the data on this port may be set to RS232 or MIL188 levels with the jumper J5. When in the RS232 position, J5SW low, the port has normal RS-232 MARK and SPACE control levels.

The remote port REMRXD is converted to TTL level (U59-6) and passed to the RXDA input on the serial controller (U66-13) after passing through the RS232/MIL188 polarity gate. The ST-8000A may read the Clear to Send, REMCTS (U59-8), to control output flow control.

The remote port REMTXD signal comes from the TXDB (U66-15) output of the serial controller and the RS232/MIL188 polarity gate. The REMTXD signal is combined with the RTSA (U66-17) serial controller output so that this signal is held in the MARK hold state when RTSA is low. Note that the RTSA output drives the REMRTS (U62-8) signal on the remote control port. In addition, a REMDTR (U62-11) and REMCTS (U62-6) signals are provided.

The remote port is configured as a mult-drop output where up to 8 ST-8000A remote port transmit data outputs, REMTXD, may be connected in parallel. Diodes D2 and D3 in Figure A1815 actively pull REMTXD to MARK and SPACE levels when RTSA (U66-17) is low or enabled, and allow the REMTXD to float when RTSA is high. Thus, the output data line is connected only when this unit has a response to transmit. The zener diodes D1 and D4 limit the REMTXD output voltage swing to MIL188 levels. To improve noise immunity on the common transmit data output line, REMTXD, one and only one ST-8000A in a group of 2 or more units should have jumper J3 set to connect the resistor to the output line. This resistor defaults the line to a MARK or negative voltage level when no unit is actively sending.

4.3.14 Synchronous Data Clocks

Figure A1816 illustrates the receive data clock, RXCLK (U60-11), recovery circuit for serial data received by the modem board. Basically, this circuit synchronizes an internal clock to the edges in the serial receive data, RXDTR (U57-2), from the modem card.

Changes in the receive data signal generate pulses (U57-11) that reset a 4 bit counter (U58) each time a change occurs. This counter is driven by a clock running at 16 times the baud rate, TXCLKB (U58-1), and the output of the most significant bit of the counter (U58-6) will change after 8 TXCLKB cycles. If this clock is properly set, the clock transition occurs at the center of the data bit and a correct receive data recovered clock, RXCLK (U60-11), is generated. Jumper J4 selects either normal or inverted clock for RS232 or MIL188 receive data.

A D-type latch is driven by the recovered clock (U55-3) to re-clock the receive data (U55-5). In some cases, re-clocking the data will reduce receive data jitter and improve system performance. Note that the receive data re-clocking latch will work with either synchronous or asynchronous receive data since it does not depend on a start or stop bit, nor does data polarity matter.

The baud rate clock TXCLKB (U58-1) is simply divided by 16 in a four bit counter (U58) to generate the TXCLK (U60-3) synchronous transmit clock. Since the transmit data input, TXDIN (U59-1), directly drives the tone generator, there is no need to change this clock phase for RS232 and MIL188 data. The ST-8000A transmits correctly in either case.